NOTE

This manual documents the Model 9000A-8051 and its assemblies at the revision levels identified in Section 7. If your instrument contains assemblies with different revision letters, it will be necessary for you to either update or backdate this manual. Refer to the supplemental change/errata sheet for newer assemblies, or to the backdating information in Section 7 for older assemblies.

9000A-8051
Interface Pod

Instruction Manual

P/N 744698
OCTOBER 1984

FLUKE®

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Section 1
Introduction

NOTE

It is assumed that the user of this manual is familiar with the basic operation of one of the 9000 Series Micro System Troubleshooters as described in the 9000 Series Operator manuals.

PURPOSE OF INTERFACE POD 1-1.

The 9000A-8051 Interface Pod interfaces any 9000 Series Micro System Troubleshooter to equipment using an 8051- or 8044-family microprocessor.

The Micro System Troubleshooter (referred to hereafter as the Troubleshooter) is used to service printed circuit boards, instruments and systems that use a microprocessor. The 9000A-8051 Interface Pod (referred to as the Pod) adapts the general purpose architecture of the Troubleshooter to a specific architecture of the 8051 and 8044 microprocessor families. The Pod adapts such microprocessor-specific functions as pin layout, status/control functions, interrupt handling, timing, and memory and I/O addressing.

DESCRIPTION OF POD 1-2.

Figure 1-1 shows the communication between the Pod, the Troubleshooter, and the unit-under-test (referred to as the UUT). The Pod connects to the Troubleshooter through a shielded 24-conductor cable. The Pod connects to the UUT through the microprocessor socket. The UUTs microprocessor is removed from the UUT and is replaced by the Pod ribbon cable plug, which gives the Troubleshooter access to all system components which normally communicate with the microprocessor. A microprocessor of the same type that was removed from the UUT is inserted into the socket located under the sliding door on the top of the Pod. Eight configuration switches, also located under the sliding cover, must be set to configure the Pod to the specific UUT being used.

The external features of the Pod are shown in Figure 1-2.

The Pod consists of a pair of printed circuit board assemblies mounted within a break-resistant case. The Pod contains a microprocessor along with the supporting hardware and control software that is required to do the following:

1. Perform handshaking with the Troubleshooter.
2. Receive and execute commands from the Troubleshooter.
3. Report UUT status to the Troubleshooter.
4. Allow the UUTs microprocessor to operate with the UUT.

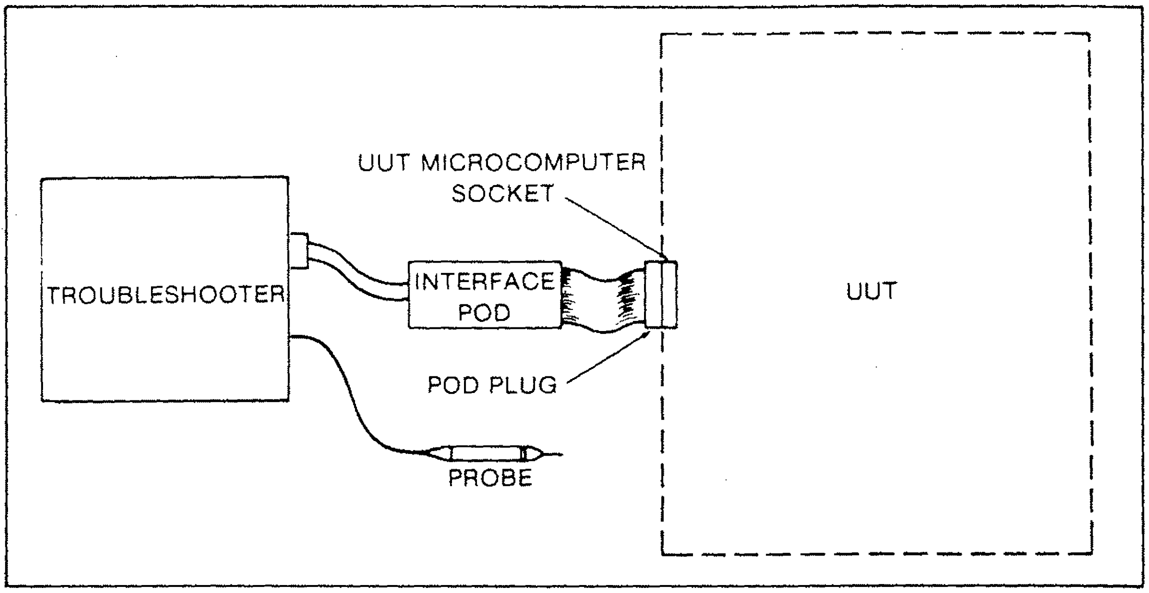

Figure 1-1. Communication Between the Troubleshooter, the Pod, and the UUT.

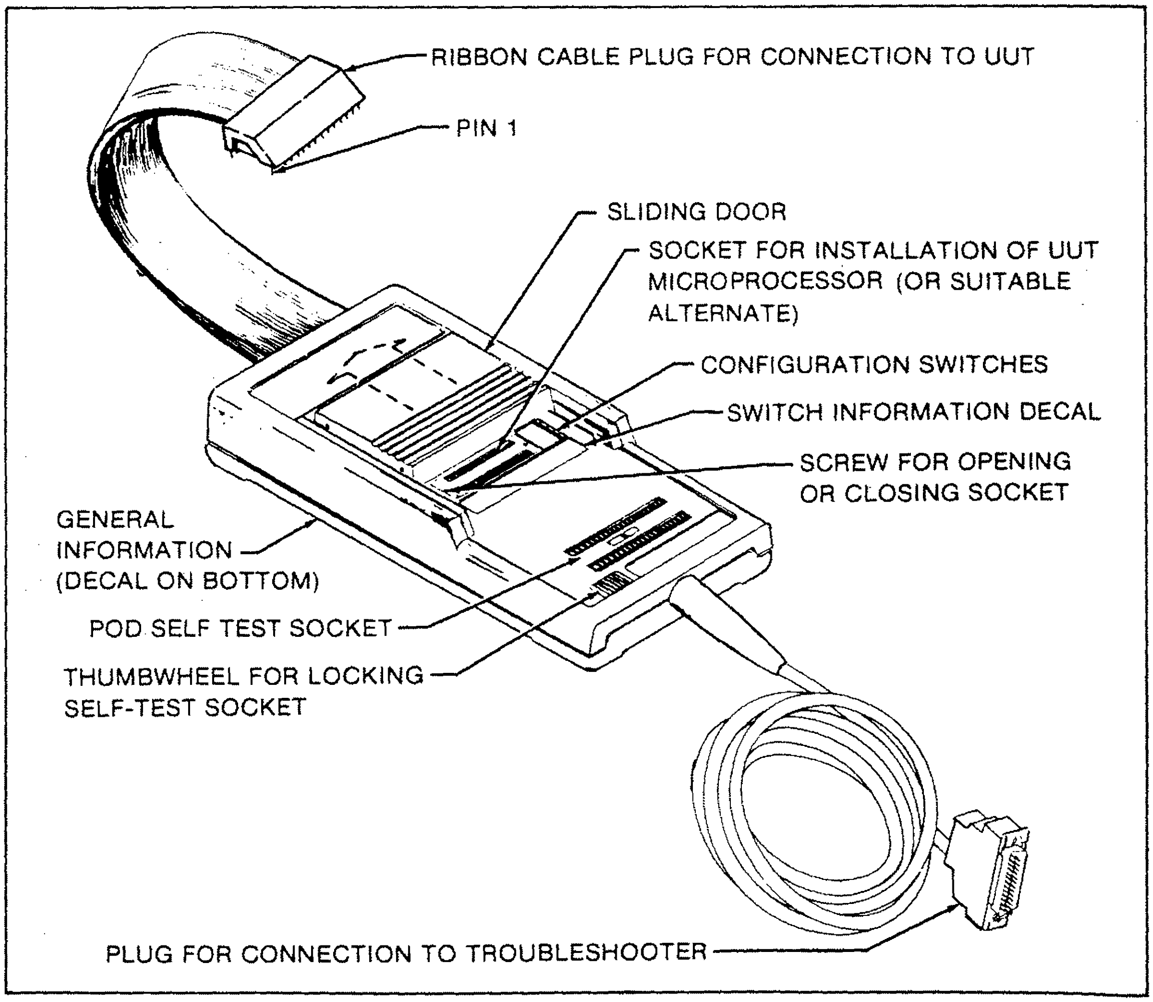
RIBBON CABLE PLUG FOR CONNECTION TO UUT
PIN 1
SLIDING DOOR
SOCKET FOR INSTALLATION OF UUT MICROPROCESSOR (OR SUITABLE ALTERNATE)
CONFIGURATION SWITCHES
SWITCH INFORMATION DECAL
SCREW FOR OPENING OR CLOSING SOCKET
GENERAL INFORMATION (DECAL ON BOTTOM)
POD SELF TEST SOCKET
THUMBWHEEL FOR LOCKING SELF-TEST SOCKET
PLUG FOR CONNECTION TO TROUBLESHOOTER

Figure 1-2. External Features of the 8051 Interface Pod.

The Troubleshooter supplies operating power for the Pod. The UUT provides the external clock signal required by the Pod for operation. Using the UUT clock signal allows the Troubleshooter and Pod to function at the designed operating speed of the UUT.

Logic level detection circuits are provided on each line to the UUT to detect bus shorts, stuck-high or stuck-low conditions, and any bus drive conflict (two or more drivers attempting to drive the same bus line).

Over-voltage protection circuits are also provided on each line to the UUT. These circuits guard against Pod damage which could result from the following:

1. Incorrectly inserting the ribbon cable plug in the UUT microprocessor socket.
2. UUT faults which place potentially-damaging voltages on the UUT microprocessor socket.

Over-voltage protection circuits guard against voltages of +12 to -7 volts on any one pin. Multiple faults, especially of long duration, may cause Pod damage.

A power level sensing circuit constantly monitors the voltage level of the UUT power supply. If UUT power rises above or drops below an acceptable level the Pod notifies the Troubleshooter of the power-fail condition.

A self-test socket on the Pod enables the Troubleshooter to check Pod operation. The self-test socket is a 40-pin zero-insertion-force type socket. The ribbon-cable plug is connected to the self-test socket during self-test operation. The ribbon-cable plug should also be inserted into this socket when the Pod is not in use to provide protection for the plug pins.

SPECIFICATIONS 1-3.

Specifications for the Pod are listed in Table 1-1.

Table 1-1. 9000A-8051 Pod Specifications

ELECTRICAL PERFORMANCE	
Power Dissipation	6 watts max.
Maximum External Voltage	-7V to +12V may be applied between ground and any ribbon cable plug pin continuously.
MICROPROCESSOR SIGNALS*	
Input Low Voltage	-0.3V min., 0.8V max.
Input High Voltage	2.0V min., 5.0V max.
Output Low Voltage	0.5V max. at rated current
Output High Voltage	2.4V min. at -400 μa
Tristate Output Leakage Current	+-0.02 mA typical, +0.1 to -0.2 mA max.
Input Current	
I_{IH} (RST)	500 μA max.
I_{IH}	40 μA max.
I_{IL}	-800 μA max.

Table 1-1. 9000A-8051 Pod Specifications (cont)

TIMING CHARACTERISTICS *	
Maximum External Clock Frequency	12.0 MHz
Insertion Delays to 8051 Signals	
Input signals	12 ns typical
Output signals	
Low Addr, ALE, $\overline{\text{PSEN}}$, data	15 ns typical
High Addr, $\overline{\text{RD}}$, $\overline{\text{WR}}$	20 ns typical
UUT POWER DETECTION	
Detection of Low Vcc Fault	Vcc< +4.5V
Detection of High Vcc Fault	Vcc> +5.5V
**Pod protection from UUT Low Power	Vcc< +3.5V
GENERAL	
Size	5.7 cm H x 14.5 cm W x 27.1 cm L (2.2 in H x 5.7 in W x 10.7 in L)
Weight	1.5 kg (3.3 lbs)
Environment	-40° C to +70° C, RH < 95% non-condensing
STORAGE	0° C to +40° C, RH < 95% non-condensing
OPERATING	+40° C to +50° C, RH < 75% non-condensing

* Signals are specified as they appear at the ribbon cable plug pins

** Pod outputs set to high-impedance or high logic level.

COMPATIBLE MICROPROCESSORS 1-4.

The 8044- and 8051-family microprocessors that can be used with the 9000A-8051 Pod are listed in Table 1-2. The Pod will work with all family members, with the following operating restrictions:

- The programming modes of the EPROM versions, the 8751 and the 8744, are not supported. The Pod only tests UUTs in the normal operating modes.

- Microprocessors with internal ROM or EPROM that have the security bit set will not execute instructions from external memory, which is needed to perform all Troubleshooter functions. A special version of the programmed microprocessor, without the security bit set, must be used if the RUN UUT function is needed. Otherwise, all testing should be done using the 8031 microprocessor that is shipped with the Pod.

Table 1-2. Products Supported by the 9000A-8051 Interface Pod

8051 FAMILY	8044 FAMILY
8031*	8344
8032	
8051*	8044
8052	
8751	8744

*Including 80C31 and 80C51

Section 2
Installation and Self Test

INTRODUCTION 2-1.

The procedures for connecting the Pod to the Troubleshooter and the UUT, for setting the Mode Switches on the top of the Pod, and for performing the Pod Self Test are given in the following paragraphs.

INSTALLING A MICROPROCESSOR INTO THE POD 2-2.

A microprocessor must be installed in the Pod before using it to test a UUT.

NOTE

An 8031 microprocessor rated for 12 MHz operation is supplied with the Pod. You will need to replace it if your application requires a different microprocessor, or if your UUT uses internal ROM.

The Pod socket is not designed for repeated insertions. It is not meant to test a new microprocessor with each tested UUT.

To install a microprocessor in the Pod, perform the following steps:

1. If the Pod is already connected, remove power from the UUT and the Troubleshooter.

2. Select a microprocessor to use in the Pod, either one out of the UUT, or another of the same type.

3. Open the sliding door on the top of the Pod (shown in Figure 2-1) to expose the microprocessor socket. Open the Pod socket by using a screwdriver to turn the screw at the end of the socket. Turn the screw counterclockwise to open the socket. Insert the microprocessor into the socket, aligning pin 1 to the marked position. Turn the screw clockwise to close the socket.

4. Set the configuration switches to the required mode as described below under Configuration. Close the sliding door.

CONNECTING THE POD TO THE UUT 2-3.

The 8044- and 8051-families of microprocessors offer a wide variety of operating modes. The Pod must be configured by the operator to match some of these modes prior to testing.

There are eight configuration switches, located on the top of the Pod under the sliding cover (see Figure 2-1). Table 2-1 and a label on the Pod show the switch positions. A brief description of each switch function follows:

- Switch 1, the Port 0 Mode switch, specifies whether the microprocessor's port 0 is used as an I/O port or as a multiplexed address/data bus.
- Switch 2, the Port 2 Mode switch, specifies whether the microprocessor's port 2 is used as an I/O port or as the upper byte of the address bus.
- Switches 3 and 4 are the Port 3 Mode switches. Switch 3 specifies that bit 2 of port 3 is used either as an I/O port or as an interrupt input ($\overline{\text{INT0}}$). Switch 4 specifies that bit 3 will be either an I/O port or an interrupt input ($\overline{\text{INT1}}$).
- Switch 5 specifies that bits 6 and 7 of Port 3 will be either I/O port lines or the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ lines respectively.
- Switch 6, the UUT Connection switch, selects whether the UUT will be tested with the Pod plug inserted into the microprocessor socket or with the Pod plug attached to the microprocessor via a clip-on connector (as would be necessary with a soldered-in micro-processor). When set to the Clip-On position, the Pod will attempt to pull the RST line high to hold the microprocessor in a Reset condition during testing.

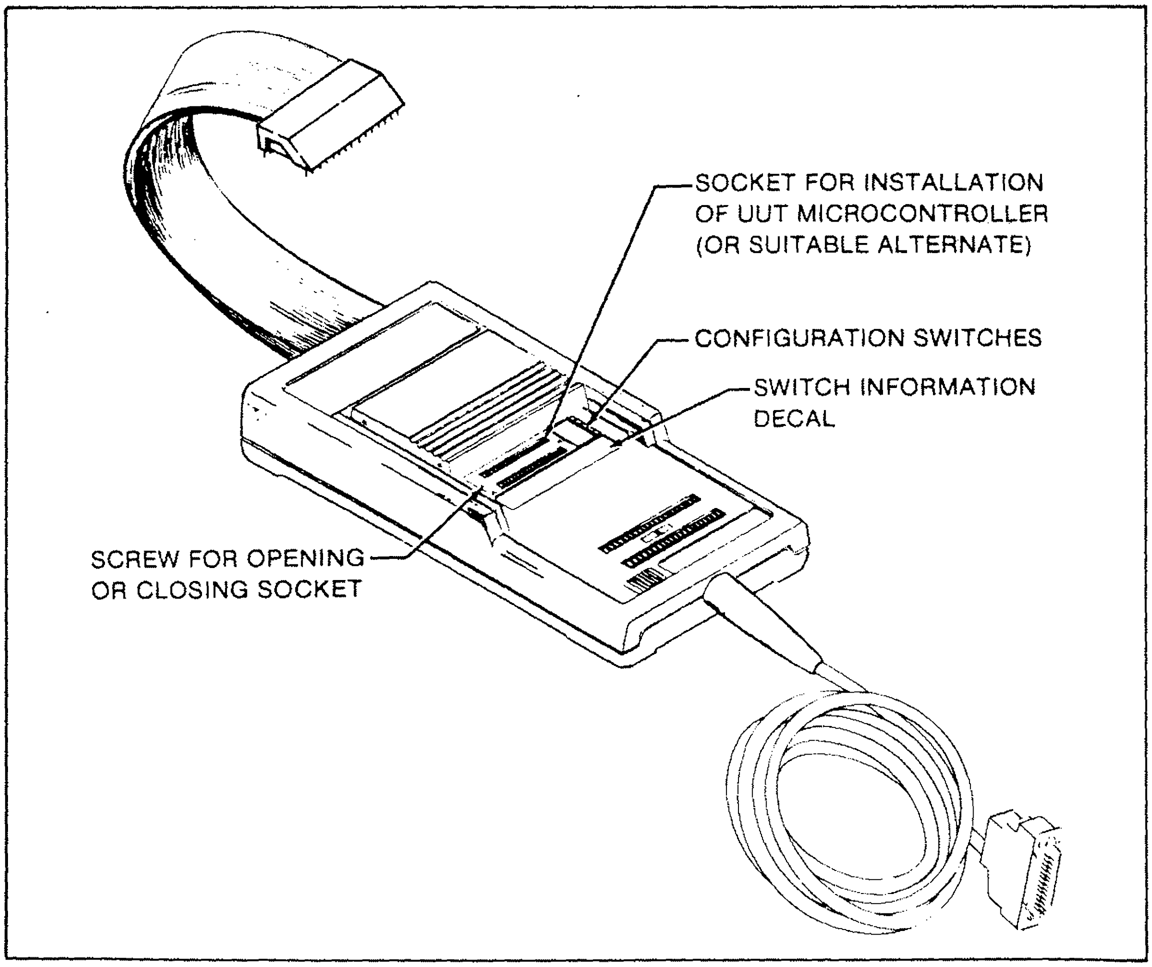

Figure 2-1. Location of Microcontroller Socket and Configuration Switches

Table 2-1. Mode Switch Settings

SWITCH FUNCTION	◢	◣
1 Port 0	I/O	Addr/Data
2 Port 2	I/O	Address
3 P3.2	I/O	$\overline{\text{INT0}}$
4 P3.3	I/O	$\overline{\text{INT1}}$
5 P3.6 and P3.7	I/O	$\overline{\text{WR}}$ and $\overline{\text{RD}}$
6 UUT Connection	Socket	Clip-on
7 Clk Source	Xtal	TTL
8 External Clock	Xtal1	Xtal2

- Switch 7, the Clock Source switch, selects between a TTL clock source and a crystal clock source.
- Switch 8, the External Clock switch. When a TTL clock source is specified by switch 7, this switch is set to specify to which input the clock source will be applied.

Switches 1 through 5 may be overridden by commands from the Troubleshooter. Refer to Special Functions of the 8051 Pod in Section 4 for a description of the Special Addresses which may be used to override the switch positions.

PERFORMING THE POD SELF TEST 2-4.

In order to perform the Pod self test, do the following steps:

1. Remove power from the UUT and the Troubleshooter.
2. Use the thumbwheel to open the pins of the Pod self test socket. Insert the ribbon-cable plug into the socket and use the thumbwheel to close the socket.
3. If it is not already connected, use the round shielded cable to connect the Pod to the Troubleshooter at the location shown in Figure 2-2. Secure the connector using the sliding collar.

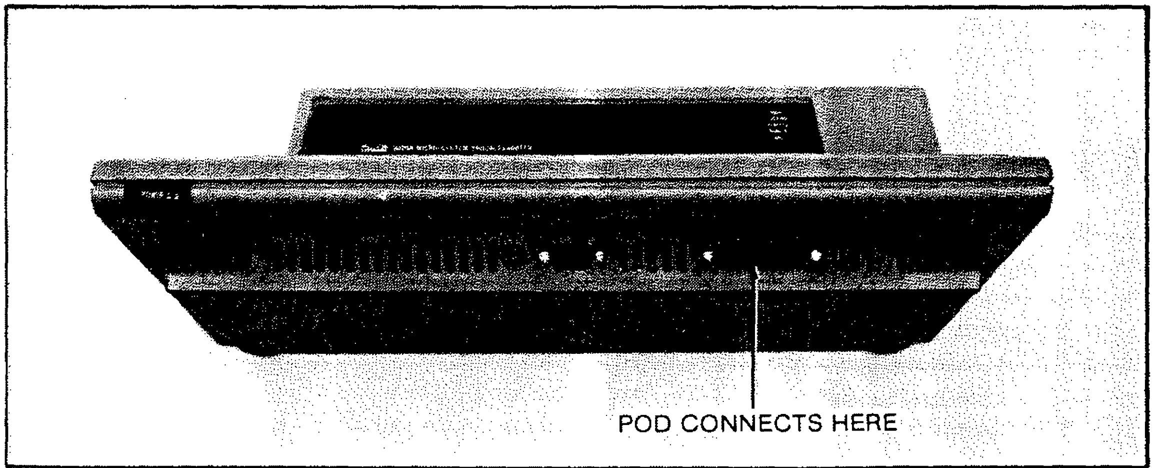

Figure 2-2. Connection of Interface Pod to Troubleshooter

4. Apply power to the Troubleshooter.

5. Press the BUS TEST key to initiate the Pod self test.

If the Troubleshooter displays the message *POD SELF TEST 80xx OK*, then the Pod is operating properly.

NOTE

The Pod name that is displayed in the self test message corresponds to the mode as determined by the switches on the top of the Pod. It is not effected by the type of processor that in contained in the Pod at the time.

If the Troubleshooter displays the message *POD SELF TEST 80xx FAIL xx*, the Pod may not be operating properly. (The letters xx correspond to a failure code describing the error; the failure codes are listed in Section 6.) If the UUT microprocessor has been installed in the Pod, the UUT microprocessor may be causing the failure. Replace the UUT microprocessor with a suitable alternate and try the self test again. Make sure the microprocessor is properly positioned in the microprocessor socket before trying the test.

For information about Pod troubleshooting and repair, refer to Section 6.

INITIALIZATION 2-5.

When power is applied to the Pod, it sends certain default information to the Troubleshooter, some of which is based on settings of the Configuration switches described above. Most of the information is used to set up the Troubleshooter for this particular Pod, such as the width of the data bus and names of enablable lines. The Configuration switches for Port 0, Port 2, and Port 3 determine what external memory will be used by default with the Troubleshooter's Learn function. Table 2-2 shows the switch settings and the resultant default external Address Blocks and BUS TEST Address.

Table 2-2. Learnable External Address Blocks

CONFIGURATION SWITCHES			LEARNABLE EXTERNAL ADDRESS BLOCKS ENABLED	BUSTEST ADDRESS	NAME DISPLAY
P0	P2	P3.6&3.7			
I/O	x	x	None	30000	8051
A/D	A	x	0000 0000 through 0000 FFFF	--	--
A/D	A	$\overline{RD}/\overline{WR}$	0001 0000 through 0001 FFFF	10000	8031
A/D	x	$\overline{RD}/\overline{WR}$	0002 0000 through 0002 00FF	20000	8051X

A/D = Address/Data
A = Address
x = Don't care

Section 3
Microprocessor Data

INTRODUCTION 3-1.

This section contains microprocessor data which may be useful during operation of the Troubleshooter. This information includes descriptions of 8044- and 8051-family signals and pin assignments.

MICROPROCESSOR SIGNALS 3-2.

Table 3-1 lists all of the 8044- and 8051-family microprocessor signals and provides a brief description of each signal. Refer to the microprocessor manufacturer's literature for complete information.

Figure 3-1 shows the 8044- and 8051-family pin assignments.

Table 3-1. Signal Descriptions

SIGNAL NAME	DESCRIPTION
ALE/$\overline{\text{PROG}}$	Address Latch Enable/Program. Latches addresses into external memory. The Program pulse for programming microprocessors with internal EPROM is applied to this pin. The Pod does not test microprocessors in the program mode.
$\overline{\text{EA}}$/VPP	When $\overline{\text{EA}}$/VPP is low, all instructions come from External Addresses. When high, some addresses (less than 0FFF in the 8051 series and less than 1FFF in the 8052 series) execute from internal ROM. Also receives the programming pulse for EPROM versions of the microprocessor. The Pod does not test microprocessors in the program mode.
PORT 0 (P0.0-P0.7)	Port 0 is an eight-bit, open-drain I/O port. When using external memory, it is multiplexed between low-order address and data. During program verification, Port 0 is used for data output. The Pod does not test microprocessors in the program mode.

Table 3-1. Signal Descriptions (cont)

SIGNAL NAME	DESCRIPTION
PORT 1 (P1.0-P1.7)	Port 1 is an eight-bit I/O port. Two of Port 1's pins are used for secondary purposes in some microprocessors as described below.
T2 (P1.0)	Trigger input to timer 2. (8032 and 8052 only.)
T2EX (P1.1)	External input to timer 2. (8032 and 8052 only.)
$\overline{RTS}$ (P1.6)	Request To Send signals that the microprocessor is ready to transmit data (in a non-looping configuration). (8044 family.)
$\overline{CTS}$ (P1.7)	Clear To Send signals to the microprocessor that the receiving station is ready to send data (in a non-looping configuration). (8044 family.)
	Port 1 is also used as the low-order addresses during program verification. The Pod does not test microprocessors in the program mode.
PORT 2 (P2.0-P2.7)	Port 2 is an eight-bit I/O port that is used for high-order addresses when using external memory, and high-order addresses and control information during program verification.
PORT 3 (P3.0-P3.7)	Port 3 is an eight-bit I/O port. Pins assigned to Port 3 also have secondary functions as described below.
RXD (P3.0) I/$\overline{O}$	RXD is the serial port's receiver data input during asynchronous communications, and its data input/output during synchronous communications (8051 family). Also functions as the data direction control in non-looping configurations (8044 family).
TXD (P3.1) DATA	TXD is the serial port's transmitter data output during asynchronous communications, and its clock output during synchronous communications (8051 family). Also functions as the data input/output in non-looping configurations (8044 family).
$\overline{INT0}$ (P3.2)	$\overline{INT0}$ is the interrupt 0 input or the gate control input for counter 0.
$\overline{INT1}$ (P3.3)	$\overline{INT1}$ is the interrupt 1 input or the gate control input for counter 1.
T0 (P3.4)	T0 is the input to counter 0.
T1 (P3.5)	T1 is the input to counter 1.
$\overline{WR}$ (P3.6)	$\overline{WR}$ (Write Control) latches the data from Port 0 into external memory.
$\overline{RD}$ (P3.7)	$\overline{RD}$ (Read Control) enables external data memory for Port 0.
$\overline{PSEN}$	Program Store Enable enables external Program Memory on the bus. $\overline{PSEN}$ is high during internal operation.
RST	The Reset signal. A high on this line resets the microprocessor.

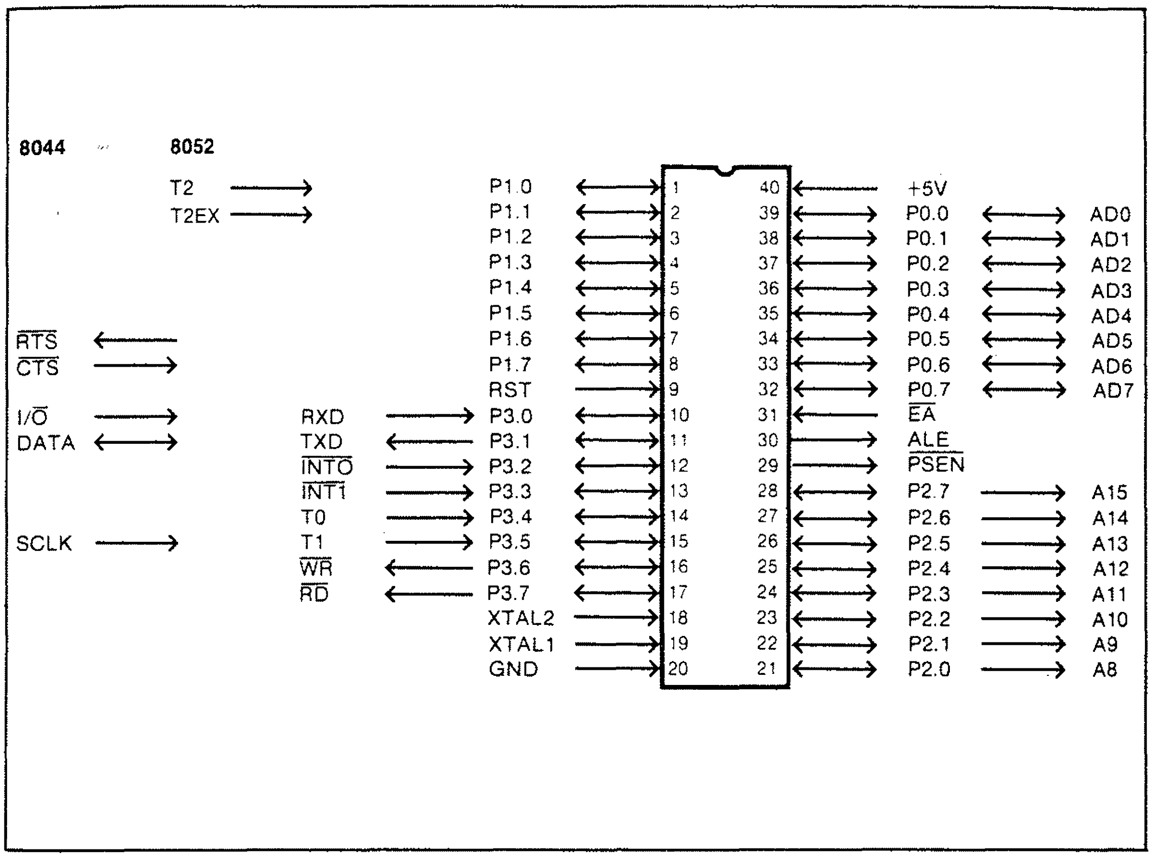

Figure 3-1. 8044 and 8051 Family Pin Assignments

Section 4
Operating Information

INTRODUCTION 4-1.

This section contains information which pertains to operating the Troubleshooter with systems employing the 8044- or 8051-microprocessor families. Information provided is in addition to and complements that provided in the Troubleshooter Operator and Programming manuals, and covers such items as the following:

- Definition and bit assignment of status lines.
- Definition of forcing and interrupt lines.
- Bit assignment of control lines.
- Address space assignment.
- Access to program memory, RAM, registers, and ports.
- Characteristics of Learn and Bus Test operations.
- Marginal UUT problems.
- Quick-Looping Read and Write functions.
- The Quick RAM test.
- The Quick ROM test.
- The Block Memory tests.

STATUS/CONTROL LINES 4-2.

Introduction 4-3.

The Pod provides the interface between the general architecture of the Troubleshooter and the specific features of the microprocessor. Part of this task is assigning the status and control lines to a consistent bit map to be used in status messages and read/write operations.

These assignments are described in the following paragraphs, and are summarized in Tables 4-1 and 4-2 and on a decal on the bottom of the Pod.

Table 4-1. Status Line Bit Assignments

BIT	8051 INPUT	DESCRIPTION
7	PWR FAIL	UUT Power Fail
6 *	MPU FAIL	UUT Processor RAM Fail
5	$\overline{\text{EA}}$	External Address Line
4 *	RST	Reset Line
3 **	$\overline{\text{INT0}}$ (P3.2)	Interrupt 0 Line
2 **	$\overline{\text{INT1}}$ (P3.3)	Interrupt 1 Line
1	-	
0	-	

* Forcing Line
** Defined by DIP Switch Setting

Table 4-2. Control Line Bit Assignments

BIT	8051 OUTPUT	DESCRIPTION
7	$\overline{\text{PSEN}}$	Program Store Enable
6	-	
5 **	$\overline{\text{WR}}$ (P3.6)	External Data Write
4 **	$\overline{\text{RD}}$ (P3.7)	External Data Read
3	-	
2	-	
1	-	
0	ALE	Address Latch Enable

** Defined by DIP Switch Setting

Status Line Bit Assignments 4-4.

The bits assigned to the specific status lines are shown in Table 4-1 and on the decal on the back of the Pod. A Read Status operation reads the actual levels on the pins or bits. However an active forcing line is reported as a high bit, regardless of its actual logic level. For example, if the Reset line is active (high), an active Reset is reported as *ACTIVE FORCE LINE, STS BTS 0001 0000*. An $\overline{\text{INT0}}$ interrupt (pin 12, active low), on the other hand, if the Troubleshooter's active interrupt trap is enabled, is reported as *ACTIVE INTERRUPT, STS BTS 0000 1000*, but a Read Status operation will report XXXX 0100.

NOTE

The Power Fail and Microprocessor Fail bits do not represent particular 8044 or 8051 signals. PWR FAIL is generated within the Pod whenever UUT voltage levels deviate from acceptable limits. MPU FAIL is generated whenever the microprocessor's internal RAM fails a RAM test which is conducted during every Pod reset cycle. MPU FAIL remains in effect until cleared by a successful Pod Reset.

Control Line Bit Assignments 4-5.

The Pod does not allow the Troubleshooter to write directly to any of the microprocessor control lines with the Write Control or Data Toggle Control functions. However, all 8044 and 8051 control lines are tested by means of the Troubleshooter Bus Test.

If a control line cannot be driven when performing a Bus Test, the Troubleshooter displays the message *CTL ERR XXXXXXXX-LOOP?* The string *XXXXXXXX* represents a binary map that identifies which lines can or cannot be driven. A 1 indicates the corresponding line cannot be driven, while a 0 indicates the corresponding line can be driven. Control line bit assignments are shown in Table 4-2 and on the decal on the back of the Pod.

For example, if the $\overline{\text{PSEN}}$ line of an 8051 cannot be driven, but all other control lines can be driven, the Troubleshooter displays the message *CTL ERR 10000000 LOOP?* (the $\overline{\text{PSEN}}$ line is represented by bit number 7).

FORCING AND INTERRUPT LINES 4-6.

Several Troubleshooter messages are used to indicate errors and conditions associated with forcing lines and interrupts. Forcing lines are those lines which, when active, force the microprocessor into some specific action. Forcing lines for the 8044- and 8051-family are RST and MPU FAIL.

The RST and interrupt lines are functionally enabled only when the Troubleshooter is operated in the RUN UUT mode (where the Pod emulates the UUT microprocessor). In all other operating modes, the Troubleshooter monitors the status lines and, when active, causes active forcing or interrupt line messages to appear on the Troubleshooter display.

NOTE

The RST line is active high. The interrupt lines are active low.

MPU FAIL denotes a failed test on the microprocessor's internal RAM. The RAM is tested during each Pod Reset cycle, and failures are reported as a forcing line error. Microprocessor RAM failures are most likely due to a defective microprocessor. When a MPU FAIL forcing line error is reported, try to correct the error by substituting the microprocessor that is plugged into the Pod's microprocessor socket for a known-good device. If a MPU FAIL forcing line error persists, refer to Troubleshooting a Defective Pod in Section 6.

The reporting of active forcing lines or active interrupt lines may be disabled with the Setup operation on the Troubleshooter. If the Reset line is driven high but the *TRAP ACTIVE FORCE LINE* is disabled, for example, the Pod reports such a condition to the Troubleshooter, but the Troubleshooter does not report the condition to the operator.

ADDRESS SPACE ASSIGNMENT 4-7.

Introduction 4-8.

The 8044- and 8051-family microprocessors are capable of addressing some or all of the memory and I/O functions listed and described briefly in Table 4-3. Additional information about access to the various address space is provided below. Address space assignments are summarized in Table 4-3.

Table 4-3. Address Space Assignments

LOWER ADDRESS	UPPER ADDRESS	DESCRIPTION OF SPACE
00 0000	00 FFFF	External program memory
01 0000	01 FFFF	External data memory (16-bit address)
02 0000	02 00FF	External data memory (8-bit address)
03 0000	03 00FF	Internal data RAM
04 0080	04 00FF	Internal Special Function Registers
05 0000	05 00FF	Int. bit (flags & spcl func) addresses
06 0000	06 FFFF	Internal program ROM
07 0000	07 FFFF	* Pod's program ROM
08 0000	08 FFFF	* Pod's external read/write space
09 0000	09 00FF	* Pod's variable RAM (int. to processor)
10 0000	10 FFFF	Quick looping ext. program ROM
11 0000	11 FFFF	Quick looping ext. RAM (16-bit address)
12 0000	12 00FF	Quick looping ext. RAM (8-bit addresss)
2X 0000	2X XXXX	Quick RAM test
3X 0000	3X XXXX	Quick ROM test
4X 0000	4X XXXX	Block write and verify
F0 0000	F0 00XX	Special Addresses

* Enabled only when self test bit is disabled, for troubleshooting Pod.

External Memory 4-9.

The external program memory address space (00 0000 - 00 FFFF) is an address space that normally only consists of Read-Only Memory. Read operations in this space exercise the $\overline{\text{PSEN}}$ control line. An attempted Write operation in this address space will yield data drivability errors for all data lines.

The 64K byte RAM address space (01 0000 - 01 FFFF) is used for variable data and memory-mapped I/O devices. Read or write operations in this area will exercise the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ control lines. The high-order address is on Port 2.

The 256 byte RAM address space (02 000 - 02 00FF) is identical to the 64K byte space above, except that only the lower eight bits of the address are sent to the UUT. Port 2 is used for I/O data. For example, a *WRITE@ 1 7FFF=AA* is the same as writing Port 2 to 7F (*WRITE @ 4 00A0=7F*), and then a *WRITE @ 2 00FF=AA*. The only difference is that port 2 is in I/O mode rather than Address mode.

Internal RAM, Registers, and Stack 4-10.

The microprocessor's internal RAM address space (03 000 - 03 00FF) may be used to load the microprocessor's RAM prior to a RUN UUT command.

Read and write operations in the address range of 03 0000 to 03 007F actually use the Pod's RAM, instead of the RAM internal to the microprocessor. Read and write operations in the address range of 03 0080 to 03 00FF use the UUT microprocessor's internal RAM (although only the 8032 and 8052 contain RAM in those locations). All of the data in this 03 XXXX address space is copied into the microprocessor's internal RAM (if applicable) at the beginning of a RUN UUT command, and transferred back to the Pod's RAM when the RUN UUT terminates.

The internal Special Function Register address space (04 0080 - 04 00FF) contains special function registers for the microprocessor's internal peripheral devices, control, and status. Since writing to some of the registers in this address range might affect Pod operation, that data is set aside until a RUN UUT command is executed and then it is loaded into the correct special function register. Note too that only registers whose actions are harmless to the Pod are writable in this address range. The xx80 - xxFF addressing scheme corresponds to the standard 8044- and 8051-family addresses as defined by the microprocessor's manufacturer.

Table 4-4 contains a list of the special function registers.

The internal bit address space (05 0000 - 05 FFFF) contains bit addresses for special function registers, internal data RAM, and individual port lines. Bits addressed in this space are mapped into specific bits in the 04 0000 - 04 00FF address spaces according to the manufacturer's bit addressing scheme. As with the 04 00xx address range, only some bits are actually written during a Write operation. Others are deferred and written just prior to beginning a RUN UUT command.

NOTE

If a UUT has a port with both input and output pins, then the bit mode (5 XXXX addresses) should be used rather than the byte mode (4 XXXX). Then, only the bit addressed will be tested for drivablility.

Table 4-5 shows the addresses for individual port lines. Table 4-6 shows the special addresses and bit assignments for internal data.

Internal Program ROM 4-11.

The Internal Program ROM address space (06 0000 - 06 FFFF) makes use of an undocumented feature of the 8051 to provide access to the internal program data of the microprocessor. By pulling the $\overline{EA}$ line high, it allows the Pod to read the contents of the microprocessor ROM. It is provided for the convenience of those who can use it, but with the understanding that it might not always work. An attempted Write operation to this area will yield data drivability errors on all data lines.

Diagnostic Addresses 4-12.

The Pod's program ROM (07 0000 - 07 FFFF), the Pod external read/write space (08 0000 - 08 FFFF), and the Pod microprocessor's internal RAM (09 0000 - 09 00FF) are accessible when the self test is disabled for troubleshooting a defective Pod. Refer to Section 6, Troubleshooting, for detailed information about using these addresses.

Quick-Looping Test Addresses 4-13.

Addresses in the 10 0000 to 12 00FF range are the same as 00 0000 to 02 00FF, except that Read or Write commands repeat until another command is received. A system fault byte is sent after the first repetition of the operation, and sync pulses are generated on each repetition, if they are enabled.

Operations to addresses 10 0000 - 10 FFFF perform quick-looping functions on the UUT's external program ROM at 00 0000 through 00 FFFF.

Operations to addresses 11 0000 - 11 FFFF perform quick-looping functions on the UUT's external (16-bit address) data space at 01 0000 through 01 FFFF.

Operations to addresses 12 0000 - 12 00FF perform quick-looping functions on the UUT's external data space (8-bit address) at 02 0000 through 02 00FF.

Table 4-4. Special Function Registers

NAME	ADDRESS	ACTION
P0	04 0080	Port 0
SP	04 0081	+Stack Pointer
DPL	04 0082	+Data Pointer (Low Byte)
DPH	04 0083	+Data Pointer (High Byte)
PCON	04 0087	◇ +Power Control
TCON	04 0088	Timer/Counter Control
TMOD	04 0089	Timer/Counter Mode Control
TL0	04 008A	Timer/Counter 0 (Low Byte)
TL1	04 008B	Timer/Counter 1 (Low Byte)
TH0	04 008C	Timer/Counter 0 (High Byte)
TH1	04 008D	Timer/Counter 1 (High Byte)
P1	04 0090	Port 1
SCON	04 0098	Serial Control
SBUF	04 0099	Serial Data Buffer
P2	04 00A0	Port 2
IE	04 00A8	+Interrupt Enable Control
P3	04 00B0	Port 3
IP	04 00B8	Interrupt Priority Control
T2CON	04 00C8 *	Timer/Counter 2 Control
STS	04 00C8 **	Status/Command
SMD	04 00C9 **	Serial Mode
RCAP2L	04 00CA *	Timer/Counter 2 Capture Register (Low Byte)
RCB	04 00CA **	Received Control Byte
RCAP2H	04 00CB *	Timer/Counter 2 Capture Register (High Byte)
RBL	04 00CB **	Receive Buffer Length
TL2	04 00CC *	Timer/Counter 2 (Low Byte)
RBS	04 00CC **	Receive Buffer Start Address
TH2	04 00CD *	Timer/Counter 2 (High Byte)
RFL	04 00CD **	Received Field Length
STAD	04 00CE **	Station Address
DMACNT	04 00CF **	DMA Count
PSW	04 00D0	+Program Status Word
NSNR	04 00D8 **	Send/Receive Count
SIUST	04 00D9 **	SIU State Counter
TCB	04 00DA **	Transmit Control Byte
TBL	04 00DB **	Transmit Buffer Length
TBS	04 00DC **	Transmit Buffer Start Address
FIFO1	04 00DD **	FIFO (Byte 1)
FIFO2	04 00DE **	FIFO (Byte 2)
FIFO3	04 00DF **	FIFO (Byte 3)
ACC	04 00E0	+Accumulator (A Register)
B	04 00F0	B Register

* unique to 8052/8032

** unique to 8044/8344/8744

+ Data written to these registers is not actually entered into that register until a RUN UUT operation is performed.

◇ The PD (Powerdown) and IDL (Idle Mode) control bits may not be accessed from the Troubleshooter.

Table 4-5. Port Access Addresses

PORT	BYTE	BIT ADDRESS	PORT	BYTE	BIT ADDRESS
Port 0	4 0080		Port 2	4 00A0	
0.0		50080	2.0		500A0
0.1		50081	2.1		500A1
0.2		50082	2.2		500A2
0.3		50083	2.3		500A3
0.4		50084	2.4		500A4
0.5		50085	2.5		500A5
0.6		50086	2.6		500A6
0.7		50087	2.7		500A7
Port 1	4 0090		Port 3	4 00B0	
1.0		50090	3.0		500B0
1.1		50091	3.1		500B1
1.2		50092	3.2		500B2
1.3		50093	3.3		500B3
1.4		50094	3.4		500B4
1.5		50095	3.5		500B5
1.6		50096	3.6		500B6
1.7		50097	3.7		500B7

For example, a *READ @ 11 5528* command initiates a Read function at address 01 5528, then continues repeating that Read operation until another command is received.

Quick ROM and RAM Test Addresses 4-14.

The Quick RAM Test addresses (2X 0000 - 2X FFFF) and the Quick ROM Test addresses (3X 0000 - 3X FFFF) are used to control the Quick ROM and RAM Tests described below.

Block Write and Verify Addresses 4-15.

The Block Write and Verify addresses (4X 0000 - 4X FFFF) are used to fill blocks of memory with data and verify the contents. See Block Memory Tests.

NOTE

Illegal addresses are mapped into the 1 XXXX or 3 XXXX address space. After reporting the error, the operation is performed using the new address.

Special Addresses 4-16.

These addresses (F0 0000 - F0 FFFF) control Pod functions described later under Special Pod Functions.

QUICK-LOOPING READ AND WRITE FUNCTIONS 4-17.

The 8051 Pod provides Quick-Looping read and write functions with repetition rates which are considerably faster than the repetition rate of the ordinary Troubleshooter Looping function that is selected by pressing the LOOP key. Because of the increased repetition rate, the Quick Looping functions are particularly useful for enhanced viewing of signal traces on an oscilloscope that is synchronized to the TRIGGER OUTPUT pulse (available on the rear panel of the Troubleshooter).

Table 4-6. Special Function Bit Addresses

MNEMONIC ADDRESS		SPECIAL FUNCTION
	05 0000 - 05 007F	Boolean variables
P0.0-7	05 0080 - 05 0087	Port 0
TCON.0-7	05 0088 - 05 008F	Timer Control Register
IT0	05 0088	Interrupt 0 Type Control Bit
IE0	05 0089	Interrupt 0 Edge Flag
IT1	05 008A	Interrupt 1 Type Control Bit
IE1	05 008B	Interrupt 1 Edge Flag
TR0	05 008C	Timer 0 Run Control Bit
TF0	05 008D	Timer 0 Overflow Flag
TR1	05 008E	Timer 1 Run Control Bit
TF1	05 008F	Timer 1 Overflow Flag
P1.0-7	05 0090 - 05 0097	Port 1
SMOD.0-7	05 0098 - 05 009F	Serial Mode Register
RI	05 0098	Receive Interrupt Flag
TI	05 0099	Transmit Interrupt Flag
RB8	05 009A	Receive Bit 8
TB8	05 009B	Transmit Bit 8
REN	05 009C	Receive Enable
SM2	05 009D	Serial Mode Control Bit 2
SM1	05 009E	Serial Mode Control Bit 1
SM0	05 009F	Serial Mode Control Bit 0
P2.0-7	05 00A0 - 05 00A7	Port 2
IE.0-7	05 00A8 - 05 00AF	Interrupt Enable Register
EX0	05 00A8	Enable External Interrupt 0
ET0	05 00A9	Enable Timer 0 Interrupt
EX1	05 00AA	Enable External Interrupt 1
ET1	05 00AB	Enable Timer 1 Interrupt
ES	05 00AC	Enable Serial Port Interrupt
ET2	05 00AD	Enable Timer 2 Interrupt (8052)
EA	05 00AF	Enable All Interrupts
P3.0-7	05 00B0 - 05 00B7	Port 3
RXD	05 00B0	Serial Port Receive Pin
TXD	05 00B1	Serial Port Transmit Pin
$\overline{\text{INT0}}$	05 00B2	Interrupt 0 Input Pin
$\overline{\text{INT1}}$	05 00B3	Interrupt 1 Input Pin
T0	05 00B4	Timer/Counter 0 External Flag
T1	05 00B5	Timer/Counter 1 External Flag
$\overline{\text{WR}}$	05 00B6	Write Pin for External Memory
$\overline{\text{RD}}$	05 00B7	Read Pin for External Memory

Table 4-6. Special Function Bit Address (cont)

MNEMONIC ADDRESS		SPECIAL FUNCTION
IP.0-7	05 00B8 - 05 00BF	Interrupt Priority Register
PX0	05 00B8	Priority of Ext. Interrupt 0
PT0	05 00B9	Priority of Timer 0 Interrupt
PX1	05 00BA	Priority of Ext. Interrupt 1
PT1	05 00BB	Priority of Timer 1 Interrupt
PS	05 00BC	Priority of Serial Port Int.
PT2	05 00BD	Priority of Timer 2 int. (8052)
T2CON	05 00C8 - 05 00CF	Timer 2 Control Register (8052)
CP/$\overline{\text{RL2}}$	05 00C8	Capture/Reload Flag
C/$\overline{\text{T2}}$	05 00C9	Timer or Counter Select 2
TR2	05 00CA	Start/Stop Control 2
EXEN2	05 00CB	Timer 2 External Enable Flag
TCLK	05 00CC	Transmit Clock Flag
RCLK	05 00CD	Receive Clock Flag
EXF2	05 00CE	Timer 2 External Flag
TF2	05 00CF	Timer 2 Overflow Flag
STS.0-7	05 00C8 - 05 00CF	Status Register (8044)
RBP	05 00C8	Receive Buffer Protect
AM	05 00C9	Auto Mode/Addressed Mode
OPB	05 00CA	Optional Poll Bit
BOV	05 00CB	Receive Inf. Buffer Overflow
SI	05 00CC	Serial Interface Unit Interrupt
RTS	05 00CD	Request to Send
RBE	05 00CE	Receive Buffer Empty
TBF	05 00CF	Transmit Buffer Full
PSW.0-7	05 00D0 - 05 00D7	Program Status Word
P	05 00D0	Parity Flag
OV	05 00D2	Overflow Flag
RS0	05 00D3	Register Bank Select Bit 0
RS1	05 00D4	Register Bank Select Bit 1
F0	05 00D5	Flag 0
AC	05 00D6	Auxiliary Carry Flag
CY	05 00D7	Carry Flag
NSNR.0-7	05 00D8 - 05 00DF	Send/Receive Count Reg (8044)
SER	05 00D8	Sequence Error Received
NR0-NR2	05 00D9 - 05 00DB	Receive Sequence Counter
SES	05 00DC	Sequence Error Send
NS0-NS2	05 00DD - 05 00DF	Send Sequence Counter
ACC.0-7	05 00E0 - 05 00E7	Accumulator
B.0-7	05 00F0 - 05 00F7	B Register

Unlike the ordinary Troubleshooter Looping function, the software that controls the Quick Looping functions resides in the Pod and not the Troubleshooter. The operator selects these functions by using the special addresses listed in Table 4-3. For example, a read operation at address 10 0F00 causes the Pod to perform the Quick-Looping read operation at address 00 0F00.

It should be noted that the diagnostics performed by the Pod during the execution of the Quick-Looping read or write operations are less rigorous than the diagnostics performed during the execution of the ordinary Looping function. The Pod reports to the Troubleshooter any UUT system errors detected during the first iteration only. Subsequent UUT system errors are not reported.

If both error reporting and the Quick Looping functions are desired, you may apply the ordinary Troubleshooter Looping function to the Quick-Looping read or write, such as *READ @ 10 2000 LOOP*. The Troubleshooter will command read operations at address 10 2000 at the normal looping speed with full error reporting. For every ordinary read operation, the Pod will interject a few Quick-Looping read operations (with no error reporting) which will enhance oscilloscope viewing.

CAUTION

To prevent possible damage to the probe or the UUT, do not use the probe to generate stimulus pulses while a Quick-Looping function is being performed if the UUT crystal or clock frequency is less than 1 MHz.

The reason for the preceding caution is that the combination of the high repetition rate of a Quick-Looping function and a slow UUT clock (below 1 MHz) greatly increases the duty cycle of the probe. If the duty cycle is excessively high, the probe stimulus pulses can cause damage to the probe or the UUT. Note that the response capability of the probe, such as logic level reading with the Read Probe operation, is unaffected by high duty cycles.

SPECIAL ADDRESSES 4-18.

Addresses in the F0 XXXX range are special addresses, used to control internal Pod functions. The special addresses are described below, and summarized in Table 4-7. Note that some of these address are for Read operation only; attempts to Write data to them will yield drivability errors.

NOTE

Some of the Special Addresses are read-only locations. Attempting to write to them will result in drivability errors.

Self Test Failure Code (F0 0000) 4-19.

This special address contains the result code from the most recent Pod self test. If the Pod passes the self test, this special address contains the value FF. Other values denote specific errors that were detected during the self test program.

For complete information on deciphering the self test failure codes, refer to Section 6. Self Test Failure codes are summarized in Tables 6-2 and 6-3.

Status and Error Reporting Group (F0 0020 - F0 0026) 4-20.

The following group of special addresses contains summaries of errors and status. When reading these addresses, the normal dummy operation is not performed, thereby preserving the accuracy of the values.

Table 4-7. Special Addresses

ADDRESSES	FUNCTION	ADDRESSES	FUNCTION
F0 0000	Self Test Fail Code		
F0 0020	Last Error Summary	F0 0050	Port 0 Bus Test
F0 0022	Last Control Errors	F0 0051	Port 1 Bus Test
F0 0024	Last Force Line Report	F0 0052	Port 2 Bus Test
F0 0026	Last Status	F0 0053	Port 3 Bus Test
F0 0028	Error Summary Mask		
F0 002A	Control Error Mask	F0 0060	Refresh Enable
F0 002C	Force Line Error Mask		
		F0 0062	DIP Switch Override Mask
F0 0040	Last High Address Errors	F0 0064	DIP Switch Override Data
F0 0042	Last Low Address Errors		
F0 0044	Last Data Errors		

LAST ERROR SUMMARY (F0 0020) 4-21.

This special address contains a description of the last encountered error. This information, also referred to as "the fault byte", is returned to the Troubleshooter for error reporting. The user may inhibit the reporting of errors detected by the Pod by using the Setup functions of the Troubleshooter. This address is used to determine the Pod error status even though error reporting by the Troubleshooter has been inhibited. A summary of any errors detected by the Pod during the immediately previous UUT operation may be read from this address. The bit assignments are shown in Figure 4-1.

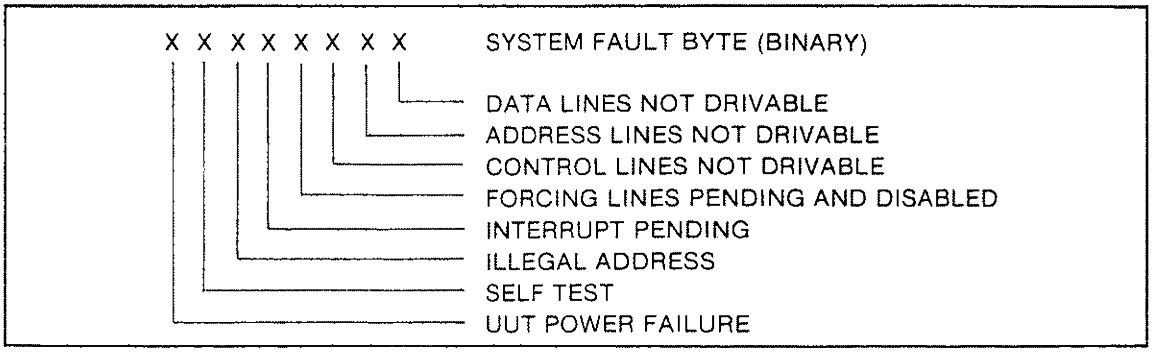
X X X X X X X X
SYSTEM FAULT BYTE (BINARY)
DATA LINES NOT DRIVABLE
ADDRESS LINES NOT DRIVABLE
CONTROL LINES NOT DRIVABLE
FORCING LINES PENDING AND DISABLED
INTERRUPT PENDING
ILLEGAL ADDRESS
SELF TEST
UUT POWER FAILURE

Figure 4-1. System Fault Byte

For example: If the Pod UUT connector is plugged into a UUT, and all error reporting is inhibited, performing a *READ @ F0 0020 = 18* indicates that:

1. An interrupt is pending.
2. Forcing line(s) are pending but disabled.

LAST CONTROL ERRORS (F0 0022) 4-22.

This special address contains a bit map of any control lines which the Pod might not have been able to drive properly during the last UUT operation. Refer to Table 4-2 or the Pod decal for bit assignments. For example:

READ @ F0 0022 = 80 OK

shows that the Pod was not able to drive bit 7, the $\overline{\text{PSEN}}$ line.

LAST FORCE LINE REPORT (F0 0024) 4-23.

This special address contains a bit map of any forcing lines which were detected as active during the last UUT operation. Refer to Table 4-1, for bit assignments for the two forcing lines, RST and MPU FAIL.

LAST STATUS (F0 0026) 4-24.

The status word from the immediately previous Pod operation may be read at this address. The data returned is displayed in hexadecimal rather than binary, as is the case with the *READ @ STS* command, but the status bit assignments are the same. Refer to Table 4-1 or the Pod decal (on the bottom of the Pod) for status line bit assignments.

For example,

READ @ F0 0026 = 08

shows $\overline{\text{INT0}}$ to be the only high level status line. Compare this to the *READ @ STS* example under Status Line Bit Assignments.

Error Reporting Masks (F0 0028 - F0 002C) 4-25.

These masks control the reporting of Error, Control Line drivability and Forcing Line detection errors. Set any bit in these masks to zero to disable the reporting of errors in that position. The default is all bits ENABLED.

ERROR SUMMARY MASK (F0 0028) 4-26.

The reporting of any individual errors in the error summary may be suppressed by setting the appropriate bits of the error summary mask to zero. The bit assignments correspond to the the System Fault Byte shown in Figure 4-1.

Errors corresponding to the suppressed bits will not be reported by the Troubleshooter. The default value is FF--all errors enabled.

Setting the self-test bit (bit 6) to 0 disables the Pod's internal self test and makes the Pod's internal addresses valid spaces. This function is used when troubleshooting a defective Pod.

CONTROL ERROR MASK (F0 002A) 4-27.

The reporting of any individual control drivability error may be suppressed by setting the appropriate bits of the control error mask to zero. The bit assignments correspond to those shown in Table 4-2. The complete error summary can be read from the Last Control Error special address. Errors corresponding to the suppressed bits will not be reported by the Troubleshooter. The default value is FF.

For example, a certain 8051 UUT may not allow the processor to drive the $\overline{\text{PSEN}}$ line low. If this is considered normal, performing a *WRITE @ F0 002A = 7F* will inhibit the reporting of $\overline{\text{PSEN}}$ line drivability errors during BUS TEST, while allowing drivability error reporting for all of the other control lines.

FORCELINE ERROR MASK (F0 002C) 4-28.

The reporting of any individual forcing line error (e.g., forcing lines asserted but not enabled) may be suppressed by setting the appropriate bits of the forcing line error mask to zero. The bit assignments correspond to those shown in Table 4-1, Status Line

Bit Assignments. The complete error summary can be read from the Last Force Line Report special address. Errors corresponding to the suppressed bits will not be reported by the Troubleshooter.

Default value = FF

Address and Data Errors (F0 0040 - F0 0044) 4-29.

This group of special addresses contains maps of drivability errors which were detected during the previous UUT operation. If reporting of these errors has been disabled using the Troubleshooter's Setup commands, reading these special addresses will reveal the source of address and data errors.

A bit set to 1 indicates a drivability error in the corresponding line. A 0 indicates a successful test on that line.

LAST HIGH ADDRESS ERRORS (F0 0040) 4-30.

A map of drivability errors detected in the high address bits during the last UUT operation.

LAST LOW ADDRESS ERRORS (F0 0042) 4-31.

A map of drivability errors detected in the low address bits during the last UUT operation.

LAST DATA ERRORS (F0 0044) 4-32.

A map of drivability errors detected in the data bits during the last UUT operation.

Bus Tests (F0 0050 - F0 0053) 4-33.

These special addresses contain a mask that specifies which pins of a port are to be tested for drivability. Output pins to be tested are specified by writing a mask to the address with the pin(s) set to 0. Input pins are set to 1.

Reading these special addresses causes a drivability test to be performed on the specified output pins. The result returned by the Read operation is a map of any pins which could not be driven properly. A 0 denotes a line which has been determined to be drivable. A 1 indicates a line where a drivability error was detected.

PORT 0 BUS TEST (F0 0050) 4-34.

Output drivability test for port 0.

NOTE

The UUT must provide external pull-up resistors on the Port 0 lines for the drivability test to work correctly. Port 0 has open-collector output drivers, and a high output will make them float if they are not pulled up.

PORT 1 BUS TEST (F0 0051) 4-35.

Output drivability test for port 1.

PORT 2 BUS TEST (F0 0052) 4-36.

Output drivability test for port 2.

PORT 3 BUS TEST (F0 0053) 4-37.

Output drivability test for port 3.

Refresh Enable (F0 0060) 4-38.

This special address allows the Pod to provide transparent read operations for the purposes of refreshing dynamic RAM or displays, keyboards, etc. in the UUT. Any non-zero value written to this address will initiate continuous program read operations at address 0000 as well as data read operations at 10000 whenever a read or write operation is done in the Pod.

The default is DISABLED (F0 0060 = 00)--no transparent read operations.

Mode Switch Manipulation (F0 0062 - F0 0064) 4-39.

Two special addresses are provided to allow the operator or a Troubleshooter program to remotely control the DIP Mode Switch located on top of the Pod. Refer to the label on the top of the Pod and Table 2-1, for identification of switch positions.

MODE SWITCH OVERRIDE MASK (F0 0062) 4-40.

This special address contains a mask that specifies which of the switch settings that are defined in Special Address F0 0064 will actually be used to override the Mode Switches. Only those switch positions identified by a 1 in this mask will be used to override the Pod's hardware Mode Switches. Writing new data to this special address is the same as changing the switch settings.

For example, if *WRITE @ F0 0062=02* is used with F0 0064=43 then only one bit (bit 1) of the data in F0 0064 will be used to override the Pod's hardware switches--that specifying port 2 to be I/O.

The default is 00, all switch overrides disabled.

MODE SWITCH OVERRIDE DATA (F0 0064) 4-41.

The Mode Switch Override special address contains a map of switch settings to be used instead of the configuration selected by the Mode Switches on the top of the Pod. Switch positions defined by this special address (and enabled by the mask in special address F0 0062) have precedence over the hardware switches. Data bit positions 0-7 correspond to the switch numbers 1-8 (i.e., bit 4 specifies switch 5). A bit that is written to a 1 specifies a switch that is enabled, and 0 specifies a switch that is disabled (open).

NOTE

Only switches 1 through 5 may be defined. Switch 6 (UUT Connection), switch 7 (Clock Source), and switch 8 (External Clock) are hardware connections and may not be overridden. Bits 5, 6, and 7 are ignored when set.

For example, a *WRITE @ F0 0064=43* configures the switches for Port 0 and 2 to be I/O, port 3 (pins 2,3, and 6) to be $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{WR}}$, and $\overline{\text{RD}}$ respectively. Bit 6 is ignored.

Quick Memory Tests (2X XXXX, 3X XXXX, F0 20XX, F0 30XX) 4-42.

The Quick Memory tests are controlled by software inside the Pod, rather than by software inside the Troubleshooter. They execute much faster than the corresponding tests that are built into the Troubleshooter.

The Quick Memory tests are controlled by writing setup information into special addresses as described below. Appendix A contains a program that may be used to automate these procedures and make the Quick Memory tests appear to the operator to work like the built-in Troubleshooter memory tests.

QUICK RAM TEST ADDRESSES (2X XXXX, F0 20XX) 4-43.

The Quick RAM Test allows the operator to test RAM address blocks more quickly than with the RAM Short test. The Quick RAM Test is considerably faster than the RAM Short test and is almost as rigorous. The Quick RAM test is particularly well suited for programming applications.

The Quick RAM Test is available in two variations: the normal RAM test and a pattern verification test.

- The normal RAM test consists of two phases: the first test phase is a read-write check, while the second checks address decoding. The read-write check is performed by writing and reading a one and a zero from each bit of each test address to ensure that there are no bits held high or low. After the read-write check is completed, a unique bit pattern has been written to each address. For the address decoding check, the Pod reads each address and compares the read data with the unique word that is expected.

- The pattern verification test simply verifies that memory contains expected data. It should be used following a normal Quick RAM Test to verify that the memory still contains the correct data after a longer period than is checked by the normal RAM test. It is provided primarily for testing dynamic RAM memory to assure that the memory is retaining information properly. If problems with dynamic RAM are suspected, it is suggested that the pattern verification test be used to follow the normal RAM test.

The starting and ending addresses for the Quick RAM Test are specified in a different manner than for the usual RAM Test. The starting and ending addresses are specified by writing to special addresses. The starting address is defined by a *WRITE @ 2X XXXX=0,* where *X XXXX* is the address to be used to start the Quick RAM test. The ending address, address increment, and test specification are defined by a *WRITE @ 2Y YYYY=ZN,* where *Y YYYY* is the desired ending address, *Z* is the desired increment, and N is the test specification. If *Z* is omitted or specified as 0, the address increment defaults to 1. N may be either 1 (normal Quick RAM test) or 2 (pattern verification test). The ending address must be greater than the starting address.

For example, to specify a normal Quick RAM test over the external RAM addresses 5000 through 5FFF with the default address increment of 1, do the following two operations:

WRITE @ 21 5000=0
WRITE @ 21 5FFF=1

To follow that test with a pattern verification test over the same address space, rewrite the ending address with the new specification:

WRITE @ 21 5FFF=2

The Quick RAM Test begins execution as soon as the operator completes the entry of the ending address. During and after execution of the test, the Troubleshooter will not display any information about the progress or results of the test unless requested by the operator. The test may be aborted before completion by selecting another operation.

To determine if the Quick RAM Test is still in progress, or what the test results are, the Troubleshooter operator should perform a *READ @ ENTER* operation (which commands a READ operation at the last entered address). In response, the Pod returns a byte indicating the status of the test or the test results. The status codes and their meanings are shown in Table 4-8.

Table 4-8. Quick RAM Test Addresses and Status Codes

OPERATION	PARAMETERS
WRITE @ 2X XXXX=0	X XXXX = Start Address
WRITE @ 2Y YYYY=ZN	Y YYYY = End Address
	Z = Increment
	N = Test Specification:
	1 = Perform RAM Test
	2 = Pattern Check
READ @ ENTER	Returns Status Code:
	00 = No test requested
	A0 = Aborted, new command entered
	A1 = Aborted, illegal data in command
	A2 = Aborted, illegal address in command
	B0 = Busy, read/write check
	B1 = Busy, address decoding check
	C0 = Complete, no errors
	F0 = Failed, read/write error
	F1 = Failed, address decoding error
READ-ONLY ADDRESS	**FUNCTION**
F0 2000	Start address, LSB
F0 2001	Start address, 2nd byte
F0 2002	Start address, MSB
F0 2004	End address, LSB
F0 2005	End address, 2nd byte
F0 2006	End address, MSB
F0 2008	Error address, LSB
F0 2009	Error address, 2nd byte
F0 200A	Error address, MSB
F0 200C	Expected data
F0 200E	Actual data
F0 2012	Hex mask - bad data bits, or address decode failed bit number
F0 20F0	Most recent code

Read-only special addresses in the F0 20XX range contain addition information about the Quick RAM Test, including records of addresses used and errors. The special addresses for the Quick RAM test are described in Table 4-8.

The Quick RAM Test is only valid in the RAM Address spaces 01 0000 through 02 00FF.

For more information about the test results, the operator may specify read operations at the other special addresses listed in Table 4-8. Make sure that you first specify the *READ @ ENTER* to find out if the test has been completed before reading at any of the special addresses. Unless the test has been completed (or failed), the information contained at the special addresses will pertain to a previous test rather than the current test, and the current test will be aborted.

For example, if any error is reported by the status byte, you can find the Least-Significant Byte of the address where the error occurred by *READ @ F0 2008*. You can get a hex mask of any bad data bits by *READ @ F0 2012*.

QUICK ROM TEST ADDRESSES (3X XXXX, F0 30XX) 4-44.

The Quick ROM Test allows the operator to test ROM address blocks more quickly than with the ordinary ROM Test. When the Quick ROM Test is performed, the Pod obtains a checksum that may be compared with a checksum obtained by performing the Quick ROM Test over the same address block of a known good UUT. Note that this checksum is not the same value as the signature that is obtained with the ordinary ROM Test.

The Quick ROM Test is not as rigorous and reliable as the signature analysis used by the ordinary ROM Test, nor does the Quick ROM Test have as extensive error reporting. However, the Quick ROM Test can detect inactive data bits, and the checksum can be used to detect a faulty ROM device with a high degree of confidence.

The Quick ROM Test is specified in a manner similar to the Quick RAM Test. The starting and ending addresses are specified by writing to special addresses. The starting address is defined by a *WRITE @ 3X XXXX=0,* where *X XXXX* is the address to be used to start the Quick ROM test. The ending address and address increment are defined by a *WRITE @ 3Y YYYY=Z1,* where *Y YYYY* is the desired ending address and *Z* is the optional increment. If *Z* is not specified or is specified as 0, the increment will default to 1. The ending address must be greater than the starting address.

For example, to specify a Quick ROM test over the internal program ROM addresses 0000 through 0FFF, do the following two operations:

WRITE @ 36 0000=0
WRITE @ 36 0FFF=1

The 3X XXXX portion of the address denotes a Quick ROM test. The X6 XXXX portion indicates operations on the internal ROM address space.

The Quick ROM Test begins execution as soon as the operator completes the entry of the ending address. During and after execution of the test, the Troubleshooter will not display any information about the progress or results of the test unless requested by the operator. The test may be aborted before completion by selecting another operation.

The Quick ROM Test is only valid in address spaces 0000 through 300FF and 06 0000 through 6 FFFF.

To determine if the Quick ROM Test is still in progress, or what the test results are, the Troubleshooter operator should perform a *READ @ ENTER* operation (which commands a READ operation at the last entered address). In response, the Pod returns a byte indicating the status of the test or the test results. The status codes and their meanings are shown in Table 4-9.

Read-only special addresses in the F0 30XX range contain addition information about the Quick ROM Test, including records of addresses used and errors. The special addresses for the Quick ROM test are described in Table 4-9.

For more information about the test results, the operator may specify read operations at the special addresses listed in Table 4-9. You should first *READ @ ENTER* to find out if the test has been completed before reading at any of the special addresses. Unless the test has been completed (or failed), the information contained at the special addresses will pertain to a previous test rather than the current test, and the current test will be aborted.

Table 4-9. Quick ROM Test Addresses and Status Codes

OPERATION	PARAMETERS
WRITE @ 3X XXXX=0 *WRITE @ 3Y YYYY=Z1*	X XXXX = Start Address Y YYYY = End Address Z = Increment
READ @ ENTER	Returns Status Code: 00 = No test requested A0 = Aborted, new command entered A1 = Aborted, illegal data in command A2 = Aborted, illegal address in command B0 = Busy, read/write check C0 = Complete, no errors C1 = Complete, inactive bits detected
READ-ONLY ADDRESS	**FUNCTION**
F0 3000	Start address, LSB
F0 3001	Start address, 2nd byte
F0 3002	Start address, MSB
F0 3004	End address, LSB
F0 3005	End address, 2nd byte
F0 3006	End address, MSB
F0 300C	Checksum LSB
F0 300D	Checksum MSB
F0 300E	Hex mask - inactive bits
F0 30F0	Most recent code

Block Memory Tests (4X XXXX, F0 40XX) 4-45.

The Block Memory Tests allow the user to fill blocks of memory with data and then verify accuracy of the contents. The Block Memory Tests are controlled by writing setup information into special addresses as described below.

The Block Memory Tests are much faster than the Troubleshooter's normal memory tests. In addition, they allow the user to customize special memory tests, such as might be desirable when testing a memory-mapped video display.

Appendix A contains a program that may be used to automate these procedures and make the Block Memory Tests appear to the operator to work like the built-in Troubleshooter memory tests.

Three variations of the Block Memory Test are available. The variations are specified when writing the ending address (see below).

- The Fill Test (specified by 1) will write the data that is contained in the starting address to all of the addresses in the block.
- The Verify Test (specified by 2) will read data from all of the addresses in the block an compare each one to the data contained in the starting address. Errors will be reported via the special addresses described below.
- The Fill and Verify Test (specified by 3) combines the Fill Test and the Verify Test into one step.

The Block Memory Test is specified in a manner similar to the Quick RAM Test. The data to be written to all addresses in the block is first written to the starting address, then the starting and ending addresses are specified by writing to special addresses. The starting address is defined by a *WRITE @ 4X XXXX=0,* where *X XXXX* is the address to be used to start the test. The ending address, address increment, and test specification are defined by a *WRITE@ 4Y YYYY=ZN,* where *Y YYYY* is the desired ending address, *Z* is the optional increment, and *N* is the test specification. If *Z* is not specified or is specified as 0, the increment will default to 1. N may be either 1 (fill block), 2 (verify block), or 3 (fill and verify block). The ending address must be greater than the starting address.

For example, to specify a Memory Fill for the external data memory (16-bit address) 0000 through 0FFF with an increment of 2 and data AA, do the following two operations:

WRITE @ 01 0000=AA	(Write data AA to starting address)
WRITE @ 41 0000=0	(Specify starting address)
WRITE @ 41 0FFF=21	(Specify ending address, increment, and test)

The Block Memory Test begins execution as soon as the operator completes the entry of the ending address. During and after execution of the test, the Troubleshooter will not display any information about the progress or results of the test unless requested by the operator. The test may be aborted before completion by selecting another operation.

Block Memory Tests are valid only in the Data Memory address space 01 0000 through 03 00FF.

Special addresses in the range of F0 40XX contain additional information about the Block Memory Test. These read-only locations contain records of the addresses used, errors, and other information. The special addresses for the Block Memory Test are described in Table 4-10.

Table 4-10. Block Memory Test Addresses and Status Codes

OPERATION	PARAMETERS
WRITE @ X XXXX=DD	X XXXX= Start Address
	DD = Fill Data
WRITE @ 4X XXXX=0	X XXXX = Start Address
WRITE @ 4Y YYYY=ZN	Y YYYY = End Address
	Z = Increment
	N = Test Specification:
	1 = Fill Memory
	2 = Verify
	3 = Fill and Verify
READ @ ENTER	Returns Status Code:
	00 = No test requested
	A0 = Aborted, new command entered
	A1 = Aborted, illegal data in command
	A2 = Aborted, illegal address in command
	B0 = Busy, filling
	B1 = Busy, verifying
	C0 = Complete, no errors
	F0 = Failed, verify
READ-ONLY ADDRESS	**FUNCTION**
F0 4000	Start address, LSB
F0 4001	Start address, 2nd byte
F0 4002	Start address, MSB
F0 4004	End address, LSB
F0 4005	End address, 2nd byte
F0 4006	End address, MSB
F0 4008	Error address, LSB
F0 4009	Error address, 2nd byte
F0 400A	Error address, MSB
F0 400C	Expected data
F0 400E	Actual data
F0 40F0	Most recent code

To determine if the Quick Block Test is still in progress, or what the test results are, the Troubleshooter operator should perform a *READ @ ENTER* operation (which commands a READ operation at the last entered address). In response, the Pod returns a byte indicating the status of the test or the test results. The status codes and their meanings are shown in Table 4-10.

For more information about the test results, the operator may specify read operations at the special addresses listed in Table 4-10. You should first *READ @ ENTER* to find out if the test has been completed before reading at any of the special addresses. Unless the test has been completed (or failed), the information contained at the special addresses will pertain to a previous test rather than the current test, and the current test will be aborted.

CHARACTERISTICS OF THE LEARN OPERATION 4-46.

The Learn operation of the Troubleshooter is designed to operate on bus-oriented systems employing RAM, ROM, and I/O that is external to the microprocessor. While the Learn operation of the Troubleshooter may be used with the 8044 and 8051 families of microprocessors, the results are not the same as those achieved with other types of microprocessors.

By default, the Learn function will evaluate only external address spaces as defined by the Mode Switch configuration. The Learn function may also be forced to evaluate internal address spaces. Such an operation might be necessary, for example, to get a checksum from internal ROM. Mode switch settings and the resultant learnable address blocks are described in Table 2-2, Learnable External Address Blocks.

I/O addresses reported by the Learn operation are those addresses which contain read/writable bits, but do not otherwise qualify as RAM.

I/O is reported for the special function registers (4 0080 - 4 00FF) and the bit address registers (5 0000 - 5 00FF) if those address ranges are specified.

NOTE

If I/O ports cause the Learn operation to stop because of drivability errors on input lines, the reporting of drivability errors may be disabled in the troubleshooter Setup operation by setting the SET-TRAP ADDR ERR and/or the SET-TRAP DATA ERR messages to NO. However, if driveability error reporting is disabled to allow the Learn operation to be performed, be sure to enable the error reporting when performing operations other than Learn.

CHARACTERISTICS OF BUS TEST 4-47.

Bus testing is dependent on the configuration switch settings for the lines being tested. If Port 0 and Port 2 are configured to be address/data lines, they are tested for drivability. If P3.6 and P3.7 are used as $\overline{\text{RD}}$ and $\overline{\text{WR}}$, they are also tested for drivability. $\overline{\text{PSEN}}$ and ALE are always tested for drivability.

The default address for the Bus Test is also determined by the configuration switch settings. If Port 0 is set to Address/Data and the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ lines are enabled, then the address is 2 0000. If Port 2 is set to Addresses then the Bus Test address is 1 0000. If the switches are all set for I/O, or if switch 5 is set for I/O (and therefore, there is no $\overline{\text{RD}}$ and $\overline{\text{WR}}$ lines), then the bus test is performed at 3 0000, the internal RAM address space.

RUN UUT Limitations 4-48.

CONFIGURATION 4-49.

The 8044's and 8051's are versatile microprocessors with many modes of operation. Because of this versatility, and because there is a serious lack of external clues as to what the microprocessor is doing or what it will do next, it is necessary to have the user declare what his UUT configuration is. The UUT/Pod configuration is accomplished through two means: the DIP switches and through a special address meant for overriding the DIP switch settings. This allows the user to test any UUT, regardless of configuration, since it is within his control to change the Pod's idea of the configuration at any time during testing.

Because of the use of DIP switches and/or special addresses to configure the Pod there is an important limitation on RUN UUT. That is, RUN UUT will only work if the UUT does not require that the Pod change the configuration of Port 0 or Port 2 during the course of the RUN UUT operation.

SYNCHRONOUS RESETS 4-50.

One further limitation on RUN UUT is that it will not work if the UUT depends on a synchronous Reset. This is because the Pod must drop out of Run UUT any time it is Reset in order to resynchronize its state counter. The state counter is essential for buffer operation in RUN UUT. The result is that when the Pod experiences a UUT Reset while performing RUN UUT, the Pod drops out of RUN UUT, takes an extra 100 μsec or so to resynchronize the state counter, and then jumps back into RUN UUT at the Reset address.

PROGRAMMING MODES 4-51.

The EPROM programming modes are not supported for RUN UUT.

ACTIVE ALE SIGNAL 4-52.

During all UUT testing, and as long as the UUT power supply is operable, the ALE signal is continuously present. This signal is provided to accommodate those UUTs which depend on ALE in order to remain active.

NOTE

The generation of the ALE output signal is suspended whenever the UUT power level falls to an unsafe level. This feature protects sensitive devices within the UUT which may otherwise be damaged by this signal.

PROBE SYNCHRONIZATION MODES 4-53.

Two synchronization modes are provided by the Pod, address sync and data sync. The modes synchronize the Troubleshooter probe operation to internal microprocessor events. When enabled, the sync output is active low once during each UUT access. The leading edge of the sync pulse begins at a time slightly prior to the event of interest so that the probe may be activated during the period of interest. The trailing edge of the sync pulse occurs at the moment when address or data is valid. If a probe is being used to capture data, then data is sampled on the trailing (rising) edge of the sync pulse.

Address sync is active from the falling edge of ALE during the cycle prior until the falling edge of ALE during UUTON and is gated to the sync output. Data sync may originate from several signal sources: $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, or UUTON. The source of the data sync signal depends on the type of access in progress. If any other sync mode other than address or data is specified, the sync output of the Pod is disabled.

MARGINAL UUT PROBLEMS 4-54.

Introduction 4-55.

The Pod is designed to approximate, as closely as possible, the actual characteristics of the microprocessor it replaces in the UUT. However, the Pod does differ in some respects. In general, these differences tend to make marginal UUT problems more visible. A UUT may operate with the actual microprocessor installed, but exhibit errors with the Pod plugged in. Since the Pod differences tend to make marginal UUT problems more obvious, the UUT is easier to troubleshoot. Various UUT and pod operating conditions that may reveal marginal problems are described in the paragraphs which follow.

UUT Operating Speed and Memory Access 4-56.

Some UUTs are designed to operate at speeds which approach the time limits for memory access. The Pod contributes a slight time delay which causes memory access problems to become apparent.

UUT Noise Levels 4-57.

As long as UUT noise level is low enough, normal operation is unaffected. Removing the UUT from its chassis or case may disturb the integrity of the shielding to the point where intolerable noise could exist. The Pod may introduce additional noise. In general, marginal noise problems will actually be made worse (and easier to troubleshoot) through use of the Pod and Troubleshooter.

Bus Loading 4-58.

The Pod loads the UUT slightly more than the UUT microprocessor. The Pod also presents more capacitance than the microprocessor. These effects tend to make any bus drive problems more obvious.

Clock Loading 4-59.

The Pod has a clock oscillator which replaces the UUT microprocessor oscillator. The Pod clock oscillator is designed to be less sensitive to capacitive loading than the UUT microprocessor oscillator. However, if the UUT has a clock source other than a crystal, it will experience greater than normal loading due to the capacitance of the Pod and its cable. While this loading will rarely have any effect on clock operation, it may make marginal clock sources easier to detect.

POD DRIVE CAPABILITY 4-60.

As a driving source on the UUT bus, the Pod generally provides equal to or better than normal 8044- and 8051-family current drive capability. However, lines P1.0 - P1.7 and P3.0 - P3.5 are not buffered and have approximately 100-ohm of series resistance (due to the protection network) between the microprocessor and the UUT. All Pod inputs and outputs (except the clock and RST) are TTL-compatible.

DRIVABILITY TESTING 4-61.

I/O Ports 4-62.

Data drivability is tested for all WRITE operations to the ports Port 0, Port 1, Port 2 and Port 3. This applies to all the byte and bit addresses listed in table 4-5. In each case, the least-significant bit of the port corresponds to data bit 0 and the most-significant bit to data bit 7. For example if a *WRITE @ 4 0090 = 00* resulted in data error 40, then it was P1.6 which had the problem.

Writes to the bit addresses will report data drivability errors as though a byte address had been used. For example, if the same error above were detected by a bit address, it would have happened as *WRITE @ 5 0096 = 00*, resulting in the same data error, 40. The data error refers to the port as a 8-bit object even though a 1-bit access was performed, and only one bit was tested.

Special Function Registers 4-63.

Only WRITE operations to registers which correspond to the I/O ports result in drivability testing. Other special function registers which may result in active outputs (such as SBUF), do not result in drivability tests being performed on those outputs. It is suggested that all port lines be tested for drivability by accessing the ports directly prior to performing functional tests using the other special function registers.

UUT POWER DETECTION 4-64.

A power sensing circuit within the Pod sends a power fail message to the Troubleshooter whenever the +5V power supply in the UUT drops below 4.5V or increases above 5.5V. This circuit causes the Troubleshooter to display a *BAD POWER SUPPLY* error message.

The *BAD POWER SUPPLY* message may be suppressed by changing the Setup command *SET - TRAP BAD POWER SUPPLY? YES* to *NO.*

Also, any time that the UUT power supply drops below about 3.5V, all active Pod outputs are disabled or driven to their high logic level. This feature has been incorporated to protect UUT circuits from possibly being damaged by Pod outputs when the power supply drops below safe operating limits. When proper power levels are restored to the UUT, the Pod outputs will return to normal, and the Troubleshooter will be ready for additional testing.

CLOCK SOURCES, SETUPS, AND PROBLEMS 4-65.

The 8051 oscillator has several different modes of operation, and for correct operation of the Pod the user must configure the Pod for his particular UUT using the mode switches. The position of switch 7, Clock Source, is determined by whether the UUT has a separate clock generator driving the processor, or a crystal across pins 18 and 19. Switch 8, External Clock, is set depending on whether pin 18 (XTAL2) is driven from an external source or pin 19 (XTAL1).

NOTE

If the UUT has a gate that is driven from pin 18 of the microprocessor and a crystal across pins 18 and 19, the switches should be configured with switch 7 set to XTAL and switch 8 set to XTAL1. This will make the Pod capable of driving a CMOS gate from pin 18. A TTL gate will load the oscillator circuit and cause unpredictable behavior.

EFFECTS OF THE CONFIGURATION SWITCHES 4-66.

Introduction 4-67.

The procedure for setting the configuration switches is explained in Section 2. Each of the switch settings has widespread effects on learnable addresses, port characteristics, and other facets of Pod operation. The effects of each of the configuration switches is described here in detail and summarized in Table 4-11. Table 2-2 shows the settings of the configuration switches.

Table 4-11. Effects of Configuration Switches

SWITCH	AFFECTED POD CHARACTERISTIC
Port 0	Default LEARN addresses Default BUS TEST address Address lines tested by BUS TEST Port 0 configuration during READ and WRITE Port 0 configuration during RUN UUT
Port 2	Default LEARN addresses Default BUS TEST address Address lines tested by BUS TEST Port 2 configuration during READ and WRITE Port 2 configuration during RUN UUT
P3.2	Generation of active interrupt report
P3.3	Generation of active interrupt report
P3.6 and P3.7	Default LEARN addresses Default BUS TEST address Control lines tested by BUS TEST
UUT Connection	Reset line behavior Forcing line report
CLK Source	Clock/oscillator circuitry
External CLK	XTAL1 and XTAL2 connections to clock/ oscillator circuitry

Switch 1 (Port 0) 4-68.

DEFAULT LEARN ADDRESSES 4-69.

If Port 0 is declared to be I/O, no external memory devices are possible. In this case there are no default LEARN addresses supplied. If Port 0 is declared to be ADDR/DATA then the default LEARN addresses depend on the setting of the Port 2 and the P3.6/P3.7 switches.

DEFAULT BUS TEST ADDRESS 4-70.

If Port 0 is declared to be I/O, no external bus is considered to exist. In this case the default BUS TEST address is 3 0000--the internal RAM space. If Port 0 is declared to be ADDR/DATA the default BUS TEST address depends on the setting of the Port 2 and P3.6/P3.7 switches. Depending on those settings, the default BUS TEST address may be 1 0000, 2 0000, or 3 0000.

ADDRESS LINES TESTED BY BUS TEST 4-71.

The low-order address bus is only checked for drivability if Port 0 is declared as ADDR/DATA.

PORT 0 CONFIGURATION DURING READ AND WRITE 4-72.

Port 0 will latch an I/O output on its lines and will keep that data there throughout testing of addresses which do not affect Port 0 only if Port 0 is declared as I/O. If it is declared ADDR/DATA, I/O outputs will not remain latched on Port 0. The port is instead tri-stated when not in use as address or data.

PORT 0 CONFIGURATION DURING RUN UUT 4-73.

Port 0 will behave as only an open-drain I/O port or as an address/data bus, depending on the switch setting, during RUN UUT. A UUT which attempts to utilize both modes in its program, may not be able to perform RUN UUT correctly.

Switch 2 (Port 2) 4-74.

DEFAULT LEARN ADDRESSES 4-75.

The default LEARN addresses depend on the settings of the Port 0, Port 2, and P3.6/P3.7 switches. Port 2 must be declared as ADDR in order for the external program ROM and 16-bit address RAM to be included as default LEARN addresses.

DEFAULT BUS TEST ADDRESS 4-76.

With Port 0 declared as ADDR/DATA and P3.6/P3.7 declared as $\overline{RD}$/$\overline{WR}$, if Port 2 is declared as ADDR, then the default BUS TEST address is 1 0000. If Port 2 is declared as I/O then the BUS TEST address is 2 0000.

ADDRESS LINES TESTED BY BUS TEST 4-77.

The high-order address bus is only checked for drivability if Port 2 is declared as ADDR.

PORT 2 CONFIGURATION DURING READ AND WRITE 4-78.

Port 2 will latch high-order addresses or I/O outputs on its lines throughout all UUT testing. However, high data on these lines is buffered differently depending upon the setting of the Port 2 switch. If Port 2 is declared as I/O then high outputs only source current on high-going transitions and only for two clock periods. The high output is then left to be driven through a 22K ohm pull-up resistor. If Port 2 is declared as ADDR, then high outputs source current continuously.

PORT 2 CONFIGURATION DURING RUN UUT 4-79.

Port 2 will behave as only a quasi-bidirectional I/O port or as an address bus, depending on the switch setting, during RUN UUT. A UUT which attempts to utilize both modes in its program, may not be able to perform RUN UUT correctly.

Switch 3 (P3.2) 4-80.

GENERATION OF ACTIVE INTERRUPT REPORT 4-81.

When P3.2 is declared as $\overline{INT0}$, a low value sensed on the line will cause an active interrupt report. When declared as I/O, values on this line do not affect the active interrupt report.

Switch 4 (P3.3) 4-82.

GENERATION OF ACTIVE INTERRUPT REPORT 4-83.

When P3.3 is declared as $\overline{INT1}$, a low value sensed on the line will cause an active interrupt report. When declared as I/O, values on this line do not affect the active interrupt report.

Switch 5 (P3.6/P3.7) 4-84.

DEFAULT LEARN ADDRESSES 4-85.

When declared as I/O, no external RAM space is included as default LEARN addresses. If this switch declares P3.6/P3.7 to be $\overline{\text{RD}}/\overline{\text{WR}}$, then one or both of the external RAM address spaces may be included as default LEARN addresses, depending on the setting of the Port 0 and Port 2 switches.

DEFAULT BUS TEST ADDRESS 4-86.

When P3.6/P3.7 are declared as $\overline{\text{RD}}/\overline{\text{WR}}$, one of the external RAM addresses 1 0000 or 2 0000 may be used as the default BUS TEST address. If this switch declares the lines to be I/O, then the internal RAM space, 3 0000, is used as the default BUS TEST address.

CONTROL LINES TESTED BY BUS TEST 4-87.

The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ control lines are only tested for drivability if this switch declares P3.6/P3.7 to be $\overline{\text{RD}}/\overline{\text{WR}}$. If they are declared to be I/O then they are not tested for drivability.

Switch 6 (UUT Connection) 4-88.

RESET LINE BEHAVIOR 4-89.

When set to the "Clip-on" position, this switch causes the RST line to be permanently pulled high.

FORCING LINE REPORT 4-90.

With the switch set to the "Clip-on" position RST is held high. This is the active state for this line which is a forcing line. In order to avoid reporting an active forcing line on every UUT operation, the RST line is omitted from the forcing line report.

Switch 7 (CLK Source) 4-91.

CLOCK/OSCILLATOR CIRCUITRY 4-92.

When set to the XTAL position, the clock circuitry behaves as an oscillator. When set to the TTL position, the clock circuitry behaves as a buffer.

Switch 8 (External CLK) 4-93.

XTAL1 AND XTAL2 CONNECTIONS TO CLOCK/OSCILLATOR CIRCUITRY 4-94.

When the CLK source switch is set to the TTL position, one of the XTAL lines is used as an input and the other is not used. The External CLK switch allow the XTAL lines to be swapped so that the proper one gets the TTL input.