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biomation

MODEL 2710
DATA DOMAIN LOGIC ANALYZER

OPERATING AND SERVICE MANUAL

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GOULD

An Electrical/Electronics Company

The above photograph shows the Model 2710 Logic Analyzer being used with its companion accessory, the Model 2710 MPU Adapter, on an Intel SDK 8085A board.

OPERATING AND SERVICE MANUAL

MODEL 2710

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SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'S WARRANTY, GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Instrument Description

Refer to Figure 1.1 for front view of Model 2710 as well as flying lead ribbon cable and 40-pin dip clip.

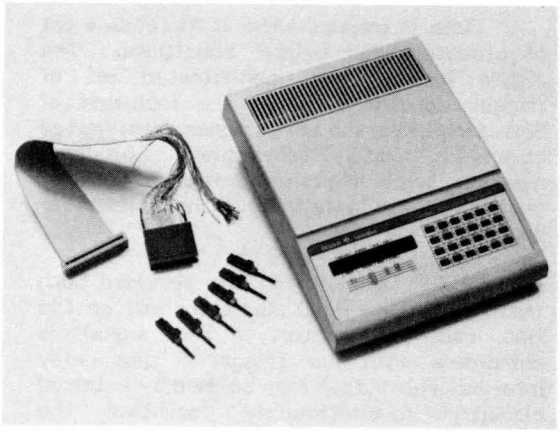


Figure 1.1 The Model 2710 Logic Analyzer is supplied with a flying lead ribbon cable, six hook-type grabbers, and a 40-pin dip clip for easy connection to your system.

The Model 2710 is a 27-channel, synchronously clocked, data domain logic analyzer. While the 2710 has been designed for compatibility in recording 8-bit microprocessor program execution steps, the instrument is flexible enough to make data domain recordings of any TTL logic system. The 2710 permits the recording of 64 words, 27 channels, or bits, wide containing the address and data buses, as well as status information, of many standard microprocessors and bit-slice processor implementations. All control of the unit is via a multifunction 24-button keyboard, while status and data conditions are displayed on the integral 16-digit, seven-segment calculator-type LED display. All inputs are TTL compatible and present one low power Schottky load. The 2710 records synchronously at rates from DC to 10 MHz, using the clock from the system under test.

The unit has four operating modes: Specify, Record, Memory, and Calculate. In the Specify mode, the conditions for recording are established. In the Record mode, the 2710

searches for those conditions to capture data from the system under test. In Memory mode, data that has been recorded from the system under test can be displayed and manipulated. In the Calculate mode, addition, subtraction, and radix (base) conversion may be done in octal, decimal, and hexadecimal.

Data is trapped when it matches a set of predetermined trigger conditions. The 2710's flexible and sophisticated set of trigger conditions allows the inclusion of both pretrigger and post-trigger data, nested triggering into subroutines, bit-level masking, logic inversion, selective clocking qualifiers, and delays by either clocks or events.

A TTL output signal is provided both from a separate BNC connector and on the flat cable connector. The signal is coincident with the Trigger B plus delay interval. This output may be used by external circuitry to ultimately facilitate the appropriate halt (if desired) of the system under test. It can also be used to make the 2710 a very sophisticated triggering device for other digital test equipment.

1.4 Specifications

CONTROLS

All control of the 2710 except the AC power switch is via the 24-button tactile feedback keyboard.

Input Specifications: Clock Slope
Clock Qualifiers
Delay by Clocks
Delay by Events
Inversion Mask

Record Controls: Trigger A
Mask A
Trigger B
Mask B
Arm
Event A
Event B
Stop

Calculator Mode: Addition
Subtraction

Number Base: Octal
Decimal
Hexadecimal

Memory Display: Step
Backstep
Go To (memory location)

DATA INPUTS

27 total; 16 labeled Address, eight labeled Data, and three labeled Qualifiers. The 2710's data Inversion Mask allows recording of positive or negative logic lines.

Input Current Levels: (Low Power Schottky TTL) Low: 0.2 mA at 0.4 V.
High: 20 µA at 2.7 V.

Threshold: TTL (normally positive logic; +2.0 V = one, +0.8 V = zero).

Setup and Hold Time: Setup = 30 ns. Hold = 0 ns (with respect to the clock's active edge).

CLOCK

External. Input via the 2710's multiconductor ribbon cable.

Input Current Levels: (Low Power Schottky TTL) Low: 0.8 mA at 0.5 V.
High: 100 µA at 2.7 V.

Threshold: TTL.

Rates: DC to 10 MHz.

Pulse Width: 30 ns minimum.

Slope: Active edge selectable, positive (rising) or negative (falling).

CLOCK QUALIFIERS

Two dedicated clock qualifiers via the 2710's multiconductor ribbon cable.

Input Current Levels: (Low Power Schottky TTL) Same as data inputs.

Threshold: TTL.

Rates: DC to 10 MHz.

States: Selectable, one or zero.

Setup and Hold Time: 30 ns and 0 ns respectively, relative to the active clock edge chosen.

TRIGGER

The 2710 has a two-stage combinational trigger, Trigger A and Trigger B. Both triggers are independently user-definable 27-bit words. Each bit of each trigger can be defined as a logic "one", "zero", or "don't care" via its trigger mask.

Sources: Manual or Internal True.

Manual: Event A and B via keyboard.

Internal True: The unit is triggered when the input data matches both of the combinational triggers in the sequence of Trigger A then Trigger B.

Arm: Manual via the keyboard.

Trigger Output: (Low Power Schottky TTL) Positive true, 32 clock period width, occurs 1 clock + 120 ns (typical delay) after occurrence of Trigger B plus user selectable delay interval.

MEMORY

64 27-bit words. Memory elements are static RAMs.

RECORD MODES

Selectable Pretrigger, Clock Delay, or Event Delay. The 2710 starts recording when the Arm button is depressed. The unit stops recording after both Trigger A and B have been recognized sequentially (or simulated via manual Event A and B) and either the appropriate number of clock delays (N+32) have been counted out or the appropriate number of events of Trigger B (N+1) have been recognized and 32 clock intervals of post-trigger information have been recorded.

Selectable Pretrigger: A recording can be made containing from 31 to 0 words of pretrigger data by entering from 0 to 31 clock delays prior to arming the unit.

Range: 0 to 31 (Decimal).

Clock Delay: A recording can be made capturing data that occurred a user selectable number of clock cycles (N+32) after the appearance of Trigger B.

Range: 0 to 9999 (Decimal).

Event Delay: A recording can be made capturing data that occurred around a user selectable number of events of Trigger B (N+1).

Range: 0 to 9999 (Decimal).

NOTE: Depressing the STOP button will terminate a recording immediately.

DISPLAY

Composed of 16 3-mm seven-segment calculator-type LEDs. Used for feedback of status conditions, input specifications, recorded data viewing, and calculator computations.

DATA FORMAT

64 words, one word viewable on the LED display at a time. Each word is formatted left to right as Memory Location, Address, Data, and three Trigger Qualifiers.

MISCELLANEOUS

Operating Temperature: Range: 0 to 50°C.

Power: 100, 117, or 234 VRMS ± 10%, 50 to 60 Hz.

Power Consumption: 25 watts.

Size: Height: 2.75 in. (7.0 cm)
Width: 9.5 in. (29.1 cm)
Depth: 13.0 in. (33.0) cm)

Weight: 7.0 lbs (3.2 kg)

ACCESSORIES INCLUDED

The unit is supplied with an integral line cord, a ribbon cable, a 40-pin dip clip, six individual grabbers, and an Operating and Service Manual.

Accessories Available. The following items may be ordered by contacting your local representative or the Gould Inc., Biomation Division, factory.

Item*	Biomation Stock No.
Spare Data Input Cable	0271-0040
Spare 40-pin IC Spring Clip	6000-0248
Extra Operating and Service Manual	0271-0015

Model 2710 MPU Adapter. This accessory is a universal microprocessor adapter that allows the 2710 to be used easily with microprocessors using multiplexed data or address lines and OR clocking for signal isolation. In addition to providing demultiplexing and combinational clocking capabilities, the adapter provides input buffering and allows the most efficient connection of the 2710 to timing logic analyzers (such as the Biomation 920-D, 1650-D or K100-D), oscilloscopes, and other digital test equipment. See Figure 1.2.

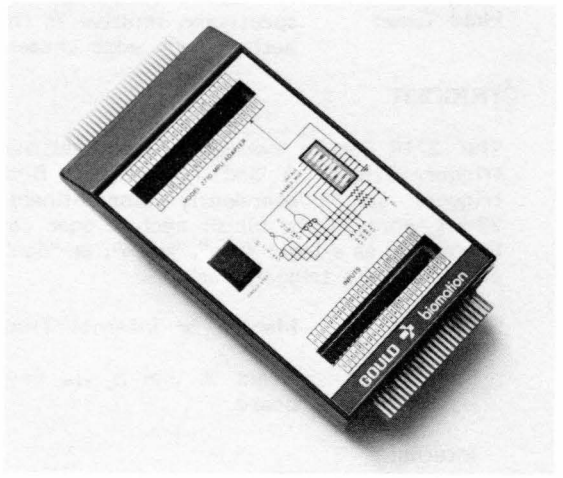


Figure 1.2 The 2710 MPU Adapter.

*Consult factory for current prices.

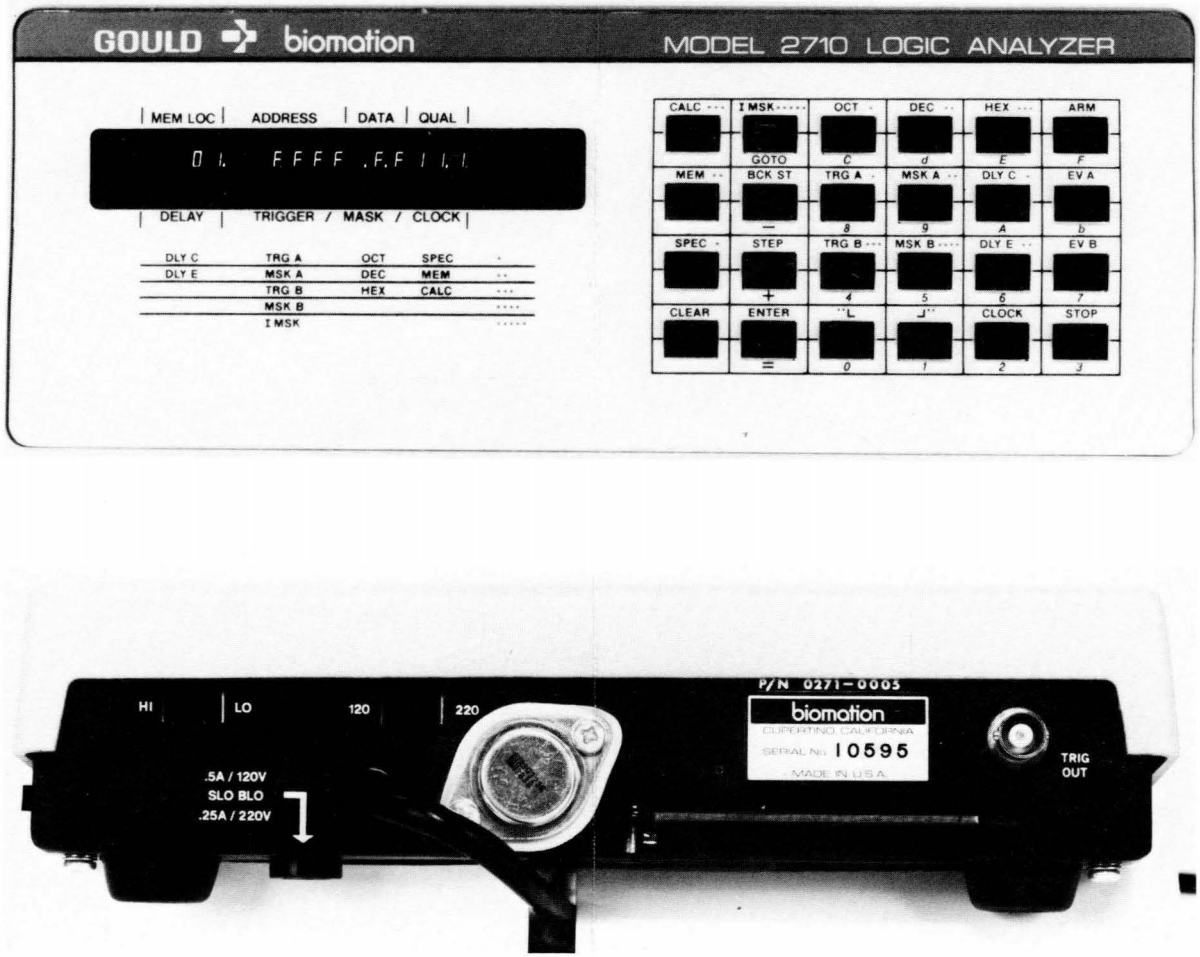


Figure 2.1 Front and Rear Panel Views of the Model 2710.

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model 2710.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken connectors or pins on ribbon cable and dip clip. Inspect case, panel, and keys for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local representative, or the Gould Inc., Biomation Divison, factory.

2.3 Storage and Shipment

Should it become necessary to store or ship your 2710, always remember to protect it as well as possible to prevent damage due to exposure to extreme environmental conditions or abusive handling. Contract packaging companies in many cities can provide dependable custom packaging on short notice. A factory approved shipping carton can also be obtained by contacting Gould Inc., Biomation Division.

2.4 Power Connection

- CAUTION -

Before connecting the 2710 to a power source, ensure that the two rear panel power line voltage selector switches are in the correct positions (See Figure 2.1) and that the proper fuse is installed as per Table 2.1.

Table 2.1 Line Voltage Selections

Lo/Hi	120/220	Nominal Line Voltage, +10%	Fuse (Amp Slow Blow)
Lo	120	100	0.5
Hi	120	120	0.5
Lo	220	200	0.25
Hi	220	240	0.25

2.5 Preparation

The 2710 is a self-contained unit with a built-in display. All that is required to use the instrument in its Calculator mode is to connect the line power properly. To make a recording requires the appropriate assignment and attachment of the input lines (provided via the rear panel ribbon cable connector) to the device to be tested. Before this is attempted, we strongly recommend a thorough reading of Section III, OPERATION.

2.6 Initial Warm-up

Although the Model 2710 is a solid state instrument, a brief warm-up period of at least two minutes is recommended for the internal circuitry to reach thermal stability.

SECTION III

OPERATION

3.1 Introduction

This section explains the use and function of the rear panel inputs and outputs, the keyboard, and the display. It also offers a step-by-step explanation and procedure for operating the unit in each of its four modes; Specify, Record, Memory and Calculate. A thorough understanding of this section is essential to the successful use of the instrument.

3.2 Inputs and Outputs

On the rear of the instrument you will find, along with the line cord and power selection switches, a BNC-type female connector and a flat, 50 pin, signal cable connector. The only output signal provided from the instrument is a TTL level HALT, or TRIGGER OUT, signal that is normally held low but gated high coincident with the trigger plus delay interval occurrence. Once gated high, it remains high until the completion of the recording (32 clock periods). This signal is available both from the BNC connector and from pin 40 on the signal cable connector. It is provided to facilitate the appropriate halting (if desired) of the system under test, and to allow the 2710 to be used as a very sophisticated triggering device for other test equipment. All of the remaining pins on the signal cable connector either provide inputs necessary for making full use of the Model 2710's recording capabilities, allow the connection of soon to be available accessories, or represent unused lines.

Table 3.1 has been provided as a guide to the input signal cable pinouts, their identification on the flying leads of the included cable, and their intended assigned function in normal operation. Please note, however, that all 27 of the lines designated as address, data, and trigger qualifier lines are dedicated only in the sense that if used as suggested, the resultant display will match the format labels presented at the top of the front panel. This allows the data to be conveniently reviewed in either hexadecimal, octal, or decimal groupings. Because of the 2710's bit-level triggering and masking capabilities, you can if you choose, use the instrument as a general purpose data recorder on any synchronous TTL logic system simply by decoding the display into a binary format.

Proper mechanical connection of all test signals is essential to obtaining the desired recording. It is usually most convenient to connect directly to your microprocessor using the supplied 40-pin DIP clip to provide connection points for the marked flying leads. The six individual grabber hooks are supplied to allow easy connection of two or more signals to the same point (such as grounds or clock and trigger qualifiers) and individual connection to test points not on the microprocessor (such as RAM and ROM enable signals). In addition, the flying leads can also be attached to any standard size (0.025 in. or 635 mm) wire wrap posts to access bus and other test signals.

3.3 Using the Keyboard

All control of the Model 2710's operation is accomplished via the 24 button, positive feedback, multi-function keyboard found on the right front panel of the instrument. The use and function of these keys is discussed at length throughout the OPERATION section (III). Refer to Figure 2.1. In addition to illustrating the positions of the various keys, it also duplicates the entire front panel layout for easy reference. Also, refer to the flowchart operation guide found at the end of Section III. This guide shows all of the keystroke sequences necessary to operate the 2710.

3.4 Reading the Display

The integral 16-digit, seven segment LED display has five main functions: 1. Provides status information on keyboard control conditions. 2. Ensures proper specification of recording parameters. 3. Allows the partial monitoring of a recording in

Table 3.1 Signal Cable Pinouts

Pin Number	Sleeve Marking	Sleeve Color	Signal
1	DO	Yellow	Data (Least Significant Bit)
2	D1		
3	D2		
4	D3		
5	D4		
6	D5		
7	D6		
8	D7	Yellow	Data (Most Significant Bit)
9	None	Black	Data Ground
10	AO	White	Address Lower Byte (Least Significant Bit)
11	A1		
12	A2		
13	A3		
14	A4		
15	A5		
16	A6		
17	A7	White	Address Lower Byte
18	None	Black	Address Lower Byte Ground
19	A8	White	Address Upper Byte
20	A9		
21	A10		
22	A11		
23	A12		
24	A13		
25	A14		
26	A15	White	Address Upper Byte (Most Significant Bit)
27	None	Black	Address Upper Byte Ground
28	R/W	Yellow	Read/Write. First of 3 qualifier bits recorded. Read = "1" (+2.0 V), Write = "0" (+0.8 V).
29	TQA		Trigger Qualifier A. Second qualifier bit recorded.
30	TQB	Yellow	Trigger Qualifier B. Last of three qualifier bits recorded.
36	None	Black	Ground for Recorded Qualifier
37	CQA	Blue	Clock Qualifier A. Not recorded.
38	CQB		Clock Qualifier B. Not recorded.
40	HALT		Output signal. Also provided via the separate BNC connector. Signal is coincident with the trigger plus delay interval occurrence.
41	ALE*	Blue	Address Latch Enable
42	None	Black	Clock Qualifier Ground
43	CK A	Red	External Clock Input A
44	CK B*		B
45	CK C*		C
46	CK D*	Red	External Clock Input D
47	None	Black	Clock Ground. This ground should always be connected. In most cases, the other grounds need not be connected.

*These lines (ALE, CK B, CK C, and CK D) are provided for use with the 2710 MPU Adapter accessory. They are not used during normal operation of the 2710.

process. 4. Provides an easy means of reviewing recorded data. 5. Facilitates both calculations and number base conversions.

Status information is provided by two methods; first, by the placement of coded dots, and second, by the placement of blinking fields. The key to the dot code is provided by the chart directly below the display. For instance, if one dot is lit in the display above the dot table column containing SPEC, MEM, and CALC (see Figure 2.1), a glance to the right side of the dot table reveals that one dot corresponds to SPEC; thus, the instrument is in the Specify mode. Two dots would denote the Memory mode and three dots the Calculate mode. Similarly, three dots above the dot table column OCT, DEC, and HEX would mean the instrument currently was operating in a hexadecimal format. Four dots above the column TRG A, MSK A, TRG B, MSK B, and I MSK would mean you were in the process of specifying trigger mask B and so on.

Understanding the status information provided by a blinking field is even simpler. Whenever a field is blinking, the unit is looking for an entry in that field. Once the field has been described as desired by using the appropriate number keys, push the ENTER key and the field will stop blinking to show that it has been entered as displayed. This continuous, non-blinking display of entered fields allows you to check an entry to ensure its proper specification.

The third purpose of the display is to allow the partial monitoring of a recording in process. This is accomplished by means of alphabetic cueing that appears on the far left of the display. The explanation of these cues is given in the corresponding boxes on the far right of the foldout flowchart guide at the end of this section.

Fourth, the display provides an easy means of reviewing recorded data by formatting it left to right according to the 8-bit microprocessor labels printed above the display. The memory location of the 27-bit word being displayed is always shown in decimal at the far left of the display.

Finally, the display allows the direct readout of answers to addition, subtraction, and radix conversion problems done in the Calculate mode.

3.5 Changing or Clearing Entries

The 2710 will accept changes of numerical entries through either of two methods. The first way is through the use of the CLEAR key. If you are in the process of making an entry and push the CLEAR key once, then the last digit entered will be replaced by a minus sign and you can re-enter that digit. If you push the CLEAR key twice, then the whole field will be replaced by a single minus sign on the far left position of the field and you can re-enter the entire field. This method can be used to make changes in either the octal, decimal, or hexadecimal modes. It **must** be used for all changes in the decimal mode, including all entries pertaining to the Delay by Clocks or Events field.

The second method is provided as a convenient way to change entries while in the octal or hexadecimal modes. Simply key in the new entries. Each new digit keyed in will appear on the far right side of the number field. This will cause all of the digits in the field to be moved one space to the left and the far left digit to be thrown away. When the field's display matches your specifications, press the ENTER key to fix that field in the 2710's memory.

3.6 Selecting Recording Parameters (Specify Mode)

Your 2710 has been designed to offer extremely sophisticated and versatile control over the data selected for a recording. You can conveniently capture virtually any program execution in the 2710's 27 bit x 64 word memory by simply entering the appropriate parameter selections via the keyboard. Each parameter, once entered, is stored in memory for use in subsequent recordings and need not be re-entered unless you desire to change it or the line power has been switched off. These

parameters allow number base selection of either hexadecimal, octal, or decimal formats, delay by clocks or events, selective qualification of the record clock, single or nested combinational triggering, full character to bit-level masking of both triggers, and input logic inversion.

Any of these changes can be made in any order as long as you're in the Specify mode, but it's easiest to make a recording if you follow a logical flow, as shown in the foldout flowchart guide.

When the 2710 is first turned on, it has a predetermined set of default parameters that are loaded into its memories. These parameters are described in Table 3.2.

Table 3.2 Default Parameters of the Model 2710

Item	Power-Up Condition
Operation Mode	Specify
Number Base	Hex
Delay by Clocks (DLY C)	All Zeros
Delay by Events (DLY E)	" "
Trigger A (TRG A)	" "
Mask A (MSK A)	" " (Don't Cares)
Trigger B (TRG B)	" "
Mask B (MSK B)	" " (Don't Cares)
Inversion Mask (I MSK)	" " (Positive Logic)
Clock (CLOCK)	Reads falling edge (⌐‾|_) when both qualifiers (CQA and CQB) are high (=1).

3.6.1 Number Base Selection

The Address and Data portions of the trigger words, when working with an 8-bit microprocessor, comprise 24 of the 27 available bits. These 24 bits are divided into three fields of eight bits each as suggested in Table 3.1; two fields for the address and one field for the data. To allow you to match the program listing of the system you are testing, the 2710 has been designed to permit entry of these fields in either hexadecimal, octal, or decimal, whichever is the most appropriate or convenient. All that is necessary to change the number base of these fields while in the Specify Mode is to press the key corresponding to the base you want to change to: OCT, DEC, or HEX. Once a new base has been selected, the display will continue to be formatted in that base until another change is entered or the line power is interrupted. The remaining three qualifiers, bits 25, 26, and 27 of the trigger, are always specified in binary. The input lines corresponding to these channels are marked, left-to-right as R/W, TQA, and TQB. For further study of the appropriate keystroke sequences under various conditions, refer to the foldout flowchart guide.

3.6.2 Delay By Clocks

On power-up condition, the Model 2710 is preset (Delay = 0000) to record 31 clock cycles of pretrigger data, the trigger word, and 32 cycles of post-trigger information. By using the Delay by Clocks feature, some or all of the pretrigger data, including the actual trigger, can be replaced by post-trigger data, and the whole recording can be moved downstream in time by as many as 9999 clock cycles. This process is illustrated in Figure 3.1. The keystroke sequence for entering a clock delay is shown in the flowchart guide.

3.6.3 Delay by Events

This is a second type of delay whereby the instrument records the 31 clock periods of data just prior to the Nth + 1 occurrence of the event of Trigger B, Trigger B, and the 32 periods of data immediately afterwards. The event, or trigger, count will begin after you have armed the unit and it has found at least one occurrence of the event of Trigger A. See Figure 3.2 for an illustration of the process that occurs when the Delay by Events feature is used. The keystroke sequence for entering a Delay by Events is very similar to entering a Delay by Clocks. As with the other functions, this sequence can be seen in the flowchart guide.

3.6.4 Clock Qualifiers

The 2710 is a completely synchronous instrument. It has no internal record clock

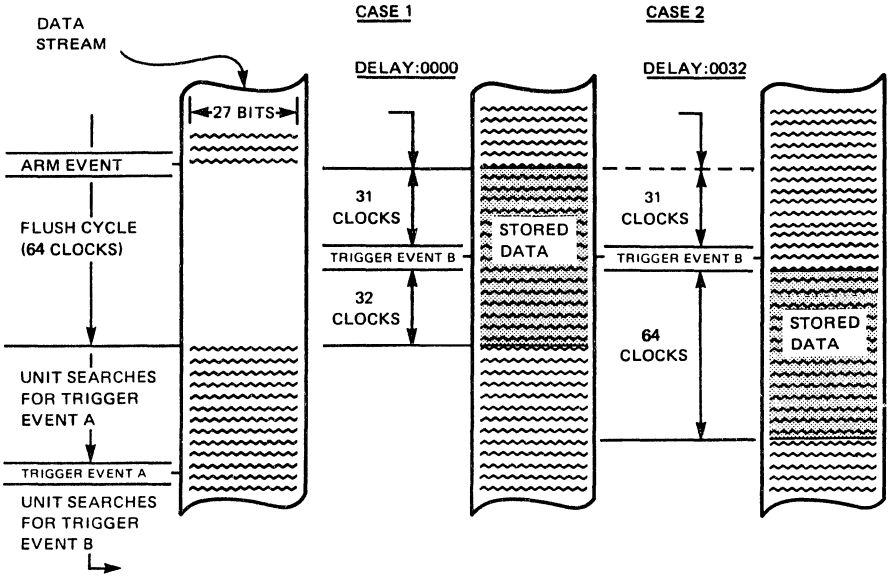


Figure 3.1. Illustration of Delay by Clocks. Case 1: DLYC = 0000. Case 2: DLYC = 0032 (range: 0-9999 Decimal). This feature allows you to slide the memory window downstream of the trigger event.

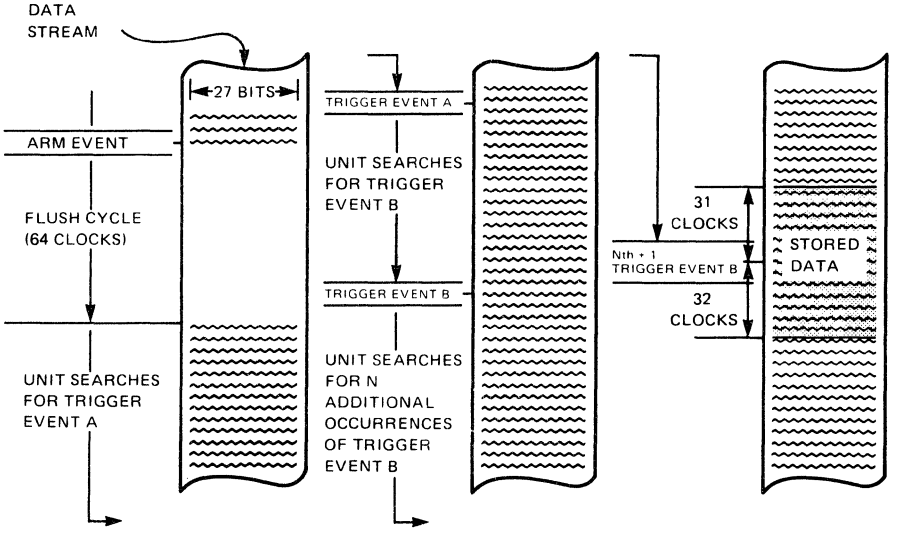


Figure 3.2. Illustration of Delay by Events (DLY E) = N (range: 0-9999 Decimal). This feature allows you to isolate specific iterations of a loop in your program.

and records one word for each clock cycle from the system under test. The unit has three clock qualifiers, however, that can effectively change and redefine the clock cycles used for a recording. The first parameter you can select is the active edge of the record clock, either rising or falling. The second parameter involves the binary specification of the two clock qualifier lines (CQA and CQB) to validate only certain desired clock cycles. The two qualifier lines can be attached to any TTL level signals, the desired binary state specified, and they will combine with the system clock to produce a new qualified record clock. If these lines are not used for a recording, you should be sure that they are held high to prevent unintentional qualifying of the record clock via crosstalk The proper keystroke sequence for modifying the clock qualifiers is shown in the flowchart guide.

To help clarify your understanding of clock qualifiers, see Figure 3.3. It illustrates the creation of a new qualified record clock.

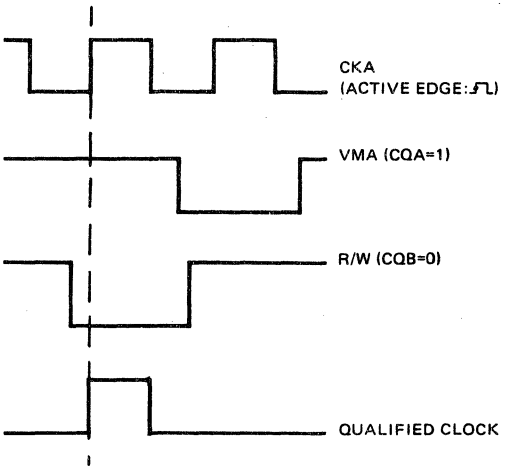


Figure 3.3 Illustration of Selective Qualification of the Record Clock. This feature allows you to achieve effective data compression by eliminating unwanted or repetitive data from a recording.

The three parameters selected are as follows: active edge = rising edge, CQA = 1, and CQB = 0. The lines selected for the illustration are typical of the Motorola 6800 microprocessor.

3.6.5 Nested Triggering

The 2710 has a two-stage combinational trigger (Trigger A and Trigger B), which is used to initiate a recording whenever the two are found sequentially after the Arm button has been pressed. Both triggers are fully definable as 27-bit words composed of ones, zeros, or don't cares. The triggers can be entered in either hex, octal, or decimal number bases. Each trigger is divided into a 16-bit address field, an 8-bit data field, and three binary qualifier bits. See the flowchart guide for the appropriate keystroke sequence governing these entries. Notice that if nested triggering is selected then Trigger A, Mask A, Trigger B, and Mask B must all be specified.

The nested triggering feature allows fairly easy access to otherwise difficult-to-isolate data such as triggering into specific executions of subroutines.

An illustration of the sequences involved in nested triggering is given in Figure 3.4. For simplicity, it assumes that no delays were specified.

3.6.6 Single Triggering

Often you will only require a single trigger specification to capture the desired data. In these cases, simply enter the trigger word into Trigger B and ignore Trigger A. On power up condition, Trigger A and Trigger B are both in an automatic default mode. See Table 3.2. Unless you have used Trigger A and entered some meaningful mask for it, the unit will pass immediately to Trigger B and begin searching for the single trigger you've specified. All other parameter specifications, such as delay by clocks, inversion masking, etc. may still be used if desired.

3.6.7 Masking

Once you have entered a trigger word

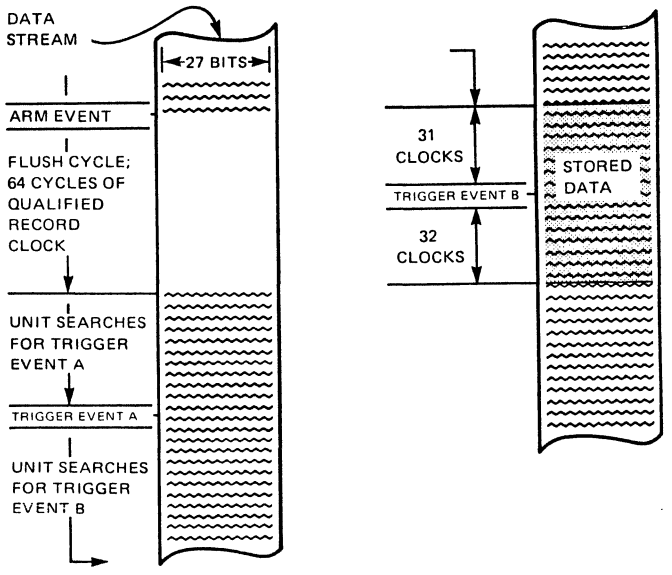


Figure 3.4. Illustration of Nested Triggering. This feature allows you easy access to otherwise difficult-to-isolate data by making it simple to trigger into specific subroutines in your program.

the concept of masking must be employed to tell the instrument which of the lines that compose the trigger word are actually of concern to you. Unless an appropriate mask is entered, the unit will assume that even though you've entered a trigger word, you really don't care whether or not any of the lines are what your trigger word specified. This feature allows you to record full 27-bit words while triggering from your own selection of any or all of these bits.

Both Trigger A and Trigger B have their own complete and separate masks. These masks, MSK A and MSK B, are entered in a manner identical to the entry of a trigger word; two address fields, one data field, and three separate binary qualifier bits. For the specified logic state of a line to actually become part of the trigger word, you must enter a one in the corresponding line of the trigger word's mask. Thus, with a pencil and paper, or conversion tables, you can enter hex, octal, or decimal characters into the unit, but specify down to the bit level which lines become part of the trigger. If you want one character in the trigger word to remain an "X" or Don't Care, simply leave the portion of the mask pertaining to that character equal to zero. See Examples 1 and 2.

3.6.8 Inversion Masking

Occasionally, you will probably find it necessary to connect the 2710 to a portion of a bus or other device where the normally positive logic sense of one or all of the lines has been inverted so that the ones are logic lows and the zeros are logic highs. Naturally, if left uncorrected, this inverted or negative logic would result in erroneous or missing trigger words, as well as an incorrect display. Because of the 2710's inversion masking capability, these situations can be easily rectified via a series of keyboard entries identical in form to the entry of a trigger word.

EXAMPLE 1. Full character masking provides the simplest case. Suppose that you had entered the hex number 0C00 for the address portion of Trigger A, but would rather trigger from 0CXX. That is, you don't care what states the lines associated with the least significant byte of the address are in for Trigger A. The proper mask to enter would be FF00 as can be seen below.

	A15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRG A (binary)	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
(hex)		0				C				0			0			
MSK A (binary)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
(hex)		F				F				0			0			
Result (binary)	0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X
(hex)		0				C				X				X		

The 2710 will now recognize any occurrence of the hex number 0C in the upper address byte as the complete address portion of Trigger A, regardless of what states the lines of the lower address byte are in at that time.

EXAMPLE 2. Bit-level masking is easy to accomplish with the 2710 by using the appropriate data mask. Suppose that you have specified the hex number 13AB for the address portion of Trigger B and the unit has failed to find this trigger. After some investigation, you conclude that unavoidable crosstalk may be occurring on input line A1. To check this possibility, you can mask out this single line so that the 2710 will trigger from the other lines and disregard the state of line A1. The proper mask to enter would be FFFD as can be seen below.

	A15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRG B (binary)	0	0	0	1	0	0	1	1	1	0	1	0	1	0	1	1
(hex)		1				3				A				B		
MSK B (binary)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
(hex)		F				F				F				D		
Result (binary)	0	0	0	1	0	0	1	1	1	0	1	0	1	0	X	1
(hex)		1				3				A			B or 9			

The 2710 will now recognize either hex number 13AB or 13A9 as the address portion of Trigger B. Only the state of line A1 has been disregarded. Masking works in the same fashion with hex, octal, or decimal notation, and it applies to the data and trigger qualifier channels just as it does to the address channels that were used in the examples.

In the inversion mask, any place a ONE appears, that channel is inverted. To determine the proper inversion mask, assign each inverted line a one and each normal line a zero. Group the lines into their corresponding address, data, and qualifier sets, convert the address and data sets into the same number base you will use for the recording, and enter the resultant mask just as you would a trigger word. From then until you enter a new inversion mask or turn off the unit, you can make any number of recordings from a partially or fully inverted bus just as though all the lines were normal and compare the resultant memory contents with your program listing directly. See Examples 3 and 4.

3.7 Making a Recording (Record Mode)

Once all of the recording parameters have been specified satisfactorily (or not at all if you just want to make a blind recording for some reason) you begin a recording by pressing the Arm Button. This will initiate a predetermined sequence of events beginning with a flush cycle that will last for the next 64 clock cycles, ensuring that the memories will all be loaded with fresh data. The unit will then search for Trigger Event A, Trigger Event B, count out the trigger delay specified, add a final 32 clock cycles of post-trigger information, stop recording, and automatically transfer itself into the Memory mode so that the recording can be reviewed. If you have the Clock Delay set to 0000, location 31 will show Trigger Event B. If you have used Event Delays, then location 31 will contain the Nth + 1 event of Trigger B. Either way, the unit will initially display the contents of memory location 31.

Most of the time, all of the above will occur so quickly that all you will see on the display after pressing the Arm button is the resultant memory display. Should this transfer to the memory mode not occur, however, one of five alphabetic prompting aids will show on the left side of the display, above the delay field, to tell you in a general way what the unit is doing. An explanation for each of the five messages is given on the far right-hand side of Figure 3.5. You can use this information to decide whether to just wait awhile longer, to manually input Event A or Event B via their respective buttons, or to abort the recording by pressing the STOP button. The use of any of these three buttons to force the completion of a recording will, of course, mean overriding certain or all of the recording parameters that you specified prior to arming the unit. Therefore, you must consider the particular circumstances in light of your requirements to decide what value, if any, the resultant recording would have for analysis purposes. Often, you will find that even a partial recording will have some use in that it may contain the information necessary to further isolate the problem so that a more complete recording can be made if desired.

3.8 Reviewing a Recording (Memory Mode)

As noted earlier, once a recording has been completed, the unit automatically transfers into the Memory Mode and displays memory location 31. When you have reviewed this word, you can either scroll forward (STEP) to view the next word above, memory location 32, backwards (BCK ST) to view the preceding word below, memory location 30, or you can jump directly (GO TO memory location, ENTER) to any of the 64 words in memory. From the next location you have the same choices as before. You can continue along these lines indefinitely until you've reviewed the full memory to your satisfaction. For a further convenience, you can change the display format from one number base to another at any time without actually disturbing the contents of the data in memory. See Figure 3.5 for the appropriate keystroke sequences to manipulate the memory display as described above.

3.9 Using the Model 2710 as a Calculator (Calculate Mode)

As a final convenience feature, the 2710

EXAMPLE 3. Suppose that you have attached the 2710 leads associated with the data and trigger qualifier channels to points where normally positive logic is available. At the same time you have found it was necessary to attach the leads associated with the address channels to a bus where the logic sense of all the lines is inverted. This full address inversion can be easily corrected by entering the hex inversion mask FFFF for the address portion of the data at any time before making a recording. This process is illustrated below.

	A15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Line Logic	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
I MSK (binary)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
(hex)		F				F				F				F		
Result New Logic	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+

The 2710 will now execute the correct trigger searches and will record data from the inverted lines just as though the logic sense from these lines was as normal as it is from the data and trigger qualifier lines. The entire recording should now correspond directly to the appropriate portion of your program listing.

EXAMPLE 4. Bit-level inversion masking is also easy to accomplish with the 2710 by using the appropriate inversion mask. Suppose that you have attached all of the 2710 leads to points where normally positive logic is available except for address input A3, which is connected to a negative logic point. This single line, or bit level, address inversion can be easily corrected by entering the hex inversion mask 0008 for the address portion of the data at any time before making a recording. This process is illustrated below.

	A15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Line Logic	+	+	+	+	+	+	+	+	+	+	+	+	-	+	+	+
I MSK (binary)	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
(hex)		0				0				0				8		
Result New Logic	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+

The 2710 will now "see" all of the input lines as having a normal (positive) logic sense so that recordings will directly match the appropriate portion of your program listing. Inversion masking can be done in either hex, octal, or decimal notation. It is used with the data and trigger qualifier channels just as it was used with the address channels in the examples.

has the capability to perform both addition and subtraction in either hex, octal, or decimal bases. The 2710 can also perform direct radix conversion between these bases to facilitate determining relative addresses and program offsets. See Figure 3.5 for the appropriate keystroke sequences.

An illustration of how relative addressing works and of how the 2710 Calculate mode can be useful is provided.

Problem

Store 128 data values, starting at memory location 5C22.

What is the ending location?

Solution

Use 2710 Calculate mode.

Turn unit ON.

Enter mode by pressing CALC.

Note, it is not necessary to specify the HEX format initially since the unit powers up in this condition.

The LED display should show four zeros, followed by six dots (HEX, CALC).

Key in 5C21. Press GO TO, DEC. LED shows blinking 23585, the decimal equivalent of 5C21, followed by five dots (DEC, CALC).

Press +, and Key in 128. LED shows blinking 00128.

Press =, and read 23713, the ending location in decimal.

Press GO TO, HEX, and LED reads 5CA1, the ending location in hex, followed by six dots (HEX, CALC).

FLOWCHART GUIDE TO OPERATING THE MODEL 2710 LOGIC ANALYZER

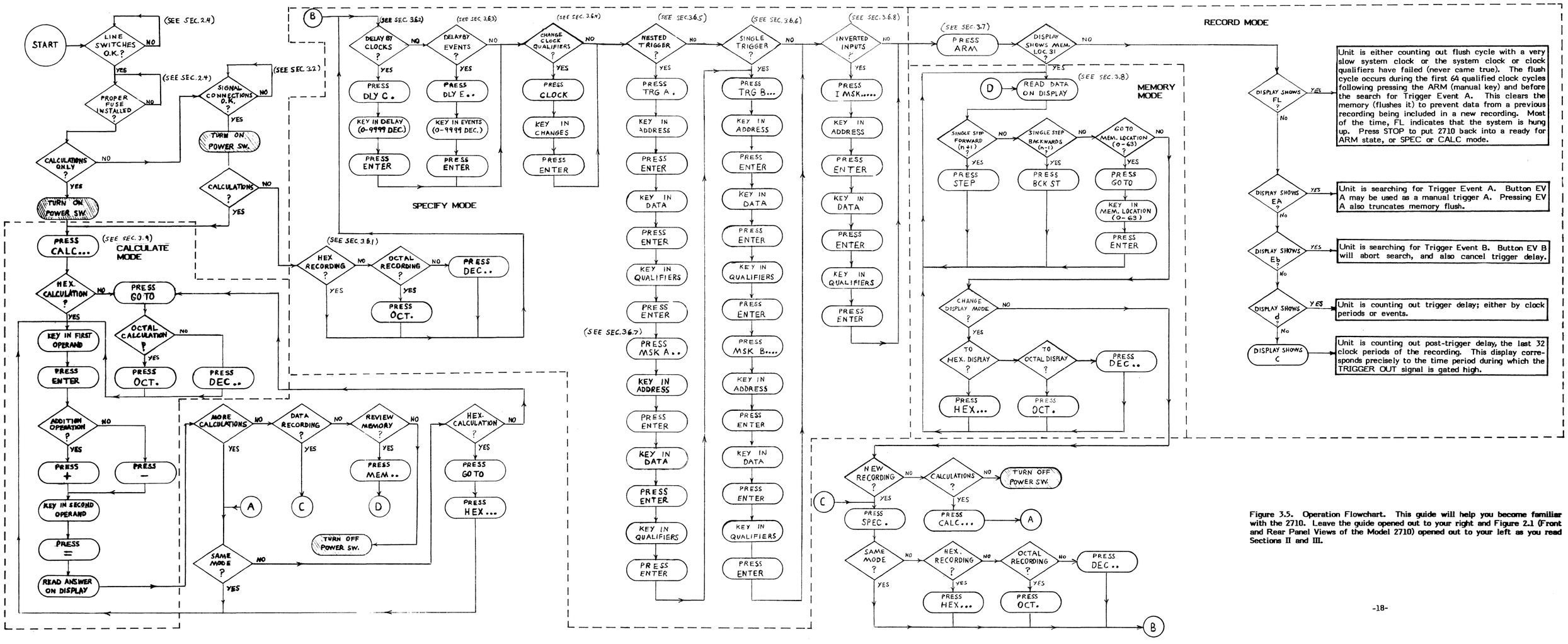


Figure 3.5. Operation Flowchart. This guide will help you become familiar with the 2710. Leave the guide opened out to your right and Figure 2.1 (Front and Rear Panel Views of the Model 2710) opened out to your left as you read Sections II and III.

SECTION V

PRINCIPLES OF OPERATION

4.1 Introduction

This section is divided into two parts. The first part gives a block diagram description of the instrument and the second part gives a detailed treatment of the theory of circuit operations.

4.2 Basic General Description

As can be seen in Figure 4.1, the 2710 block diagram has two main parts, the microprocessor circuitry and the record electronics. The microprocessor circuitry, which includes the display, the keyboard and the microprocessor, controls the operation of the record electronics and the operator interface. The record electronics, which includes the Input Buffer Register, Clock Circuit, Trigger Memory, Record Memory, Trigger Delay Counter, and Record Electronics Controller, implement the collection of the data from the system under test in the manner specified by the operator. The individual blocks of the 2710 are actually quite simple in design.

4.2.1 Keyboard

The keyboard contains 24 keys or switches positioned in a four by six matrix for input of data and control commands.

4.2.2 Display

The 2710 has a hexadecimal plus decimal LED display for output of status and data.

4.2.3 Microprocessor Circuitry

The microprocessor receives commands from the keyboard, outputs status and data to the display and controls the record electronics.

4.2.4 Input Buffer Register

The input buffer receives the data from the system under test and holds it stable for the trigger circuit and record memory.

4.2.5 Trigger Circuit

The trigger circuit detects the combination of input signals specified as Event A and Event B.

4.2.6 Record Memory

The record memory stores the data from the system under test.

4.2.7 Clock Circuit

The clock circuit selects the active edge of the system-under-test (SUT) clock and provides the delayed and qualified clock to the record electronics.

4.2.8 Trigger Delay Counter

The trigger delay counter counts the number of delayed and qualified SUT clocks and/or "Event Bs" to determine the correct time to end a record cycle.

4.2.9 Record Electronics Controller

The record electronics controller controls the recording sequence by receiving inputs from the microprocessor and record electronics and outputting the record cycle status to the record electronics and microprocessor.

4.2.10 Power Supply

The power supply converts the utility power source to 5 VDC for the 2710's circuits.

4.3 Detailed Description

4.3.1 Clock Circuit

The clock from the system under test comes in on pin 43 and is buffered by U59-18 and U54-18. If a rising edge clock is selected, U59-18 is enabled. The buffered SUT clock

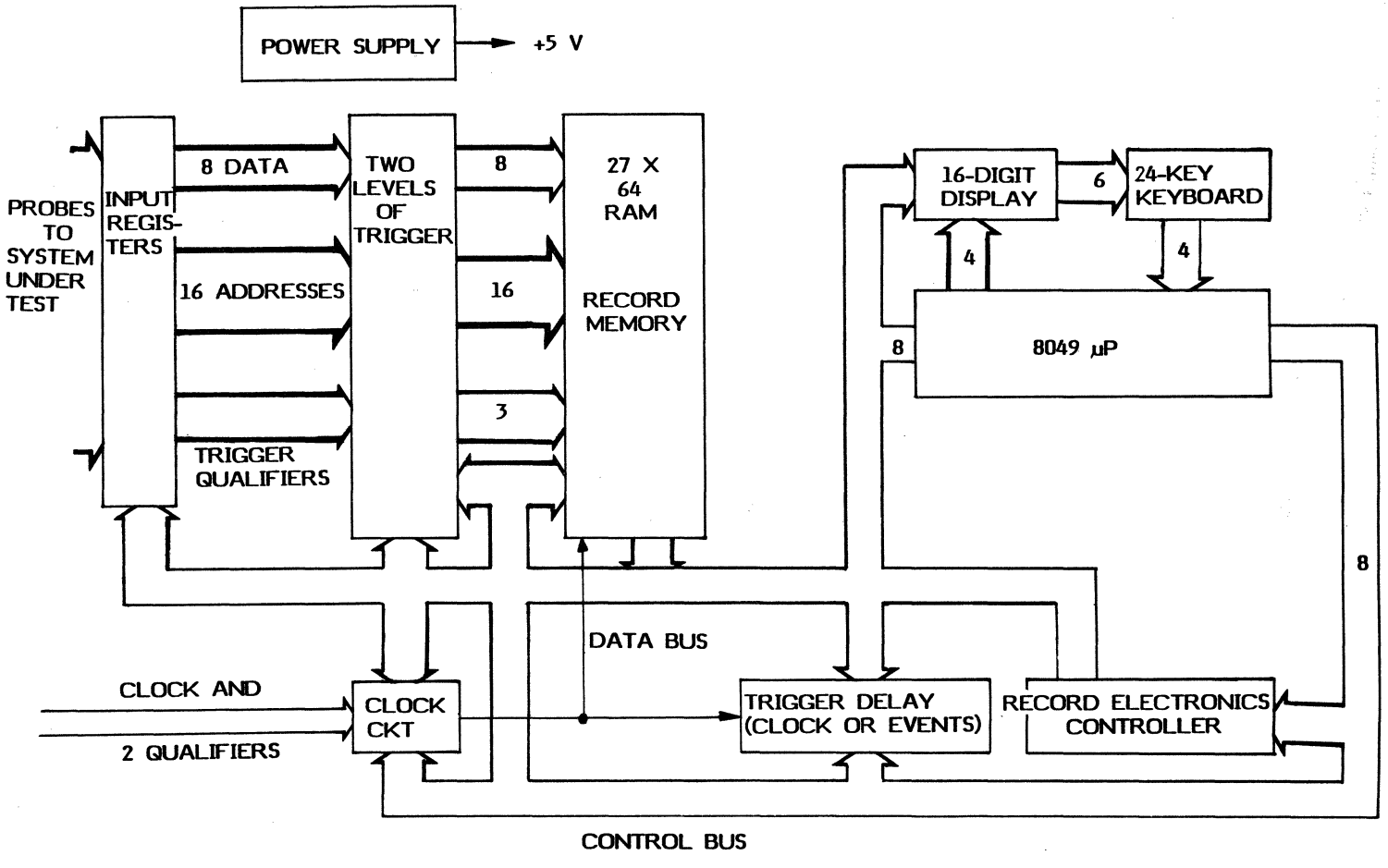


Figure 4.1 2710 Block Diagram

clocks the input registers and is delayed by U53. See Figure 4.2.

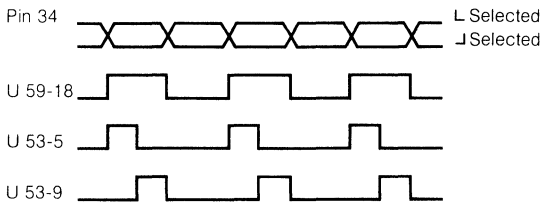


Figure 4.2 Clock Circuitry

The delayed record electronics is synchronized by the delayed system clock U53-9.

4.3.2 Input Buffer Circuit

The DATA, ADDRESS, TRIGGER QUALIFIERS and CLOCK QUALIFIERS are buffered and delayed by 74LS244's Schmitt trigger gates. The delayed outputs are connected to the preset inputs of the 74LS161, counter-registers U44, 45, 46, 47, 55, 56, 57, and U58.

During a recording cycle, the SUT inputs are clocked into the 74LS161's by the buffered SUT clock. The enabling condition of the two clock qualifiers is selected by U43-8 and U43-11. If clock qualifiers A and B are correct, the delay clock is enabled through U51-6 and U51-8. Prior to a recording cycle, the 74LS161 input registers are used as address counters for the trigger circuitry.

4.3.3 Trigger Circuit

The DATA, ADDRESS and TRIGGER QUALIFIER outputs of the input registers are coupled to the Trigger Circuit. Prior to a recording cycle, the microprocessor loads the trigger memory with triggers A and B. The input registers are reset through U1-3, and set to count mode through U19-2. The outputs of the input registers are now addressing bit "0" in each random access memory of the trigger memory. If the corresponding 7 bits from the SUT produce trigger A, a "one" will be placed on the data input of the RAM (U33, 34, 35 or 36) and clocked in by U52-6. The same clock also advances the input register to trigger memory location 1, where the second 4-bit trigger word will be loaded.

After 128 locations have been written, U45-11 goes high and the microprocessor proceeds to load Trigger B into the RAMs. After the trigger memory is loaded, the Input Registers are switched back to load mode by U19-2.

During the record cycle, initially the Trigger A part of the Trigger RAMs is selected. Each 7-bit group of outputs from the Input Registers selects (or reads) a bit in the corresponding RAMs. If all of the selected bits are "ones," the output is pulled high by R16 and is clocked into the Trigger A memory (U40-9) by the delayed and qualified SUT clock. After Trigger A has been detected, the Trigger B portion of the trigger RAM is selected by U37-3. When Trigger B is detected, it is clocked into U40-5.

4.3.4 Record Memory

The DATA, ADDRESS and TRIGGER QUALIFIER outputs of the input registers are also coupled to the data inputs of the Record Memory, U23, 24 and U25. Prior to the record cycle, the record memory address counters U15 and U16 are reset by U1-3. During the flush cycle (which may be disabled by cutting the input to U38-8 and tying U38-8 to +5 V), each qualified and delayed clock writes the output of the input register into the record memory and advances the address counter. When the address counter has been clocked 64 times, U16-12 goes high signaling the end of the flush cycle. Recording continues until the trigger delay counter signals the end.

After the record cycle, the microprocessor can access the contents of the record memory by stepping the address counter to the desired word and reading the contents through U14 and U22.

4.3.5 Trigger Delay Counter

Before a record cycle starts, the trigger delay counters U10, 11, 17 and 18 are loaded by the microprocessor. U17 and U18 are

loaded from the data bus by U1-11 and U10, and U11 is loaded by U1-8. During the record cycle, the Trigger Delay Counter starts counting and is incremented by each delayed and qualified clock through U31-6. In the delay by events mode the trigger delay counter is incremented by the delayed and qualified clock each time Trigger B is detected. The trigger delay counter is incremented until U11-11 goes high, signaling the middle of the "record window." Then the trigger delay counter is further incremented 32 times by the delayed and qualified clock until U18-13 goes high, signaling the end of the record cycle.

4.3.6 Record Controller

The recording cycle is controlled by record controller U37 and associated gates. Cross-coupled latches A (U26-8 and U26-6), B (U26-12 and U27-13), and C (U39-13 and U39-1) remember the current state of the recording cycle. Decoder U37 decodes the current state and enables the gates to detect the event that advances the latches to the next state. The record controller can be advanced by either the record electronics or by the microprocessor. The record controller is described in Table 4.1. The microprocessor observes the state of the record controller through U22 and outputs it to the display so that the operator will know what the record electronics is doing.

4.3.7 Display and Keyboard

The display and keyboard circuit is located on a separate PC board mounted to the

Table 4.1 Record Controller

Latched State	Description	Decoder Output Active Pin	Signal Required to Address to this State		Display Contents
			Record Electronics	Microprocessor	
CBA					
000	Reset	1	None	Push Arm, U19-2	(Blank)
001	Armed	2	None	Push Arm, U19-2	FL
011	Flushed	4	U16-12	Push EV A or Stop, U19-5	EA
010	A Triggered	3	Trigger A, U40-9	Push EV A or Stop, U19-5	Eb
110	B Triggered	7	Trigger B, U40-5	Push EV B or Stop, U19-6	d
111	Delay Counted	9	End of Delay, U11-11	Push EV B or Stop, U19-6	c
101	EOR	6	End of Delay, U18-13	Push Stop, U19-9	Contents of location 31
100	(Not Used)	--	--	--	HU*

*Indicates an error condition.

top cover of the 2710. The display consists of 16 seven-segment plus decimal point characters. The microprocessor illuminates one of the characters by outputting the binary code of the character to be illuminated to decoders U1 and U2, writing ones in the required pattern to segment register U3. It then writes all zeros to the segment register to turn off the character before advancing to the next one. Each character is illuminated approximately 100 times per second. If a key is depressed, a zero will occur on one of the keyboard output lines to U6-31, 32, 33 or 34. The microprocessor determines which key was depressed by knowing which character is being displayed and which keyboard output line is low. If two keys are depressed, the processor will not recognize either one.

4.3.8 Microprocessor Circuit

Several microprocessors may be used in the 2710. Table 4.2 shows what external support circuits are required for each one.

Table 4.2
Microprocessor Support Circuits

Microprocessor (U6)	Read Only Memory (U21)	Read Write Memory (U12 and U13)
8049	--	--
8748	2716	2111
8036	2716	2111
8039	2716	--

The microprocessor circuits reads the keyboard, displays data and control information through the display and controls the record electronics. The control program is contained in either the microprocessor or the 2716, and the data are contained in either the microprocessor or the 2111. The data from a record cycle is always retained in the record memory.

The microprocessor controls the display and keyboard through P1-0 to P1-7 as described in that section. The microprocessor controls the record electronics through the data bus and P2-0 to 7. P2-0 to 7 are used as enables to select which portion of the electronics is affected by the microprocessor. Table 4.3 lists the functions of these pins.

Table 4.3 Pin Functions

Port 2, Pin	Function
0	Loads trigger memory and increments trigger address.
1	Loads low byte of trigger delay counter.
2	Loads high byte of trigger delay counter.
3	Enables read-write memory U12 and 13 (active low).
4	Reads record memory and increments record memory address.
5	Loads record control register.
6	Loads segment register in display circuit.
7	Resets record control register and trigger address counter.

The microprocessor controls the record electronics primarily through the record control register (U19). The functions of the pins of U19 are listed in Table 4.4.

The microprocessor is initialized by C6 when power is turned on. Crystal CR1 with C8 oscillate at 6 MHz to supply the microprocessor with a clock.

4.3.9 Power Supply

The 2710 uses only a 5 V power supply. Utility grade power is supplied through a standard line cord to a fuse mounted in the bottom pan. From the fuse the line voltage is switched on and off by a switch on the right side of the bottom pan near the rear of the 2710. Line voltage switches on the rear panel switch the primaries of the power transformer to allow operation from 100, 120, 200 and 240 V sources. The output of the transformer is

fullwave rectified by CR2 and filtered by C50. LM323 (mounted on the rear panel) regulates the voltage on C50 to 5 V.

Table 4.4 Functions of the Pins of U19

Record Control Register (U19)	Function
1Q	Sets input register to LOAD or COUNT.
2Q	Simulates Event A.
3Q	Simulates Event B.
4Q	Stops the record process.
5Q	Sets delay counter to delay by clocks or events.
6Q	Enables rising or falling edge clock.
7Q	Sets clock qualifier A for high or low.
8Q	Sets clock qualifier B for high or low.

SECTION V

CALIBRATION PROCEDURES

5.1 Recalibration of Internal Circuits

The following calibration procedure is to be used in recalibrating the internal circuits of the Model 2710. The unit was calibrated prior to shipment and should not require any recalibration for at least six months or 1000 hours of operation.

5.2 Required Test Equipment

The following test equipment are required to calibrate the Model 2710.

1. 250 MHz Oscilloscope (Tektronix 475A).
2. Digital Voltage Meter (Dana 4200).
3. Two Pulse Generators (Tektronix PG502 or equivalent.)

5.3 Power Supply Verification

Refer to Figure 5.1 while performing the following procedure.

Remove the top cover of the 2710 via six screws located on the bottom pan. Turn on the power to the 2710 and verify that it is +5 on the Main Board PCB at connector pin J3-49, 50.

The acceptable range is +4.75 to +5.25 VDC.

5.4 Adjustments

Unless otherwise specified, the following connections are to be maintained.

a. Connect a 1-MHz TTL clock to I/O pin 43, CLK A on cable assembly.

b. With the scope probe, monitor IC53 (pin 5) for 40 ns ±2 ns positive-going pulse; adjust R18 to obtain the desired results.

c. In a similar manner, adjust R17 to obtain 20 ns ±2 ns positive-going pulse on IC53 (pin 9).

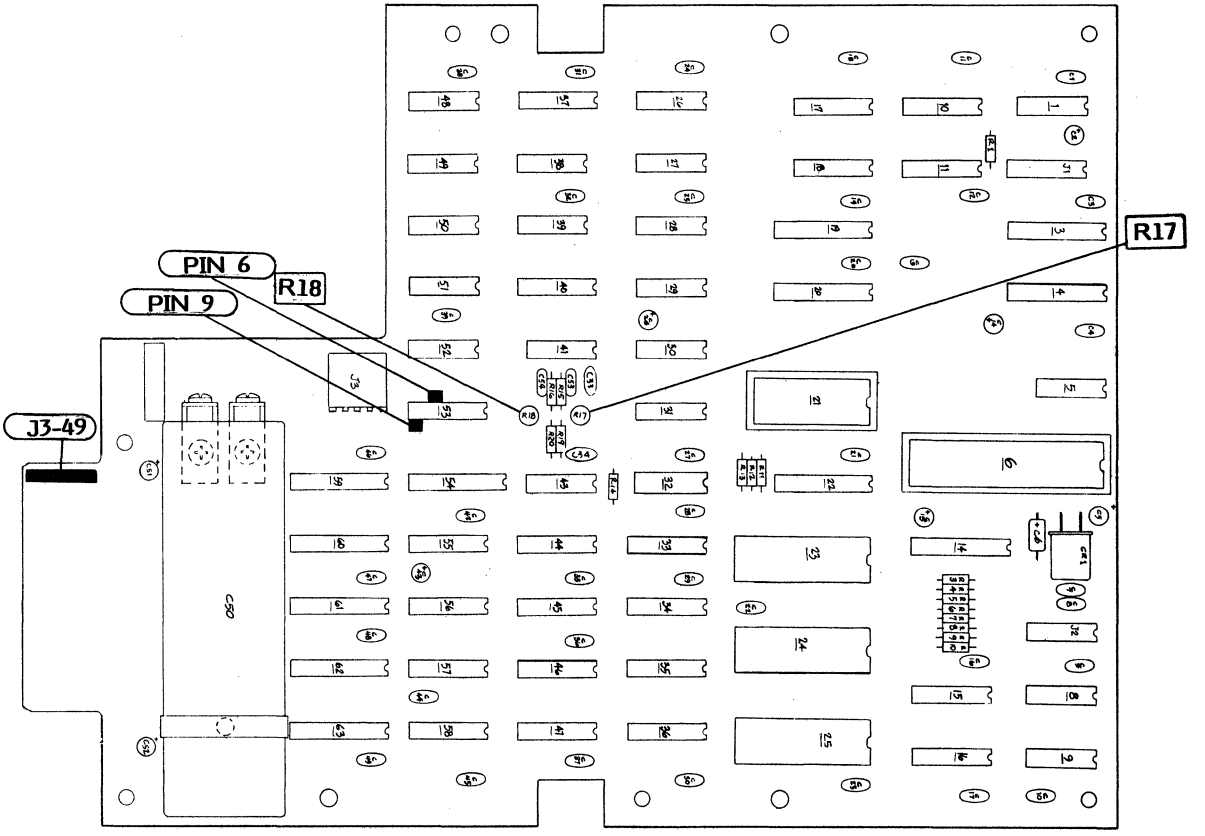


Figure 5.1 Main Board Voltage Chart

SECTION VI

MAINTENANCE

6.1 Introduction

This section covers the 2710 diagnostic routine. Repair to the main board can be performed with the aid of the technical description in Section IV as well as the diagnostic chart in Section 6.3.

The drawings in Section VII have been included to aid service personnel who wish to troubleshoot to the component level. Additional assistance regarding a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

6.2 Keyboard Checkout, Verification

The following procedure exercises the microprocessor and its associated RAM and ROM components. Step 6.2.2 initially checks most of the microprocessor circuitry in the 2710. If dots appear as specified, continue; if not, then verify the operation of the microprocessor to the keyboard circuits. There is a built-in time delay for POWER ON RESET. **Please allow 1 minute before reinitializing the 2710 for turn-on!**

6.2.1 Connect the 2710 input cable pin "CLK A" to a 1-MHz TTL clock source. Turn clock source off until step 6.2.20

6.2.2 Turn on the 2710. Verify that the LED display shows three dots under the "DATA" column and one under the "QUAL."

6.2.3 Press "MEM"; verify that there are two dots under "QUAL" (Ignore characters).

6.2.4 Press "CALC"; verify that there are three dots under "QUAL."

6.2.5 Press "GO TO." Press "OCT"; verify that there is one dot under "DATA."

6.2.6 Press "GO TO." Press "DEC"; verify that there are two dots under "DATA."

6.2.7 Press "SPEC" and "TRIG A"; verify that there is one dot under "ADDRESS."

6.2.8 Press "SPEC" and "MSK A"; verify that there are two dots under "ADDRESS."

6.2.9 Press "SPEC" and "TRIG B"; verify that there are three dots under "ADDRESS."

6.2.10 Press "SPEC" and "MSK B"; verify that there are four dots under "ADDRESS."

6.2.11 Press "SPEC" and "GO TO"; verify that there are five dots under "ADDRESS."

6.2.12 Press "SPEC" and "DLY C"; verify that there is one dot over "DELAY."

6.2.13 Press "SPEC" and "DLY E"; verify that there are two dots over "DELAY."

6.2.14 Press "CLEAR"; verify that the display under "MEM LOC" is "000.-."

6.2.15 Press "CLEAR" again; verify that a single hyphen is at the first location.

6.2.16 Press "ENTER"; verify that the display returns to "000.0."

6.2.17 Press "ARM"; verify that the display shows "FL" blinking at left.

6.2.18 Press "EV A"; verify that the display shows "Eb" blinking at left.

6.2.19 Press "STOP"; verify that the display shows "31" under "MEM LOC."

6.2.20 Press "ARM" and turn on the 1-MHz clock source to pin 43. Verify that the display shows "31" under "MEM LOC"; five under "ADDRESS"; three under "DATA" and "111" under "QUAL."

6.2.21 Press "OCT"; verify that there are six characters under "ADDRESS."

6.2.22 Press "HEX"; verify that there are four characters under "ADDRESS" and two under "DATA."

6.2.23 Press "SPEC" and "CLOCK"; verify that "L11" is blinking over "CLOCK."

6.2.24 Press "J"" (1 key) three times; verify that "J11" is blinking.

6.2.25 Press ""L" (0 key) three times; verify that "L00" is blinking.

6.2.26 Press "MEM"; verify that there is a full display with "31" under "MEM LOC."

6.2.27 Press "STEP"; verify that "32" is under "MEM LOC."

6.2.28 Press "BCK ST"; verify that "31" is under "MEM LOC."

6.2.29 Press "CALC," "0," "1," "2," "3," ---"F." Verify that the appropriate character is displayed for each key.

6.2.30 Press "GO TO," "OCT," "0," "1," "2," "3," "4," "5," "6," and "7." Verify display as above. Verify that characters 8-F are not displayed.

6.2.31 Press "GO TO," "DEC," "CLEAR," "CLEAR," "1," "2," "3," "4," and "5." Verify proper display.

6.2.32 Press "CLEAR," "CLEAR," "6," "0," "8," "9," and "7." Verify proper display.

6.2.33 As above, verify that characters A-F are not valid and that numbers greater than 65535 cannot be entered.

6.2.34 Press "CLEAR," "CLEAR," "6," "5," "5," "3," "5," "+," "1," and "=."

6.2.35 Verify that display shows "00000."

6.2.36 Press "0," "-," "1," and "=." Verify that display shows "65535."

6.2.37 Press "GO TO" and "OCT." Verify that display shows "177777."

6.2.38 Press "GO TO" and "HEX." Verify that display shows "FFFF."

NOTE: The following steps check out the record memories of the 2710. Note that Section 6.3 describes a more thorough checkout of the high-speed record circuitry.

6.2.39 Tie all Data and Address input lines to a TTL low; tie the R/W line and the TQA, TQB line to a TTL logic high.

Press the following sequence of keys for the next five steps.

"ARM", "EV A", "EV B", "STOP."

6.2.40 Remove Data line 0 and tie to logic 1; press the above keys. Verify display

0000-01-111.

Remove Data line 1 and tie to logic 1. Verify 0000-03-111.

Remove Data line 2 and tie to logic 1. Verify 0000-07-111.

Remove Data line 3 and tie to logic 1. Verify 0000-0F-111.

Remove Data line 4 and tie to logic 1. Verify 0000-1F-111.

Remove Data line 5 and tie to logic 1. Verify 0000-3F-111.

Remove Data line 6 and tie to logic 1. Verify 0000-7F-111.

Remove Data line 7 and tie to logic 1. Verify 0000-FF-111.

6.2.41 Remove Address lines for the following steps and follow the same procedure outlined above.

Add 0 high. Verify 0001-FF-111.

Add 1 high. Verify 0003-FF-111.

Add 2 high. Verify 0007-FF-111.

Add 3 high. Verify 000F-FF-111.

Add 4 high. Verify 001F-FF-111.

Add 5 high. Verify 003F-FF-111.

Add 6 high. Verify 007F-FF-111.

Add 7 high. Verify 00FF-FF-111.

Add 8 high. Verify 01FF-FF-111.

Add 9 high. Verify 03FF-FF-111.

Add 10 high. Verify 07FF-FF-111.

Add 11 high. Verify 0FFF-FF-111.

Add 12 high. Verify 1FFF-FF-111.

Add 13 high. Verify 3FFF-FF-111.

Add 14 high. Verify 7FFF-FF-111.

Add 15 high. Verify FFFF-FF-111.

6.2.42 Remove R/W line and tie to a logic "0."

Verify FFFF-FF-011.

6.2.43 Remove TQA line tie to a logic "0."

Verify FFFF-FF-001.

6.2.44 Remove TQB line and tie to a logic "0."

Verify FFFF-FF-000.

6.3 Functional Checkout

The following steps check out the high-speed record circuitry of the 2710.

Note the following chart (Table 6.1) describing the circuitry involved for each step. Refer to the main board schematic for each step.

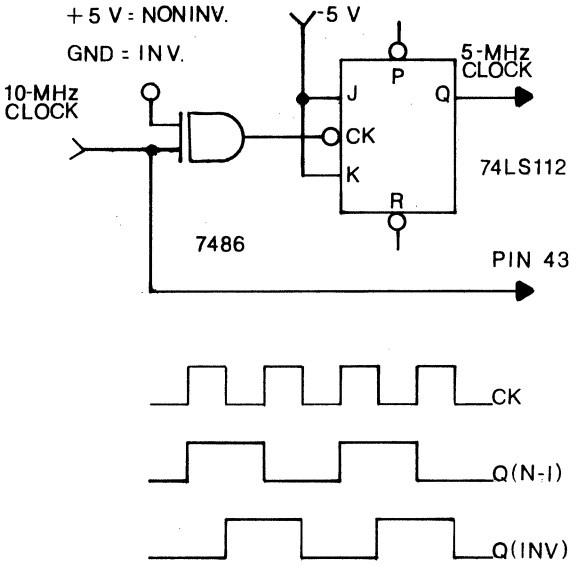
Table 6.1 Circuitry Chart

STEP NO.	DESCRIPTION and CIRCUITRY
6.2.39-6.2.41	Input latches, trigger detect memory, high-speed record RAM (27x64), asynchronous controller, clock circuit.
6.2.42-6.2.44	Clock qualifier check out.
6.3.2-6.3.5	Trigger qualifier check out. ICs 41, 53 and latches.
6.3.6	Clock delay check out. Trigger delay counters and associated circuitry.
6.3.7	Event delay check out. Trigger delay counters and associated circuitry.

6.3.1 Turn 2710 power OFF. Input a 10-MHz square wave into "CLOCK A" (I/O pin 43).

Synchronize the second pulse generator to the 10-MHz generator. Set the output rate to 5 MHz (TTL level).

NOTE: The following circuitry will accomplish the same purpose as the second pulse generator.



6.3.2 With the 5-MHz signal's rising edge lining up to the 10-MHz clock's rising edge, input the 5-MHz clock to I/O pins 10 and 37.

SPECIFY [TRIG] B 0001-00-000

[MASK] B 0001-00-000

[CK] ∫ 11

[ARM]; Verify display of 31. XXX1-XX-XXX in all memory locations.

6.3.3 Convert the rising edge of the 5-MHz clock to correspond to the falling edge of the 10-MHz clock.

SPECIFY [CK] ⌊11

ARM; verify display of 31. XXX1-XX-XXX in all memory locations.

6.3.4 Input the 5-MHz clock into I/O pin 38.

Repeat step 6.3.2.

6.3.5 Repeat step 6.3.3.

6.3.6 Remove clocks from 2710. Input a 1-Hz TTL clock into I/O pin 43.

SPECIFY [TRIG B] 0000-00-000

[MASK B] 0000-00-000

[DLC 0010]

[ARM], [EVA], [EVB] display XXXX-XX-XXX

Verify that display occurs 10 s after pushing event B button.

6.3.7 Speed up clock to I/O pin 43 to 10 MHz. Set pulse generator to manual pulse. Input to pin 10 of I/O connector.

SPECIFY [TRIG B] 0001-00-000

[MASK B] 0001-00-000

[EV DELAY] 0010

[ARM]. Manually pulse the generator. Verify that display occurs after 11 pulses.

This completes the functional check of the Model 2710.

SECTION VII

SCHEMATICS AND ASSEMBLY DRAWINGS

7.1 Introduction

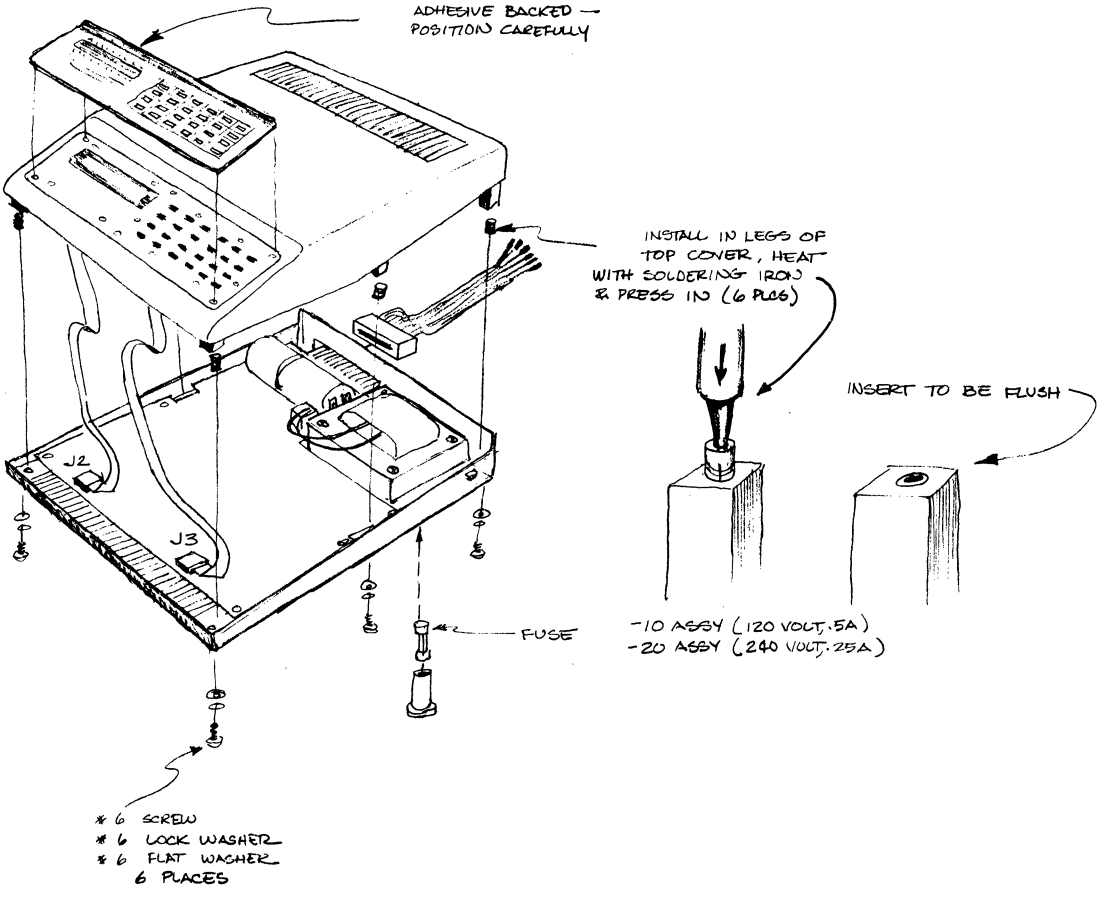
This section contains the schematics and assembly drawings for the Model 2710. Parts lists are also included for user convenience.

7.2 List of Drawings

7.3 Parts Lists

The materials in the following lists are subject to change without Gould Inc.'s prior notification. For list verification, contact the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

7.3.1 List of Parts Lists


ADHESIVE BACKED — POSITION CAREFULLY
INSTALL IN LEGS OF TOP COVER, HEAT WITH SOLDERING IRON & PRESS IN (6 PLCS)
INSERT TO BE FLUSH
J2
J3
FUSE
-10 ASSY (120 VOLT, 5A)
-20 ASSY (240 VOLT, 25A)
6 SCREW
6 LOCK WASHER
6 FLAT WASHER
6 PLACES

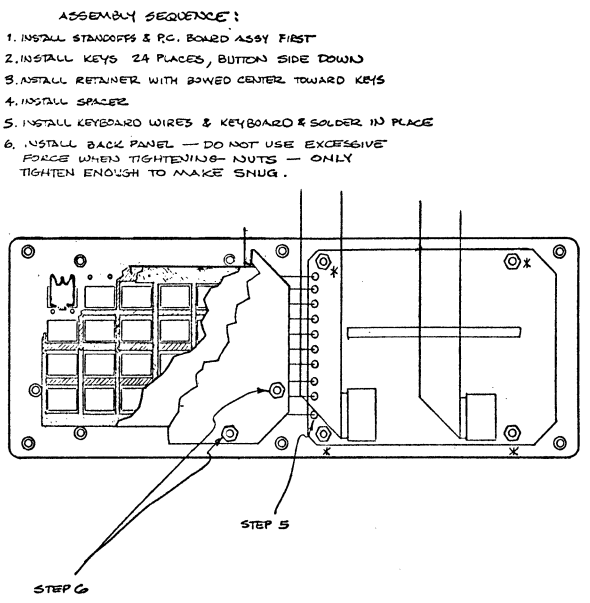
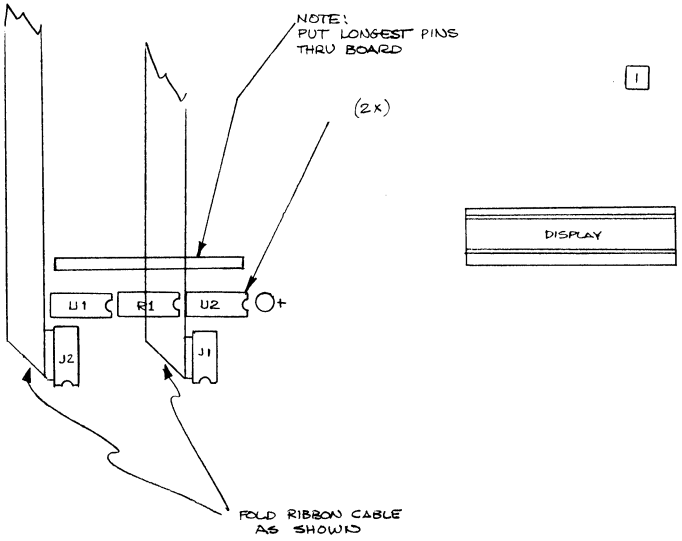


Figure 7.2 Front Panel Assembly 0271-0008



NOTES

[1] WHEN HANDLING THE DISPLAY, IT IS NECESSARY TO WEAR COTTON GLOVES. AVOID SKIN CONTACT TO THE DISPLAY

Figure 7.3 Front Panel P.C. 0271-0020

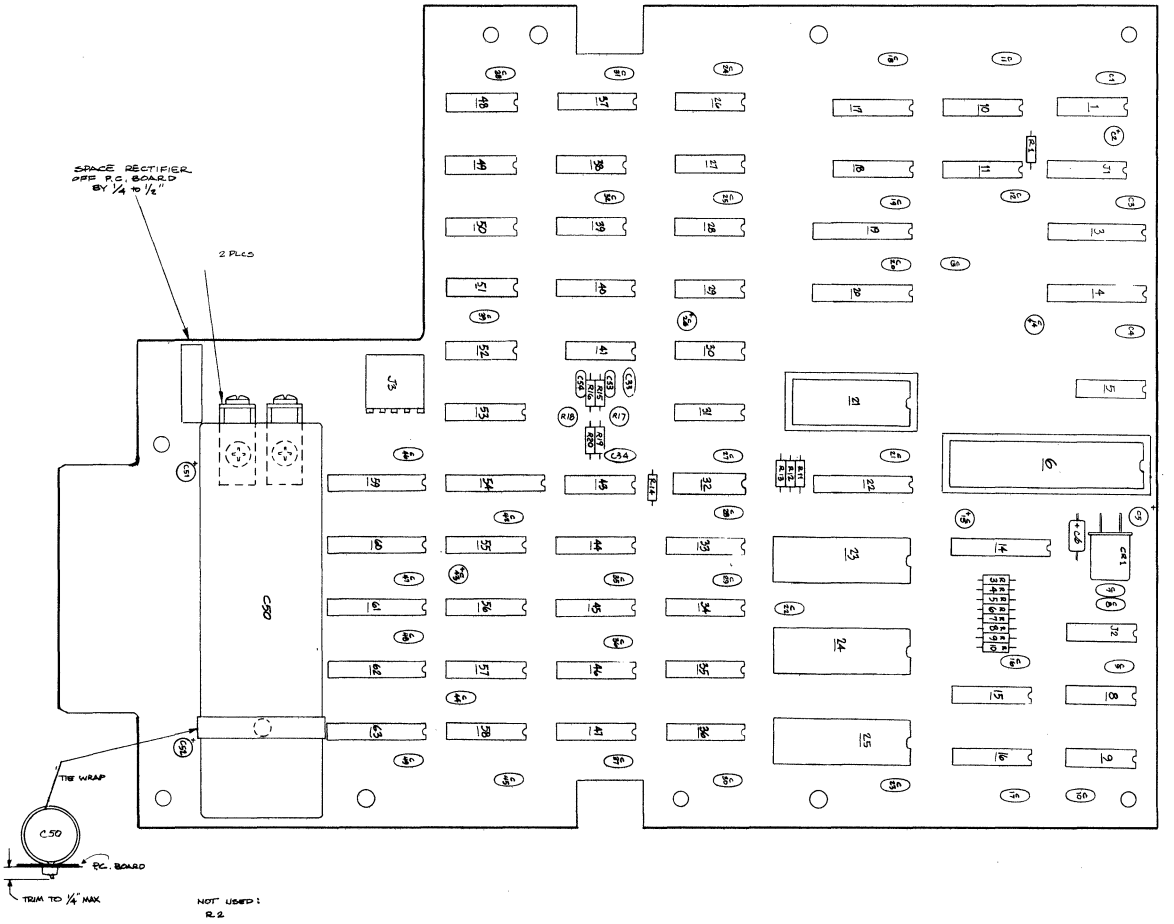


Figure 7.4 Main Board Assembly 0271-0030

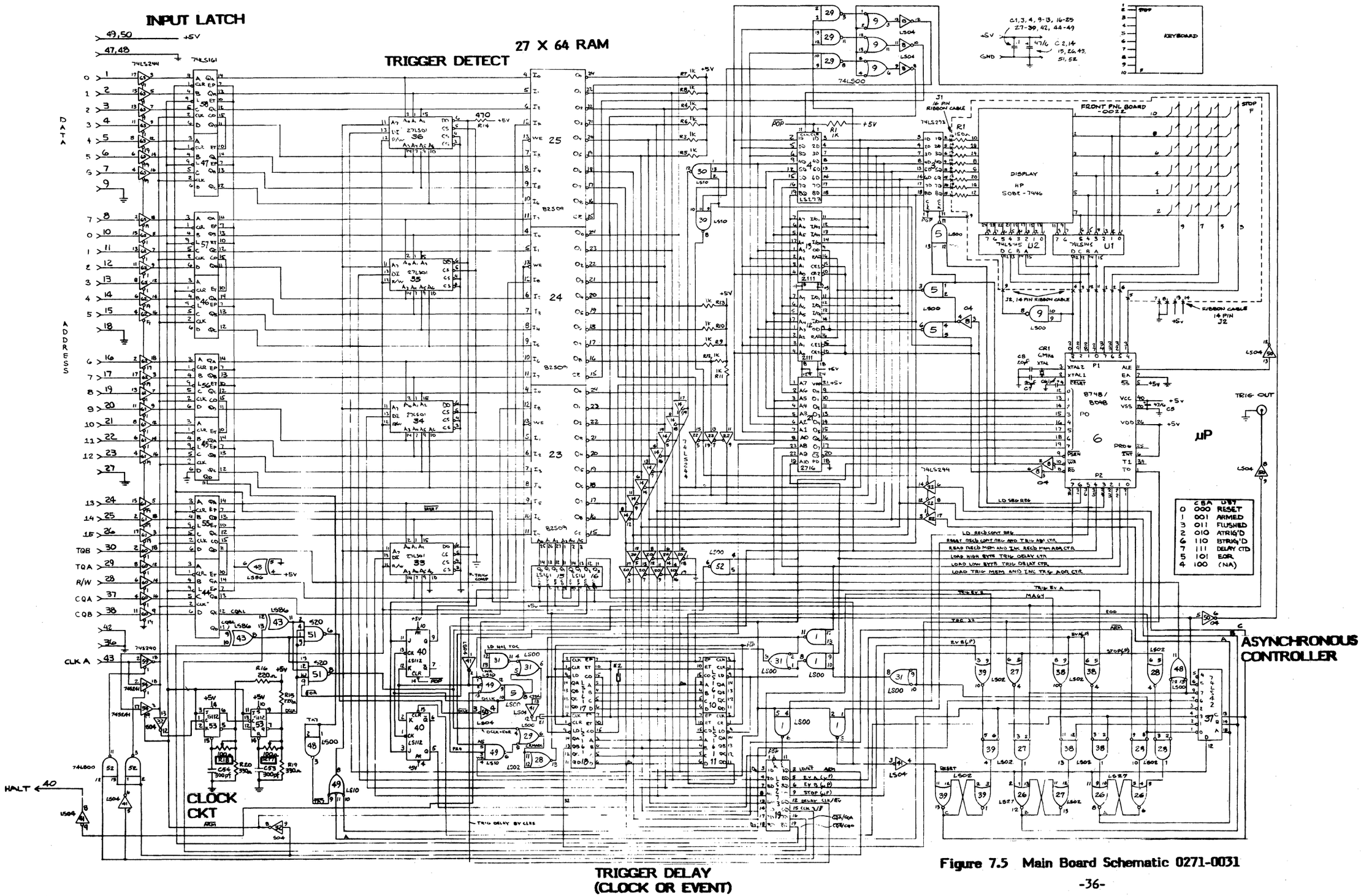


Figure 7.5 Main Board Schematic 0271-0031

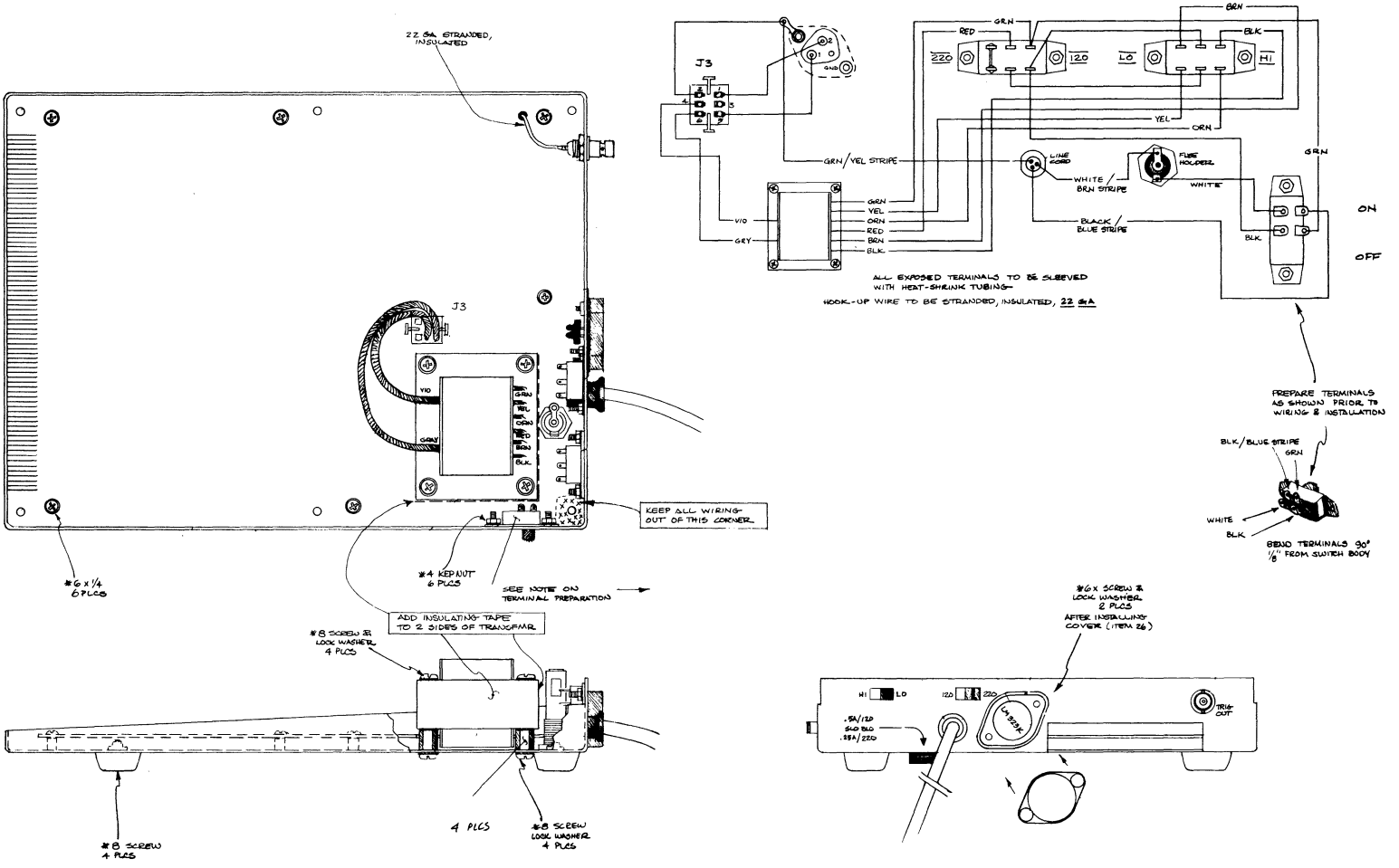


Figure 7.6 Bottom Pan Assembly 0271-0004

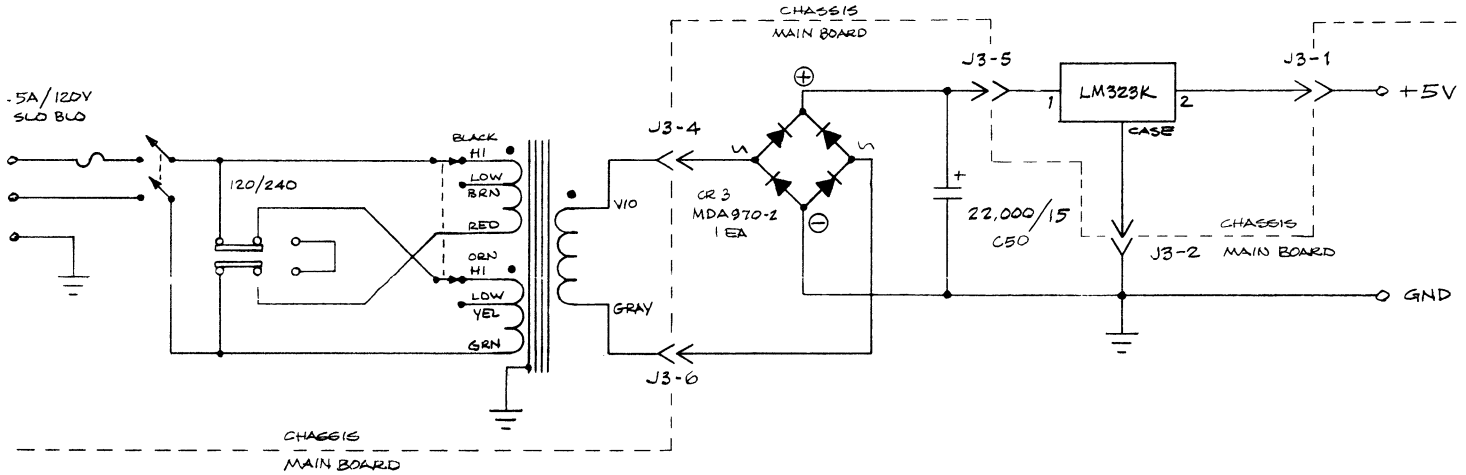


Figure 7.7 Power Supply Schematic 0271-0026

Top Assembly 0271-0001

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1					1	1	0271-0003	ASSY TOP COVER				LM
2					1	1	0271-0004	ASSY BOTTOM PAN				LM
3					1	1	0271-0040	FAB PROBE SET				LM
4					1	1	0271-0010	FRONT PANEL OVERLAY			PLASTIC, ADHESIVE BACKED	
5					6	6	7000-0283	INSERT		IN-X 800632	3/16 DIA BRASS, 4 VANE, 6-32	
6					X	1	7300-0016	FUSE		120V	.5A SLO BLO	
7					1	X	7300-0017	FUSE		240V	.25A SLO BLO	
8					1	1	7300-0024	FUSE CARRIER				
9												
10												
11												
12												
13												
14												
15												
16												
17												
18												

Assembly Front Panel PCB 0271-0020

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0271-0022	FRT PNL BOARD			P.W. BOARD	
2						1	6400-0048	DISPLAY		HP 5082-7446	16 STATION 7 SEGMENT WITH LENS, LED DISP.	
3						2	1800-0281	IC	U1, U2	74LS145	BCD TO DECIMAL DECODER/DRIVER	
4						1	3700-0042	RESISTOR PACK	R1	DALE LDP16-01-1500J	150Ω 5% (8 RESISTORS)	
5						1	0820-0105-10	RIBBON CABLE		J2	14 PIN 14" LONG	
6						1	0820-0105-80	RIBBON CABLE		J1	16 PIN 12" LONG	
7						1	6000-0225	WIRE WRAP POSTS	DISPLAY PINS 1-24	BERG 65501-424	.025 SQ ON .100 C-to-C PLASTIC CARRIER	24 PINS
8												
9						1	4300-0025	CAPACITOR	C1		47μf/6V	
10												

Assembly Main Board 0271-0030

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0271-0032	PROCESSOR & MEMORY BOARD			P.W. BOARD	
2						4	1800-0106	IC.	27,28,38,39.	74L$02		
3						3	-0107	"	8, 41, 50	74L$04		
4						2	-0110		30, 49	74L$10		
5						1	-0215		26	74L$27		
6						1	-0117		43	74L$86		
7						1	-0039		53	74S112		
8						1	-0180		37,	74L$42	BCD TO DECIMAL DECODER	
9						7	-0105		1,5,9,29,31,48,52	74L$00		
10						14	-0125		10,11,15-18,44,45,46, 47,55,56,57,58	74L$161		
11						1	-0261		59	74$240		
12						7	-0240		14,20,22, 60-63	74L$244		
13						3	-0231		3, 4, 19	74L$273		
14						4	-0127		33,34,35,36	27L$01		
15						3	-0283		23,24,25	82$09	64x4 TTL BIPOLAR RAM	
16						1	-0294		6	INTEL P8039-6	MICROCOMPUTOR PLASTIC CASE	
17												
18						1	1800-0241	I.C.	2	INTEL 2716	2K x 8 E PROM	
19						1	1800-0285	I.C.	54	74$241	OCTAL BUFFER	
20						1	1800-0068	I.C.	40	74L$112		
21						1	1800-0092	I.C.	32	74$04		
22						1	1800-0038	I.C.	51	74$20		
23						2	3000-2200	RESISTOR	R15,16		220Ω, 1/4W, 5%	
24						12	3000-1001	" "	R1,3-13		1K 5% 1/4W	
25						2	3300-0002	TRIM POT	R17,18		100Ω, 4½T	
26						1	5100-0012	CRYSTAL	CR1	CTS MP-060	6 MHz .015% 0-70°C H3W CASE	
27						2	3000-3300	RESISTOR	R19,20		330Ω, 1/4W, 5%	
28						1	3000 4700	RESISTOR	R 14		470Ω 1/4W 5%	
29				•		2	4100-0006	CAPACITOR	C7,8,		20pf	
30						38	4000-0025	CAPACITOR	C1,3,4,9,10-13,16-25 27-39,42,44-49		.1μf Ceramic	
31						8	4300-0025	" "	C2,5,14,15, 26 43,51,52		47μf/6V Ta	
32						1	4300-0001	" "	C6		1μf 35V Ta	
33						1	4400-0035	" "	C50	SPRAGUE 36D X 223G015A C2A	22,000μf 15V	
34						2	4100-0042	" "	C53,54		300 PF	
35												
36												

Continued Assembly Main Board 0271-0030

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37												
38						1	1200-0005	RECTIFIER	CR 2	MDA 970-2 MOTOROLA	FULL WAVE BRIDGE	
39												
40						2	7000-0354	ANGLE BRKT	(C50)	KEYSTONE # 620		
41												
42						1	6100-0061	24 PIN SOCKET	(U21)	AUGAT 524-AG1D		
43						1	6100-0021	6 PIN SOCKET	J3	AMP		
44						1	6100-0044	14 PIN DIP SKT	J2	AUGAT 514-AG-10D		
45						1	6100-0046	16 PIN DIP SKT	J1	AUGAT 516-AG-10D		
46						1	6100-0072	40 PIN SOCKET	(U6)	AUGAT 540-AG11D		
47												
48												
49						1	7200-0040	TIE WRAP	(C50)		3/16 WIDE	
50												
51												
52												
53												
54												

Assembly Bottom Pan 0271-0004

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0271-0005-10	BOTTOM PAN				
2												
3						1	0271-0050	ASSY MAIN BOARD				LM
4												
5						1	0271-0035	TRANSFORMER				
6						1	6700-0031	SWITCH	ON – OFF	CW GF-695 WITH G-02-76-A5 BUTTON	G-20-27 TERMINALS	
7						2	6700-0015	SWITCH	120 - 220 VAC	CW GF-626 WITH G-02-153 BUTTON	G-20-31 TERMINALS	
8						1	7000-0355	STRAIN RELIEF	PWR CORD	HEYCO # SR 5N-5		
9						1	7100-0049	POWER CORD		BELDEN # 17251-C	3 COND, 5V, SVT	
10						1	6000-0014	BNC		KINGS KC-79-35		
11						4	7000-0193	FEET		H. H. SMITH # 2135	RECESS RUBBER BUMPERS 3/8 x 31/32 D	
12												
13												
14						6	6100-0006	PIN		AMP # 61173-1		
15						1	6100-0022	CONNECTOR HOUSING		AMP # 1-480-270-0		
16												
17												
18												
19												
20												
21						1	1700-0046	REGULATOR		LM 323 K	5V REGULATOR TO-3 CASE	
22						1	7200-0016	INSULATOR		CHOMERICS 60-11-4996-1666	BLUE PLASTIC TO3	
23						A/R	——	WIRE			22ga, stranded, insulated	
24						4	7000-0360	STANDOFF	KFMR	AMETON 8572-B0832	3/8 HEX 7/16 L 8-32 BRASS	
25						1	6100-0103	SOCKET	FOR ITEM 21		2 pin, Pwr Transistor	
26						1	7000-0242	COVER	TRANSISTOR	THERMALLOY 8903 NB	BLACK NYLON COVER FOR TO-3	
27						1	7300-0023	FUSE HOLDER	FEU 031.1653	SCHURTER		
28												
29												