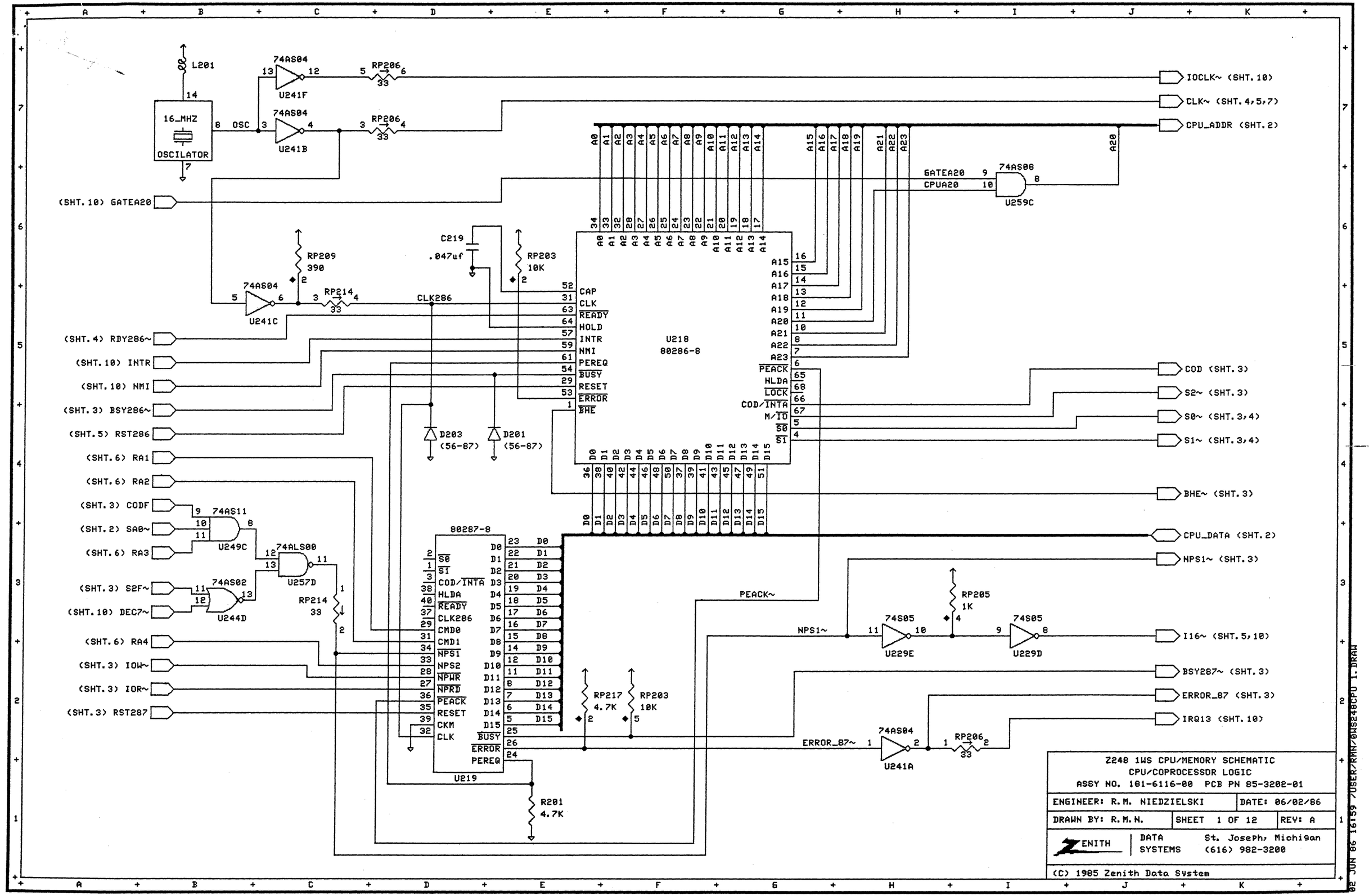
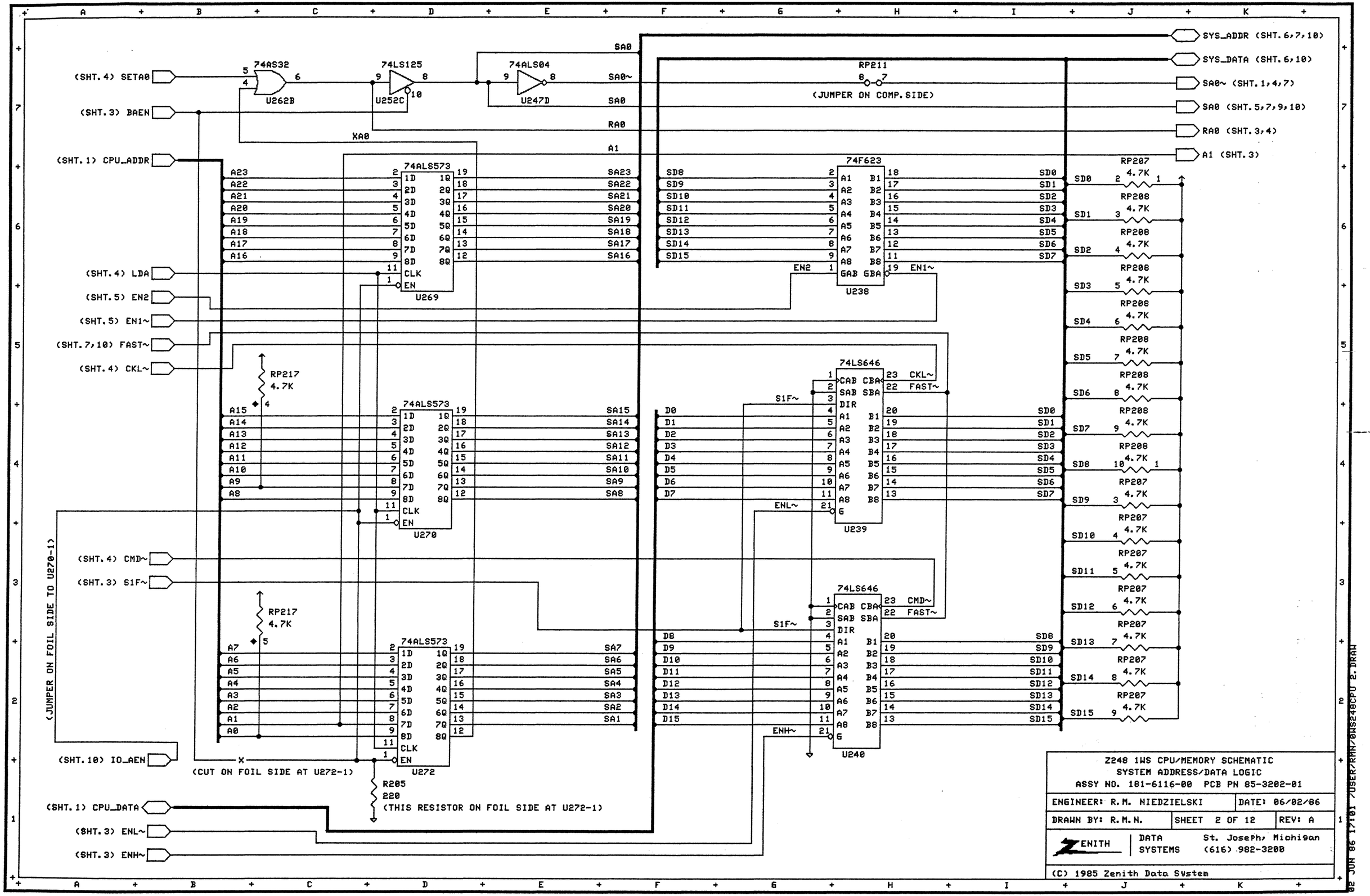


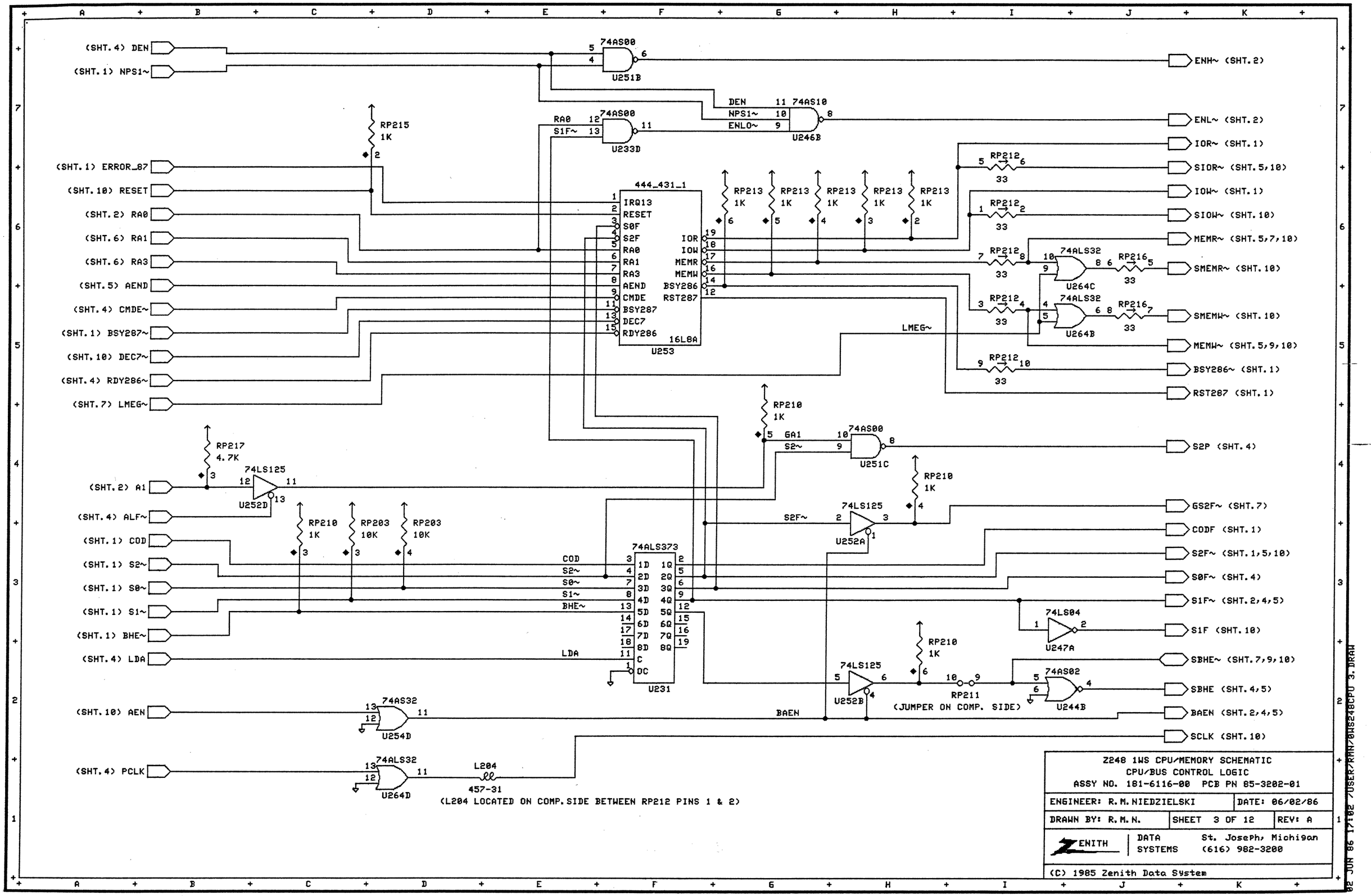
Z248 1WS CPU/MEMORY SCHEMATIC
CPU/COPROCESSOR LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M. NIEDZIELSKI		DATE: 06/02/86
DRAWN BY: R.M.N.	SHEET 1 OF 12	REV: A

ZENITH DATA SYSTEMS — St. Joseph, Michigan (616) 982-3200

02 JUN 86 16:59 /USER/RMN/8WS248CPU 1.DRAW


(SHT.4) SETA0
(SHT.3) BAEN
(SHT.1) CPU_ADDR
(SHT.4) LDA
(SHT.5) EN2
(SHT.5) EN1~
(SHT.7,10) FAST~
(SHT.4) CKL~
(SHT.4) CMD~
(SHT.3) S1F~
(SHT.10) IO_AEN
(SHT.1) CPU_DATA
(SHT.3) ENL~
(SHT.3) ENH~
74AS32
U262B
74LS125
U252C
74ALS04
U247D
SA0
SA0~
SA0
RA0
XA0
A1
74ALS573
U269
U270
U272
74F623
U238
74LS646
U239
U240
RP211
(JUMPER ON COMP.SIDE)
RP217
4.7K
R205
220
(THIS RESISTOR ON FOIL SIDE AT U272-1)
(JUMPER ON FOIL SIDE TO U270-1)
(CUT ON FOIL SIDE AT U272-1)
RP207
RP208
SYS_ADDR (SHT.6,7,10)
SYS_DATA (SHT.6,10)
SA0~ (SHT.1,4,7)
SA0 (SHT.5,7,9,10)
RA0 (SHT.3,4)
A1 (SHT.3)
Z248 1WS CPU/MEMORY SCHEMATIC
SYSTEM ADDRESS/DATA LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01
ENGINEER: R.M. NIEDZIELSKI
DATE: 06/02/86
DRAWN BY: R.M.N.
SHEET 2 OF 12
REV: A
ZENITH DATA SYSTEMS
St. Joseph, Michigan
(616) 982-3200
(C) 1985 Zenith Data System
02 JUN 86 17:01 /USER/RMN/0WS248CPU 2.DRAW

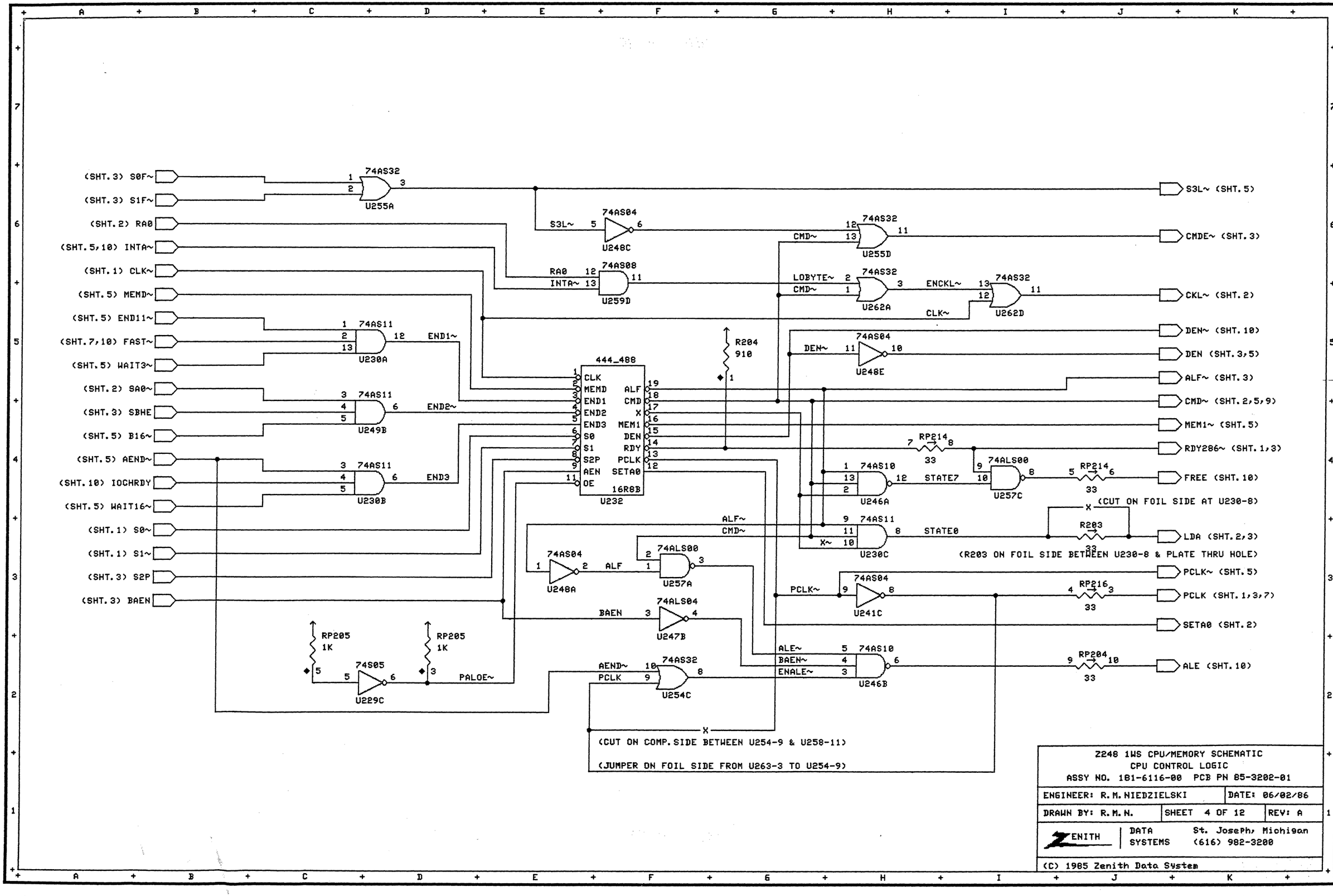


Z248 1WS CPU/MEMORY SCHEMATIC
CPU/BUS CONTROL LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 06/02/86
DRAWN BY: R.M.N.	SHEET 3 OF 12	REV: A

ZENITH DATA SYSTEMS — St. Joseph, Michigan (616) 982-3200

02 JUN 86 17:02 /USER/RMN/0MS248CPU 3.DRAW


(SHT.3) S0F~
(SHT.3) S1F~
74AS32
U255A
S3L~ (SHT.5)
(SHT.2) RA0
(SHT.5,10) INTA~
(SHT.1) CLK~
(SHT.5) MEMD~
S3L~
74AS04
U248C
CMD~
74AS32
U255D
CMDE~ (SHT.3)
RA0
INTA~
74AS08
U259D
LOBYTE~
CMD~
74AS32
U262A
ENCKL~
74AS32
U262D
CKL~ (SHT.2)
CLK~
(SHT.5) END11~
(SHT.7,10) FAST~
(SHT.5) WAIT3~
74AS11
U230A
END1~
R204
910
444_488
DEN~ (SHT.10)
DEN~
74AS04
U248E
DEN (SHT.3,5)
ALF~ (SHT.3)
CMD~ (SHT.2,5,9)
MEM1~ (SHT.5)
RDY286~ (SHT.1,3)
(SHT.2) SA0~
(SHT.3) SBHE
(SHT.5) B16~
74AS11
U249B
END2~
RP214
33
74ALS00
U257C
FREE (SHT.10)
(SHT.5) AEND~
(SHT.10) IOCHRDY
(SHT.5) WAIT16~
74AS11
U230B
END3
74AS10
U246A
STATE7
(CUT ON FOIL SIDE AT U230-8)
(SHT.1) S0~
(SHT.1) S1~
(SHT.3) S2P
(SHT.3) BAEN
ALF~
CMD~
74AS11
U230C
STATE0
R203
LDA (SHT.2,3)
(R203 ON FOIL SIDE BETWEEN U230-8 & PLATE THRU HOLE)
74AS04
U248A
ALF
74ALS00
U257A
PCLK~ (SHT.5)
PCLK~
74AS04
U241C
RP216
33
PCLK (SHT.1,3,7)
BAEN
74ALS04
U247B
SETA0 (SHT.2)
RP205
1K
RP205
1K
74S05
U229C
PALOE~
AEND~
PCLK
74AS32
U254C
ALE~
BAEN~
ENALE~
74AS10
U246B
RP204
33
ALE (SHT.10)
(CUT ON COMP. SIDE BETWEEN U254-9 & U258-11)
(JUMPER ON FOIL SIDE FROM U263-3 TO U254-9)
Z248 1WS CPU/MEMORY SCHEMATIC
CPU CONTROL LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01
ENGINEER: R.M.NIEDZIELSKI
DATE: 06/02/86
DRAWN BY: R.M.N.
SHEET 4 OF 12
REV: A
ZENITH DATA SYSTEMS
St. Joseph, Michigan
(616) 982-3200
(C) 1985 Zenith Data System
02 JUN 86 17:03 /USER/RMN/Z0S248CPU 4.DRAW

(SHT.1) CLK~
(SHT.10) RC~
(SHT.10) 0WS~
(SHT.4) PCLK~
(SHT.4) CMD~
(SHT.10) DCOK
(SHT.10) SLOW
(SHT.10) IOCHRDY
(JUMPER ON FOIL SIDE FROM U230-4 TO U256-9)

444_429_4
CLK
RC
AENDD
0WS
PCLK
CMD
DCOK
SLOW
IORDY
OE
DLY1
QA
QB
QC
QD
R286
AEND
W286
16R6A
U256

WAIT3~ (SHT.4)
AEND~ (SHT.4)
WAIT16~ (SHT.4)

AENDD~
AEND~

74ALS04
U247E
AEND (SHT.3)

(SHT.4) S3L~
(SHT.3) S2F~
(SHT.3) S1F~
(SHT.3) BAEN
(SHT.3,10) MEMR~
(SHT.3,10) SIOR~
(SHT.3) SBHE
(SHT.2,10) SA0
(SHT.7,10) M16~
(SHT.1,10) I16~
(SHT.4) DEN

74AS11
U249A

444_457
S3L
AEND
CMD
S2F
S1F
AEN
MEMR
IOR
EN
M16
PCLK
I16
DLY1
DEN
EN1
MEMD
RST1
AENDD
INTA
B16
EN2
END11
20L8A
U258

EN1~ (SHT.2)
MEMD~ (SHT.4)
RST286~ (SHT.1)
INTA~ (SHT.4,10)
EN2 (SHT.2)
END11~ (SHT.4)

RA1
74AS32
U254B

74ALS00
U257B

74ALS04
U247C

B16~
B16~ (SHT.4)

(SHT.6) RA1

S1F~
74ALS04
U247F

74AS02
U244A

ENWRT~
74AS02
U242A

(L203 LOCATED ON COMP.SIDE AT RP211, BETWEEN PINS 5 & 6)
L203
475-31
WRT~ (SHT.7,10)

(SHT.4) MEM1~
(SHT.3,10) MEMW~

74AS02
U242D

MEMW

(L202 LOCATED ON COMP.SIDE AT RP211, BETWEEN PINS 3 & 4)
L202
475-31
MEM~ (SHT.7,10)

MEM1~
74AS08
U245D

ENPAR~ (SHT.7)

MEMR~
74AS00
U251D

74AS00
U251A

ENMEM

AEND

Z248 1WS CPU/MEMORY SCHEMATIC
CPU DELAY & MISC. CONTROL LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M.NIEDZIELSKI	DATE: 06/02/86	
DRAWN BY: R.M.N.	SHEET 5 OF 12	REV: A

ZENITH DATA SYSTEMS
St. Joseph, Michigan
(616) 982-3200

02 JUN 86 17:05 /USER/RMN/0WS248CPU 5.DRAW

(SHT.2,10) SYS_DATA

(SHT.7) MWLO~
(SHT.7) MRLO
(SHT.7) MWHI~
(SHT.7) MRHI
(SHT.7) T60~
(SHT.7) PARLO
(SHT.10) REF~
(SHT.7) PARHI
(SHT.2,10) SYS_ADDR

74F623 U236: SD0–SD7 → MD0–MD7
74F623 U234: SD8–SD15 → MD8–MD15
74F280 U237: SD0–SD7 → PWLO, PWLO~
74F280 U235: SD8–SD15 → PWHI
RP203 10K
74LS590 U271: SA1–SA8
74AS244 U267: SA1–SA8 → RA1–RA8
74AS244 U268: SA9–SA16 → RA9–RA16
74F158 U211: RA9, RA1, RA11, RA3, RA13, RA5, RA15, RA7 → RP201/RP204 33Ω → MA0, MA2, MA4, MA6
74F158 U210: RA10, RA2, RA12, RA4, RA14, RA6, RA16, RA8 → RP201/RP204 33Ω → MA1, MA3, MA5, MA7
T60~

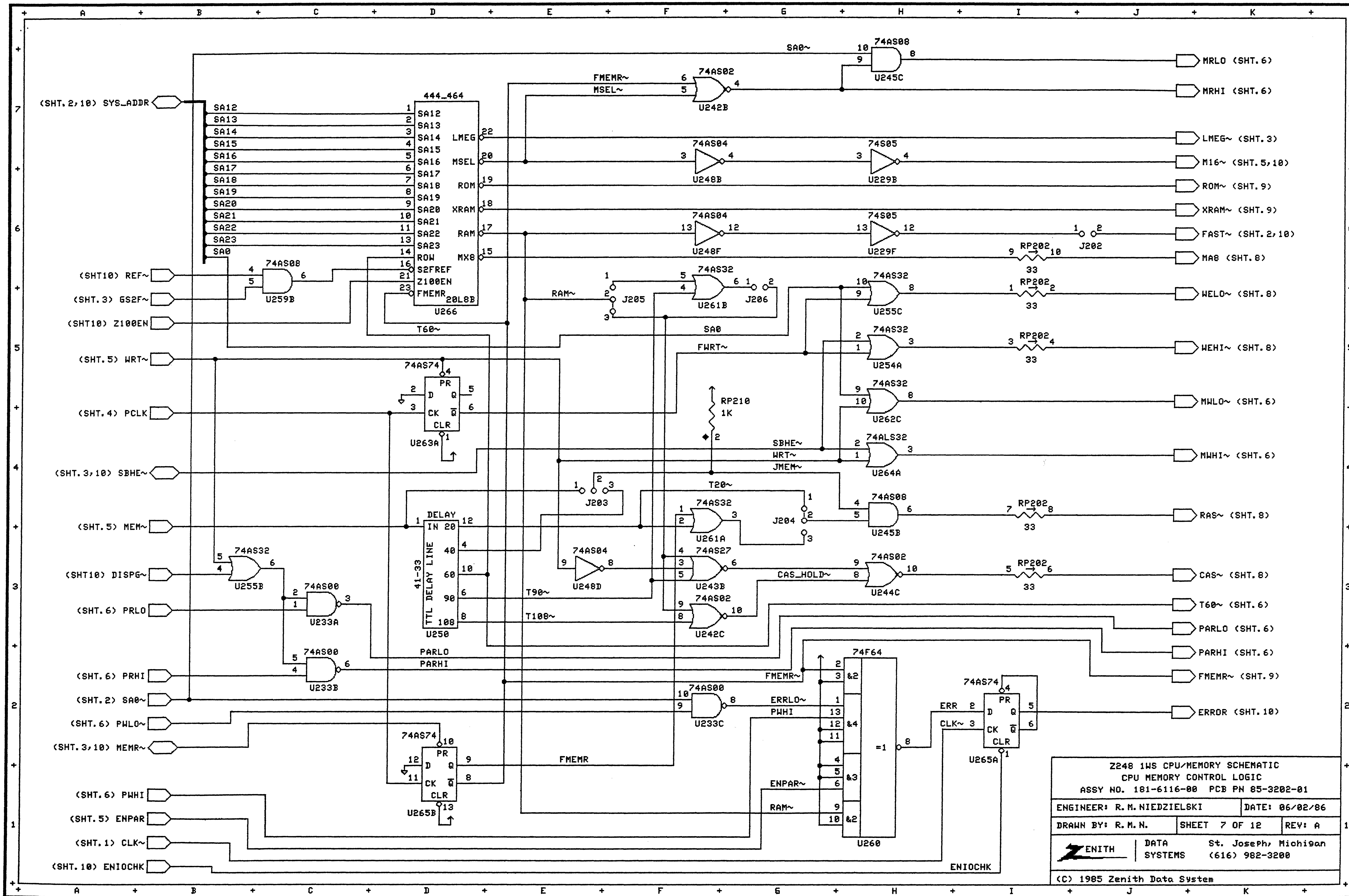
MEM_DATA (SHT.8,9)
MEM_ADDR (SHT.8,9)
RA1 (SHT.1,3)
RA2 (SHT.1)
RA3 (SHT.1,3)
RA4 (SHT.1)
DRAM_ADDR (SHT.8)
PWLO (SHT.8)
PWLO~ (SHT.7)
PWHI (SHT.7,8)

Z248 1WS CPU/MEMORY SCHEMATIC
MEMORY ADDRESS/DATA BUS LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M.NIEDZIELSKI	DATE: 06/02/86	
DRAWN BY: R.M.N.	SHEET 6 OF 12	REV: A

ZENITH DATA SYSTEMS — St. Joseph, Michigan (616) 982-3200

02 JUN 86 17:56 /USER/RMN/8WS248CPU 6.DRAW



Z248 1WS CPU/MEMORY SCHEMATIC
CPU MEMORY CONTROL LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 06/02/86
DRAWN BY: R.M.N.	SHEET 7 OF 12	REV: A

ZENITH DATA SYSTEMS St. Joseph, Michigan (616) 982-3200

(SHT.6) MEM_ADDR

(SHT.7) MA8

(SHT.6) MEM_DATA

U201 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, MD0 14

U202 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, MD1 14

U203 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, MD2 14

U204 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, MD3 14

U205 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, MD4 14

U206 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, MD5 14

U207 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, MD6 14

U208 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, MD7 14

U209 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WELO~ 3, RAS~ 4, CAS~ 15, PWLO 2, 14

PRLO (SHT.7)

U220 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, MD8 14

U221 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, MD9 14

U222 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, MD10 14

U223 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, MD11 14

U224 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, MD12 14

U225 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, MD13 14

U226 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, MD14 14

U227 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, MD15 14

U228 HM51256 256K X 1 D_RAM — MA0 5, MA1 7, MA2 6, MA3 12, MA4 11, MA5 10, MA6 13, MA7 9, MA8 1, WEHI~ 3, RAS~ 4, CAS~ 15, PWHI 2, 14

PRHI (SHT.7)

(SHT.7) WELO~

(SHT.7) WEHI~

(SHT.7) RAS~

(SHT.7) CAS~

(SHT.7) PWLO

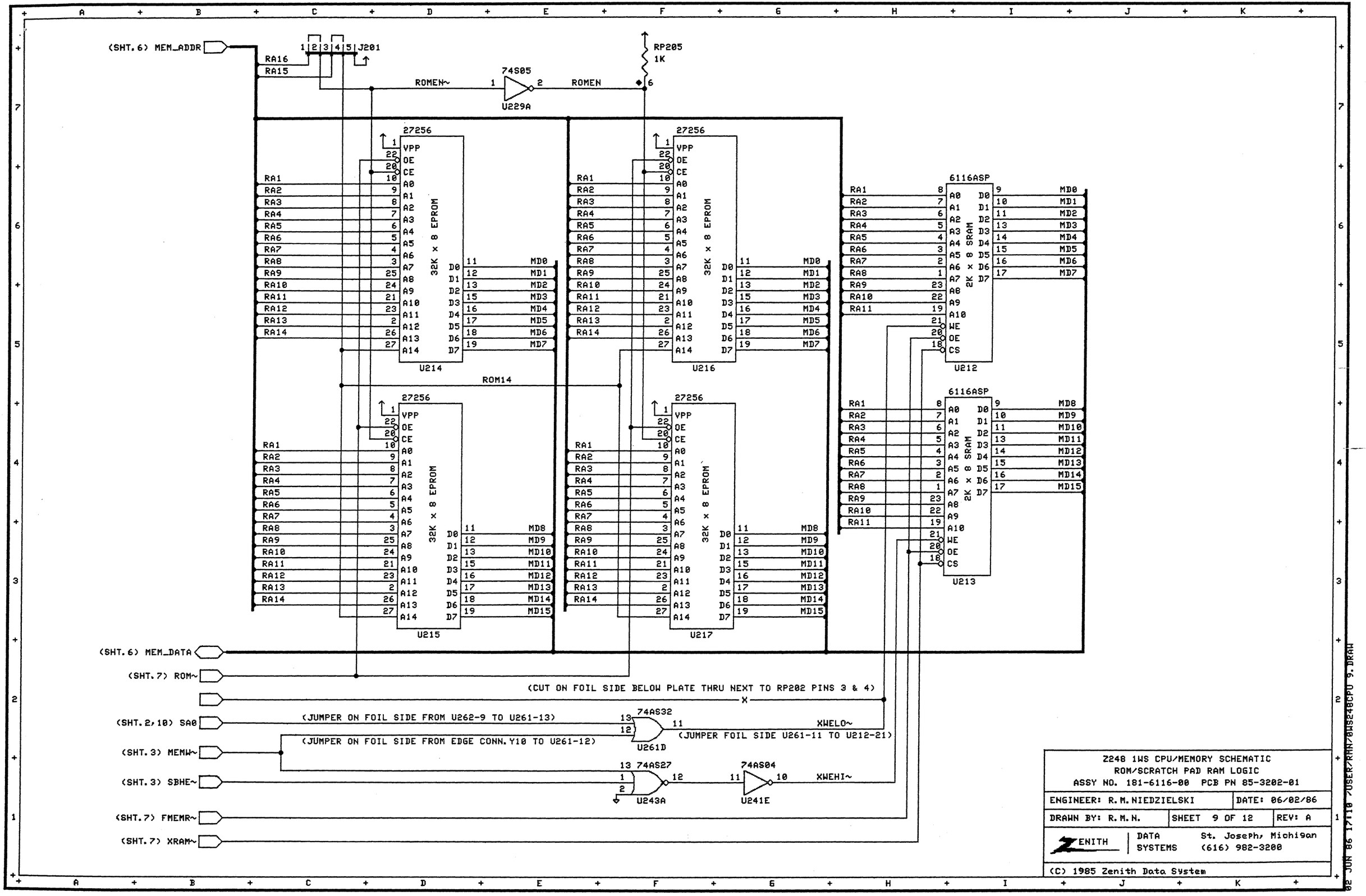
(SHT.7) PWHI

Z248 1WS CPU/MEMORY SCHEMATIC
512K MEMORY ARRAY LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M.NIEDZIELSKI	DATE: 06/02/86	
DRAWN BY: R.M.N.	SHEET 8 OF 12	REV: A

ZENITH DATA SYSTEMS — St. Joseph, Michigan (616) 982-3200

02 JUN 86 17:09 /USER/RMN/0WS248CPU 8.DRAW

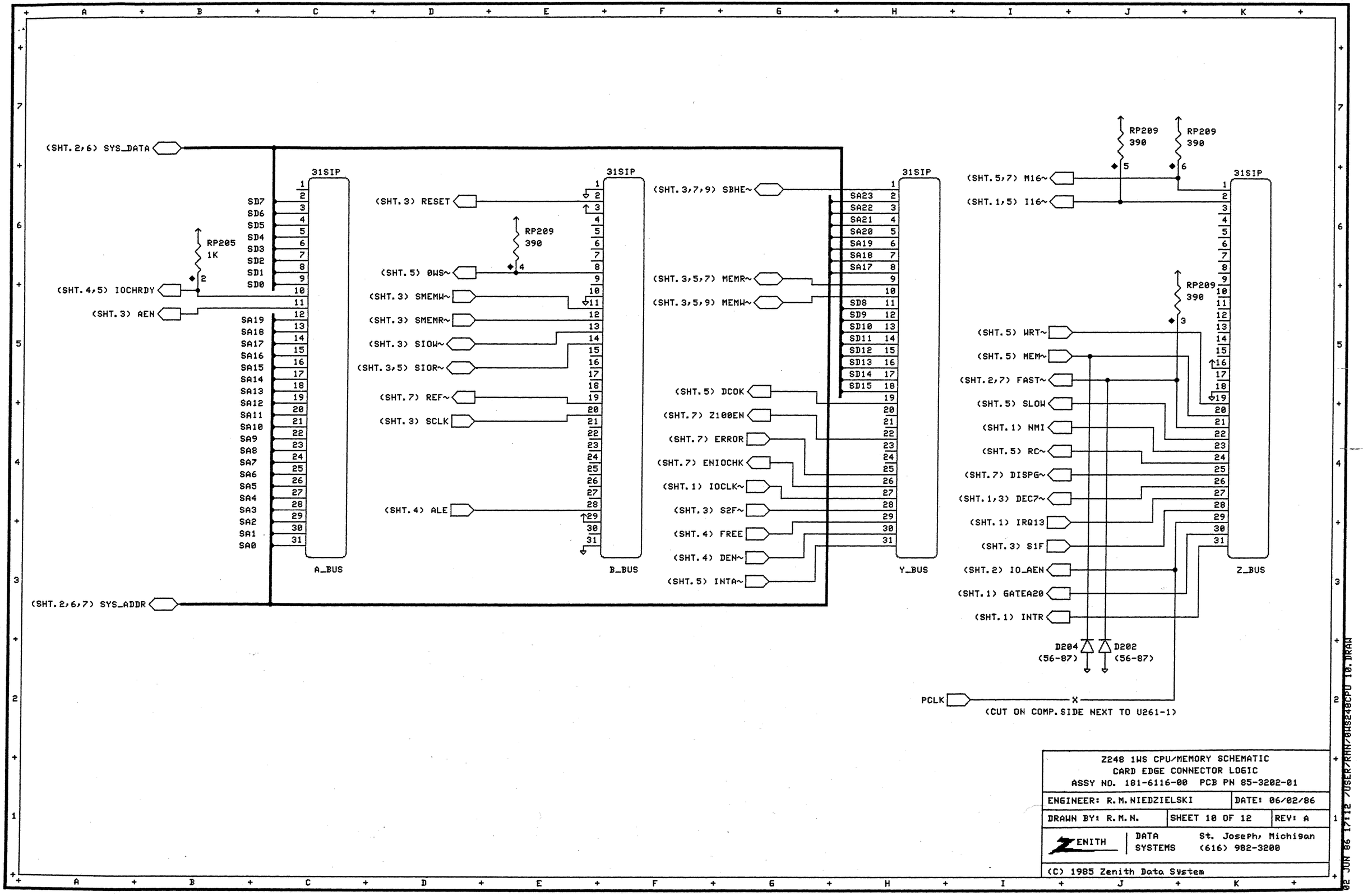


Z248 1WS CPU/MEMORY SCHEMATIC
ROM/SCRATCH PAD RAM LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 06/02/86
DRAWN BY: R.M.N.	SHEET 9 OF 12	REV: A

ZENITH DATA SYSTEMS — St. Joseph, Michigan (616) 982-3200

02 JUN 86 17:10 /USER/RMN/8MHz248CPU 9.DRAW



Z248 1WS CPU/MEMORY SCHEMATIC
CARD EDGE CONNECTOR LOGIC
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M.NIEDZIELSKI		DATE: 06/02/86
DRAWN BY: R.M.N.	SHEET 10 OF 12	REV: A

ZENITH DATA SYSTEMS — St. Joseph, Michigan (616) 982-3200

02 JUN 86 17:12 /USER7/RMN/0H3248CPU 10.DRAW

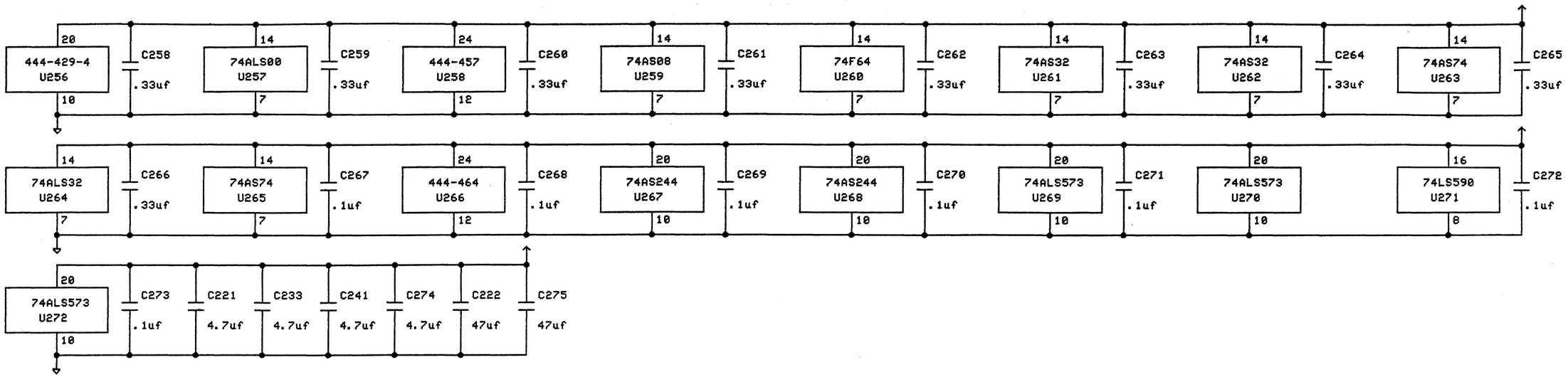
8	HM51256P-12 U201	16	C201 .33uf	8	HM51256P-12 U202	16	C202 .33uf	8	HM51256P-12 U203	16	C203 .33uf	8	HM51256P-12 U204	16	C204 .33uf	8	HM51256P-12 U205	16	C205 .33uf	8	HM51256P-12 U206	16	C206 .33uf
8	HM51256P-12 U207	16	C207 .33uf	8	HM51256P-12 U208	16	C208 .33uf	8	HM51256P-12 U209	16	C209 .33uf	16	74F158 U210	8	C210 .1uf	16	74F158 U211	8	C211 .1uf	24	6116ASP U212	12	C212 .1uf
24	6116ASP U213	12	C213 .1uf	28	27256-20 U214	14	C214 .1uf	28	27256-20 U215	14	C215 .1uf	28	27256-20 U216	14	C216 .1uf	20	27256-20 U217	14	C217 .1uf	30,62	80286-8 U218	9,35,60	C218 .1uf
9	80287-8 U219	10,30	C220 .1uf	8	HM51256P-12 U220	16	C223 .33uf	8	HM51256P-12 U221	16	C224 .33uf	8	HM51256P-12 U222	16	C225 .33uf	8	HM51256P-12 U223	16	C226 .33uf	8	HM51256P-12 U224	16	C227 .33uf
8	HM51256P-12 U225	16	C228 .33uf	8	HM51256P-12 U226	16	C229 .33uf	8	HM51256P-12 U227	16	C230 .33uf	8	HM51256P-12 U228	16	C231 .33uf	14	74AS02 U242	7	C242 .1uf	14	74AS27 U243	7	C243 .1uf
14	74AS02 U244	7	C244 .1uf	14	74AS08 U245	7	C245 .1uf	14	74AS10 U246	7	C246 .1uf	14	74ALS04 U247	7	C247 .1uf	14	74AS04 U248	7	C248 .1uf	14	74AS11 U249	7	C249 .1uf
14	74S05 U229	7	C232 .1uf	14	74AS11 U230	7	C234 .1uf	20	74ALS373 U231	10	C235 .1uf	20	444-488 U232	10	C236 .1uf	14	74AS00 U233	7	C237 .1uf	20	74F623 U234	10	C238 .1uf
14	74F280 U235	7	C239 .1uf	20	74F623 U236	10	C240 .1uf	14	74F280 U237	7	C242 .1uf	20	74F623 U238	10	C243 .1uf	24	74LS646 U239	12	C244 .1uf	24	74LS646 U240	12	C245 .1uf
14	16 MHZ OSC Y201	7	C250 .1uf	14	74AS04 U241	7	C251 .1uf	14	41-33 DELAY U250	7	C252 .1uf	14	74AS00 U251	7	C253 .1uf	14	74LS125 U252	7	C254 .1uf	20	444-431-1 U253	10	C255 .1uf
14	74AS32 U254	7	C256 .1uf	14	74AS32 U255	7	C257 .1uf																

Z248 1WS CPU/MEMORY SCHEMATIC
POWER SUPPLY RAILS
ASSY NO. 181-6116-00 PCB PN 85-3202-01

ENGINEER: R.M.NIEDZIELSKI	DATE: 06/02/86	
DRAWN BY: R.M.N.	SHEET 11 OF 12	REV: A

ZENITH DATA SYSTEMS — St. Joseph, Michigan (616) 982-3200

02 JUN 86 17:45 /USER/RMN/WS248CPU 11.DRAW



Z248 1WS CPU/MEMORY SCHEMATIC POWER SUPPLY RAILS ASSY NO. 181-6116-00 PCB PN 85-3202-01		
ENGINEER: R.M.NIEDZIELSKI		DATE: 06/02/86
DRAWN BY: R.M.N.	SHEET 12 OF 12	REV: A
ZENITH DATA SYSTEMS	St. Joseph, Michigan (616) 982-3200	

02 JUN 86 17:15 /USER/RMN/0WS248CPU 12.DRAW