Xylogics®

MODEL 472

Users' Manual

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MODEL 472

Users' Manual

Burlington, MA 01803

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472 MANUAL TABLE OF CONTENTS

SECTION 1 SPECIFICATIONS

1.0 GENERAL

The Xylogics Model 472 Peripheral Processor can interface up to 8 Pertec Fomatted Interface 1/2 inch streaming or start-stop tape drives to IEEE P796 Multibus[1] systems. Data transfers are implemented via DMA, which allows maximum throughput. System control is implemented via I/O Parameter Blocks (IOPBs) and byte I/O registers. The 472 circuitry is comprised of a DMA sequencer and a microprocessor for control and is the fastest tape controller available for Multibus systems with a DMA tranfer rate capability of 3.0 Megabytes per second.

1.1 DESIGN RELIABILITY

XYLOGICS' design minimizes the likelihood (and the expense) of failure by the following:

- o low parts-count, through microprogramming;
- o low-power Schottky Integrated Circuits;
- o low-stress design on all components;
- o all components burned-in;
- o one card, resident in backplane or expansion chassis;
- o controller is power-cycled under thermal stress during test.

1.2 PHYSICAL

Packaging -- The 472 is completely resident on one printed circuit board (PCB) that plugs into any 16-, 20- or 24-bit Intel Multibus or IEEE P796 card cage.

Dimensions -- 12-inch length x 6.75-inch height (30.48 cm X 17.15 cm); the 472 is identical in form-factor to the standard Intel Multibus, and IEEE P796 printed circuit board (PCB).

Shipping Weight -- 8 pounds (3.6 kg).

1.3 ENVIRONMENTAL

The Model 472 Peripheral Processor environmental requirements are the same as the Intel 86/12 SBC or equivalent Multibus processors. (Typically 0-55°C and up to 90% relative humidity without condensation.)

1.4 ELECTRICAL

Power -- The 472 requires 5.0 Amperes at +5 Volts DC.

Tolerance -- Voltages must be within plus or minus five percent.

Grounding -- Common earth ground must be established between the tape drives and the CPU chassis, backplane, and expansion cabinets.

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[1] Multibus is a Trademark of Intel Corporation

1.5 SYSTEM RELATED SPECIFICATIONS

Transfer Control -- Direct Memory Access (DMA).

DMA Throttle Control -- Programmable throttle value supports any Multibus throughput speed.

Interrupt Priority -- INT5/ standard, others jumper selectable.

Interrupts -- Non-Bus-Vectored.

Control Technique -- Channel Driven Control -- Programmable microprocessor.

Addressing Capability -- 16, 20, and 24 bit.

Controller I/O Parameter Block (IOPB) Length -- 18 bytes.

Controller Registers -- Six 8-bit I/O Registers.

I/O Addressing Capability -- The 472 decodes byte addresses for its on-board registers. It will respond to either 8 or 16 bit I/O addresses.

Data Transfer Modes -- Data is transferred in 8-bit bytes or 16-bit words.

Data Buffering -- On-board FIFO memory accomodates 2K bytes. Optional buffer accomodates 8K bytes.

Data Transfer Limit -- Data transfer length, from 1 to 65,535 bytes.

Software Support -- Standard software driver samples supplied for use in RMX-86, UNIX, and Unix-like systems (source included).

Status LEDs -- two status LEDs are implemented. One LED indicates successful completion of on-board diagnostics. The second LED indicates that the controller is active.

DMA Data Transfer Rate -- The 472 can transfer data at a rate of up to 3.0 MB/sec to the system bus (assuming XACK from memory in 300ns), however the actual data rate is dependant on memory response time. With appropriate memory, the 472 can run a streaming 6250 BPI GCR tape at 75 IPS or a start-stop drive at 125 IPS.

RMX-86 - Trademark of Intel Corporation
UNIX - Trademark of Western Electric

1.6 TAPE DRIVE - RELATED SPECIFICATIONS

Tape Interface -- Industry standard Pertec Formatted Interface.

Number of Tape Drives -- The Model 472 supports up to eight tape drives, including mixed speeds and densities.

Tape Speed -- Tape speeds of from 12.5 IPS (inches per second) up to 125 IPS are supported by the 472.

Tape Density -- The 472 supports tape densities of 800 BPI (bits per inch), 1600 BPI, 3200 BPI and 6250 BPI.

Data Verification -- 800 BPI (NRZI) - horizontal and vertical parity; 1600/3200 BPI (PE) - phase encoding; 6250 BPI (GCR) - group encoding.

Recording Mode -- 9 track, ANSI and IBM compatible.

Tape Data Transfer Rate -- Dependant on particular tape drive speed and density; 6250 BPI at 75 IPS yields 469 KBS (kilobytes per second) data rate.

Cabling -- Standard Pertec Formatted Interface consisting of two 50-pin flat ribbon cables.

1.7 PROGRAMMABLE FEATURES

- Software Controlled 16- or 20/24-bit Address Bus Support
- Software Controlled 8- or 16-bit Data Transfers
- Software Controlled Interrupt or Software Polled Operation
- Software Programmable DMA Throttle
- Software Selectable Tape Drive Speed and Density

1.8 472 REGISTERS

The use of specific bits within the 472 I/O Registers is described in Section 2.3. The 472's registers, which can be loaded and read by the software driver to initiate commands are listed in Table 2-1.

1.9 COMMAND TECHNIQUE

The 472 command technique allows command-chaining with concurrent host and peripheral processor operations. Channel control allows a software driver to establish an I/O Parameter Block (IOPB) with a command and parameters in system memory. Each of many processes (or tasks) may prepare their own IOPBs. The use of specific bits within the IOPBs is described in Section 2.4. IOPB formats are listed in Table 2-2.

The software driver initiates a command or command chain by loading the memory address of the first IOPB in the chain into the 472 Relocation and Address Registers and setting the 472 Status Register Bit 7 (GBSY), which stays set until (chained) command completion or an error is detected.

The 472 reads the command IOPB from system memory by direct memory access (DMA) and performs the required function. On detecting an error, the 472 writes an Error code into bytes 3 and 4 of the IOPB related to the operation which caused the error. Hard errors are normally cleared by writing a one to the error status bit in the Controller Status Register.

1.9.1 Chained Commands

The 472 provides inherent command-chaining capability for complex operations. The software driver can set up a string of commands (e.g., disk to tape copy) to allow executing a series of tape operations without operating system intervention. At any time, the operating system can add new IOPBs or remove completed IOPBs from the chain using the attention request protocol. Chained commands may provide overlap rewind operations on multi-drive systems.

1.10 USING THIS MANUAL

A card in the front of this manual can be cut and folded to provide two program reference cards. Installing the 472 is described in Section 3. If you wish to program it, read sections 2.1, 2.6.1, and 2.6.2. This will give a good overview of the programming procedures. Section 2.3 describes the registers, section 2.4 describes the IOPB, and section 2.5 describes the commands.

1.10.1 Abbreviations

In many places in this manual several letters are used as mnemonics to encode various functions. The following table can be utilized to decode these various codes into meaningful information.

BPI	Bits Per Inch
CPU	Central processor Unit and/or computer
CSR	Control and Status Register
DMA	Direct Memory Access
FIFO	First In First Out buffer
GCR	Group coded recording
H	Notation for numerical values expressed in Hexadecimal.
IPS	Inch Per Second
IOPB	Input / Output Parameter Block
I/O	Input / Output
NRZI	Non-return to zero
PE	Phase encoded
RAM	Random Access Memory

SECTION 2 PROGRAMMING REFERENCE

2.0 GENERAL

This section contains the information needed to program the XYLOGICS Model 472 Tape Peripheral Processor. The 472 was designed to easily interface many different processors with a wide variety of tape drives.

2.1 PROGRAMMING TECHNIQUES

Commands for the 472 are set up by the preparation of an I/O Parameter Block (IOPB) in system memory. The command is initiated by loading the address of the IOPB into registers on the 472 controller and setting GBSY of the Controller Status Register. GBSY stays set until all commands in the IOPB chain are completed or a hard error is detected. Upon completion of a command, the 472 writes the corresponding completion codes into bytes 3 and 4 of the completed IOPB. Table 2-2 lists the bytes in an IOPB.

The IOPB is an area in system memory used for passing command level information between the 472 and the CPU. The CPU writes and reads the IOPB by using normal byte or word instructions. The 472 reads and writes the IOPB by using byte mode Direct Memory Access (DMA).

The CPU builds the IOPB in system memory with the appropriate information and then passes the address of the IOPB by loading the Address and Relocation Registers. After the CPU sets GBSY in the CSR, the 472 will transfer the IOPB from memory and process the command, resetting GBSY of the CSR on completion. While processing the command, the 472 may access the IOPB again and may also DMA data to or from memory. IOPBs may be chained together. When chained, the 472 may perform overlapped operations on multiple drives and execute data transfers without CPU intervention.

Each byte in the IOPB has an address relative to the command byte. In order to maintain IOPB integrity, all 18 bytes of allowable IOPB space must be reserved.

2.2 MULTIBUS ADDRESS RELOCATION

When accessing Multibus memory the 472 uses a technique called Address Relocation. Address Relocation is the addition of two addresses to form a larger physical address. Two types of Address Relocation are supported by the 472: 20-bit relocation and 24-bit relocation. Either type of relocation may be used when specifying 16 bits of memory address. For 16-bit memory addressing the relocation registers should be loaded with zero. A staple on the 472 board selects either 20-bit relocation or 24-bit relocation. The positon of the 20- or 24-bit mode staple can be determined by examining bit 3 (ADMD) of the CSR.

NOTE

This manual refers to both IOPB relocation and data relocation. Do not get them confused. IOPB relocation refers to the address at which the IOPB resides in memory. Data relocation refers to the address at which the data buffer exists. Data relocation may be affected by bit 6 (RELO) of Command byte 0, but IOPB relocation will not. The jumper for 20/24 bit address selection affects how address relocation is computed for both Data and IOPBs.

2.2.1 20-Bit Address Relocation

The 472 forms a 20-bit physical address by adding a 16-bit address word to a shifted 16-bit relocation word. The relocation word is shifted by 4 bits as shown in Figure 2-1A.

2.2.2 24-Bit Address Relocation

For 24-bit Address Relocation the 472 calculates a 32-bit physical address. The address word comprises the least significant 16-bits, and the relocation word becomes the most significant 16 bits. When addressing memory, only the lower 24 bits of the physical address are used. See Figure 2-1B.

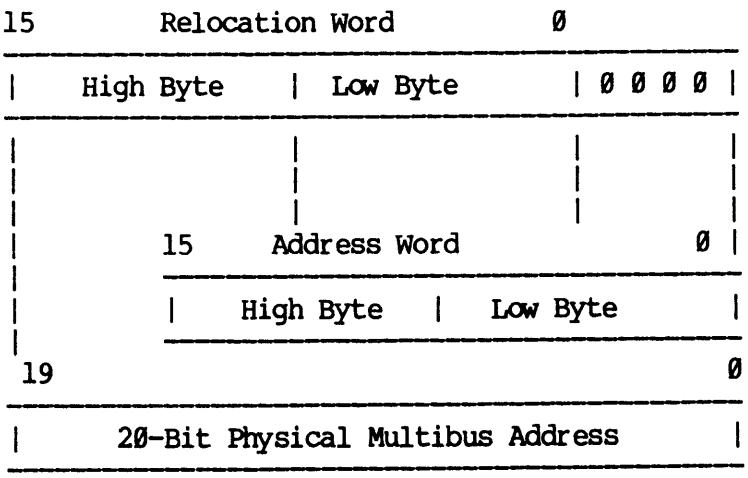


FIGURE 2-1A. 20-BIT MULTIBUS ADDRESS RELOCATION

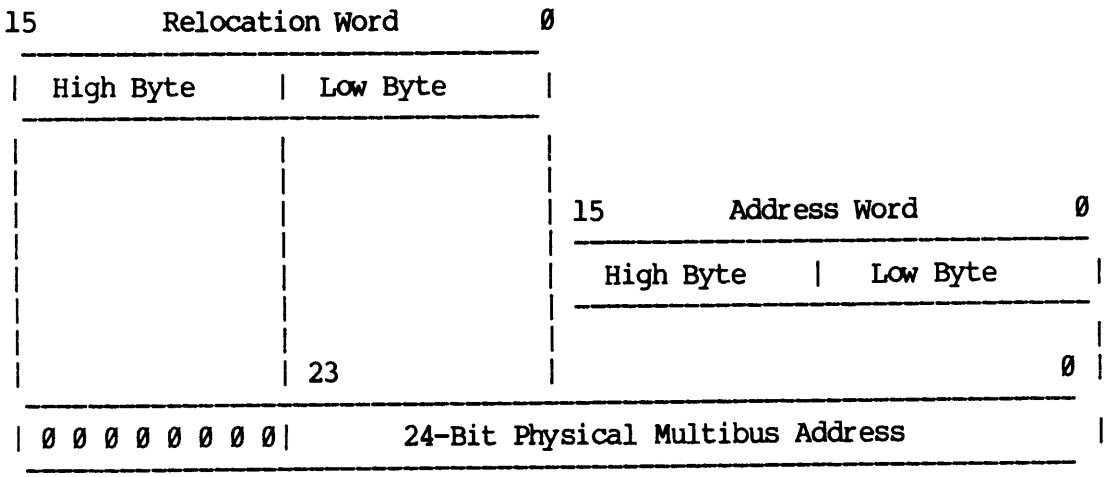


FIGURE 2-1B. 24-BIT MULTIBUS ADDRESS RELOCATION

2.2.3 IOPB Address Relocation

IOPB Relocation occurs whenever a value is loaded into the IOPB Relocation registers. The IOPB Address registers and IOPB Relocation registers are combined to form either a 20-bit or 24-bit physical memory address as shown in Figure's 2-1.

2.2.3 IOPB Address Relocation (continued)

When chaining IOPBs, the Relocation registers are used in conjunction with the IOPB Next Address bytes to form a new 20-bit or 24-bit physical Multibus address. This address points to the next IOPB in the chain. All IOPBs in a chain must reside in the same 64K byte segment whose base is in the Relocation Registers. The base address is computed by shifting the Relocation Registers 4 or 16 bits to the left depending on the relocation mode. See Figure 2-1.

2.2.4 Data Transfer Address Relocation

The starting memory address, for a data transfer operation is specified by IOPB bytes A, B, C, and D. If the RELO bit in the Command byte (byte 0) is clear, the Data Address bytes (bytes A and B) specify the physical Multibus address for the transfer. If the RELO bit is set, the 472 uses bytes C and D as the Data Relocation bytes and bytes A and B as the Data Address bytes. Data relocation occurs in the same manner as IOPB relocation. Figure 2-1A shows how a 20-bit data address is formed and Figure 2-1B shows how a 24-bit address is formed.

2.3 472 I/O REGISTERS

	STANDARD I/O ADDRESSES (HEX)	
USAGE	8-Bit	16-Bit
IOPB Relocation Register Low Byte	60	EE60
IOPB Relocation Register High Byte	61	EE61
IOPB Address Register Low Byte	62	EE62
IOPB Address Register High Byte	63	EE63
Controller Status Register (CSR)	64	EE64
Controller Reset/Update IOPB Register	65	EE65

TABLE 2-1. 472 INPUT/OUTPUT REGISTERS

2.3.1 472 I/O Register Addressing

The 472 Input/Output Registers are addressed as input-output byte ports on the Multibus. The I/O Registers use a standard base address of 60(H) or EE60(H). Table 2-1 summarizes usage and addressing of the 472 I/O Registers. See section 3.2.1 for alternate base addresses.

2.3.2 472 I/O Register Definitions

2.3.2.1 Relocation Registers

There are two Relocation Registers, containing the low and high byte of the relocation address. The two Relocation Registers are the most significant portion of the IOPB memory address. On power-up these registers are cleared by the 472. When using 16 bit addresses, these registers should be zero. Writing anything except zero to these registers causes IOPB relocation. See Figure 2-1 for an example of how 20- or 24-bit addresses are determined.

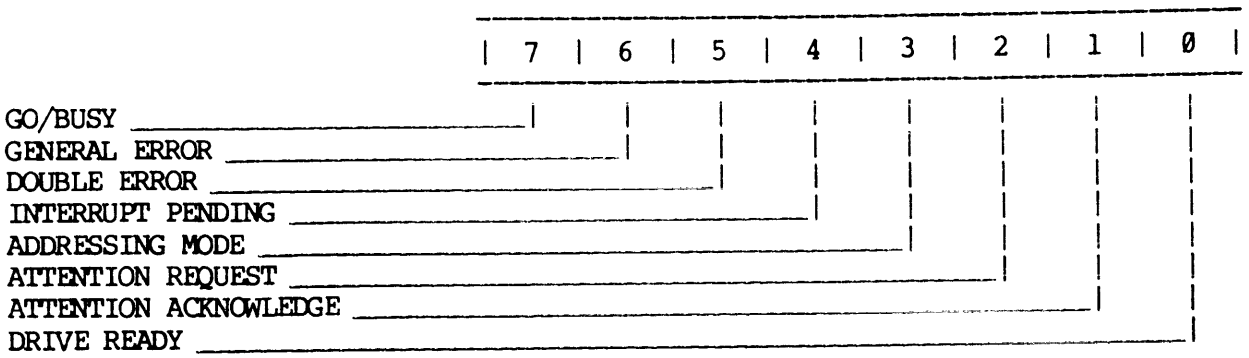
2.3.2.2 Address Registers

There are two Address Registers containing the low and high byte of the IOPB address. These registers are the least significant portion of the IOPB memory address. On power-up these registers are cleared by the 472.

2.3.2.3 Controller Status Register

This register is used to start 472 operation and to report status of the controller.

Controller Status Register



BIT	MNEMONIC	ACCESS	MEANING
7	GBSY	R/W	Go/Busy Bit - set it to start a transfer. GBSY remains set until the 472 completes the current IOPB command or command-chain. The 472 then clears GBSY to show readiness for another IOPB operation.
6	ERR	R/W	General Error Bit - indicates that a hard error has been encountered. This bit must be cleared before another command can be executed by either writing a 1 to this bit or executing a Controller Reset. Set only on fatal errors.
5	DERR	R	Double Error - if ERR is set and this bit is set, a Double Error is indicated. A Double Error indicates that an error occured and a previous error condition has not been cleared. This usually means that the 472 cannot properly DMA the Status bytes to memory as a result of an error. A single or double error is cleared by writing a 1 to ERR or by a Controller Reset. If bit 6 (ERR) is not set, bit 5 set indicates that the status bits in the CSR are invalid The program must wait for bit 5 to clear before interpreting CSR status.

NOTE

It is more efficient to clear an error on the 472 by writing a one to bit 6 (ERR) than by Controller Reset.

4	IPND	R/W	Interrupt Pending Bit - indicates that an IOPB is complete, the 472 has interrupted, and the interrupt has not been serviced. The interrupt service routine must clear this condition by writing a 1 to this bit or by executing a Controller Reset before another command (except IOPB update) can be executed. This and AREQ are the only two bits that can be written into the CSR while the 472 is busy.

2.3.2.3 Controller Status Register (continued)

NOTE

It is more efficient to acknowledge an interrupt by writing a one to bit 4 (IPND) than by a Controller Reset.

BIT	MNEMONIC	ACCESS	MEANING
3	ADMD	R	Addressing Mode - when clear, indicates that the 472 is stapled for 20-bit addressing mode. When this bit is set it indicates the 472 is in 24-bit addressing mode. The addressing mode is selected by a hardware jumper on the 472 Board. The controller addressing mode is not software selectable.
2	AREQ	R/W	Attention Request - is used to gain the attention of the 472 when it is busy processing commands. It is used in conjunction with AACK, Attention Acknowledge. Software sets AREQ and waits until the 472 acknowledges the attention request with AACK. When AACK is set, system software may remove completed IOPBs and add new IOPBs. When work on the IOPB chain is complete, AREQ should be cleared by software, the 472 will clear AACK and resume operation.
1	AACK	R	Attention Acknowledge - is set by the 472 to acknowledge an AREQ by the system software. It is cleared after AREQ is cleared. If Interrupt on each IOPB (IEI) is enabled, an interrupt occurs when the controller sets this bit.
Ø	DRDY	R	Drive Ready - sets when the currently selected drive is online. After a Controller Reset drive Ø is automatically selected and its ready status is latched. Execution of any IOPB selects the drive specified in the IOPB Unit Select byte and displays the selected drive status in DRDY.

NOTE

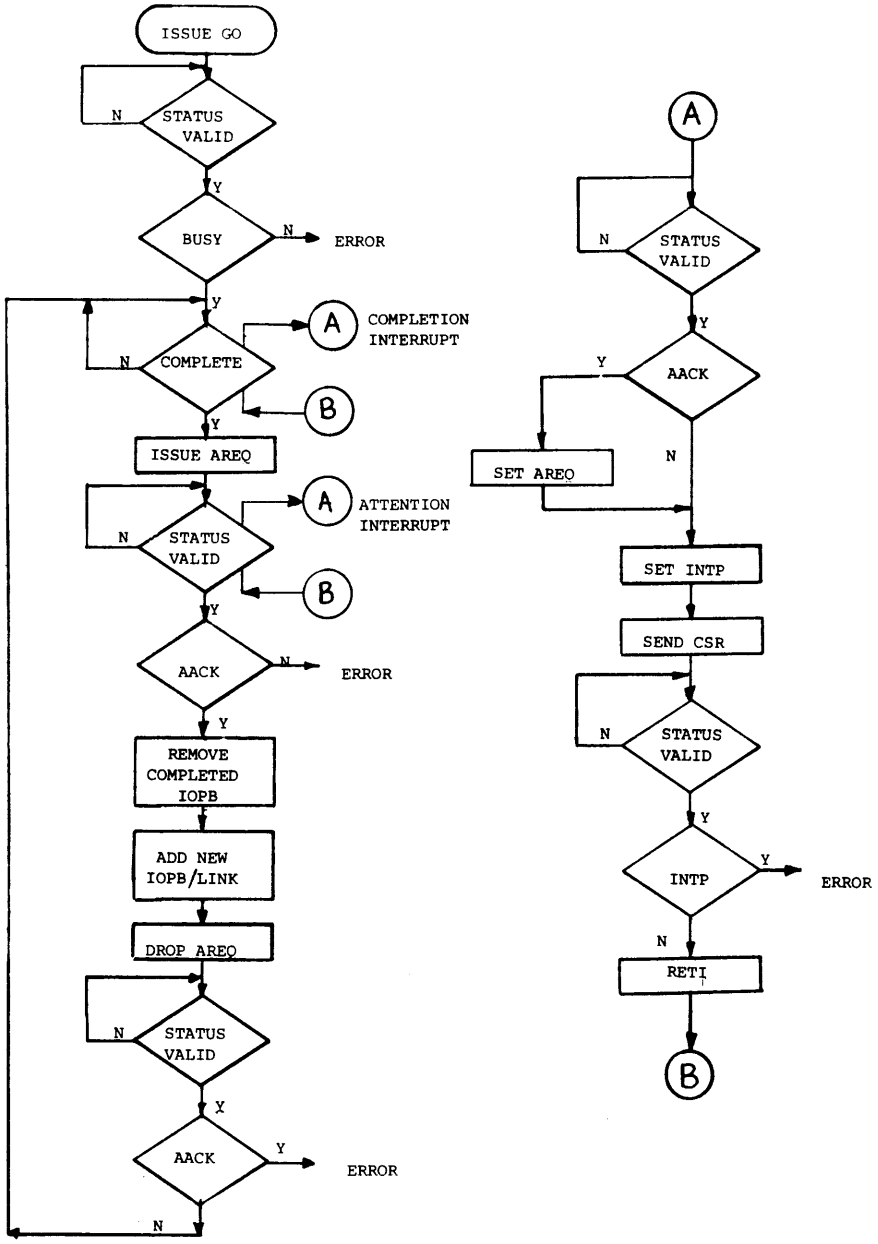
While the controller is busy the only write access allowed to the controller registers is bits 2 & 4 of the CSR.

2.3.2.3.1 Read Control Status Register Protocol

The CSR consists of a write register (control) and a read register (status). When the CSR is written by the system, the 472 will post status invalid (AØH) in the CSR as read by the system to indicate that the 472 is busy updating its internal registers. When reading the CSR to do a bit test, a compare should be made with the value AØH and if true the CSR should be read again. When the 472 has updated its internal registers, it will clear (AØH) and post the correct status. The first CSR read that is not equal to AØH will have a valid status and the bit test can be done. A CSR read in an interrupt handler must follow this protocal even if it is not proceeded by a CSR write. The CSR may have been written just prior to the interrupt.

Inline Code

Interrupt Handler



FLOWCHART 2-1. TYPICAL IOPB CHAIN HANDLER

2.3.2.4 Controller Reset/Update IOPB Register

This is a special register whose functions are:

1. When the Controller Reset/Update IOPB Register is READ, the 472 performs a Controller Reset, i.e., the registers will be cleared and IPND, ERR, DERR will be cleared, drive Ø will be reselected, and the ready status latched. READING this register will cause the 472 to go busy while it executes the clear function. The programmer should wait for not busy before issuing commands.

2.3.2.4 Controller Reset/Update IOPB Register

2. When the Controller Reset/Update IOPB Register is WRITTEN (actual data written is insignificant), the 472 updates the IOPB whose address is currently stored in the Address and Relocation Registers. The Update IOPB command writes the information contained in the 472 internal registers back to the current IOPB. Writing this register will cause the 472 to go busy (GBSY) until the update is complete. The programmer should wait for not busy before issuing commands.

2.4 IOPB DESCRIPTION

BYTE ADDRESS (HEX)	DESCRIPTION	MNEMONIC
Ø	Command	COMM
1	Subfunction	SUBFUN
2	Status Byte 1	STAT1
3	Status Byte 2	STAT2
4	Status Byte 3	STAT3
5	Interrupt Mode	IMODE
6	Throttle	THROT
7	Unit Select	DRIVE
8	Count Low	CNTL
9	Count High	CNTH
A	Data Address Low	DATAL
B	Data Address High	DATAH
C	Data Relocation Low	DATARL
D	Data Relocation High	DATARH
E	Next IOPB Address Low	NIOPL*
F	Next IOPB Address High	NIOPH*
1Ø	Actual Count Low	ACNTL
11	Actual Count High	ACNTH

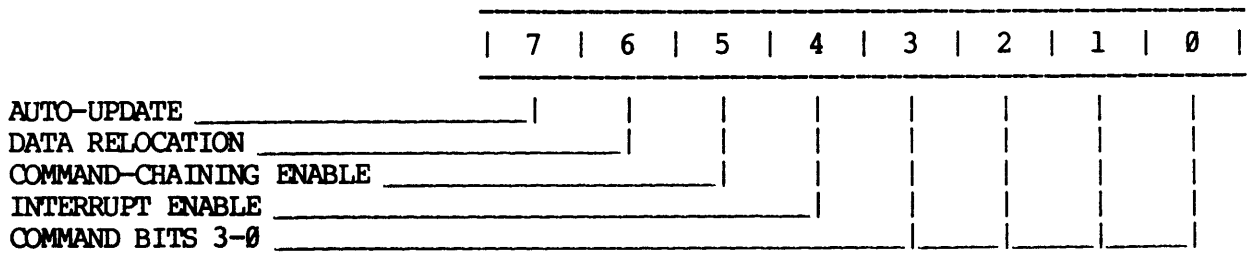
TABLE 2-2. 472 IOPB BYTE UTILIZATION

NOTE

* All IOPBs in a chain must exist in the same 64K byte segment whose base address is specified by the 472 IOPB Relocation Registers.

2.4.1 Command Byte (IOPB Byte Ø)

Command Byte - (COMM)



2.4.1 Command Byte (IOPB Byte 0) (continued)

BIT	MNEMONIC	MEANING
7	AUD	Auto-Update - when clear only Status bytes 1 and 2 are updated. When set the current IOPB is updated upon its completion. Status bytes 1, 2 and 3 are updated for all commands. For read or write commands the Data Address and Relocation Address are updated and used as pointers to the end or beginning of the memory buffer depending on the direction of the command. Also the Actual Count bytes are updated if supported by the command issued.
6	RELO	Data Relocation - if clear, Multibus data addresses are generated as 16-bit values, bits 16 through 23 are set to zero, and the Data Relocation Address bytes are ignored. If set, physical Multibus addresses are formed as shown in Figure 2-1. This bit enables only data relocation. IOPB relocation occurs whenever the IOPB Relocation registers are non-zero.
5	CHEN	Chaining Enable - if clear, the 472 executes the current IOPB and clears GBSY upon completion. If set, the 472 starts processing the next IOPB. The new IOPB's address is specified in the Next IOPB Address bytes.
4	IEN	Interrupt Enable - if clear, the 472 will not generate interrupts. If set, the 472 generates appropriate interrupts as defined by the Interrupt Mode byte.
3-0	COM	Command - See Section 2.5 for detailed descriptions. Interpreted in Table 2-3 as follows:

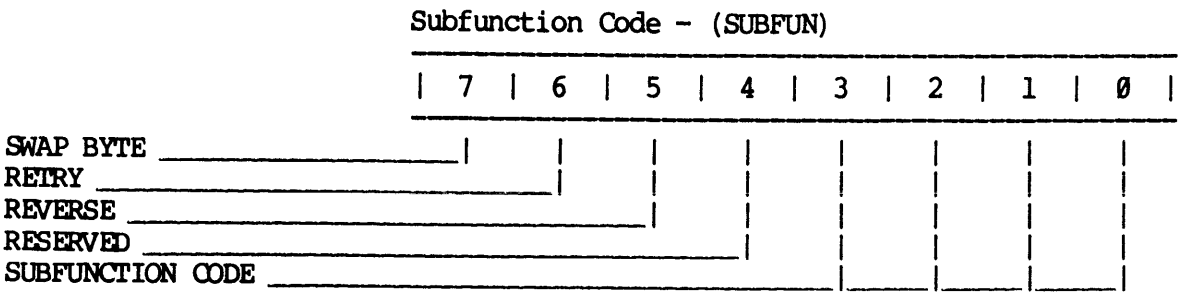
Hex Value	Bits 3 2 1 0	Command
0	0 0 0 0	No Operation (NOP)
1	0 0 0 1	Write
2	0 0 1 0	Read
3	0 0 1 1	Reserved
4	0 1 0 0	Reserved
5	0 1 0 1	Position
6	0 1 1 0	Drive Reset
7	0 1 1 1	Write Tapemark/Erase
8	1 0 0 0	Reserved
9	1 0 0 1	Read Drive Status
A	1 0 1 0	Reserved
B	1 0 1 1	Set Parameters
C	1 1 0 0	Self Test
D	1 1 0 1	Reserved
E	1 1 1 0	Reserved
F	1 1 1 1	Reserved

TABLE 2-3. 472 COMMANDS

2.4.2 Subfunction Code (IOPB Byte 1)

Each command may have one or more subfunctions associated with it as specified in Section 2.5. This byte has both bit encoded and bit flag fields associated with the actual subfunction code.

2.4.2 Subfunction Code (IOPB Byte 1) (continued)



BIT	MNEMONIC	MEANING
7	SWAP	Swap Byte - when set indicates that the operation specified in the Subfunction Code will be performed with the most significant byte in the word swapped with the least significant byte. This feature is used for data transfer and allows compatibility with machines that order their bytes in a word opposite that of the Multibus (referred to as IBM format compatibility). When clear the bytes are ordered as they normally appear in Multibus memory. Reference Section 2.5 for further detail.
6	RETY	Retry - when set indicates that the requested operation specified will be retried up to four times before returning a hard error code if an error occurs.
5	REV	Reverse - when set indicates the operation is to be performed in the reverse direction on the tape.
4	-	Reserved
3-0	SUBF	Subfunction Code - most of the 472 commands (IOPB Command Byte) have subfunction codes associated with them. The actual subfunction code is defined by the command (see Table 2-4). Reference Section 2.5 for detailed description of each subfunction command.

COMMAND CODE	COMMAND	SUBFUN CODE	DESCRIPTION
1	Write	00	Write
		40	Write Retry
		80	Write Swap Byte
		C0	Write Retry Swap Byte
2	Read	00	Read Next
		20	Read Previous
		40	Read Next Retry
		60	Read Previous Retry
		80	Read Next Swap Bytes
		A0	Read Previous Swap Bytes
		C0	Read Next Retry Swap Bytes
		E0	Read Prev. Retry Swap Bytes
7	Write Tapemark/Erase	00	Write Tape Mark
		01	Erase
		40	Write Tape Mark Retry

TABLE 2-4. SUBFUNCTION CODES

2.4.2 Subfunction Code (IOPB Byte 1) (continued)

COMMAND CODE	COMMAND	SUBFUN CODE	DESCRIPTION
9	Read Drive Status	00	Completion Codes
		01	Read Sense Bytes
		02	Read Extended Sense Bytes
B	Set Parameters	00	Set PE Mode
		01	Set GCR Mode
		02	Set Low Speed
		03	Set High Speed

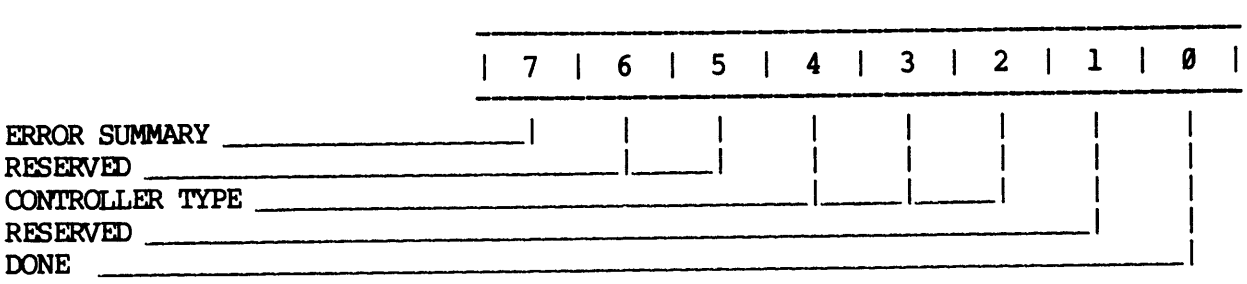
TABLE 2-4. SUBFUNCTION CODES

NOTE

If retries are enabled, up to four tries will be performed automatically unless the error clears. If the error does not clear, IOPB processing will be terminated (general error). If retries are disabled, all hard errors will cause IOPB termination.

2.4.4 Status Byte 1 (IOPB Byte 2)

Status Byte 1 - (STAT1)



BIT	MNEMONIC	MEANING
7	ERRS	Error Summary - when set indicates an error occured during IOPB processing. Clear indicates successful completion.
6-5	-	Reserved
4-2	CTYP	Controller Type - Each Xylogics Multibus controller has been assigned a controller type code as follows:

Bit 4	Bit 3	Bit 2	Controller
0	0	0	440
0	0	1	450
0	1	0	472

1	-	Reserved
0	DONE	Done - when set, Status Byte 2 holds the Completion Code for the IOPB.

2.4.4 Status Byte 1 (IOPB Byte 2) (continued)

NOTE

Status bytes 1, 2 and 3 must be cleared by software before giving the IOPB to the 472.

2.4.5 Status Byte 2 (IOPB Byte 3) (STAT2)

When IOPB processing has been completed, Status Byte 2 contains its Completion Code. Completion Codes are summarized in Table 2-5 and described, with any required corrective action, in the sections that follow. Unless otherwise noted, either writing a 1 into ERR or Controller Reset will clear a hard error. Hard errors stop the controller and thus stop the processing of a command chain. To continue, the hard error must be cleared and the controller restarted. Status errors do not stop IOPB processing.

CODE	TYPE	DEFINITION
ØØ	Status	Successful Completion - No Errors
Ø1	Hard	Interrupt Pending
Ø2	-	Reserved
Ø3	Hard	Busy Conflict
Ø4	Hard	Operation Time Out
Ø5	-	Reserved
Ø6	Hard	Uncorrectable Data
Ø7	-	Reserved
Ø8	-	Reserved
Ø9	-	Reserved
ØA	-	Reserved
ØB	-	Reserved
ØC	-	Reserved
ØD	-	Reserved
ØE	Hard	Slave ACK Error (Non-existent Memory)
ØF	-	Reserved
1Ø	-	Reserved
11	-	Reserved
12	-	Reserved
13	-	Reserved
14	Hard	Write Protect Error
15	Hard	Unimplemented Command
16	Hard	Drive Offline
17	-	Reserved
18	-	Reserved
19	-	Reserved
1A	Hard	Self Test A Failed
1B	Hard	Self Test B Failed
1C	Hard	Self Test C Failed
1D	Hard	Tape Mark Failure
1E	Hard	Tape Mark Detected on Read
1F	Status	Corrected Data
2Ø	-	Reserved
21	-	Reserved

TABLE 2-5. SUMMARY OF COMPLETION CODES

2.4.5 Status Byte 2 (IOPB Byte 3) (STAT2) (continued)

CODE	TYPE	DEFINITION
22	Hard	Record Length Short
23	Hard	Record Length Long
24	-	Reserved
25	-	Reserved
26	-	Reserved
27	-	Reserved
28	-	Reserved
29	-	Reserved
30	Hard	Reverse into BOT
31	Hard	EOT Detected

TABLE 2-5. SUMMARY OF COMPLETION CODES

2.4.5.1 Status Code Descriptions

ØØ Successful Completion - Not an error, it indicates that the command is complete and the packet may be removed from the queue.

Ø1 Interrupt Pending Error -- This error occurs when an operation is attempted with an interrupt pending. Only Interrupt Acknowledge, Update IOPB, Error Reset or Controller Reset operations are allowed while an interrupt is pending.

Ø2 Reserved

Ø3 Busy Conflict -- This error occurs if a register write is tried while the 472 is busy. Bits 2 (AREQ) and 4 (IPND) of the CSR are the only bits that can be written while the 472 is busy.

Ø4 Operation Timeout - Requested operation did not complete within the 472 operation timeout window which is in the order of several seconds.

Ø5 Reserved

Ø6 Uncorrectable Data - Data error; retry the operation or erase tape.

Ø7-ØD Reserved

ØE Slave ACK Error (Non-Existent Memory) -- This error occurs if the memory addressed by the 472 fails to respond within the 472 slave ACK timeout window which is in the order of several seconds. Validate the memory address or memory itself and retry the command.

ØF Reserved

1Ø-13 Reserved

2.4.5.1 Status Code Descriptions (continued)

14 Write Protect Error -- This error occurs when attempting a Write operation on a write protected tape reel. Remove the write protect ring and retry the write operation.

15 Unimplemented Command -- This error occurs on all reserved commands or invalid subfunctions.

16 Drive Offline -- Requested operation could not be performed because selected drive is offline. If the tape is properly loaded and the drive ONLINE indicator is illuminated, check these possible causes:

- o bad or improperly connected cable,
- o no drive of the specified unit number connected to the 472,
- o Signal "ACLO" on Multibus backplane connector P2 is low.

17-19 Reserved

1A Self Test A Failure - Either the microprocessor or its internal RAM failed diagnostics.

1B Self Test B Failure - Either the microprocessor or address counter test has failed.

1C Self Test C Failure - Either the microprossor or data buffer test has failed.

1D Tape Mark Failure - Tape mark was not detected during a write tape mark operation.

1E Tape Mark Detected - Tape mark detected on a read, no data was transferred.

1F Corrected Data - Read data had a single bit error and was corrected prior to DMA.

20-21 Reserved

22 Record Length Short - Record length was shorter than expected, part of the read buffer has not been used.

23 Record Length Long - Record length was longer than expected, only the requested byte count was transfered.

24-29 Reserved

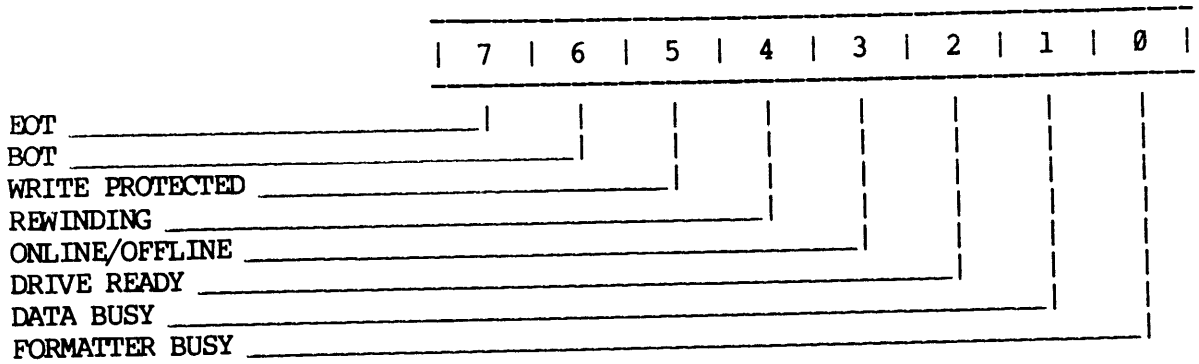
30 Reverse into BOT - Begining of tape marker detected while moving in the reverse direction, tape motion will cease.

31 EOT Detected - The end of tape reflector marker has been passed in the forward direction.

2.4.6 Status Byte 3 (IOPB byte 4)

This byte contains eight drive status flags. The flag bits are actual tape drive interface lines which are updated on a command by command basis. If the auto-update bit (AUD) in the Command byte is set, the command has it's flags updated upon completion.

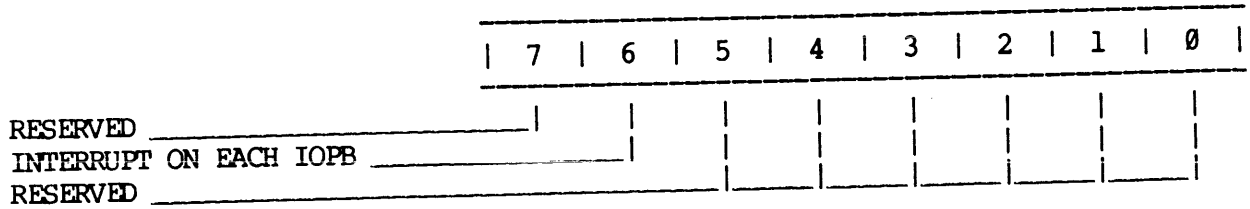
Status Byte 3 - (STAT3)



BIT	MNEMONIC	MEANING
7	EOT	End of Tape - if set the EOT marker has been reached. Will remain set for any commands issued beyond EOT. Programmer determines further actions.
6	BOT	Beginning of Tape - if set the BOT marker has been reached. Tape is now at load point.
5	FPT	Write Protected - if set mounted tape is write protected.
4	REW	Rewinding - if set selected tape drive is rewinding.
3	ONL	Online/Offline - if set indicates the drive selected is online. When clear drive is offline.
2	RDY	Drive Ready - if set the drive is ready to accept a command.
1	DBY	Data Busy - if set the selected drive has encountered data.
Ø	FBY	Formatter Busy - if set indicates that the selected drive is executing a command. Remains set until completion of command execution.

2.4.3 Interrupt Mode (IOPB Byte 5)

Interrupt Mode - (IMODE)



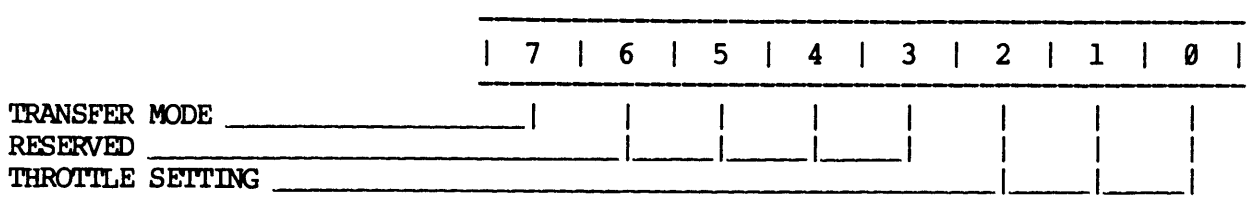
2.4.3 Interrupt Mode (IOPB Byte 5) (continued)

BIT	MNEMONIC	MEANING
7	-	Reserved
6	IEI	Interrupt On Each IOPB - when interrupts are enabled, and IEI is set, the 472 will interrupt each time an IOPB is completed or when AACK is set in the CSR.
5-Ø	-	Reserved

2.4.7 Throttle (IOPB Byte 6)

The Throttle byte selects the number of DMA cycles in a DMA burst and word or byte mode data transfers.

Throttle -- (THROT)



BIT	MNEMONIC	MEANING
7	BWM	Transfer Mode - selects either word or byte DMA transfers between the 472 and system memory allowing the 472 to operate with word- and byte-oriented memory. BWM should be clear when transferring 16-bit words and should be set when transferring 8-bit bytes.
6-4	-	Reserved
2-Ø	THRO	Throttle Setting - selects the maximum number of DMA cycles the 472 executes each time it assumes bus mastership as shown in Table 2-6. During one DMA cycle, one word or one byte (depending on BWM) is transfered. This throttle value determines the DMA burst length for both data and IOPB DMA transfers.

Value of Bits 2-Ø	DMA Cycles	Average Bus Utilization (us)
Ø	2	1.6
1	4	3.Ø
2	8	5.8
3	16	11.4
4	32	22.6
5,6,7	64	45.Ø

TABLE 2-6. 472 THROTTLE SETTING

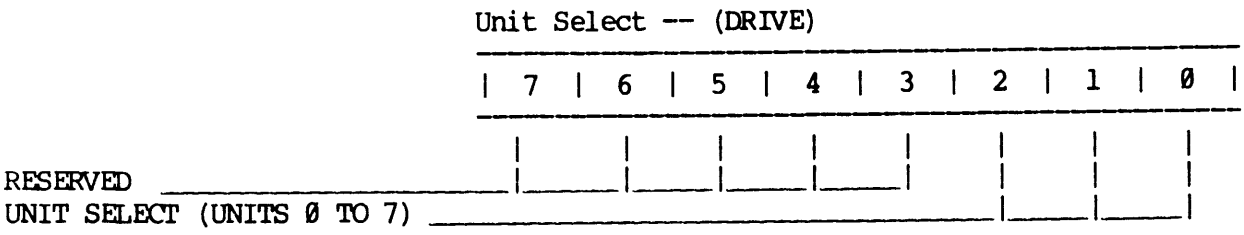
NOTE

The above bus utilization times were calculated using a memory XACK response during a write of 3Ø0ns. For other memory XACK response times use the following formula to determine your average bus utilization.

2.4.7 Throttle (IOPB Byte 6) (continued)

[XACK Response Time + 400ns (472 overhead)] X Number of DMA cycles (words) + 200ns (busack/req) = Bus Usage (usec).

2.4.8 Unit Select (IOPB Byte 7)



BIT	MNEMONIC	MEANING
7-3	-	Reserved
2-0	UNIT	The Unit Select bits contain the physical unit number of one of the eight possible units to be accessed.

2.4.9 Count (IOPB Bytes 8 and 9) (CNTL & CNTH)

The 472 tape controller transfers information in bytes. The byte count, a 16-bit number stored as 2 bytes in the IOPB, is the number of bytes to be transferred. Byte 8 of the IOPB is the least significant half of the byte count while byte 9 is the most significant half. With a 16-bit byte count you can execute a continuous transfer of up to 65,535 bytes with one IOPB.

The Count byte is also used in conjunction with the Position commands. The number of records or tape marks to be spaced is specified with these bytes.

2.4.10 Data Address (IOPB Bytes A and B) (DATAL & DATAH)

The Data Address is composed of two bytes. Byte A is the Data Address Low byte, and byte B is the Data Address High byte. The Data Address is the memory address to or from which a data transfer will start. The 16-bit Data Address is added to a shifted Data Relocation word to form the physical starting address of a data transfer (Figure 2-1).

2.4.11 Data Relocation Pointer (IOPB Bytes C and D) (DATARL & DATARH)

The Data Relocation Pointer is composed of two bytes in the IOPB. Byte C is the low byte and byte D is the high byte. When forming a physical address, the Data Relocation bytes and Data Address bytes are used to create Multibus addresses, as shown in Figure 2-1. However, the Data Relocation bytes are ignored if RELO is clear in the IOPB Command byte.

2.4.12 Next IOPB Address (IOPB Bytes E and F) (NIOPL & NIOPH)

When using command chaining, the starting address of the next IOPB must be specified. These two bytes (E and F) are combined with the IOPB Relocation registers to determine the next IOPB address. They are the link in the IOPB chain.

2.4.12 Next IOPB Address (IOPB Bytes E and F) (NIOPL & NIOPH) (continued)

Byte E is the low byte and byte F is the high byte of the Next IOPB Address. These two bytes make up a 16-bit address similar to the IOPB Address Registers. The Next IOPB Address is added to the IOPB Relocation Registers to form a physical address (Figure 2-1). This physical address is 20- or 24-bits in length, depending on the addressing mode jumper, and is used as the pointer to the next IOPB in the chain.

All IOPBs in a chain are relative to the same relocation address and thus must be within a 64K byte block of memory. To enable command chaining, set CHEN in the Command byte of each IOPB except the last. If command chaining is not enabled bytes E and F are ignored.

2.4.13 Count Actually Read (IOPB Bytes 10 and 11) (ACNTL & ACNTH)

On a READ command, the number of bytes actually read is returned in bytes 10 (low) and 11 (high). On a SPACE command, the number of records actually spaced over is posted. On a SKIP TAPEMARK command, the number of files actually skipped is posted. These bytes are useful in determining the number of bytes transferred when a record length short status code is returned.

2.5 COMMANDS

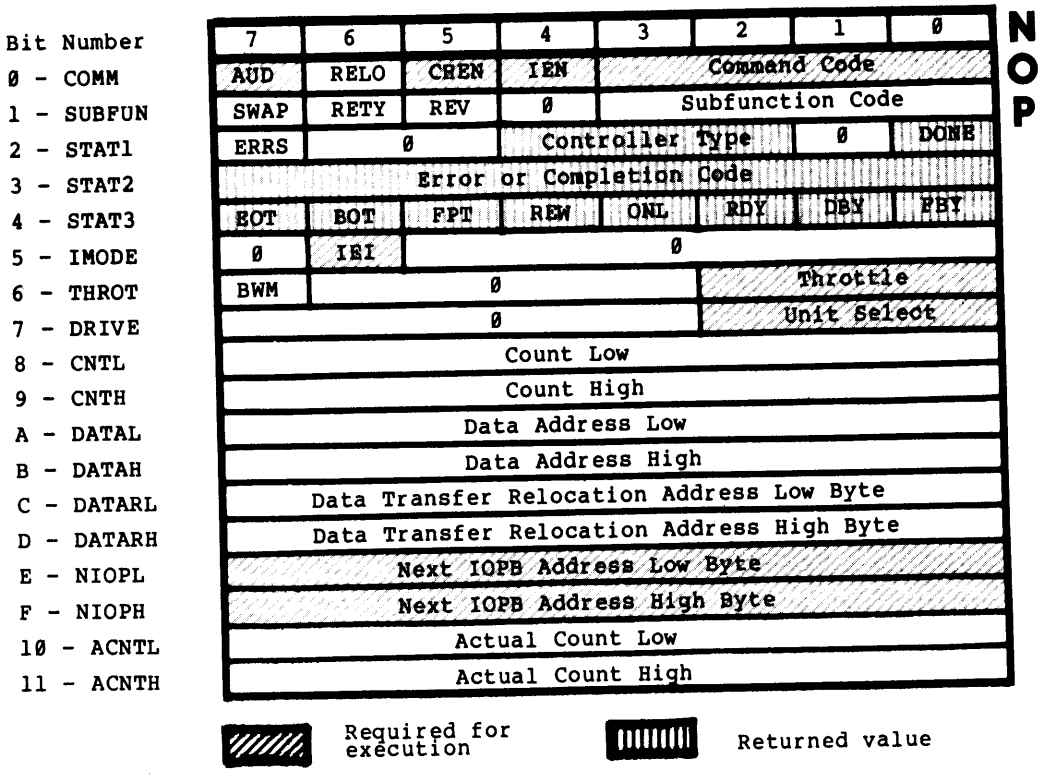
The four least-significant bits of the Command byte are the IOPB Command bits. These four bits allow up to sixteen possible commands of which seven command codes are reserved for future use. The commands are transfered to the 472 via an 18 byte long IOPB. Subfunction codes allow additional flexibility in command definition.

2.5.1 NOP Command (Command Code 0)

2.5.1.1 General

The No Operation (NOP) command causes the controller to select a tape drive and set its status in DRDY (bit 0 of CSR).

2.5.1.2 IOPB



2.5.2 Write Command (Command Code 1)

2.5.2.1 General

The Write command is the standard command used to transfer a record of data to the tape. It transfers data from the memory buffer pointed to by the IOPB transfer address and relocation words to the tape.

2.5.2.2 IOPB

WRITE

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - SUBFUN	SWAP	RETY	REV	0	Subfunction Code			
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - STAT3	EOT	BOT	FPT	REW	ONL	RDY	DBY	FBY
5 - IMODE	0	IEI	0					
6 - THROT	BWM	0				Throttle		
7 - DRIVE	0					Unit Select		
8 - CNTL	Count Low							
9 - CNTH	Count High							
A - DATAL	Data Address Low							
B - DATAH	Data Address High							
C - DATARL	Data Transfer Relocation Address Low Byte							
D - DATARH	Data Transfer Relocation Address High Byte							
E - NIOPL	Next IOPB Address Low Byte							
F - NIOPH	Next IOPB Address High Byte							
10 - ACNTL	Actual Count Low							
11 - ACNTH	Actual Count High							

Required for execution Returned value

2.5.2.3 Write Command Error Handling

The write command will abort if the tape is write protected, the drive is offline, or an illegal subfunction is specified. The tape drive and DMA will be started simultaneously, this way the 472 buffer is partially full by the time the drive needs the first byte. DMA is continued until the specified byte count is transfered and tape writing is continued until the buffer is emptied. The 472 then waits for drive not busy and checks EOT error status.

On reaching EOT, the program should execute an end of volume routine. The

2.5.2.3 Write Command Error Handling (continued)

472 will not prevent reading or writing past EOT, however the EOT flag will set and a hard error code will be issued which will break an IOPB chain. The 472 if so enabled by a subfunction code, will automatically retry a write until the error is cleared or the retry count (4) is exhausted. The latter condition is considered a fatal error and will halt IOPB execution.

2.5.2.4 Throttle

The throttle is the maximum number of transfers that will be allowed each time the 472 becomes bus master. On a write operation the first DMA bursts will be at maximum specified throttle value until the buffer is full. After data starts moving to the tape, the typical burst will be less than the throttle value. Data will continue to be transfered into the controller as required until the byte count goes to zero.

2.5.2.5 Completing a Transfer

The byte count will be decremented until the the specified number of bytes are transferred. When the transfer is complete, the Status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. If the auto-update bit of the IOPB command byte was set, the IOPB will be updated. Status bytes 1, 2, 3, Actual Count bytes and the Data and Relocation Address bytes are updated. The Data and Relocation bytes are used as pointers to the last buffer location plus one (Figure 2-2).

Write a 9 byte record with a starting address of 1000H.

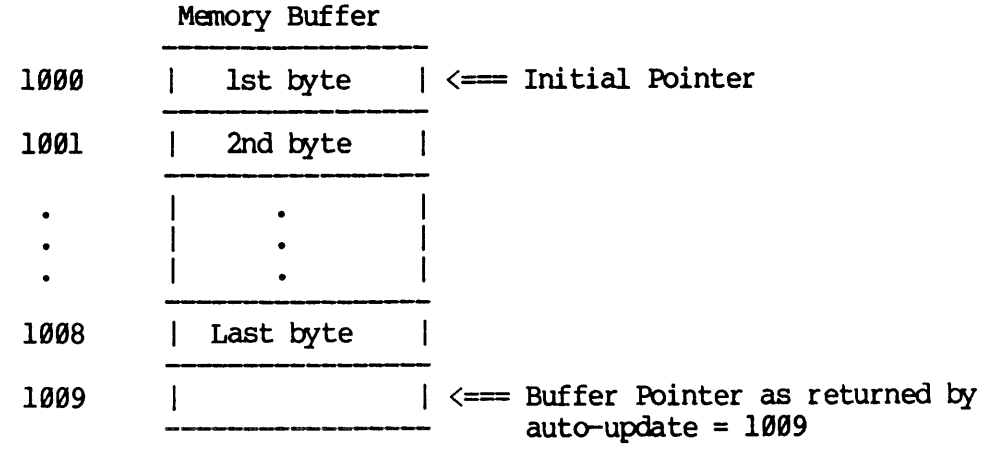


FIGURE 2-2. WRITE BUFFER POINTER AFTER AUTO UPDATE

If the transfer ends in a hard error, it is stopped, the Status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. Any chained operations will be halted. The IOPB Address and Relocation registers will be pointing to the IOPB which caused the error. If the auto-update bit of the IOPB command byte was set, the IOPB will be updated.

2.5.2.5 Completing a Transfer (continued)

If the transfer ends with a soft error, the Status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. Any chained operations will be continued. If the auto-update bit of the IOPB Command byte was set, the IOPB will be updated. The ERR bit of the CSR will not be set since this is a soft error.

2.5.2.6 Write Subfunction Codes

There are four subfunctions associated with the write command. They are write, write with retry, write swap bytes and write with retry swap bytes.

Code 00 - Write: transfers are made from memory to tape according to the IOPB Address and Byte count. Retries are disabled and on an error, IOPB execution is halted.

Code 40 - Write (with retry): same as write but up to four retries are automically attempted if the write operation fails. If the retry count is exhausted without clearing the error a hard error is indicated and the programmer must take appropriate action.

Code 80 - Write Swap Bytes: same as write except the most significant byte of the word is swapped with the least significant byte. This subfunction allows compatibility with machines that order their bytes in a word opposite that of the Multibus.

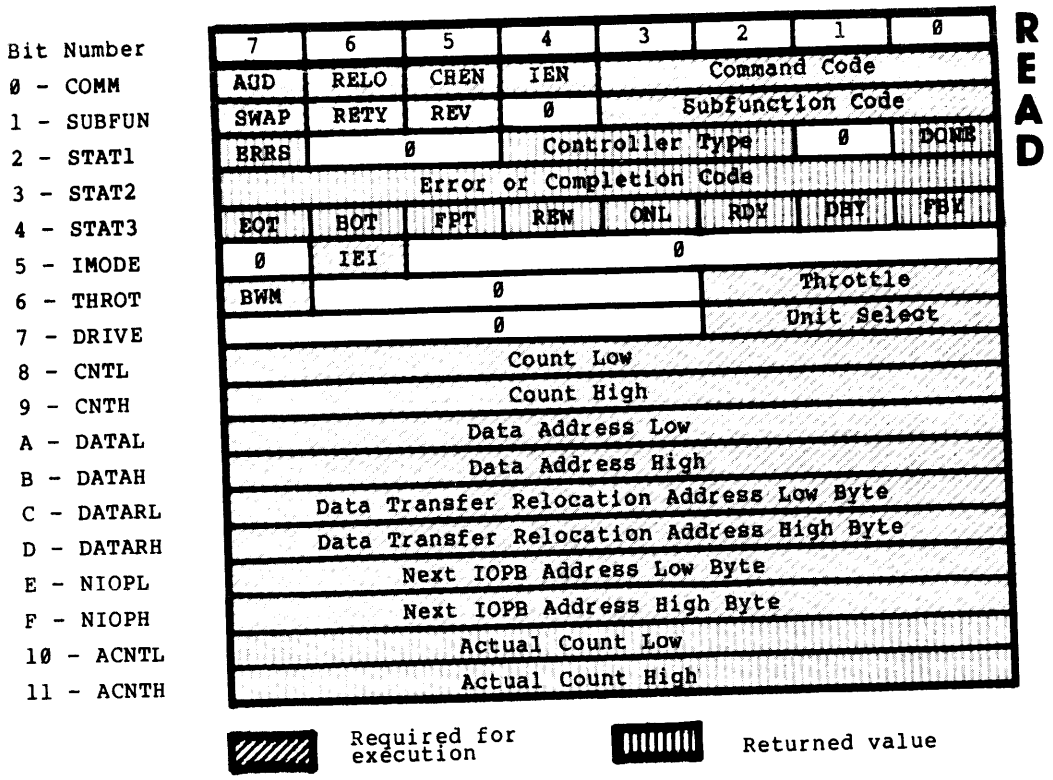
Code C0 - Write Swap Bytes (with retry): swap byte format with retries enabled.

2.5.3 Read Command (Command Code 2)

2.5.3.1 General

The Read Command transfers data from the tape to memory. Data is tranferred from the current record into the memory buffer pointed to by the IOPB Address and Relocation bytes.

2.5.3.2 IOPB



2.5.3.3 Read Command Error Handling

The Read command will be aborted if the drive is offline or an illegal subfunction code is specified. A read reverse will transfer data starting at the top of the memory buffer with addresses decremented rather than incremented, this results in the record being "right side up" in memory.

The drive is started and drive busy is timed out in case the record was written at the wrong density. Then the DMA is started and also timed out in case the record is shorter than the byte count. In the latter case, record length short error status results and the actual bytes read will be posted. Otherwise, DMA will complete when the byte count overflows. If the on-board buffer is not empty at this time, record length long error status results.

2.5.3.3 Read Command Error Handling (continued)

The 472 will wait for drive not busy and check actual bytes read, corrected error, EOT or reverse into BOT, hard error, record length short or long, and tape mark detected. If an error was corrected, the programmer should log the error but the data in memory will be correct. If EOT is reached futher reads should be limited to avoid running off the end of tape. If reverse into BOT is detected, no futher read reverse commands should be sent as the tape drive will not read reverse beyond BOT. If a tape mark was detected no data was transferred. If retries are enabled, the 472 will automatically retry a read until the error clears or the retry count (4) is exhausted. The latter will result in a hard error and will halt IOPB execution.

2.5.3.4 Throttle

The throttle is the maximum number of transfers that will be allowed each time the 472 becomes bus master. On a read operation the first DMA bursts will be at minimum value since the limiting factor of the DMA burst length is the number of words available from the FIFO. After the initial few DMA bursts, the typical burst length will increase, possibly approaching the throttle limit. Data will continue to be transfered from the controller as required until the byte count goes to zero or the buffer is empty.

2.5.3.5 Completing a Transfer

When the transfer is complete, the status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. If the auto-update bit of the IOPB Command byte was set, the IOPB will be updated. The Status bytes, Actual Count bytes and the Data and Relocation bytes are updated. On a read forward the Data and Relocation bytes are pointing to the last buffer location plus one, exactly the same as a write command (Figure 2-3A). On read reverse the pointer is first decremented by one (programmer transparent) and now is pointing at the last location in the buffer and the transfer begins. When complete the Data and Relocation bytes are pointing to the first location in the buffer (Figure 2-3B).

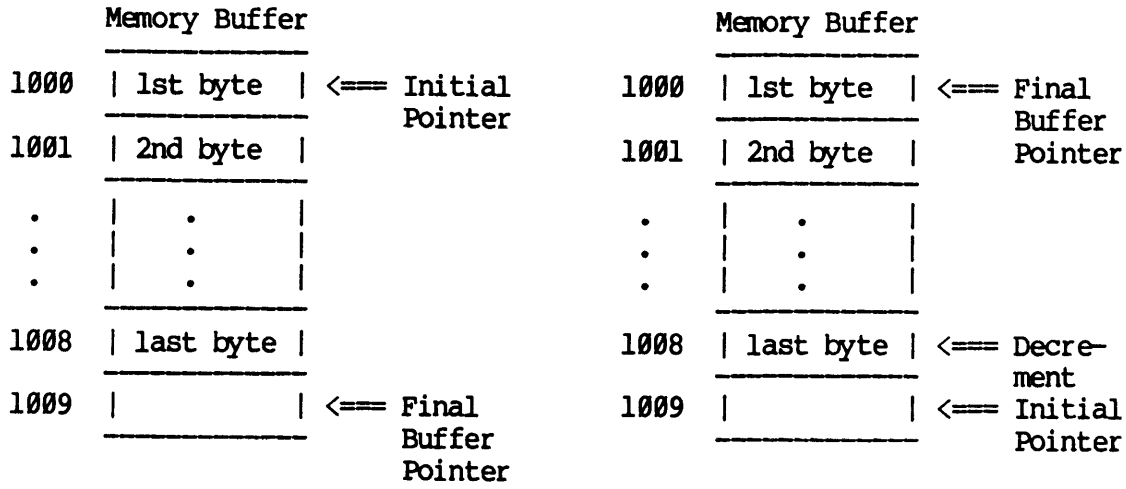


FIGURE 2-3. READ BUFFER POINTERS AFTER AUTO UPDATE

2.5.3.5 Completing a Transfer (continued)

If the transfer ends in a hard error, the transfer is stopped, the status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. Any chained operations will be halted. The IOPB address and relocation registers will be pointing to the IOPB which caused the error. If the auto-update bit of the IOPB command byte was set, the IOPB will be updated.

If the transfer ends with a soft error, the status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. Any chained operations will be continued. If the auto-update bit of the IOPB Command byte was set, the IOPB will be updated. The ERR bit in the CSR will not be set since this is a soft error.

2.5.3.6 Read Subfunction Codes

There are eight subfunctions for the read command. Their use is as follows;

Code 00 - Read Next: read in the forward direction from tape to memory as specified by the Data Address and Byte count. On any error IOPB execution is aborted. The buffer address should point to the lowest address in the buffer.

Code 20 - Read Previous: read in the reverse direction from tape to memory as specified by the Data Address and Count bytes. On any error, IOPB execution is aborted. The buffer address should point to the highset address plus one in the buffer.

Code 40 - Read Next (with retry): same as Read Next but with retries enabled. If retry count is exhausted, a hard error is reported and IOPB execution is halted.

Code 60 - Read Previous (with retry): same as Read Previous but with retries enabled.

Code 80 - Read Next Swap Bytes: same as Read Next but swaps position of each pair of bytes in a word read from the tape.

Code A0 - Read Previous Swap Bytes: same as Read Previous but swaps position of each pair of bytes read from tape.

Code C0 - Read Next Swap Bytes (with retry): same as Read Next Swap Bytes but with retries enabled.

Code E0 - Read Previous Swap Bytes (with retry): same as Read Previous Swap Bytes but with retries enabled.

The following figures (2-4 and 2-5) indicate the memory positions for the bytes as they are read from or written on the tape. In these examples, the bytes of data in the block on tape are numbered starting at 0. Byte 0 is always the data byte at the beginning of the block (i.e., that end of the block which is closest to BOT).

2.5.3.6 Read Subfunction Codes (continued)

Swap Bytes = 0
Buffer Address = 1000H
Byte Count = 8

| 1 | 0 | 1000
| 3 | 2 | 1002
| 5 | 4 | 1004
| 7 | 6 | 1006

Swap Bytes = 1
Buffer Address = 1000H
Byte Count = 8

| 0 | 1 | 1000
| 2 | 3 | 1002
| 4 | 5 | 1004
| 6 | 7 | 1006

Swap Bytes = 0
Buffer Address = 1001H
Byte Count = 8

| 0 | | 1000
| 2 | 1 | 1002
| 4 | 3 | 1004
| 6 | 5 | 1006
| | 7 | 1008

Swap Bytes = 1
Buffer Address = 1001H
Byte Count = 8

| | 0 | 1000
| 1 | 2 | 1002
| 3 | 4 | 1004
| 5 | 6 | 1006
| 7 | | 1008

FIGURE 2-4. BYTE SWAP SEQUENCE,
FORWARD TAPE DIRECTION (Read or Write)

Swap Bytes = 0
Buffer Address = 1008H
Byte Count = 8

| 1 | 0 | 1000
| 3 | 2 | 1002
| 5 | 4 | 1004
| 7 | 6 | 1006

Swap Bytes = 1
Buffer Address = 1008H
Byte Count = 8

| 0 | 1 | 1000
| 2 | 3 | 1002
| 4 | 5 | 1004
| 6 | 7 | 1006

Swap Bytes = 0
Buffer Address = 1009H
Byte Count = 8

| 0 | | 1000
| 2 | 1 | 1002
| 4 | 3 | 1004
| 6 | 5 | 1006
| | 7 | 1008

Swap Bytes = 1
Buffer Address = 1009H
Byte Count = 8

| | 0 | 1000
| 1 | 2 | 1002
| 3 | 4 | 1004
| 5 | 6 | 1006
| 7 | | 1008

FIGURE 2-5. BYTE SWAP SEQUENCE,
REVERSE TAPE DIRECTION (Read)

2.5.3.6 Read Subfunction Codes (continued)

Swap Bytes = 0
Buffer Address = 1007H
Byte Count = 7

1	0	1000
3	2	1002
5	4	1004
	6	1006

Swap Bytes = 1
Buffer Address = 1007H
Byte Count = 7

0	1	1000
2	3	1002
4	5	1004
6		1006

Swap Bytes = 0
Buffer Address = 1008H
Byte Count = 7

0		1000
2	1	1002
4	3	1004
6	5	1006

Swap Bytes = 1
Buffer Address = 1008H
Byte Count = 7

	0	1000
1	2	1002
3	4	1004
5	6	1006

FIGURE 2-5. BYTE SWAP SEQUENCE REVERSE TAPE DIRECTION (READ) (Continued)

NOTE

When reading reverse, the first data byte seen on tape is the highest numbered byte. The read reverse command stores data in the buffer from top to bottom (high address to low address) so the result the same as reading forward.

2.5.4 Position (Command Code 5)

2.5.4.1 General

The position commands move tape forward and reverse as specified in the Subfunction code and Count bytes without transferring data.

2.5.4.2 IOPB

POSITION

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - SUBFUN	SWAP	RETY	REV	0	Subfunction Code			
2 - STAT1	ERRS	0		Controller Type		0		DONE
3 - STAT2	Error or Completion Code							
4 - STAT3	EOT	BOT	FPT	REW	ONL	RDY	DBY	FBY
5 - IMODE	0	IEI	0					
6 - THROT	BWM	0				Throttle		
7 - DRIVE	0					Unit Select		
8 - CNTL	Count Low							
9 - CNTH	Count High							
A - DATAL	Data Address Low							
B - DATAH	Data Address High							
C - DATARL	Data Transfer Relocation Address Low Byte							
D - DATARH	Data Transfer Relocation Address High Byte							
E - NIOPL	Next IOPB Address Low Byte							
F - NIOPH	Next IOPB Address High Byte							
10 - ACNTL	Actual Count Low							
11 - ACNTH	Actual Count High							

Required for execution Returned value

2.5.4.3 Position Command Error Handling

The command is aborted if the drive is offline or an illegal subfunction is specified.

2.5.4.4 Position Subfunction Codes

Code 00 - Space Records Forward : space forward the number of records specified in IOPB Count field or until a filemark is encountered. Tape motion will cease when a filemark is detected and record length short status will be returned. If auto-update (AUD) is set the actual number of records spaced over is posted in IOPB bytes 10 and 11. If EOT is encountered the EOT flag is set in Status byte 3, a hard error is posted and if the IOPB was chained it is broken. However it is still possible to issue unchained space foward commands.

2.5.4.4 Position Subfunction Codes (continued)

Code 20 - Space Records Reverse : space reverse the number of records specified in the byte count field. A space reverse command will stop if BOT is encountered. If auto-update (AUD) is set the BOT flag will be set in Status byte 3 and IOPB bytes 10 and 11 will have the count of records spaced over.

Code 01 - Skip Tape Marks Forward : skip foward the number of tape marks specified in the IOPB Count bytes. If (AUD) is set the actual number of tape marks skipped are posted in IOPB bytes 10 and 11. Tape motion will not stop if EOT is encountered. The EOT flag in Status byte 3 is set, a hard error is posted and if the IOPB was chained it is broken. To prevent skipping off end of tape, write a tape mark at the logical end of tape.

Code 21 - Skip Tape Marks Reverse : skip reverse the number of tape marks specified in the IOPB Count bytes. A skip reverse will stop tape motion if BOT is encountered. If (AUD) is set the BOT flag in Status byte 3 will be set and the actual number of tape marks skipped will be posted in IOPB bytes 10 and 11.

Code 02 - Rewind : the Rewind command will move tape at high speed in the reverse direction until BOT is encountered. Normally the tape will overshoot BOT and then be positioned at a slow speed exactly at BOT. The rewind command completes immediately following initiation of the rewind. It is up to the programmer to determine when the rewind command is complete by issuing a Get Status command. Subsequent commands to the same drive will automatically wait for the rewind motion to complete.

Code 03 - Unload : the Unload command will move tape at high speed in the reverse direction until BOT is encountered, the tape continues moving at low speed until tension is lost. The drive will then go offline. The unload command completes immediately following initiation of the rewind. It is up to the programmer to determine when the drive has finished rewind and gone off-line using the Get Status command. The operator must load a new tape and place the drive online before any further motion commands can be accepted by the drive.

2.5.5 Drive Reset (Command Code 6)

2.5.5.1 General

This command selects a drive and resets it.

2.5.5.2 IOPB

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - SUBFUN	SWAP	RETY	REV	0	Subfunction Code			
2 - STAT1	ERRS	0		Controller Type		0		DONE
3 - STAT2	Error or Completion Code							
4 - STAT3	EOT	BOT	FPT	REW	ONL	RDY	DBY	FBY
5 - IMODE	0	IEI	0					
6 - THROT	BWM	0				Throttle		
7 - DRIVE	0					Unit Select		
8 - CNTL	Count Low							
9 - CNTH	Count High							
A - DATAL	Data Address Low							
B - DATAH	Data Address High							
C - DATARL	Data Transfer Relocation Address Low Byte							
D - DATARH	Data Transfer Relocation Address High Byte							
E - NIOPL	Next IOPB Address Low Byte							
F - NIOPH	Next IOPB Address High Byte							
10 - ACNTL	Actual Count Low							
11 - ACNTH	Actual Count High							

DRIVE RESET

Required for execution Returned value

2.5.5.3 Detailed Drive Reset Description

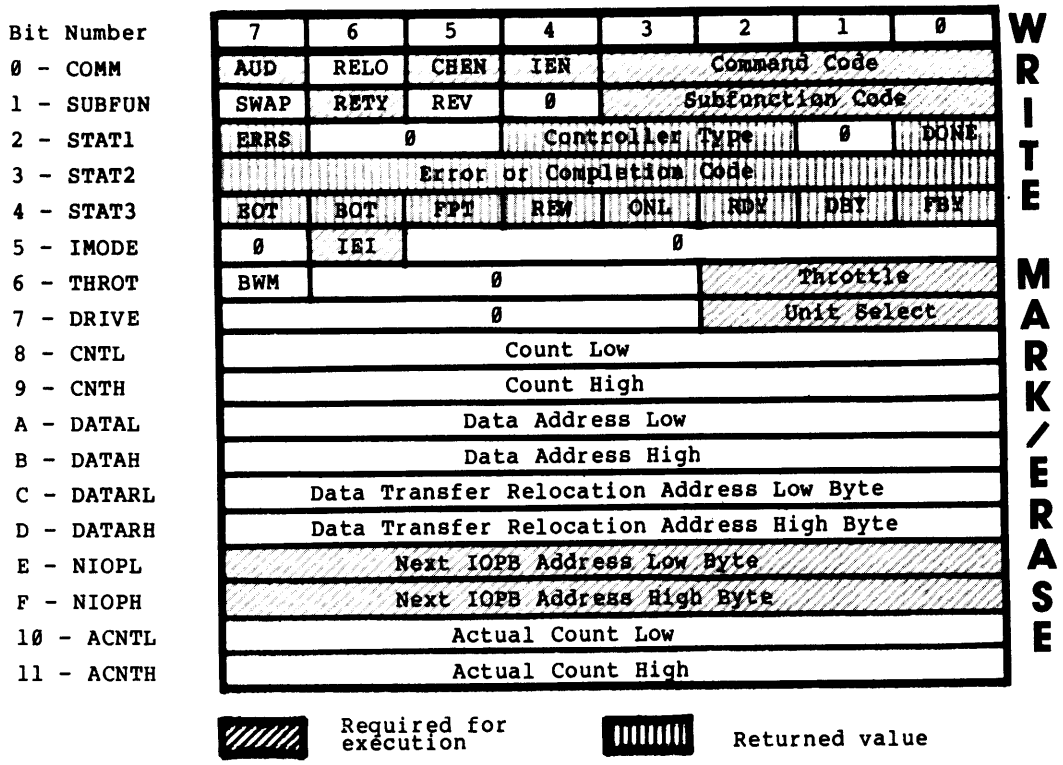
The effect of this command is to abort any operation in progress. It should only be used if a runaway condition is suspected. Tape position after a reset must be considered unknown.

2.5.6 Write Tapemark/Erase (Command Code 7)

2.5.6.1 General

This command erases bad spots on the tape or writes tape marks.

2.5.6.2 IOPB



2.5.6.3 Write Tapemark/Erase Command Error Handling

The command will be aborted if the tape is write protected, drive is offline or an illegal subfunction is specified. If write retries fail to clear a data error, the tape should be erased (approximately 3 inches per command) and the write tried again. Tape marks are used to logically group records and should always be written at the logical end of tape to prevent spacing or skipping off the end of tape. If EOT is detected, the status is posted, but the 472 will not prevent writing past EOT. If a tape mark is not detected on a write mark command, a tape mark failure status will be returned. The 472 will retry the write mark until the mark is detected or the retry count is exceeded if so enabled by the subfunction. A failure to write a tape mark is considered a hard error and will halt IOPB execution.

2.5.6.4 Write Tapemark/Erase Subfunction Codes

This command has three subfuctions, erase, write mark and write mark with retry.

Code ØØ - Write Mark: write a tape mark. Tape marks are used to logically group records on tape. At least one tape mark should be written at the logical end of tape.

Code Ø1 - Erase: this function is used when write with retries fail to write the desired data. Failure to write successfully usually results from media degradation and can be overcome by writing a long gap over the media defect. This function will erase approximately 3 inches of tape per command.

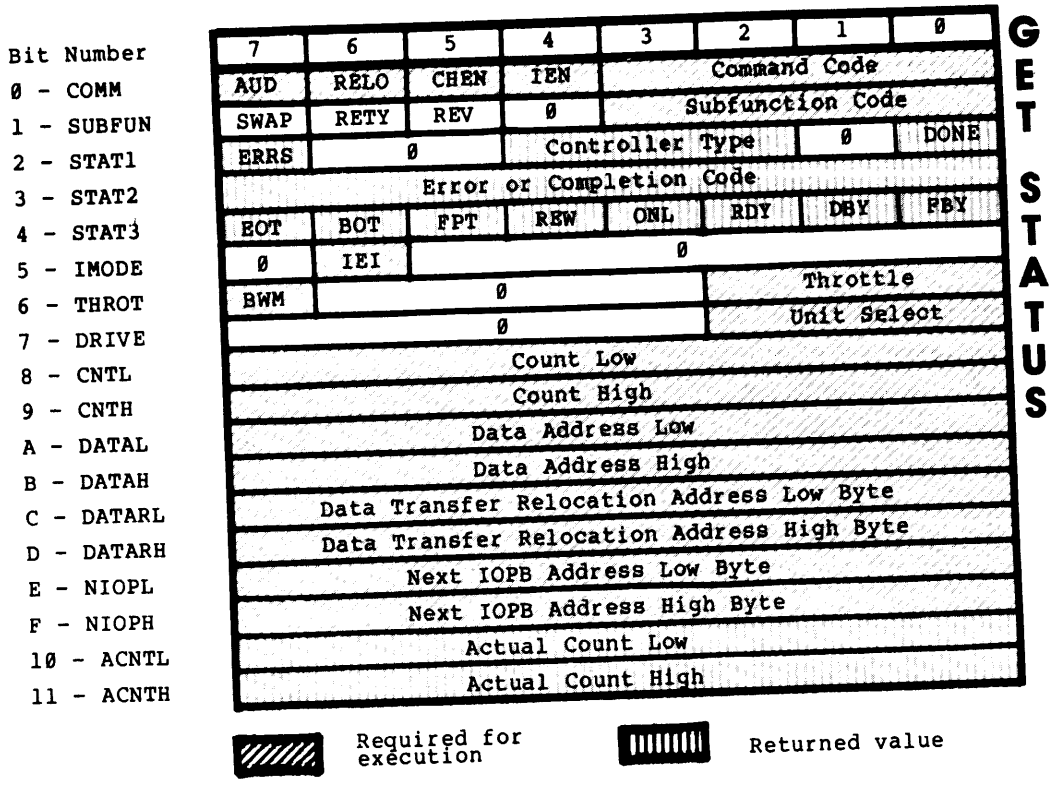
Code 4Ø - Write Mark (with retry): will attempt a write tape mark function up to four times unless sucessful. If the retry count is exhausted, a hard error is reported and IOPB execution is halted.

2.5.7 Get Status (Command Code 9)

2.5.7.1 General

The Get Status command selects a drive and checks for online, BOT, EOT, write protect status and rewind status (Status byte 3). It can also be used to read sense information back from the drive. These bytes are useful in determining the cause of drive malfunctions and are for maintenance purposes. Currently sense bytes are only available with certain manufacturer's drives. Consult your drive manual for further information.

2.5.7.2 IOPB



2.5.7.3 Detailed Get Status Description

The selected drive status is posted in Status byte 3 and in additional bytes pointed to by the buffer address. Status byte 3 contains status flags and can be used by the system software to determine if a drive is ready for a particular command. The status flags are defined in section 2.4.6. This command can also read back from the drive sense information, supported in some PE and GCR streamers. The user must setup the proper byte count (IOPB bytes 8 and 9) (see subfunction code or drive manufacturer manual for number of sense bytes) and buffer address (IOPB bytes A and B).

2.5.7.4 Get Status Subfunction Codes

Code ØØ - Drive Status Flags: this code returns the current drive status in Status byte 3 as described in section 2.4.6.

Code Ø1 - Read Sense Bytes: this code returns to a memory buffer drive status information. The programmer must issue the correct byte count and buffer address. Reference the drive manufacturer's manual for the number of and definitions of bytes.

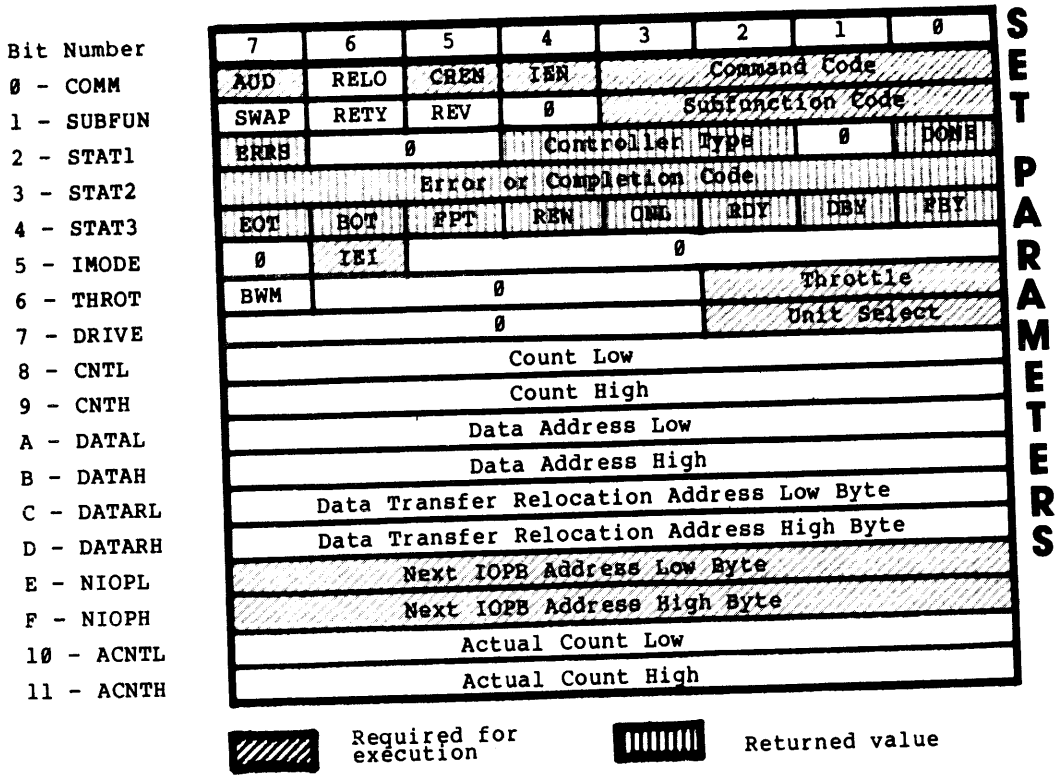
Code Ø2 - Read Extended Sense Bytes: (Currently only supported on CDC 92185 GCR Streamer) return to a memory buffer drive status information usefull in determining drive malfunctions. The programmer must issue the correct byte count and the data address. The CDC 92185 has 27 bytes of extended sense information. Reference the drive manufacturer's manual for definition of bytes.

2.5.8 Set Parameters (Command Code B)

2.5.8.1 General

The Set Parameters command is used to change the density or speed of a selected drive.

2.5.8.2 IOPB



2.5.8.3 Detailed Set Parameters Description

Density changes will be aborted if the tape is not at BOT (illegal command status) to ensure that each tape is written at a single density. The density change commands apply to to both PE 1600/3200 bpi and PE 1600/GCR 6250 bpi tape drives.

The speed change commands are accepted anywhere on the tape. Set high speed puts the streamer drive into streaming mode, in this mode consecutive reads or writes will move the tape continously at high speed as long as the reinstruct time of the drive is met. If the reinstruct time is not met the drive will be forced to reposition. As repositioning is inefficient, set high speed should only be used when the system can guarantee meeting the reinstruct time (preferably using chained IOPBs).

2.5.8.3 Detailed Set Parameters Description (continued)

Set low speed puts the tape drive into start/stop mode; 12.5 or 25 IPS. In stop-start mode no repositioning is done. Over the length of a tape stop-start mode is more efficient than repositioning on every record in streaming mode.

On non-streaming drives, the set speed commands select density. Set low speed mode selects NRZI (800 BPI) and set high speed mode selects PE (1600 BPI). The drive must be configured for remote control of density selection.

2.5.8.4 Set Parameters Subfunction Codes

This command has four subfunctions associated with setting the selected tape drive into a particular mode.

Code 00 - Set Low Density Mode: used with dual density streaming tape drives and sets the drive formatter into PE (1600 BPI) mode.

Code 01 - Set High Density Mode: used with dual density streaming tape drives and sets the drive formatter into 3200 BPI or GCR (6250 BPI) mode.

Code 02 - Set Low Speed Mode: used with streaming tape drives and selects the drive speed, 12.5 or 25 IPS, depending on manufacturer. Selects NRZI (800 BPI) on non-streaming tape drives.

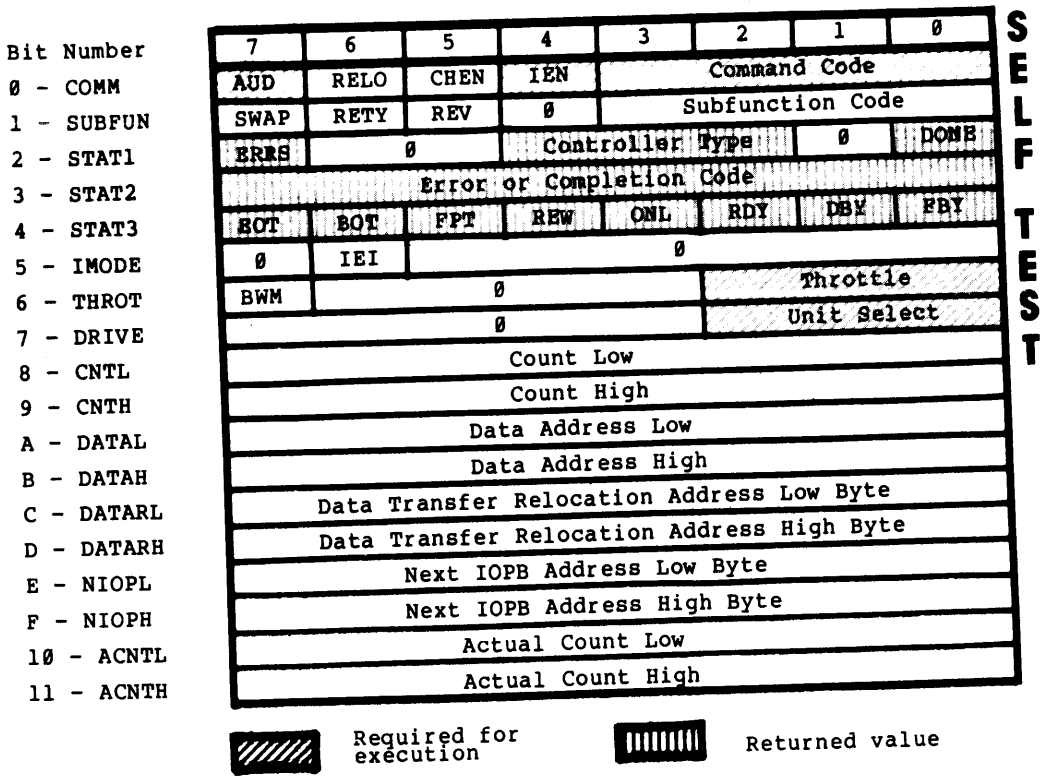
Code 03 - Set High Speed Mode: used with streaming tape drives and sets the drive into constant streaming mode, typically 100 IPS. Selects PE (1600 BPI) on non-streaming tape drives.

2.5.9 Self Test (Command Code C)

2.5.9.1 General

This command will start the same self test that is run automatically on power-up. If successfully completed, a success status will be reported. If not, the appropriate error status will be reported. This command can only be utilized in non-chained mode.

2.5.9.2 IOPB



2.5.9.3 Detailed Self Test Description

This test is the same test performed during the power-up sequence. The self test LED goes on at the start of the test and off when the test completes sucessfully. If a failure is detected, the self test LED will stay on. The Self Test error codes are posted in Status byte 2. The following three tests are performed.

2.5.9.3.1 Processor RAM Test

This test verifies that the RAM internal to the microprocessor and the microprocessor itself are functioning properly. If the RAM fails this test, error code 1A(H) will be returned.

2.5.9.3.2 Address Counter Test

This test verifies that the address counter and the microprocessor are functioning properly. If this test fails an error code of 1B(H) is returned.

2.5.9.3.3 Buffer Test

The on-board FIFO buffer is tested for faulty memory. A 1C(H) will be returned on error.

2.5.10 Commands 3,4,8,A,D,E and F - Reserved

2.6 HOW TO PROGRAM THE 472

This section deals with recommended methods of programming the 472 Peripheral Processor. In the following, it is assumed that interrupts are enabled; thus ignore the sentences about interrupting if they are not enabled in your situation.

2.6.1 IOPB Processing With No Command Chaining

- o Set up IOPB

  Allocate an 18 byte segment of memory to build an IOPB. Set the various parameters in the IOPB as required to perform a function. See Section 2.4.

- o Point 472 to IOPB

  Write the address of the IOPB into the 472 IOPB Address and Relocation Registers.

- o Set Go

  Write an 80(hex) which is GBSY into the CSR register. This effectively starts the operation. The host processor should either poll the CSR for done, or wait for the interrupt. If polling, wait for valid status as described in section 2.3.2.3.1.

- o 472 Processing

  The 472 starts to process the IOPB after it detects that GBSY has been set in its CSR. It uses the Address and Relocation Registers to address Multibus memory and read the IOPB. It executes the function and when complete, updates the status bytes of the IOPB, resets GBSY, and interrupts.

- o Check for Errors

  You should read both the CSR, and Status byte 1 of the IOPB to determine if the command completed successfully. You should test the CSR to determine if the double error bit is set, since this may mean that Status byte 1 was not updated. If the double error bit isn't set, check Status byte 1 and determine if the general error bit (bit 7) is set. If this bit is not set the command completed succesfully.

  The completion code of a command will appear in Status byte 2. A code of 0 indicates successful completion, while any other value indicates an error. Error codes are fully explained in section 2.4.4. Depending upon the error, you may want to try to recover and retry the command. See Section 2.6.3.

2.6.2 IOPB Processing with Command Chaining Enabled

The 472 supports IOPB chaining so that many IOPBs may be queued and processed as fast as possible. The chain starts with the IOPB pointed to by the IOPB Address and Relocation registers and follows the address pointers in each IOPB to the next IOPB. The 472 will complete all IOPBs or stop the chain when a hard error is detected.

2.6.2.1 The Chain

Each IOPB has a field (NIOPL and NIOPH) which points to the next IOPB in the chain. The 472 does not look at the chain pointer to the next IOPB unless CHEN in the current IOPB Command byte is set. The Next IOPB Address bytes are relocated using the IOPB Relocation Registers, therefore all IOPBs in a chain must be located within the 64KB memory block starting at the base address in the IOPB Relocation Register.

2.6.2.2 Executing the Chain

Set the chain enable bit (bit 5, byte Ø) of the IOPB and write the address of the next IOPB into bytes 12 and 13 of the last IOPB in the current chain. The new IOPB is now the last one in the chain. The last IOPB in a chain should have the Next Address field zero and CHEN cleared. Once the 472 has started processing a chain of commands, it is considered busy and you must not add or remove IOPBs from the chain without executing the attention request protocol. This protocol will insure that all IOPBs are in good order. The IOPB in memory, excluding the Status bytes, will not be updated unless the auto-update bit is set or the Update Register is written. By queueing multiple IOPBs system software may take advantage of the command overlap feature of the 472.

2.6.2.3 Completing IOPBs

As each IOPB is completed, the Status bytes in the IOPB are updated to indicate DONE along with the completion code. If Interrupt at each IOPB is enabled, the 472 will interrupt as it completes each IOPB. An interrupt is acknowledged by writing a "1" into the Interrupt Pending Bit in the CSR. The Interrupt Pending and/or Error bits must not be reset with a Controller Reset, as certain operating parameters may be modified and chaining will be stopped.

The 472 will remain busy until either the chain is complete, or a hard error occurs. If the 472 completes processing its current IOPB while there is an active attention request, reseting AREQ will cause the 472 to Go Busy again.

2.6.2.4 Modifying the Chain During Execution

There are two bits in the 472 Controller Status Register used in the 472 Attention Request protocol: Attention Request and Attention Request Acknowledge.

System software should set the Attention Request bit (AREQ) to notify the 472 that it wishes to add or remove IOPBs from the queue. When the 472 has noticed this request it will set Attention Request Acknowledge (AACK) in the Controller Status Register and if the Interrupt at each IOPB bit (IEI) is set, an interrupt will occur. Typically the interrupt handler will write the interrupt pending bit (IPND) to clear the interrupt. The CSR must have the (AREQ) bit set if (ACCK) is read in the CSR upon entering the interrupt handler.

System software may now remove IOPBs which have been marked as complete and may add new IOPBs to the queue. IOPBs which were queued previously but are not marked complete may <u>not</u> be touched except to modify CHEN and Next IOPB address.

When system software has completed adding or removing IOPBs, it should clear (AREQ) and the 472 will clear (AACK). The 472 will continue processing the chain at this time. Whenever reading the CSR the programmer must check for valid status.

2.6.2.5 Chain Interrupts

The 472 supports a mode of interrupting that will provide an interrupt at the end of each IOPB. An interrupt may occur due to one IOPB being complete, several chained IOPBs having completed, or (AACK) having been granted. One interrupt will occur and it is up to the software to determine why the interrupt occured.

2.6.2.6 Completing a Chain

When all IOPBs in a chain have been completed, the chain is complete. If one IOPB had a hard error, the chain completes with an error and later IOPBs may not have been processed, this is indicated by the contents of Status bytes 1 and 2. If interrupts are enabled, an interrupt will occur.

2.6.3 Error Recovery

Certain errors may be recovered by appropriate procedures. The procedures will vary depending upon the type of error encountered. The errors are shown below and are grouped according to the recommended recovery procedure. The error code will appear in Status byte 2.

2.6.3.1 Errors Ø1, Ø3 and 15

Ø1	Interrupt Pending
Ø3	Busy Conflict
15	Unimplemented Command

These errors are either programming errors or hard failures and should not be retried in a normal software driver. For further explanation see Section 2.4 of this manual.

2.6.3.2 Errors Ø4 and Ø6

Ø4	Operation Time Out
Ø6	Uncorrectable Data

These errors may be recovered by retrying the operation. Four retries should be executed and if the error persists the error is unrecoverable.

2.6.3.3 Errors 14 and 16

14	Write Protect Error
16	Drive Offline

The operator must follow suitable action ie., remove tape reel write ring, load tape, etc.

2.6.3.4 Error ØE

ØE	Slave ACK Error

Check the parameters issued, correct them, and try again. You have accessed non-existant memory.

2.6.3.5 Error 1F

1F Corrected Data

This error is for information purposes only and may be logged by the operating system. This is a soft error.

2.6.3.6 Error 1D

1D Tape Mark Failure

Retry operation or if enabled the subfunction will retry four times. If the error does not clear, erase that section of tape and retry function.

2.6.3.7 Error 1E

1E Tape Mark Detected on Read

You have reached a tape mark. Action to be taken is operating system dependant.

2.6.3.8 Errors 22 and 23

22 Record Length Short
23 Record Length Long

This is not necessarily an error, the actual number of bytes read are posted in IOPB bytes 10 and 11. If necessary retry the read operation after correcting the byte count. In either case, the 472 stops in the interrecord gap.

2.7 PERFORMANCE CONSIDERATIONS

This section deals with how to get the most from the 472. It discusses the various tradeoffs and their advantages and disadvantages. Using the following information, you should be able to get the best performance possible for YOUR application.

2.7.1 Streaming Considerations

The 472 has several features which make streaming easy to achieve; high speed DMA sequencer, DMA throttle and a 2K byte buffer or optional 8K byte buffer. However, streaming could become difficult due to a slow disk controller or inadequate software. The disk controller should have a DMA transfer rate sufficiently higher than the disk transfer rate to allow time for the 472 to DMA from memory to the tape. If this is true and no other devices need the bus during the backup, then streaming can be achieved as long as the combined transfer rates of the disk and tape add up to less than the DMA capacity of the system. An SMD disk transfers at 1.2 MB/sec and the GCR streamer transfers at Ø.5 MB/sec. The combined rate of 1.7 MB/sec is below the throughput capability of the Multibus with 3ØØns memory (eg. 3.Ø MB/sec). For slower disk controllers or slower memory this must be recomputed. Where the transfer rate capabilities of the two controllers are different, each rate must be multiplied by the percentage of bus time needed by each controller in order to come up with a composite transfer rate.

The transfer rate considerations define a theoretical ability to stream the tape. To actually stream the tape, software must meet the reinstruct time of the tape drive, typically 3.5ms. To send the next tape command within this 3.5ms window should be easy provided there is valid data to be written. Typically a data buffer is set up in memory to hold disk data waiting to be written to tape. In this way, the stream of data is uninterrupted, even if the disk must access a new track or skip a bad sector. Programming options which may help are sequential sector reads, sector interleaving, adjusting the size of the tape record and adjusting the size and number of the data buffers. Parity and ECC errors will cause the tape to reposition. It is not possible to do much file processing during streaming backup. Data compare between disk and tape is best done in start-stop mode.

2.7.1.1 Data Buffering

The key to efficient system integration of streaming tapes drives is in matching the dissimilar and variable transfer rates of tape and disk. One way to solve this problem is by using appropriate multiple buffer schemes. The size of the buffer should be determined by the maximum disk latency that must be supported in a streaming mode operation. One buffering scheme is to have several buffers arranged as a circular queue. Memory buffers along with on board FIFO buffers provide a steady data flow to the streaming tape, avoiding frequent stopping for new data.

2.7.2 Throttle Considerations

From the 472 tape controller's viewpoint, the throttle value should be as high as possible so that the controller will never get data lates or have to reposition tape. However, you may have some other real time application that must get to the bus periodically. See section 2.4.6 for bus utilization formula.

In these applications:

- o determine the maximum time that the 472 can be bus master (less time then another unit can be without the bus);
- o determine the response time of your memory, add 400 nsec. and divide into the allowable 472 bus master time. The number you come up with is the maximum throttle value. For smaller throttles this number must be reduced to allow for getting on and off the bus;
- o pick the closest number from the 472 throttle values without going over the actual amount.

2.7.2.1 High Throttle Advantage

- o Maximum bus throughput with minimum bus overhead.

2.7.2.2 High Throttle Disadvantages

- o Tendency to "hog" the bus - time critical devices fail.
- o Other DMA units may not get enough bus time.

2.7.3 Word or Byte Mode

Word mode is definitely more efficient on the bus. It takes the same length of time to transfer a word in word mode as it does a byte in byte mode. Using word mode therefore effectively doubles the throughput of the 472.

2.7.3.1 Word Mode Advantages

- o Increased throughput with less bus utilization.
- o Helps DMA keep up with tape.

2.7.3.2 Word Mode Diasadvantages

- o Works only on word oriented memory.

2.7.4 Transfers on Address Boundaries

The 472 will react differently to transfers on various address boundaries. Word mode transfers on odd addresses obviously must compensate for the odd address. The internal architecture of the 472 dictates how transfers across page boundaries are handled.

2.7.4.1 Word Mode on Odd Boundary

If a word mode transfer begins on an odd address, the 472 compensates by mixing word and byte mode. It will do the first transfer in byte mode, the remaining transfers in word mode, and complete the transfer with the final byte in byte mode. The disadvantage is that the on-board microprocessor must get involved with the transfers more often when starting a word mode transfer on an odd byte. This added involvement requires more time during a transfer and reduces the margin for keeping up with the tape. The extra time involved by the microprocessor does not result in any extra bus time.

2.7.4.2 Transfers to Page Addresses

Each time the 472 crosses a 256 byte address boundary, the onboard microprocessor must update the upper address bits and restart the DMA sequencer. It is more efficient to align transfers on page boundaries so that this occurs the minimum number of times.

2.7.5 Chaining Operations

Chaining will have an effect on the performance of your system. Chaining IOPBs results in several performance advantages:

- The 472 will automatically perform overlap operations, which will have a impact for multidrive systems during multiple volume backup or restore operations.

- The operating system does not have to respond as rapidly at the end of a command; the 472 will continue to execute the next command without operating system intervention. The 472 will allow interrupts at the end of each IOPB and notify the system that the IOPB is complete.

2.9 SAMPLE PROGRAM

2.9.1 Sample Listing for 8080 Processors

The following program will give the address of the IOPB at 120H to the controller, set GBSY, wait for done, and halt.

```
100   AF              XRA   A       ;Clear Accumulator
101   D3 60           OUT   IRELL   ;Clear Relocation Register
103   D3 61           OUT   IRELH
105   3E 20           MVI   A,20H   ;Low byte of IOPB address
107   D3 62           OUT   IADRL   ;send to IOPB address register
109   3E 01           MVI   A,01H   ;High byte of IOPB address
10B   D3 63           OUT   IADRH
10D   3E 80           MVI   A,GBSY  ;Set GBSY
10F   D3 64           OUT   CSR     ;Tell controller to GO
111   DB 64     LOOP: IN    CSR     ;Get status
113   E6 80           ANI   GBSY    ;Test for done
115   C2 11 01        JNZ   LOOP    ;No - Wait
118   76              HLT           ;Yes - Stop
```

3.0 INSTALLATION AND CHECKOUT

The following section describes the procedures used to unpack, configure, install, and checkout your 472.

3.1 UNPACKING AND INSPECTION

3.1.1 Inspect Shipping Carton

Inspect the shipping carton for possible shipping damage. Carefully unpack the 472 from its carton and save the carton and other shipping material for possible later use. If you determine that there has been shipping damage, do not unpack the unit. Notify Xylogics and the freight carrier immediately.

3.1.2 Contents

472 is a single printed circuit board. Optional items which may be included are drive cables, a manual and/or software on a magtape or floppy disk.

If any items are missing please contact Xylogics at one of the following telephone numbers:

United States 617-272-8140
United Kingdom 44-753-78921
West Germany 49-6196-47004

3.1.3 Inspect the 472

Inspect the 472 for socketed parts that may have become loosened during shipment. Assure that all parts are firmly seated in their sockets. If any parts must be reinserted, observe proper orientation.

3.2 CONFIGURING THE 472

The 472 has several jumper options which can be configured by the customer. These options are described in the following paragraphs. Refer to Figure 3-1 for a board layout.

3.2.1 Base Address Selection

There are two separate parts to selecting the base address. The first is selecting response to 8 or 16 bit register addresses. This is controlled by the jumper JL. The jumper is factory configured for 16 bit.

Mode	Jumper JL
8 bit	Installed
16 bit	Removed

The actual base address is controlled by jumpers JA/JB 1-8 and JC/JD 1-5. Jumpers JC/JD 6, 7 and 8 must be installed and should not be changed. If 8 bit addressing is selected, the jumpers for address bits 0-7 are the only valid jumpers, and jumpers for bits 8-F are ignored. Table 3-1 shows how to set the staples for commonly used base addresses. Factory configuration is EE60.

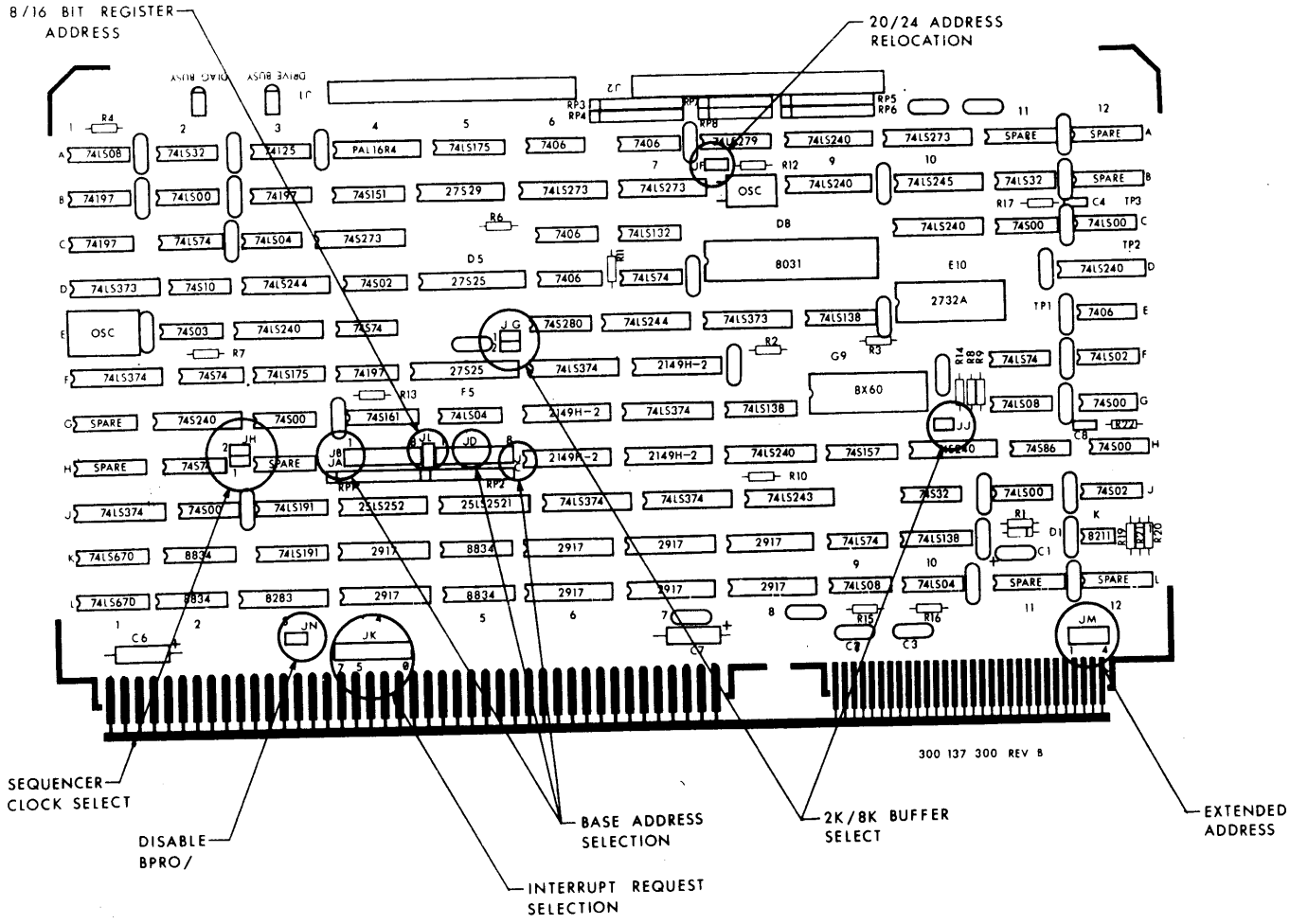


FIGURE 3-1. 472 COMPONENT SIDE

3.2.1 Base Address Selection (continued)

Address Bit:	F	E	D	C	B	A	9	8	7	6	5	4	3	8/16
Pin Numbers														
Jumper JA/JB	1	2	3	4	5	6	7	8						
Jumper JC/JD									1	2	3	4	5	
Jumper JL														X
Address														
60 - 8 bit	X	X	X	X	X	X	X	X	I	Ø	Ø	I	I	I
EE60 - 16 bit	O	O	O	I	O	O	O	I	I	Ø	Ø	I	I	O
50 - 8 bit	X	X	X	X	X	X	X	X	I	Ø	I	Ø	I	I
0050 - 16 bit	I	I	I	I	I	I	I	I	I	Ø	I	Ø	I	O

TABLE 3-1. BASE ADDRESS

Where O = remove, I = installed, and X = don't care.

3.2.2 20/24 Bit Address Relocation

The 472 can function in backplanes of 16, 20, and 24 bit addresses. The 20 bit or 24 bit mode must be selected via jumpers. The 16 bit mode is software selectable. The status of the jumper can be determined by reading bit 3 (ADMD) of the CSR, if set this indicates that the board is jumpered for 24 bit address mode. Both 20 and 24 bit modes support 16 bit addressing. Factory configuration is 16/20 bit.

Mode	Jumper JF	ADMD Value
16/20	Removed	Ø
16/24	Installed	1

TABLE 3-2. 20/24 BIT ADDRESS

3.2.3 24 Bit Extended Address

For systems not utilizing the 472's 24 bit address capability, jumpers have been provided to disconnect the those signals from the P2 connector of the 472. Normally these jumpers are installed.

Address Bit	Jumper JM Position
ADR17/	1
ADR16/	2
ADR15/	3
ADR14/	4

TABLE 3-3. 24 BIT EXTENDED ADDRESS

3.2.4 Interrupt Request Levels

Any one of 8 interrupt request levels can be chosen. The 472 is supplied from the factory jumpered for INT5/. The selection is performed by connecting a jumper per table 3-4.

3.2.4 Interrupt Request Levels (continued)

Interrupt Request Level	Jumper JK Position
INT0/	0
INT1/	1
INT2/	2
INT3/	3
INT4/	4
INT5/	5
INT6/	6
INT7/	7

TABLE 3-4. INTERRUPT LEVEL

3.2.5 Disable BPRO/

If the 472 is to be used in parallel DMA arbitration (see Section 3.3.2.2) the BPRO/ signal must be isolated from the Multibus. This can be accomplished by removing the jumper from JN. Factory configuration has JN installed.

3.2.6 DMA Sequencer Clock

The source for the DMA sequencer clock can come from either an on-board 10 MHz crystal or BCLK/. In general the 472 will always function properly if the clock is connected to 10 MHz. If BCLK/ is running at 10 MHz, the sequencer will be syncronized to the clock, and therefore maximize the throughput of the 472. If BCLK/ is slower or faster than 10MHz then the sequencer should be connected to 10 MHz. Factory configuration is JH in position 2.

Clock	Jumper JH Position
10 MHz	2
BCLK/	1

TABLE 3-5. DMA CLOCK

3.2.7 Factory Use Jumpers

There are several jumpers on the 472 which should not be changed since they are for factory use only. The jumper settings are determined by the size of the on board FIFO buffer.

Buffer Size	Jumper JG Position	Jumper JJ
2KB (Standard)	1 - Installed 2 - Removed	Removed
8KB (Optional)	1 - Removed 2 - Installed	Installed

TABLE 3-6. BUFFER OPTION

3.3 PREPARING THE COMPUTER SYSTEM

Several steps must be followed in preparing your computer system to accept the 472 controller. A Multibus slot must be provided in the backplane for the 472, the slot must be capable of handling a bus master, and the power source must handle the power consumption of the entire system including the 472.

3.3.1 Card Cage Slot

The card cage must have a slot available for the 472. Placement of the 472 in the DMA priority chain may be critical and thus may affect which slot is chosen.

3.3.2 DMA Bus Arbitration

The 472 can use either serial or parallel DMA arbitration. Serial arbitration is much easier to implement but has restrictions on the number of bus masters it can arbitrate. Parallel bus arbitration is more difficult to implement but is more versitile and can handle more bus masters. The choice of priority scheme is purely system dependant and has no impact on 472 performance.

3.3.2.1 Serial DMA Priority

Serial priority is implemented by connecting the BPRØ/ and BPRN/ lines in a serial fashion as shown in figure 3-2. The highest priority is the first slot and must have its BPRN/ line grounded. The next highest priority is the next slot. To become bus master a unit must have its BPRN/ line asserted. If a unit is not currently a bus master, it passes the state of the BPRN/ to the BPRO/. If the unit is bus master, it de-asserts its BPRO/ so that the following units will not have BPRN/ asserted and therefore cannot become bus master.

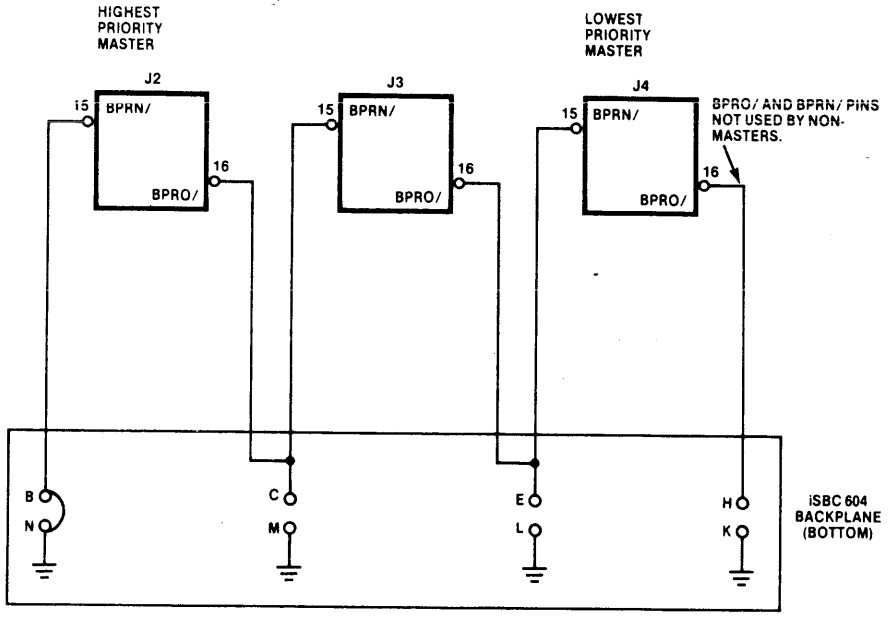
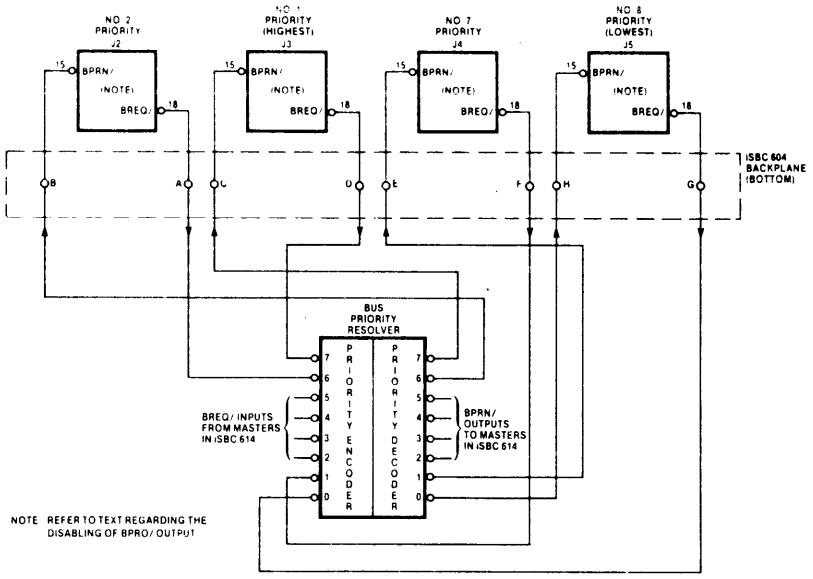


FIGURE 3-2. SERIAL PRIORITY

3.3.2.2 Parallel DMA Priority

Parallel priority uses the same connections to each board, and connects them to a circuit similar to that of figure 3-3. This external circuit does the bus arbitration. The BPRO/ lines must be disconnected between each board and the BREQ/ lines are connected to the external priority resolver circuit.



3.3.3 Power Considerations

The 472 will affect the power consumption of the entire computer system. Be sure that the power supplies are adequate to handle the entire power load and re-adjust the voltages AFTER the 472 has been plugged in. A power supply that is just adequate may cause intermittant and unusual problems due to noise generated by occasionally going into overcurrent protection. The 472 draws 5.0 amps at 5.0 VDC.

Min/Max Limits: 4.75 to 5.25 VDC.

3.4 TAPE DRIVE PREPARATION

The tape drive must be unpacked and prepared for use with the 472. Inspect the shipping container of the tape drive for any shipping damage and if any, notify the carrier immediately. Unpack the drive and remove any shipping constraints.

Configure the drive for use by the 472. This will entail setting up several parameters such as formatter address, unit select, remote density select, etc. Consult the drive manual for the exact method of configuring your drive.

3.5 INSTALL AND CABLE THE 472

In sections 3.1 through 3.4, directions for configuring the controller and drive in preparation for the installation are given. In this section directions for installing and cabling the controller are given.

3.5.1 Install the 472

Place the 472 into the computer cardcage being sure that it is facing in the proper direction and that it is firmly seated. Be careful not to dislodge any socketed ICs.

Mount or place the tape drive in the area it is to occupy. Connect the drive to the appropriate power source.

3.5.2 Cable up the Subsystem

3.5.2.1 Connect Cables

Optional cables can be purchased with each 472, the set consists of two identical 50 pin flat ribbon cables which conform to the Pertec Format Interface standard, typical length for these cables is 15 ft. (reference section 5.2 for tape drive interface pinout). Check the tape drive manufacturer manual for any interface adapters which may be necessary. Observe the pin '1' markings on the cable connector for proper orientation on both the drive and 472.

3.5.2.2 Mechanical Restraint

At this time be sure that both cables are mechanically restrained at each end to prevent the cables from accidentally disconnecting.

3.5.2.3 Tape Drive Grounds

Install a ground braid wire between the ground terminal on the tape drive(s) and the computer system ground. This will complete the cabling.

3.6 INITIAL TESTS

This section relys upon the operators familiarity with the monitor of the computer system.

3.6.1 Power up and Self Test

The initial test is the self test indicated by the LED upon power up. This LED should go on for a brief period and then go off. If it remains on, the board is not functioning properly and Xylogics should be contacted for further help.

NOTE

Check the power supply voltages to insure that they are within limits. (4.75 to 5.25 volts)

3.6.2 Register Verification

It is also suggested that a check of the 472 registers be made. On power up the registers are cleared (all zeros), verify this by reading them. If you were unable to access the registers re-check the 472 base address jumpers and/or your particular system I/O register requirements. Next try writing some value to the registers and read them back to verify the data was correct.

3.6.3 Tape Drive Diagnostics

Many tape drive manufacturers offer power-on and offline diagnostic capabilities. Consult your particular tape drive manual for futher information.

3.6.4 Drive Online

Load a tape reel, hit the load switch and wait for the on line indicator to be illuminated. Read the 472 Reset Register, this will reset the controller, select drive Ø and test the drive online status. Next, read the CSR which will contain the results of the drive online check. The CSR should contain Ø1(H).

If bit Ø is not set, re-check the drive cable connections and try again. If you are still unable to get the proper status, check the tape drive for functionality with offline diagnostics or tester.

3.7 CABLING MULTIPLE DRIVES

If multiple drives are to be used, the cables must be properly connected. Daisy chaining tape drives requires cables with a daisy chain connector which will accept the 5Ø pin end of the cable normally plugged into the 472. Simply attach the additional drive cables into the previous drive cables, then plug in the drive end. Be sure not to reverse the cables. Up to eight tape drives can be daisy chained in this manner. (Reference figure 3-4 and 3-5)

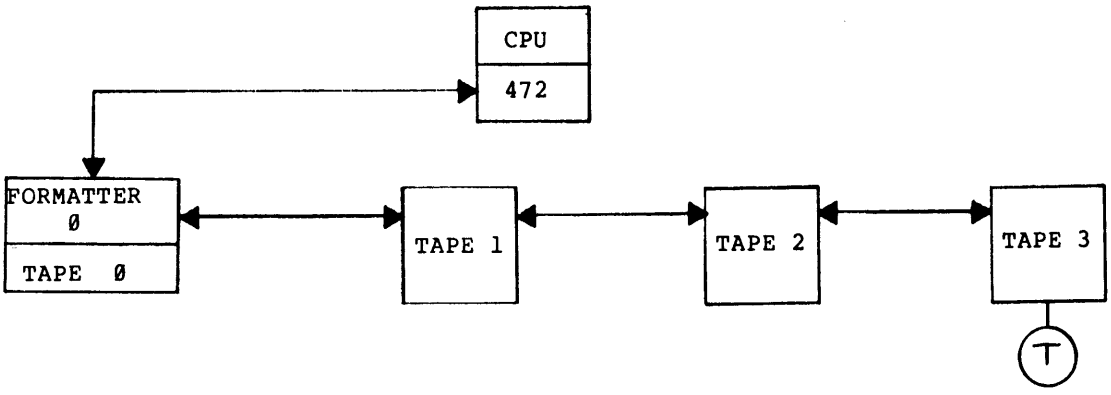


FIGURE 3-4. TAPE DRIVE DAISY CHAINING - SINGLE FORMATTER

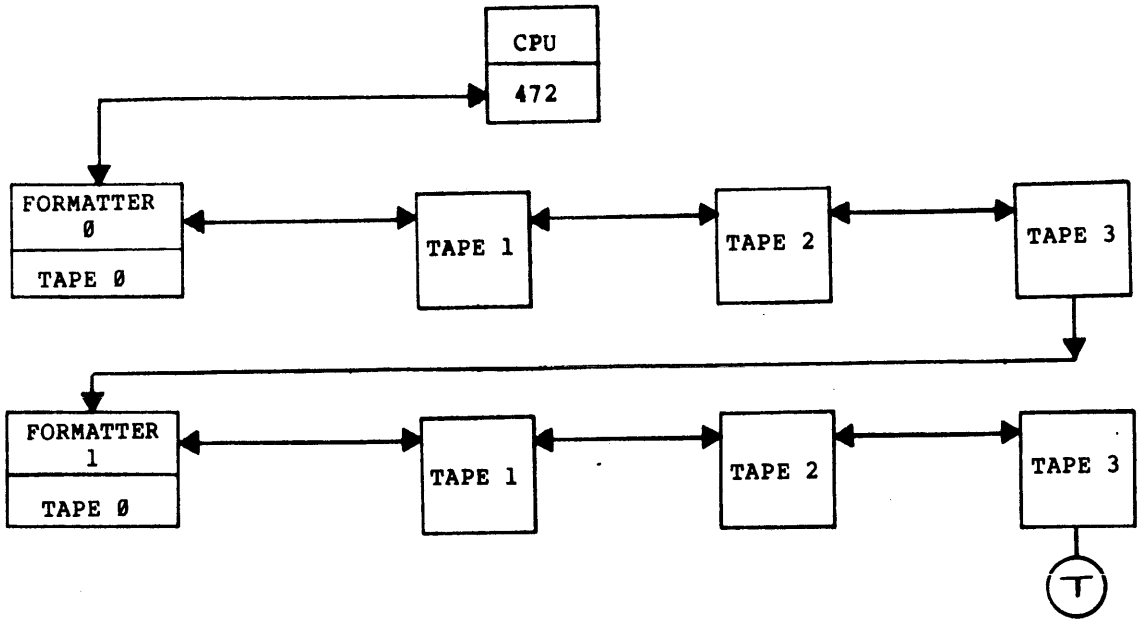


FIGURE 3-5. TAPE DRIVE DAISY CHAINING - TWO FORMATTERS

3.7.3 Formatter/Unit Select

One formatter board is required for each four tape drives connected. An additional formatter board is required for systems using more than four drives. Each formatter has an address which can be selected via switches. The tape drives must also be set for unique unit numbers which are also selected via switches in the drive. Consult the drive manufacturers manual for the location and proper setting of the switches.

3.8 DIAGNOSTICS

Now you should run the diagnostics. Section 4 describes how to use the diagnostics.

3.9 IMPLEMENT OPERATING SYSTEM

The subsystem has been completely tested at this point. Consult your operating system manuals on how to incorporate it into your system.

5.0 MAINTAINENCE AIDS

The following information is provided for use in installing and maintaining your 472.

5.1 MULTIBUS INTERFACE SIGNALS

Mnemonic	Conn.	Pin	Used by 472	Description
ADR0/	P1	57	Y	
ADR1/	P1	58	Y	
ADR2/	P1	55	Y	
ADR3/	P1	56	Y	
ADR4/	P1	53	Y	
ADR5/	P1	54	Y	
ADR6/	P1	51	Y	
ADR7/	P1	52	Y	
ADR8/	P1	49	Y	
ADR9/	P1	50	Y	
ADRA/	P1	47	Y	
ADRB/	P1	48	Y	
ADRC/	P1	45	Y	
ADRD/	P1	46	Y	Address Bus
ADRE/	P1	43	Y	
ADRF/	P1	44	Y	
ADR10/	P1	28	Y	
ADR11/	P1	30	Y	
ADR12/	P1	32	Y	
ADR13/	P1	34	Y	
ADR14/	P2	57	Y	
ADR15/	P2	58	Y	
ADR16/	P2	55	Y	
ADR17/	P2	56	Y	
DAT0/	P1	73	Y	
DAT1/	P1	74	Y	
DAT2/	P1	71	Y	
DAT3/	P1	72	Y	
DAT4/	P1	69	Y	
DAT5/	P1	70	Y	
DAT6/	P1	67	Y	
DAT7/	P1	68	Y	
DAT8/	P1	65	Y	Data Bus
DAT9/	P1	66	Y	
DATA/	P1	63	Y	
DATB/	P1	64	Y	
DATC/	P1	61	Y	
DATD/	P1	62	Y	
DATE/	P1	59	Y	
DATF/	P1	60	Y	

5.1 MULTIBUS INTERFACE SIGNALS (continued)

Mnemonic	Conn.	Pin	Used by 472	Description
STROBE				
IORC/	P1	21	Y	I/O Read Cmd
IOWC/	P1	22	Y	I/O Write Cmd
MRDC/	P1	19	Y	Mem Read Cmd
MWTC/	P1	20	Y	Mem Write Cmd
XACK/	P1	23	Y	XFER Acknowledge
CLOCKS				
BCLK/	P1	13	Y	Bus Clock
CCLK/	P1	31		Constant Clock
PLC/	P2	31	N	Power Line Clock
INTERRUPTS				
INT0/	P1	41	P	
INT1/	P1	42	P	
INT2/	P1	39	P	
INT3/	P1	40	P	
INT4/	P1	37	P	Interrupt Request Levels
INT5/	P1	38	P	
INT6/	P1	35	P	
INT7/	P1	36	P	
INTA/	P1	33	Y	Interrupt Acknowledge
DMA				
BPRN/	P1	15	Y	Bus Priority In
BPRO/	P1	16	Y	Bus Priority Out
BREQ/	P1	18	P	Bus Request
BUSY/	P1	17	Y	Busy Ready
CBRQ/	P1	29	P	Common Bus Request
MISCELLEANEOUS CONTROL				
BHEN/	P1	27	Y	Byte High Enable
BD RESET/	P2	36	N	Board Reset
HALT/	P2	28	N	Bus Master Wait State
INH1/	P1	24	N	Inhib. 1 disable RAM
INIT/	P1	14	Y	Initialize
MISCELLEANEOUS				
ACLO/	P2	18	N	AC Low
ALE/	P2	32	N	Bus Master ALE
AUX RESET/	P2	38	N	Reset Switch Reserved
LOCK/	P1	25	N	Inhib. 2 dis. PROM or ROM
MPRO/	P2	20	N	Memory Protect
PAR1/	P2	27	N	Parity 1
PAR2/	P2	29	N	Parity 2
WAIT/	P2	30	N	Bus Master Wait State

5.1 MULTIBUS INTERFACE SIGNALS (continued)

Mnemonic	Conn.	Pin	Used by 472	Description
POWER				
12VB	P2	11,12	N	+12V Battery
5VB	P2	3	N	+5V Battery
GVB	P2	4	N	Return
-5VB	P2	7,8	N	-5V Battery
-12VB	P2	15,16	N	-12V Battery
+5V	P1	3,4,5,6,81,82,83,84	Y	+5DC
+12V	P1	7,8	N	+12VDC
+15V	P2	23,24	N	+15V
-5V	P1	9,10	N	-5 volt supply
-12V	P1	79,80	N	-12Vdc
-15V	P2	25,26	N	-15V
EEVPP	P2	6	N	E^2 PROM Power
GND	P1	1,2,11,12,75,76,85,86	Y	Signal GND
GND	P2	1,2,21,22	N	Signal GND

5.2 PERTEC FORMATTED INTERFACE

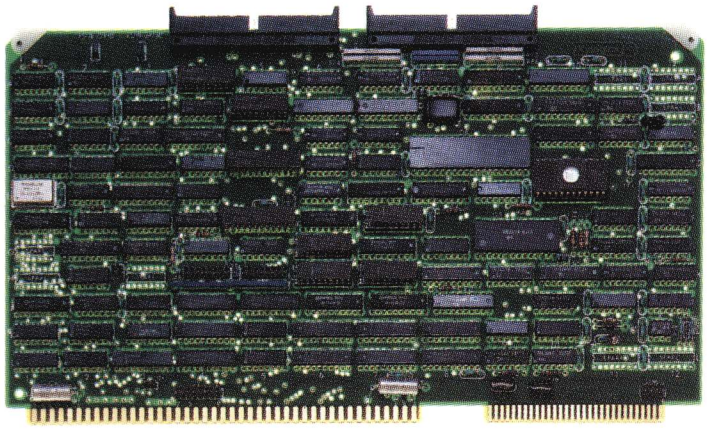
Signal mnemonics may be different from one manufacturer to the next but the function of those signals should remain the same. Several of the signals listed are only used with GCR Streamer's and are indicated as such. Consult the manufacturer's interface specification for futher explanations.

Name	Cable	Signal Pin	Ground Pin	Description	Used by 472
FBY	P1	2	1	Formatter Busy	Y
LWD	P1	4	3	Last Word	Y
WD4	P1	6	5	Write Data 4	Y
GO	P1	8	7	Initiate Command	Y
WD0	P1	10	9	Write Data 0 (MSB)	Y
WD1	P1	12	11	Write Data 1	Y
Spare	P1	14	13	Reserved	N
LOL	P1	16	15	Load On Line	Y
REV	P1	18	17	Reverse/Forward	Y
REW	P1	20	19	Rewind	Y
WDP	P1	22	21	Write Data Parity	Y
WD7	P1	24	23	Write Data 7	Y
WD3	P1	26	25	Write Data 3	Y
WD6	P1	28	27	Write Data 6	Y
WD2	P1	30	29	Write Data 2	Y
WD5	P1	32	31	Write Data 5	Y
WRT	P1	34	33	Write/Read	Y
LGAP	P1	36	35	Long Gap	N
EDIT	P1	38	37	Edit	Y
ERASE	P1	40	39	Erase	Y
WFM	P1	42	41	Write File Mark	Y
THR	P1	44	43	High Clip	N
TAD0	P1	46	45	Transport Address	Y
RD2	P1	48	47	Read Data 2	Y
RD3	P1	50	49	Read Data 3	Y

5.2 PERTEC FORMATTED TAPE DRIVE INTERFACE (continued)

Name	Cable	Signal Pin	Ground Pin	Description	Used by 472
RDP	P2	1	5	Read Data P	Y
RDØ	P2	2	5	Read Data Ø (MSB)	Y
RD1	P2	3	5	Read Data 1	Y
LDP	P2	4	5	Load Point	Y
RD4	P2	6	5	Read Data 4	Y
RD7	P2	8	7	Read Data 7	Y
RD6	P2	1Ø	9	Read Data 6	Y
HER	P2	12	11	Hard Error	Y
FMK	P2	14	13	File Mark	Y
ID	P2	16	15	PE ID Burst	N
FEN	P2	18	17	Formatter Enable	Y
RD5	P2	2Ø	19	Read Data 5	Y
EOT	P2	22	21	End of Tape	Y
OFL	P2	24	23	Offline/Unload	Y
GCR	P2	26	25	Density Status	N
RDY	P2	28	27	Ready	Y
RWD	P2	3Ø	29	Rewinding	Y
FPT	P2	32	31	File Protect	Y
RSTR	P2	34	33	Read Strobe	Y
WSTR	P2	36	35	Write Strobe	Y
DBY	P2	38	37	Data Busy	Y
HSPD	P2	4Ø	39	Speed	N
CER	P2	42	41	Corrected Error	Y
ONL	P2	44	43	On Line	Y
TAD1	P2	46	45	Transport Address 1	Y
FAD	P2	48	47	Formatter Address	Y
HISP	P2	5Ø	49	High Speed Select	Y

XYLOGICS 472 TAPE CONTROLLER.



The Xylogics 472 is a high performance tape controller for streaming and start/stop tape drives that sets the standard for price, performance and size for the IEEE-796 Multibus! Residing on one single-height Multibus printed circuit board, the 472 can address up to 16 MB of memory and control up to eight tape drives. These drives may run at speeds from 12.5 ips to 125 ips at densities of 800 bpi NRZI, 1600/3200 bpi PE, or 6250 bpi GCR. The 472 can interface to any drive which conforms to the Pertec formatted interface.

The 472 uses the advanced technique of channel control for an optimal match to the multi-processing environment of the IEEE-796 bus and 16/32 bit microprocessors such as the 8086, 68000, 16032 and Z8000. Commands are issued from an operating system by creating an I/O parameter block (IOPB) in memory and pointing the 472 at the IOPB. Multiple IOPBs may be linked together for optimal throughput. By using multiple IOPBs, the functions of scatter-read and gather-write may be implemented.

FEATURES	BENEFITS
• Fast DMA (up to 3.0 MB/sec.)	• Low Bus Utilization Overhead
• Supports Streaming	• Software Selectable Streaming Mode
• Single Board Design	• Requires Less Backplane Space
• IEEE-796 Bus Compatible	• Industry Standard Bus
• 16, 20, or 24 Bit Addressing	• Compatible with all Multibusses
• 8 or 16 Bit Data Transfers	• Supports 8 and 16 Bit Processors
• 2 or 8 KB FIFO Buffer	• Eliminates Date Lates
• Tape Speeds of 12.5 to 125 ips	• Selection of Many Tape Drives

FEATURES	BENEFITS
• Densities of 800, 1600, 3200 and 6250 bpi	• Selection of Many Tape Drives
• Pertec Formatted Interface	• Industry Standard
• Up to 8 Drives per Board	• Growth Capability Built-In
• Mixed Drive Speeds & Densities	• Drive Mix User Defined
• Programmable Throttle	• Support any Multibus Speed
• Selectable Device Addresses	• Match System Requirements
• On-Board Diagnostic with Status LED	• Power Up Self Test
• Burned-in Components/Power Cycled	• Built-In Reliability

Xylogics®

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MULTIBOOST

PRODUCT SPECIFICATIONS

Command Technique: The 472 uses the technique of channel control which allows the operating system to create a tape drive command in an I/O parameter block (IOPB) in memory. The command is initiated by loading the address of the IOPB into the IOPB address registers and setting the Go-bit in the command and status register. The 472 will execute the command and when complete, set a completion status and clear the Go-bit in the command status register. If interrupts are enabled, an interrupt will be generated when the Go-bit is cleared. If an error is detected, an error code is returned in the IOPB for examination by the operating system. A channel program may be created by linking IOPBs together in a chain to execute many functions sequentially with little or no host processor intervention.

I/O Parameter Block Format

Byte Offset	Description	Byte Offset	Description
0	Command	A	Data Address Low
1	Subfunction	B	Data Address High
2	Status Byte 1	C	Data Relocation Low
3	Status Byte 2	D	Data Relocation High
4	Status Byte 3	E	Next IOPB Address Low
5	Interrupt Mode		
6	Throttle	F	Next IOPB Address High
7	Unit Select		
8	Count Low	10	Actual Count Low
9	Count High	11	Actual Count High

Commands: The 472 supports the following commands and subfunction roles:

Command	Subfunction
NOP	–
WRITE	Write
	Write Retry
	Write Swap Bytes
	Write Retry Swap Bytes
READ	Read Next
	Read Previous
	Read Next Retry
	Read Previous Retry
	Read Next Swap Byte
	Read Previous Swap Byte
	Read Next Retry Swap Byte
	Read Previous Retry Swap Byte
POSITION	Space Records Forward
	Space Records Reverse
	Skip Tape Marks Forward
	Skip Tape Marks Reverse
	Rewind
	Unload
DRIVE RESET	–
WRITE FILEMARK	Write Filemark
	Write Filemark Retry
	Erase
READ DRIVE STATUS	Drive Status
	Read Sense Bytes
	Read Extended Sense Bytes
SET PARAMETERS	Set Low Density
	Set High Density
	Set Low Speed
	Set High Speed
SELF TEST	–

Programmer Visible Registers: The 472 has six 8-bit programmer visible registers addressable as IEEE-796 byte I/O ports.

Byte 0 IOPB Relocation Low
Byte 1 IOPB Relocation High
Byte 2 IOPB Address Low
Byte 3 IOPB Address High
Byte 4 Controller Command and Status
Byte 5 Controller Reset/Update IOPB

SPECIFICATION SUMMARY

Data Verification: 800 bpi – horizontal and vertical parity; 1600/3200 bpi – phase encoding; 6250 bpi – group encoding.

Tape Diagnostics: Comprehensive diagnostic is available for most 16/32 bit microprocessors written in C.

Customer Acceptance Tool: Xylogics Customer Acceptance Tool (XYCAT) is a Multibus-based single board processor with Xylogics 400 series diagnostics in ROM. It is used by Xylogics as a final acceptance test before shipping and is available to customers for use in incoming tests. XYCAT contains the identical diagnostics that are available in C source code.

Software Support: Support for RMX[2]-86, XENIX[3] and Berkeley UNIX[4] 4.2 is available.

Data Transfer: From one to 65535 bytes may be transferred with one request.

Transfer Mode: Throttle controlled, direct memory access (DMA). Throttle value specified in IOPB.

Transfer Rate: The 472 can transfer data at up to 3.0 MB/sec. to the system bus (assuming XACK from memory in 300 ns); however, actual data rate is dependent on memory response time. With appropriate memory, the 472 can run a streaming 6250 bpi GCR tape at 75 ips or a start/stop drive at 125 ips.

Drive Compatibility: The 472 is compatible with any tape drive which conforms to the Pertec formatted interface, including start/stop or streaming drives produced by the following manufacturers: Control Data, Cipher, Innovative Data, Kennedy, Pertec, and others.

Registers: Six.

I/O Parameter Block Length: 18 bytes.

Command Chaining: Inherent in IOPB.

Address Capability: Up to 16 MB supported by the IEEE-796.

Packaging: One IEEE-796 Multibus standard size printed circuit card. Requires 5 Amps @ +5 VDC power from the backplane.

Environment: Meets IEEE-796 specifications.

IEEE-796 Compliance: Master D16 M24 V0L and Slave D8 I16.

FOOTNOTES

[1]Multibus is a trademark of Intel Corp.
[2]RMX is a trademark of Intel Corp.
[3]XENIX is a trademark of Microsoft Corp.
[4]UNIX is a trademark of Western Electric Corp.

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International Subsidiary: Xylogics International Ltd., 46-48 High Street, Slough, Berkshire SL1 1ES United Kingdom (753) 78921 TLX (851) 847978

Corporate Headquarters:
Xylogics, Inc., 144 Middlesex Turnpike, Burlington, MA 01803
(617) 272-8140 TWX (710) 332-0262

144 Middlesex Turnpike
Massachusetts 01803