

**Xylogics**



HOME OF THE PHOENIX

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Phoenix 211 Disk Controller

Operator's Manual

Volume 1 of 11

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PHOENIX 211 CDC DISK SUBSYSTEM UNPACKING AND  
INSTALLATION INSTRUCTIONS

1.0 Unpacking Instructions

The Phoenix 211 Disk Controller physically consists of five printed circuit boards and one systems unit. The boards and systems unit are individually packed in one common shipping container, along with the appropriate documentation.

Inspect the shipping container for obvious shipping damage and notify the carrier immediately in the event of any damage.

Carefully unpack and set aside each printed circuit board and systems unit assembly.

Refer to Phoenix 211 Installation Instructions.

2.0 CDC SMD Disk Drive Unpacking Instructions

The CDC documentation manuals are located in the storage cabinet at the base of the drive, or in the shipping box.

Follow the detailed unpacking and installation instructions outlined in Section 1.0, Volume 1 of 2 of the CDC Hardware Maintenance Manual.

WARNING      The CDC disk drive has been shipped with a restraint installed to prohibit head carriage movement. This restraint must be removed prior to applying power to the disk drive. Failure to remove this shipping pin prior to power application may damage the disk drive.

2.1 Installation Procedure for Storage Module Drive Index/Sector on "B" Cable, 75 Pin Amp Connector Interface

Note 1) This procedure is applicable for units serial number 713 and above.

Note 2) Skip Section 2.1 for Flat Cable Interface



- 2.1.1 Power down unit.
- 2.1.2 Open case assembly
- 2.1.3 Loosen logic chassis hold-down bar. Raise logic chassis, and support with logic support arm.
- 2.1.4 Remove connector (PA6) from the logic backpanel.
- 2.1.5 Remove the following pins from the P6 connector, PA6-05A, PA6-05B, PA6-06A and PA6-06B. Insulate these wires to prevent any shorting.
- 2.1.6 Locate spare wires in the existing harness which are presently capped. Remove the heatshrink caps from the wires which go to P2-EE, HH, FF, and JJ.
- 2.1.7 Determine the continuity of each wire and install them in connector PA6 as follows:
 

J2-HH to PA6-06B	White Wire	Bottom Cable
J2-EE to PA6-06A	Black Wire	
J2-JJ to PA6-05B	White Wire	Top Cable
J2-FF to PA6-05A	Black Wire	
- 2.1.8 Reinstall connector PA6 onto backpanel.
- 2.1.9 Remove logic chassis card cover.
- 2.1.10 Remove transmitter card (BTVV) in Location A06.
- 2.1.11 Rework the transmitter card by cutting the foil to Pin 10 of I.C. A3. Then add a jumper from Pin 10 to Pin 5 of I.C. A3. (see Figure 1 attached).
- 2.1.12 Reinstall BTVV in location A06.
- 2.1.13 Change manual No. 83308400 Pg. 4.12 as shown in Figure 2.

2.2 Sector Selection Procedure # 1 (For all CDC Drives)

- 2.2.1 Remove FLTV logic card from the card cage.  
(See table for location)
- 2.2.2 Using Figure 3 set the switches to the desired sector quantity. If the desired sector number is not shown on Figure 3 see section 2.3 for explanation of dibits and the equation required to select switch settings.

LOGIC CARD LOCATION

DRIVE	FLTV
9760/62, BJXX	A03
9764/66, BJXX	
9760/62, BK4, BK5	B08
9764/66, BK6, BK7	A06

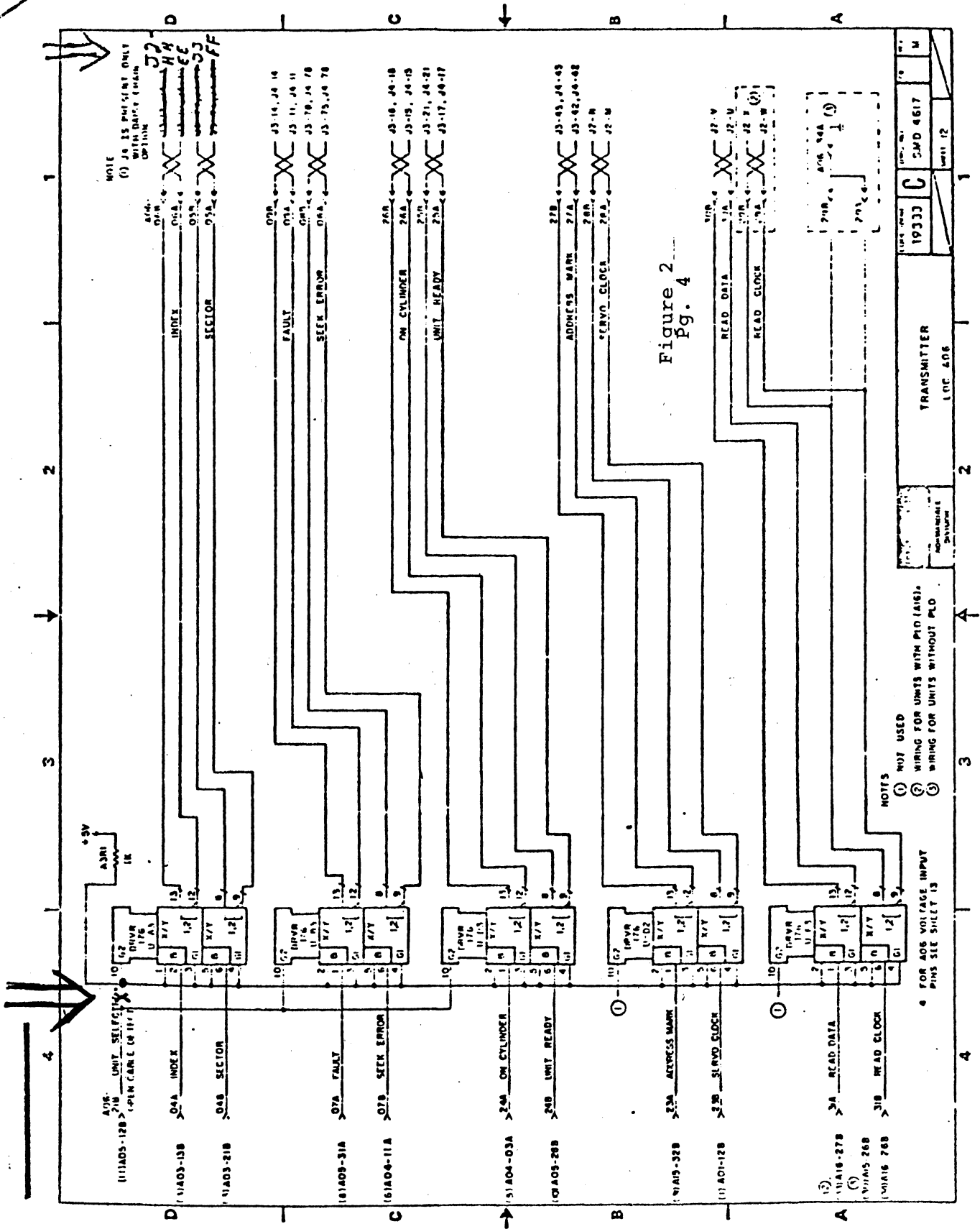
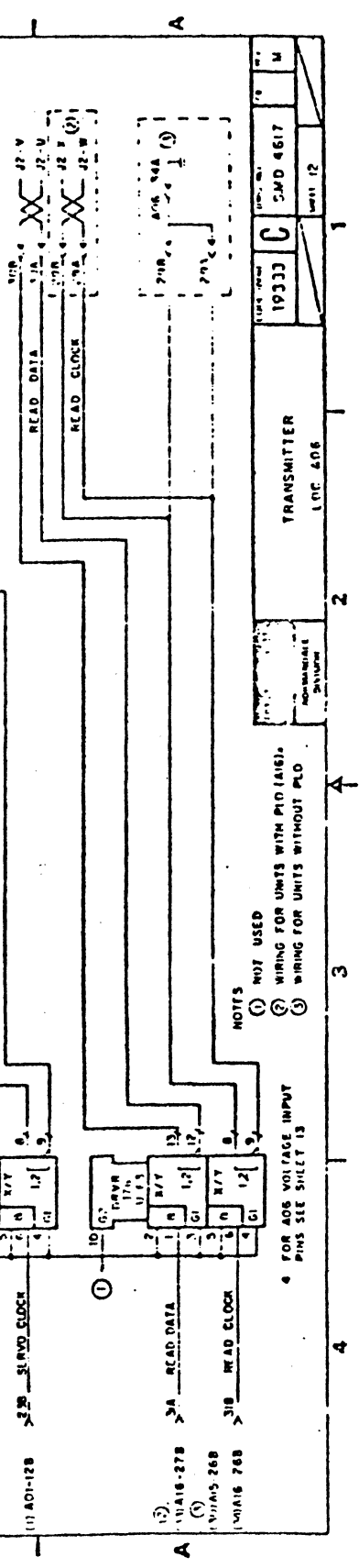


FIGURE 1

Figure 2  
Pg. 4



- NOTES
- (1) NOT USED
  - (2) WIRING FOR UNITS WITH PID (AISI)
  - (3) WIRING FOR UNITS WITHOUT PID
  - (4) FOR A06 VOLTAGE INPUT PINS SEE SHEET 13

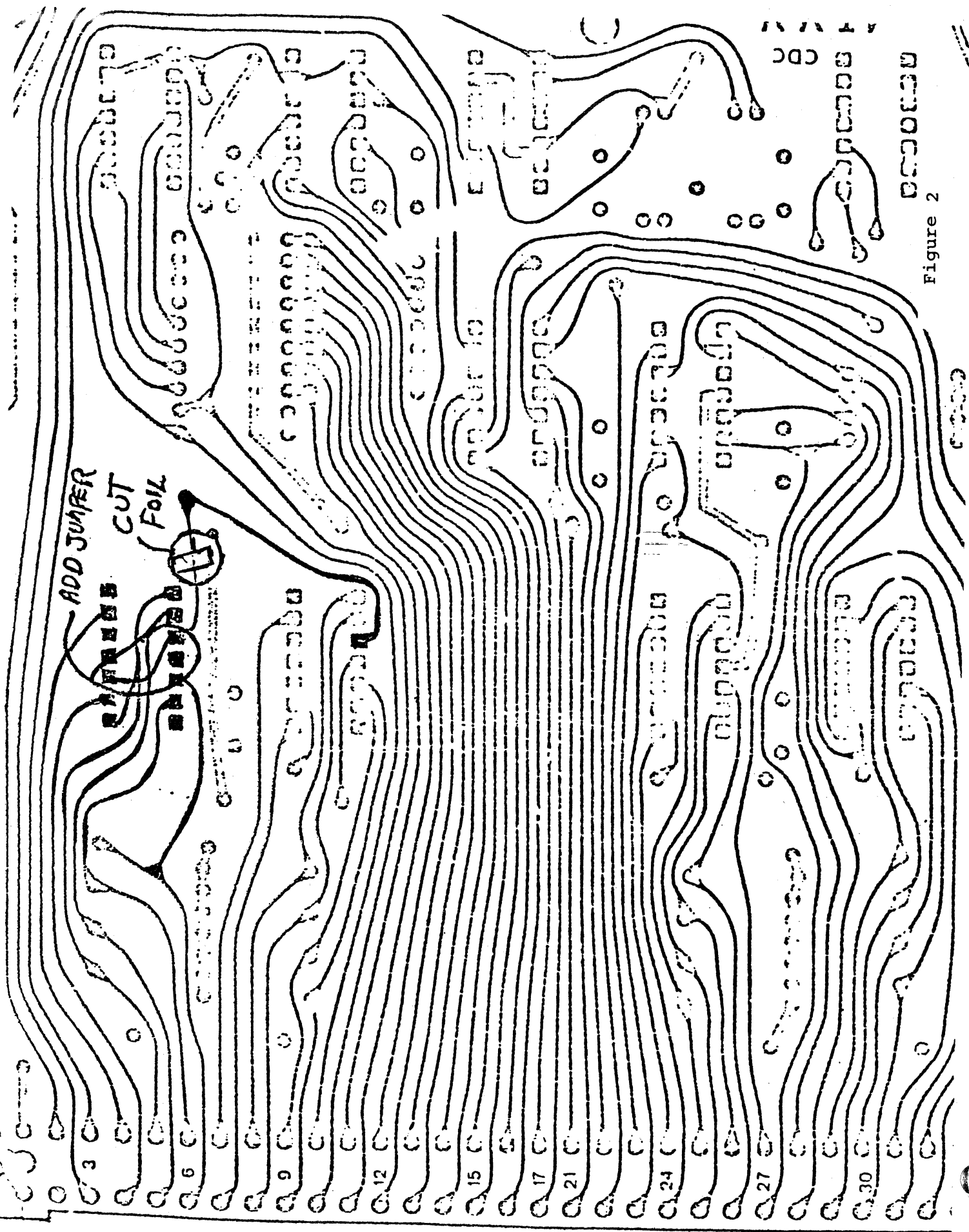


Figure 2

100-100

TABLE 2  
SW POSITION FOR EVEN LENGTH SECTORS

SECTORS	0	1	2	3	4	5	6	7	8	9	10	11
4	0	0	0	0	0	+	+	+	0	+	0	0
5	0	0	0	0	0	0	0	+	+	0	+	0
6	0	0	0	0	0	0	+	0	+	+	+	0
7	0	0	0	0	0	0	0	+	0	0	0	+
8	0	0	0	0	+	+	+	0	+	0	0	+
10	0	0	0	0	0	0	+	+	0	+	0	+
12	0	0	0	0	0	+	0	+	+	+	0	+
14	0	0	0	0	0	0	+	0	0	0	+	+
15	0	0	0	0	0	0	0	+	0	0	+	+
16	0	0	0	+	+	+	0	+	0	0	+	+
20	0	0	0	0	0	+	+	0	+	0	+	+
21	0	0	0	0	0	0	0	+	+	0	+	+
24	0	0	0	0	+	0	+	+	+	0	+	+
28	0	0	0	+	+	+	0	+	+	+	+	+
30	0	0	0	0	0	0	+	0	0	+	+	+
32	0	0	+	+	+	0	+	0	0	+	+	+
35	0	0	0	0	0	0	0	+	0	+	+	+
40	0	0	0	+	0	+	+	0	0	+	+	+
42	0	0	0	0	0	0	+	+	0	+	+	+
48	0	0	0	+	0	+	+	+	0	+	+	+
56	0	0	0	0	+	0	0	0	+	+	+	+
60	0	0	0	0	0	+	0	0	+	+	+	+
64	0	+	+	+	0	+	0	0	+	+	+	+
70	0	0	0	0	0	0	+	0	+	+	+	+
80	0	0	0	+	+	0	+	0	+	+	+	+
84	0	0	0	0	0	+	+	0	+	+	+	+
96	0	0	+	0	+	+	+	0	+	+	+	+
105	0	0	0	0	0	0	0	+	+	+	+	+
112	0	0	0	+	0	0	0	+	+	+	+	+
120	0	0	0	0	+	0	0	+	+	+	+	+
128	+	+	+	0	+	0	0	+	+	+	+	+
22	0	+	+	+	+	0	0	+	+	0	+	+
36	0	+	0	+	0	0	0	+	0	+	+	+

NOTE: + Open  
0 Closed

Fig. 3



Note: The switch positions referred to in Figure 3 do not apply to the numbers physically on the switch module but rather to the etched numbers, 0 - 11, on the logic card itself.

- 2.2.3 Reinstall the FLTV card in the proper location. Replace logic chassis card cover. Lower and secure logic chassis.
- 2.3 Sector Selection Procedure # 2 (Omit This Section if Sector Selection Completed in Section 2.2)
  - 2.3.1 Remove FLTV logic card from Position A03 or B08 in the card cage.
  - 2.3.2 Follow the explanation below and select the proper switch setting.

The FLTV card has the capability of selecting sector quantity. The number of sectors is determined by counting dibits, and each switch position gives a fixed number of dibits when closed (table 1).

TABLE 1

SW POSITION	0	1	2	3	4	5	6	7	8	9	10	11
NO. DIBITS	1	2	4	8	16	32	64	128	256	512	1024	2048

One dibit is used in resetting the counters and has to be added to each sector. To calculate the correct switch position for the number of sectors required use the following formula.

Total no. dibits  $\frac{13,440}{12}$  + no. of sectors equals the maximum number dibits per sector.

To calculate the correct no. of sectors, close the switches, which is the closest total without going over the maximum dibits per sector.

EXAMPLE:                   WANT 12 Sectors

$$\frac{13,440}{12} = 1,120$$

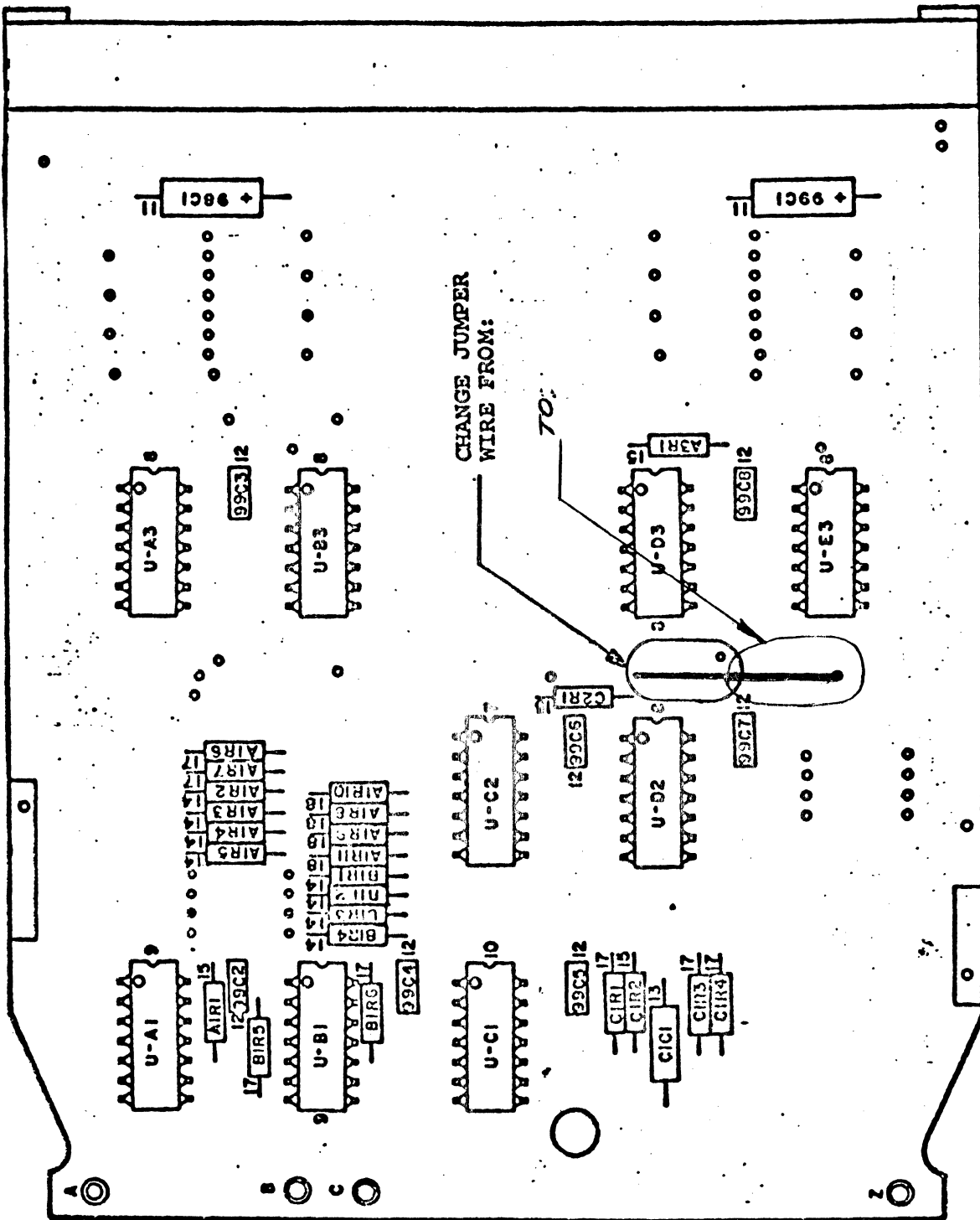


FIGURE 3A

Close SW 10 = 1024 dibits  
 Close SW 6 = 64 dibits  
 Close SW 4 = 16 dibits  
 Close SW 3 = 8 dibits  
 Close SW 2 = 4 dibits  
 Close SW 1 = 2 dibits  
 Close SW 0 = 1 dibit  
 One dibit for reset = 1 dibit  
 1120 dibits

Note: each dibit is equivalent to 12 data bits.

2.3.3 Reinstall the FLTV card in the proper location. Replace logic chassis card cover. Lower and secure logic chassis.

2.3.4 Close case assembly.

2.4 Installation Procedure for Storage Module Drive, CDC #9760 or 9762 Flat Cable

Index, Sector and Unit Select Modification (Refer to CDC SPO 68542-4)

NOTE: Skip this Section for any drive other than 40-80 MB Flat cable drive.

2.4.1 Power down unit and unplug power cable.

2.4.2 Open top case assembly and swing open logic chassis.

2.4.3 Remove the following wires from the wire wrap logic panel as follows:

<u>From</u>	<u>To</u>	<u>Z</u>	<u>From</u>	<u>To</u>	<u>Z</u>
B01-06B	JA82-18B	1	B03-06B	JA83-18B	1
B01-06A	JA82-18A	1	B03-06A	JA83-18A	1
B01-05B	JA82-25B	1	B03-05B	JA83-25B	1
B01-05A	JA82-25A	1	B03-05A	JA83-25A	1

2.4.4 Add the following wires to the wire wrap logic panel as follows:

<u>From</u>	<u>To</u>	<u>Z</u>	<u>From</u>	<u>To</u>	<u>Z</u>
B01-06B	JA82-43B	1	B03-06B	JA83-43B	1
B01-06A	JA82-44A	1	B03-06A	JA83-44A	1
B01-05B	JA82-45B	1	B03-05B	JA83-45B	1
B01-05A	JA82-45A	1	B03-05A	JA83-45A	1

2.4.5.1 Remove wire from JA82-41A.

2.4.5.2 Remove wire from JA82-41B and install this wire on JA82-41A.

2.4.5.3 Install wire removed from JA82-41A on JA82-41B.

- 2.4.6 Repeat 2.4.5 for JA83-41A and JA83-41B.
- 2.4.7 Secure logic chassis in closed position.
- 2.4.8 Locate and remove the transmitter card FTW in location B01. For dual channel units the second transmitter card is found in Location B03.
- 2.4.9 Rework the transmitter FTW as shown in Figure 3A. Remove the letter "F" from the card type designation FTW and mark a "G" in its place so that the card type becomes GTW.
- 2.4.10 Install the GTW into Location B01. For dual channels units, install the second GTW into Location B03. Close top case assembly.
- 2.4.11 Update unit FCO log, add this option as an entry on the units FCO log.

2.5 Installation Procedure for Storage Module Drive. CDC 9764 or 9766 Flat Cable Interface Index, Sector and Unit Select Modification

NOTE: Skip this section for any drive other than 150 - 300 MB flat cable drive.

- 2.5.1 Power down unit and unplug power cable.
- 2.5.2 Open top case and remove side panel to access I/O connectors.
- 2.5.3 Move the following wires:

<u>A Connector (60 Pin)</u>	<u>B Connector (26 Pin)</u>
25	13
55	26
18	12
48	24

- 2.5.4 Remove and insulate the following wires from the other A Connector, 25, 55, 18, and 48.
- 2.5.5.1 Remove wire from B Connector Pin 9 .
- 2.5.5.2 Remove wire from B Connector Pin 22 and install in Pin Location 9.
- 2.5.5.3 Install other wire in Location 22.
- 2.5.6 Remove FTW Logic Card from cage assembly location A01 (and A03 for dual port drives. )
- 2.5.7 Rework card as shown in Fig. 3A. Remove the letter "F" and add letter "G".
- 2.5.8 Install GTW card(s) in proper location(s).
- 2.5.9 Update FCO Log, add this option as an entry on the FCO Log.



### 3.0 Phoenix 211 Installation Instructions

#### 3.1 General

The Phoenix 211 Disk Controller is designed to mount directly in any 10 $\frac{1}{2}$ " PDP11 processor chassis or BALL-K Expansion Box. Installation consists of:

- a.) Physically mounting the Phoenix 211 systems unit in the PDP11 computer chassis or expansion box.
- b.) Plugging the Phoenix 211 systems unit power harness to the computer or expansion box power distribution panel.
- c.) Plugging in the four Phoenix 211 printed circuit boards supplied into the systems unit.
- d.) Plugging in the Phoenix 211 interface board and cable into PDP11 SPC slot.
- e.) Connecting the Disk Drive to the Phoenix 211 Controller using the supplied cables.
- f.) Running diagnostics to verify the integrity of the disk subsystem.

Detailed Phoenix 211 installation instructions are contained in the following paragraphs.

#### 3.2 Phoenix 211 Systems Unit Mounting Instructions

3.2.1 The Phoenix 211 Disk Controller Systems Unit will mount in any available systems unit slot in any PDP11 computer or BALL-K expansion box which allows insertion of full hex boards.

3.2.2 PDP11/05-NC, PDP11/05-SC, BALL-K Instructions

- 1.) Remove top and bottom covers of computer or expansion box to gain access to system unit mounting area.

Carefully save all screws removed for later installation.

- 2.) Tilt computer or expansion box up on slides to expose system unit wirewrap field.

Caution: Insure that existing cables have adequate slack before tilting unit.

Note: The PDP11/05-NC chassis requires a 9 position power connector, all other configurations are 15 position.

- 3.) Physically place the Phoenix 211 Systems Unit in the next available systems unit slot.

Caution: Insure that the system unit is physically oriented such that the systems unit power harness extends over the computer or expansion box power distribution panel.

- 4.) Fasten the systems unit to the computer or expansion box chassis by engaging the two captive screws located at each end of the systems unit with matching threaded holes in the computer or expansion box chassis.

Tighten the captive screws with a screwdriver.

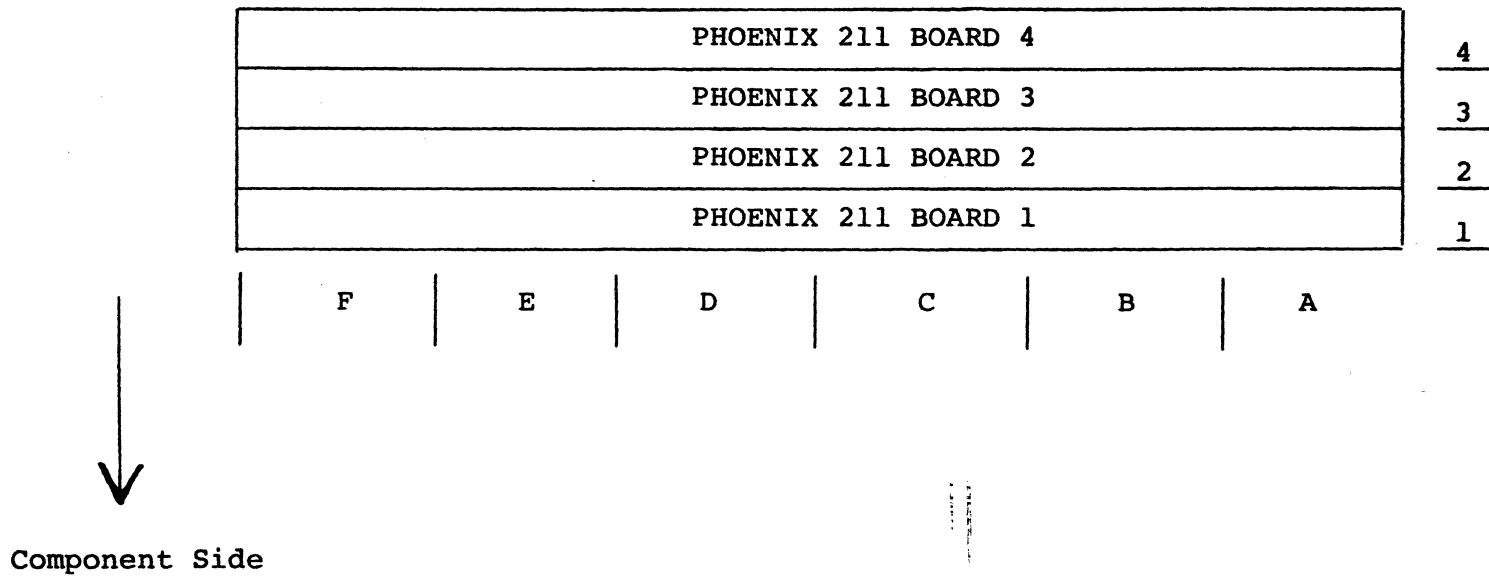
- 5.) Connect the systems unit power harness to the computer or expansion box power distribution panel by plugging the power harness connector into a matching distribution panel receptacle.

- 6.) With the computer in the "Halt" turn power on. Insure that +5v DC is present on the systems unit backplane printed circuit board between the power harness red wire pads (+5v) and the black wire pads (GND). Insure that -15VDC is present on the systems unit backplane between the power harness violet wire pad (-15) and the black wire pads (GND). Turn power off.

- 7.) Tilt computer and expansion box chassis to normal position.

FIGURE 4  
PHOENIX 211 DISK CONTROLLER  
SYSTEMS UNIT UTILIZATION

(Top of Board View)



4.0 Reference: Figure 4

Phoenix 211 Printed Circuit Board Installation

4.2 Carefully plug Phoenix 211 Board #1 into the system unit slot.

Caution: Insure that board is correctly oriented with respect to other boards before plugging in board.

4.3 Carefully plug Phoenix 211 Board #2 into the system unit slots A2-F2.

a.) Slide board carefully along computer or expansion box card guides until connector fingers engage the systems unit connector receptacles.

b.) Start board to seat into systems unit by firmly "rocking" the board into place by pushing down alternately on left and right handles of board.

c.) Seat board in final position by pushing down evenly on the board handles.

4.4 Carefully plug Phoenix 211 Board #3 and #4 into the system unit slots A3-F3 and A4-F4 respectively by following the procedure outlined in 4.3 for board #2.

4.5 Insure that all boards are seated properly by checking the relative height of the board handles.

4.6 Carefully plug the Phoenix 211 PDP11 coupler Board into the available standard small peripheral controller (SPC) slot by following the procedure outlined in section 4.3 and 4.5.



- 4.7 Install the interconnect cable between the Phoenix 211 Board #1 and the Phoenix 211 PDP11 interface Board.

IMPORTANT - Note the pin #1 designations on the cable and on the Boards.

#### 5.0 NPR Grant Jumper Removal Instructions

- 1.) The Non-Processor Request grant is normally jumpered across in all standard peripheral slots. This line must be removed in order to operate the Phoenix 211 Disk Controller as in all direct memory access devices. This jumper is located between CA1→CB1.
- 2.) Reference Fig. 6 - Locate the C connector field of the SPC slot containing the Phoenix 211 PDP11 coupler card.
- 3.) Reference Fig. 6 - Remove the wirewrap wire connecting pins CA1 to CB1 of the slot containing the Phoenix 211 PDP11 coupler card and only of that slot.

Note: a.) Connector "C" is the third connector from the Unibus end of the backplane.

b.) The CA1 and CB1 pins are the first positions of the "C" connector (See Fig. 6).

c.) If the Phoenix 211 PDP11 coupler is ever relocated or removed, reconnect CA1 to CB1.

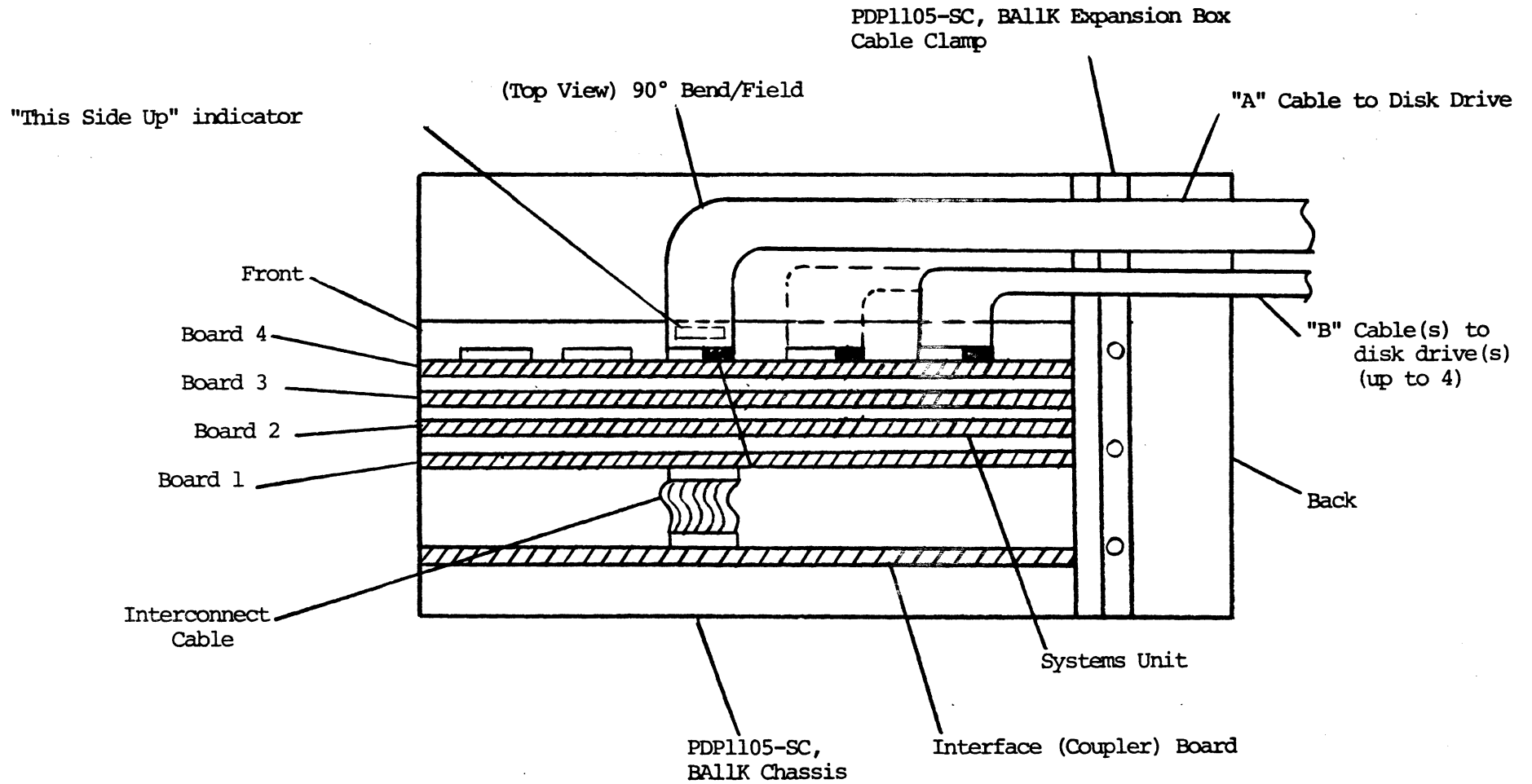
#### 6.0 Phoenix 211 Cabling Instructions

The Phoenix 211 can have from 2 to 5 cables connected from Board #4 going to from one up to four disk drives.

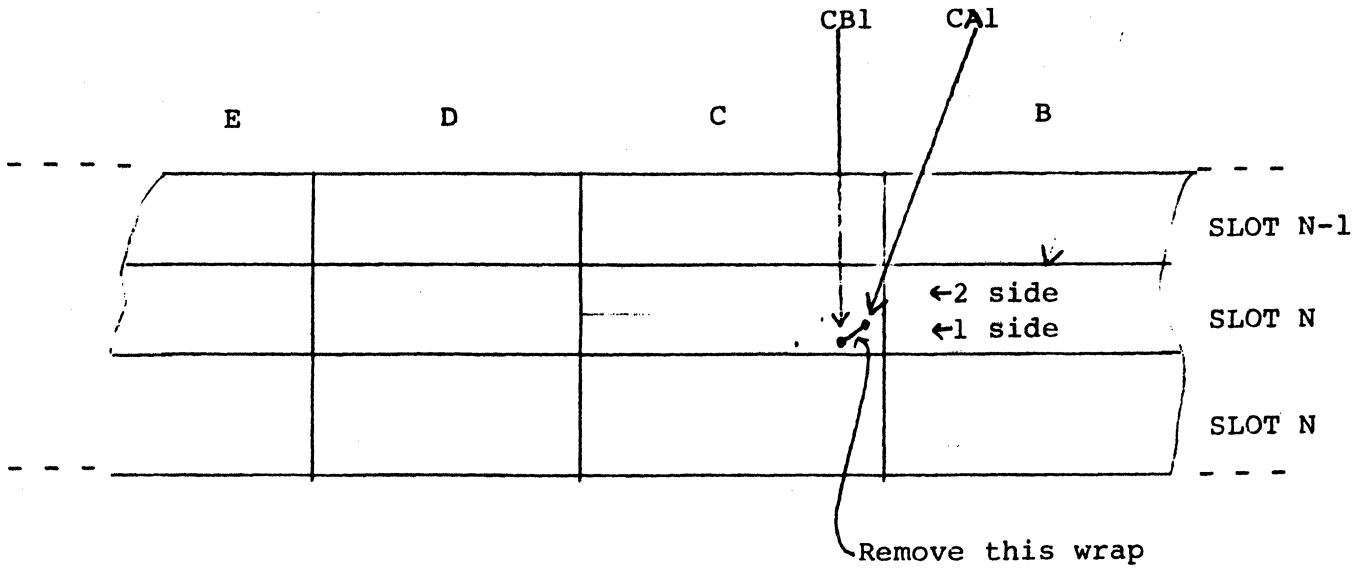
- 6.1 A 60 conductor ribbon "A" cable and a 26 conductor ribbon "B" cable per drive is used to connect the Phoenix 211 formatter to the disk(s).
  - 6.1.1 Remove the screws on the top rear of the computer or expansion box holding the cable clamp.
  - 6.1.2 Plug the "A" cable (60 pin) into the connector on Board #4 making sure the pin #1 designations of both cable and connector are correctly aligned.
  - 6.1.3 Plug the "B" cable(s) into the drive port connectors on Board #4.

Note: The port designations do not correspond to the drive identification numbers, i.e. drive number 0 can be plugged into any port 0-3 and it will remain drive 0.

FIGURE 5  
PHOENIX 211 DISK CONTROLLER  
DISK DRIVE CABLE INSTALLATION



Slot containing  
Phoenix 211 PDP11  
coupler card



PHOENIX 211 DISK CONTROLLER  
REQUIRED DMA GRANT BACKPLANE CONNECTIONS

FIGURE 6

NOTE: Backplane connector "A" is normally at the top, when the backplane is vertically mounted or at the front of the computer or expansion box when the backplane is horizontally mounted.

Caution: Insure that the cable connections are oriented such that pin #1 to the cable matches pin #1 of the receiving connector.

6.1.4 Dress the cables to obtain minimum strain on the board connectors. (this may require a 90 degree bend). Check that when the computer or expansion box cover is reinstalled all cables are clear if being pinched or cut. (See Fig. 5)

6.1.5 Reinstall the cable clamp and screws

#### 7.0 Disk Drive Connection Instructions

For Flat Cable Interface skip to 7.4

Reference: Control Data Hardware

Maintenance Manual vol. 1 of 2 Pg. 1-10, 11

The disk drive cable is terminated at the disk drive end with a drive terminator plug (CDC P/N 40067207) which plugs into an "A" cable position, J4, at the rear of the drive.

7.1 Attach the "A" Cable to J3 at the rear of the disk drive.

7.2 Attach the "B" cable (s) to J2 at the rear of the disk drive(s).

7.3 Attach the terminator plug to J4 at the rear of the drive.

(See Note end of Section 7)

Continue on Section 8

7.4 Attach the "A" Cable to IJ3 (IIJ3 for Port II). (See Fig. 7 for CDC9762)

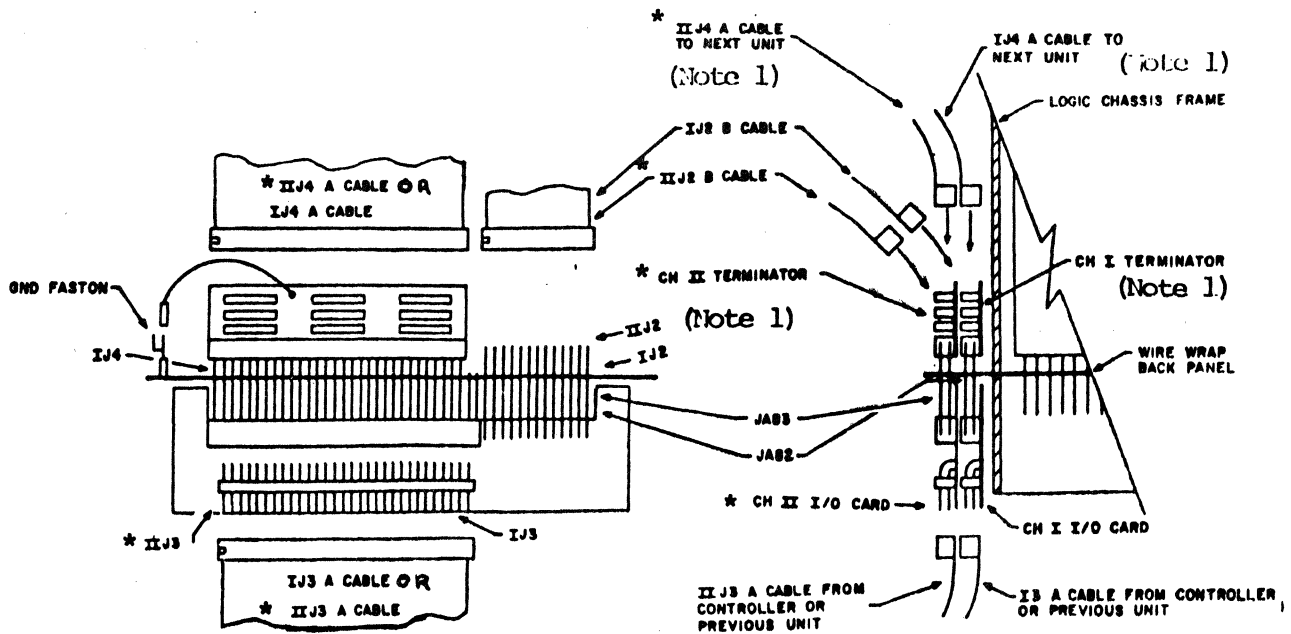
7.5 Attach the "B" cable to IJ2 (IIJ2 for Port II).

7.6 Attach Terminator (s) to IJ4 (IIJ4 for Port II). See Note at end of Section 7.

Caution: Insure that the cable connections are oriented such that pin #1 to the cable matches pin #1 of the receiving connector.

Note: Units interfaced with more than one disk drive require a daisy chain cable. This cable is connected in place of the terminator plug. At the end of the chain a terminator is still required. (See Hardware Maintenance Manual Vol. 1 of 2 Fig. 1-7, pg. 1-11).





\*All CHII Designations refer to Channel II on a dual port drive.

Notes 1.) If there is only one drive or if the drive being cabled is the last daisy chained drive a terminator must be installed. If the drive is to be in the daisy chain, the "A" cable from the previous unit must connect to J3 and the "A" cable to the next unit must connect to J4.

FIGURE 7

## 8.0 Initial Power Turn-On Instructions

### 8.1 Disk Drive Power Turn-On Instructions

Remove all shipping hardware and go through initial power turn-on procedure outlined by the disk drive manufacturer in his respective reference manual.

**Warning:** Failure to remove all disk drive shipping constraints before applying power may cause permanent damage to the disk drive.

### 8.2 Phoenix 211 Disk Controller Power Turn-On Instructions

8.2.1 With the computer in "Halt" mode turn power on to the system. Observe that the computer "run" indicator remains out.

### 8.2.2 Manual Console Control Check

Insure that the computer bus is normal by checking that all console switch register functions operate properly.

Check specifically for proper operation of "Load Address", Deposit, and Examine functions in multiple mode.

If console functions do not operate properly, check for proper Unibus connections, and termination.

### 8.2.3 Manual Disk Controller Status Check

- 8.2.3.1 With the disk drive stopped insert 764000 (Control and Status Reg.) Address into Console Switch Register.
- 8.2.3.2 With the Halt/Enable Switch in Halt Position, momentarily depress the "Load Address" and "Start" Console switches in succession.
- 8.2.3.3 Successively momentarily depress the "Examine" console switch. Observe that each of the Disk Controller Registers contains the proper content as specified in Table 1.
- 8.2.3.4 Run the Phoenix 211 Disk Controller Diagnostic per section 9.

TABLE 1

PHOENIX 211 DISK CONTROLLERINITIAL POWER ON REG STATUS

<u>REGISTER</u>	<u>ADDRESS</u>	<u>PROPER CONTENTS</u>
Control & Status	164000	200
Unit, Sector, Head	164002	0
Buss Address	164004	0
Word Count	164006	0
Cylinder Address	164010	0
Disk Status	164012	0
Disk Error	164014	0

9.0 Diagnostic Program Loading & Operating Instructions9.1 General

The Phoenix 211 Disk Controller Diagnostic is supplied as a paper tape load module. The diagnostic load module is in absolute format and can be loaded by the standard DEC Absolute Loader.

9.2 User Considerations - .1 Diagnostic will destroy data on any disk cartridge contained in the disk drive when it is run.

User should put a scratch disk cartridge in the disk drive before running the disk diagnostic.

The Diagnostic Program requires a formatted scratch disk cartridge for proper operation. Disk cartridges may be formatted using the format program located at the end of the diagnostic (Test 49).

## 9.3 Detailed Operating Instructions -

Detailed operating instructions are contained at the beginning of the disk diagnostic.

## 10.0 Phoenix 211 Parameter Selection

The Phoenix 211 Disk controller may be configured to varied system application requirements by appropriately adjusting strappable control parameters. This section is devoted to defining all Phoenix 211 adjustable parameters and available settings.

### 10.1 Base Register Address Selection (Reference Drawing D-1025-08, Sht 3)

The base Unibus register address of the standard Phoenix 211 Disk Controller is selectable MOD 20<sub>g</sub> and the Command Queue version of the Phoenix 211 Disk Controller is selectable MOD 40<sub>g</sub>.

- 10.1.2 The standard base address of the Phoenix 211 Disk Controller is 764000<sub>g</sub>, and staples are provided on the Phoenix 211 Coupler Board to enable other base addresses to be utilized.
- 10.1.3 The Address selection logic is shown on the upper lefthand corner of sheet 4 of D-1025-08.
- 10.1.4 The following Table shows the selectable address bits and the corresponding control staples.

TABLE 1

Base Register Address Selection

<u>Address Bit</u>	<u>Control Staple Point</u>
A12	B15-13
A11	B15-15
A10	C15-02
A09	C15-04
A08	C15-06
A07	C15-11
A06	C15-13
A05	C15-15

Note: 1.) For an address bit to be a logic "1", the control staple point must be wired high to the pull up string associated with J5-15.

2.) For an address bit to be a logic "0", the control staple point must be wired low to any convenient ground point.

### 10.2 Interrupt Vector Address Selection (Reference D-1025-08, Sht 1)

10.2.1 The standard interrupt vector value for the Phoenix 211 Disk Controller is 270<sub>g</sub>.

10.2.2 The interrupt vector control logic is shown on the lower right section of sheet 1 of D-1025-08.

- 10.2.3 Other interrupt vector values are selectable by wiring appropriate vector control signals directly to the corresponding Unibus Data Signals.
- 10.2.4 Table 2 below shows the interrupt vector Address bits and the corresponding required wiring.

TABLE 2

Interrupt Vector Address Selection

<u>Vector Address Bit</u>	<u>Required Control Wiring</u>
A02	A08-01 to CU2
A03	A08-04 to CT2
A04	A08-10 to CN2
A05	A08-13 to CP2
A06	C08-01 to CV2
A07	C08-04 to CM2

Note: 1.) Logic 1 = control wire in.

2.) Logic  $\emptyset$  = control wire removed.

10.3 Interrupt Priority Level Selection (Reference D-1025098, Sht 1)

- 10.3.1 The standard interrupt priority level for the Phoenix 211 Disk Controller is BR5.
- 10.3.2 The interrupt priority level of the Phoenix 211 Disk Controller is determined by staples at component location A9 on the Phoenix 211 Coupler Board as shown on the lower right hand corner of sheet 1 of D-1025-08.
- 10.3.3 Required BR4 Stapling

Required stapling for BR4 interrupt priority stapling is as follows:

- 1.) A09-01 to A09-05
- 2.) A09-02 to A09-15
- 3.) A09-03 to A09-14
- 4.) A09-04 to A09-13
- 5.) A09-07 to A09-11
- 6.) A09-12 to A09-16

#### 10.3.4 Required BR5 Stapling

Required stapling for BR5 interrupt priority is as follows:

- 1.) A09-01 to A09-16
- 2.) A09-02 to A09-05
- 3.) A09-03 to A09-14
- 4.) A09-04 to A09-13
- 5.) A09-07 to A09-10
- 6.) A09-12 to A09-15

#### 10.3.5 Required BR6 Stapling

Required stapling for BR6 interrupt priority is as follows:

- 1.) A09-01 to A09-16
- 2.) A09-02 to A09-15
- 3.) A09-03 to A09-05
- 4.) A09-04 to A09-13
- 5.) A09-07 to A09-09
- 6.) A09-12 to A09-14

#### 10.3.6 Required BR7 Stapling

Required stapling for BR7 interrupt priority is as follows:

- 1.) A09-01 to A09-16
- 2.) A09-02 to A09-15
- 3.) A09-03 to A09-14
- 4.) A09-04 to A09-05
- 5.) A09-07 to A09-08
- 6.) A09-12 to A09-13

### 10.4 DMA Throttle Value Selection (Reference D-1025-08, Sht 2)

On the Phoenix 211 Disk Controller the number of consecutive DMA Memory cycles that are to be used by the disk controller for data transfers is uniquely selectable from 1 to 256 words via the DMA "Throttle" Control Logic and associated control staples are shown on the lower right hand corner of sheet 2 of D-1025-08.

10.4.1 The normal factory setting for the DMA Throttle is 8.

10.4.2 The DMA Throttle setting enables the user to adapt the Phoenix 211 Disk Controller to the Unibus environment and system configuration of his application via limiting the maximum number of consecutive DMA cycles utilized by the disk controller for data transfers.

### 10.4.3 Throttle Selection

DMA throttle value selection is accomplished via staples located on connector J1.

(J1 is the rightmost connector position at the top of the Phoenix 211 Interface Board.) Table 3 below defines the control staples and corresponding binary weighted values associated with the DMA Throttle Logic.

TABLE 3

DMA THROTTLE SELECTION

<u>Staple No.</u>	<u>Binary Weight</u>	<u>Required Connection Points</u>
1	1	J1-19 to J1-20
2	2	J1-21 to J1-22
3	4	J1-23 to J1-24
4	8	J1-25 to J1-26
5	16	J1-27 to J1-28
6	32	J1-29 to J1-30
7	64	J1-31 to J1-32
8	128	J1-33 to J1-34

Note: The DMA Throttle value selected is equal to the sum of the binary weights of the control staples inserted.

### 10.5 Maximum Head Value Selection (Reference Board 3 Logic Drawing D-1034-01, Sheet 5)

The Phoenix 200 Disk Controller may be used with a large number of disk drives of varying capacities and number of heads.

The disk controller will automatically abort on any attempt to utilize a non-existent head of any disk drive connected to it, provided that the maximum number of allowable heads to be utilized is defined to it via control staples.

10.5.1 The maximum head decode logic is shown on the lower right hand corner of sheet 5 of logic drawing D-1034-01.

10.5.2 Normal Maximum Head Selection. Normal or not mixed drive head configurations are provided by connecting or not connecting pins 1-5 of location E11 of Phoenix 200 Board 3 to ground as appropriate to select the desired maximum number of heads.

10.5.2.1 The interconnections on the logic drawing select a maximum of five heads ( $\emptyset$ -4).

10.5.2.2 Table 4 below shows the binary weight of each control pin at location E11.

TABLE 4

Maximum Head Value Selection

<u>Board 3, Location Ell Control Pin No.</u>	<u>Binary Weight</u>
1	1
2	2
3	4
4	8
5	16

- Note: 1.) For a logic 1, leave pin open  
2.) For a logic 0, tie pin to ground at Ell-15 or Ell-8.  
3.) The maximum head value selected is equal to the sum of all logic "1" or open Ell select pins plus 1.

10.5.3 Mixed Disk Drive Maximum Head Selection

When drives of different numbers of heads are connected to the disk controller at the same time, two alternatives are possible for head selection.

10.5.3.1 Mixed Drive Head Select Option 1

The user could select per above procedure the maximum number of heads allowable for the disk drive of the largest capacity.

The only possible disadvantage to this approach is that this would permit the programmer to attempt to overrun any disks of lesser capacity and could result in putting the disk drive in the Fault state.

10.5.3.2 Mixed Drive Head Select Option 2

Location Ell is already preconnected to accommodate a ROM. A ROM could be optionally inserted into location Ell (at extra cost) which would provide the correct maximum number of head value to the selection logic as a function of what disk drive is selected.

This solution thus will not allow the programmer to select a not existent head on any disk drive connected to the disk controller no matter what number of heads is associated with what disk drive.

The only restriction is that the system cabling configuration, once defined, must remain constant with respect to what capacity disk drive is connected to what radial port of board 4 of the disk controller.



- 10.6 Maximum Sector Value Selection (Reference Board 3 Logic Drawing D-1034-01, Sheet 5 and Board 3 Assembly Drawing D-1034-03)
- 10.6.1 The Phoenix 200 Disk Controller may be set up to accommodate a varying number of sectors per track by selection staples provided on Board 3 of the Formatter at Component location E11.
- 10.6.2 The standard factory setting for the number of sectors/track is 32.
- 10.6.3 The disk controller will automatically abort when any attempt is made to utilize a non existent sector of any disk drive connected to it.
- 10.6.4 The disk controller maximum sector selection and comparison logic is shown at the upper right hand corner of Sheet 5 of logic drawing D-1034-01.
- 10.6.5 The selection reference value established by the user by tying pins 1-7 of component location E10 to ground or leaving them open is compared with the sector address contained in the DUSH register.

A non existent sector error is generated whenever the contents of the sector field of the DUSH Register is greater than that specified by the strapping of location E10.

- 10.6.6 The strapping shown on the logic drawing is for the standard 32 sectors per track configuration.
- 10.6.7 Table 5 below shows the binary maximum sector selection value of each control pin at location E10.

Table 5

Maximum Sector Value Selection

<u>Board 3 Location E10 Control Pin No.</u>	<u>Sector Select Binary Weight</u>
1	1
2	2
3	4
4	8
5	16
6	32
7	64

- Note:
- 1.) For a logic 1, leave pin open.
  - 2.) For a logic 0, tie the pin to ground at E10-15 or E10-08.
  - 3.) The maximum sector value selected is equal to the sum of all logic "1" or open E10 select pins plus 1

10.7 Defective Sector Identification and Skip Option Selection (Reference Sheet 1 of Board 3 Logic Drawing D-1034-01 and Assembly Drawing D-1034-03.)

If any sectors on a disk medium utilized are defective, in terms of any bit cells being unable to properly contain both logic 1 and logic data states, as determined by a disk pack initialization utility after the medium is formatted, the disk controller may be optionally set up to skip over such defective sectors whenever they are encountered during normal data transfers.

10.7.1 Normal Handling of "Hard" Defective Sectors

Hard defective sectors are normally located by disk utility programs such as "BAD" under RSX11-M.

The utility program rotates a worst case data pattern through every character of every sector data field on the disk medium.

Any defective sectors found are cataloged by the utility program and allocated to a file created on the medium called "BAD".

Hence, all "hard" defective sectors are then prevented from being allocated to normal user programs by the file management and no special action is required by the disk controller.

10.7.2 Normal Disk Controller Staple Setting

The proper factory setting for the disk controller for normal handling of any "hard" defective sectors is for staple W1 on Board 3 to be removed.

10.7.3 Optional Skip on Detection of Defective Sector

Optionally the disk controller may be set up to automatically skip over any hard defective sectors referenced in any data transfer operation.

- 10.7.3.1 In this mode of operation the header of any defective sectors found by the disk initialization utility program would be re-formatted to set the two "Bad Sector Flag" bits contained in the sector header.
- 10.7.3.2 The disk controller would then automatically skip over any such sector when the Bad Sector Flag bits were accessed along with the header during sector position verification.
- 10.7.3.3 This mode of operation permits the user to perform multiple sector transfers involving defective sectors without having the data transfers to be delimited by defective sectors.
- 10.7.3.4 This mode of operation is selected by connecting staple W1 on board 3 as shown on the lower left hand corner of Sheet 1 of logic drawing D-1034-01.

#### 10.7.4 Optional Abort on Detection of Defective Sector

- 10.7.4.1 The disk controller may be optionally set up to abort any operation involving a flagged defective sector in any data transfer on the basis that the file management system should not allocate any defective sectors for transfers.
- 10.7.4.2 In this mode of operation defective sectors are determined by the disk utility and the Bad Sector Flag bits are set in the headers of all defective sectors as above.
- 10.7.4.3 However, whenever the disk controller detects that a defective sector is being accessed, as determined by the presence of the "Bad Sector Flag" header bits, the disk controller will immediately abort whatever data transfer is being conducted.
- 10.7.4.4 This abort on detection of defective sector mode is selected by removing staple W1 from board 3 as shown on the lower right hand corner of Sheet 1 of logic drawing D-1034-01.

#### 10.7.5 W1 Control Staple Location (Reference Board 3 Assembly Drawing D-1034-03)

The defective sector control staple W1 is etched onto the etch side of the printed circuit board just above and parallel to resistor R9.

#### 10.8 CDC Disk Radial Port Selection (Reference Sheet 2 of CDC Board 4 Logic Drawing D-1035-01 and CDC Board 4 Assembly Drawing D-1035-03)

- 10.8.1 The Phoenix 200 Disk Formatter can control up to four disk drives.

Each disk drive requires connection to the disk formatter via the so called "B" or "Radial" Cable.

- 10.8.2 Four 26 pin Berg connectors are provided on Board 4 of the formatter to accommodate up to four radial disk drive cables. These connectors are labeled J1, J2, J4 and J5, with J1 being the rightmost connector on the board and J5 being the leftmost connector.

- 10.8.3 Any disk drive radial cable may be connected to any physical radial connector provided on the board.

However, any radial connector ports not being used should be disabled by staple selection to prevent introduction of noise into the disk formatter.

- 10.8.4 The radial cable interface logic for the four possible disk drives is contained on Sheet 4 of the CDC Board 4 logic drawing D-1035-01.

- 10.8.5 The presence of control staples W35, W6, W34 and W33 enable the formatter receiving logic for connectors J1, J2, J4 and J5 respectively. (These are located in the middle of each port logic section.)

10.8.6 The factory staple settings for various numbers of disk drives is shown below.

<u>Number of Connected Disk Drives</u>	<u>Connectors Used</u>	<u>Staples Inserted</u>
1	J1	W35
2	J1,J2	W35,W6
3	J1,J2,J4	W35,W6,W34
4	J1,J2,J4,J5	W35,W6,W34,W33

Note: User must use radial connectors corresponding to radial port enable staple configuration.

10.9 Rotational Positioning Sensing Selection (Reference Sheet 3 of CDC Board 4 Logic Drawing D-1035-01 and Board 4 Assembly Drawing D-1035-03)

10.9.1 Rotational Position Sensing (RPS) is a standard feature of the Phoenix 200 Formatter. Rotational Position Sensing enables a user to maximize disk subsystem throughput by considering sector position information as well as head cylinder position information in transfer allocation among multiple disk drives.

10.9.2 Seek Complete in the Phoenix 200 Formatter is defined as being both "ON CYLINDER" and "ON SECTOR".

To allow for operating system overhead the seek complete signal is normally generated four sectors before the actual target sector allowing a nominal two millisecond for software setup time. (This delay is programmable.)

10.9.3 The Rotational Positioning Sensing logic is shown on Sheet 3 of the CDC Board 4 logic drawing D-1035-01.

10.9.4 Rotational Position Sensing Enable/Disable Control Staple

10.9.4.1 Rotational Position Sensing is enabled if control staple W3 is inserted. When this staple is inserted, seek complete cannot be generated until the current actual and reference commanded sector are identical, as determined by the sector comparator logic.

When sector comparison occurs, signal LASECCOMP is high or active.

10.9.4.2 When staple W3 is removed, rotational position sensing is disabled as LASECCOMP is always active.

10.9.5 Sector Remapping ROM's

10.9.5.1 In order to generate the sector comparison signal four or more sectors ahead of the actual target sector, the actual target sector address is mapped via ROM's A7, C7, B7 & C8 to the address of the sector two after it.

10.9.5.2 ROM A7 is normally the only one supplied with a standard 32 sector formatter, since only one (32 X 8) ROM is required to remap 32 sectors.

10.9.5.3 ROM's C7, B7 & C8 are only required if the formatter is set up for more sectors as indicated on the logic drawings.

#### 10.9.6 Temporary Storage of Reference Target Sector Address

10.9.6.1 Seek Commands for multiple drives may be overlapped by the user, and the formatter has only one sector command field in the DUSH Register.

10.9.6.2 To provide rotational position sensing in an overlapped seek environment, the commanded sector must be saved temporarily to provide a reference target sector address for each disk drive.

10.9.6.3 The commanded target sector for each disk drive is stored in the internal registers implemented by components A9 & A10 when any Seek operation is initiated. This reference sector value is then accessed and used by the seek sector comparison logic.

Note: To utilize rotational position sensing properly, the user must define the target sector at the time that a Seek Only command is initiated.

#### 10.10 Optional Sector Interleaving Selection (Reference Sheet 5 of CDC Board 4 logic drawing D-1035-01 and Board 4 Assembly drawing D-1035-03.

10.10.1 The Phoenix 200 Formatter supports absolute contiguous sector addressing as standard and interleaved sector addressing as optional.

10.10.2 The Sector interleaving control logic is shown on the upper right hand corner of Sheet 5 of Board 4 logic drawing D-1035-01.

10.10.3 Sector Interleaving in the Phoenix 200 Formatter is achieved by ROMS C6, D6, A6 and B6 so that any desired interleaving can be readily programmed. One to four ROM's may be required for interleaving depending on how many sectors are used, as shown on the logic drawing.

10.10.4 Phoenix 200 Formatters are normally set up at the factory for absolute contiguous sector addressing so that at location C6, jumpers are shown directly connecting input sector address lines to corresponding output sector address lines.

10.10.5 A one time, non-recurring charge will be assessed for any controllers ordered with interleaving to recover programming and testing costs.

#### 10.10.6 Control Staple Settings for Interleaving More Than 32 Sectors

When sectors are to be interleaved, control staples W1 and W2 must be removed.

Table 6

Sector Interleaving Required Control Staples and ROMS

<u>No. of Sectors</u>	<u>Required Staple Deletes</u>	<u>Required ROMS</u>
0 - 31	W1,W2	C6
32 - 63	W1,W2	C6,D6
64 - 95	W1,W2	C6,D6,A6
96 - 127	W1,W2	C6,D6,A6,B6

10.11 Maximum Cylinder Selection Logic (Reference Sheet 4 of CDC Board 4 Logic Drawing D-1035-01 and CDC Board 4 Assembly Drawing D-1035-03)

10.11.1 The Phoenix 200 Formatter may be used with a large number of disk drives with a varied number of cylinders.

The disk formatter will automatically abort on any attempt to utilize a non-existent cylinder of any disk drive connected to it, provided that the maximum number of allowable cylinders to be utilized is defined to it via control staples.

10.11.2 The maximum cylinder decode logic is shown on the lower right hand corner of Sheet 4 of the CDC Board 4 logic drawing D-1035-01.

10.11.3 This logic compares the cylinder address contained in the formatter Cylinder Address Register with a maximum cylinder value specified by the user via staples or ROM's at component locations E12 & F12.

10.11.4 Any time that the contents of the Cylinder Address Register is larger than the user defined maximum value, a Non-Existent Cylinder Error will be generated and cause any transfer operation to be aborted.

10.11.5 Normal Maximum Cylinder Selection

Normal maximum cylinder address selection is accomplished by connecting or not connecting pins 1-7 of location E12 and pins 1 & 2 of location F12 to ground as appropriate to select the desired maximum cylinder value.

10.11.5.1 The interconnections shown on the logic drawings select a maximum cylinder value of 823 appropriate to a CDC 9762 80 MB Disk Drive.

10.11.5.2 Table 8 shows the binary weight of each control pin involved in maximum cylinder selection.

Table 8

Maximum Cylinder Control Pins

<u>Board 4 Control Location &amp; Pin</u>	<u>Cylinder Select Binary Weight</u>
E12-01	1
E12-02	2
E12-03	4
E12-04	8
E12-05	16
E12-06	32
E12-07	64
E12-09	128
F12-01	256
F12-02	512

- Note: 1.) For a logic 1, leave pin open.  
2.) For a logic 0, tie pin to ground at pin 08, or 15 of component location.  
3.) The maximum cylinder value selected is equal to the sum of all logic "1" or open select pins plus 1.

10.12 External -5VDC Supply Option Selection (Reference CDC Board 4 Logic Drawing D-1035-01 Sheet 1 (top center of page) and Assembly Drawing D-1035-03.

The Phoenix 200 Formatter requires -5VDC power as bias voltage for the differential drivers and receivers used to interface with the CDC disk drives.

The -5VDC is normally generated from -15VDC by a 7905 power regulator as shown on the logic diagram. Provision is made to enable the user to supply the -5VDC voltage directly from an external source by removing the supplied 7905 regulator and inserting staple W36.

- Note: 1.) Staple W36 is a vertical staple just to the right of and below SIP component RP131 just above the "A" connector of Board 4.  
2.) If the user chooses this option, -5VDC can be brought into the formatter via any unused pin on the power harness to backplane pin AN2.

10.13 Maintenance Error Abort Inhibit Option Selection (Reference Board 3 Logic Drawing Sheet 4 (top center of page) and Assembly Drawing D-1034-03.

- 10.13.1 For maintenance fault isolation purposes it may be desirable to temporarily inhibit the formatter from aborting any commanded operation at the detection of any error condition.

- 10.13.2 This maintenance only mode of operation can be entered by removing staple W9 on Board 3.
- 10.13.3 Staple W9 is etched diagonally onto the printed circuit board immediately above and to the left of component G8.

Warning!!

If staple W9 is temporarily removed for maintenance purposes, it must be replaced before putting the formatter back into normal service.

10.14 Maintenance Mode Data Complementation Option Selection (Reference CDC Board 4 Logic Drawing D-1035-01 Sheet 4 (top center) and Assembly Drawing D-1035-03)

- 10.14.1 In Maintenance Mode the contents of the 32 bit header are used to determine the validity of all internal data paths back to computer memory.

The data words determined by the contents of the header words are used as received disk data and transmitted to the host computer via normal means.

- 10.14.2 By varying the contents of the Cylinder and Unit, Sector Head Registers, varying data patterns may be used to thoroughly exercise all formatter logic and data paths.
- 10.14.3 Staples W27 and W28 determine whether or not the header data will be continuously used as "data" for the number of words to be read as determined by the commanded transfer block length, or whether the data will be complemented every other transmission.
- 10.14.4 If staple W27 is in place, the contents of the header words will be used continuously as data words and the pattern will repeat every two words.

Note: Staple W27 is a vertical run etched onto the printed circuit board immediately above decoupling capacitor C85.

- 10.14.5 If staple W28 is in place, the header words will be complemented after each two words resulting in a four word repeating data pattern.

Note: 1.) The staple W28 common point is immediately above decoupling capacitor C85 and the other point is diagonally to the left at the same height as staple W27 connection point.

2.) Staple W27, which is etched onto board, must be cut is staple W28 option is to be selected.



10.15 Header Format Staple Selection (Reference Sheet 4 of CDC Board 4 Logic Drawing D-1035-01, Sheet 4 (right hand side) and CDC Board 4 Assembly Drawing D-1035-03)

10.15.1 The Phoenix 200 Disk Dormatter utilizes two basic header formats, one for the Control Data Corporation family of disk drives and one for Calcomp Disk Drives.

10.15.2 Header Cylinder Format Staple Selection

The 32 bit Header Shift Register and associated staples are shown on the lower right side of Sheet 4 of Logic Drawing D-1035-01.

Note: The logic drawing shows the proper staples for the normal Control Data Corporation disk drive family. Table 9 below shows the required staples for both Control Data Corporation and Calcomp Disk Drives.

10.15.3 Header Cylinder Comparison Enable Count Selection

A 4 stage counter at location A2 of Board 4 is used to determine when the Cylinder Bits of the header are to be compared with the current contents of the Cylinder Register during the position verification cycle performed by the formatter at the beginning of each sector.

This logic and associated control staples are shown at the upper center of Sheet 4 of CDC Board 4 logic drawing D-1035-01.

Table 9

Header Format Cylinder Staple Selection

(Reference D-1035-01 Sheet 4, D-1035-03)

<u>Staple #</u>	<u>CDC Configuration</u>	<u>Optional Configuration</u>	<u>Staple Location</u>
W7	OUT	IN	E9
W8	IN	OUT	E9
W9	OUT	IN	E9
W10	IN	OUT	E9
W11	OUT	IN	E9
W12	IN	OUT	E9
W13	OUT	IN	E10
W14	IN	OUT	E10
W15	OUT	IN	E9
W16	IN	OUT	E9
W17	OUT	IN	E9
W18	IN	OUT	E9
W19	IN	OUT	E10
W20	OUT	IN	E10
W21	IN	OUT	E10
W22	OUT	IN	E10
W23	IN	OUT	E10
W24	OUT	IN	E10
W25	IN	OUT	E10
W26	OUT	IN	E10

Note: All staples required for normal CDC configuration are etched on board and must be cut if header format is to change.

- 10.15.3.1 When the board is configured normally for CDC disk drives, the counter is prebiased with a count of 0, enabling the cylinder comparison to begin during the second header word,
- 10.15.3.2 When the board is configured for Calcomp Disk Drive emulation, the counter is prebiased with a count of 148 enabling the cylinder comparison to begin at the beginning of bit 13 of the first header word.
- 10.15.3.3 The logic drawing shows proper staple selection for the normal CDC disk drive configuration. Table 10 below shows proper staple selection for both CDC and Calcomp Disk Drive configurations.

Table 10

Header Cylinder Comparison Enable Count Selection

(Reference D-1035-01 Sheet 4, D-1035-03)

<u>Staple #</u>	<u>CDC Configuration</u>	<u>Calcomp Configuration</u>	<u>Staple Location</u>
W29	IN	IN	Immed.Below A2
W30	IN	IN	Immed.Below A2
W31	IN	OUT	Immed.Below A2
W32	IN	OUT	Immed.Below A2

10.16 FIFO Memory Storage Capacity Selection (Reference Board 2 Logic Drawing D-1033-01, Sheet 5 and Assembly Drawing D-1033-03)

- 10.16.1 The Phoenix 200 Formatter may be equipped with 128, 256, or 512 words of FIFO memory. Standard memory factory FIFO capacity is 128 words.
- 10.16.2 The formatter FIFO storage is provided by two physical memory banks, each of which contains half of the storage provided.
- 10.16.3 The memory banks are alternately accessed to half the access time of one equivalent memory bank.
- 10.16.4 Both memory banks are shown on Sheet 5 of the logic drawing wired for a full 256 word storage capacity each.
- 10.16.5 In actual practice the FIFO memory banks are depopulated when less than 512 words of storage are to be utilized, and jumper wires are added from the data outputs of last used memory elements to the output of pin of the last corresponding memory element location in the matrix.

10.16.6 Table 11 shows the components required for 128 and 256 memory storage capacity options while Table 12 shows the required jumper wires for these capacities.

Caution: The FIFO Request Delay Selection Logic must also be changed anytime that the FIFO memory capacity is changed. See Section 10.17.

Table 11

FIFO Memory Elements Required for 128 AND 256 Word Capacities

(Reference Board 2 Logic Drawing D-1033-01 Sheet 5 and  
Assembly Drawing D-1033-03)

1.) Memory Elements Required for 128 Word Storage Capacity

Memory Bank 0

U87  
U98  
U109  
U121

Memory Bank 1

U92  
U103  
U114  
U126

2.) Memory Elements Required For 256 Word Storage Capacity

Memory Bank 0

U87, U88  
U98, U99  
U109, U110  
U121, U122

Memory Bank 1

U92, U93  
U103, U104  
U114, U115  
U126, U127

Note: The basis memory element is a 64 x 4 FIFO MOS memory device.

Table 12

Jumper Wire Connections Required for 128 & 256 Word Memories

(Reference Board 2 Logic Drawing D-1033-01 Sheet 5 and  
Assembly Drawing D-1033-03)

Memory Bank 0 Required Jumpers

<u>Data Bit Number</u>	<u>128 Word Origin Point</u>	<u>256 Word Origin Point</u>	<u>Destination Point</u>
0	U122-04	U123-04	U124-13
1	U122-05	U123-05	U124-12
2	U122-06	U123-06	U124-11
3	U122-07	U123-07	U124-10
R(0-3)	U122-03	U123-03	U124-14
SO(0-3)	U122-02	U123-02	U124-15
4	U110-04	U111-04	U112-13
5	U110-05	U111-05	U112-12
6	U110-06	U111-06	U112-11
7	U110-07	U111-07	U112-10
R(4-7)	U110-03	U111-03	U112-14
SO(4-7)	U110-02	U111-02	U112-15
8	U99-04	U100-04	U101-13
9	U99-05	U100-05	U101-12
10	U99-06	U100-06	U101-11
11	U99-07	U100-07	U101-10
R(8-11)	U99-03	U100-03	U101-14
SO(8-11)	U99-02	U100-02	U101-15
12	U88-04	U89-04	U90-13
13	U88-05	U89-05	U90-12
14	U88-06	U89-06	U90-11
15	U88-07	U89-07	U90-10
R(12-15)	U88-03	U89-03	U90-14
SO(12-15)	U88-02	U89-02	U90-15

Memory Bank 1 Required Jumpers

<u>Data Bit Number</u>	<u>128 Word Origin Point</u>	<u>256 Word Origin Point</u>	<u>Destination Point</u>
0	U127-04	U128-04	U129-13
1	U127-05	U128-05	U129-12
2	U127-06	U128-06	U129-11
3	U127-07	U128-07	U129-10
R(0-3)	U127-03	U128-03	U129-14
SO(0-3)	U127-02	U128-02	U129-15
4	U115-04	U116-04	U117-13
5	U115-05	U116-05	U117-12
6	U115-06	U116-06	U117-11
7	U115-07	U116-07	U117-10
R(4-7)	U115-03	U116-03	U117-14
SO(4-7)	U115-02	U116-02	U117-15
8	U104-04	U105-04	U106-13
9	U104-05	U105-05	U106-12

Table 12

Memory Bank 1 Required Jumpers (Cont'd)

<u>Data Bit Number</u>	<u>128 Word Origin Point</u>	<u>256 Word Origin Point</u>	<u>Destination Point</u>
10	U104-06	U105-06	U106-11
11	U104-07	U105-07	U106-10
R(8-11)	U104-03	U105-03	U106-14
SO(8-11)	U104-02	U105-02	U106-15
12	U93-04	U94-04	U95-13
13	U93-05	U94-05	U95-12
14	U93-06	U94-06	U95-11
15	U93-07	U94-07	U95-10
R(12-15)	U93-03	U94-03	U95-14
SO(12-15)	U93-02	U94-02	U95-15

10.17 FIFO Memory Request Delay Selection (Reference Board 2 Logic Drawing D-1033-01, Sheet 4 (bottom right hand corner and Assembly Drawing D-1033-03)

- 10.17.1 When a word is entered into the FIFO memories contained in the formatter the data word has to "fall through" all 64XN locations of the memory before it can be accessed and retrieved from the memory.
- 10.17.2 The amount of time to "fall through" the memory elements is a direct function of how large the memory is and how many FIFO elements the data has to serially fall through.
- 10.17.3 When a data word is entered into a FIFO memory, no formatter action can be taken on such word until the word is available for access after fall through time has elapsed.
- 10.17.4 All requests for formatter direct memory access based upon FIFO data word entry are delayed by a time equal to the data FIFO memory "fall through: time by the logic shown on Sheet 4 prior to being used by the formatter.
- 10.17.5 This is accomplished by entering a bit into the delay logic when data is entered into or retrieved from the FIFO memory. This bit is then shifted through the required number of stages at a known clock frequency. When the delayed request signal appears at the selected output point of the delay logic, it can be safely used to cause a DMA transfer operation to load or access the FIFO memory.
- 10.17.6 Staples W44, W45, and W46 adjust the request delay to 128, 256 or 512 word memory capacities respectively and only one of these staples must be inserted at any one time. Table 13 shows the staple locations as well as the associated memory capacities.

Table 13

FIFO Memory "Fall Through" Request Delay Selection

(Reference Board 2 Logic Drawing D-1033-01  
Sheet 2 and Assembly Drawing D-1033-03)

<u>FIFO Memory Capacity</u>	<u>Staple Required</u>	<u>Staple Location</u>
128	W44	Immed.Below A1-06
256	W45	Immed.Below A1-07
512	W46	Immed.Below A1-08

Note: W44 is etched onto the etch side of the printed circuit board and must be cut if W45 or W46 are to be inserted.

- 10.18 Pack Change Seek Interrupt Selection (Reference Board 2 Logic Drawing D-1033-01 Sheet 3 (bottom left of page) and Assembly Drawing D-1033-03)
- 10.18.1 Whenever a disk drive is powered down and then up by an operator the transition is detected by the disk controller and the "Pack Change" Status bit is set in the Disk Status Register.
- 10.18.2 If staple W28 is inserted in board 2 of the formatter the transition can also generate a Seek Done Interrupt to flag the host computer of the occurrence of the change in the disk drive status.
- 10.18.3 The Pack Change Interrupt is normally not enabled at the factory (W28 is removed)
- 10.18.4 Staple W28 connection points are immediately below and to the left and right of U50-01 and U50-02 respectively.

## 10.19 Optional Data Port Interface Selection

### 10.19.1 General

The data bus of the Phoenix 200 Formatter may be uniquely isolated from the control bus via staples. This permits the user to utilize his computer to control and initiate data transfers between the selected disk drive(s) and user external equipment physically connected to the Optional Data Port Connector located on Board 2 of the formatter.

The following paragraphs of this section are devoted to defining all of the staple changes required to put the formatter in the Optional Data Port Configuration.

### 10.19.2 Required Data Bus Modifications (Reference Board 2 Logic Drawing D-1033-01 Sheet 1 and Assembly Drawing D-1033-03)

#### 10.19.2.1 Data Bus Transceiver Insertion

- 10.19.2.1.1 The Optional Data Port Interface Logic is shown on the extreme right of Sheet 1 and is comprised of components U130, U118, U107 and U96.
- 10.19.2.1.2 The transceiver receiver outputs (DØH-D15H) are hard-wired to the input of the 2=1 data multiplexer and latch shown on the extreme left of Sheet 1.
- 10.19.2.1.3 DMA write data and disk read data are multiplexed and latched by the 74298's shown on extreme left of Sheet 1 prior to being written into one of the two formatter FIFO memories.
- 10.19.2.1.4 To prevent noise from entering the formatter through the unused transceivers in normal formatter configurations, the transceivers U130, U118, U107 and U96 are not normally provided.
- 10.19.2.1.4 Transceivers U130, U118, U107 and U96 must be physically inserted into board 2 of the formatter for the Optional Data Port Configuration.

#### 10.19.2.2 Isolation of Control Bus and Optional Data Port Input Buses

- 10.19.2.2.1 With the Optional Data Port Transceivers in place, incoming data from the Optional Data Port Interface and host computer are both connected to same input of the data multiplexer and latch shown on the extrmem left of sheet 1.
- 10.19.2.2.2 To isolate the incoming computer and Optional Data Port data, staples W12-W27 must be removed.

Note: 1.) All of these staples are etched onto the printed circuit board and must be carefully cut with an XACTO knife.

- 2.) Staples W14, W15 and W16 are horizontal staples located immediately below U86.
- 3.) All other staples (W17-W27) are physically located immediately below U120. (Staples run vertically in two rows.)

10.19.2.2.3 Isolation of Outgoing Data from Internal Bus

- 10.19.2.2.3.1 To prevent data being sent to the Optional Data Port Interface (during any Read operation) from being gated onto the internal formatter bus staple W5 must be removed.
- 10.19.2.2.3.2 Staple W5 is etched onto the printed circuit board and must be carefully cut.
- 10.19.2.2.3.3 Staple W5 is the second vertical staple from the left of the lower row of staples occupying area directly above U65-15.

10.19.2.2.4 Gating of Data Onto Optional Data Port Interface

- 10.19.2.2.4.1 In order to enable the DMRDSTBL Signal from the Optional Data Port to enable data to be gated onto the Optional Data Port Interface, two staples must be removed and two more must be added as follows.
- 10.19.2.2.4.2 Staple Removals

<u>Staple Number</u>	<u>Location</u>
W6	Vertical staple above U65-16
W9	Vertical staple below U66-02

Note: W6 and W9 are etched onto the printed circuit board and must be cut carefully.

10.19.2.2.4.3 Staple Additions

<u>Staple Number</u>	<u>Location</u>
W7	Vertical staple above U65-13
W8	Vertical staple above U65-14

10.19.2.2.5 Clocking of Optional Data Port Data into Formatter Latch

- 10.19.2.2.5.1 Optional Data Port Interface data during Write operations is strobed into the 74298 latches prior to being written into one of the two formatter FIFO memories.
- 10.19.2.2.5.2 In order to allow the Optional Data Port DMLDSTB Signal to clock the data into the latches, staple W10 must be removed and staple W11 must be inserted.
- 10.19.2.2.5.3 Staple W10 is etched onto the printed circuit board and is located below U47. This staple runs horizontally below U47-05 to U47-07.



- 10.19.2.2.5.4 Staple W11 is located below U47 and is to run horizontally from connection points approximately at U47-01 and U47-03.
- 10.19.2.2.6 Gating of Optional Data Port DMACK Signal to DMA Request Logic (Reference Board 2 Logic Drawing D-1033-01 Sheet 4 (top center of sheet) and Assembly Drawing D-1033-03)
- 10.19.2.2.6.1 The Optional Data Port Interface Signal DMACK must be gated into the formatter DMA Request Logic shown on Sheet 4 in lieu of the normal computer supplied DMA acknowledge signal.
- 10.19.2.2.6.2 This is accomplished by removing staple W39 and inserting staple W38.
- 10.19.2.2.6.3 Staple W39 is a horizontal staple located below U60 and running approximately from U60-07.
- 10.19.2.2.6.4 Staple W38 should be located immediately to the left of the original W39 staple.
- 10.19.2.2.7 Gating of Optional Data Port Overflow Signal  
(Reference Board 2 Logic Drawing D-1033-01, sheet 4 (left center of sheet) and Assembly Drawing D-1033-03)
- 10.19.2.2.7.1 The Optional Data Port Word Count Overflow Signal WCROVFL is enabled for internal formatter use by inserting staple W37 into Board 2.
- 10.19.2.2.7.2 Staple W37 is vertically installed between points immediately to the left of U119.
- 10.19.2.2.8 Disabling of Normal DMA Word Count Overflow Signal  
(Reference Board 1 Logic Drawing D1032-01, Sheet 1 and Assembly Drawing D1032-04)
- 10.19.2.2.8.1 The normal DMA Word Count Register Overflow Signal (WCROVH) generated on the Phoenix 211 Interface Board must be disabled when using the Optional Data Port Interface, since it is to be supplied by user external equipment.
- 10.19.2.2.8.2 This is accomplished by physically removing staple W1 shown on the top center of sheet 1 of Board 1 Logic Drawing D1032-01.
- 10.19.2.2.8.3 (Reference Board 1 Assembly Drawing D1032-04) Staple W1 is a vertical staple etched onto the printed circuit board on the component side, immediately to the left of component F9 and must be carefully cut.

- 10.19.2.2.9 Disabling of Normal DMA DMDATIL Signal (Reference Board 1 Logic Drawing D1032-01, Sheet 1 and Assembly Drawing D1032-04).
- 10.19.2.2.9.1 The normal DMA Input Data Signal (DMDATIL) generated on the Phoenix 211 Interface Board must be disabled when using the Optional Data Port Interface.
- 10.19.2.2.9.2 This is accomplished by physically removing staple W2 shown on the center of Sheet 1 of Board 1 Logic Drawing D1032-01.
- 10.19.2.2.9.3 (Reference Board 1 Assembly Drawing D1032-04) Staple W2 is horizontal staple located immediately below and connected to pin 4 of component G8.
- 10.19.2.2.10 Disabling of Formatter DMA Request Signal (DMRL) To 211 Interface Board, (Reference Board 1 Logic Drawing D1032-01, Sheet 1 and Assembly Drawing D1032-04)
- 10.19.2.2.10.1 The normal DMA Request Signal generated by the formatter (DMRL) must be inhibited from making DMA requests to the Phoenix 211 Interface Board when the Optional Data Port Interface is used.
- 10.19.2.2.10.2 This is physically accomplished by removing staple W3 shown on the top right side of sheet 1 of Board 1 Logic Drawing D1032-01.
- 10.19.2.2.10.3 (Reference Board 1 Assembly Drawing D1032-04) Staple W3 is a horizontal staple physically etched onto the etch side of the printed circuit board, immediately above and connected to pin 5 of mini component J8B. (left most mini dip at location J8). The staple can be readily removed by carefully cutting the etch on the component side of the board connecting J8B-04 to the feed through pad immediately above J8B-04.
- 10.19.2.2.11 Disabling of Formatter DMA Directional Signal (DMDIRL) to 211 Interface Board (Reference Board 1 Logic Drawing D1032-01 Sheet 1 and Assembly Drawing D1032-04)
- 10.19.2.2.11.1 The normal DMA Direction Definition Signal (DMDIRL) generated by the formatter to the 211 Interface Board must be disabled when the Optional Data Port Interface is used.
- 10.19.2.2.11.2 This is physically accomplished by cutting the etch connecting the DMDIR driver output to the associated 01 connector pin as shown on the top of sheet 1 of Board 1 Logic Drawing D1032-01.
- 10.19.2.2.11.3 (Reference Board 1 Assembly Drawing D1032-04) The etch should be carefully cut on the component side of the printed circuit board immediately above Pin 5 of mini component J8A. (rightmost mini dip at location J8)

- 10.19.2.2.12 Disabling of Formatter Data Onto Data Bus to 211 Interface Board (Reference Board 1 Logic Drawing D1032-01, Sheet 1 and Assembly Drawing D1032-04)
- 10.19.2.2.12.1 The formatter must be inhibited from putting DMA data onto the data bus to the 211 Interface Board when the Optional Data Port Interface is used.
- 10.19.2.2.12.2 This is physically accomplished by cutting the etch connecting the DMDATIL bus gating signal to Pin 1 of the bus control gate E2 as shown on the bottom left of Sheet 1 of Logic Drawing D1032-01, and then adding a jumper wire connecting E2-01 to E2-02.
- 10.19.2.2.12.3 (Reference Board 1 Assembly Drawing D1032-04) The etch should be carefully cut on the etch side of the printed circuit board at Pin 1 of E2. A jumper wire should then be added on the etch side of the board connecting E2-01 to E2-02.
- 10.19.2.2.13 Termination Removal When Autoswitch Board Used (Reference Board 1 Logic Drawing D1032-01, Sheet 1 and Assembly Drawing D1032-04)
- 10.19.2.2.13.1 When the Autoswitch Board is used in conjunction with the Optional Data Port Interface the 211 Interface Board is physically connected to both Board 1 of the formatter and the Computer Port Connector of the Autoswitch.
- 10.19.2.2.13.2 To facilitate checkout of all ports of the Autoswitch, the normal termination resistors shown for the J1 211 Interface connector Board 1, on Sheet 1 Logic Drawings are physically removed from Board 1.
- 10.19.2.2.13.3 In this configuration the Autoswitch provides the proper termination for the 211 Interface Signals.
- 10.20 Abort Inhibit on Cylinder Header Error Parameter Selection(Reference Board 1 Logic Drawing D1032-01, Sheet 2 and Assembly Drawing D1032-04)
- 10.20 The Phoenix 211 Disk Controller will normally abort any operation in process upon detection of any error condition.
- 10.20.1 The user may optionally prevent the disk controller from aborting any operation in process whenever a cylinder header error is detected by removing staple W33, as shown on right center of Sheet 2 of Board 1 Logic Drawing D1032-01.
- 10.20.2 (Reference Board 1 Assembly Drawing D1032-04) Staple W33 is a horizontally oriented staple permanently etched onto the etch side of the printed circuit board, immediately below and connected to Pin 5 of component C3.
- 10.20.3 Staple W33 should be removed by carefully cutting the run on the etch side of the printed circuit board connecting C3-05 to the feed thru pad beneath C3-07.

10.21 Abort Inhibit on Sector Header Error Parameter Selection  
(Reference Board 1 Logic Drawing D1032-01, Sheet 2, and  
Assembly Drawing D1032-04)

- 10.21.1 The user may optionally prevent the disk controller from aborting any operation in process whenever a Sector Header Error is detected.
- 10.21.1 This is accomplished by physically removing staple W20 as shown on the bottom center of Sheet 2 of Logic Drawing D1032-01.
- 10.21.3 (Reference Board 1 Assembly Drawing D1032-04) Staple W20 is a vertical staple on the component side of the printed circuit board connecting Pin 5 of component D3 to the feed thru located immediately below D3-05, and should be carefully cut.

10.22 Abort Inhibit on CRC Error Parameter Selection (Reference Board 1  
Logic Drawing D1032-01, Sheet 2 and Assembly Drawing D1032-04)

- 10.22.1 The user may optionally prevent the disk controller from aborting any operation in process whenever a CRC Error is detected.
- 10.22.2 This is accomplished by removing staple W32 as shown on lower right center of Sheet 2 of Board 1 Logic Drawing D1032-01.
- 10.22.3 (Reference Board 1 Assembly Drawing D1032-04) Staple W32 is a permanently etched staple on the etch side of the printed circuit board connected to Pin 2 of C3 and running horizontally to the left of and below C3 to a point below and to the left of C3-01.

This staple should be removed by carefully cutting the run on the etch side of the printed circuit board.

10.23 Abort Inhibit On Sector Write Protect Error Parameter Selection  
(Reference Board 1 Logic Drawing D1032-01 Sheet 2 and Assembly  
Drawing D1032-04)

- 10.23.1 The user may optionally prevent the disk controller from aborting any operation in process whenever a Sector Write Protect Error is detected.
- 10.23.2 This is accomplished by physically removing Staple W31 as shown on the lower right center of Sheet 2 of Board 1 Logic Drawing D1032-01.
- 10.23.3 (Reference Board 1 Assembly Drawing D1032-04) Staple W31 is permanently etched onto the etch side of the printed circuit board and runs horizontally to connect feed thru pads located directly above C3-11 and C3-09.

The run should be carefully cut on the etch side of the printed circuit board.

10.24 Abort Inhibit on Data Late Error Parameter Selection (Reference Board 1 Logic Drawing D1032-01 Sheet 2, and Assembly Drawing D1032-04)

10.24.1 The user may optionally prevent the disk controller from aborting any operation in process whenever a Data Late Error is detected.

10.24.2 This is accomplished by physically removing staple W30 as shown on the lower right center of Sheet 2 of Board 1 Logic Drawing D1032-01.

10.24.3 (Reference Board 1 Assembly Drawing D1032-04) Staple W30 is permanently etched onto the etch side of the printed circuit board and runs horizontally to connect feed thru pads located directly above B3-14 and B3-12.

The run should be carefully cut on the etch side of the printed circuit board.

PHOENIX 211 9-SLOT SYSTEMS UNIT BOARD PLACEMENT CHART

SLOT  
NO.

	A	B	C	D	E	F
1.	UNIBUS IN		SPC SLOT (QUAD)			
2.	-----					
3.	SPC SLOT (HEX)					
4.	-----					
5.	UNIBUS OUT OR TERMINATOR		SPC SLOT (QUAD)			
6.	PHOENIX 211 BOARD NO. 1					
7.	PHOENIX 211 BOARD NO. 2					
8.	PHOENIX 211 BOARD NO. 3					
9.	PHOENIX 211 BOARD NO. 4					

PHOENIX 9-SLOT CHASSIS  
LEFT SIDE VIEW

\* NPR GRANT JUMPER IS REMOVED FROM THIS SLOT (CA1 → CB1)

CONNECTOR A

PIN	NAME	SOURCE BOARD-SHEET	DEST.	PIN	NAME	SOURCE BOARD-SHEET	DEST.
A1	NOT USED			A2	+5		
B1	"			B2	-15		
C1	"			C2	GND		
D1	"			D2	ACLO	BACKPLANE PC	4
E1	"			E2	NOSIPH	UREF 2-3	3
F1	"			F2	DRVONH	4-5	
H1	"			H2	RUESRL	1-1	1
J1	"			J2	NOT USED		
K1	"			K2	"		
L1	"			L2	"		
M1	"			M2	"		
N1	GOSEEKL	4-1	2	N2	-5	4-1	
P1	PORTREQL	3-2		P2	EOSH	3-3	1,3,4
R1	NOT USED			R2	PORTREL	3-2	4
S1	"			S2	WCKERR(Ø)	2-2	1
T1	GND			T2	NOT USED		
U1	NOT USED			U2	"		
V1	"			V2	"		

## CONNECTOR B

PIN	NAME	SOURCE		PIN	NAME	SOURCE	
		BOARD-SHEET	DEST.			BOARD-SHEET	DEST.
A1	ROMTAG 3	3-3	4	A2	+5		
B1	HSHDRH	4-4	3	B2	-15		
C1	IHBSEEKL	3-2	4	C2	GND		
D1	SPARE			D2	SEEKACKH	4-1	3
E1	SPARE			E2	GODLYH	1-2	2,3,4
F1	WORDL	3-4		F2	CLOCKH	1-2	2
H1	SET SEKH	3-4	2	H2	WCROVEØ	3-4	
J1	WCROVEH	(2-4) (1-1)		J2	FFORH	2-1	2
K1	SWPEP (1)	3-1	1	K2	CRCDATOUTH	3-1	2
L1	BAD SECT H	3-1	1	L2	CRC ERR(1)	3-1	1,3
M1	THEADERR(1)	3-1	1	M2	SHEADERR(1)	3-1	1
N1	GENERRORL	1-2	3	N2	ENBDMRH	3-4	1,2
P1	SYSCLEARL	3-2	1	P2	DATAOUTL	2-2 4-2	3
R1	SEEKENDØH	4-2	2	R2	PUNSELØH	4-1	2,4
S1	SEEKENDLH	4-2	2	S2	PUNSEL1H		2,4
T1	GND			T2	NONSTRIPH	3-2	1
U1	WGH	3-3	2,3,4	U2	WRCHKH	3-2	
V1	RDGATEH	3-3	2,3,4	V2	SPARE		



## CONNECTOR C

PIN	NAME	SOURCE		PIN	NAME	SOURCE	
		BOARD-SHEET	DEST.			BOARD-SHEET	DEST.
A1	ONCYH	4-1	1,3	A2	+5		
B1	BUSY (Ø)	3-4	1	B2	-15		
C1	MAXHEAD	3-5	1,4	C2	GND		
D1	DATAH	3-3	2,3	D2	SERVOMH	1-2	3,4
E1	WCOGH	3-3	2	E2	SERVOPH	1-2	3,4
F1	WSBH	3-3	2,3	F2	DSEH	1-2	4
H1	LASECCOMP	4-3	2	H2	DSLH	1-2	4
J1	DONE (1)	3-4	1,3	J2	SECPLSI	4-4	4
K1	QUNABLE (1)	1-5	1,3	K2	DATLATE	2-4	1
L1	FLICLRLL	3-2	4	L2	DMREQH	2-4	1,2
M1	RTZL	3-2	3,4	M2	QSEKINGL	2-3	1
N1	DMDATOH	1-1	2	N2	QSKDONEH	2-3	1
P1	RDDONE (1)	3-4	3	P2	SEKINTRL	2-3	1
R1	INTACKH	1-1		R2	LQSCANZH	1-5	2
S1	CARRYH	3-4	2	S2	LQSCANLH	1-5	2
T1	GND			T2	INCHDL	3-5	3,4
U1	SPARE			U2	LDUSHRL	1-1	3,4
V1	SEEKL	3-2	1,3,4	V2	DATAOUTH	2-2	4

## CONNECTOR D

PIN	NAME	SOURCE		PIN	NAME	SOURCE	
		BOARD-SHEET	DEST.			BOARD-SHEET	DEST.
A1	RDCLKH	4-5	3	A2	+5		
B1	RDDATAH	4-5	3	B2	-15		
C1	WRICK (H)	4-5	3	C2	GND		
D1	HDH	4-4	3	D2	GOINITL	1-2	1,2,3,4
E1	GOREL	3-2	3,4	E2	INITL	1-1	1,2,3,4
F1	READ DATAH	3-1	2,3	F2	COM0H	1-2	3
H1	READDATAH	4-5	4,3	H2	COM1H	1-2	3
J1	SECT1H	4-5	4,3	J2	COM2H	1-2	3
K1	SECT2H	4-5	4,3	K2	COM3H	1-2	3
L1	SEC3H	4-5	4,3	L2	RDCKH	3-1	2,3
M1	SECT4H	4-5	4,3	M2	UNSEL0 (1)	3-5	2,3,4
N1	SECT5H	4-5	4,3	N2	UNSEL 1 (1)	3-5	2,3,4
P1	SECT6H	4-5	4,3	P2	WRICKH	3-1	2,3
R1	HFBDH	4-4	3,4	R2	DMACKH	1-1	2
S1	IOMHZH	3-1	1,2,3	S2	READ H	3-2	1,2,3
T1	GND			T2	WRITE H	3-2	1,2,3
U1	CKINTRL CLKINIL	1-3	1,3	U2	DISRCHNGH	2-3 3-4	4
V1	ENBHDRH	3-1	4	V2	DSKXFD (1)	3-4	1 (Data Port Opt.)

## CONNECTOR E

PIN	NAME	SOURCE		PIN	NAME	SOURCE	
		BOARD-SHEET	DEST.			BOARD-SHEET	DEST.
A1	CONICKH	3-3	3,4	A2	+5		
B1	SECADD0H	3-5	4	B2	-15		2
C1	SECADD1H	3-5	3,4	C2	GND		
D1	SECADD2H	3-5	3,4	D2	SEEKEND2H	4-2	2
E1	SECADD3H	3-5	3,4	E2	SEEKEND3H	4-2	2
F1	SECADD4H	3-5	3,4	F2	LASEL0H	2-2	4
H1	SECADD5H	3-5	3,4	H2	LASEL1H	2-2	4
J1	SECADD6H	3-5	3,4	J2	ENBTAGL	3-5	1
K1	HEAD0H	3-5	4	K2	SKINBL	1-2	4
L1	HEAD1H	3-5	4	L2	DONCYLH	4-1	1
M1	HEAD2H	3-5	4	M2	FLTH	4-1	1
N1	HEAD3H	3-5	4	N2	SKEERORH	4-1	1 2
P1	HEAD4H	3-5	4	P2	RDDSRL	1-1	4
R1	MAXCYLH	4-4	1,4	R2	DMDATIL	1-1	2
S1	LDCARL	1-1	4	S2	RDCARL	1-1	
T1	GND			T2	INCTARL	3-5	3
U1	MAXSECTH	3-5	1,3	U2	LOAD HDRL	3-1	4
V1	RDUSHRL	1-1		V2	LDWCRL	1-1	1,3

CONNECTOR F

PIN	NAME	SOURCE		PIN	NAME	SOURCE	
		BOARD-SHEET	DEST.			BOARD-SHEET	DEST.
A1	IDB0H	*	1	A2	+5		
B1	IDB1H	*	1	B2	-15		
C1	IDB2H	*	1	C2	GND		
D1	IDB3H	*	1	D2	IDB10H	*	1
E1	IDB4H	*	1	E2	IDB11H	*	1
F1	IDB5H	*	1	F2	IDB12H	*	1
H1	IDB6H	*	1	H2	IDB13H	*	1
J1	IDB7H	*	1	J2	IDB14H	*	1
K1	IDB8H	*	1	K2	IDB15H	*	1
L1	IDB9H	*	1	L2	DATA 15H	1-1	2, 3, 4
M1	DATA 14-H	1-1	1, 2, 3, 4	M2	DATA 7H	1-1	2, 3, 4
N1	DATA 13H	1-1	2, 3, 4	N2	DATA 6H	1-1	1, 2, 3, 4,
P1	DATA 12H	1-1	2,3,4	P2	DATA 5H	1-1	1, 2,3,4
R1	DATA 11H	1-1	1, 2,3,4	R2	DATA 4H	1-1	1,2,3,4
S1	DATA 10H	1-1	1,2,3,4	S2	DATA 3H	1-1	1,2,3,4
T1	GND			T2	DATA 2H	1-1	1,2,3,4
U1	DATA 9H	1-1	1,2,3,4	U2	DATA 1H	1-1	1,2,3,4
V1	DATA 8H	1-1	1,2,3,4	V2	DATA 0H	1-1	1,2,3,4
* SOURCES							
	Board	Sheet					
	1	1-5					
	2	1,4					
	3	5					
	4	1,4					



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Phoenix 211 Disk Controller  
Programming Reference Manual

Dwg. No. 1043-10

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## 1.0 Introduction

The Phoenix 211 Disk Controller is a high performance, cost effective disk controller which will enable any PDP11 computer user to access up to 1.2 billion bytes of on-line storage.

The Phoenix 211 Disk Controller is a new generation disk controller employing microprocessor technology to enable improved performance at lower cost. The controller can be connected to up to four disk drives of the new "storage module" generation offered by Control Data Corp., Calcomp and other manufacturers.

Two versions of the disk controller are currently available, the standard 211 model, and the Phoenix 215 Controller with Command Queue Capability. The standard Phoenix 211 Disk Controller is used under direct user program control, while the Command Queue equipped 215 unit is controlled by a additional microprocessor which automatically queues commands for up to four disk drives and performs all of the seek overlapping and data transfer initiation functions normally performed by a user operating system.

This manual is dedicated to defining the programming interface to the standard Phoenix 211 Disk Controller in terms of the capabilities provided and how they can be best utilized.

The programming interface to the Phoenix 211 Command Queue Disk Controller is covered in a separate supplement to this manual.

## 2.0 Overview

This section presents a overview of the controller programming interface and general capabilities.

### 2.1 Program Visible Registers (Loadable and Readable)

<u>Register</u>	<u>Description</u>	<u>Standard Bus Address</u>
DCSR	CONTROL AND STATUS	164000
DUSH	UNIT, SECTOR, HEAD	164002
DCAR	BUS ADDRESS REGISTER	164004
DWCNT	WORD COUNT	164006
DCYL	CYLINDER ADDRESS	164010
DSTAT	DISK STATUS REGISTER	164012
DERR	ERROR REGISTER	164014



Note: Base Bus Register Address is Strappable

- 2.2 Standard Interrupt Vector Address Assignment : 270<sub>8</sub>-272<sub>8</sub> (Strappable)
- 2.3 Interrupt Priority: Level 5 (Strappable)
- 2.4 Number of 16 Bit Words Per Sector: 256 Standard - others available
- 2.5 Number of Sectors Per Track: 32 standard - others available
- 2.6 Disk Sector Addressing: Absolute Contiguous or optionally interlaced
- 2.7 Direct Memory Access Burst Duration ("Throttle") Control = 8 Strappable from 1 to 256 words
- 2.8 Number of Temporary Data Storage Buffers: Two
- 2.9 Temporary Data Storage Buffer Capacity: 128 words standard (Selectable to 512 in increments of 128)
- 2.10 Disk Unit Switching Time Latency: Zero\*  
\*Separate sector counter is maintained for each disk drive
- 2.11 Disk Data Transfer Initiate Latency From Seek Done Interrupt: 1200 us Max. \*\*  
\*\* Rotational position sensing is utilized. Seek done interrupt occurs when drive is on cylinder and 1200  $\mu$ sec before selected sector. (Latency time is selectable)
- 2.12 Data Transfer Length: 1 to 65,556 words  
Data transfer length controller by Word Count Register.  
Data Transfer may cross sector, surface and cylinder boundaries
- 2.13 Seek Control: Direct & implicit  
All data transfer instructions contain an implicit seek command.
- 2.14 Functional Controller Commands
  - 1. Seek
  - 2. Read
  - 3. Write
  - 4. Format
  - 5. Recalibrate
  - 6. Fault Clear

7. System Clear
8. Read Header, Data, and CRC
9. Read Data, Ignore Position Verification Check
10. Write Header, Data, CRC
11. Write Over Write Protected Sector
12. Compare Disk Data, Memory Data
13. Port Release (Dual Port Disk Drives Only)

#### 2.15 Simultaneous Seek Implementation

1. Supports true parallel simultaneous seek operations
2. Separate "seeking" and "seek done" status bits are provided for each drive.
3. Interrupt is generated at completion of seek only function.
4. Identity of disk drive terminating seek is presented to user as a word index.

#### 2.16 Position Verification Technique

1. Uses separate header preamble for each sector.
2. Header contains sector, head, and cylinder positioning data
3. Header Words are followed by a header CRC value word
4. Header preamble automatically is checked 100% before any data transfer takes place on any accessed sector.

#### 2.17 Disk Formatting Technique

1. Sector preamble header and header CRC words are generated once by Format program.
2. Once a disk pack has been formatted it is not normally formatted again for the life of the medium

#### 2.18 Data Integrity Verification Technique

1. A CRC value is computed by controller during each write operation based upon actual data content written onto each sector
2. Computed CRC value is automatically appended to the end of each sector data field by controller
3. During read operations controller automatically recomputes the CRC value based on actual data read and compares resultant value with the reference value read from the disk
4. User may alternatively perform a actual data comparison with data written on disk and reference data contained in memory using a standard controller command.

#### 2.19 Soft Error Recovery Technique

Recommended drive manufacturer's Retry Algorithm based on high resolution programmed offsets of both the head cylinder position and data strobe timing

2.20 Control Technique: Programmable special purpose microprocessor

2.21 Fault Isolation Capability

Can isolate fault to either disk drive or controller using self test mode to check integrity of the disk controller independently of the disk drive.

### 3.0 REGISTER ASSIGNMENTS -- SMD/PDP11 CONTROLLER

#### 3.1 CONTROL AND STATUS REGISTER

##### 3.1.1 FORMAT:

ERROR SUM.	SEEK IN- HIBIT	MEMORY EXTENSION	DSE	DSL	SV+	SV-	FOR- MATTER READY	INTER- RUPT ENABLE	Multi CPU Request	COMMAND	GO
15	14	13 12	11	10	9	8	7	6	5	4 3 2 1	0

##### 3.1.2 FORMAT EXPLANATION:

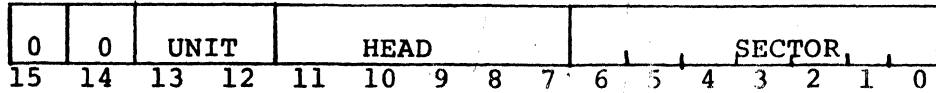
BIT	NAME	FUNCTION
0	GO (R/W)	Starts the command specified by bits 1-4. Clears Formatter Ready. The command will not start until GO is set. This bit will always read as a logic 0.
1-4	COMMAND (R/W) F <sub>0</sub> - F <sub>3</sub>	Specifies what function is to be performed per the following: Detailed definitions of each command function performed are given in section 4.0.
	F <sub>3</sub> F <sub>2</sub> F <sub>1</sub> F <sub>0</sub>	COMMAND
0	0 0 0 0	SYSTEM CLEAR
0	0 0 0 1	SEEK ONLY
0	0 0 1 0	NORMAL READ
0	0 0 1 1	NORMAL WRITE
0	0 1 0 0	FORMAT
0	0 1 0 1	READ Header, Data, and CRC Word
0	0 1 1 0	WRITE Header, Data, and CRC Word
0	0 1 1 1	READ Data, Ignoring Header Check
1	1 0 0 0	WRITE OVER WRITE PROTECTED SECTOR
1	1 0 0 1	Drive FAULT Clear
1	1 0 1 0	RECALIBRATE (RTZ)
1	1 0 1 1	Write Check Disk Data
1	1 1 0 0	Port Release
1	1 1 0 1	Read No Strip (Special Option)
1	1 1 1 0	Port Request (Calcomp Disk Drives Only)
1	1 1 1 1	NOP

CONTROL AND STATUS REGISTER EXPLANATION CONTINUED

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION</u>
5	MULTI CPU REQUEST (R/W)	This bit is used to request access to a 211 formatter equipped with the multiple cpu option. In 211's without this option this bit is always a zero.
6	INTERRUPT ENABLE (R/W)	Allows Interrupts to occur if set to a '1'.
7	FORMATTER READY (READ ONLY)	Specifies that the Controller is ready to accept a new command.
8	SV- (R/W)	Servo Offset Minus. When this bit is true the drive head is offset from the normal on cylinder position away from the spindle (Read Error Recovery).
9	SV+ (R/W)	Servo Offset Plus. When this bit is true the drive head is offset from the normal on cylinder position towards the spindle. (Read Error Recovery).
10	DSL (R/W)	Data Strobe Late. When this bit is true the disk drive will strobe data at a time later than optimum. When false, normal strobe timing will be returned. (Error Recovery).
11	DSE (R/W)	Data Strobe Early. When this bit is true the disk drive will strobe data at a time earlier than optimum. When false, normal strobe timing will be returned. (Error Recovery).
12-13	MEMORY EXTENSION (R/W)	Upper extension bits of the Buss Address Register. Set under program control or incremented when an overflow of the Bus Address Register occurs.
14	SEEK INHIBIT (R/W)	Inhibits the implied seek during a Read or Write Command.
15	ERROR SUMMARY	'OR' condition of all error conditions in the Phoenix 211 SMD Controller System.

### 3.2 UNIT-SECTOR-HEAD REGISTER 164002 \*

#### 3.2.1 Format



#### 3.2.2 Format Explanation

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION</u>
0-6	SECTOR 0-SECTOR 6 (R/W)	<ol style="list-style-type: none"> <li>1. Selects the initial sector to be written or read. (Standard format = 32 sectors/track for CDC Storage Module Disk Drives.</li> <li>2. Sector field value is incremented by controller at the end of each sector during a data transfer operation.</li> <li>3. When the last sector of a track is reached, sector counter overflows and causes incrementation of head field.</li> <li>4. A separate sector counter is maintained for each disk drive connected to the controller to minimize disk latency associated with unit switching. There is no disk latency time associated with unit switching in the Phoenix 211 Disk Controller.</li> </ol>
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">                     Typically unit switching latency is <math>\frac{1}{2}</math> revolution to allow a single sector counter to be resynchronized with the index pulse of the newly selected disk drive.                 </div>		
7-11	HEAD (R/W)	<ol style="list-style-type: none"> <li>1. Selects the initial Head (Surface) to be written or read.</li> <li>2. Is incremented once for each overflow of the sector counter.</li> <li>3. When the last surface on the current cylinder is processed, the head counter overflows and increments the Cylinder Register.</li> <li>4. Incrementation of the Cylinder Register automatically initiates a seek to the cylinder specified by the new contents of the Cylinder Register.</li> </ol>

\* Typical - See Configuration Chart for Address used in your controller

12-13 UNIT NUMBER (R/W)

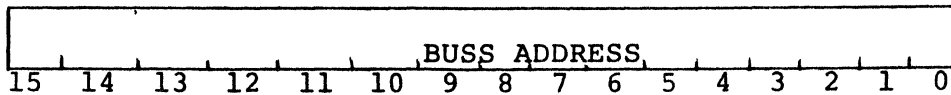
1. Selects the desired logical disk unit on which an operation is to be performed.
2. Controller can interface to a maximum of four disk drives.
3. Disk drive unit numbers can be assigned logically with the plug in elements supplied by the manufacturer with no re-cabling required.

14-15 NOT USED  
(READ ONLY)

1. Always Zeros.

### 3.3 BUSS ADDRESS REGISTER 164004

#### 3.3.1 Format

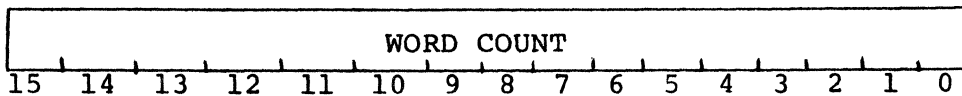


#### 3.3.2 Format Explanation

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION</u>
0-15	BA0-BA15 (READ/WRITE)	<ol style="list-style-type: none"><li>1. Loaded by the program to specify the starting memory address of a transfer. The BA register is incremented by two after each transfer of a word to or from memory.</li><li>2. Overflow of Bus Address Register increments memory extension field (Bits 12 &amp; 13) of Control and Status Register.</li></ol>

### 3.4 WORD COUNT REGISTER 164006

#### 3.4.1 Format



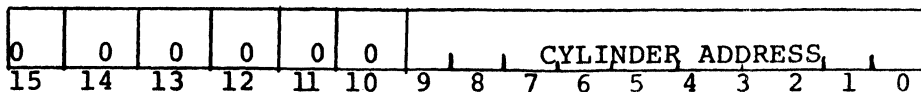
#### 3.4.2 Format Explanation

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION</u>
0-15	WCO-WC15 (READ/WRITE)	<ol style="list-style-type: none"><li>1. Set by the program to specify the number of words to be transferred in 2's complement form. The WC Register is incremented once for each word transferred to or from memory.</li></ol>

2. Overflow of Word Count Register terminates all word transfers to or from memory.

### 3.5 CYLINDER ADDRESS REGISTER 164010

#### 3.5.1 Format



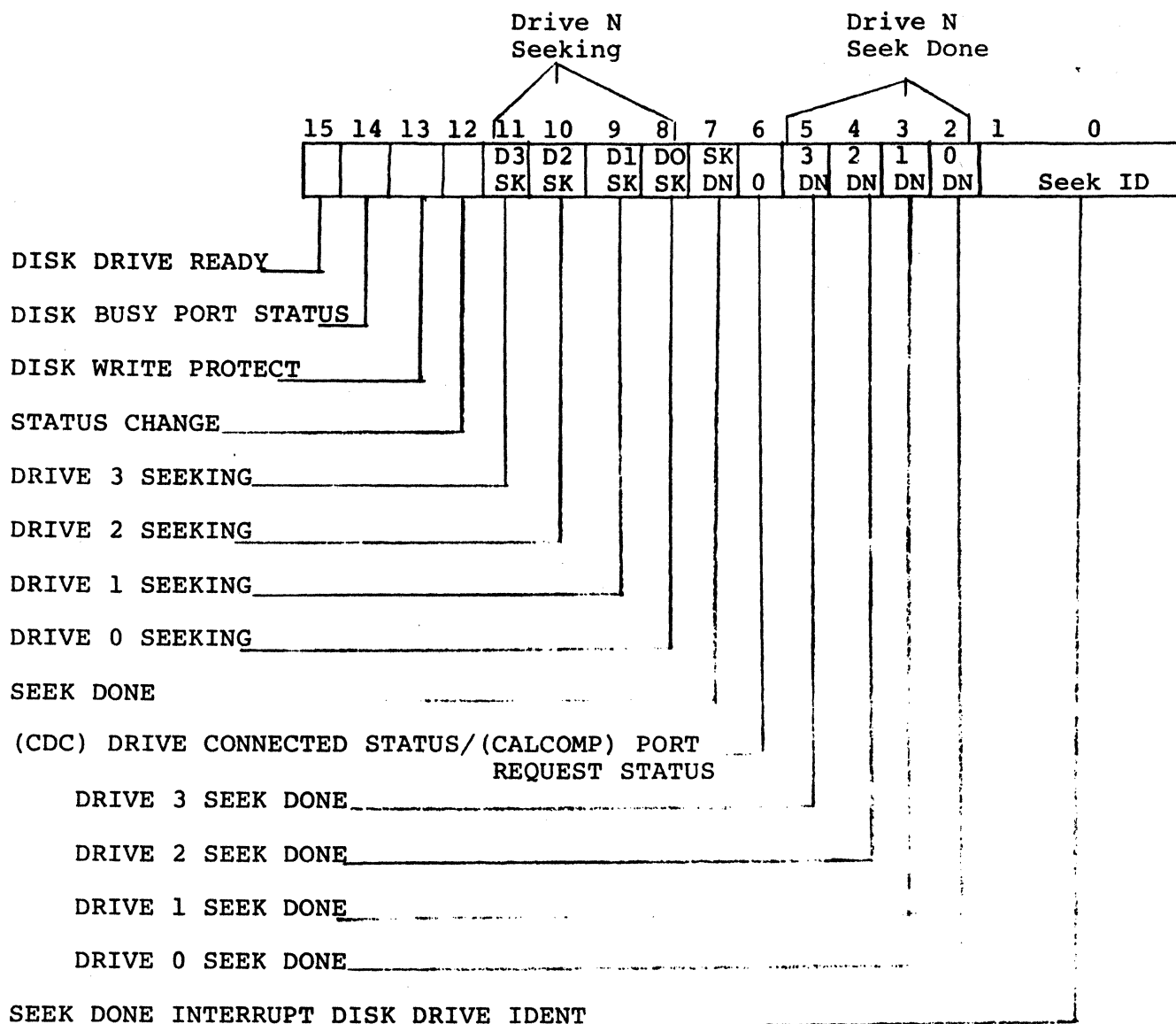
#### 3.5.2 Format Explanation

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION</u>
0-9	CA0-CA15 (READ/WRITE)	<ol style="list-style-type: none"> <li>1. Selected by the program to specify the initial cylinder on which a data transfer will take place.</li> <li>2. Is incremented by the overflow of the Head Counter.</li> <li>3. A seek is initiated at each incrementation to the cylinder specified by the new contents of the Cylinder Address Register.</li> <li>4. Incrementation of the Cylinder Address register beyond the last physical cylinder available on the disk will generate an Overrun Error and set bit 03 on the Error Register.</li> </ol>
10-15	NOT USED (READ ONLY)	<ol style="list-style-type: none"> <li>1. Always Zeros.</li> </ol>



### 3.6 DISK STATUS REGISTER 164012\* (Read Only)

#### 3.6.1 Format



#### 3.6.2 Format Explanation

BIT	NAME	FUNCTION/EXPLANATION
0-1	Seek Done Interrupt Drive Identification Field	<p>1. The contents of this field identifies the Logical disk drive generating a seek done interrupt. A seek done interrupt is generated whenever any one of the three seek done interrupt conditions occurs and the interrupt enable bit (06) of the Control and Status Register is set.</p> <p>The seek done interrupt conditions are defined in the Seek Done Interrupt Flag section.</p>

\*Typical - See Configuration Chart for Address of your controller  
10

Disk Status Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
------------	-------------	-----------------------------

2. Whenever a seek done interrupt is generated bit 07 of the Disk Status Register will be set.

Note: The Phoenix 211 Disk Controller utilizes Rotational Positioning Sensing (RPS) to maximize total system throughput. A Seek Done Interrupt is normally generated when the disk head is both on cylinder and on sector (2 sectors before specified target sector)

02-05 Seek Done Drive  
Status Bits

1. A seek done status bit is provided for each of the four disk drives serviced by the controller.
2. The seek done status bit for a given disk drive will be set whenever any one of the three seek interrupt conditions are detected by the controller for the associated disk drive.
3. When the Seek Done Status is set the corresponding Seeking Status bit for the associated disk drive is automatically reset by the controller.
4. The Seek Done status bits are mutually exclusive in that only one seek done status bit will ever be set any any one time.
5. The Seek Done status bit, once set will remain set until the associated disk drive is selected by loading the corresponding disk drive unit number into the Unit, Sector, Head Register and issuing any command to the disk controller.

CAUTION: Every Seek Done Status Bit must be serviced by clearing the associated seek done status flag per the above procedure.

No additional seek done status bits will be generated by the disk controller as long as any seek done status bit is set.

## Disk Status Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
		<p>6. <u>Rotational Position Sensing</u> The Phoenix 211 Disk Controller normally utilizes rotational position sensing to maximize total system throughput.</p> <p>In this technique both cylinder and sector head positions are combined to generate the "Seek Done" signal. A disk drive head must be both on the desired cylinder and over the "target" sector where the operation is to begin before the seek done signal and resulting interrupt are generated.</p>
		<p>7. <u>Sector Look-A-Head</u> In order to provide the programmer with ample time to set up the disk controller with parameters for the data transfer to be performed after receipt of a Seek Done Interrupt, a programmable sector look-ahead feature is incorporated to generate the on sector signal one, two, or some other predetermined number of sectors before the actual physical sector on which the transfer is to be initiated. (Standard look-ahead factory setting is 2 sectors 1200 usec.)</p>
		<p>8. <u>Rotational Position Sensing Programming Considerations</u></p> <ol style="list-style-type: none"><li>a. Rotational Position Sensing is intended for use in a multi drive system where disk latency is to be minimized by overlapping seeks under direct program control.</li><li>b. The target sector must be specified at the time that each overlapped seek is to be initiated. This requirement is satisfied by loading the Unit, Sector, Head</li></ol>

## Disk Status Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
		Register with the required parameters. (Note that the unit # was required in any case.)
		c. An analysis of operating systems overhead and system interrupt priorities is necessary in order to determine the proper look-ahead time for a given system application. Rotational Position-Sensing cannot be used effectively in any system with variable unpredictable overhead interrupt response times.
		Note: The Command Queue Option automatically performs the functions of overlapping seeks and initiating data transfer operations on the basis of rotational position sensing in order to maximize system throughput while minimizing the disk driver software burden.
		This option should be seriously considered for users with high throughput objectives and unpredictable operating systems interrupt responses.
07	Seek Done Flag	The Seek Done Flag, when set indicates that: <ol style="list-style-type: none"><li>1. A disk drive has completed a seek only or RTZ operation.</li><li>2. A disk drive has completed an unscheduled power down power up sequence. In this instance the programmer "pack change" status bit (12) of the Disk Status Register will also be set.</li><li>3. The port of the existing disk drive is now available for use. In this instance the port busy status bit (bit 14) of the Disk Status Register will be reset.</li></ol>

## Disk Status Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
------------	-------------	-----------------------------

Note that this condition is only associated with dual ported disk drives.

Note: Conditions Two and Three set bit 12, the Pack Change bit in the Disk Status Register.

Note that the Seek Done Interrupt flag may or may not be set when the controller completes a data transfer operation and generates a normal transfer operation complete interrupt.

When a disk drive completes a commanded seek only or RTZ operation:

1. The corresponding seek done drive status bit is set.
2. An interrupt is generated if the controller is not busy performing a data transfer operation.
3. The Seek Done Interrupt flag is set. If the controller is busy performing a data transfer operation when any seek operation completes:
  - a. The corresponding seek done drive status bit is set.
  - b. No seek done interrupt is generated.
  - c. One interrupt is generated at the completion of the current data transfer in process.
  - d. When this interrupt is generated the Seek Done Interrupt Flag is set indicating that a disk drive has completed a seek operation during the data transfer operation.

## Disk Status Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
		The Seek Done Interrupt Flag once set, will remain set until a new command is issued to the disk controller.
08-11	Drive Seeking Status	<p>One seeking status bit is provided for each of the four disk drives connected to the controller. This bit is set whenever the corresponding disk drive starts to execute a commanded seek only or RTZ operation.</p> <p>The bit is reset when the commanded seek only or RTZ operation has been completed and the associated disk drive seek done status bit has been set.</p>
12	Disk Status (Pack?) Change	<p>The disk Status Change bit, when set, indicates that a seek done condition has been detected on the selected drive which was <u>not</u> generated as a result of a commanded seek only or RTZ operation.</p> <p>The Status Change bit, once set, will remain set until a new command is issued to the selected drive.</p> <p>See the Seek Done Flag section for details on other Seek Done conditions.</p>
13	Disk Write Protect Status	<p>The Disk Write Protect Status Bit, when set, indicates that the selected disk drive is in a Write Protected State, as controlled by a manual switch on the front of some disk drives.</p> <p>If a drive has been so write-protected and an attempt is made to write on it, a Disk Fault Error will be generated and the write operation will be aborted by the controller.</p>

## Disk Status Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
14	Dual Port Status	<p>The Phoenix 211 Disk Controller supports the dual port option offer by some disk drive manufacturers. This bit is only applicable on systems configured with dual port disk drives. (Through this option two disk controller may "share" or access the same disk drive).</p> <p>The meaning of this bit is different dependent upon which type of disk drive is connected to the controller.</p>

### CDC Storage Module Disk Drive Interpretation

1. The Disk Port Busy Status Bit, when set indicates that another controller is currently accessing the disk drive through the other port, and that the user will have to wait until the drive is available for use, at which time, the port busy status bit will be in the reset state.
2. The bit, once set, can be reset by the execution of a "Release Command" by the controller using the other port, or by the timeout feature provided by the disk drive manufacturer.

When this bit is reset the selected disk drive is available for use by the controller.

06	Disk Drive Connected/ Port Request Status Bit	Bit 06 of the Disk Status Register has different meaning depending upon which type of disk drive is physically connected to the disk controller.
----	--	--

### CDC Storage Module Disk Drive Interpretation Disk Drive Connected

If a CDC disk drive is used with the disk controller bit 06 will be set whenever the

Disk Status Register Explanation Continued

BIT      NAME

FUNCTION/EXPLANATION

selected disk drive is physically connected to the disk controller and has power applied to it. Bit 06 will be reset if the selected drive is nonexistent or does not have power applied to it.

This status bit is provided to enable user software to determine how many disk drives are connected to the disk controller.

Calcomp Trident Disk Drive Interpretation  
Port Request Status

If Calcomp dual port disk drives are used with the disk controller bit 06 is used to indicate the status of the port request signal issued by the disk controller.

Bit 06 will be set if the Port Request Signal for the selected disk drive is currently active, and will be reset if it is not active.

Notes:

1. This status signal is applicable only to dual ported Calcomp disk drives.
2. The Port Request signal for a given disk drive is set by selecting the disk drive and issuing a Port Request Command to the Calcomp Disk Drive.
3. If the controller interrupt is enabled a Port Available interrupt will be generated when the Disk Port Busy signal is reset after having been set, to facilitate systems utilization of this drive option.

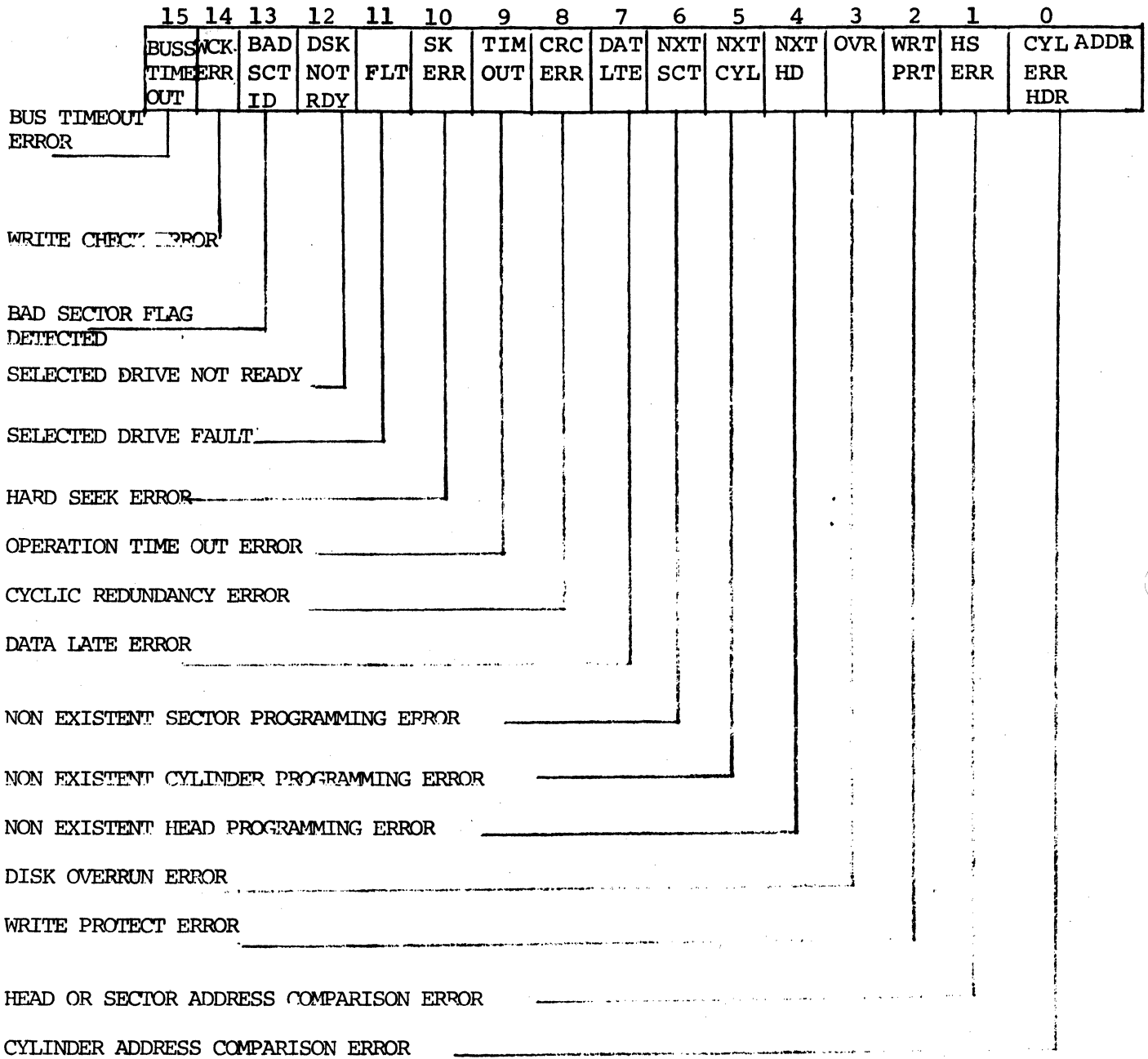
15      Disk Drive Ready

The disk drive ready bit, when set indicates that the selected disk drive is up to speed, the heads are loaded, and no fault condition exists. This bit must be set before a Seek, Recalibrate, or Data Transfer Command is issued.



3.7 ERROR REGISTER 164014\*(Read Only)

3.7.1 Format



\* Typical - See Configuration Chart for Address used in your controller

### 3.7.2 Error Register Format Explanation

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
0	Cylinder Address Comparison Error (Soft Seek Error)	<p>Set whenever the commanded cylinder address and actual cylinder address read from the sector header word in sector being accessed do not agree during position verification check performed by controller prior to performing any normal data transfer operation. Also set whenever a difference is detected between the computed header CRC value read from the disk. If such a header CRC error is detected bit 8 of the Error Register will also be set.</p> <p>Once set, it is reset when the next functional command is issued to the disk controller.</p>
01	Sector/Head Address Comparison Error (Soft Seek Error)	<p>Set whenever the commanded head and sector address and actual head and sector address read from sector header in sector being accessed do not agree during position verification check performed by controller prior to performing any normal data transfer operation.</p> <p>Once set, it is reset when the next functional command is issued to the disk controller.</p>
02	Write Protect Error	<p>Set whenever an attempt is made to write on a sector in which the write protect header bit has been set using the normal write commands. In such an instance the write operation is aborted and the protected data is not over written.</p> <p>This error bit is <u>not</u> set if a write protected sector is rewritten using the Write Protect Override Command.</p> <p>Once set, the error bit will remain set until a new functional command is issued to the controller.</p> <p>Note: Writing on a write protected disk drive does not set this error bit.</p>
03	Disk Overrun Error	<p>The Disk Overrun Error bit will be set anytime an attempt is made to utilize a cylinder larger than the physical capacity of the disk drive itself.</p> <p>Once set, the error bit will remain set until a new functional command is issued to the controller.</p>

## Error Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
		<p>The maximum number of cylinders allowed before the overrun error will be set is strappable to accomodate various disk capacities.</p>
04	Non Existent Head Error	<p>Set whenever an attempt is made to utilize a non existent head by loading the head field of the DUSH Register with a value beyond the range of the disk drives connect to the controller.</p> <p>The maximum number of allowable heads is strappable to accomodate disk drives of varying capacities.</p> <p>Once set, the error bit is cleared by issuing any functional command to the controller.</p> <p>The maximum number of allowable head is optionally physically programmed (Via ROM) for <u>each</u> physical cable port.</p>
05	Non Existent Cylinder Error	<p>Set whenever an attempt is made to utilize a non existent cylinder by loading the DCYL Register with a value beyond the physical capacity of the disk drives connected to the disk controller.</p> <p>The maximum number of allowable cylinders is strappable to facilitate disk drives of varying cylinder capacities.</p> <p>Once set, the error bit is cleared when a new functional command is issued to the controller.</p> <p>The maximum number of allowable cylinders is optionally physically programmed (Via ROM) for <u>each</u> physical cable port.</p>

## Error Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
------------	-------------	-----------------------------

06	Non Existent Sector Error
----	---------------------------

Set whenever an attempt is made to utilize a non existent sector by loading the sector field of the DUSH Register with a value beyond that of the capacity of the disk drives connected to the controller.

The maximum allowable sector value is strappable to facilitate varying sector formats.

Once set, the error bit may be cleared by issuing any functional command to the disk controller.

The maximum number of allowable sectors is optionally physically programmed (Via ROM) for each cable port.

NOTE: All nonexistent error conditions are established every time a disk controller command is executed by setting the "go" bit in the Control Status Register.

All error conditions once set, remain set until a new command or Bus INIT is generated.

07	Data Late Error
----	-----------------

This bit when set indicates that the effective direct memory access transfer rate between memory and the disk controller was less than that required to maintain proper synchronized data transfers with the disk drive.

- a. During a write operation this indicates that data transfers from memory to the controller FIFO memory buffer were not able to keep up with the rate at which data was taken from the FIFO memory to be written on the disk. The Data Late Error Bit was set when the FIFO memory was empty and another word was needed to write on the disk. At this point the operation was aborted.

## Error Register Explanation Continued

BIT

NAME

FUNCTION/EXPLANATION

CAUTION: If a "data Late" error is detected during a write operation, the operation must be repeated to preclude generation of a unreadable sector.

- b. During a read operation the presence of a Data Late Error Bit indicates that the data transfers from the controller FIFO memory to CPU memory was not able to keep up with the data transfers from the disk drive to the FIFO memory.

The Data Late Error bit is set when the FIFO controller memory is full and there is no place to put the next word obtained from the disk drive, at which point the operation is aborted.

- c. The frequent occurrence of Data Late Errors indicates that the controller DMA Burst Throttle is not properly set for the system environment in which the controller is being used.

To eliminate Data Late Error occurrence the duration of the maximum DMA burst should be increased. The DMA burst duration is strappable from one to 64 words.

Error Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
		<p>This error, once set, is cleared whenever a new command is issued to the controller.</p>
08	Cyclic Redundancy Check Error	<p>During every write operation a cyclic redundancy check (CRC) word is computed within the controller from the data being written on the disk. This CRC value is appended to the end of the data field at the end of each sector.</p> <p>During every read operation a new CRC value is computed from the actual data read, and compared with the original value generated during the write operation.</p> <p>The presence of the error indicates that these two computed values did not agree and that a data error occurred during the write or read operation.</p> <p>In any case the read operation should be repeated to verify the error as being "hard" per the error recovery algorithm.</p> <p>The CRC error bit is also set if a header CRC error was detected. In this case bit 0 of the Error Register will also be active.</p> <p>Once set, this bit may be cleared by issuing a new command to the controller.</p>
09	Command Timeout Error	<p>This bit is set whenever a commanded controller function exceeds the maximum time allowed by the controller for any commanded operation. (4 Seconds)</p> <p>The presence of this error indicates that the controller and/or disk drive hung up during the commanded operation.</p> <p>The error bit, once set, may be cleared by the issuance of any command to the controller.</p>
10	Hard Seek Error	<p>This bit is set whenever the selected disk drive is unable to complete a move within 500ms, or the carriage has moved to a position outside of the recording field, or that a cylinder address greater than the maximum physical number allowed has been issued to the disk drive. Once set this may be cleared only by commanding the selected drive to perform a RTZ operation.</p>

Error Register Explanation Continued

<u>BIT</u>	<u>NAME</u>	<u>FUNCTION/EXPLANATION</u>
11	Drive Fault Error	<p>This bit, when set indicates the presence of a fault condition in the selected disk drive rendering it unfit for use without operator remedial action. Please refer to the associated Disk Drive Manual.</p> <p>If the fault condition is temporary it may be cleared by the issuance of the FAULT CLEAR Command.</p>
12	Drive Not Ready Error	<p>This bit is set if an attempt was made to initiate a command on a disk drive that was not in the "Ready" state.</p> <p>This bit is reset when a new functional command is issued to the controller.</p>
13	Bad Sector Detected	<p>This error/status bit is set if an attempt is made to utilize a sector for data transfer operations which has the optional Sector Integrity Bit Set.</p> <p>In such a case the controller will optionally (strappable) automatically skip over the sector thus flagged as defective to the next available sector in which the Sector Integrity Bit is reset.</p> <p>The error bit is provided more as a status flag to alert the programmer than at least one intended sector did contain an active integrity bit, and that the controller did skip over at least one sector during the commanded operation.</p> <p>This bit is reset whenever a new command is issued to the disk controller.</p>
14	Write Check Data Error	<p>This bit is set during the Write Check Command execution whenever data read from computer memory does not agree exactly with data read from the disk.</p> <p>This bit is reset whenever a new command is issued to the controller.</p>

Error Register Explanation Continued

15 Buss Timeout Error

Set when the controller is performing a DMA Transfer and the memory address specified in the Buss Address Register is nonexistent.

CAUTION: The disk controller will abort any operation when a bus timeout error is detected.

If a disk write operation was being performed it must be repeated to preclude the possibility of generating a "unreadable" sector.



#### 4.0 PHOENIX 211 COMMAND DESCRIPTIONS

Note: All commands are initiated by a "GO" bit.

##### 4.1 System Clear (00g)

When selected, this command does not cause the formatter to go busy. All formatter and interface flip flops are cleared to the reset state. This command is similar to a computer's I/O reset command except it applies only to the formatter and interface logic. It does not clear a seek error or drive fault. No interrupt is generated by the execution of this command.

##### 4.2 Seek Only (01g)

When selected, this command causes the heads to be positioned to the cylinder specified by the Cylinder Address Register. The Formatter goes Not Ready while the disk drive accepts the cylinder address. Formatter Ready is set when the disk drive accepts the new cylinder address and starts seeking. Therefore, no other command may be given until the drive accepts the cylinder address, approximately 10.0  $\mu$ secs. If an error occurs while the drive is seeking, an interrupt is generated. Seek done is set when the seek completes, and an interrupt is generated. To determine which drive caused the interrupt, the disk status register bits 0-1 identify that drive which caused the interrupt and bit 7 will be set to signify that the seek has been completed. The program should check to see if an error occurred during a Seek Only command by selecting the drive and interrogating the error summary bit of the Control & Status Register. Once the disk drive accepts the cylinder address, the program is free to select another drive and perform an operation on it, i.e. Seek, Write, Read, etc. The Seek Inhibit Bit has no effect on this command.

##### 4.3.0 Normal Read (02g)

4.3.1 This command causes the controller to become busy for the duration of the operation.

4.3.2 A seek is initiated automatically (unless inhibited by bit 14 of the Control and Status Register, CSR) on the disk drive specified by the Unit Select Field of the Unit, Sector, Head Register (DUSH) to the Cylinder and Sector specified by the contents of the Cylinder Address Register (DCYL) and Unit, Sector Head Register.

4.3.3 At seek complete data is transferred from the accessed disk sector(s) to consecutive computer memory locations specified by the contents of the Bus Address Register (DBAR).

4.3.4 Once initiated the data transfer continues until the word count register overflows. The Word Count Register is initially loaded with the two's complement of the number of words to be transferred.

4.3.5 Transfers from one to 65, 556 words may be transferred in one operation.

4.3.6 During the course of the transfer the controller will automatically increment across sector, head, and cylinder boundaries, performing automatically additional seeks as necessary to complete the specified transfer.

#### 4.3.7 Read Positioning Verification

Prior to performing a read operation on any sector the header preamble is accessed to verify that the proper sector is being accessed. A 100% position verification technique verifies sector, head, and cylinder disk addressing information.

A cyclic redundancy check value is computed for the header data and is also recomputed and verified as part of the positioning verification procedure performed on every sector involved in a data transfer operation.

#### 4.3.8 Data Field CRC Verification

During the data transfer for each sector a cyclic redundancy check value is computed by the controller based on the actual data read. This computed value is then compared with the reference value appended to the data field and based on the data when written. Any differences in the two CRC values will generate an error and cause the read operation to terminate.

#### 4.3.9 Odd Length ReadData Transfers

If the number of words to be read, as defined by the Word Count Register, does not fall exactly on a sector boundary, direct memory access transfers to memory terminate when the Word Count Register Overflows. However, the controller will continue to read the remaining words in the sector in order to verify the integrity of the data by computing a CRC value for comparison with the reference value at the end of the sector data field.

4.3.10 The disk controller becomes ready when the Word Count Register has overflowed and the controller has completed the CRC data verification check on the last sector accessed, if no errors are encountered. If an error is encountered, the operation is terminated when the error is detected.

4.3.11 An interrupt is generated when the controller becomes ready if bit 06 of the Control & Status Register is set.

#### 4.4.0 Normal Write (03g)

4.4.1 This command causes the controller to go busy for the duration of the operation.

4.4.2 A seek is initiated automatically (unless inhibited by bit 14 of the Control and Status Register) on the disk drive specified by the Unit Select Field of the Unit, Sector, Head Register to the cylinder and sector specified by the contents of the Cylinder Address Register and Unit, Sector, Head Register.

4.4.3 At seek complete, data is transferred from consecutive memory locations specified by the Bus Address Register to consecutive disk sectors addressed by Unit, Sector, Head Register and Cylinder Address Register.

4.4.4 The duration or length of the data transfer in 16 bit words is defined by the Word Count Register, which is initially loaded with the two's complement of the number of words to be transferred. (From 1 to 65,556 words may be transferred in one operation).

4.4.5 The controller will automatically increment across sector, head, and cylinder boundaries, initiating seeks as appropriate to enable the total number of words specified to be automatically, successfully transferred to the disk.

#### 4.4.6 Write Positioning Verification

Before any write operation is performed on any sector the header preamble of each sector is automatically read by the controller and verified for proper sector, head, and cylinder addressing information. Further, the header field itself is verified by a cyclic redundancy check (CRC) value that is computed by the controller and verified each time the header data is accessed.

#### 4.4.7 Data Field CRC Value Generation

During the write operation a CRC value is computed by the controller for the data being written onto each sector. The computed CRC value is automatically written on to the disk at the end of the data field for use as a reference value by the controller during read operations.

The use of the CRC values during read and write insures the user that the integrity of all transferred data is preserved.

#### 4.4.8 Odd Lot Write Transfers

If the number of words to be written, as defined by the Word Count Register, does not fall on an even sector boundary, direct memory access transfers from memory terminate when the Word Count Register Overflows. However, the controller will continue to repeatedly write the contents of the last two data words received from memory onto the disk until the end of the sector is reached. A checksum computed by the controller from the total sector data written is then written onto the end of the sector data field. This checksum is used to verify data integrity during all subsequent read operations.

#### 4.4.9 Write Complete Interrupt

The controller will become ready when the Word Count Register overflows and the checksum has been written onto the last sector accessed, or when an error is detected.

When the controller becomes ready, an interrupt will be generated if bit 06 of the Control & Status Register is set.

#### 4.5 Format Command (04g)

This command is utilized to format the disk medium, and physically writes Sector, Head, and Cylinder position verification data as well as write protect and integrity status information onto the disk at the beginning of each disk sector as a header data preamble. This information is followed by a 16 bit CRC value unique to each sector which is generated and verified automatically by the controller.

Note: All "VIRGIN" disk packs must be "formatted" with this command before they can be read or written by using any of the data transfer commands.

This command specifically writes the absolute disk address of the current sector, in terms of sector, head, and cylinder, as well as write protect and sector information at the beginning of the sector being addressed. This positional information is then followed by a 16 bit CRC value derived from the two header words and written automatically by the controller. The above header information is contained in two 16 bit words of the format given below. When executed this command causes the Formatter to go Not Ready and starts an automatic seek. Upon completion of the seek normally a two word data transfer takes place which transfers the two header words containing the absolute disk address of the sector being addressed from memory to the header of the addressed sector. The Bus Address Register is initially loaded with the memory address of the first header word while the Unit, Sector, Head and Cylinder Registers are initialized to address the sector to be formatted. The two header words must be formatted as indicated below.

Note: 1.) It is up to the program to construct the header words correctly.

2.) A given disk pack is normally only formatted once to generate the proper header data preamble at the beginning of each sector. The positioning information contained in the header preamble is automatically accessed by the controller and used to verify that the proper sector(s) are being accessed prior to initiating any data transfer operation.

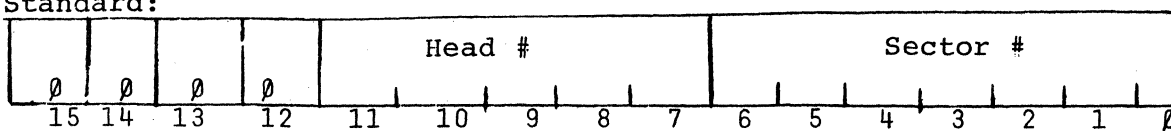
Failure of the accessed actual header position information to agree with the commanded disk position or address will cause the operation to abort and any one or more of the following "soft seek" error to be generated.

#### 4.5 Format Command (04<sub>8</sub>) Continued

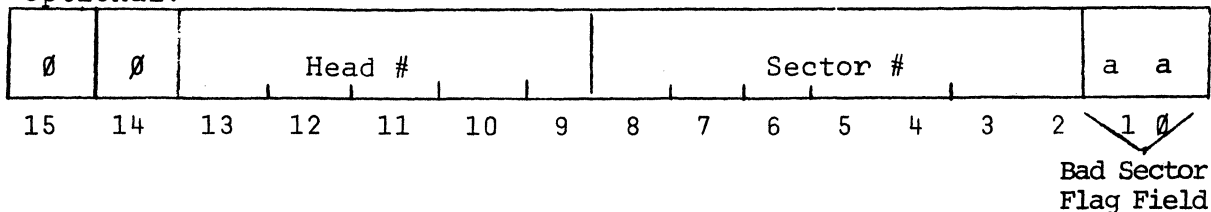
- . Cylinder Address Comparison Error
- . Sector/Head Address Comparison Error
- . Header CRC Error

4.5.1.1 Required Format For Header Word

Standard:



Optional:



4.5.1.2 Header Word 1 Format Explanation

Sector Field

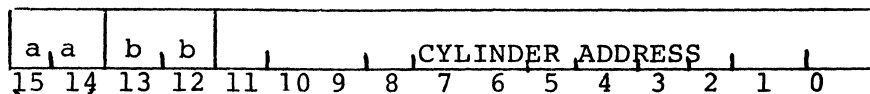
Should contain sector address of the current sector being formatted. Information should be the same as the sector field of the Unit, Sector, Head Register.

Head Field

Should contain head address of the current sector being formatted. Information should be the same as the head field of the Unit, Sector, Head Register.

4.5.1.3 Required Format For Header Word 2

Note: Header word two must be stored in the next consecutive memory location following header word 1.



a/a: BAD SECTOR FLAG FIELD

b/b: SECTOR WRITE PROTECT FIELD

4.5.1.4 Header Word 2 Format Explanation

4.5.1.4.1 Cylinder Address Field

Should contain the cylinder address of the current sector being formatted. Information should be the same as contained in the Cylinder Address Register.

4.5.1.4.2 Sector Write Protect Field

The Phoenix 200 Disk Formatter provides the user with the capability of selectively write protecting data on the disk storage medium to the individual sector level by means of the Write Protect bits in header word 2.

If the write protect bits are set by the user the sector will be write protected. Any subsequent attempt to write on the sector will cause the controller to abort the operation and generate a Write Protect Error.

#### 4.5.1.4.3 Bad Sector Flag Field (Automatic Sector Skip Flags)

The Bad Sector Flag Field is used to identify known defective sectors to be controller.

Normally, the Bad Sector Flag Field bits should be reset. If the bits are set by the user, indicating that the corresponding sector is "defective" the controller will automatically skip over the sector during any disk data transfer and resume operation with the next available sector not flagged as being "defective".

#### 4.5.1.4.4 Bad Sector Flag Utilization

The Bad Sector Flag is intended to enable multiple sector transfers to be conducted on a disk medium with known defective sectors. Such known defective sectors would normally be found and flagged by an Initialization Program which attempted to write and read "1" and "0" data into every bit cell of every sector on the disk. Once the defective sectors had been catalogued and flagged, multiple sector transfers could be conducted "around" a defective sector using the bad sector flag and skip feature without having to make the transfer operations begin and/or end on defective sector boundaries.

#### 4.5.2 Manual Format Enable Switch

Since this command alters the head position verification data or "header" stored on the disk, the "Format" switch on the optional Formatter Control Panel or closure must be manually enabled when this command is executed. This insures that the Format command will not be erroneously executed and result in any loss of data.

Warning: It is not possible to use this command to reformat the header field of a given sector without affecting the data field as well.

If a sector header is to be reformatted and the sector contains meaningful data, the data should be saved before the sector header is reformatted.

Use of this command destroys the data field content of any sector.



#### 4.5.3 Data Field Write Option

A complete sector data field or portion thereof may be written at the same time that the sector is being formatted by appropriately increasing the Word Count Register value and following the header words in memory with the data to be written.

Note: The controller automatically generates a valid CRC value for any data written into the sector field during execution of the Format Command.

#### 4.5.4 Multiple Sector Format Option

Multiple sectors may be formatted by the Format Command by simply increasing the Word Count value and providing the proper data buffer format.

If a multiple sector formatting technique is to be used, the user should remember that a total of two header words plus the appropriate number of data field words is required per sector.

#### 4.5.5 Format Done Interrupt

The disk controller will become Not Busy when the Word Count Register has overflowed and the checksum value has been written at the end of the data field of the last sector accessed. When the Controller becomes ready an interrupt will be generated if bit 06 of the Control & Status Register is set.

#### 4.6 Read Header, Header CRC, Data Field, and Data CRC Command (05g)

##### 4.6.1 Function

The Read Header, Header CRC, Data Field, and Data CRC Command is provided to enable the user to:

1. Read the header field (including the header CRC) of any sector for diagnostic or maintenance verification purposes.
2. Read the data and Data CRC values for any sector for diagnostic or maintenance verification purposes.
3. Recover data from any sector by overriding soft-seek errors encountered during execution of the normal read command.

##### 4.6.2 Operation

4.6.2.1 This command causes the controller to go Not Ready and starts an automatic seek to the specified cylinder, if not inhibited by bit 14 of the Control & Status Register.

4.6.2.2 Upon completion of the seek operation, data is transferred from the addressed sector (starting with header data) to the specified memory locations until the Word Count Register Overflows.

4.6.2.3 The command will transfer in sequential order, the two header words, header CRC value, data field contents, and data CRC value if the word count value permits.

4.6.2.4 This command may be utilized to read header, data, and CRC fields for more than one sector at a time by increasing the word count value accordingly.

If the user chooses to read more than one sector at a time he should remember that the total word count per sector is equal to the data field word count +4.

4.6.2.5 During the execution of this command all softseek and CRC error detection logic is disabled to facilitate data recovery.

4.6.2.6 An interrupt is generated when the operation completes if bit 06 of the Control & Status Register is set.

#### 4.7 Write Header, Data Field and CRC Command (06g)

##### 4.7.1 Function

The Write Header, Data Field and CRC Command is provided to enable the user to readily rewrite the header, data, and CRC fields of any sector for diagnostic and/or maintenance verification purposes.

#### 4.7.2 Operation

- 4.7.2.1 This command causes the controller to go busy and starts an automatic seek to the specified cylinder if not inhibited by bit 14 of the Control & Status Register.
- 4.7.2.2 Upon completion of the seek operation, data is transferred from specified memory locations, sequentially to the header, header CRC, data field, and data CRC fields of the addressed sector until the Word Count Register Overflows.
- 4.7.2.3 No position verification takes place prior to initiation of the data transfer since the header position verification data itself is being written.
- 4.7.2.4 The first two words transferred are the header position verification words and should be formatted by the user per section 4.5.
- 4.7.2.5 The third word transferred is the header CRC value. This standard CRC value should be derived from the actual two header words if a valid value is to be generated.
- 4.7.2.6 If a full sector plus data CRC value is to be written, the CRC value, to be valid, must be derived from the actual data field contents.
- 4.7.2.7 More than one sector can be written by increasing the word count value as desired.

#### Caution:

This command should be used with great care and discretion since it affects the formatting of the disk medium itself.

#### Warning:

This command cannot be used with a word count of three to reformat only the header portion of a sector without affecting the data field. If the header field of a sector is to be rewritten the contents of the data field must be first recovered and saved. Reformatting the header without first saving the data will result in the loss of all data in the sector data field.

- 4.7.2.8 The disk controller becomes ready when the Word Count Register overflows, and will generate an interrupt at that time if bit 06 of the Control & Status Register is set.

## 4.8 Read Data with No Position Verification Command (07g)

### 4.8.1 Function

The Read Data and CRC Command facilitates data recovery by overriding soft seek position verification prior to performing a read operation. It is identical to the Normal Read Command except that the header is not checked prior to reading the data field. (A CRC check is made on the data field contents only.)

### 4.8.2 Operation

- 4.8.2.1 This command causes the controller to go busy and starts an automatic seek to the specified cylinder if not inhibited by bit 14 of the Control & Status Register.
- 4.8.2.2 Upon completion of the seek operation data is transferred from the addressed sector to the specified memory locations until the Word Count Register overflows.
- 4.8.2.3 A CRC Check is made of all data read.
- 4.8.2.4 All controller position verification and position CRC error detection logic is inhibited during the execution of this command.
- 4.8.2.5 More than one sector may be read using this command by increasing the word count value as desired. If a CRC error is detected, the controller will abort the operation and set the CRC Error bit in the Control & Status Register.
- 4.8.2.6 When the operation completes an interrupt will be generated if bit 06 of the Control & Status Register is set.

## 4.9 Write Over Write Protected Sector (10g)

### 4.9.1 Functions

This command enables the user to write on a sector which has active Write Protect Field bits in Header Word 2 if the manual Write Protect Override Closure is also enabled.

### 4.9.2 Operation

- 4.9.2.1 This command is identical in operation to the normal Write Command, except that it will not abort when a sector with active write protect bits in the header is detected, if the Write Protect Override closure is enabled.
- 4.9.2.2 If this command is executed and the Write Protect Override Closure is not enabled, the command will abort and generate a Write Protect Error when a sector with active Write Protect header bits is detected.

#### 4.10 Drive Fault Clear Command (11g)

##### 4.10.1 Function

This command is used to clear the Disk Fault Signal and Condition in the selected disk drive.

Note: This command is the only means by which a Disk Fault can be cleared under program control.

##### 4.10.2 Operation

4.10.2.1 This command executes immediately upon activation and therefore does not cause the controller to go busy.

4.10.2.2 An interrupt is not generated upon completion of this command, since it executes immediately.

#### 4.11 Recalibrate Disk Drive (RTZ) Command (12g)

##### 4.11.1 Function

This command is utilized to clear the selected disk drive electronics of all erroneous conditions except "fault", and to cause heads of the selected disk drive to return to the cylinder 0 position.

Note: This command must be issued to any disk drive which incurs a "hard seek" error before any other operational command can be issued to it.

##### 4.11.2 Operation

4.11.2.1 When this command is executed the controller does not become busy.

4.11.2.2 The selected drive "seeking" bit in the Disk Status Register is set at the beginning of the operation.

4.11.2.3 When the operation is complete and the selected disk head is at cylinder 0, the selected drive "seek done" status bit will be set, the "seeking" status bit will be reset, and the seek done summary bit in the Control & Status Register will be set. A "Seek Done" Interrupt will be generated if the interrupt enable bit (06) of the Control & Status Register is set.

#### 4.12 Write Check Disk Data Command (13g)

##### 4.12.1 Function

This command enables the user to automatically compare data in memory with data contained on the disk, and thus perform an additional check on data written on the disk.

#### 4.12.2 Operation

- 4.12.2.1 This command causes the controller to become busy for the duration of the operation.
- 4.12.2.2 A seek is automatically started to the specified cylinder unless inhibited by bit 05 of the Control & Status Register.
- 4.12.2.3 At seek completion data is transferred from specified memory locations and the addressed disk sectors to the controller.
- 4.12.2.4 The controller automatically performs a bit by bit comparison of the memory and disk data until the Word Count Register overflows.
- 4.12.2.5 If the memory and disk data do not agree a Write Check Error will be generated and the operation will be aborted.
- 4.12.2.6 When the operation terminates an interrupt will be generated if bit 06 of the Control & Status Register is set.

#### 4.13 Release Command (14g) (Dual Port Option Disk Drives Only)

##### 4.13.1 Function

- 4.13.1.2 This command releases the selected disk drive for use by another controller connected to the other port. Execution of this command specifically causes the other disk drive port to be granted a not busy port status.

##### 4.13.2 Operation

- 4.13.2.1 This command is executed immediately upon activation and does not cause the controller to become Not ready.
- 4.13.2.2 No interrupt is generated at the end of the operation since execution and termination are immediate.

Differentiate between CDC and Calcomp.

#### 4.14 Port Request Command

This command causes the Port Request Signal of the selected disk drive to be set.

## 5.0 MARGINAL DATA RECOVERY

Bits 8-11 of the Command and Status Register allow control of the servo positioner and the read recovery circuits in the disk drive. These controls are used to recover marginal data from the disk drive. Allowable combinations during Read command are:

<u>BIT</u>				<u>FUNCTION</u>	
<u>11</u>	<u>10</u>	<u>9</u>	<u>8</u>		
0	0	0	0	Settings are optimum--this is the value normally used.	
0	0	0	1	Data strobe normal	Servo minus
0	0	1	0	Data strobe normal	Servo plus
0	1	0	0	Data strobe late	Servo normal
1	0	0	0	Data strobe early	Servo normal
0	1	0	1	Data strobe late	Servo minus
0	1	1	0	Data strobe late	Servo plus
1	0	0	1	Data strobe early	Servo minus
1	0	1	0	Data strobe early	Servo plus

Certain data errors are considered recoverable, and a sequence of error recovery procedures is outlined below for these. These data errors are:

Header Compare Error

CRC Error

Data Late Error

For these errors the recommended procedure is:

1. Three in-place retries of the operation in error; then if no recovery occurs,
2. Three in-place retries of the operation in error for each allowable marginal recovery state;
3. Perform a Recalibrate;
4. Repeat step (1);
5. Repeat step (2).

## 6.0 PROGRAMMING CONSIDERATIONS

- 6.1 Interrupts are generated upon completion of a command with the exception of Fault Clear and System Clear.
- 6.2 The program must set up the register parameters before 'GO' is issued. Normally the last register to be loaded will be the Command and Status Register which contains the 'GO' bit.
- 6.3 To perform overlapping seeks, the program must select the disk drive (as in all cases) and perform a seek only command on that drive. The Formatter goes NOT Ready while the disk drive accepts the cylinder address. Formatter ready is set to signify that the drive has accepted the cylinder address. At this time, the appropriate seeking bit is set, identifying the Seeking Drive. After this, the program is free to issue any other Drive, a Seek, Recalibrate, Read, or Write command provided a seek error did not occur.
- 6.4 If a seek error occurs, the program must issue a Recalibrate to that disk drive which caused the seek error.
- 6.5 Upon Interrupt, the interrupt service routine should always check for possible error conditions.
- 6.6 Seek Done or Seek Error interrupts are inhibited while the Formatter is currently busy performing a data transfer.
- 6.7 The Formatter will abort, i.e. Formatter Ready will set, whenever an error condition is detected.
- 6.8 An automatic seek occurs for a read or write instruction. Therefore, the program need only give one command to cause the drive to seek and do a data transfer. The program should expect only one interrupt for a read or write command.
- 6.9 The Fault Clear command is used in lieu of operator intervention on the disk drive control panel.
- 6.10 Crossing of head and cylinder boundaries occur the following way:

When the maximum sector of a track is reached, the Formatter will increment to the next logical head and clear the Sector Address. If the maximum sector is reached on the maximum head, the Formatter will increment the cylinder address to the next logical cylinder and Reset the Head and Sector Address.



The Formatter will continue to process data in this manner until the Word Count Register overflows. Overrun Error is flagged when the formatter detects that a read or write operation has finished on the maximum sector and head of the maximum cylinder and the Word Count Register had not yet overflowed.

- 6.11 Seek Done is defined as on specified cylinder and two sectors before the desired sector.
- 6.12 The disk drive must be reselected prior to the issue of any command by loading the Unit, Head, Sector Register.
- 6.13 Calcomp Trident Only. To clear any condition which caused a device check (fault) both a fault clear and a RTZ command must be issued.
- 6.14 Servo Offset
  - a. Must set seek inhibit.
  - b. Error recovery must be limited to single Sector Transfers, or less.
- 6.15 Calcomp Dual Port
- 6.16 CDC Dual Port Operation
- 6.17 Power Fail
  - On ACLO, Failsafe sequence drive down.
- 6.18 Calcomp Trident Only

After the completion or issuing of any command to the 211 controller, software must not access the Controller for a minimum period of 12  $\mu$ S (micro-seconds). This delay allows the Controller to clear any associated interrupts (attention) pending on the selected disk drive.

APPENDIX APHOENIX 211 DISK CONTROLLEROne Sector Read/Write Hand Loop

<u>LOCATION</u>	<u>CONTENTS</u>	<u>INSTRUCTION</u>	<u>COMMENT</u>
1000	12737	MOV #UNIT, DUSH	; Select Disk Drive
1002	Ø		
1004	164002		
LOOP: 1006	12700	MOV # DSTAT, RØ	; Get Disk Status Register Address
1010	164012		
1012	5710	TST @ RØ	; Is disk drive ready?
1014	100401	BMI .+2	; Continue if yes
1016	Ø	HALT	; Halt, Disk Drive Not Ready
1020	12740	MOV # CYL, -(RØ)	; Specify cylinder address
1022	CYL		; Cylinder Value Variable
1024	12740	MOV #-256.,-(RØ)	; Specify one sector word count
1026	177400		
1030	12740	MOV #ADR,-(RØ)	; Specify origin memory address
1032	2000		; 2000 is arbitrary
1034	12740	MOV #TUSH,-(RØ)	; Specify disk, sector,head addresses
1036	Ø		; Ø is arbitrary
1040	105740	TSTB -(RØ)	; Disk controller ready?
1042	100401	BMI .+2	; Continue if yes
1044	Ø	HALT	; Stop if not
1046	12740	MOV #CMP,-(RØ)	; Specify and initiate operation
1057	7-Write 5-Read		
1060	105710	TSTB (RØ)	; Controller done yet?
1062	100376	BPL.-2	; Wait till controller done
1064	5710	TST (RØ)	; Any errors?
1066	100001	BPL .+4	; Continue if not
1070	Ø	HALT	; Stop on error
1070	Ø	HALT	; Normal Stop
1070	137	JMP LOOP	
1072	1006.		



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Phoenix 211 Disk Controller

Diagnostic Manual

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## PHOENIX 211 DISK CONTROLLER DIAGNOSTIC

### 1.0 ABSTRACT

The Phoenix 211 Disk Controller Diagnostic is a series of tests that verify the operation of the Phoenix 211 Disk Controller and attached disk drives.

These tests check all Controller operations with associated disk drive (s) and host PDP-11 computer.

The Phoenix 211 Diagnostic Program and associated manual are the chief tools provided by Xylogics to facilitate maintenance fault isolation to the board level.

The disk diagnostic is organized to exercise in each test a small, finite functional block of logic. The functional block of logic being exercised by each test or subtest is identified to the user in the diagnostic manual along with the board (s) where the logic is physically located.

In the event that the logic being exercised is contained on more than one board, the boards are listed in order of most probable failure location.

It is the intent that the disk diagnostic program and associated manual be utilized by both the user and/or third party maintenance groups to both verify the integrity of any Phoenix 211 Disk Subsystem as well as to readily isolate any failure to the board level.

## 2.0 REQUIREMENTS

- 2.1 PDP11 Minicomputer with 8K core
- 2.2 PHOENIX 211 Disk Controller
- 2.3 CDC 9760, 9762, 9764, 9766 SMD Disk Drive or CALCOMP TRIDENT T-25, T-50, T-80, T-200 Disk Drive

## 3.0 LOADING PROCEDURE

- 3.1 Verify that the Boot Loader is in memory
- 3.2 Set the Switch Register = #750

### MEMORY SIZE #

4K	=	17
8K	=	37
12K	=	57
16K	=	77
20K	=	117
24K	=	137
28K	=	157

- 3.3 Depress Load Address
- 3.4 Depress START

## 4.0 OPERATING INSTRUCTIONS

NOTE 1: This diagnostic must be run on a formatted disk pack and will destroy all data on the pack.

If it is desired to format a pack, use the formatting program included in the diagnostic (Tests 45,47,50)

NOTE 2: For CPU's without a switch register see Section 4.4.

- 4.1.1 Set Program Counter (PC) to program "START" address (See Diagnostic Listing)
- 4.1.2 Enter starting test number in the most significant byte of the console switch register.
- 4.1.3 Enter desired end test number in the least significant byte of the console switch register. The first test number is zero.
- 4.1.4 Set the most significant bit (Bit 15) of switch register if the tests are to be repeated. Leave reset if the tests are to be executed only once.
- 4.1.5 Depress "START" switch on computer console. The computer will start and then halt.

- 4.1.6 Enter starting disk drive number into the most significant byte of console switch register.
- 4.1.7 Enter number of the last disk drive to be tested in the least significant byte of console switch register. Note that the maximum drive number = 3 (0 through 3).
- 4.1.8 Depress the CONTINUE switch on the computer console.
- 4.1.9 The computer will then execute all tests specified on all disks specified. It will also stop if any error is encountered unless the following switch settings are used.

4.2 CONSOLE SWITCH SETTINGS (ERROR MODES)

BIT 15	BIT 14	BIT 7	SETTING REFERENCE
0	0	0	SSA
0	0	1	SSB
0	1	0	SSC
0	1	1	SSD
1	0	0	SSE
1	0	1	SSF
1	1	0	SSG
1	1	1	SSH

4.2.1 SSA

All three console bits "OFF" will allow the computer to halt upon encountering any type of error (most commonly used mode).

4.2.2 SSB

Switch Register Bit 7 set alone applies only to Data Compare errors and allows for data reliability checking. Each time a Data Compare error is flagged, location "ERRCNT" is incremented and no retry occurs. The Data Compare routine "DATCMP" then continues on with the next consecutive data word.

4.2.3 SSC

This mode applies only to soft controller errors outlined below:



## SOFT CONTROLLER ERRORS

DATA LATE

HEADER COMPARE (SOFT SEEK)

DATA CRC

HEADER CRC

Console Bit 14 enables the controller to retry the command previously issued that caused one of the above error conditions. When used alone Bit 14 will allow the PHOENIX 211 up to four retries before the error is logged as a "hard" error and the general error flag "ERRFLG" is set.

### 4.2.4 SSD

Designed primarily for use as data error logging exercise in conjunction with TEST #32 (Complete Disk Read), this mode combines both Soft Controller Error Retry and Data Compare Error Retry. Explanation of each error counter and flag is given below.

<u>LOCATION</u>	<u>LABEL</u>	<u>EXPLANATION</u>
	SOFERR	- This is the total number of soft controller errors encountered (Bit 14).
	ERRFLG	- This flag is set each time a "hard" error is detected, and causes a program halt unless Bit 15 is set.
	ERRCNT	- This is the total number of data compare errors (Bit 7).
	HERCNT	- A counter for hard data errors; this location will be incremented each time a data word fails after eight attempts to reread that particular sector (Bits 7, 14, TEST32 ).
	ERROR	- If Bit 15 is set and an error is flagged (ERRFLG $\neq$ 0), this location is incremented (Bits 7, 14, 15).
	SKIPER	- Hard controller error counter that is incremented in the Retry mode when four attempts to reread a sector have resulted in an error condition (Bit 14, TEST 32 only). Test 32 will then skip over that sector and continue on.

#### 4.2.5 SSE

This mode inhibits all errors from causing a Program Halt. When an error is detected (ERRFLG  $\neq$  0) in an exercise sequence of more than one test, control is transferred back to the program executive and testing continues with the next consecutive test. Location "ERROR" is incremented each time a failure is detected.

#### 4.2.6 SSF

Data Compare Logging is incorporated along with Program Halt upon detection of any Controller error (errors flagged by the DERR register).

#### 4.2.7 SSG

Data Compare Errors are considered "hard" errors and would be captured in location "ERROR". "Soft" controller errors would be retried without a Program Halt. (Bits 14, 15).

#### 4.2.8 SSH

Data Errors would be logged and retried, "soft" Controller errors would be logged and retried, "hard" Controller errors would be logged and the sequence (TEST32) would be restarted (all error counters would be reset at RESTART).

### 4.3 RECOMMENDED TEST SEQUENCES

#### 4.3.1 Logic

For a complete test of the PHOENIX 211 and attached Disk Drive(s), it is recommended that a complete "pass" of the diagnostic is used. This sequence is defined as Tests 0 - 32 with all Error Inhibit and Retry switches OFF.

#### 4.3.2 Reliability

Reliability testing is accomplished using Test32 (Entire Disk Read) in the Repeat mode. Since Test32 uses only the Read command, Test 31 (Entire Disk Write and Read) must be run prior to Test32.

#### 4.4 ALTERNATE OPERATING MODES

##### 4.4.1 NON SWITCH REGISTER MODE

This mode is used when a switch register is not present on the user's PDP11. To enter this mode deposit a non zero number into location "NONCON" (LOCATION 1266). At this point test parameters should be entered by depositing the selected sequence into memory starting at label "STPTN" (ending test number). (See diagnostic listing). The default setting is test sequence 0 thru 30 on drive 0.

At the end of a test sequence or when an error is detected the program counter (PC) will be changed to 173000<sub>0</sub>, activating the M9301 rom. Before the console is made live, the CPU registers, R0 R6, are saved in memory starting at location "REG0." The general error flag "ERRFLG" is loaded into register R0 and the current test number is loaded into CPU register R4 just prior to activating the Emulator giving a quick detection of passage or failure.

##### 4.4.2 ERROR CORRECTION CONTROLLERS (ECC)

Phoenix 211 Disk Controllers equipped with error correction are tested by depositing a non-zero number into location "ECC" (1074<sub>8</sub>). Modifying this location enables the test executive to use an alternate test origin table, containing ECC logic tests.

##### 4.4.3 AUTO-SWITCH OPTION

Controllers equipped with the auto-switch option can be tested the normal test procedure if the alternate DATA PATH, (AUTO SWITCH BIT # 7 OFF), is not enabled.

To test the alternate data path the operator must do two things:

1. Deposit a non-zero number in location "AUTOSW" (2310<sub>8</sub>)
2. Mov the Interface Data Cable from J1 conn. to J2 conn. on the auto switch board (See Auto Switch Manual).

With the autoswitch mode enabled the program will set bit #7 on the autoswitch board before a transfer (DMA).

##### 4.4.4 MULTIPLE COMPUTER PORT OPTION

###### 4.4.4.1 SINGLE CPU

To run the controller with a single CPU, deposit a non-zero number into location "MULCPU" and use normal diagnostic procedures. Setting the "MULCPU" flag forces the program to request the controller each function to be performed. Because the diagnostic, in some tests, issues I/O resets and system clear commands, multiple CPU's cannot be run simultaneously.

#### 4.4.4.2 SIMULTANEOUS CPU EXERCISE

To check possible conflict among two or more CPU's requesting a single Phoenix 211 formatter, it becomes necessary to run a special exercise. Test 33<sub>g</sub> has been modified to release the Phoenix controller after completing a write/read sequence. Normally during the Diagnostic Testing, all tests except 33, the formatter is not released. Operation is as follows:

1. Deposit a non-zero number in location "MULCPU" of each CPU under test.
2. Use test 33 as starting and ending test number.
3. Continue normal operating instructions.

#### 4.4.5 NO TEST INPUT MODE

This mode is the same as non-console mode (section 4.4.1) except that it halts at normal halt locations instead of activating the console emulator. This mode is useful when:

1. CPU type is PDP11/04 or PDP11/34 and has programmers console (byte loading of test parameters) or,
2. The same test sequence is repeated often.

OPERATION: Deposit a non-zero number in location "NINPUT " Start at normal start location

#### 5.0 GENERAL DIAGNOSTIC STRUCTURE

5.1 The PHOENIX 211 Disk Controller Diagnostic uses small subtests that are linked together through the test executive routine. The subtests use common subroutines to execute all data transfers. Ending Controller parameters are checked following each controller operation and Interrupt mode is employed in all exercises.

#### 5.2 COMPUTER ERROR HALT

If the computer halts for an error these registers will define the condition:

R0 = 2 x the disk drive number

R1 = test number

R2 = reference data

R3 = actual data received

R4 = subtest number

R5 = address where error was detected

NOTE: In some cases Registers R2 and R3 do not necessarily point to the cause of the Error Halt. The user should always use the subtest number (R4) to locate the area of failure in the test.

#### 5.3 DISK AND CONTROLLER PARAMETER CHANGES

5.3.1 THE STANDARD DISK PARAMETERS ARE AS FOLLOWS:

Number of Cylinders =  $823_{10}$  ( $1467_8$ )  
Number of Heads = 5  
Number of Sectors =  $32_{10}$  ( $40_8$ )  
Number of Words Per Sector =  $256_{10}$  ( $400_8$ )

5.3.2 THE STANDARD CONTROLLER PARAMETERS ARE AS FOLLOWS:

Base Address (DCSR) = 164000  
Interrupt Sector = 270

5.3.3 INSTRUCTIONS FOR CHANGING PARAMETERS

Located in Sections 3 and 4 of the Diagnostic Assembly listing are all the parameters listed above. To change any or all of these values, deposit into memory the desired value.

5.3.3.1 DISK CHANGES There are only 4 changes that apply, the labels are the following:

MAXSEC: Word 37 ; Last sector  
MAXHD: Word 1000 ; Last head - justified for DUSH  
MAXCYL: Word 1466 ; Last cylinder  
WPSEC: Word 177400 ; # of words per sector in 2's complement

All other references to these values will be set up by subroutine "ADRSTP" during program start up.

5.3.3.2 CONTROLLER CHANGES The base address and interrupt vector labels are the following:

DCSR: Word 164000 ; Base Address  
INTVEC: Word 270 ; Interrupt Vector

When a base address change is necessary, only change the location "DCSR". The remaining register assignments will be built by subroutine "ADRSTP" during program start up.

6.0 TEST ABSTRACTS

6.1 INDIVIDUAL TESTS

6.1.1 Test Ø

This test issues an I/O command and verifies that "INIT" clears all registers in the PHOENIX 211 Controller.

6.1.1.1 Initialization Test Subtest Listing

<u>Board</u>	<u>Subtest</u>	
<u>Being Tested</u>	<u>Number (R4)</u>	<u>Subtest Name/Error Condition</u>
211+1	Ø	Incorrect Control & Status Register Initialization
211	1	Incorrect Bus Address Register Initialization
211	2	Incorrect Word Count Register Initialization
4	3	Incorrect Cylinder Address Register Initialization
2	4	Incorrect Disk Status Register Initialization
1	5	Incorrect Disk Error Register Initialization
3	6	Incorrect Sector, Head Register Initialization

6.1.2 Test 1: Register Load and Read Tests

This routine tests the capability of the selected formatter registers to be loaded and interrogated with any data. Each register is checked with four constants 100 times.

6.1.2.1 Patterns used are as follows:

Pattern 1 - ∅  
 Pattern 2 - 052525  
 Pattern 3 - 125252  
 Pattern 4 - 177777

6.1.2.2 Load and Read Sub Test Listing (R4 Value at Error Halt)

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
211+1	∅	Incorrect Control & Status Register Load OR Read
211	1	Incorrect Bus Address Register Load OR Read
211	2	Incorrect Word Count Register Load OR Read
4+1,211	3	Incorrect Cylinder Address Register Load OR Read
3,1,211	4	Incorrect Unit, Sector, Head Register Load OR Read

6.1.2.3 Read only, and constant, bits in the controller registers are masked out of the test process.

6.1.3 Test 2: Sliding One Register Load & Read Tests

In this test all of the controller registers are loaded with a sliding 1 data pattern and interrogated for proper content. The logic one bit constant is "slid" from the bit zero position to the bit 15 position in 16 separate tests.

6.1.3.1 Sliding One Register Load and Read Subtest Listing

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
1	∅	Incorrect Control & Status Register Load OR Read
3	1	Incorrect Unit, Sector, Head Register Load OR Read
211	2	Incorrect Bus Address Register Load OR Read
211	3	Incorrect Word Count Register Load OR Read
4	4	Incorrect Cylinder Address Register Load OR Read

6.1.4 Test 3: Sliding Zero Register Load & Read Test

In this test all of the controller registers are loaded with a "sliding zero" data pattern and interrogated for proper content.

The logic zero bit constant is slid from the bit zero position to the bit 15 position in 17 separate tests.

#### 6.1.4.1 Sliding Zero Register Load and Read Subtest Listing

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
1	0	Incorrect Control & Status Register Load OR Read
3	1	Incorrect Unit, Sector, Head Register Load OR Read
211	2	Incorrect Bus Address Register Load OR Read
211	3	Incorrect Word Count Register Load OR Read
4	4	Incorrect Cylinder Address Register Load OR Read

#### 6.1.5 Test 4: Disk Error and Status Register Tests

These tests verify that the nonexistent Head, Sector and Cylinder (Track) errors can be set and cleared properly.

Also tested in this test is the byte loading capability of the Command and Status register (DCSR).

##### 6.1.5.1 Disk Error and Status Register Subtest Listing

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
3,1	0	No Illegal Sector Error Summary Generation
3,1	1	No Illegal Sector Error Bit Generation
3,1	2	Illegal Sector Error Bit did not clear
3,1	3	No Illegal Head Error Summary Generation
3,1	4	No Illegal Head Error Bit Generation
3,1	5	Illegal Head Error Bit did not clear
4,1	6	No Illegal Cylinder Error Summary Generation
4,1	7	No Illegal Cylinder Error Bit Generation
4,1	10	Illegal Cylinder Error Bit did not clear
1	11	No Illegal Sector,Head,Cylinder Error Summary Generation
3,4,1	12	Illegal Sector,Head,Cylinder Error Bits did not set
3,4,1	13	Illegal sector, head, cylinder error summary set
1,211	14	Control & Status Upper Byte Did Not Load
1,211	15	Control & Status Lower Byte Did Not Load

#### 6.1.6 TEST 5: Unit Select Tests

These tests verify that the Unit Select lines access the proper Disk Drives. This testing is accomplished by selecting each Disk Drive Port and issuing a SEEK. The DSTAT register-seeking flops are checked for proper seeking status and a Formatter Clear is then given to clear them. This test does not wait for Seek Done.



### 6.1.6.1 Unit Select Seeking Tests Subtest Listing

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
1,2,3,4	Ø	Disk Drive or Formatter, not ready
2,3,1	1	Did Not Set Unit Ø Seeking Flop Via Seek CMD
3	2	No Formatter Ready Generation on Formatter Clear CMD
2	3	Did Not Set Unit 1 Seeking Flop Via Seek Card
3	4	No Formatter Ready Generation on Formatter Clear CMD
2	5	Did Not Set Unit 2 Seeking Flop Via Seek CMD
3	6	No Formatter Ready Generation on Formatter Clear CMD
2	7	Did Not Set Unit 3 Seeking Flop via Seek CMD
3	10	No Formatter Ready Generation on Formatter Clear CMD

### 6.1.7 TEST 6: Seeking Test

In this exercise two seeking commands are issued, Seek and Recalibrate, and proper Seek-Done flops are checked. Also checked in this test is that an illegal track address used on a Seek command causes a Nonexistent Track Error and not a Seek Error.

#### 6.1.7.1 Seeking Test Subtest Listing

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Name</u>
1	Ø	Formatter not ready
4,2,3	1	Selected Drive Not Ready
4,2	2	Error Generation on RTZ CMD, No Seek Done Summary Status Bit Generation on RTZ
2,4	3	No Selected Drive Seek Done Status Bit Generation on RTZ
3,1	4	No Formatter Ready at RTZ Completion
4	5	No Illegal Cylinder Error Bit Generation on Seek CMD
4	6	Other Error Bit Generation on Illegal Seek CMD
3	7	No Seek Done Summary Bit Generation On Seek CMD
3	1Ø	No Selected Drive Seek Done Status Bit Generation on Seek CMD
4	11	Other Drive Seek Done Bit Generation on Seek CMD

### 6.1.8 TEST 7: Interrupt Test

The Interrupt tests use two formatter commands, the Recalibrate command and the Seek Only command. At this stage of testing, the Seek logic should be operable. The Interrupt logic uses these commands to cause the Seek Done identification bits to generate an Interrupt.

NOTE: If the CPU halts during this test at some memory location between 14 and 776, the Interrupt branched to a wrong location. This indicates a fault in the Interrupt Vector Address.

#### 6.1.8.1 Interrupt Test Subtest Listing

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
1	Ø	Drive Not Ready
	1	None
2,1,211	2	No Interrupt Generation with RTZ CMD
2	3	Improper Disk Ident Bits set in Disk Status Register at RTZ Interrupt
3	4	No Interrupt Generation With Seek CMD
2	5	Improper Disk Ident Bits set in Disk Status Register at Seek Interrupt

### 6.1.9 TEST 10: One Word Write Test

This test is the first Write attempted by the Formatter. It is only a one word transfer and only the ending formatter register parameters are checked.

- 6.1.9.1 This test will write data onto the first usable sector on the disk medium.
- 6.1.9.2 The write operation is conducted by the "DXFER" Subroutine which tests all controller parameters before, during, and after the specified operation.
- 6.1.9.3 If an error occurs it will be detected by DXFER Subroutine and the subtest count will be contained in location "DTCNT". For a complete description of the DXFER Subroutine subtest error conditions see Appendix A. Test10 DTCNT subtest error conditions are defined below.

TEST 10: DXFER DTCNT Subtest Error Conditions

Note: This is the first test to use the DMA logic. If the computer bus hangs up, the 211 Interface Board or CPU backplane is suspect.

<u>DTCNT Value</u>	<u>Subtext Name/Error Conditon</u>	<u>Board Being Tested</u>
Ø	Controller Not Ready	1
1	Selected Disk Drive Not Ready	4,2
2	Controller Went Busy with No "GO" CMD	3
3	Controller did not go busy with "GO" CMD	3
4	Interrupt did not occur before timeout	3,4,1
5	Controller Hang in "BUSY" State	3,211,2
6	Word Count Register did not overflow	211,2,3
9	End Bus Address Register Incorrect	211
10	End Sector Value Incorrect	3
11	End Head Value Incorrect	3
12	End Cylinder Address Value Incorrect	4
13	Controller Error Bit Set	3,2,4

Note: 1. This test exercises so much incrementally new logic in the disk controller that the user should examine the disk controller register images saved by the diagnostic at the time of error detection.

Correct Ending Values for Disk Controller Registers are as follows:

	<u>Register</u>	<u>Correct Contents</u>
1	Control & Status	000306
2	Unit, Sector, Head	0x0001
3	Bus Address	xxxxxx
4	Word Count	000000
5	Cylinder	000000
6	Disk Status	100000
7	Error	00000Ø

Note: 2. Any soft seek header or header CRC error will cause the controller to abort the write operation before actually writing any data onto the disk.

6.1.10 TEST 11: One Sector Write Test:

6.1.10.1 This test writes data on one sector of the disk. The Cylinder address is normally determined by RWCYL, while the Sector, Head and Unit value is determined by RDUSH.

NOTE: 1.) This is the first time that a full sector transfer has been attempted.

2.) No data is checked during this test.

3.) The object of this test is to verify that the disk controller properly goes through the motions of performing a disk write operation:

4.) Specific functions verified during this test are:

- 1 - Multiple Write DMA Data Path to Controller FIFO memory
- 2 - Multiple Write FIFO data path to disk
- 3 - Multiple Word Count Register Write Incrementation
- 4 - Multiple Bus Address Register Write Incrementation

6.1.10.2 Optionally, the Sector and Head are dynamically selectable by the console switch register if CSWTCH is loaded with any non-zero value.

6.1.10.3 RWCYL and RDUSH locations are normally set up to write the data on the last available sector on the medium.

6.1.10.4 The actual write operation is performed under control of "DXFER" Subroutine and all appropriate errors are detected by "DXFER" and the error subtest count is contained in location "DTCNT" ..

Please refer to Appendix A for a complete description of the DXFER Subroutine and subtest error conditons.

Note: If this test fails while test10 passes, the most probable suspect is board 2 followed by the 211 Interface Board.

6.1.10.5 DXFER DTCNT Subtest Error Conditions

<u>DTCNT Value</u>	<u>Subtest Name/Error Condition</u>	<u>Board Being Tested</u>
Ø	Controller Not Ready	1
1	Selected Disk Drive Not Ready	4
2	Controller went Busy with no "GO" CMD	3
3	Controller did not go Busy with "GO" CMD	3
4	Interrupt did not occur before timeout	2
5	Controller Hang in "BUSY" State	2
6	Word Count Register did not overflow	2,211
9	End Bus Address Register Incorrect	211
10	End Sector Value Incorrect	3
11	End Head Value Incorrect	3
12	End Cylinder Address Value Incorrect	4
13	Controller Error Bit Set	3,2,4

6.1.11 TEST 12: One Sector Read Test

6.1.11.1 This test reads data from one sector of the disk. The Cylinder address is normally determined by RWCYL, while the Sector and Head address are normally determined by RDUSH. Optionally, the Sector and Head address may be dynamically selectable by the console switch register if CSWTCH is loaded with any non-zero value.

NOTE: 1.) This is the first time that any disk Read data transfer operation has been attempted.

2.) No data is checked during this test.

3.) The object of this test is to verify that the disk controller properly goes through the motions of performing a disk read operation.

4.) Specific functions verified during this test are:

1 - Multiple Read DMA data path from controller FIFO memories to computer memory.

2 - Multiple Read data path from disk to FIFO memories.

3 - Word Count Register Read Incrementation

4 - Bus Address Register Read Incrementation

6.1.11.2 RWCYL and RDUSH locations are normally set up to read the last usable sector on the disk medium.

6.1.11.3 Data Read Back is stored in Input Buffer 1 (IDBUF1)

6.1.11.4 The actual read operation is performed by the "DXFER" Subroutine and all appropriate errors are detected by DXFER and the error subtest count is stored in location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine. Subtest error conditions for Test 12 are defined below.

6.1.11.5 DXFER DTCNT Subtest Error Conditions

<u>DTCNT Value</u>	<u>Subtest Name/Error Condition</u>	
Ø	Controller Not Ready	1
1	Selected Disk Drive Not Ready	4
2	Controller Went Busy with no "GO" CMD	3
3	Controller did not go Busy with "G" CMD	3
4	Interrupt did not occur before timeout	3
5	Controller Hang in "BUSY" state	3,2
6	Word Count Register did not overflow	2,3
9	End Bus Address Register Incorrect	211
10	End Sector Value Incorrect	3
11	End Head Value Incorrect	3
12	End Cylinder Address Value Incorrect	4
13	Controller Error Bit Set	3,2*

\* Data Late Error

Note: 1. This test exercises so much incrementally new logic in the disk controller that the user should examine the disk controller register images saved by the diagnostic at the time of error detection.

Correct Ending Values for Disk Controller Registers are as follows:

<u>Register</u>	<u>Correct Status</u>
1 Control & Status	000304
2 Unit, Sector, Head	XXXXXX
3 Bus Address	XXXXXX
4 Word Count	XXXXXX'S
5 Cylinder	100000
6 Disk Status	000000
7 Error	

Note: 2. Any soft seek header or header CRC error will cause the controller to abort the read operation before actually receiving any data from the disk.

6.1.12 TEST 13: Write Count Test

6.1.12.1 This test performs Write operations with an ever-increasing word count starting with 1 and increasing in power of 2 to a maximum of 4096 words. Each Write operation starts at absolute 0 Disk address.

NOTE:

- 1.) No data is checked during this test.
- 2.) The object of this test is to verify that the disk controller sequences logic performs correctly under data transfers less than and greater than one sector in word length.

6.1.12.2 All thirteen data transfer operations performed in this test are done by the "DXFER" Subroutine. Any errors detected by the DXFER Subroutine during any of the 13 data transfers performed will be indicated by the DXFER subtest count value contained in location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine and DTCNT subtest error conditions.

6.1.12.3 Write Count Subtest Listing

R4 in this test is used to define what one of 13 write data transfer operations is to be performed by DXFER per the following table:

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
	Ø	Error During 1 Word Write
	1	Error During 2 Word Write
	2	Error During 4 Word Write
	3	Error During 8 Word Write
	4	Error During 16 Word Write
	5	Error During 32 Word Write
	6	Error During 64 Word Write
	7	Error During 128 Word Write
2	10	Error During 256 Word Write
3,211	11	Error During 512 Word Write
3,211	12	Error During 1024 Word Write
3,211	13	Error During 2048 Word Write
3,211	14	Error During 4096 Word Write

6.1.12.4 Logic specifically tested includes sector sequencer control, DMA word count Incrementation and Disk Word Count Incrementation

6.1.12.5 No new logic is exercised by subtests Ø - 7.



6.1.13 TEST 14: One-Sector Read, Write, Compare Test

- 6.1.13.1 This Test writes data on one sector of the disk, reads it back, and compares the data obtained with the original data written. The cylinder address is specified by RWCYL while the Sector and Head values are normally supplied by RWUSH. Optionally, the Sector and Head data may be dynamically supplied from the console switch register if CSWTCH contains any non-zero value.
- 6.1.13.2 Data is normally written onto the last physical sector on the disk medium from the Output Buffer (ODBUF) and written back into Input Buffer 1 (IDBUF1).

6.1.13.3 All disk data transfers physically performed by the "DXFER" Subroutine. Any data transfer errors detected by DXFER will be indicated by the DXFER subtest count value contained in location DTCNT.

Please refer to Appendix A for a complete description of the DXFER Subroutine and subtest error conditions.

6.1.13.4 The Read, Write, Compare Subroutine (WRC) is used in this test to manage the Write, Read and Data Comparisons. (Reference Appendix B)

1.) If an error is encountered during the write data transfer (by DXFER) the "WRTErr" location is incremented.

2.) If an error is encountered during the write data transfer (by DXFER) the "RDERR" location is incremented.

3.) All Data comparisons between original data written onto disk from ODBUF and data received from the disk in IDBUF1 are performed by the Data Comparison Subroutine "DATCMP". (Reference Appendix C)

If an error is detected during the data comparison subroutine "CMPCNT" contains the number of words compared before the error occurred while R2 and R3 contain the correct and actual data values respectively.

6.1.13.5 R4 has no significance in this test with respect to subtest identification.

6.1.13.6 At this point the controller can at least go correctly through all the motions of doing both read and write operations, and is correctly reading the sector header data.

6.1.13.7 The capability to write or read data correctly has not been previously verified.

6.1.13.8 The most probable error to occur during this test is a data comparison error. If a data comparison error occurs, the most probable board at fault is Board 2 which contains all of the data path logic, followed by the 211 coupler.

#### 6.1.14 TEST 15: Read, Write, Compare Count Test

6.1.14.1 This test performs Write, Read, and Data Compare operations with an ever increasing word count starting with one and increasing by powers of two to a maximum of 512 words.

Each disk operation starts at absolute disk address 0.

6.1.14.2 All disk parameters are checked during the test by the DXFER Subroutine. Any data transfer errors detected by the "DXFER" Subroutine will be indicated by the subtest count value contained in location DTCNT.

Please refer to Appendix A for a complete description of the DXFER Subroutine and subtest error conditions.

6.1.14.3 The Write, Read, Data Comparisons are managed by the Read, Write, Data Comparison Subroutine (WRC).

Reference Appendix B.

- 1.) If an error is encountered during a write operation (by DXFER) the "WRTERR" location is set to a non zero value.
- 2.) If an error is detected during a read operation (by DXFER) the "RDERR" location is set to a non zero value.
- 3.) If an error is detected during the data comparison (by DATCMP) location "CMPCNT" contains the word count value when the error was detected.

6.1.14.4 Write, Read, Compare Count Subtest Listing  
R4 is utilized in the test to determine which one of 9 Write, Read, Compare Operations is being performed per the following:

<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
Ø	Error During 1 Word Write, Read, Compare
1	Error During 2 Word Write, Read, Compare
2	Error During 4 Word Write, Read, Compare
3	Error During 8 Word Write, Read, Compare
4	Error During 16 Word Write, Read, Compare
5	Error During 32 Word Write, Read, Compare
6	Error During 64 Word Write, Read, Compare
7	Error During 128 Word Write, Read, Compare
10	Error During 256 Word Write, Read, Compare
11	Error During 512 Word Write, Read, Compare

6.1.14.5 This test does not specifically test any new controller logic but is executed to gain additional confidence in the capability of the disk controller to read and write data correctly. If an error occurs during data comparison, Board 2 is probably at fault.

#### 6.1.15 TEST 16: Write-Protect Test\*

This test verifies that the Controller will not Write over Write-Protected sectors.

6.1.15.1 First the test sets the Write-Protect bits of the absolute sector Ø and then attempts to write on that sector. The test then verifies that the Controller aborted the Write operation and that the Write-Protect error bit is activated.

6.1.15.2 All required disk data transfers are performed by the "DXFER" Subroutine and any errors detected by DXFER are indicated by the DXFER subtest count saved at location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine and subtest error conditions.

\* Does not apply on ECC equipped controllers.

### 6.1.15.3 Write Protect Subtest Listing

<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
∅	Write Protect Sector Format Error
1	No Error Detection on Write over Write Protected Sector
2	Write Over Write Protected Sector Error Bit Not Set
3	Error During Read of Write Protected Sector
4	Data Error-Attempted Write on Protected Sector Not Aborted
5	Error During Reformat of Write Protected Sector

6.1.15.4 This verifies that the attempted write on a Write Protected Sector was aborted by reading the data back and comparing it with original known data by the "DATCMP" Subroutine.

Reference Appendix C.

6.1.15.5 The Sector Write Protect logic exercised by this test is contained on Board 3.

6.1.15.6 Error Register logic is on Board 1.

### 6.1.16 TEST 17: Header Override - HEADER READ TEST \*

6.1.16.1 This test verifies that the Read-Without-Header-Check logic is functioning properly. The Header is first erroneously written and then a normal Read operation is attempted to insure that we cannot read the sector.

6.1.16.2 The Read-Without-Header-Check command is then used to Read the sector. Checks are made to insure that no error occurs and that the data is correct.

6.1.16.3 All required data transfers are performed by the "DXFER" Subroutine, and any detected errors are indicated by the DXFER subtest count saved at location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine and subtest error conditions.

### 6.1.16.4 Header Override Subtest Listing

<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
∅	Error During Erroneous Header Format
1	No Error During Read of Sector with Bad Header OR No Header Error Bit Set
2	Error During Header Override Read of Sector with Bad Header
3	Header Override Read Error - Data Incorrect
4	Error During Reformat of Sector
*	Does not apply to ECC equipped controllers



6.1.16.5 The header logic exercised by this test is contained on Board 3

6.1.16.6 The Error Register logic is contained on Board 1.

6.1.16.7 This section of Test 17 checks the ability of the controller to read the header field, header CRC, Data Field, and the Data Field CRC.

6.1.16.8 Header read verify subtest listing subtest number (R4)

Subtest Number (R4)	<u>Subtest Namer/Error Condition</u>
5	Error during reformat using write header, data, CRC command
6	Error during read of header, data, CRC, command
7	Data error on sector field
10	Error during normal format

6.1.16.9 Early Phoenix 211's were shipped with the read hdr, CRC, Data, CRC command operating as a read header and CRC only command. If the Operator's controller constantly fails Subtest 7 of this Test (17), deposit a non-zero number in location "OLDHDR". This modification will cause the program to skip a certain section of the test.

Note: This difference will not cause any compatibility problems in mixing new or old controllers and, or disk packs. The Read Header, Header CRC, Data and Data CRC command is not used by any DEC\* Operating Systems, and would only be used in special application programs, (pack verification), or in diagnostics.

\*Digital Equipment Corporation

6.1.17 TEST 20: Write-Protect Override - Write Check Test

This test verifies that the Write-Protect-Override command logic functions properly.

- 6.1.17.1 Known data is written onto the disk. The sector to be Write-Protected is then so protected and new data is written using the Override command. The new data is then read back and checked to verify that the Write operation actually took place.
- 6.1.17.2 All required data transfers are performed by the "DXFER" Sub-routine, and any detected errors are indicated by the DXFER subtest count saved in location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine and subtest error conditions.

6.1.17.3 Write Protect Override Subtest Listing

<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Conditions</u>
Ø	Error During Write Protect Sector Format
1	Error During Write Over Write Protected Sector Override
2	Error During Read of Protected Sector
3	Data Error - Write Operation did <u>Not</u> Override Protected Sector
4	Error During Sector Reformat

6.1.17.4 The Write Protect Override Logic exercised by this test is located on Board 3.

6.1.17.5 The second section of Test 20 verifies the write check logic of the 211 controller. Known data is first written using normal write command. A write check command is issued and checks are made to insure no error was generated. The last step is to destroy a part of the memory buffer and to issue write-check commands (2) to insure that an error is generated.

#### 6.1.17.6 Write Check Subtest Listing

<u>SUBTEST NUMBER (R4)</u>	<u>SUBTEST NAME/ERROR CONDITION</u>
5	Error during initial normal write
6	Error during write check command
7	Error not detected during write check command with destroyed buffer
10	Write check error bit not set
11	Other errors bits set
12	Error not detected during second erroneous write check command
13	Write check error not set or some other error set as well
14	Corrected buffer with write check command reissued caused error



6.1.18 TEST 17: Header-Write Command Test

6.1.18.1 This test verifies that the Header can be written by the Write-Header-and Verify command (CRC). The Header is written to an erroneous value using the command and then a normal Read is attempted and the presence of the appropriate Header Error bit (s) is (are) checked.

6.1.18.2 All required data transfers are performed by the "DXFER" Subroutine, and any detected errors are indicated by the DXFER subtest count saved in location "DTCNT".

6.1.18.3 Header-Write Command Subtest Listing

<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
Ø	Error During Erroneous Sector Header Format
1	No Detected Error During Read of Sector with Bad Sector Header
	OR
2	Sector Header Error Bit Not Set
3	Bus Address Register Erroneously Incremented
4	Word Count Register Erroneously
5	Error During Sector Reformat to Illegal Head Header
6	No Detected Error During Read of Sector with Bad Head Header
7	Header Error Bit Not Set
8	Other errors generated other than sector/head error
10	Error during reformat to illegal cylinder address
11	Error not detected when read attempted on sector with bad cylinder header
12	Error during final sector reformat

6.1.18.4 The Header logic exercised by this test is contained on Board 3.

6.1.18.5 Error logic is located on Board 1.

## 6.1.19 TEST 22: CRC and Header Compare Tests

- 6.1.19.1 These tests check the logic governing the detection of Header and CRC errors. Using the Write Header Data and CRC commands, erroneous Headers and CRC Checks are written in various combinations. Checks are then made for proper error bit settings.
- 6.1.19.2 All data transfers in this test are performed by the "DXFER" Subroutine, and any errors detected are indicated by the contents of the DXFER subtest location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine and associated subtest error conditions.

### 6.1.19.3 CRC and Header Compare Subtest Listing

<u>Subtest Number</u>	<u>Subtest Name/Error Conditions</u>
Ø	Error During Write Format of Erroneous Header CRC
1	No Error Detected During Read of Bad Header CRC Sector
2	Header CRC Error Bit Did Not Set During 1
3	Some Other Error Bits Erroneously Set During 1
4	Error During Write Format of Erroneous Header
5	No Error Detected During Read of Bad Header Sector
6	Sector or Cylinder or CRC Header Error Bit Not Set
7	Error During Write Format of Erroneous Header
10	No Error Detected During Read of Bad Header Sector
11	CRC or Cylinder Error Bit Not Set During Read
12	Other Error Bit Erroneously Set During Read
13	Error During Write Format of Erroneous Header
14	No Error Detected During Read of Bad Header Sector
15	No CRC Header Word 1 Error
16	Other Error Bit Erroneously Set
17	Error During Write Format of Bad Sector Header
20	No Error Detected During Read of Sector with bad Header
21	No CRC Header Error Detected
22	Other Error Bit Erroneously Set
23	Error During Final Correct Format Write

6.1.19.4 The Header and CRC logic exercised in this test is contained on Board 3.

6.1.19.5 The error register logic is contained on Board 1.

#### 6.1.20 TEST 23: Bad Sector Flag Test

This test checks the Bad Sector logic

6.1.20.1 Bad Sector bits are added to Header Word #1 of Sector 0, Head 0, Track 0, and a Read command is issued.

6.1.20.2 The disk controller Error Register (DEERR) is then checked to see if the Bad Sector Flag Bit is set.

6.1.20.3 A check is then made to insure that the controller "skipped" the flagged "defective" sector 0 and conducted a read operation on Sector 1.

This is done by comparing the data actually obtained during the read with data known to have been on Sector 1 of the disk.

6.1.20.4 All data transfers in this test are conducted by the "DXFER" Subroutine, and any errors detected are indicated by the contents of the DXFER subtest count location "DTCNT".

6.1.20.5 Bad Sector Flag Subtest Listing

<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
0	Error During Bad Sector Flag Reformat of Sector 0
1	Error During Write of Known Data to Sector 1
2	No Error Detected During Read of Sector 0 (Bad Sector Flag Set)
3	Bad Sector Flag Bit Not Set in Error Register
4	Other Error Bit Erroneously Set
5	Erroneous End Sector Field Value
6	Error During Reformat of Sector 0.
7	No Error During Timeout Test
10	Time Out Error Bit Did Not Set
11	No Error Clear on Formatter Clear Command

6.1.20.6 The Bad Sector Flag logic exercised in this test is contained on Board 3 and associated error status logic is contained on Board 1.

#### 6.1.21 TEST 24: Recalibrate Test

These tests check the RTZ command for two areas.

6.1.21.1 The first section verifies that the drive is indeed positioned on Track 0 after an RTZ.

6.1.21.2 Secondly, the conditions of the seeking flip-flops are checked (DSTAT) during and after the RTZ command.

### 6.1.21.3 Recalibrate Subtest Listing

<u>Board Being Tested</u>	<u>Subtest Number (R4)</u>	<u>Subtest Number/Error Condition</u>
1	Ø	Controller Not Ready
4	1	Selected Disk Drive Not Ready
4	2	Error During Seek Operation
2	3	Correct Seeking Flop Not Set
2	4	Other Seeking Flop Erroneously Set
2,4	5	Proper Seek Done Flop Not Set
2	6	Seeking Flop Still Set After Seek Done
3	7	Seeking Flop Erroneously Set During Seek Inhibit Read
4,3	10	Drive Did Not Go to Cylinder Ø - Error During Seek Inhibit Read of Cylinder Ø
3	11	Seek Status Flops Erroneously Set During Seek Inhibit Read
3	12	No Error Detected During Erroneous Seek Inhibit Read
3	13	Cylinder Header Error Bit Did Not Set

### 6.1.22 TEST 25: Implied Seek Test

This test verifies that the seek done flag will not be set during an "implied" seek operation and that no seek operation takes place when the Seek Inhibit Bit ( ) of the Control and Status Register is set.

- 6.1.22.1 First the implied Seek is utilized in a Read command and a check is made to see that the Seek Done flag is not set.
- 6.1.22.2 Secondly, two Read commands are given, one with a proper cylinder location and Seek Inhibit set to insure the original seek was to the proper cylinder, and the other with an erroneous cylinder address and Seek Inhibited to force a Cylinder Header Compare error.
- 6.1.22.3 All data transfers in this test are performed by the "DXFER" Subroutine, and any errors detected are indicated by the contents of the DXFER Subtest location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine and associated subtest error conditions.

#### 6.1.22.4 Implied Seek Subtest Listing

<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
Ø	Selected Disk Drive Not Ready
1	Error During RTZ Operation
2	Error During Implied Seek Read
3	Seek Done Flag Erroneously Set
4	Error During Same Track Seek Inhibit Read
5	No Error During Seek Inhibit Read from Different Track
6	No Header Error Bit Set During Read of Sub- test 5
7	No Controller Ready on Formatter Clear

6.1.22.5 The Seek Inhibit logic exercised in this test is contained on Boards 1 and 4. If Seek Done Flag in subtest 3 is set, the most probable board at fault is Board 3.

6.1.23 TEST 26: Converge/Diverge Worst Case Seek Loop Test - Address Test

- 6.1.23.1 This test sends the disk drive into a Worst-Case-Seeking loop, and is a test of the disk drive servo electronics rather than of the disk controller.
- 6.1.23.2 The seeking starts at the extreme ends of the disk cartridge (Track 0 and Track 1466g) and alternates between an increasing track address and a decreasing track address. This process continues until each track has been searched twice.
- 6.1.23.3 No data is transferred during this test.
- 6.1.23.4 If an error occurs:

- R1 = Current decreasing Cylinder Address
- R2 = Current increasing Cylinder Address
- R3 = Loop Count that error occurred on
- R4 = subtest count
- R5 = Loop Control Flag
- R5 = 1 For Increasing Cylinder Seek Cycle
- R5 = 0 For Decreasing Cylinder Seek Cycle

6.1.23.5 Converge/Diverge Worst Case Seek Loop Subtest Listing

<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Condition</u>
0	Controller Not Ready
1	Selected Disk Drive Not Ready

6.1.23.6 The logic in the disk controller principally exercised by this test is the seek logic contained on Board 2 and the disk interface logic contained on Board 4.

6.1.23.7 Disk Address Test

This section of Test 26 checks the logic of the three disk address functions:

- A. Sector
- B. Head (Surface)
- C. Cylinder

Starting at disk address ABS. 0, one sector write/read commands are issued incrementing the sector and head values until the first cylinder boundary is crossed. (CYO 0 → CYL 1) See Fig. 6.1.

Sector X = Variable

Cylinder M = 410822

fig 6.1 Disk Structure

After cylinder one is reached, transfers are issued from maximum sector and maximum head addresses. These one sector commands increment the cylinder counter each time and continue until the overrun error is detected.

The result of the above sequence is that all disk address lines, sector, head and cylinder have been exercised.

6.1.23.8 The transfers in this section of Test 26 are performed by subroutine "DXFER", and any errors detected are indicated by the subtest location "DTCNT".

6.1.24 Test 27 Functions Tested:

1. Memory Extension
2. Buss Timeout
3. Overrun Error
4. Memory Address Increment

6.1.24.1 Overrun Error

Disk address parameters are loaded as maximum values. i.e. last addressable sector, head and cylinder. A two sector write command is issued and checks are made to ensure that the overrun error was generated and that the controller aborted operations.



### 6.1.24.2 Memory Extension

One word write commands are issued with memory address loaded to a value that will increment an extension bit. Checks are made to ensure that the boundary was properly crossed. See Table 6.1

<u>MEM EXT</u>	<u>MEM ADDR</u>	<u>MEM EXT</u>	<u>MEM ADDR</u>
00	177776	01	0
01	177776	10	0
10	177776	11	0
11	177776	00	0
Before Command		After Command	

TABLE 6.1 MEMORY EXTENSION TEST

### 6.1.24.3 Buss Timeout Error

A one word write command is issued with memory address set to a nonexistent value. A check that the proper error bit is set and that no other errors are present.

### 6.1.24.4 Memory Increment Test

This test was designed to detect the failure or faulty wiring of the memory address register.

A one word write is issued from every possible starting memory address, including the memory extension bits. An illegal sector address is used to speed up the process. (Using an illegal sector aborts the command early and therefore stops the sequencer from looking for sector coincidence.)

No errors are checked or cared about in this exercise, only the incrementing of the memory address register by 2 on each transfer.

### 6.1.24.5 Test 27 Subtest Listing

<u>Boards Being Tested</u>	<u>Subtest Number</u>	<u>Subtest Name/Error Condition</u>
1,4	0	No error detected during overrun
1,4	1	Overrun error bit not set
1,3,4	2	Some other errors set
1,3	3	Error not cleared by system clear
211	4	First memory extension didn't set
211,1,3	5	If an error was present wasn't cleared by system clear or second memory extension didn't set
211,1,3	6	Memory ext. didn't overflow or error condition wasn't cleared by system clear
211,1	7	Didn't force error with buss timeout
211	10	Buss timeout not set
1,3	11	Other error with timeout
211,1	12	Error not cleared by system clear
211 (w.w.)	13	Special wirewrap test. If this subtest fails FCO #75 is missing from your 211 (wirewrap only)

6.1.24.5 Test 27 Subtest Listing Continued

<u>Boards Being Tested</u>	<u>Subtest Number</u>	<u>Subtest Name/Error Condition</u>
211	14	At this subtest we are checking the memory address incrementation if an error should occur here it would be because either the increment didn't take place at all or the mem. reg incremented to an erroneous value.

6.1.25 TEST 30: Seek/Write, Seek/Read Test - Random Transfer Test

- 6.1.25.1 This test is a disk subsystem reliability test. The drive is made to seek a Worst Case pattern and write data generated by a subroutine (PATGEN), that creates a unique array of data each time it is called.
- 6.1.25.2 After every track has been written the same seeking pattern in reverse is commanded and Read and Compare is done from each track.
- 6.1.25.3 The same converge/diverge seeking loop utilized in Test 18 is used in this test.
- 6.1.25.4 All data transfers in this test are performed by the "DXFER" Subroutine, and any errors detected are indicated by the contents of the DXFER Subtest location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine and associated subtest error conditions.

6.1.25.5 Seek Write, Seek Read Subtest Listing

This test is divided into two parts for write and read.

During the write operation R4 is incremented each time a data transfer is made, four transfers being made per cycle until the complete disk is written.

During the read operation R4 is reinitialized to 5 and then incremented for each read operation performed.

	<u>Subtest Number (R4)</u>	<u>Subtest Name/Error Conditions</u>
Write Cycle	Ø, 5, etc.	Error During First Decreasing Cylinder Disk Write
	1, 6, etc.	Error During Second Decreasing Cylinder Disk Write
	2, 7, etc.	None
	3, 10, etc.	Error During First Increasing Cylinder Disk Write
	4, 11, etc.	Error During Second Increasing Cylinder Disk Write
Read Cycle	5, 15, etc.	Error During #1 Decreasing Cylinder Read
	6, 16, etc.	Error During #1 Read Data Comparison
	7, 17, etc.	Error During #2 Decreasing Cylinder Read
	10, 20, etc.	Error During #2 Read Data Comparison
	11, 21, etc.	Error During #3 Increasing Cylinder Read
	12, 22, etc.	Error During Read Data Comparison Cycle
	13, 23, etc.	Error During #4 Increasing Cylinder Read
	14, 24, etc.	Error During #4 Read Data Comparison

6.1.25.6 This test is more of a disk drive exerciser than a test of disk controller logic.

6.1.25.7 Most probable error to occur during this test is a soft header seek error indicating a disk drive positioning problem.

6.1.25.8 The second portion of this test is also a disk subsystem reliability test. The only difference in the second part is that all disk addresses and data patterns as well as transfer sizes are random.

If more than one disk has been selected during Diagnostic startup, the unit selection will also be random.

6.1.25.9 Subtest Listing

The subtest number remains 5 throughout the test. If an error occurs refer to Section 6.1.25.4

## 6.1.26 TEST 31 : Disk Data Test

This test writes over the entire disk surface and then verifies the data by reading it back and comparing it with the original data written.

Data is written two sectors at a time and read into two sectors at a time through all of the surfaces before the cylinder register is incremented.

The data pattern used is a rotating test pattern with the exception that the first three words of every sector contain the absolute disk address.

### 6.1.26.1 Write Program

This program writes over all of the disk surfaces two sectors at a time. If an error is detected CURSEC, CURHD, and CURCYL indicate the disk address at which the failure occurred.

### 6.1.26.2 Read Program

This program reads the entire disk surface two sectors at a time. If an error is detected, CURSEC, CURHD and CURCYL indicate the disk address at which the failure occurred.

### 6.1.26.3 Boundary Crossing

Both the Write and Read routines command their operations to include Boundary Crossing, i.e. two-sector writes are issued at MAXSECTOR and continue on to increment the Head bits and Cylinder bits.

### 6.1.26.4 All data transfers in this test are conducted by the "DXFER" Subroutine, and any errors detected are indicated by the contents of the DXFER subtest count location "DTCNT".

Please refer to Appendix A for a complete description of the DXFER Subroutine and associated subtest error conditions.

### 6.1.26.5 The Data Comparison Subroutine "DATCMP" is used to perform all of the data comparisons made in the read portion of this test. Refer to Appendix C for a complete description of this subroutine and associated error conditions.

- Note:
1. The disk data test is more of a disk drive and media reliability test than a disk controller test.
  2. The test will normally stop at the detection of any error condition.
  3. If the test stops with an error the user should note the contents of the DUSH and DCYL Registers and rerun the test.
  4. Repeated test failures at the same absolute disk address is indicative of a defective sector in the media.

#### 6.1.27 TEST 32: Read and Compare Test

- 6.1.27.1 This program reads the complete disk surface and compares data received with reference data. Before entering this test, Test 31 must be run, since only Read commands are used during this exercise. Test 32 is essentially the Read portion of Test 25 modified to include a data error counter for use as a reliability test.
- 6.1.27.2 Setting Switch 7 of the console during step 4.1.7 of the starting procedure inhibits Program Halt when a Data Compare error is detected. Location "ERRCNT" is incremented each time an error is found. For explanation of Retry mode, see Section 4.2.
- 6.1.27.3 All data transfers in this test are conducted by the "DXFER" Subroutine, and any errors detected are indicated by the contents of the DXFER subtest count location "DTCNT".
- Please refer to Appendix A for a complete description of the DXFER Subroutine and associated subtest error conditions.
- 6.1.27.4 The Data Comparison Subroutine "DATCMP" is used to perform all of the data comparisons made in this test.
- Refer to Appendix C for a complete description of this subroutine and associated error conditions.

## 6.1.28 TEST 36: Simultaneous Overlapped Seek Test

6.1.28.1 Objective: This test verifies proper operation of the disk controller seek logic by initiating simultaneous seeks on multiple disk drives and verifying that:

- 1.) A seek complete interrupt is received from each disk drive commanded to seek.
- 2.) The seeking, and seek done status bits for each disk drive and seek summary status bit operate correctly.
- 3.) The seek drive identification logic correctly identifies the disk drive generating the Seek Done Interrupt.

### 6.1.28.2 Operation:

6.1.28.2.1 This test will operate on the number of disk drives from 1-4 defined to the diagnostic program by the operation via the computer switch register at the time of program initiation.

6.1.28.2.2 Initially all disk drives to be used in test are commanded to cylinder zero via repeated use of the Select and Seek Subroutine (SELASK) defined in Appendix E.

6.1.28.2.3 All disk drives utilized are then commanded to seek to the last cylinder on the disk (MAXCYL) via the Select and Seek Subroutine (SELASK) defined in Appendix E.

6.1.28.2.4 The disk controller interrupt is then enabled and the test waits for the seeks to complete via entering the WAITI Subroutine.

6.1.28.2.5 A special seek interrupt service routine (SKINT) is used for this test which checks for proper:

- .1 Seek Done Summary Bit Set
- .2 Seeking Status Bit Reset
- .3 Drive Seek Done Status Bit Set

This interrupt service routine also increments an interrupt count location (ICNT) once for each interrupt received, and enters the Seek Ident field value received in the corresponding Interrupt Flag Table (INTTBL) location.

6.1.28.2.6 The Seek End Check Subroutine (SENCHK) is then used to verify that the proper number of seek done interrupts was received and that the Seek Ident Field values previously saved in INTTBL are correct. See Appendix F for detailed description of SENCHK.

### 6.1.28.3 Subtest Listing

6.1.28.3.1 A separate subtest count is maintained for each disk drive utilized in this test.

6.1.28.3.2 The subtest count for each disk drive is contained in the corresponding drive location in the Seek Subtest Count Table (SKCNT).

6.1.28.3.3 Seek Subtest Disk Drive Values are as follows:

<u>SKCNT Table Value</u>		<u>Functional Test/Error Condition</u>
SELASK Errors	∅	Disk Drive Not Ready When Selected For RTZ Drive Seeking Status Bit Not Set at Beginning of RTZ
	1	
	2	
SKINT Errors	3	Disk Drive Not Ready When Selected For Seek Drive Seeking Status Bit Not Set at Beginning of Seek Command
	4	
	5	
SENCHK Error	6	Drive Seek Done Status Bit Not Set at Interrupt Drive Seeking Status Bit Not Reset at Interrupt Seek Done Summary Bit Not Set at Interrupt Disk Controller Error at Interrupt Disk Drive Not Ready at Interrupt
	7	
	10	
	11	Drive Seek Identification Field Incorrect at Interrupt

6.1.28.3.4 R4 Subtest Values

R4 is incremented for subtests not unique to a disk drive.  
R4 subtest listings are as follows:

<u>R4 Value</u>	<u>Function/Error Condition</u>
∅	Disk Controller Not Ready
1	Incorrect Number of Interrupts or other seek error. See SKCNT Table Subtest values.

6.1.29 TEST 37: Overlapped Seek and Data Transfer Test

6.1.29.1 Objectives

This test verifies that the Disk Controller functions properly when seek operations are overlapped with data transfer operations.

6.1.29.2 Operation

This test initiates a 8K word data transfer on the MAXCYL of unit ∅ after having initiated seeks to cylinder 5 on all other units connected to the disk controller, as defined by the operator at time of program initiation.

6.1.29.2.1 The Seek operations on all units but ∅ should complete before the 8K data transfer being conducted on unit ∅.



6.1.29.2.2 When unit  $\emptyset$  completes the data transfer:

- 1.) Seek status data should be present for one of the other drives when the transfer done interrupt is generated.
- 2.) Seek interrupts for all other drives commanded to seek will be pending.

6.1.29.2.3 The Program:

- 1.) Verifies that seek status is present and proper for one disk when transfer complete interrupt is received.
- 2.) Redirects pending seek interrupts to seek interrupt service routine.
- 3.) Verifies that seek interrupts are received for all other drives commanded to seek, and that status is proper.

NOTE:

This test requires a minimum of two disk drives for proper operation.

6.1.29.2.4 Initially all disk drives to be exercised are returned to cylinder  $\emptyset$  via executing a RTZ command via the Select and Seek Subroutine "SELASK". (See Appendix E)

6.1.29.2.5 The SELASK Subroutine is used to initiate commanded Seek Operations on all other disk drives but unit  $\emptyset$ .

6.1.29.2.6 The DXFER Subroutine is used to conduct the 8K write data transfer on MAXCYL of unit  $\emptyset$  and to check all standard controller functions for normal operation: (Please see Appendix A for description of DXFER Subroutine)

6.1.29.2.7 The Seek Interrupt Service Routine (SKINT) is used to field seek done interrupts for disk drives 8 and 3 (if used) and to check for proper drive seek status conditions. (See Appendix G for a description of the SKINT Routine)

6.1.29.2.8 The Seek End Check Subroutine (SENCHK) is used to verify that the correct number of interrupts was received and the seek identification field values received at time of interrupt are correct. (See Appendix F for description of SENCHK.)

6.1.29.3 Subtest Listing

R4 is used to indicate primary subtest values while the Seek Count Table (SKCNT) is used to catalogue subtest values associated with each disk unit.

### 6.1.29.3.1 R4 Subtest Listing

<u>R4 Value</u>	<u>Functional Test/Error Condition</u>
∅	Controller Not Ready
1	RTZ Initiate Error
2	Seek Initiate Error on Unit 1,2, or 3
3	DXFER Transfer Error on Unit ∅
4	Seek Done Summary Flag not Set at Unit ∅ transfer Complete
5	Drive Seek Done Flag Not Set at Unit ∅ Transfer complete
6	Drive Seeking Flag Set at Unit ∅ transfer complete
7	Other Disk Drive Seek Done Interrupt Errors
10	Wrong Number of Interrupts or Seek Ident. Error.

### 6.1.29.3.2 Seek Count Table SKCNT Drive Subtest Listing (Drives 1, 2 or 3)

<u>SKCNT Table Value</u>	<u>Functional Test/Error Condition</u>	
SELASK Errors {	∅	Disk Drive Not Ready When Selected for RTZ
	1	Drive Seeking Status Bit Not Set at Beginning of RTZ
	2	Disk Drive Not Ready When selected for Seek
SKINT Errors {	3	Drive Seeking Status Bit Not Set at Beginning of Seek
	4	Drive Seek Done Status Bit not Set at Interrupt
	5	Drive Seeking Status Bit Not Reset at Interrupt
	6	Seek Done Summary Bit Not Set at Interrupt
	7	Disk Controller Error at Interrupt
SENCHK Error	10	Disk Drive Not Ready at Interrupt
	11	Drive Seek Identification Field Incorrect Interrupt



Compatibility with other controllers is checked by reading a newly created CRC/ECC word and comparing it with a word previously generated at Xylogics' manufacturing facilities.

#### 6.2.3.1 Subtest Listing Test 17A

In all subtests the order of board test is

1. Board #1
2. Board #3

<u>Subtest Number</u>	<u>Error Condition</u>
∅	Formatter not ready
1	Error during reformat
2	No error during bad hdr read
3	CRC not detected
4	Other error with CRC
5	Word count incremented
6	Bus address incremented
7	Sector (DUSH) didn't increment properly
1∅	Error during reformat - Sector ∅
11	Error during reformat - Sector 1
12	Error during read of Sector
13	Error during read of Sector 1 using read hdr, data, CRC command
14	First CRC word not compatible
15	Second CRC word not compatible
16	First CRC word, second pair, not compatible
17	Second CRC word, second pair, not compatible
2∅	Reformat Sector ∅ caused error
21	No error detected during read of sector ∅
22	CRC error not detected
23	Reformat of Sector ∅ caused error
24	Error not detected during read of sector ∅
25	CRC error not detected
26	Error during reformat of sector ∅
27	Error not detected during read of sector ∅
3∅	CRC error not detected
31	Error during sector ∅ reformat
32	Error during sector ∅ read
33	First CRC word ≠∅
34	Second CRC Word ≠∅
35	Third CRC Word ≠∅
36	Fourth CRC Word ≠∅

#### 6.2.4 Test 21A ECC Detection Test

This test sequence checks the ECC detection logic of the Phoenix 211. All subtests use the ECC inhibit option that stops all correction actions that would normally occur if one encounters an ECC error. The purpose of inhibiting ECC is that at this time in testing the correction logic has not been checked.

#### 6.2.4.1 ECC Sector Format and Read Routine

This routine issues 4 disk commands during the ECC test sequence. The general function of the exercise is to force ECC errors by destroying a small section of a sector by using the write header, CRC, data and ECC command. The operator can select the area in the data field where he desires to cause the error. The steps to accomplish this are as follows:

1. Using the normal write command, write a single sector executing this command will cause ECC words to be generated.
2. Read the sector using the read format command this command reads the entire sector, including headers, header CRC's, data and ECC words.
3. Rewrite the sector after changing desired data word (from 1 to 16 bits).
4. Issue normal read on that sector to cause ECC error
5. Exit routine.

Calling sequence:

```
(X)      JSR      R5,WRTECC      ; Program call
(X+2)    .Word 0      ; Data pattern desired
(X+4)    .Word 0      ; Word position (X2)
(X+6)    .Word 0      ; Bit (S) cleared to
                                cause error
```

Note: This routine does not modify the ECC inhibit bit (bit 15 of the ECC bit pattern reg). It is therefore possible to use this call to check ECC correction as well as detection logic.

#### 6.2.4.2 Subtest Listing

In all subtests the order of board under test is:

1. Board #2
2. Board #3

<u>Subtest Number</u>	<u>Error Condition</u>
0	Error correct sector 0
1	Error not detected bit position 1
2	ECC error bit not set
3	Error not detected bit position 4096
4	ECC error bit not set
5	Error not detected bit position 2048
6	ECC error bit not set
7	Error all one's - good sector
10	Error not detected bit position 1
11	ECC error not detected
12	Error not detected bit position 4096
13	ECC error not detected
14	Error not detected bit position 2048

<u>Subtest Number</u>	<u>Error Condition</u>
15	ECC error not detected
16	Error not detected bit pos. 2048 with checkboard pattern
17	ECC error not detected
20	Error not detected bit position 2048 - reverse checkboard
21	ECC error bit not set

#### 6.2.5 Test 22A ECC Detection/Correction Test

This test is the first to check the capabilities of the ECC logic in correcting bad data as a result of non-writable spots on a disk pack.

The Phoenix 211 has commands that enable the programmer to write data on any part of the sector field including the header CRC words and the data ECC words. This option makes it very easy to check other controller functions like the ECC generation.

The following tests will try to force ECC errors in the below manner:

1. Issue a write with preselected data field  
This command is a normal write function.
2. Issue a read command to read ECC words  
This command reads all fields of the sector.
3. Issue a second write command after having changed the data field to force the ECC error.  
This command write all fields of the sector.
4. Issue a second normal read to force the ECC error
5. Later in the test procedure the ECC position and pattern registers will be checked for proper values.

#### 6.2.5.1 Subtest Listing

All subtests are exercising Bd. #1 and Bd. #3

<u>Subtest Number</u>	<u>Error Condition</u>
0	Error not detected bit position 1 bad (ECC inhibit set)
1	ECC error bit not set
2	Word count overflowed - shouldn't have
3	ECC PB $\neq 0$
4	Error not detected bit position 1 bad (ECC inhibit reset)
5	ECC error bit not set
6	ECCPB $\neq 1$
7	ECCPW $\neq 1$ (Does not equal)
10	Error not detected (11 bit error)
11	ECC error not detected
12	ECCPB $\neq 1$
13	ECCPW $\neq 3777$ (11 bit XOR)

Subtest NumberError Condition

14	Error not detected (12 bit error)
15	ECC error bit not set
16	ECCPB <del>#</del> 110041 (bit 15)
17	Error not detected during sliding 1 bit error
20	ECC error bit not set
21	ECCPB <del>#</del> 1 (count always = 1 until error bit passes 11th bit position into the sector)

6.2.6 Test 23A ECC Compatibility/Exercise

6.2.6.1 These tests check that the controller under test is generating the same CRC/ECC patterns that previous 211 controllers have generated.

6.2.6.2 A second part of this exercise is to force CRC errors on various areas of the disk and check that the ECC information generated by the ECC logic is correct. Tests TNA21 and TNA22 do similar checks however, those tests center on the first word of the data field.

6.2.6.3 Subtest NumberError Condition

0	Error during sector 0 write
1	Error during sector 0 read (This reads all fields)
2	First ECC word is bad
3	Second ECC word is bad

Boards under test are Boards #1 and #3

6.3 Test 33 Multiple CPU Exercise

6.3.1 This test is an exercise for Phoenix 211 systems that are operating with the multiple CPU option. This is the only 211 Diagnostic Test that will allow more than one CPU to be requesting the 211. The format of the test is as follows:

1. The formatter is requested. If this CPU has access before the request is made than an error is logged.
  2. A write/read and data compare routine is started and normal subroutines are used to drive this sequence.
  3. If step #2 is successful the program releases formatter and if another CPU has a request set then it should receive access.
  4. A counter of 1000 transfers is decremented and if not done, steps 1 thru 3 are repeated.
- ; \*\*\*This test can be run if a controller does not have a multiple CPU setup, steps 1 and 3 are omitted.

The disk address and the data pattern are random.

The units used are any and all that are on line and ready. (chosen randomly also)

6.3.2 In the Multiple CPU Test the subtest is not kept in the test body itself. The subroutine "REQUEST" which does all transfer and request/release functions holds the subtest count. The subtest listing for this test will refer to the code in "REQUEST".

6.3.3 Subtest Listing (REQUEST SUBROUTINE)

<u>Subtest Number</u>	<u>Error Condition</u>
Ø	Formatter ready - should be dead
1	No interrupt from request
2	No formatter ready/interrupt enable
3	Error during write/read/data compare -Look at "DTCNT" if équal to 14 then look look for data erro
4	Formatter stayed ready after release command issued.



## 7.0 Simultaneous Multiple Controller Exerciser Test

### 7.1 Objective

This test exercises "N" Phoenix 211 Disk Controllers simultaneously in order to verify that the disk controllers will operate properly in a system with other DMA devices.

### 7.2 Program Loading

This program is a stand-alone program and is supplied as a loadable tape in absolute format. Program can be loaded in any computer with 8K of memory via the standard DEC supplied absolute loader.

### 7.3 Program Operating Instructions

7.3.1 Select the number of Phoenix 211 Disk Controllers to be simultaneously exercised by entering the appropriate binary number in location "CNUM". (i.e. for two controllers, 2 should be deposited in location CNUM.)

7.3.2 Start program execution at location "START".

#### NOTE!!!!

7.3.2.1 This test assumes that the disk controller base register addresses are assigned sequentially and Mod 20 starting at location 164000.

7.3.2.2 This test, once started will conduct 50 data transfers run on each disk drive and stop at location "ENDTST".

7.3.2.3 The test will stop upon detection of any error condition.

7.3.2.4 If an error is detected:

R0 = Base address of associated controller  
R1 = Subtest No.  
R2 = Reference data value  
R3 = Actual Erroneous data value  
R4 = Program address where error was detected

7.3.2.5 Actual Disk Controller register images at time of any error are saved in the error register image table "ERRIMG".

### 7.4 Program Operation

7.4.1 The test physically conducts simultaneous 2048 word write transfers on the number of disk controllers selected by the value inserted into location "CNUM" by the operator.

7.4.2 Data from absolute memory locations 0-2048 is written on cylinder 0 of the disk drive connected to each disk controller.

7.4.3 All disk controller end parameters are verified for proper value.

#### 7.4.4 Disk Controller Addressing

Since multiple disk controllers are used, all references to disk controller registers are made indirectly via the Controller Register Address Table. The actual register addresses for a given controller are computed and entered into the address table by the Controller Base Address Setup Subroutine (ADRSTP). See Appendix I for a detailed description of this subroutine.

#### 7.4.5 Data Transfer Subroutine and Initiation

A common subroutine (XFRST) is used to initiate all data transfers in this test. This subroutine is described in Appendix J.

7.4.5.1 Initially transfers are initiated on both controllers by the program and the controller interrupts are enabled.

7.4.5.2 Subsequent data transfers on each disk controller are initiated by the common interrupt service routine at the completion of any data transfer after all controller parameters are checked for proper ending values.

#### 7.4.6 Program End Address

When the test has been successfully run, the program will stop at location "DONE".

### 7.5 Program Subtest Listing

Since the test involves the use of two or more controllers simultaneously, more parameters are required to define the controller and the associated error condition per the following:

#### 7.5.1 Disk Controller Identity (CERRNO)

The identity of the disk controller associated with any error condition is saved in location "CERRNO".

### 7.5.2 Disk Transfer Subtest Count (XFRIER)

Any Errors discovered during the initiation of any disk data transfer are identified by the subtest value save in location "XFRIER". XFRIER Subtest Values are as follows:

<u>XFRIER Value</u>	<u>Functional Test/Error Condition</u>
Ø	Selected Disk Controller Not Ready
1	Selected Disk Drive Not Ready

### 7.5.3 End Transfer Parameter Subtest Count (ENDCT)

Any error discovered at the completion of any data transfer during the check of all end parameter values is identified by the subtest value saved in location "ENDCT".

<u>ENDCT Value</u>	<u>Functional Test/Error Condition</u>
Ø	Controller Error at Interrupt
1	Word Count Register Did not Overflow
2	End Bus Address Register Value Incorrect
3	End Cylinder Address Register Value Incorrect
4	End Unit, Sector, Head Register Value Incorrect

#### NOTE:

Any error detected on one controller will cause "data late" and other errors on other disk controllers being exercised by this test since any error will cause the computer to halt.

## 8.0 Format Program Abstracts

There are three format programs available:

Test 45  
Test 47  
Test 50

For most purposes, test 45 is most convenient. It is slightly faster than test 47 and can be used for any # of sectors. Test 47 will run in 8K of memory, however the # of sectors on a surface must be evenly divisible by 4. Test 50 is useful only to add sector integrity bits to sector formats.

### 8.1.1 Test 45 Format Program

This program formats up to 32 sectors (256 words per sector) at each transfer. No operator intervention is required. It is the only format program that uses the Data Transfer routine "DXFER" therefore, if an error should occur, more data is saved than in the other format programs. 16K of memory is required to run this test.

### 8.1.2 TEST 47: Format Program #1

This program formats the disk without the operator entering any parameters. The number of sectors and the number of data words in each sector are specified in the first portion of the diagnostic. If the operator wishes to format a section or one sector of the disk surface, TEST 50 allows him to do so (Bad Sector bits, Write-Protect, etc.).

### 8.1.3 TEST 50: Format Program #2 (NON ECC ONLY)

This program is set up so that the user is able to format the entire pack or only one sector if he wishes.

After entering the program through Test Control the test will halt.

If it is desired to format the entire diskpack in the standard form shown below, raise Switch #15 on the front panel and depress CONTINUE. The program will proceed to format the disk.

#### TABLE OF STANDARD DISK PARAMETERS

(1)	#Sectors	40 (octal)	0-37
(2)	#Heads	5	0-4
(3)	#Tracks	1467 (octal)	0-1466

After the Program Halt as in the above steps, the user enters the formatting parameters in the following manner:

- (1) Enter the starting sector number.  
(All of these entries are to be set in lower byte of the switch register.)
- (2) Depress CONTINUE.
- (3) Enter ending sector number.
- (4) Depress CONTINUE.
- (5) Enter starting surface number.
- (6) Depress CONTINUE.
- (7) Enter ending surface number.
- (8) Depress CONTINUE.
- (9) Enter starting track (cylinder) number.
- (10) Depress CONTINUE.
- (11) Enter ending track number.
- (12) Depress CONTINUE.
- (13) Enter sector condition information:
  - (A) Bit 15 = 1 - Bad Sector
  - (B) Bit 15 = 0 - Good Sector
- (14) Depress CONTINUE.
- (15) Enter Write-Protect information:
  - (A) Bit 15 = 1 - Write Protect
  - (B) Bit 15 = 0 - Non-Write-Protect
- (16) Depress CONTINUE.

When the program halts and the location of the halt is the normal location of Test Control, the pack will have been formatted.

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## Appendix A

### Disk Data Transfer Subroutine

#### 1.0 Overview

The Disk Data Transfer Subroutine is the "driver" of the disk diagnostic. This subroutine is used to perform all disk data transfers whether they be read or write in nature.

#### 2.0 Linkage

All parameters defining the data transfer operation to be performed are contained in a control block. The origin address of this control block is contained in R0.

#### 3.0 Control Block Format

Entry 1 = Unit, Sector, Head Register (DUSH) Image  
2 = Bus Address Register (DCAR) Image  
3 = Word Count Register (WDCNT) Image  
4 = Cylinder Address Register (DCYL) Image  
5 = Control & Status Register (DCSR) Image

#### 4.0 Parameter Checks Made

The data transfer routine checks to insure that the disk controller goes busy, an interrupt occurs, no error occurs, and that all end disk parameters are correct.

#### 5.0 Interrupt Mode

All data transfers made by this subroutine utilize interrupts.

#### 6.0 Data Transfer Subtest Count (DTCNT)

A separate data transfer subtest count is maintained in location DTCNT to facilitate error isolation.

#### 7.0 Data Transfer Error Value Image (ERRWRD)

If an error (controller) occurs or is detected at the end of the disk operation, the image of the first error detected is saved in location -ERRWRD-.

#### 8.0 Disk Controller Register Image (ERIMGE & ERRBLK)

The image of the disk controller error register at the time of any controller error is saved in location -ERIMGE-. All Disk Controller Register images are saved in "ERRBLK" in sequential order.

## 9.0 Subroutine Return Parameters (ERRFLG) Error Flag State

- 9.1 Control is transferred to the calling routine with or without the general error flag set (ERRFLG), as appropriate.
- 9.2 If an error is detected, the general error flag ERRFLG is set and control is returned to the calling program.
- 9.3 Registers R0, R1, R4, and R5 are used and saved.
- 9.4 Registers R2 and R3 are not saved and will be returned to the calling program in the event of an Error with the reference and actual data values respectively.

## 10.0 Data Transfer Subroutine Subtest Listing

The following table shows the possible values of subtest numbers contained in location DTCNT and the corresponding failure conditions.

<u>Subtest/DTCNT Value</u>	<u>Subtest Name/Error Condition</u>
0	Controller Not Ready
1	Selected Disk Drive Not Ready
2	Controller Went Busy With No "Go" Bit Cmd.
3	Controller Did Not Go Busy With "Go" Bit Cmd.
4	Interrupt Did Not Occur Before Timeout
5	Controller Hung in "Busy" State
6	Word Count Register Did Not Overflow
7	End Bus Address Register Value Incorrect
10	End Sector Value Incorrect
11	End Head Value Incorrect
12	End Cylinder Address Value Incorrect
13	Controller Error Bit Set

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## Appendix B

### Read, Write, Comparison Subroutines

1.0 This subroutine writes the specified data block onto the specified device at the specified address. The routine then reads the written data back from the disk and compares the data read with the original data written.

2.0 Calling Sequence:

```
JSR R5,WRC
```

3.0 At the time of the call, R0 must contain the origin address of the control block defining the parameters of the operations to be performed.

4.0 Required Control Block Format is as follows:

```
Entry 1 = Desired DUSH Image
       2 = Blank (Used by WRC for DCAR Image)
       3 = Desired DWDCNT Image
       4 = Desired DCYL Image
       5 = Blank (Used by WRC for DCSR CMD Image)
```

5.0 Return Parameters

5.1 1. Normal return is with general error flag reset.

5.2 2. If an error is detected during any operation, control is transferred to user with the error flag set. In this case, error information is contained in the DXFER or DATCMP error flags as appropriate.

5.3 Write Transfer Error Flag (WRTERR)

If an error is detected during the write data transfer by DXFER, the "WRTERR" location is incremented to a non zero state.

5.4 Read Transfer Error Flag (RDERR)

If an error flag is detected during the read data transfer by DXFER, the "RDERR" location is incremented to a non zero state.

5.5 Data Comparison Error Flag (CMPCNT)

If a data comparison error is detected by the Data Comparison Subroutine "DATCMP":

- 1.) The "CMPCNT" location contains the comparison word count value at the time the error was detected.
- 2.) R2 contains the correct or reference dates.
- 3.) R3 contains the erroneous actual data.



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## Appendix C

### Data Comparison Subroutine

- 1.0 This subroutine compares data obtained from the disk during any disk read operation in the input data buffer (IDBUFI) with the reference data actually written onto the disk and contained in the output data buffer (ODBUF).
- 2.0 At entry R0 contains the number of words that are to be compared.
- 3.0 If an error occurs:
  - 3.1 The error flag is set and control is transferred back to the calling program.
  - 3.2 The "CMPCHT" count location contains the comparison word count value when the error was detected.
  - 3.3 R2 contains the correct or reference data value.
  - 3.4 R3 contains the actual data value.

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Appendix D

Individual Test Select Switch Register Values

<u>Test No.</u>	<u>Test Name</u>	<u>Test Select Value</u>
Ø	Register Initialization	Ø
1	Register Load and Read	401
2	Register Sliding Ones	1002
3	Register Sliding Zero	1403
4	Register Error and Status Register	2004
5	Unit Select	2405
6	Seeking	3006
7	Interrupt Logic	3407
10	One Word Write	4010
11	One Sector Write	4411
12	One Sector Read	5012
13	Incrementing Word Count Write	5413
14	One Sector Write, Read, and Compare	6014
15	Write, Read, Compare	6415
16	Write Protect	7016
17	Header Override	7417
20	Write Protect Override	10020
21	Header Write Command	10421
22	CRC/Header Test	11022
23	Bad Sector Flag Test	11423
24	RT Æ Test	12Ø24
25	Implied Seek Test	12425

<u>Test No.</u>	<u>Test Name</u>	<u>Test Select Value</u>
26	Converge/diverge seeking test	13026
27	Mem. Ext. - Buss Timeout Test	13427
30	Converge/diverge write/read test	14030
31	Disk Data Test (Entere Disk Write/Read)	14431
32	Disk Reliability Read	15032
33	Multiple CPU Exercise Test	15433

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## Appendix E

### Select and Seek Subroutine

#### 1.0 Objective

This subroutine selects a disk drive based on the unit number contained in R0 at the time of the program call, and then issues a seek or RTZ command to the selected disk.

#### 2.0 Usage

This subroutine is used in the Overlapped Seek Tests (TN36 & TN37).

#### 3.0 Calling Sequence

(X)	JSR	R5, SELASK	;Program Call
(X+2)	Word	CYL	;Cylinder Address
(X+4)	Word	CMD	;Seek or RTZ CMD

R0 - Disk Drive Number

#### 4.0 Error Conditions

- 4.1 The general Error flag is set if the selected disk drive is not ready or if the associated seeking status flag is not set when the disk is commanded to seek or RTZ.
- 4.2 This subroutine increments the subtest count location associated with the specified disk drive in the SKCNT Table.

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## Appendix F

### Seek End Check Subroutine

#### 1.0 Objective

This subroutine is used to verify:

- 1.1 That all of the drives commanded to seek did generate a seek done interrupt.
- 1.2 That the right number of interrupts were received.
- 1.3 That the seek ident value generated by each drive was correct.

#### 2.0 Usage

This Subroutine is used in tests 36 & 37, the overlapped seek tests.

#### 3.0 Calling Sequence

JSR R5, SENCHK

R0 - Number of Disk Drives

#### 4.0 Error Conditions

- 4.1 If an error is detected the general error flag is set.
- 4.2 The disk drive subtest count located in the "SKCNT" Table is incremented if the Seek Identification Field value for that drive is correct.
- 4.3 R4 is incremented if the correct number of seek complete interrupts was received.

# Phoenix 211 Controller Diagnostic Manual

## Appendix G

### Seek Interrupt Service Routine

#### 1.0 Objective

This interrupt service routine is used to verify that all of the seek parameters are correct when seek done interrupts are received at the end of commanded seek operations.

This interrupt service routine specifically

1. Extracts the unit No of the interrupting disk drive.
2. Verifies that the drive seeking status flag is reset.
3. Verifies that the dirve seek done status flag is set.
4. Verifies that the seek done summary flag is set.
5. Selects the interrupting disk drive.
6. Verifies that there is no controller errors.
7. Verifies that the interrupting drive is ready.
8. Issues a NOP CMD to drive to clear out seek done flag.
9. Sets interrupt flag in table location determined by the seek ident value at time of interrupt.

#### 2.0 Usage

This interrupt service routine is used for tests 36 & 37, the overlapped seek logic tests.

#### 3.0 Error Conditions

- 3.1 The subtest count value in the SKCNT Table for the interrupting disk drive is incremented for each subtest conducted by this routine.
- 3.2 If any error is detected, the general error flag is set.

# Phoenix 211 Controller Diagnostic Manual

## Appendix H

### Format Subroutine

#### 1.0 Objective

This subroutine establishes a known one sector (256 words) data pattern in the Output Data Buffer used for most Write disk data transfer operations.

#### 2.0 Resultant Sector Buffer Format

A 256 word buffer will be formatted per the following by this subroutine.

<u>Buffer Word Number</u>	<u>Content</u>
1 - 64	Decreasing binary count value starting at 100 <sub>8</sub> and going to 1.
65 - 128	(177400) Low order byte = 0, High Order Byte = all 1's
129 - 192	(125125) Low order byte = 125, High Order Byte = 252
193 - 208	Rotating Sliding zero Value Sliding from Bit 5 to Bit 15
209 - 224	Rotating Sliding One Value from Bit 0 to Bit 15
225 - 240	Rotating Sliding zero Value sliding from Bit 0 to Bit 15
241 - 256	Rotating Sliding One Value sliding from Bit 0 to Bit 15

#### 3.0 Calling Sequence

JSR R5, FORMAT

R1 = Origin Address of Buffer to be Formatted

#### 4.0 Error Conditions

None

# Phoenix 211 Controller Diagnostic Manual

## Appendix I

### Multiple Controller Register Address Setup Subroutine

#### 1.0 Objective

This subroutine computes the proper base register addresses for the disk controller defined by the value on top of the stack after the calling sequence. The computer addresses are then loaded into the controller register address table.

#### 2.0 Usage

This subroutine is used by the Simultaneous Multiple Controller Exerciser Test.

#### 3.0 Calling Sequence

```
JSR R4, ADRSTP
```

R4 = disk controller number (1,2,3, etc.)

#### 4.0 Error Conditions

None



# Phoenix 211 Controller Diagnostic Manual

## Appendix J

### Disk Transfer Start Subroutine

#### 1.0 Objective

Initiate all data transfers performed during the Simultaneous Multiple Disk Controller Test.

#### 2.0 Calling Sequence

JSR R5, XFRST

- 1.) R5 = specified disk controller
- 2.) R0 must contain origin address of control block at entry.
- 3.) Parameters defining data transfers are contained in a control block of origin address X per the following:

(X) = Desired DUSH Image  
(X+2) = Desired DBAR Image  
(X+4) = Desired DWCNT Image  
(X+6) = Desired DCYL Image  
(X+8) = Desired DCSR Image

#### 3.0 Error Conditions

3.1 Controller Not Ready

3.2 Selected Disk Drive Not Ready

3.3 If an error occurs, the general error flag is set and R2 contains the reference value while R3 contains the actual value.

# Phoenix 211 Controller Diagnostic Manual

## Appendix K

### Multiple Controller Test Interrupt Service Routine

#### 1.0 Objective

This routine services all of the transfer complete interrupts generated by all of the disk controllers exercised in the Multiple Disk Controller Exerciser Test. This service routine specifically:

1. properly sets up the controller register addresses for the interrupting disk controller;
2. verifies proper end controller parameter values;
3. verifies no error occurrence;
4. initiates a new data transfer on the selected controller;
5. exits via an RTI instruction.

#### 2.0 Error Conditions

If an error occurs:

- 2.1 The associated disk controller indent is saved in location "CERRNO".
- 2.2 The selected controller register images are saved in "ERRBLK".
- 2.3 The error condition is identified by the subtest number saved in location "ENDCT".  
ENDCT subtest values and associated error conditions are as follows:

<u>ENDCT VALUE</u>	<u>FUNCTIONAL TEST/ERROR CONDITION</u>
Ø	Controller Error Condition at Interrupt
1	Word Count Register did not overflow
2	End Bus Address Register Value incorrect
3	End Cylinder Address Register value incorrect
4	End Unit, Sector, Head Register value incorrect

Appendix L

Typical Register Address Assignments \* - Phoenix 211

**CONTROL AND STATUS REGISTER 164000**

Error Sum.	Seek Inhibit	Memory Extension	DSE	DSL	SV <sup>1</sup>	SV	Done (Ready)	Interrupt Enable	Command				Go		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**UNIT-SECTOR-HEAD REGISTER 164002**

0	0	Unit No.	Head				Sector								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**BUSS ADDRESS REGISTER 164004**

Buss Address															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**WORD COUNT REGISTER 164006**

Word Count															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**CYLINDER ADDRESS REGISTER 164010**

0	0	0	0	0	0	Cylinder Address									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**DISK STATUS REGISTER 164012 (READ ONLY)**

Drive Ready	Disk Port Busy	Disk Write Protected		Drive 3 Seeking	Drive 2 Seeking	Drive 1 Seeking	Drive 0 Seeking	Seek Done	*Request Flag Status	Seek 3 Done	Seek 2 Done	Seek 1 Done	Seek 0 Done	Drive Done	Seek ID No.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**ERROR STATUS REGISTER 164014 (READ ONLY)**

Bus Timeout Error	Write Check Error	Bad Sector Found	Disk Drive Not Ready	Fault Error	Seek Error	Time Out Error	CRC Error	Data Late	Non Existent Sector	Non Existent Cylinder	Non Existent Head	Overrun Error	Sector Write Protected	Sector/Head Header Compare Error	Track Header Compare Error
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

\* See Configuration Chart for actual Register Addresses

Appendix M

DECIMAL TO OCTAL CONVERSION TABLE

DECIMAL		OCTAL	DECIMAL		OCTAL
0	=	0	26	=	32
1	=	1	27	=	33
2	=	2	28	=	34
3	=	3	29	=	35
4	=	4	30	=	36
5	=	5	31	=	37
6	=	6	32	=	40
7	=	7	33	=	41
8	=	10	34	=	42
9	=	11	35	=	43
10	=	12	36	=	44
11	=	13	37	=	45
12	=	14	38	=	46
13	=	15	39	=	47
14	=	16	40	=	50
15	=	17	41	=	51
16	=	20	42	=	52
17	=	21	43	=	53
18	=	22	44	=	54
19	=	23	45	=	55
20	=	24	46	=	56
21	=	25	47	=	57
22	=	26	48	=	60
23	=	27	49	=	61
24	=	30	50	=	62
25	=	31			



PHOENIX 211 DISK

DIAGNOSTIC MONITOR MANUAL

(Supplement To Diagnostic Manual 1043-05/06)

2/21/78

## TABLE OF CONTENTS

### SECTION

1. General Description
2. Operation
3. Command Table
4. Individual Command Descriptions
5. Disabling The Monitor

## 1.0 General Description

The Phoenix 211 Diagnostic Monitor is used to facilitate operation of the Phoenix Disk diagnostics. The monitor allows the operator to change all disk and controller parameter selections as well as test sequences via a terminal. Phoenix 211's delivered prior to March 1978 do not have diagnostics with this feature. The diagnostic tests have not been modified and the monitor version remains operable via the computer switch register.

## 2. Operation

### 2.1 Active Keyboard Operation

2.1.1 The Phoenix 211 diagnostic should be loaded via the normal procedure described in the diagnostic manual. Startup is by loading the starting address (3000) and depressing start.

2.1.2 The program will initialize the keyboard and printer (keyboard printer), print the test program heading and request the operator to enter the date.

2.1.3 After the date has been properly entered, a prompt will appear and the operator can now issue one of 13 different commands. The commands are described in detail in section 4.

2.1.4 During a test sequence the operator can produce a test halt by typing a control C. The monitor will only accept an interrupt generated by a control C character.

When the monitor detects a control C during testing it saves the CPU registers and enters The Command Line Interpreter. At this point, the operator can examine the test progress and 211 controller registers if he wishes. If the operator desires to continue testing, without re-initializing the pass count, the Continue "CO", command can be used.

## 3. Command Table

Table 3.1 is the valid command table for the Phoenix 211 Monitor. Typing an "H" (CR) after startup will produce this table on the keyboard printer.

Table 3.1 Monitor Commands

	<u>Command Mnemonics</u>	<u>Description</u>
A.	G	Go command - starts testing
B.	DK	Disk Parameters
C.	TS	Test Sequence
D.	FT	Controller parameters
E.	PR	Test progress report
F.	DA	Date
G.	SC	Scope Loop Parameters
H.	PR	Controller Register Read
I.	H	Help
J.	TE	Test Error Conditions
K.	FO	Format
L.	CO	Continue Testing



## 4.0 Individual Command Descriptions

### 4.1 Command Format

- 4.1.1 All command requests are terminated by a carriage return. (CR).
- 4.1.2 All numerical responses must be in octal
- 4.1.3 A response can be defaulted by typing only (CR) to a query.
- 4.1.4 A parameter select command can be terminated by typing an E (CR).
- 4.1.5 The default answer for numerical entries is outputted during selection.
- 4.1.6 The default answer for yes - no questions is the last selected or NO initially.

### 4.2 Command Descriptions

#### 4.2.1 GO command

Mnemonic: G

Description: The "go" command starts testing at the specified test and drive sequence start point.

After executing this command the monitor is disabled

#### 4.2.2 Disk Command

Mnemonic: DK

Description: The Disk command allows 4 disk oriented parameters to be loaded.

1. Maximum sector
2. Maximum head
3. Maximum cylinder
4. Words per sector

#### 4.2.3 Test Sequence Command

Mnemonic: TS

Description: The test command allows the operator to define the test sequence he desires: there are 8 parameters.

1. Starting test number
2. Ending test number
3. Starting drive number
4. Ending drive number
5. Continuous testing mode
6. Repeat on error mode
7. Inhibit pass printout
8. Inhibit error printout

#### 4.2.4 Controller Command

Mnemonics: FT

Description: The controller command allows selection of 5 controller oriented parameters.

1. DCSR or base address
2. Interrupt vector
3. ECC option
4. Multiple CPU option
5. Auto-switch option

#### 4.2.5 Progress Report

Mnemonic: PR

Description: The progress command outputs current testing values. This command is primarily used when a control "C" has been typed during testing. If the operator halts the CPU and restarts the monitor, the values will still be valid. i.e. current test number and pass count are only reset during the "go" command. 5 messages are outputted:

1. Date
2. Pass count
3. Starting test number
4. Ending test number
5. Current test number
6. Error flag

#### 4.2.6 Date Command

Mnemonic: DA

Description: The date command requests the operator to enter the date. It must be in the form:

DD-MMM-YY

#### 4.2.7 Scope Mode

Mnemonic: SC

Description: The Scope command allows four of the five possible registers to be selected for a scope loop. The code for the actual scope loop is the subroutine labeled "DXFER" which is described in Appendix A of the Diagnostic manual. 1043/05/06

This subroutine is interrupt driven and the monitor is lost after executing the Scope command.

The disk address parameters must be loaded in image fom i.e., a write command = 6. For aid in selecting parameters refer to the Phoenix 211 Programming Reference Manual.

#### 4.2.8 Register Read Command

Mnemonic: RR

Description: The Register Read command outputs the contents of the seven (or 9, if Error Correction Controller) Phoenix 211 registers.

#### 4.2.9 Help Command

Mnemonic: H

Description: The Help command lists the command table and explains a few of the operating procedures.

#### 4.2.10 Test Error Conditons Command

Mnemonic: TE

Description: This command prints the Error conditions that were reported upon failure of testing previously by the monitor. This command is useful when error conditions in the 211 controller have been cleared by an I/O reset pulse. (Start Key). The format of this printout is shown below.

```
Failing drive number = ##  
Failing test number  = ##  
Reference data       = ##  
Actual data          = ##  
Subtest number      = ##
```

If the error is a data error the output will be a message saying "Data Error"

If any other error occurs the controller register will be outputed.

#### 4.2.11 Format Command

Mnemonic: FO

Description: The format command allows you to format any drive (0-3) however only one drive for each command call. The command responses\* are below:

```
Disk unit to be formatted ### 0 (CR)  
Are you sure??? Y or N Y (CR)
```

#### 4.2.12 Continue Command

Mnemonic: CO

Description: The Continue command is useful in only one case: after testing has been halted using a control C. A Return to testing will be generated if this condition is satisfied, all other uses of the continue command are illegal and may result in destruction of memory contents.

\* Operator responses are underlined

## 5.0 Disabling The Monitor

5.1 The Phoenix Monitor can be disabled by depositing a 0 into location "TTYPUT" (memory address 1104<sub>8</sub>) after the diagnostic has been loaded into memory.

The program can now be run via the CPU's switch register or via the console emulator.

## 5.2 Non Terminal Operation

5.2.1 Instructions for operating the Phoenix diagnostics via the switch register are located both on the front section of the Diagnostic's assembly listing and in the Diagnostic Manual, #1043/05/06.



1	:	
2	:	
3	:	
4	:	
5	:	PHOENIX 211 DISK DIAGNOSTIC
6	:	
7	:	*****
8	:	
9	:	COPYRIGHT 1975
10	:	XYLOGICS DEM COMPONENTS GROUP
11	:	42 THIRD AVENUE
12	:	BURLINGTON MASS 01803
13	:	
14	:	GERARD JOHNSON JR.
15	:	
16	:	617-272-8140
17	:	
18	:	REV E 19-APR-78
19	:	
20	:	
21	:	
22	:	TABLE OF CONTENTS
23	:	*****
24	:	
25	:	
26	:	SECTION 1 OPERATING INSTRUCTIONS
27	:	
28	:	SECTION 2 OPTIONAL MODES OF OPERATION
29	:	
30	:	2.1 ECC CONTROLLERS
31	:	2.2 AUTO SWITCH OPTION
32	:	2.3 MULTIPLE COMPUTER PORT OPTION
33	:	2.4 NON CONSOLE MODE(NO SWITCH REG.)
34	:	2.5 NO TEST INPUT MODE
35	:	2.6 FORMATTING INSTRUCTIONS
36	:	
37	:	SECTION 3 REGISTER ASSIGNMENT TABLE
38	:	
39	:	SECTION 4 DISK/CONTROLLER ASSIGNMENT TABLE
40	:	
41	:	SECTION 5 MIXED CONSTANT TABLE
42	:	
43	:	SECTION 6 TEST PARAMETER CONSTANT TABLE
44	:	
45	:	SECTION 7 TEST ORIGIN ADDRESS TABLES
46	:	
47	:	SECTION 8 REGISTER MASKS/PATTERN TABLES
48	:	
49	:	SECTION 9 ERROR HALT REGISTER IMAGE TABLE
50	:	
51	:	SECTION 10 TEST CODE
52	:	
53	:	
54	:	
55	:	
56	:	
57	:	



58	;	
59	;	
60	;	8. DEPRESS THE CONTINUE SWITCH ON THE COMPUTER CONSOLE.
61	;	
62	;	9. THE COMPUTER WILL THEN EXECUTE ALL TESTS SPECIFIED
63	;	ON ALL DISKS SPECIFIED. IT WILL ALSO STOP IF
64	;	ANY ERROR IS ENCOUNTERED UNLESS THE FOLLOWING
65	;	SWITCH SETTINGS ARE USED:
66	;	
67	;	
68	;	(A). BIT 15 SWITCH RAISED DURING STEP 7 WILL
69	;	INHIBIT PROGRAM HALT IF ANY ERROR OCCURS. THE
70	;	PROGRAM CONTINUES TESTING STARTING WITH THE
71	;	NEXT CONSECUTIVE TEST. IF THE USER IS REPEATING
72	;	ONE OR MORE TESTS THE PROGRAM ATTEMPT THAT SEQUENCE
73	;	INDEFINITELY INCREMENTING LOCATION ERROR EACH TIME
74	;	AN ERROR OCCURS.
75	;	
76	;	
77	;	(B). BIT 7 SWITCH RAISED DURING STEP 7 WILL
78	;	INHIBIT PROGRAM HALT WHEN A DATA COMPARE ERROR
79	;	IS ENCOUNTERED. LOCATION ERRCNT IS INCREMENTED
80	;	EACH TIME A COMPARE IS BAD. IF SWITCH 15 IS LEFT OFF
81	;	IN THIS MODE THE PROGRAM WILL STOP ON A CONTROLLER
82	;	ERROR (ERRORS FLAGGED BY REGISTER DERR).
83	;	
84	;	
85	;	
86	;	(C). BIT 14 SWITCH RAISED DURING STEP
87	;	7 WILL ALLOW THE PHOENIX 211 TO RETRY CERTAIN SOFT
88	;	ERRORS. THESE SOFT ERRORS CAN BE DATA OR CONTROLLER
89	;	IN NATURE IE. A HEADER COMPARE ERROR WOULD BE
90	;	CONSIDERED A SOFT CONTROLLER ERROR. IF AFTER 8
91	;	ATTEMPTS ON A DATA ERROR OR 4 ON A CONTROLLER ERROR
92	;	THE ERROR STILL EXISTS IT IS RECLASSIFIED TO A HARD ERROR
93	;	AND THE PROGRAM WILL HALT (IF BITS 7 AND 15 ARE OFF).
94	;	EACH TIME A SOFT DATA ERROR IS ENCOUNTERED LOCATION
95	;	ERRCNT IS INCREMENTED. THE COUNT FOR SOFT CONTROLLER
96	;	ERRORS IS KEPT IN LOCATION SOFERR. WHEN A HARD DATA ERROR
97	;	IS FOUND LOCATION HERCNT IS USED RATHER THAN THE
98	;	GENERAL ERROR FLAG ERRFLG SO THAT THE MODE USING
99	;	SWITCH 7 STILL OPERATES.
100	;	
101	;	
102	;	SWITCH SETTINGS
103	;	-----
104	;	
105	;	
106	;	15 7 14 EFFECT
107	;	-----
108	;	0 0 0 PROGRAM WILL HALT ON ANY ERROR
109	;	
110	;	0 0 1 PROGRAM WILL RETRY SOFT ERRORS AND
111	;	STOP ON ANY HARD ERRORS
112	;	0 1 0 PROGRAM WILL NO STOP ON ANY DATA ERRORS
113	;	BUT WILL STOP ON CONTROLLER ERRORS
114	;	0 1 1 PROGRAM WILL STOP ONLY ON HARD ERORS



6	115					
7	116					
8	117		1	0	0	PROGRAM WILL NOT STOP ON ANY ERRORS NO RETRY OR DATA ERROR DISCRIMINATION
9	118		1	0	1	PROGRAM WILL RETRY AND NOT STOP ON ANY ERRORS.
10	119					
11	120		1	1	0	NO RETRY NO STOP ON ANY ERRORS
12	121					
13	122		1	1	1	NO STOP ON ANY ERRORS AND INCREMENTING DATA ERROR COUNTER
14	123					
15	124					
16	125					
17	126					
18	127					
19	128					
20	129					
21	130					
22	131					10. IF THE COMPUTER HALTS FOR AN ERROR:
23	132					R0 CONTAINS THE DISK DRIVE NUMBER
24	133					R1 CONTAINS THE TEST NUMBER
25	134					R2 CONTAINS THE CORRECT OR REFERENCE DATA
26	135					R3 CONTAINS THE ACTUAL DATA RECEIVED
27	136					R4 CONTAINS THE SUBTEST NUMBER
28	137					R5 CONTAINS THE ADDRESS WHERE THE ERROR WAS DETECTED.
29	138					
30	139					
31	140					11. TEST STARTING ADDRESS IS "START"
32	141	000002 003000				.WORD START
33	142					
34	143					12. ERROR HALT LOCATION IS "STOP8"
35	144					
36	145	000004 003474				.WORD STOP8
37	146					
38	147					
39	148					13. NORMAL TEST HALT IS "HALT8"
40	149					
41	150	000006 003776				.WORD HALT8
42	151					
43	152					14. AFTER HAVING SET UP PARAMETERS, THE OPERATOR CAN RESTART AT ADDRESS TNINTA AND THE PROGRAM WILL START RUNNING THE TEST SEQUENCE PREVIOUSLY SET UP EITHER THROUGH THE SWITCH REGISTER OR BY DEPOSITING INTO THE START AND END TEST LOCATIONS.
44	153					
45	154					
46	155					
47	156					
48	157					
49	158					
50	159	000010 004000				.WORD TNINTA
51	160					
52	161					
53	162					
54	163					*****
55	164					*****
56	165					
57	166					
58	167					
59	168					
60	169					
61	170					SECTION 2
62	171					2.1 ERROR CORRECTION CONTROLLERS

172  
173  
174  
175  
176  
177  
178  
179  
180  
181  
182  
183  
184  
185  
186  
187  
188  
189  
190  
191  
192  
193  
194  
195  
196  
197  
198  
199  
200  
201  
202  
203  
204  
205  
206  
207  
208  
209  
210  
211  
212  
213  
214  
215  
216  
217  
218  
219  
220  
221  
222  
223  
224  
225  
226  
227  
228

000012 001074

000014 001100

\*\*\*\*\*

211 CONTROLLERS WITH THE ECC OPTION REQUIRE  
A SEPARATE TEST SEQUENCE DUE TO  
DIFFERENT HEADER AND CRC WORD CONFIGURATIONS  
TO OPERATE THIS PROGRAM ON SUCH A SYSTEM THE  
OPERATOR MUST SET A FLAG CALLED "ECC"  
THE WORD BELOW CONTAINS THE MEMORY ADDRESS OF "ECC"  
IF ECC IS INCORPORATED DEPOSIT A "1" INTO "ECC".

THERE ARE TWO TEST TABLES ON THIS LISTING  
AND ONE OF THEM IS DEDICATED TO ECC.  
.WORD ECC

2.2 AUTO-SWITCH OPTION

14. SYSTEMS EQUIPTED WITH PHOENIX AUTO SWITCH  
OPTION BOARD CAN BE TESTED USING LOCATION AUTOSW:  
(A). BEFORE SYSTEM POWER UP, INSTALL DATA  
CABLE INTO CONNECTOR ON PHOENIX 211  
BOARD #2 (CONSULT AUTO SWITCH MANUAL)  
(B). POWER UP SYSTEM AND AFTER LOADING  
(B). POWER UP SYSTEM AND LOAD 211 DIAGNOSTIC  
(C). START NORMAL OPERATING PROCEDURES  
AND DURING STEP 7 RAISE CONSOLE SWITCH 13  
(D). IF RUNNING IN A NO-INPUT MODE OR NONCONSOLE  
MODE DEPOSIT A "1" IN LOCATION "AUTOSW"

.WORD AUTOSW

\*\*\*\*\*

2.3 MULTIPLE COMPUTER PORT OPTION

=====

TO USE THIS PROGRAM TO TEST PHOENIX 211'S  
WITH THE MULTIPLE COMPUTER PORT OPTION, DEPOSIT A "1" INTO  
CORE LOCATION "MULCPU" AND USE NORMAL OPERATING PROCEDURES.

2.3.1 SINGLE CPU TESTING

IN MULTIPLE CPU MODE, WITH THE EXCEPTION OF TEST 33, ONLY ONE CPU CAN  
BE EXERCISED AT A TIME. THIS IS DUE TO THE DURATION OF  
TIME THAT SOME TESTS REMAIN IN CONTROL OF THE FORMATTER.  
IN NORMAL OPERATING SYSTEM ENVIRONMENTS THE CPU WOULD BE  
RELINQUISHING POSSESSION OF THE FORMATTER WHEN

229	;	NO DISK OPERATIONS ARE QUEUED. DURING THESE DIAGNOSTICS
230	;	THE FORMATTER IS NEVER FORCED IDLE THEREFORE A COMPETING
231	;	CPU RUNNING 211 DIAGNOSTICS WOULD TIME OUT AS A RESULT
232	;	OF DIAG. REQUEST LOOPS.
233	;	
234	;	
235	000016 001076	.WORD MULCPU
236	;	
237	;	
238	;	2.3.2 SIMULTANEOUSLY RUNNING CPU'S
239	;	
240	;	
241	;	TO EXERCISE TWO OR MORE CPU'S RUNNING ON
242	;	ONE 200 FORMATTER TEST 33 HAS BEEN ADDED TO
243	;	THE DIAGNOSTIC PROCEDURE. THIS EXERCISE
244	;	ENABLES THE OPERATOR TO DETECT ANY CONFLICT
245	;	THAT MIGHT OCCUR BETWEEN REQUESTING CPU'S.
246	;	
247	;	A DESCRIPTION OF THE TEST FORMAT IS LOCATED
248	;	PRECEDING THE ACTUAL TEST CODE.
249	;	
250	;	
251	;	*****
252	;	
253	;	2.4 NON CONSOLE MODE
254	;	*****
255	;	
256	;	
257	;	1. TO OPERATE DIAGNOSTIC WITHOUT A SWITCH REGISTER
258	;	DEPOSIT A NON ZERO NUMBER INTO LOCATION "NONCON"
259	;	AND ENTER TEST PARAMETERS INTO APPROPRIATE LOCS.
260	;	STARTING WITH LOCATION "STPTN".
261	;	
262	;	
263	;	
264	000020 001244	.WORD NONCON
265	;	
266	;	
267	;	
268	;	2.5 NO TEST INPUT MODE
269	;	*****
270	;	
271	;	
272	;	
273	;	TO OPERATE TESTS WITHOUT ENTERING NEW TEST DATA
274	;	EACH PASS OR STARTUP, DEPOSIT A "1" IN LOCATION
275	;	"NINPUT" AND START OPERATION AT LOCATION "START"
276	;	
277	;	THE TEST(S) AND DISK(S) RUN WILL BE THOSE
278	;	ENTERED IN LOCATIONS "STPTN" THROUGH "STROSK".
279	;	
280	;	
281	000022 001242	.WORD NINPUT
282	;	
283	;	
284	;	2.6 FORMATTING INSTRUCTIONS
285	;	*****

286				
287				
288				1. ALL CONTROLLERS CAN USE FORMATTING PROGRAM - TEST 45
289				THIS PROGRAM RUNS IN 16K OF MEMORY.
290				
291				2. ALL CONTROLLERS THAT HAVE A TOTAL SECTOR COUNT THAT IS
292				DIVISIBLE BY 4 CAN USE FORMATTING PROGRAM - TEST 47
293				THIS PROGRAM RUNS IN 8K OF MEMORY.
294				
295				3. ALL NON ECC CONTROLLERS THAT WISH TO ADD SECTOR INTEGRITY
296				BITS TO CERTAIN OR ALL SECTORS CAN USE FORMATTING PROGRAM
297				TEST 50 . THIS PROGRAM RUNS IN 8K OF MEMORY.
298				
299				
300				.TITLE SMDIA.MAC
301				
302				
303	000000		R0=X0	
304	000001		R1=X1	
305	000002		R2=X2	
306	000003		R3=X3	
307	000004		R4=X4	
308	000005		R5=X5	
309	000006		SF=X6	
310	000007		PC=X7	
311	177570		CSWR=177570	CONSOLE SWITCH REGISTER
312	177776		PS=177776	PROGRAM STATUS REGISTER
313	000012		LF=12	LINE FEED
314	000015		CR=15	CARRIAGE RETURN
315				
316				
317				
318				
319				
320				
321				.INTERRUPT VECTOR ASSIGNMENTS
322				
323				
324	000000		.ASECT	DEFINE ASSEMBLY AS ABSOLUTE
325			.ENABL AMA	DEFINE ABSOLUTE ADDRESSING
326	000000	000002	+2	ERRONEOUS INTERRUPT VECTOR TRAP
327	000002	000000	WORD 0	H
328		000004	=4	BUS ERROR TRAP LOCATION
329	000004	000006	WORD 6	
330	000006	000000	WORD 0	BUS ERROR WILL HALT AT 6
331	000010	000012	WORD 12	ILLEGAL INSTRUCTION TRAP
332	000012	000000	WORD 0	ILLEGAL INSTRUCTION HALTS AT 12
333	000014	000016	+2	ERRONEOUS INTERRUPT VECTOR TRAP
334	000016	000000	WORD 0	
335	000020	000022	+2	ERRONEOUS INTERRUPT VECTOR TRAP
336				
337				
338				

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001000

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REGISTER ASSIGNMENTS WILL START HERE

SECTION 3 REGISTER ASSIGNMENT TABLE

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13	001000	164000	DCSR:	WORD 164000	CONTROL AND STATUS REGISTER
14	001002	164002	DUSH:	WORD 164002	UNIT SECTOR HEAD REGISTER
15	001004	164004	DCAR:	WORD 164004	CORE ADDRESS REGISTER
16	001006	164006	DWCNT:	WORD 164006	WORD COUNT REGISTER
17	001010	164010	DCYL:	WORD 164010	CYLINDER ADDRESS REGISTER
18	001012	164012	DSTAT:	WORD 164012	DISK STATUS REGISTER
19	001014	164014	DERR:	WORD 164014	CONTROLLER ERROR REGISTER
20	001016	164016	ECCPB:	WORD 164016	ECC BIT POSITION REGISTER
21	001020	164020	ECCPW:	WORD 164020	ECC WORD PATTERN REGISTER
22	001022	000000		WORD 0	BLANK
23	001024	000000		WORD 0	BLANK
24	001026	000000		WORD 0	BLANK
25	001030	000000		WORD 0	BLANK
26	001032	000000		WORD 0	BLANK
27	001034	164036	DSCAR:	WORD 164036	STRIP CORE ADDRESS REGISTER
28	001036	164600	AUTO:	WORD 164600	AUTO SWITCH REGISTER

SECTION 4 DISK/CONTROLLER DEFINITIONS

34	001040	000037	MAXSECT:	WORD 37	MAXIMUM SECTOR ADDRESS
35	001042	001000	MAXHD:	WORD 1000	MAXIMUM HEAD ADDRESS JUSTIFIED
36	001044	001466	MAXCYL:	WORD 1466	MAXIMUM CYLINDER ADDRESS
37	001046	177400	WPSEC:	WORD 177400	NUMBER OF WORDS PER SECTOR(2'S COMPLEMENT)
38	001050	000400	POSWP:	WORD 400	NUMBER OF WORDS PER SECTOR
39	001052	017304	INTSAV:	WORD DSKDN	INTERRUPT SERVICE ROUTINE ADDRESS
40	001054	001037	RDUSH:	WORD 1037	MAXIMUM DUSH ADDRESS
41	001056	001466	RWCYL:	WORD 1466	MAXIMUM CYLINDER ADDRESS
42	001060	000004	MAXHED:	WORD 4	MAXIMUM HEAD VALUE
43	001062	000000	STRCNT:	WORD 0	STRIP COUNT
44	001064	000000	OLDHDR:	WORD 0	FLAG OLD HEADER ROMS
45	001066	000000	MICRO:	WORD 0	NONCOMPATIBLE DISK DRIVE
46	001070	164000	DCSRA:	WORD 164000	DCSR ADDRESS
47	001072	000270	INTVEC:	WORD 270	INTERRUPT VECTOR ADDRESS
48	001074	000000	ECC:	WORD 0	FLAG ECC CONTROLLER
49	001076	000000	MULCPU:	WORD 0	MULTIPLE CPU FLAG
50	001100	000000	AUTOSW:	WORD 0	AUTOSWITCH FLAG
51	001102	000000	MCPU:	WORD 0	MULTIPLE CPU SELECT BIT
52	001104	000001	TTYPUT:	WORD 1	KEYBOARD ACTIVE FLAG
53	001106	000000	MDRIVE:	WORD 0	SIMULTANEOUS DRIVE SWITCH
54	001110	000000	TDATE:	WORD 0	DATE CODE FOR DIAGNOSTIC REV
55					UPPER BYTE IS WEEK (0-53)
56					LOWER BYTE IS YEAR

58					
59					);
60					);
61					);
62					);
63					);
64					);
65					);
66	001112	000000	SKCNT:	•WORD 0	);DRIVE 0 INTERRUPT SUBTEST COUNT
67	001114	000000		•WORD 0	);DRIVE 1 INTERRUPT SUBTEST COUNT
68	001116	000000		•WORD 0	);DRIVE 2 INTERRUPT SUBTEST COUNT
69	001120	000000		•WORD 0	);DRIVE 3 INTERRUPT SUBTEST COUNT
70					);
71					);
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83					);
84					);
85					);
86					);
87	001122	000000	INTTBL:	•WORD 0	);DRIVE 1 INTERRUPT LOCATION
88	001124	000000		•WORD 0	); 2
89	001126	000000		•WORD 0	); 3
90	001130	000000		•WORD 0	); 4
91					);
92					);
93					);
94					);
95					);
96					);
97					);
98					);
99					);
100	001132	000000	SOFTRY:	•WORD 0	);RETRY FLAG IN READ DATA TEST
101	001134	000000	CMPCNT:	•WORD 0	);DATA COMPARISON WORD COUNT USED BY DATCMP
102	001136	000000	CURSEC:	•WORD 0	);CURRENT SECTOR IMAGE
103	001140	000000	CURHDD:	•WORD 0	);CURRENT HEAD IMAGE
104	001142	000000	CURCYL:	•WORD 0	);CURRENT CYLINDER IMAGE
105	001144	000000	DKEND:	•WORD 0	);END OF DISK FLAG
106	001146	000000	ENDFLG:	•WORD 0	);END PARAMETER ROUTINE EXIT FLAG
107	001150	000000	INTFLG:	•WORD 0	);GENERAL INTERRUPT FLAG
108	001152	000000	DTCNT:	•WORD 0	);DATA XFER ROUTINE SUBTEST COUNT
109	001154	000000	IPFLG:	•WORD 0	);INTERRUPT PRIORITY FLAG( TEST 37)
110	001156	000000	ICNT:	•WORD 0	);SEEK INTERRUPT COUNT( TEST 36,37)
111	001160	000000	ERRWRD:	•WORD 0	);IDENT OF FIRST ERROR BIT IN ERROR REGISTER
112	001162	000000	ENDSEC:	•WORD 0	);ENDING SECTOR VALUE FOR DISK OPERATION
113	001164	000000	ENDHDD:	•WORD 0	);ENDING HEAD VALUE
114	001166	000000	ENDCYL:	•WORD 0	);ENDING CYLINDER VALUE

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172	007400	SKFLOP=7400	JDSTAT SEEKING FLOP
173			
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175			
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189			
190	001200 047314	IBFTBL:	WORD IDBUF1 ; DRIVE 0 INPUT BUFFER ORIGIN ADDRESS
191	001202 047314		WORD IDBUF1 ; 1
192	001204 047314		WORD IDBUF1 ; 2
193	001206 047314		WORD IDBUF1 ; 3
194			
195	000033	INTCNT=<IBFTBL-SKCNT>/2	INITIALIZATION LOOP COUNT
196			
197			
198		EOT	END OF TAPE
199			
200			
201	000000	RO=X0	
202			
203			
204			
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206			
207			
208	001210	SKTTN:	
209	001210 000032	STPTN: WORD 32	ENDING TEST NUMBER(DEFAULT IS TEST 25)
210	001212 000000	STRTN: WORD 0	BEGINNING TEST NUMBER
211	001214 000000	STPDSK: WORD 0	END DISK DRIVE NUMBER
212	001216 000000	STRDQSK: WORD 0	START DISK NUMBER
213	001220 000000	REPFLG: WORD 0	REPEAT FLAG
214	001222 000000	NOSTOP: WORD 0	REPEAT ON ERROR FLAG
215	001224 000000	PASINH: WORD 0	INHIBIT PASS COUNT PRINTOUT
216	001226 000000	ERPRIN: WORD 0	INHIBIT ERROR PRINTOUT
217	001230 000000	CONST: WORD 0	SKIP FLAG(TEST31,32 ONLY)
218	001232 000000	CURTN: WORD 0	CURRENT TEST NUMBER
219	001234 000000	CURDSK: WORD 0	CURRENT DISK NUMBER
220	001236 000000	PASCNT: WORD 0	PASS COUNTER
221	001240 000000	UNIT: WORD 0	CURRENT UNIT NUMBER IN UNIT FIELD
222	001242 000000	NINPUB: WORD 0	FLAG NO TEST INPUT
223	001244 000000	NONCON: WORD 0	FLAG NO CONSOLE INPUT
224	001246 000000	SKPBAD: WORD 0	FLAG ABORT OR SKIP BAD SECTOR DETECT(0=SKIP)
225	001250 000000	CSWTCH: WORD 0	CONSOLE SWITCH FOR DYNAMIC DUSH VALUES
226	001252 176345	RAMBLER: WORD 176345	RANDOM NUMBER
227	001254 000000	DSKSAV: WORD 0	TEMPORAY LOCATION FOR SAVING CURRENT DISK NUMBER
228	001256 027767	POLY: WORD 27767	XOR NUMBER FOR RANDOM POLY



229	001260	001223	HDR1:	WORD 1223	HEADER WORD #1 OF SECTOR 1
230	001262	151140	HDR2:	WORD 151140	HEADER WORD #2 OF SECTOR 1
231	001264	000553	ECCV1:	WORD 553	ECC WORD 1 FOR DATA=1 BIT
232	001266	026500	ECCV2:	WORD 26560	ECC WORD 2 FOR DATA=1 BIT
233	001270	177000	MAXTR:	WORD 177000	MASK FOR LIMITING TRANSFER SIZE
234	001272	000000	LPCNT:	WORD 0	TEMP LOCATION FOR LOOP COUNTS
235	001274	173000	EMULAT:	WORD 173000	REBOOT ADDRESS FOR PDP11 CONSOLE EMULATOR
236		030000		UNIFLD=30000	BIT SET FOR EXTRACTING UNIT SELECT
237		000136		FUNC=136	BITS ANDED TO CLEAR FUNCTION+INTERRUPT BITS
238		000136		FUNC=136	BITS ANDED TO CLEAR FUNCTION AND INTERRUPT BITS
239	001276	140000	BADBIT:	WORD 140000	BAD SECTOR BITS
240	001300	002000	BUFCLR:	WORD 2000	DATA BUFFER CLEAR
241	001302	040000	SEKINB:	WORD 40000	SEEK INHIBIT BIT
242	001304	030000	WPRBIT:	WORD 30000	MAXIMUM DUSH VALUE
243	001306	003400	SEKMP:	WORD 3400	COMPARE SEEKING FLOPS WORD
244	001310	000004	TMHP:	WORD 4	TIME OUT LOOP COUNT
245		177777		TIME=177777	NUMBER USED IN WAIT LOOPS
246	001312	000000	SKIPR:	WORD 0	COUNTER FOR HADR CONTROLLER ERRORS IN READ MODE(26)
247	001314	000000	ERRCNT:	WORD 0	DATA COUNTER(ERRORS)
248	001316	000000	HERCNT:	WORD 0	HARD ERROR INDEX
249	001320	000000	DATER:	WORD 0	DATA ERROR FLAG
250	001322	000000	ERRFLG:	WORD 0	ERROR FLAG (MAIN)
251	001324	000000	ERROR:	WORD 0	ERROR COUNT USED WITH BIT 15 REPEAT ON ERROR
252	001326	000000	SOFER1:	WORD 0	SOFT CONTROLLER ERROR COUNTER RETRY
253	001330	000000	SOFERR:	WORD 0	SOFT CONTROLLER ERROR COUNTER
254	001332	000000	RTRYIN:	WORD 0	DATA RETRY INDEX
255					

DATA ERROR TABLE

THIS TABLE CONTAINS DATA ENTRY COUNTS  
 CONTAINS THE NUMBER OF DATA ERRORS AND CORRESPONDING NUMBER  
 OF RETRYS MADE BEFORE THE DATA WAS RECOVERED CORRECTLY.  
 ANY DATA STILL IN ERROR AFTER 8 RETRYS IS CONSIDERED  
 A "HARD ERROR" AND IS COUNTED AS SUCH.

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ADDRESS	WORD 0	UNUSED	RETRY DATA ERROR COUNT
001334	000000		1
001336	000000		2
001340	000000		3
001344	000000		4
001346	000000		5
001350	000000		6
001352	000000		7
001354	000000		8

TTY OUTPUT MESSAGE ADDRESS TABLE

ADDRESS	WORD ENTMSG	ENDING TEST MESSAGE ADDRESS
001356	001400	
001360	001426	
001362	001456	
001364	001505	
001366		
001366	001536	
001370	001574	
001372	007320	
001374	007365	
001376	007425	

ADDRESS	ENTMSG	ASCII	ENDING TEST NUMBER
001400	105	116	104
001403	111	116	107
001406	040	124	105
001411	123	124	040
001414	116	125	115
001417	102	105	122
001422	040	075	040





1	002032	104	104	055				
2	002035	115	115	115				
3	002040	055	131	131				
4	002043	040						
5	92 002044	000						•BYTE 0
6	93 002045	104	101	124	DTE:			•ASCII /DATE: /
7	002050	105	072	040				
8	94 002053	000						•BYTE 0
9	95							;
10	96							;
11	97							;
12	98							;
13	99							;
14	100							CONTROLLER PARAMETER MESSAGES
15	101							;
16	102							•EVEN
17	103 002054	002066			DCMSG:			•WORD DCMSG
18	104 002056	002114						•WORD INTMSG
19	105 002060							•DCSR MESSAGE ADDRESS
20	106 002060	002137			DECGSH:			•INTERRUPT VECTOR MESSAGE ADDRESS
21	107 002062	002204						•WORD ECCMSG
22	108 002064	002241						•WORD MULMSG
23	109							•ECC OPTION MESSAGE ADDRESS
24	110							•MULTIPLE CPU MESSAGE ADDRESS
25	111 002066	104	103	123	DCMSG:			•WORD AUTMSG
26	002071	122	040	050				•AUTO SWITCH OPTION MESSAGE ADDRESS
27	002074	102	101	123				•ASCII /DCSR (BASE) ADDRESS =/
28	002077	105	051	040				
29	002102	101	104	104				
30	002105	122	105	123				
31	002110	123	040	075				
32	112 002113	000						•BYTE 0
33	113 002114	111	116	124	INTMSG:			•ASCII /INTERRUPT VECTOR =/
34	002117	105	122	122				
35	002122	125	120	124				
36	002125	040	126	105				
37	002130	103	124	117				
38	002133	122	040	075				
39	114 002136	000						•BYTE 0
40	115 002137	105	122	122	ECCMSG:			•ASCII /ERROR CORRECTION CONTROLLER? Y OR N /
41	002142	117	122	040				
42	002145	103	117	122				
43	002150	122	105	103				
44	002153	124	111	117				
45	002156	116	040	103				
46	002161	117	116	124				
47	002164	122	117	114				
48	002167	114	105	122				
49	002172	077	040	131				
50	002175	040	117	122				
51	002200	040	116	040				
52	116 002203	000						•BYTE 0
53	117 002204	115	125	114	MULMSG:			•ASCII /MULTIPLE CPU OPTION? Y OR N /
54	002207	124	111	120				
55	002212	114	105	040				
56	002215	103	120	125				
57	002220	040	117	120				

1	002223	124	111	117	
2	002226	116	077	040	
3	002231	131	040	117	
4	002234	122	040	116	
5	002237	040			
6	118 002240	000			•BYTE 0
7	119 002241	101	125	124	AUTMSG? •ASCII /AUTO SWITCH OPTION? Y OR N /
8	002244	117	040	123	
9	002247	127	111	124	
10	002252	103	110	040	
11	002255	117	120	124	
12	002260	111	117	116	
13	002263	077	040	131	
14	002266	040	117	122	
15	002271	040	116	040	
16	120 002274	000			•BYTE 0
17	121				;
18	122				;
19	123				;
20	124				;
21	125				;
22	126				;
23	127				PRINT COMMAND MESSAGES
24	128				;
25	129				;
26	130				;
27	131				SECTION 7 TEST ORIGIN ADDRESS TABLES
28	132				;
29	133				(NON ECC CONTROLLERS)
30	134				;
31	135				;
32	136				TABLE CONTAINS ORIGIN ADDRESS OF EACH TEST IN ASCENDING
33	137				ORDER.
34	138				;
35	139				;
36	140				;
37	141				;
38	142				;
39	143				•EVEN
40	144 002276	016530			TNORG: •WORD TN0
41	145 002300	017412			•WORD TN1
42	146 002302	017654			•WORD TN2
43	147 002304	020006			•WORD TN3
44	148 002306	020244			•WORD TN4
45	149 002310	021110			•WORD TN5
46	150 002312	021544			•WORD TN6
47	151 002314	022216			•WORD TN7
48	152 002316	023626			•WORD TN10
49	153 002320	023670			•WORD TN11
50	154 002322	023760			•WORD TN12
51	155 002324	024042			•WORD TN13
52	156 002326	024130			•WORD TN14
53	157 002330	024220			•WORD TN15
54	158 002332	024314			•WORD TN16
55	159 002334	024664			•WORD TN17
56	160 002336	025474			•WORD TN20
57	161 002340	026350			•WORD TN21

•REGISTER INITIALIZATION TEST  
 •REGISTER LOAD AND READ TEST  
 •REGISTER SLIDING ONES TEST  
 •REGISTER SLIDING ZERO TEST  
 •REGISTER ERROR AND STATUS REGISTER TESTS  
 •UNIT SELECT TESTS  
 •SEEKING TESTS  
 •INTERRUPT LOGIC TEST  
 •ONE WORD WRITE TEST  
 •ONE SECTOR WRITE TEST  
 •ONE SECTOR READ TEST  
 •INCREMENTING WORD COUNT TEST  
 •ONE SECTOR WRITE READ COMPARE TEST  
 •WRT/RD/CMP INCREASING WORD COUNT TEST  
 •WRITE PROTECT TEST  
 •HEADER OVERRIDE-HEADER READ TEST  
 •WRITE PROTECT-WRITE CHECK TEST  
 •HEADER WRITE COMMAND TEST

162	002342	027170	•WORD TN22	]CRC/HEADER TEST
163	002344	030160	•WORD TN23	]BADSECTOR FLAG TEST
164	002346	030542	•WORD TN24	]RTZ TEST
165	002350	031360	•WORD TN25	]IMPLIED SEEK TESTS
166	002352	031724	•WORD TN26	]CONVERGE/DIVERGE SEEKING TEST - DISK ADDRESS TEST
167	002354	032346	•WORD TN27	]MEM. EXT.-BUSS TIME OUT-OVRRUN-MEM INC TEST
168	002356	033712	•WORD TN30	]CONVERGE/DIVERGE-RANDOM TEST(DATA COMPARE)
169	002360	034204	•WORD TN31	]DISK DATA TEST(ENTIRE TEST OF DISK PACK)
170	002362	035532	•WORD TN32	]READ ENTIRE DISK TEST
171	002364	036144	•WORD TN33	]MULTIPLE CPU EXERCISE
172	002366	000000G	•WORD TN34	]
173	002370	000000G	•WORD TN35	]
174	002372	000000G	•WORD TN36	]OVERLAPPED SEEK TEST
175	002374	000000G	•WORD TN37	]OVERLAPPED SEEK AND DATA TRANSFERED TEST
176	002376	000000G	•WORD TN40	]LINKAGE REGISTER LOAD AND READ
177	002400	000000G	•WORD TN41	]LINKAGE WRITE TEST
178	002402	000000G	•WORD TN42	]LINKAGE READ TEST
179	002404	000000G	•WORD TN43	]LINKAGE WRITE/READ/COMPARE TEST
180	002406	000000G	•WORD TN44	]LINKAGE BLOCKED READ TEST
181	002410	042762	•WORD TN45	]FORMAT PROGRAM(> 8K)
182	002412	043314	•WORD TN46	]HEADER READ TEST/PACK VERIFY TEST
183	002414	043506	•WORD TN47	]FAST FORMAT PROGRAM
184	002416	000000G	•WORD TN50	]FORMAT PROGRAM
185			]	
186			]	
187			]	
188			]	
189			]	TEST ORIGIN ADDRESS TABLE (ECC CONTROLLERS)
190			]	
191			]	
192			]	
193			]	
194	002420	016530	TNORGA: •WORD TNO	]REGISTER INITIALIZATION TEST
195	002422	017412	•WORD TN1	]REGISTER LOAD AND READ TEST
196	002424	017654	•WORD TN2	]REGISTER SLIDING ONES TEST
197	002426	020006	•WORD TN3	]REGISTER SLIDING ZEROES TEST
198	002430	020244	•WORD TN4	]REGISTER ERROR AND REGISTER STATUS TESTS
199	002432	021110	•WORD TN5	]UNIT SELECT TEST
200	002434	021544	•WORD TN6	]SEEKING TESTS
201	002436	022216	•WORD TN7	]INTERRUPT LOGIC TEST
202	002440	023626	•WORD TN10	]ONE WORD WRITE TEST
203	002442	023670	•WORD TN11	]ONE SECTOR WRITE TEST
204	002444	023760	•WORD TN12	]ONE SECTOR READ TEST
205	002446	024042	•WORD TN13	]INCREMENTING WORD COUNT TEST
206	002450	024130	•WORD TN14	]ONE SECTOR WRITE/READ DATA COMPARE
207	002452	024220	•WORD TN15	]WRT/RD/CMP INCREASING WORD COUNT TEST
208	002454	036464	•WORD TNA16	]ECC REGISTER TESTS
209	002456	036774	•WORD TNA17	]ECC CRC DETECTION TESTS(HEADERS ONLY)
210	002460	025740	•WORD TNA20	]WRITE CHECK TESTS
211	002462	041076	•WORD TNA21	]ECC DETECTION TESTS
212	002464	041674	•WORD TNA22	]ECC DETECTION/CORRECTION TESTS
213	002466	042516	•WORD TNA23	]ECC COMPATIBILITY/EXERCISE TESTS
214	002470	030542	•WORD TN24	]RTZ TEST
215	002472	031360	•WORD TN25	]IMPLIED SEEKING TEST
216	002474	031724	•WORD TN26	]CONVERGE/DIVERGE SEEKING AND DISK ADDRESS TESTS
217	002476	032346	•WORD TN27	]MEM. EXT,BUSS TIME OUT,OVRRUN, MEM INC. TESTS
218	002500	033712	•WORD TN30	]CONVERGE/DIVERGE,RANDOM WR/RD CMP TEST

219	002502	034204	•WORD TN31	);DISK DATA TEST(ENTIRE DISK PACK)
220	002504	035532	•WORD TN32	);DISK RELIABILITY (READ ) TEST
221	002506	036144	•WORD TN33	);MULTIPLE CPU EXERCISE
222	002510	000000G	•WORD TN34	);
223	002512	000000G	•WORD TN35	);
224	002514	000000G	•WORD TN36	);OVERLAPPED SEEK TEST
225	002516	000000G	•WORD TN37	);OVERLAPPED SEEK/WRITE TEST
226	002520	000000G	•WORD TN40	);
227	002522	000000G	•WORD TN41	);
228	002524	000000G	•WORD TN42	);
229	002526	000000G	•WORD TN43	);
230	002530	000000G	•WORD TN44	);
231	002532	042702	•WORD TN45	);FORMAT PROGRAM ( > 8K)
232	002534	043314	•WORD TN46	);HEADER VERIFY TEST
233	002536	043506	•WORD TN47	);FORMAT TEST
234	002540	000000G	•WORD TN50	);
235			);	
236			);	
237			);	
238			);	
239			);	
240			);	
241			);	
242			);	
243			);	
244			);	
245			);	
246			);	
247			);	
248			);	
249			);	
250			);	
251			);	
252			);	
253			);	
254			);	
255	002542	000000	•WORD 0	); DRIVE 0 COMMANDED CYLINDER ADDRESS
256	002544	000000	•WORD 0	); 1
257	002546	000000	•WORD 0	); 2
258	002550	000000	•WORD 0	); 3
259			);	
260			);	
261			);	

DISK DRIVE SEEK TABLE

);THE DISK DRIVE SEEK TABLE CONTAINS THE CURRENT COMMANDED  
 );CYLINDER ADDRESS OF EACH OF THE DISK DRIVES. THE  
 );CYLINDER ADDRESS WORD FOR EACH DRIVE IS UPDATED BY THE  
 );TEST PROGRAMS AND TRANSMITTED TO THE DISK DRIVE VIA  
 );THE CONTROLLER.

CYLADR

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9					
10	002552	107577	REGHSC:	•WORD 107577	•DISK CONTROL AND STATUS REGISTER MASK
11	002554	140000		•WORD 140000	•UNIT-HEAD-SECTOR MASK
12	002556	000001		•WORD 1	•CORE ADDRESS MASK
13	002560	000000		•WORD 0	•WORD COUNT MASK
14	002562	176000		•WORD 176000	•CYLINDER ADDRESS MASK
15	002564	000000		•WORD 0	•DISKSTATUS DUMMY MASK
16	002566	000000		•WORD 0	•DISK ERROR REGISTER DUMMY MASK
17	002570	000000		•WORD 0	•GCSR REGISTER DUMMY MASK
18	002572	000000		•WORD 0	•GMSC REGISTER MASK
19	002574	000000		•WORD 0	•GUSH MASK
20	002576	000000		•WORD 0	•GBAR MASK
21	002600	000000		•WORD 0	•GWCNT MASK
22	002602	000000		•WORD 0	•GCYL MASK
23	002604	000000		•WORD 0	
24	002606	177774		•WORD 177774	•STRIP CORE EXTENTION MASK
25	002610	000001		•WORD 1	•GSCAR REGISTER MASK
26					
27					
28					
29					
30					
31					
32					
33					
34					
35					
36					
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43					
44					
45	002612	000001	S10RG:	•WORD 1	
46	002614	000002		•WORD 2	
47	002616	000004		•WORD 4	
48	002620	000010		•WORD 10	
49	002622	000020		•WORD 20	
50	002624	000040		•WORD 40	
51	002626	000100		•WORD 100	
52	002630	000200		•WORD 200	
53	002632	000400		•WORD 400	
54	002634	001000		•WORD 1000	
55	002636	002000		•WORD 2000	
56	002640	004000		•WORD 4000	
57	002642	010000		•WORD 10000	

SLIDING ONE CONSTANT TABLE

•CONSTANTS ARE USED IN REGISTER TESTS

•GLOBL S10RG,S00RG,CNSTNT

58	002644	020000		WORD 20000	;
59	002646	040000		WORD 40000	;
60	002650	100000		WORD 100000	;
61					;
62					;
63					;
64				SLIDING ZERO CONSTANT TABLE	
65					;
66	002652	177776	SUORG:	WORD 177776	;
67	002654	177775		WORD 177775	;
68	002656	177773		WORD 177773	;
69	002660	177767		WORD 177767	;
70	002662	177757		WORD 177757	;
71	002664	177737		WORD 177737	;
72	002666	177677		WORD 177677	;
73	002670	177577		WORD 177577	;
74	002672	177377		WORD 177377	;
75	002674	176777		WORD 176777	;
76	002676	175777		WORD 175777	;
77	002700	173777		WORD 173777	;
78	002702	167777		WORD 167777	;
79	002704	157777		WORD 157777	;
80	002706	137777		WORD 137777	;
81	002710	077777		WORD 077777	;
82					;
83					;
84					;
85				MIXED CONSTANT TABLE	
86					;
87					;
88					;
89	002712	000000	CNSTNT:	WORD 0	; ALL ZEROS
90	002714	052525		WORD 052525	; CHECKERBOARD
91	002716	125252		WORD 125252	; REVERSE CHECKERBOARD
92	002720	177777		WORD 177777	; ALL ONES
93					;
94					;
95					;
96				ODT FILLER CONSTANT	
97				SECTION 9 ERROR HALT REGISTER IMAGE (CPU REGISTERS)	
98					;
99	002722	000000	REGO:	WORD 0	; DRIVE CURRENTLY UNDER TEST
100	002724	000000		WORD 0	; FAILED TEST NUMBER
101	002726	000000		WORD 0	; REFERENCE DATA
102	002730	000000		WORD 0	; ACTUAL DATA
103	002732	000000		WORD 0	; SUBTEST NUMBER
104	002734	000000		WORD 0	; LAST SUBROUTINE JUMP ADDR.
105	002736	000000		WORD 0	; CPU STACK ADDR.
106					;
107					;
108					;
109				THIS CONSTANT IS USED TO ENABLE ODT TO BE LINKED WITH	
110				THE DIAGNOSTIC AND USED IN A STAND ALONE SYSTEM	
111					;
112					;
113				GLOBL \$\$CON	;
114					;

```

115                                     )
116                                     )           START ROUTINE
117                                     )
118                                     )
119                                     )
120                                     ) SECTION 10 TEST CODE
121          003000                       ) =3000           )START LOCATION =3000
122                                     )
123                                     )
124          003000  012706  000776      )START:  MOV   #DCSR-2,SP      )POINT STACK TO SAFE VALUE
125          003004  010600                       )MOV   SP,R0           )USE R0 TO CLEAR CORE
126          003006  005720                       )TST   (R0)+          )LOOK AT PROPER VECTOR
127          003010  005040                       )CORE: CLR  -(R0)      )ENTER HALT
128          Z      003012  010040                       )MOV   RO,-(R0)       )ENTER VECTOR TRAP
129          003014  005700                       )TST   RO             )CHECK IF LOADED LOCATION 0
130          003016  001401                       )BEQ   CORE1          )EXIT IF YES
131          003020  000773                       )BR    CORE           )DOAGAIN
132                                     )
133                                     )
134                                     )
135                                     )
136          003022  005046                       )CORE1: CLR  -(SP)     )SET PROCESSOR STATUS WORD
137          003024  012746  003032      )MOV   #PSWORD,-(SP)  )LOAD RETURN ADDRESS
138          003030  000002                       )RTI                    )FAKE INTERRUPT
139          003032  005737  001104      )PSWORD: TST  TYPUT     )KEYBOARD SETUP?
140          003036  001402                       )BEQ   TSTART         )NO GO ON
141          003040  000137  006170      )JMP   TTSTART        )SET UP READER/PRINTER
142                                     )
143                                     )
144          003044  004537  015644      )TSTART: JSR  R5,ADRSTP )SET UP PARAMETERS NOW
145          )*****
146          003050  005737  001244      )TST   NONCON         )SEE IF SWITCH REGISTER PRESENT
147          003054  001014                       )BNE  TSTCON          )CONTINUE IF NO PARAMETER ENTRY
148          003056  005737  001242      )TST   NINPUT         )TEST NO TEST INPUT
149          003062  001011                       )BNE  TSTCON          )CONTINUE IF NO
150          003064  005737  001104      )TST   TYPUT         )KEYBOARD?
151          003070  001006                       )BNE  TSTCON          )GO ON IF YES
152          003072  013700  177570      )STARTA: MOV  CSWR,R0   )ENTER FIRST PARAMETER
153          003076  010003                       )MOV  R0,R3           )SAVE IN R3 ALSO
154          003100  100513                       )BHI  SREPFL         )SET REPEAT FLAG IF NEGITIVE
155          003102  005037  001220      )CLR   REPFLG        )RESET REPEAT FLAG
156          003106  012704  001312      )TSTCON: MOV  #SKIPR,R4 )SET UP TO CLEAR ERROR LOCS.
157          003112  010401                       )MOV  R4,R1           )
158          003114  012702  001332      )MOV  #RTRYIN,R2     )
159          003120  160102                       )SUB  R1,R2           )
160          003122  006202                       )ASR  R2              )
161          003124  005024                       )STST1: CLR  (R4)+     )CLEAR LOCATION
162          003126  005302                       )DEC  R2              )
163          003130  001375                       )BNE  STST1           )
164          003132  005037  001236      )CLR   PASCNT        )RESET PASS COUNTER
165          003136  005737  001244      )TST   NONCON        )TEST CONSOLE MODE AGAIN
166          003142  001046                       )BNE  STCLR          )START TESTING IF NON ZERO
167          003144  005737  001242      )TST   NINPUT        )TEST NO DISK INPUT
168          003150  001043                       )BNE  STCLR          )CONTINUE IF NO
169          003152  005737  001104      )TST   TYPUT         )KEYBOARD?
170          003156  001040                       )BNE  STCLR          )CONTINUE IF NO
171          003160  042700  177400      )BIC  #177400,R0     )EXTRACT STOP TEST NUMBER
    
```

172	003164	042703	100377	BIC	#100377,R3	EXTRACT START TEST NUMBER	
173	003170	000303		SWAB	R3		
174	003172	012701	001210	MOV	#STPTN,R1	POINT R1 TO STOP TEST NUMBER LOCATION	
175	003176	010021		MOV	RO,(R1)+	SAVE ENDING TEST NUMBER	
176	003200	010321		MOV	R3,(R1)+	SAVE STRING TESTNUMBER	
177	003202	000240		NOP			
178	003204	000000		HALT		WAIT FOR OPERATOR	
179	003206	005737	001250	TST	CSWTC	SEE IF IN SCOPE MODE	
180	003212	001403		BEQ	TSTCA	CONTINUE IF NO	
181	003214	005000		CLR	RO	MAKE DRIVE SELECTION DRIVE ZERO	
182	003216	005002		CLR	R2		
183	003220	000415		BR	TSTCB	CONTINUE INIT	
184	003222	013700	177570	TSTCA: MOV	CSWR,RO	PUT TEST DRIVE PARAMETERS IN RO	
185	003226	010002		MOV	RO,R2	ENABLE AUTO SWITCH FLAG IF APPL.	
186	003230	042702	157777	BIC	#157777,R2	EXTRACT AUTO SWITCH	
187	003234	010237	001100	MOV	R2,AUTOSW		
188	003240	010002		MOV	RO,R2	SAVE IN R2 ALSO	
189	003242	042700	177600	BIC	#177600,RO	EXTRACT END DISK NUMBER	
190	003246	042702	160377	BIC	#160377,R2	EXTRACT STARTING DISK NUMBER	
191	003252	000302		SWAB	R2		
192	003254	010021		TSTCB: MOV	RO,(R1)+	SAVE LAST DRIVE NUMBER	
193	003256	010221		MOV	R2,(R1)+	SAVE BEGINNING DISK DRIVE NUMBER	
194	003260	013737	001212	001232	STCLR: MOV	STRTN,CURTN	ESTABLISH CURRENT TEST NUMBER
195	003266	013737	001216	001234	MOV	STRDSK,CURDSK	ESTABLISH CURRENT DRIVE NUMBER
196	003274	012700	001336	MOV	ERRTAB,RO	GET ERROR TABLE ORIGIN ADDRESS	
197	003300	012701	000010	MOV	#8,,R1	SET UP LOOP COUNT	
198	003304	005020		CLR	(R0)+	CLR RETRY COUNT LOCATION	
199	003306	005301		DEC	R1	DECREMENT LOOP COUNT	
200	003310	001375		BNE	.-1	REPEAT IF NOT ZERO	
201	003312	000005		RESET		RESET I/O	
202	003314	004737	015414	JSR	PC,TTYSET	ENABLE INTERRUPTS FOR KEYBOARD	
203	003320	004537	016352	JSR	R5,DKINIT	INITIALIZE DISKS	
204	003324	000137	003532	JMP	PARINT	GO TO PARAMETER INTIALIZATION	
205	003330	005237	001220	SREPFL: INC	REPFLG	SET TEST REPEAT FLAG	
206	003334	042700	010000	BIC	#10000,RO	MASK OUT TEST PARAMETERS	
207	003340	000602		BR	TSTCON	CONTINUE	
208							
209							
210							
211						TEST CONTROL ROUTINE	
212							
213							
214						AT ENTRY:	
215						1. R5 CONTAINS CALLING PROGRAM ADDRESS IF ROUTINE	
216						WAS CALLED AS A RESULT OF DETECTION	
217						OF ANY ERROR.	
218							
219						2. CURDSK = CURRENT DISK NUMBER	
220							
221						3. CURTN = CURRENT TEST NUMBER	
222							
223						PROGRAM EXITS TO APPROPRIATE TEST ROUTINE OR	
224						HALTS DEPENDING ON SPECIFIED ERROR PARAMETERS	
225							
226							
227						GLOBAL INTCNT INITIALIZATION LOOP COUNT	
228							

229										
230										
231	003342	004737	015414	TSTCTL:	JSR	PC,TTYSET				ENABLE INTERRUPTS FOR KEYBOARD
232	003346	005737	001322		TST	ERRFLG				ERRORS?
233	003352	001461			BEO	TNTST				BRANCH IF NO
234	003354	004737	015440		JSR	PC,REGSAV				SAVE CONTROLLER
235	003360	005737	001104		TST	TTYPUT				KEYBOARD?
236	003364	001012			BNE	STOP				SAVE CPU IF YES
237	003366	005737	001244	TST2:	TST	NONCON				CONSOLE MODE?
238	003372	001404			BEO	TST1				CONTINUE IF YES
239	003374	005737	001222		TST	NOSTOP				TEST NO CONSOLE CONTINUE ON ERROR FLG
240	003400	001046			BNE	TNTST				GO ON IF DESIRED
241	003402	000403			BR	STOP				HALT IF NOT
242	003404	005737	177570	TST1:	TST	CSWR				IS STOP ON ERROR INHIBITED?
243	003410	100442			BMI	TNTST				CONTINUE WITH NEXT TEST IF YES
244	003412	013700	001234	STOP:	MOV	CURDSK,RO				ESTABLISH FAILED DISK DRIVE NO
245	003416	013701	001232		MOV	CURTNR,R1				ESTABLISH FAILED TEST NO.
246	003422	010037	002722		MOV	RO,REGO				SAVE CPU REGISTER
247	003426	012700	002722		MOV	#REGO,RO				
248	003432	005720			TST	(RO)+				POINT TO NEXT ENTRY
249	003434	010120			MOV	R1,(RO)+				
250	003436	010220			MOV	R2,(RO)+				
251	003440	010320			MOV	R3,(RO)+				
252	003442	010420			MOV	R4,(RO)+				
253	003444	010520			MOV	R5,(RO)+				
254	003446	010620			MOV	SP,(RO)+				INCLUDE STACK POINTER
255	003450	013700	002722		MOV	REGO,RO				RESTORE RO
256	003454	005737	001104		TST	TTYPUT				KEYBOARD ACTIVE?
257	003460	001462			BEO	TST3				GO ON IF NO
258	003462	000137	012030		JMP	TTERR				PRINT FAILURE IF YES
259	003466	005737	001244	TST3:	TST	NONCON				CONSOLE(SWITCHFS)?
260	003472	001002			BNE	BOOT				BOOT EMULATOR IF NO
261	003474	000000		STOP8:	HALT					QUIT*****
262	003476	000415			BR	PARINT				
263										
264										
265										
266	003500	004537	004020	BOOT:	JSR	R5,REBOOT				LOAD SOMETHING INTERESTING
267										
268										
269										
270										
271	003504	005737	001220	STPTST:	TST	REPFLG				IS TEST SEQUENCE TO BE REPEATED?
272	003510	001740			BEO	STOP				STOP HERE IF NO
273	003512	000137	003720		JMP	PASINC				JUMP TO PASS INCREMENT IF YES
274	003516	023737	001232	001210	TNTST:	CMR	CURTNR,STPTN			ENDING TEST NUMBER?
275	003524	001466			BEO	LSTTST				BRANCH IF YES
276	003526	005237	001232		INC	CURTNR				INCREMENT CURRENT TEST NUMBER
277	003532	012700	001112	PARINT:	MOV	#SKCNT,RO				POINT TO FLAG CLEAR LOCATION
278	003536	013777	001052	175326	MOV	INTSAV,@INTVEC				LOAD INTERRUPT VECTOR
279	003544	013702	001072		MOV	INTVEC,R2				ENTER PRIORITY LEVEL 5
280	003550	005722			TST	(R2)+				
281	003552	012712	000240		MOV	#240,(R2)				
282	003556	012701	000033		MOV	#INTCNT,R1				ESTABLISH LOOP COUNT IN R1
283	003562	005002		INITLP:	CLR	R2				
284	003564	010220			MOV	R2,(RO)+				CLEAR LOCATION
285	003566	005301			DEC	R1				DECREMENT LOOP COUNT

286	003570	001374		BNE	INITLP		]	REPEAT IF NOT DONE	
287	003572	004537	004034	JSR	R5,CLRBUF		]	CLEAR DISK BUFFER AREA	
288	003576	004537	004276	JSR	R5,REQUEST		]	GO REQUEST FORMATTER IF MULTI CPU	
289	003602	005777	175172	TST	@DCSR		]	ERROR STILL?	
290	003606	100002		BPL	FMTCLR		]	GO ON IF NO	
291	003610	004537	016352	JSR	R5,DKINIT		]	INITAILIZE DISKS	
292	003614	022606		FMTCLR:	CMP	(SP)+,SP	]	POP R5 OFF THE STACK	
293	003616	005737	001322	TST	ERRFLG		]	ERROR DURING PAST TEST?	
294	003622	001404		BEQ	+10.		]	CONTINUE IF NO	
295	003624	005037	001322	CLR	ERRFLG		]	RESET ERROR FLAG	
296	003630	005237	001324	INC	ERROR		]	INCREMENT ERROR COUNTER	
297	003634	013700	001232	MOV	CURTN,R0		]	ESTABLISH TEST NO. INDEX	
298	003640	005737	001100	TST	AUTOSW		]	AUTO SWITCH DESIRED?	
299	003644	001403		BEQ	+8.		]	CONTINUE IF NO	
300	003646	012777	000200	MOV	#200,@AUTO		]	TURN AUTOSWITCH ON IF YES	
301	003654	006300		ASL	R0		]	MAKE VALID WORD INDEX OF TEST NO.	
302	003656	012777	000041	MOV	#SYSCLRIBITS,@DCSR		]	CLEAR FORMATTER	
303	003664	005737	001074	TST	ECC		]	IS THIS AN ECC CONTROLLER?	
304	003670	001402		BEQ	GOTEST		]	RUN NORMAL TEST SEQUENCE IF NO	
305	003672	000170	002420	JMP	@TNORGA(R0)		]	RUN EDD TESTS IF YES	
306	003676	000170	002276	GOTEST:	JMP	@TNOR6(R0)	]	RUN NORMAL TESTS IF NO	
307	003702	023737	001234	001214	LSTTST:	CMP	CURDSK,STPDSK	]	HAVE WE TESTED ALL OF THE DISKS?
308	003710	001403		BEQ	PASINC		]	GO ON IF YES	
309	003712	005237	001234	INC	CURDSK		]	REPEAT TESTS ON NEXT DISK IF NO	
310	003716	000453		BR	TNINT		]		
311	003720	005237	001236	PASINC:	INC	PASCNT	]	INCREMENT PASS COUNT LOCATION	
312	003724	005737	001104	TST	TTYPUT		]	KEYBOARD?	
313	003730	001402		BEQ	PINC1		]	GO ON IF NO	
314	003732	000137	011640	JMP	PASS		]	GO TO PASS PRINT OUT IF YES	
315	003736	005737	001220	PINC1:	TST	REPFLG	]	REPEAT?	
316	003742	001016		BNE	TNINTA		]	FINISH UP IF NO	
317	003744	013700	001236	MOV	PASCNT,R0		]	SET R0 TO PASS COUNT	
318	003750	005737	001244	TST	NONCON		]	DO WE HAVE A CONSOLE?	
319	003754	001410		BEQ	HALT8		]	END IT IF NO	
320	003756	000137	003500	JMP	BOOT		]	SPIT OUT RESULTS IF YES	
321	003762	000405		BR	HALT8		]	END AT 4000	
322							]		
323							]		
324							]		
325							]		
326		003776				=3776	]		
327	003776	000000		HALT8:	HALT		]	END IT HERE	
328	004000	013737	001216	001234	TNINTA:	MOV	STRDSK,CURDSK	]	SET UP FIRST DISK AS CURRENT DISK
329	004006	013737	001212	001232	TNINT:	MOV	STRTN,CURTN	]	SET UP FIRST TEST AS CURRENT TEST
330	004014	000137	003532		JMP	PARINT	]	CONTINUE REINITIALIZATION	
331							]		
332							]		
333							]		
334							]		
335							]		
336							]	EMULATOR BOOT ROUTINE	
337							]	*****	
338							]		
339							]		
340							]		
341	004020	013700	001322	REBOOT:	MOV	ERRFLG,R0	]	LOAD ERRFLG INTO R0	
342	004024	013704	001232		MOV	CURTN,R4	]	LOAD ENDING TEST NUMBER	

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343 004030 013707 001274      MOV      EMULAT,PC      ;BOOT UP THE EMULATOR
344                          ;      CAN'T DO ANYTHING NOW !
345                          ;
346                          ;
347                          ;
348                          ;
349                          ;
350                          ;
351                          ;      BUFFER CLEAR ROUTINE
352                          ;      *****
353                          ;
354                          ;
355                          ;
356          007012      CLRCNT=IDBUF5-<0DBUF-10>      ;CLEAR COUNT
357                          ;
358                          ;
359 004034 004537 015474      CLRBUF: JSR      R5,SAVE      ;SAVE CPU
360 004040 012700 044302      MOV      #0DBUF-10,R0      ;USE R0 TO POINT
361 004044 012701 007012      MOV      #CLRCNT,R1      ;USE R1 TO COUNT
362 004050 006201      ASR      R1      ;MAKE USEFUL
363 004052 005020      CLRBF1: CLR      (R0)+      ;CLEAR MEMORY
364 004054 005301      DEC      R1      ;DECREMENT COUNTER
365 004056 001375      BNE     CLRBF1      ;CONTINUE IF NOT ZERO
366 004060 004537 015510      JSR      R5,REST      ;RESTORE CPU
367 004064 000205      RTS     R5      ;AND EXIT
368                          ;
369                          ;
370                          ;
371          007012      CLRCNT=IDBUF5-<0DBUF-10>
372                          ;
373                          ;      SEEK TIME OUT LOOP
374                          ;      *****
375                          ;
376                          ;      THIS ROUTINE ISSUES A SEEK TO MAXCYL IN CURRENT DISK
377                          ;      • IT THEN ISSUES A RECALIBRATE AN USES A COUNTER TO
378                          ;      ESTABLISH A WAIT LOOP SIZE FOR TIMING A SEEK •
379                          ;
380                          ;
381                          ;
382                          ;
383 004066 004537 015474      SEKTIM: JSR      R5,SAVE      ;SAVE CPU REGISTERS
384 004072 012701 000003      MOV      #3,R1      ;SET UP MAXIMUM TIMEOUT LOOP
385 004076 004537 016332      JSR      R5,DISKID      ;SET UP DISK SELECT BITS
386 004102 004537 004276      JSR      R5,RQUEST      ;REQUEST FORMATTER
387 004106 010277 174670      MOV      R2,#DUSH      ;SELECT DISK
388 004112 000240      NOP      ;WAIT FOR SELECTION
389 004114 000240      NOP
390 004116 005777 174670      TST     @DSTAT      ;DISK OUT THERE?
391 004122 100044      BPL     SEKER      ;EXIT NO
392 004124 013777 001044 174656      MOV      MAXCYL,@DCYL      ;LOAD MAXCYL
393 004132 052777 000002 174640      BIS     #SEKCMD,@DCSR      ;LOAD SEEK COMMAND
394 004140 005277 174634      INC     @DCSR      ;SET GO BIT
395 004144 012700 177777      SKLP1: MOV      #1,R0      ;LOAD LOOP COUNT
396 004150 000240      NOP      ;
397 004152 105777 174634      SKLP:  TSTB     @DSTAT      ;SEEK DONE?
398 004156 100405      BMI     SEKOUT      ;EXIT IF YES
399 004160 005300      DEC     R0      ;DECREMENT SEEK LOOP
    
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400	004162	001373			BNE	SKLP		LOOK AGAIN
401	004164	005301			DEC	R1		DECREMENT OUTER LOOP
402	004166	001366			BNE	SKLP1		GET OUT OF HERE?
403	004170	000421			BR	SEKER		EXIT IF HAVN'T FINSHED
404	004172	012701	000003		SEKOUT:	MOV	#3,R1	RESTORE OUTER LOOP
405	004176	004537	004276		JSR	R5,RQUEST		REQUEST FORMATTER
406	004202	052777	000025	174570	BIS	#RECAL,#DCSR		ISSUE RECAL
407	004210	000240			NOP			
408	004212	012700	177777		SEKOU2:	MOV	#-1,R0	RESTORE LOOP COUNT
409	004216	105777	174570		SEKOUT:	TSTB	#DSTAT	SEEK DONE?
410	004222	100416			BMI	SKDON		EXIT IF YES
411	004224	005300			DEC	R0		DECREMENT IF NO
412	004226	001373			BNE	SEKOUT1		LOOK AGAIN
413	004230	005301			DEC	R1		DEC OUTER LOOP
414	004232	001367			BNE	SEKOU2		LOOK AGAIN IF NOT DONE
415	004234	005237	001322		SEKER:	INC	ERRFLG	SOMETHING WRONG GET OUT OF HERE
416	004240	012777	000041	174532	SEK8K:	MOV	#SYSCLR,#BITS,#DCSR	ISSUE SYSCLR
417	004246	004537	004276		JSR	R5,RQUEST		REGAIN FORMATTER
418	004252	004537	015510		JSR	R5,REST		RESTORE CPU REGS
419	004256	000205			RTS	R5		AND RETURN TO CALLER
420	004260	012705	000003		SKDON:	MOV	#3,R3	COMPUTE LOOPSIZE
421	004264	160103			SUB	R1,R3		
422	004266	005203			INC	R3		INSURE LOOP
423	004270	010337	001310		MOV	R3,TIMLP		AND MAKE NUMBER PERM.
424								
425								
426								
427								
428								
429								
430	004274	000761			BR	SEK8K		AND LEAVE
431								
432								
433								
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453								
454								
455								
456	004276	005737	001076		ROUEST:	TST	MULCPU	DO WE WANT THIS CONTROLLER?

CONTROLLER REQUEST ROUTINE

THIS ROUTINE REQUESTS COMMAND OF THE PHOENIX  
211 CONTROLLER IF THE MULTIPLE CPU OPTION IS  
INOPERATION.



457	004302	001434					BEQ	RQEX	;	EXIT IF NO
458	004304	005037	001150				CLR	INTFLG	;	RESET INTERRUPT FLAG
459	004310	105777	174464				TSTB	@DCSR	;	DO WE HAVE CONTROLLER ALREADY?
460	004314	100005					BPL	RQ2	;	REQUEST IT IF NO
461	004316	032777	000040	174454			BIT	#BITS,@DCSR	;	IS REQUEST SET?
462	004324	001421					BEQ	RQ3	;	EXIT IF NO
463	004326	000426					BR	RQ1	;	CHECK FOR ERROR
464	004330	012777	000100	174442	RQ2:		MOV	#INTON,@DCSR	;	SET INTERRUPT BIT
465	004336	053777	001102	174434			BIS	MCPU,@DCSR	;	REQUEST 211
466	004344	004537	017342				JSR	R5,WAIT	;	WAIT FOR INTERRUPT
467	004350	005737	001150				TST	INTFLG	;	INTERRUPT?
468	004354	001407					BEQ	RQEX	;	EXIT IF NO
469	004356	005037	001150				CLR	INTFLG	;	CLEAR INTERRUPT FLAG(NOT A FUNCTION TESTED)
470	004362	105777	174412				TSTB	@DCSR	;	DO WE HAVE THE 211?
471	004366	100406					BHI	RQ1	;	CONTINUE IF YES
472	004370	005237	001322		RQ3:		INC	ERRFLG	;	SET ERROR FLAG IF NO
473	004374	042777	000136	174376	RQEX:		BIC	#FUNC,@DCSR	;	CLEAR FUNCTION BITS
474	004402	000205					RTS	R5	;	AND RETURN
475	004404	005777	174370		RQ1:		TST	@DCSR	;	ERROR IN FORMATTER?
476	004410	100371					BPL	RQEX	;	EXIT IF NO
477	004412	042777	000136	174360			BIC	#FUNC,@DCSR	;	LOOSE FUNCTION BITS IF YES
478	004420	052777	000041	174352			BIS	#SYSLRIBITS,@DCSR	;	ISSUE FORMATTER CLEAR HERE
479	004426	000240					NOP			
480	004430	013777	001102	174342			MOV	MCPU,@DCSR	;	RESELECT FORMATTER(WE HAD IT ONCE)
481	004436	000240					NOP			
482	004440	000240					NOP			
483	004442	000240					NOP			
484	004444	000753					BR	RQEX	;	EXIT EITHER WAY
485							;			
486							;			
487							;			
488							;			
489							;			
490							;			
491							;			
492							;			
493							;			
494							;			
495							;			
496							;	PHGR.P11	6-JAN-77	
497							;			
498							;			
499							;			
500							;	PROGRAM MANAGER		
501							;			
502							;			
503							;	THE PROGRAM HANGER IS USED TO DIRECT INPUT FROM		
504							;	THE KEYBOARD READER,ONLY TWO DECISIONS ARE MADE IN THIS CODE:		
505							;	1. TO WAIT FOR MORE INTERRUPTS(READER)		
506							;	2.TO ENTER COMMAND LINE INTERPRETER.		
507							;			
508							;	ENTRY IS BY FORCING PC THRU RTI OR		
509							;	BY A SUBROUTINE CALL.		
510							;			
511							;			
512							;			
513	004446						INWAIT:			



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TTY INPUT ROUTINE

THIS ROUTINE ACCEPTS INPUT FROM THE  
MONITOR AND STORES IT IN AN AREA FOR USE  
LATER AS A COMMAND FUNCTION OR AS A DISK/TEST PARAMETER.  
THE ONLY REQUIREMENT FOR DATA ENTRY IS THAT REGISTER  
R4 POINTS TO THE COMMAND BLOCK USED TO DEFINE ENTRY BUFFERS  
AND SPECIAL FUNCTIONS. THIS ROUTINE IS CALLED ONLY BY THE  
MONITOR INTERRUPT SERVICE CODE.

589	004650	005237	005536	TTYIN:	INC	ECHOEM	;	SET ECHO MODE FOR OUTPUT
591	004654	004537	015474		JSR	R5,SAVE	;	SAVE CPU
593	004660	005737	001150		TST	INTFLG	;	INTERRUPT FLAG SET?
594	004664	001002			BNE	TTZ	;	GO ON IF YES
595	004666	000137	005336		JMP	TIBAD	;	STOP IF NO
598	004672	005037	001150	TTZ:	CLR	INTFLG	;	RESET FLAG IF SET
601	004676	005737	005720		TST	TTYINT	;	INPUT FLAG SET?
602	004702	001002			BNE	TTZ	;	GO ON IF YES
603	004704	000137	005336		JMP	TIBAD	;	STOP IF NO
606	004710	005037	005720	TTZZ:	CLR	TTYINT	;	RESET IF YES
609	004714	005737	005536		TST	TTYACT	;	ARE WE ON A LINE?
610	004720	001005			BNE	TT1	;	YES SKIP BUFFER INIT
611	004722	013737	005544	005546	MOV	PARMB,PPARB	;	START INPUT AT BEGINNING OF BUFFER
612	004730	005237	005536		INC	TTYACT	;	AND SET LINE ACTIVE FLAG
615	004734	117700	000764	TT1:	MOVB	@TKB,RO	;	FETCH READER WORD
616	004740	005277	000756		INC	@TKS	;	SET READER ENABLE
617	004744	142700	000200		BICB	#200,RO	;	LOSE PARITY BIT
618	004750	001003			BNE	TT2	;	CONTINUE PROCESSING IF NOT NULL
619	004752	005037	005536		CLR	TTYACT	;	RESET ACTIVE STATUS
620	004756	000207			RTS	PC	;	AND LEAVE
624	004760	123700	005732	TT2:	CMPB	CONC,RO	;	IS IT A 'C' ?
625	004764	001447			BEQ	TT8	;	IF YES OUTPUT IT



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685 ) -----
686 )
687 )
688 )
689 ) THIS ROUTINE CONTROLS THE OUTPUT TO THE
690 ) CONSOLE DEVICE, EITHER AN ECHO CHARACTER
691 ) FROM THE KEYBOARD OR A COMPLETE MESSAGE FROM
692 ) A COMMAND.
693 )
694 )
695 )
696 )
697 )
698 ) CALLING SEQUENCE# JSR PC,TTYOUT
699 )
700 ) OR JSR PC,TT08
701 )
702 ) R4 = ADDRESS OF COMMAND BLOCK
703 )
704 )
705 )
706 005134 004537 015474 TTYOUT# JSR R5,SAVE ;SAVE CPU REGISTERS
707 005140 005037 001150 CLR INTFLG ;RESET INTERRUPT FLAGS
708 005144 005037 005716 CLR TTOINT ;INCLUDING PRINTER
709 )
710 )
711 )
712 005150 005737 005534 TT02# TST ECHOEM ;ECHO MODE?
713 005154 001407 BEQ TT05 ;PRINT STRAIGHT LINE IF NO
714 )
715 )
716 )
717 005156 005737 005536 TT03# TST TTYACT ;END OF INPUT?
718 005162 001452 BEQ TT05 ;PRINT CR/LF IF YES
719 )
720 )
721 )
722 005164 013702 005546 TT04# MOV PPARMB,R2 ;LOAD CHARACTER ADDRESS
723 005170 005302 DEC R2 ;MAKE ACCURATE ADDRESS
724 005172 000402 BR TT06 ;START PRINT PROCESS
725 )
726 )
727 )
728 005174 013702 005526 TT05# MOV MSGADR,R2 ;POINT R2 TO MESSAGE ADDRESS
729 )
730 )
731 )
732 005200 005046 TT06# CLR -(SP) ;DRAG CPU STATUS DOWN
733 005202 012746 005210 MOV #TT07,-(SP) ;AND FAKE INTERRUPT
734 005206 000002 RTI ;RTI TO LOAD PROCESSOR STATUS WORD
735 )
736 )
737 )
738 005210 012777 000100 000510 TT07# MOV #INTON,#ATPS ;ENABLE INTERRUPTS
739 005216 111277 000506 MCVB (R2),#TPB ;PRINT CHARACTER
740 005222 004537 017342 JSR R5,WAIT ;WAIT FOR INTERRUPT
741 )

```









913	005510	122	122	.ASCII /RR/ .WORD RCREAD	;REGISTER READ COMMAND ; RR
914	005512	013564			
915					
916	005514	120	103	.ASCII /PC/ .WORD PASS	;PASS COUNT PRINTOUT ; PC
917	005516	011640			
918					
919					
920					
921	005520	000000		.WORD 0	
922					
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939	005522			CONBL:	
940	005522	000000		CIMODE: .WORD 0	;COMMAND MODE FLAG
941	005524	000000		TSTACT: .WORD 0	;TEST ACTIVE FLAG
942	005526	000000		MSGADR: .WORD 0	;MESSAGE ADDRESS FOR TTY OUT
943	005530	000000		NCR: .WORD 0	;INHIBIT CR FLAG
944	005532	000000		KEOFLG: .WORD 0	;CLI REQUEST FLAG
945	005534	000000		ECHOEM: .WORD 0	;ECHO MODE TTY
946	005536	000000		TTYACT: .WORD 0	;TTY ACTIVE MODE
947	005540	000000		NUMBER: .WORD 0	;NUMBER MODE(INPUT)
948	005542	000000		TRASH: .WORD 0	; SKIP HEADING FLAG
949	005544	005550		PARMB: .WORD TTBUF	;INPUT BUFFER FOR TTY
950	005546	005550		PPARMB: .WORD TTBUF	;POINTER FOR TTY BUFFER
951					
952	005550	000000		TTBUF: .WORD 0	;START OF BUFFER
953		005716		.=. +100.	;BUFFER SIZE=100.
954					
955					
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961					
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964					
965					
966	005716	000000		TTINT: .WORD 0	;TTY INTERRUPT FLAG
967	005720	000000		TTYINT: .WORD 0	;TTY INTERRUPT FLAG (INPUT)
968					
969	005722	177560		TKS: .WORD 177560	;KEYBOARD READER STATUS REGISTER

COMMAND BLOCK

THIS CONTROL BLOCK CONTAINS ALL INFORMATION NECESSARY TO PERFORM ALL INPUT AND OUTPUT FUNCTIONS ALL WELL AS FLAG CERTAIN PARAMETERS DURING A TESTING COMMAND.

OFFSETS IN CONTROL BLOCK

-----

970	005724	177562		TKB:	WORD 177562		KEYBOARD READER BUFFER REGISTER
971	005726	177564		TPS:	WORD 177564		PRINTER STATUS REGISTER
972	005730	177566		TPB:	WORD 177566		PRINTER BUFFER REGISTER
973							
974	005732	000003		CONC:	WORD 3		CONTROL C
975	005734	000025		CONU:	WORD 25		CONTROL U
976	005736	000177		RUB:	WORD 177		RUB OUT
977	005740	000012		LFCODE:	WORD 12		LINE FEED
978	005742	000015		CRCODE:	WORD 15		CARRIAGE RETURN
979	005744	000000		IGERR:	HALT		CRASH IF I/O ERROR
980	005746	000000		ITWORK:	WORD 0		TEMP LOCATION
981	005750	000000		ITINT:	WORD 0		SAVE LOCATIONS FOR ACTIVE TEST INTERRUPT
982	005752	000000			WORD 0		
983	005754	000000			WORD 0		
984	005756	000000			WORD 0		
985	005760	000000			WORD 0		
986	005762	000000			WORD 0		
987	005764	000000			WORD 0		
988	005766	000000			WORD 0		
989							
990							TTY INPUT SERVICE ROUTINES
991							-----
992							
993							
994	005770	005237	001150	TTISEV:	INC	INTFLG	SET GENERAL INTERRUPT SERVICE
995	005774	005237	005720		INC	TTYINT	SET READER INTERRUPT FLAG
996							
997							
998	006000	005777	177716	TS1:	TST	@TKS	ERRORS?
999	006004	000411			BR	TS3	IGNORE THEM NOW
1000							
1001							
1002	006006	005237	001322		INC	ERRFLG	SET GENERAL ERROR FLAG
1003	006012	005046			CLR	-(SP)	FORCE CPU LEVEL DOWN
1004	006014	005066	177776		CLR	-2(SP)	FORCE CPU LEVEL DOWN
1005	006020	012766	005744 177774		MOV	#IOERR,-4(SP)	AND POINT PC TO ERROR ROUTINE
1006							
1007							
1008	006026	000002		TS2:	RTI		EXIT HERE
1009							
1010							
1011	006030	005737	005524	TS3:	TST	TSTACT	CURRENTLY TESTING?
1012	006034	001774			BEQ	TS2	EXIT IF NOT
1013							
1014							
1015	006036	127737	177662 005732		CMPB	@TKB,CONC	IS IT A CONTROL C
1016	006044	001405			BEQ	TS3A	SET UP TO CANCEL TESTING
1017							
1018							
1019	006046	005037	001150		CLR	INTFLG	RESET INTERRUPT FLAG
1020	006052	005037	005720		CLR	TTYINT	
1021	006056	000763			BR	TS2	AND GO BACK TO TESTING
1022							
1023							
1024	006060	005037	005524	TS3A:	CLR	TSTACT	RESET ACTIVE FLAG
1025	006064	010037	005750		MOV	RO,TSTINT	START SAVING
1026	006070	012700	005750		MOV	#TSTINT,RO	LOAD SAVE ADDRESS FOR CPU



1084	006214	005037	005522		CLR	CIMODE	);RESET COMMAND MODE
1085	006220	005037	005534		CLR	ECHOEM	);REST ECHO MODE
1086	006224	005037	005530		CLR	NCR	);RESET CARRIAGE RETURN INHIBIT
1087	006230	005037	005524		CLR	TSTACT	);RESET TEST ACTIVE MODE
1088	006234	005037	005532		CLR	REQFLG	);RESET REQUEST FLAG
1089	006240	005037	005720		CLR	TTYINT	);RESET INTERRUPT FLAG
1090	006244	005037	005716		CLR	TTOINT	);BOTH IN AND OUTPUT
1091					;		
1092	006250	012777	000100	177444	MOV	#100,WTKS	);SET INTERRUPT ENABLE
1093	006256	012777	000100	177442	MOV	#100,WTPS	);FOR READER AND PRINTER
1094	006264	005277	177432		INC	WTKS	);ENABLE READER
1095					;		
1096	006270	005737	005542	TRSH1	TST	TRASH	);SKIP ALL THIS BALONEY?
1097	006274	001402			BEO	TRSH1	);NO PRINT IT
1098	006276	000137	004506		JMP	PHG1	);YES WAIT FOR INPUT
1099					;		
1100	006302			TRSH1:			
1101					;		
1102					;		
1103	006302	012737	005742	005526	MOV	#CRCODE,MSGADR	);SET UP FOR CLEAN SCREEN
1104	006310	004737	005134		JSR	PC,TTYOUT	);ISSUE CR
1105	006314	012737	005740	005526	MOV	#LFCODE,MSGADR	);NOW ISSUE LINE FEED
1106	006322	004737	005134		JSR	PC,TTYOUT	);
1107					;		
1108					;		
1109	006326	012737	006424	005526	MOV	#P2MSG,MSGADR	);ENTER OUTPUT MESSAGE ADDRESS
1110	006334	004737	005134		JSR	PC,TTYOUT	);PRINT HEADING
1111	006340	012737	006507	005526	MOV	#STRMSG,MSGADR	);UNDER LINE HEADING
1112	006346	004737	005134		JSR	PC,TTYOUT	);HERE
1113					;		
1114					;		
1115	006352	012737	005740	005526	MOV	#LFCODE,MSGADR	);PRINT 2 LINE FEEDS HERE
1116	006360	004737	005134		JSR	PC,TTYOUT	);
1117	006364	004737	005134		JSR	PC,TTYOUT	);
1118					;		
1119	006370	012737	006603	005526	MOV	#P3MSG,MSGADR	);NOW TELL PEOPLE ABOUT ANSWERS
1120	006376	004737	005134		JSR	PC,TTYOUT	);
1121					;		
1122	006402	012737	005740	005526	MOV	#LFCODE,MSGADR	);ONE LINE FEED HERE
1123	006410	004737	005134		JSR	PC,TTYOUT	);
1124					;		
1125					;		
1126	006414	004737	005134		JSR	PC,TTYOUT	);
1127					;		
1128					;		
1129	006420	000137	010676		JMP	DATE	);ASK FOR DATA NOW
1130							);PROGRAM MANAGER
1131					;		
1132					;		
1133					;		
1134					;		
1135					;		
1136					;		
1137					;		
1138					;		
1139					;		
1140	006424	040	040	040	P2MSG:	ASCII /	PHOENIX 211 DISK CONTROLLER DIAGNOSTIC /

	006427	040	040	040	
	006432	040	040	040	
	006435	040	040	120	
1	006440	110	117	105	
2	006443	116	111	130	
3	006446	040	062	061	
4	006451	061	040	104	
5	006454	111	123	113	
6	006457	040	103	117	
7	006462	116	124	122	
8	006465	117	114	114	
9	006470	105	122	040	
10	006473	104	111	101	
11	006476	107	116	117	
12	006501	123	124	111	
13	006504	103	040		
14	1141 006506	000			.BYTE 0
15	1142 006507	052	052	052	STRMSG: .ASCII /*****
16	006512	052	052	052	
17	006515	052	052	052	
18	006520	052	052	052	
19	006523	052	052	052	
20	006526	052	052	052	
21	006531	052	052	052	
22	006534	052	052	052	
23	006537	052	052	052	
24	006542	052	052	052	
25	006545	052	052	052	
26	006550	052	052	052	
27	006553	052	052	052	
28	006556	052	052	052	
29	006561	052	052	052	
30	006564	052	052	052	
31	006567	052	052	052	
32	006572	052	052	052	
33	006575	052	052	052	
34	006600	052	052		
35	1143 006602	000			.BYTE 0
36	1144 006603	040	040	040	P3MSG: .ASCII / TYPE H <CR> FOR HELP/
37	006606	040	040	124	
38	006611	131	120	105	
39	006614	040	040	110	
40	006617	040	074	103	
41	006622	122	076	040	
42	006625	040	106	117	
43	006630	122	040	110	
44	006633	105	114	120	
45	1145 006636	000			.BYTE 0
46	1146				;
47	1147				.EVEN
48	1148				;
49	1149				;
50	1150				;
51	1151				;
52	1152				;
53	1153				;
54	1154				;

```

1155 ; ASCII NUMBER CONVERSION
1156 ;
1157 ; THIS ROUTINE CONVERTS AN ASCII NUMBER
1158 ; INTO OCTAL FORMAT.
1159 ; THE NUMBER TO BE CONVERTED IS LOCATED STARTING
1160 ; AT INPUT BUFFER "PARMB" AND IS ENDED
1161 ; BY DETECTING A CR WORD
1162 ;
1163 ; NO CHARACTERS LARGER THAN A 7 ARE ACCEPTED
1164 ; AND IF A BAD CHARACTER IS RECEIVED,
1165 ; THE FLAG "BADNUM" IS SET.
1166 ;
1167 ; THE OCTAL NUMBER IS LOCATED IN "DATA" AT
1168 ; EXIT
1169 ;
1170 ;
1171 006640 010046 OCTAL: MOV RO,-(SP) ;SAVE RO,R1,R2
1172 006642 010146 MOV R1,-(SP) ;
1173 006644 010246 MOV R2,-(SP) ;
1174 006646 005037 006750 CLR BADNUM ;START CLEAN
1175 006652 013701 005544 MOV PARMB,R1 ;POINT TO INPUT BUFFER
1176 006656 005000 CLR RO ;CLR RO
1177 006660 111102 COCTI: MOVB (R1),R2 ;FETCH CHARACTER
1178 006662 162702 000060 SUB #60,R2 ;LOSE ASCII PART
1179 006666 100417 BMI COCTER ;LEAVE IF ERROR
1180 006670 022702 000010 CMP #10,R2 ;SEE IF GREATER THAN 7
1181 006674 002414 BLT COCTER ;LEAVE IF YES WITH ERROR
1182 006676 006100 ROL RO ;SHIFT DOWN THREE BITS FOR
1183 006700 103412 BCS COCTER ;OVERFLOW = ERROR
1184 006702 006100 RGL RO ;
1185 006704 103410 BCS COCTER ;
1186 006706 006100 ROL RO ;
1187 006710 103406 BCS COCTER ;
1188 006712 060200 ADD R2,RO ;LOAD FINISHED CHARACTER
1189 006714 105721 TSTB (R1)+ ;LOOK AT NEXT CHARACTER
1190 006716 121127 000015 COCTDN: CMPB (R1),#CR ;CARRIAGE RETURN?
1191 006722 001404 BEQ COCEX ;EXIT IF YES
1192 006724 000755 BR COCTI ;
1193 006726 005237 006750 COCTER: INC BADNUM ;SET BAD NUMBER FLAG
1194 006732 000402 BR CEXIT ;AND LEAVE
1195 ;
1196 ;
1197 006734 010037 006752 COCEX: MOV RO,DATA ;LOAD GOOD NUMBER
1198 ;
1199 ;
1200 006740 012602 CEXIT: MOV (SP)+,R2 ;RELOAD REGS
1201 006742 012601 MOV (SP)+,R1 ;
1202 006744 012600 MOV (SP)+,RO ;
1203 006746 000207 RTS PC ;AND LEAVE
1204 ;
1205 006750 000000 BADNUM: .WORD 0 ;BAD DATA WORD FLAG
1206 ;
1207 006752 000000 DATA: .WORD 0 ;CONVERTED ASCI TO OCTAL WORD
1208 ;
1209 ;
1210 ;
1211 ;

```

```

1212      ;
1213      ;
1214      ;
1215      ;          OCTAL TO ASCII CONVERSION ROUTINE
1216      ;
1217      ;
1218      ;          THIS ROUTINE CONVERTS AN OCTAL NUMBER TO IT'S
1219      ;          ASCII EQUIVALENT.
1220      ;
1221      ;
1222      ;
1223      ;          THE NUMBER TO BE WORKED ON SHOULD
1224      ;          THE NUMBER TO BE CONVERTED IS IN REG R3
1225      ;          THE OUTPUT GENERATED WILL BE IN OUTBUF AREA
1226      ;          AND A NULL WILL TERMINATE STRING.
1227      ;
1228      ;
1229 006754 010146          ASCII: MOV    R1,-(SP)          ;SAVE R1,R2,R3
1230 006756 010246          MOV    R2,-(SP)          ;
1231 006760 012746 000005  MOV    #5,-(SP)          ;SET COUNTER
1232      ;
1233 006764 012701 010574  MOV    #OUTBUF,R1      ;POINT TO BUFFER AREA
1234 006770 000241          CLC                    ;CLEAR CARRY BIT
1235 006772 006103          RCL    R3              ;SHIFT CARRY IN
1236 006774 006103          ROL    R3              ;INTO BIT 0
1237 006776 010302          MOV    R3,R2          ;LOAD INTO R2
1238 007000 006003          ROR    R3              ;RETURN CARRY INTO R3
1239 007002 042702 177776  BIC    #177776,R2      ;LOOSE GARBAGE
1240 007006 062702 000060  ADD    #60,R2          ;MAKE ASCII
1241 007012 110221          MOVB  R2,(R1)+         ;LOAD INTO BUFFER AREA
1242 007014 006103          CASCI: RCL    R3      ;NOW SHIFT HALF BYTES IN
1243 007016 006103          ROL    R3              ;
1244 007020 006103          ROL    R3              ;
1245 007022 006103          ROL    R3              ;
1246 007024 010302          MOV    R3,R2          ;LOAD INTO R2 FOR CONVERSION
1247 007026 006003          ROR    R3              ;RETURN CARRY BIT INTO R3
1248 007030 042702 177770  BIC    #177770,R2      ;LOOSE GARBAGE AGAIN
1249 007034 062702 000060  ADD    #60,R2          ;MAKE HALF BYTE ASCII
1250 007040 110221          MOVB  R2,(R1)+         ;LOAD IN OUPUT BUFFER
1251 007042 005316          DEC    (SP)           ;DECREMENT SHIFT COUNTER
1252 007044 001363          BNE  CASCI           ;GO ON IF MORE
1253 007046 005011          CLR    (R1)           ;SET NULL FOR OUPUT FLAG FINISH
1254 007050 005726          TST    (SP)+         ;FIX STACK
1255 007052 012602          MOV    (SP)+,R2      ;RESTORE R2 REG.
1256 007054 012601          MOV    (SP)+,R1      ;AND R1
1257 007056 000207          RTS    PC            ;LEAVE THIS PLACE
1258      ;
1259      ;
1260      ;
1261      ;
1262      ;          MISC. OUTPUT MESSAGES
1263      ;
1264      ;
1265 007060 077          QUEST:  .ASCII /?/
1266 007061 000          .BYTE 0
1267 007062 052          PROMPT: .ASCII /#/
1268 007063 007          .BYTE 7
    
```







1	007433	117	116	040				
2	007436	105	122	122				
3	007441	117	122	040				
4	007444	050	124	105				
5	007447	123	124	123				
6	007452	040	063	061				
7	007455	054	063	062				
8	007460	040	117	116				
9	007463	114	131	051				
10	007466	040	077	040				
11	007471	151	040	117				
12	007474	122	040	116				
13	007477	040						
14	1361	007500	000		.BYTE 0			
15	1362				.EVEN			
16	1363							
17	1364							
18	1365							
19	1366							
20	1367							
21	1368							
22	1369							
23	1370							
24	1371							
25	1372							
26	1373							
27	1374							
28	1375							
29	1376							
30	1377							
31	1378							
32	1379							
33	1380							
34	1381							
35	1382							
36	1383							
37	1384							
38	1385							
39	1386							
40	1387							
41	1388							
42	1389							
43	1390	060040			SPACE=40			
44	1391	007502	012037	005526	LOADIN: MOV	(R0)+,MSGADR		SPACE DEFINITION
45	1392	007506	005037	005534	CLR	ECHOEM		POINT TO MESSAGE ADDRESS
46	1393	007512	005237	005530	INC	NCR		RESET ECHO MODE
47	1394	007516	004737	005134	JSR	PC,TTYOUT		SET NO CR FLAG
48	1395	007522	005737	005540	TST	NUMBER		TYPE QUESTION
49	1396	007526	001415		BEO	LD1A		PRINT DEFAULT?
50	1397	007530	011203		MOV	(R2),R3		GO NO IF NO
51	1398	007532	004737	006754	JSR	PC,ASCII		SET UP TO PRINT IF YES
52	1399	007536	012737	010574	MOV	OUTBUF,MSGADR		MAKE ASCII
53	1400	007544	004737	005134	JSR	PC,TTYOUT		LOAD OUTPUT BUFFER
54	1401							OUTPUT IT
55	1402	007550	012737	000040	MOV	SPACE,OUTBUF		INCLUDE SPACE
56	1403	007556	004737	005134	JSR	PC,TTYOUT		PRINT IT
57	1404							

LOADIN .P11 11-JAN-78

THIS SUBROUTINE IS USED BY SEVERAL MONITOR  
 COMMANDS TO HANDLE INPUT FROM THE KEYBOARD.  
 THE EXPECTED DATA IS IN TWO FORMS, ONE IS  
 AN OCTAL NUMBER AND THE SECOND IS EITHER  
 A "Y" OR AN "N". ANY OTHER INPUT  
 WILL BE IGNORED. UPON ENTRY THE FLAG "NUMBER" MUST  
 BE SET IF THE INPUT DESIRED IS TO BE IN OCTAL FORM.

CALLING SEQUENCE: JSR PC,LOADIN

R0=MESSAGE ADDRESS  
 R1=# OF EXPECTED DATA LINES  
 R2=ADDRESS OF DATA LOCATIONS

1405	007562	004737	004446	LD1A:	JSR	PC,INWAIT	;	COLLECT ANSWER	
1406					;				
1407					;				
1408	007566	117703	175752	LD1:	MOV	QPARMB,R3	;	FETCH FIRST ENTRY	
1409	007572	042703	000200		BIC	#BIT7,R3	;	LOSE PARITY BIT	
1410	007576	020327	000015		CMR	R3,#CR	;	CARRIAGE RETURN?	
1411	007602	001013			BNE	LD3	;	GO ON IF NO	
1412					;				
1413					;				
1414	007604	005722		LD2:	TST	(R2)+	;	DEFAULT ANSWER	
1415	007606	012737	005740	005526	MOV	#LFCODE,MSGADR	;	ISSUE LINE FEED HERE	
1416	007614	005037	005534		CLR	ECHOEM	;	RESET ECHO MODE	
1417	007620	004737	005134		JSR	PC,TTYOUT	;	PRINT IT	
1418					;				
1419					;				
1420	007624	005301			DEC	R1	;	DECREMENT ENTRY NUMBER	
1421	007626	001325			BNE	LOADIN	;	DO ANOTHER	
1422	007630	000207		LDEX:	RTS	PC	;	RETURN HERE	
1423					;				
1424					;				
1425	007632	020327	000105	LD3:	CMR	R3,#105	;	IS IT AN "E"	
1426	007636	001774			BEO	LDEX	;	EXIT IF YES	
1427					;				
1428					;				
1429	007640	005737	005540	LD4:	TST	NUMBER	;	EXPECTING NUMBER?	
1430	007644	001423			BEO	LD7	;	CHK IT IF YES	
1431	007646	004737	006640		JSR	PC,OCTAL	;		
1432	007652	005737	006750		TST	BADNUM	;	GOOD?	
1433	007656	001413			BEO	LD6	;	GO ON IF YES	
1434					;				
1435					;				
1436	007660	012737	007060	005526	LD5:	MOV	#QUEST,MSGADR	;	LOAD ADDR OF "Q"
1437	007666	005037	005534		CLR	ECHOEM	;	RESET ECHO MODE	
1438	007672	005037	005530		CLR	NCR	;	RESET CR INHIBIT	
1439	007676	004737	005134		JSR	PC,TTYOUT	;		
1440	007702	024042			CMR	-(R0),-(R2)	;	RESET POINTERS	
1441	007704	000676			BR	LOADIN	;	TRY IT AGAIN	
1442					;				
1443					;				
1444	007706	013712	006752	LD6:	MOV	DATA,(R2)	;	ENTER DATA WORD	
1445	007712	000734			BR	LD2	;	AND GO ON	
1446					;				
1447					;				
1448	007714	020327	000131	LD7:	CMR	R3,#131	;	SEE IF	
1449	007720	001002			BNE	LD10	;	IT IS A "Y"	
1450	007722	005212			INC	(R2)	;	SET FLAG IF YES	
1451	007724	000727			BR	LD2	;	AND GO ON	
1452					;				
1453					;				
1454	007726	020327	000116	LD10:	CMR	R3,#116	;	IS IT AN "N"	
1455	007732	001352			BNE	LD5	;	IGNORE IT IF NO	
1456	007734	005012			CLR	(R2)	;	RESER FLAG IF YES	
1457	007736	000722			BR	LD2	;	AND GO ON	
1458					;				
1459					;				
1460					;				
1461					;				

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1471
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1474
1475 007740 005037 005532      DISKIN: CLR      REOFLG      )RESET REQUEST FLAG
1476 007744 005037 005524      CLR      TSTACT      )RESET TEST ACTIVE
1477 007750 005037 005534      CLR      ECHOEM      )RESET ECHO MODE
1478 007754 005237 005522      INC      CIMODE      )SET COMMAND MODE
1479 007760 004537 015474      JSR      R5,SAVE      )SAVE CPU
1480 007764 012700 001642      MOV      #DISKP,R0    )R0 IS ADDRESS OF MESSAGES
1481 007770 012701 000004      MOV      #4,R1        )R1= NUMBER OF ENTRIES
1482 007774 012702 001040      MOV      #MAXSEC,R2   )R2=PARAMETER ADDRESS
1483 010000 005237 005540      INC      NUMBER
1484 010004 004737 007502      JSR      PC,LOADIN    )ENTER DATA
1485 010010 005037 005540      CLR      NUMBER      )CLR NUMBER FLAG
1486 010014 005037 005522      CLR      CIMODE      )RESET COMMAND MODE
1487 010020 013737 001042 001060  MOV      MAXHD,MAXHD  )FIX HEAD SELECTION
1488 010026 012702 000007      MOV      #7,R2        )SHIFT
1489 010032 006237 001060      DISKHD: ASR      MAXHD  )SHIFT
1490 010036 005302      DEC      R2           )
1491 010040 001374      BNE      DISKHD      )REPEAT UNTIL DONE
1492 010042 013737 001046 001050  MOV      WPSEC,POSWP  )
1493 010050 005437 001050      NEG      POSWP        )MAKE POSITIVE WORDS PER SECTOR
1494 010054 004537 015510      JSR      R5,REST     )RESTORE CPU
1495 010060 000137 004506      JMP      PMG1        )WAIT FOR NEXT STUFF
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509 010064 005037 005532      RUN:  CLR      REOFLG      )RESET REQUEST FLAG
1510 010070 005037 005522      CLR      CIMODE      )
1511 010074 005237 005524      INC      TSTACT      )SET TEST ACTIVE FLAG
1512 010100 023727 001212 000045  CMP      STRTN,#45    ) DID WE JUST DO A FORMAT?
1513 010106 001005      BNE      RUN1        ) GO ON IF NO
1514
1515 010110 005037 001212      CLR      STRTN       ) DEFAULT TO TEST 0
1516 010114 012737 000030 001210  MOV      #30,STPTN   ) AND END WITH 30
1517
1518 010122      RUN1:

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1519	010122	000137	003044	JMP	TSTART	;	START TESTING
1520						;	
1521						;	
1522						;	
1523						;	
1524						;	
1525						;	
1526						;	
1527						;	
1528						;	
1529						;	
1530						;	PRINT PROGRESS COMMAND
1531						;	
1532						;	THIS COMMAND PRINTS THE CURRENT TEST PROGRESS
1533						;	OF THE PHOENIX 211 CONTROLLER. THE VALUES OUTPUTED
1534						;	ARE THE FOLLOWING:
1535						;	
1536						;	1. PASS COUNT
1537						;	2. PASS DEFINITION (STARTING AND ENDING TEST)
1538						;	3. CURRENT TEST
1539						;	4. ERROR COUNT
1540						;	5. DATE
1541						;	
1542						;	
1543						;	
1544	010126	004537	015474	PRINT:	JSR	R5,SAVE	SAVE CPU
1545	010132	005037	005524		CLR	TSTACT	RESET TEST ACTIVE
1546	010136	005237	005522		INC	CIMODE	SET COMMAND MODE
1547	010142	005037	005534		CLR	ECHOEM	CLEAR ECHO MODE
1548	010146	005037	005532		CLR	REOFLG	RESET REQUEST FLAG
1549	010152	012737	010334	005526	MOV	#PNTMSG,MSGADR	LOAD PRINT HEADING
1550	010160	004737	005134		JSR	PC,TTYOUT	PRINT IT
1551	010164	012737	005740	005526	MOV	#LFCODE,MSGADR	LINE FEED
1552	010172	004737	005134		JSR	PC,TTYOUT	
1553	010176	004737	005134		JSR	PC,TTYOUT	
1554							
1555							
1556	010202	005237	005530		INC	NCR	INHIBIT CR
1557	010206	012737	002045	005526	MOV	#DTE,MSGADR	POINT TO DATE MESSAGE
1558	010214	004737	005134		JSR	PC,TTYOUT	PRINT DATE
1559	010220	005037	005530		CLR	NCR	RESER CR INHIBIT
1560	010224	005037	005524		CLR	TSTACT	RESET TEST ACTIVE
1561	010230	012737	011222	005526	MOV	#DATE,MSGADR	POINT TO ACTUAL DATE
1562	010236	004737	005134		JSR	PC,TTYOUT	PRINT DATE
1563							
1564							
1565	010242	012737	005740	005526	MOV	#LFCODE,MSGADR	PRINT LINE FEED (2)
1566	010250	004737	005134		JSR	PC,TTYOUT	
1567	010254	004737	005134		JSR	PC,TTYOUT	
1568							
1569							
1570	010260	004537	013104		JSR	R5,POUT	PRINT TEST PARAMETERS
1571	010264	010322				WORD PRMSG	TEST MESSAGES
1572	010266	010306				WORD PRDATA	TEST P'S
1573	010270	000005				WORD 5	NUMBER OF MESSAGES
1574							
1575							

1576 010272 005037 005522  
 1577 010276 004537 015510  
 1578 010302 000137 004506

CLR  
 JSR R5,REST  
 JMP PHG1

);RESET COMMAND MODE  
 );RESTORE CPU  
 );DO SOMETHING ELSE

1579  
 1580  
 1581  
 1582

DATA TABLE OF LOCS FOR PRINT COMMAND

1583 010306 001236  
 1584 010310 001212  
 1585 010312 001210  
 1586 010314 001232  
 1587 010316 001322  
 1588 010320 000000

PRDATA: ;WORD PASCNT  
 ;WORD STRN  
 ;WORD STPIN  
 ;WORD CURTN  
 ;WORD ERRFLG  
 ;WORD 0

);PASS COUNTER  
 );STARTING TEST NUMBER  
 );ENDING TEST NUMBER  
 );CURRENT TEST NUMBER  
 );ERROR FLAG  
 );WHO KNOWS?

1589  
 1590  
 1591  
 1592  
 1593  
 1594

PRINT COMMAND MESSAGES

1595  
 1596  
 1597

1598 010322 010403  
 1599 010324 010434  
 1600 010326 010464  
 1601 010330 010514  
 1602 010332 010544

PRMSG: ;WORD PASHSG  
 ;WORD T1MSG  
 ;WORD T2MSG  
 ;WORD CMSSG  
 ;WORD ERCNTM

);PASS COUNT MESSAGE  
 );STARTING TEST MESSAGE  
 );ENDING TEST MESSAGE  
 );CURRENT TEST MESSAGE  
 );ERROR FLAG MESSAGE

1603  
 1604  
 1605

1606 010334 011 120 110  
 010337 117 105 116  
 010342 111 130 040  
 010345 062 061 061  
 010350 040 104 111  
 010353 101 107 116  
 010356 117 123 124  
 010361 111 103 040  
 010364 124 105 123  
 010367 124 040 120  
 010372 122 117 107  
 010375 122 105 123  
 010400 123 040

PNTMSG: ;ASCII / PHOENIX 211 DIAGNOSTIC TEST PROGRESS /

1607 010402 000  
 1608 010403 120 101 123  
 010406 123 040 103  
 010411 117 125 116  
 010414 124 105 122  
 010417 040 040 040  
 010422 040 040 040  
 010425 040 040 040  
 010430 075 040

;BYTE 0  
 PASMSG: ;ASCII /PASS COUNTER = /

1609 010432 000  
 1610  
 1611 010434 123 124 101  
 010437 122 124 111  
 010442 116 107 040

;BYTE 0  
 ;EVEN  
 T1MSG: ;ASCII /STARTING TEST NUMBER = /

1	010445	124	105	123				
2	010450	124	040	116				
3	010453	125	115	102				
4	010456	105	122	040				
5	010461	075	040					
6	1612 010463	000			.BYTE 0			
7	1613 010464	105	116	104	TZMSG: .ASCII /ENDING	TEST NUMBER = /		
8	010467	111	116	107				
9	010472	040	040	040				
10	010475	124	105	123				
11	010500	124	040	116				
12	010503	125	115	102				
13	010506	105	122	040				
14	010511	075	040					
15	1614 010513	000			.BYTE 0			
16	1615 010514	103	125	122	CHSSG: .ASCII /CURRENT	TEST NUMBER = /		
17	010517	122	105	116				
18	010522	124	040	040				
19	010525	124	105	123				
20	010530	124	040	116				
21	010533	125	115	102				
22	010536	105	122	040				
23	010541	075	040					
24	1616 010543	000			.BYTE 0			
25	1617 010544	105	122	122	ERCNTM: .ASCII /ERROR	FLAG = /		
26	010547	117	122	040				
27	010552	040	040	040				
28	010555	106	114	101				
29	010560	107	040	040				
30	010563	040	040	040				
31	010566	040	040	040				
32	010571	075	040					
33	1618 010573	000			.BYTE 0			
34	1619				.EVEN			
35	1620				;			
36	1621				;			
37	1622				;			
38	1623 010574	000000			OUTBUF: .WORD 0	OUTPUT BUFFER ARE (TTY)		
39	1624	010676			.=.+100	;		
40	1625				;			
41	1626				;			
42	1627				;			
43	1628				;			
44	1629				;			
45	1630				;			
46	1631				;			
47	1632				;			
48	1633				;	DATE COMMAND		
49	1634				;			
50	1635				;	THE DATE COMMAND ENTERS THE DATE		
51	1636				;	INTO A MEMORY BUFFER FOR LATER USE		
52	1637				;	AS OUTPUT MESSAGE HEADING DATA.		
53	1638				;			
54	1639				;			
55	1640				;			
56	1641 010676	004537	015474		DATE: JSR	R5,SAVE	JSAVE CPU	
57	1642 010702	005037	005532		CLR	REOFLG	RESET REQUEST FLAG	

1	1643	010706	005237	005522		INC	CIMODE	);SET COMMAND MODE
2	1644	010712	005037	005534		CLR	ECHOEM	);RESET ECHO MODE
3	1645	010716	012737	002024	005526 DT1:	MOV	#DTADR,MSGADR	);POINT TO MESSAGE ADDRESS
4	1646	010724	005237	005530		INC	NCR	);SET CR INHIBIT
5	1647	010730	004737	005134		JSR	PC,TTYOUT	);PRINT "DATE"
6	1648	010734	005037	005530		CLR	NCR	);RESET CR INHIBIT
7	1649	010740	004737	004446		JSR	PC,INWAIT	);WAIT FOR RESPONSE
8	1650	010744	013702	005546		MOV	PPARM,R2	);LOAD ENDING DATA ADDRESS
9	1651	010750	013703	005544		MOV	PARMB,R3	);LOAD STARTING DATA ADDRESS
10	1652	010754	100302			SUB	R3,R2	);COMPUTE LENGTH OF DATE
11	1653	010756	020227	000012		CHP	R2,#12	);I1 CHARACTERS?
12	1654	010762	001027			BNE	DT5	);PRINT "?" IF NO
13	1655	010764	012700	011154		MOV	#MONTH,R0	);POINT TO MONTH TABLE
14	1656	010770	013702	005544	DT2:	MOV	PARMB,R2	);LOAD FIRST CHARACTER
15	1657	010774	010201			MOV	R2,R1	);SET UP R1 TO POINT TO DATA
16	1658	010776	062701	000003		ADD	#3,R1	);FIRST DATE LETTER IS THE
17	1659					;		);FOURTH CHARACTER RECEIVED
18	1660	011002	012702	000003		MOV	#3,R2	);LOAD MONTH COUNT
19	1661	011006	111003		DT3:	MOVB	(R0),R3	);LOAD TABLE ENTRY
20	1662	011010	120311			CHPB	R3,(R1)	);IS IT A LEGAL ENTRY?
21	1663	011012	001404			BEQ	DT4	);LOOK AT NEXT IF YES
22	1664	011014	060200			ADD	R2,R0	);UPDATE MONTH TABLE
23	1665	011016	105710			TSTB	(R0)	);END OF MONTHS?
24	1666	011020	001410			BEQ	DT5	);GO PRINT "?"
25	1667	011022	000762			BR	DT2	);TRY AGAIN IF NOT
26	1668					;		
27	1669					;		
28	1670	011024	020227	000001	DT4:	CHP	R2,#1	);LAST CHARACTER?
29	1671	011030	001416			BEQ	DT6	);STORE DATE IF YES
30	1672	011032	005200			INC	R0	);CHECK NEXT IF MORE
31	1673	011034	005201			INC	R1	);UPDATE DATA POINTER
32	1674	011036	005302			DEC	R2	);DECREMENT CHARACTER COUNTER
33	1675	011040	000762			BR	DT3	);CHECK THIS ONE
34	1676					;		
35	1677					;		
36	1678	011042	012737	007060	005526 DT5:	MOV	#QUEST,MSGADR	);LOAD "?" ADDRESS
37	1679	011050	005037	005534		CLR	ECHOEM	);RESET ECHOEM MODE
38	1680	011054	005037	005530		CLR	NCR	);RESET CR INHIBIT
39	1681	011060	004737	005134		JSR	PC,TTYOUT	);PRINT IT
40	1682	011064	000714			BR	DT1	);START OVER
41	1683					;		
42	1684					;		
43	1685	011066	013700	005544	DT6:	MOV	PARMB,R0	);R0 DATA BUFFER
44	1686	011072	012701	000011		MOV	#11,R1	);R1=DATA COUNTER
45	1687	011076	012702	011222		MOV	#DATBUF,R2	);R2=DATE RESIDENCE
46	1688	011102	112022		DT7:	MOVB	(R0)+,(R2)+	);LOAD DATE
47	1689	011104	005301			DEC	R1	);DECREMENT COUNTER
48	1690	011106	001375			BNE	DT7	);CONTINUE IF NOT DONE
49	1691	011110	105012			CLRB	(R2)	);INSURE PROPER OUPUT
50	1692					;		
51	1693					;		
52	1694					;		
53	1695	011112	012737	007062	005526	MOV	#PROMPT,MSGADR	);SET CR INHIBIT
54	1696	011120	005037	005534		CLR	ECHOEM	);REST ECHOEMODE
55	1697	011124	005237	005530		INC	NCR	);SET CR INHIBIT
56	1698	011130	004737	005134		JSR	PC,TTYOUT	);OUT PUT PROMPT
57	1699	011134	005037	005530		CLR	NCR	);RESET CR INHIBIT



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1700 ;
1701 ;
1702 ;
1703 ;
1704 011140 005037 005522 DT10: CLR CIMODE ;RESET COMMAND MODE
1705 011144 004537 015510 JSR RS,REST ;BRING BACK CPU
1706 011150 000137 004446 JHP PMGR ;DO SOMETHING ELSE
1707 ;
1708 ;
1709 ;
1710 ;
1711 ;
1712 ;
1713 ; MONTH TABLE FOR FINDING CORRECT DATE
1714 ;
1715 ;
1716 011154 112 101 116 MONTH: *ASCII /JANFEBMARAPRMYJUNJULAU GSEP OCTNOVDEC/
      011157 106 105 102
      011162 115 101 122
      011165 101 120 122
      011170 115 101 131
      011173 112 125 116
      011176 112 125 114
      011201 101 125 107
      011204 123 105 120
      011207 117 103 124
      011212 116 117 126
      011215 104 105 103
1717 011220 000 ;BYTE 0
1718 ; ;EVEN
1719 ;
1720 ;
1721 ; DATE BUFFER (HOLDS CURRENT DATE IN ASCII)
1722 ;
1723 ;
1724 011222 DATEW:
1725 011222 000000 DATEBUF: *WORD 0
1726 011236 ; ;=*+10*
1727 ;
1728 ;
1729 ;
1730 ;
1731 ; SCOPE MODE COMMAND
1732 ;
1733 ;
1734 ; THE SCOPE COMMAND IS USED ONLY FOR
1735 ; DEBUGGING PURPOSES.IT ALLOWS THE OPERATOR TO
1736 ; CHOSE THE FOLLOWING VALUES IN HIS SCOPR LOOP:
1737 ;
1738 ; 1. TYPE OF COMMAND
1739 ; 2.STARTING DUSH ADDRESS
1740 ; 3.STARTING CYLINDER(DCYL) ADDRESS
1741 ; 4.WORD COUNT (2'S COMPLEMENT)
1742 ;
1743 ; THE COMMAND WILL BE ISSUED VIA THE DATA TRANSFER
1744 ; SUBROUTINE (DXFER).IF THE CONTROLLER DOES NOT
1745 ; COMPLETE THE COMMAND,THE NORMAL WAIT ROUTINE WILL

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1803	011422	044312				•WORD 0DBUF	•CORE ADDRESS
1804	011424	177400				•WORD 177400	•WORDS PER SECTOR
1805	011426	000000				•WORD 0	•CYLINDER ADDRESS
1806	011430	000006				•WORD WRTCMD	•COMMAND
1807	011432	000000				•WORD 0	
1808						;	
1809						;	
1810						;	
1811	011434	000000			SCBLTP:	•WORD 0	•TEMP LOCS
1812	011436	000000				•WORD 0	
1813	011440	000000				•WORD 0	
1814	011442	000000				•WORD 0	
1815	011444	000000				•WORD 0	
1816						;	
1817						;	
1818						;	MESSAGE ADDRESSES FOR SCOPE COMMAND
1819						;	
1820						;	
1821						;	
1822	011446	011456			SCOADR:	•WORD COMMSG	•COMMAND TYPE MESSAGE
1823	011450	011510				•WORD DUMSG	•DUSH MESSAGE
1824	011452	011550				•WORD WSMMSG	•WORDS PER SECTOR MESSAGE
1825	011454	011612				•WORD CYMSG	•CYLINDER ADDRESS MESSAGE
1826						;	
1827						;	
1828	011456	103	117	115	COMMSG:	•ASCII /COMMAND TYPE (OCTAL) = 6 /	
	011461	115	101	116			
	011464	104	040	124			
	011467	131	120	105			
	011472	040	050	117			
	011475	103	124	101			
	011500	114	051	040			
	011503	075	040	066			
	011506	040					
1829	011507	000				•BYTE 0	
1830	011510	104	125	123	DUMSG:	•ASCII /DUSH ADDRESS (SECTOR,HEAD) = 0 /	
	011513	110	040	101			
	011516	104	104	122			
	011521	105	123	123			
	011524	040	050	123			
	011527	105	103	124			
	011532	117	122	054			
	011535	110	105	101			
	011540	104	051	040			
	011543	075	040	060			
	011546	040					
1831	011547	000				•BYTE 0	
1832	011550	127	117	122	WSMSG:	•ASCII /WORD COUNT (2'S COMPL.) = 177400 /	
	011553	104	040	103			
	011556	117	125	116			
	011561	124	040	050			
	011564	062	047	123			
	011567	040	103	117			
	011572	115	120	114			
	011575	056	051	040			
	011600	075	040	061			
	011603	067	067	064			

1833	011606	060	060	040			
1834	011611	000				•BYTE 0	
	011612	103	131	114	CYMSG:	•ASCII /CYLINDER ADDRESS = 0 /	
	011615	111	116	104			
	011620	105	122	040			
	011623	101	104	104			
	011626	122	105	123			
	011631	123	040	075			
	011634	040	060	040			
1835	011637	000				•BYTE 0	
1836						•EVEN	
1837						;	
1838						;	
1839						;	
1840						;	
1841						;	
1842						;	
1843						;	PASS COMMAND
1844						;	
1845						;	THE PASS COMMAND IS CALLED ONLY BY THE TEST
1846						;	EXECUTIVE. IT OUTPUTS THE PASS COUNTER AND RETURNS
1847						;	VIA A RTS PC. THE OUTPUT IS IN THE FORM:
1848						;	
1849						;	PASS COUNT = ###
1850						;	
1851						;	
1852	011640	004537	015474		PASS:	JSR	R5,SAVE
1853	011644	005037	005532			CLR	REQFLG
1854	011650	005037	005534			CLR	ECHOEM
1855	011654	005737	001224			TST	PASINH
1856	011660	001031				BNE	PSS1
1857	011662	005237	005522			INC	CIMODE
1858	011666	005237	005530			INC	NCR
1859	011672	012737	012006	005526		MOV	#PSMSG,MSGADR
1860	011700	004737	005134			JSR	PC,TTYOUT
1861	011704	005037	005530			CLR	NCR
1862	011710	013703	001236			MOV	PASCNT,R3
1863	011714	004737	006754			JSR	PC,ASCII
1864	011720	012737	010574	005526		MOV	#OUTBUF,MSGADR
1865	011726	004737	005134			JSR	PC,TTYOUT
1866	011732	012737	005740	005526		MOV	#LFCODE,MSGADR
1867	011740	004737	005134			JSR	PC,TTYOUT
1868						;	
1869	011744	005037	005522		PSS1:	CLR	CIMODE
1870	011750	004537	015510			JSR	R5,REST
1871	011754	005737	005524			TST	TSTACT
1872	011760	001002				BNE	PSS1
1873						;	SEE IF REPEAT IF YES
1874	011762	000137	004506		PSS2:	JMP	PMG1
1875						;	
1876						;	
1877	011766	005737	001220		PSS1:	TST	REPFLG
1878	011772	001402				BEQ	PSS3
1879	011774	000137	004000			JMP	TNINTA
1880						;	
1881	012000	005037	005524		PSS3:	CLR	TSTACT
1882	012004	000766				BR	PSS2

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1883      ;
1884      ;
1885      ;
1886      ;
1887      ;
1888      ;          PASS MESSAGE
1889      ;
1890      ;
1891 012006      PSMSG:
1892 012006      040      040      040      .ASCII /      PASS COUNT = /
      012011      040      120      101
      012014      123      123      040
      012017      103      117      125
      012022      116      124      040
      012025      075      040
1893 012027      000      .BYTE 0
1894      .EVEN
1895      ;
1896      ;
1897      ;
1898      ;
1899      ;          ERROR REPORTING ROUTINE
1900      ;
1901      ;
1902      ;          THIS ROUTINE PRINTS OUT THE TEST AND DRIVE
1903      ;          DATA NECESSARY TO DIAGNOSTIC PROBLEMS OCCURRING
1904      ;          WITH THE PHOENIX 211 OR THE ATTACHED DRIVE(S).
1905      ;
1906      ;
1907      ;          THE OUTPUT IS IN THE FOLLOWING FORM
1908      ;
1909      ;          FAILING DRIVE NUMBER = ##
1910      ;          FAILING TEST NUMBER  = ##
1911      ;          REFERENCE DATA      = ##
1912      ;          ACTUAL DATA         = ##
1913      ;          SUBTEST NUMBER      = ##
1914      ;
1915      ;
1916      ;          $$$ IF THE ERROR IS A DATA ERROR THE OUTPUT WILL
1917      ;          BE A MESSAGE SAYING "DATA ERROR"
1918      ;
1919      ;          IF ANY OTHER ERROR OCCURS THE CONTROLLER
1920      ;          REGISTER WILL BE OUTPUTED.
1921      ;
1922      ;
1923      ;
1924 012030 005737 001222      TTERR: TST      MOSTOP      ;SKIP PRINTOUT?
1925 012034 001402      bEQ      TER1          ;GO ON IF NO
1926 012036 000137 003516      JHP      INTST          ;REPEAT TEST SEQUENCE IF YES
1927      ;
1928      ;
1929 012042 005037 005524      TERT: CLR      TSTACT      ;RESET TEST ACTIVE
1930 012046 005737 001222      TST      ERPRIN      ;NO PRINTOUT?
1931 012052 001056      BNE      TER5          ;THEN EXIT
1932 012054 005237 005522      INC      CINHDE      ;SET COMMAND MODE HERE
1933 012060 004537 013104      JSR      R5,POUT      ;OUTPUT WHAT HAPPENED
1934 012064 012352      .WORD   ERM5C          ;ERROR MESSAGE ADDRESSES
    
```

						WORD	ERDATA	ERROR DATA WORDS
						WORD	5	MESSAGE COUNT
1935	012066	013220						
1936	012070	000005						
1937								
1938								
1939	012072	005737	001320	TER2:	TST	DATERR		DATA ERROR?
1940	012076	001427			BEO	TER4		PRINT CONTROLLER REGISTERS IF NO
1941								
1942								
1943	012100	012737	005740	005526	TER3:	MOV	#LFCODE,MSGADR	POINT TO LINE FEED
1944	012106	005037	005534		CLR	ECHOEM		REST ECHO
1945	012112	005037	005530		CLR	NCR		
1946	012116	004737	005134		JSR	PC,TTYOUT		PRINT IT
1947	012122	004737	005134		JSR	PC,TTYOUT		TWICE
1948								
1949	012126	012737	013034	005526	MOV	#DATMSG,MSGADR		NOW PRINT ERROR MESSAGE
1950								
1951	012134	004737	005134		JSR	PC,TTYOUT		PRINT MESSAGES
1952								
1953								
1954	012140	012737	005740	005526	MOV	#LFCODE,MSGADR		TWO MORE LF'S
1955	012146	004737	005134		JSR	PC,TTYOUT		PRINT
1956	012152	004737	005134		JSR	PC,TTYOUT		NOW
1957								
1958								
1959	012156	004537	013104	TER4:	JSR	R5,POUT		PRINT CONTROLLER REGISTERS
1960	012162	012560			WORD	DCCMSG		CONTROLLER MESSAGES(REGISTER)
1961	012164	013176			WORD	EBMSG		ERROR REGISTER SAVE BLOCK
1962	012166	000007			WORD	7		OUTPUT COUNT
1963								
1964	012170	005737	001074		TST	ECC		IS THIS AN ECC CONTROLLER?
1965	012174	001405			BEO	TERS		EXIT IF NO
1966								
1967	012176	004537	013104		JSR	R5,POUT		PRINT REGISTERS IF YES
1968	012202	012576			WORD	ECRMSG		ECC REGISTER MESSAGES
1969	012204	013214			WORD	ECCBB		SAVE LOCATIONS FOR REGISTERS
1970	012206	000002			WORD	2		PRINT COUNT
1971								
1972								
1973	012210	005737	001230	TER5:	TST	CONTST		CONTINUE TEST MODE?(TEST31,32)
1974	012214	001454			BEO	TER6		EXIT IF NOT
1975								
1976	012216	023727	001232	000031	CMP	CURTN,#31		TEST 31?
1977	012224	001404			BEO	TER7		SET UP FOR GO AHEAD IF YES
1978	012226	023727	001232	000032	CMP	CURTN,#32		TEST 32?
1979	012234	001044			BNE	TER6		EXIT IF NEITHER
1980								
1981	012236	017700	166536	TER7:	MOV	#DCSR,RO		FIND OUT WHAT COMMAND
1982	012242	042700	177770		BIC	#177770,RO		LOOSE GARBAGE
1983	012246	020027	000006		CMP	RO,#WKTCHD		WAS IT A WRITE?
1984	012252	001030			BNE	TER8		GO ON IF NO
1985								
1986	012254	012700	023602		MOV	#WRTBLK,RO		POINT TO WRITE BLOCK IF YES
1987								
1988	012260			TER9:				
1989	012260	062700	000004		ADD	#4,RO		ADJUST FOR BLOCK
1990	012264	004537	022436		JSR	R5,ENDPAR		COMPUTE AS IF NO ERROR
1991	012270	005737	001162		TST	ENDSEC		SECTOR =0



6		012502	125	101	114				
7		012505	040	040	040				
8		012510	040	040	040				
9		012513	104	101	124				
10		012516	101	040	040				
11		012521	040	040	040				
12		012524	075	040					
13	2028	012526	000				.BYTE 0		
14	2029	012527	123	125	102	SUBMSG:	.ASCII /SUBTEST NUMBER	= /	
15		012532	124	105	123				
16		012535	124	040	116				
17		012540	125	115	102				
18		012543	105	122	040				
19		012546	040	040	040				
20		012551	040	040	040				
21		012554	075	040					
22	2030	012556	000				.BYTE 0		
23	2031						.EVEN		
24	2032								
25	2033								
26	2034								
27	2035								
28	2036								
29	2037							CONTROLLER REGISTER PRINT OUT MESSAGES	
30	2038								
31	2039								
32	2040	012560	012602			DCCMSG:	.WORD DCRMSG		DCSR MESSAGE ADDRESS
33	2041	012562	012623				.WORD DUSMSG		DUSH MESSAGE ADDRESS
34	2042	012564	012644				.WORD DARMMSG		DCAR MESSAGE ADDRESS
35	2043	012566	012665				.WORD DWCMSG		DWCNT MESSAGE ADDRESS
36	2044	012570	012706				.WORD DCYMSG		DCYL MESSAGE ADDRESS
37	2045	012572	012727				.WORD DSKMSG		DSTAT MESSAGE ADDRESS
38	2046	012574	012750				.WORD DERMSG		DERR MESSAGE ADDRESS
39	2047						.EVEN		MAKE EVEN
40	2048								
41	2049	012576	012771			ECRMSG:	.WORD ECBMSG		ECCPB MESSAGE ADDRESS
42	2050	012600	013012				.WORD ECPMSG		ECCPW MESSAGE ADDRESS
43	2051								
44	2052								
45	2053	012602	040	040	040	DCRMSG:	.ASCII / DCSR	= /	
46		012605	040	040	104				
47		012610	103	123	122				
48		012613	040	040	040				
49		012616	075	040	040				
50		012621	040						
51	2054	012622	000				.BYTE 0		
52	2055	012623	040	040	040	DUSMSG:	.ASCII / DUSH	= /	
53		012626	040	040	104				
54		012631	125	123	110				
55		012634	040	040	040				
56		012637	075	040	040				
57		012642	040						
58	2056	012643	000				.BYTE 0		
59	2057	012644	040	040	040	DARMMSG:	.ASCII / DCAR	= /	
60		012647	040	040	104				
61		012652	103	101	122				
62		012655	040	040	040				



	012660	075	040	040		
	012663	040				
6	2058	012664	000		.BYTE 0	
1	2059	012665	040	040	DVCMMSG: .ASCII /	DVCNT = /
2		012670	040	040		104
3		012673	127	103		116
4		012676	124	040		040
5		012701	075	040		040
6		012704	040			
7	2060	012705	000		.BYTE 0	
8	2061	012706	040	040	DCYMSG: .ASCII /	DCYL = /
9		012711	040	040		104
10		012714	103	131		114
11		012717	040	040		040
12		012722	075	040		040
13		012725	040			
14	2062	012726	000		.BYTE 0	
15	2063	012727	040	040	DSKMSG: .ASCII /	DSTAT = /
16		012732	040	040		104
17		012735	123	124		101
18		012740	124	040		040
19		012743	075	040		040
20		012746	040			
21	2064	012747	000		.BYTE 0	
22	2065	012750	040	040	DERMSG: .ASCII /	DERR = /
23		012753	040	040		104
24		012756	105	122		122
25		012761	040	040		040
26		012764	075	040		040
27		012767	040			
28	2066	012770	000		.BYTE 0	
29	2067	012771	040	040	ECBMSG: .ASCII /	ECCPB = /
30		012774	040	040		105
31		012777	103	103		120
32		013002	102	040		040
33		013005	075	040		040
34		013010	040			
35	2068	013011	000		.BYTE 0	
36	2069	013012	040	040	ECPMSG: .ASCII /	ECCPW = /
37		013015	040	040		105
38		013020	103	103		120
39		013023	127	040		040
40		013026	075	040		040
41		013031	040			
42	2070	013032	000		.BYTE 0	
43	2071				.EVEN	
44	2072				;	
45	2073				;	
46	2074				;	
47	2075				.DATA ERROR MESSAGE	
48	2076				;	
49	2077				;	
50	2078	013034	040	040	DATMSG: .ASCII /	***** DATA ERROR *****/
51		013037	040	040		052
52		013042	052	052		052
53		013045	052	052		052
54		013050	052	052		052

1	013053	040	040	104				
2	013056	101	124	101				
3	013061	040	105	122				
4	013064	122	117	122				
5	013067	040	040	052				
6	013072	052	052	052				
7	013075	052	052	052				
8	013100	052	052					
9	013102	000						
10	2079				.BYTE 0			
11	2080							
12	2081							
13	2082							
14	2083							
15	2084							
16	2085							
17	2086							
18	2087							
19	2088							
20	2089				PRINT OUT ROUTINE			
21	2090							
22	2091				THIS SUBROUTINE PRINTS OUT AN ASCII LINE			
23	2092				FOLLOWED BY A SINGLE OCTAL WORD.			
24	2093				THE FORMAT OF THE OUTPUT IS THE FOLLOWING			
25	2094							
26	2095				ENDING TEST NUMBER = #####			
27	2096							
28	2097				THE SUBROUTINE CALL IS:			
29	2098				(X) JSR R5,POUT ;CALL HERE			
30	2099				(X)2 .WORD NNNN ;ADDRESS OF MESSAGES			
31	2100				(X)4 .WORD NNNN ;ADDRESS OF DATA WORDS			
32	2101				(X)6 .WORD # ;NUMBER OF MESSAGES			
33	2102							
34	2103							
35	2104							
36	2105				.EVEN			
37	2106	013104	000240		POUT: NOP			
38	2107	013106	011500		MOV (R5),R0 ;LOAD R0 WITH MESSAGE ADDRESS			
39	2108	013110	016501	000002	MOV 2(R5),R1 ;LOAD R1 WITH DATA ADDRESS			
40	2109	013114	016502	000004	MOV 4(R5),R2 ;LOAD R2 WITH MESSAGE COUNT			
41	2110							
42	2111	013120	005237	005530	PT1: INC NCR ;INHIBIT CARRIAGE RETURNS			
43	2112	013124	012037	005526	MOV (R0)+,MSGADR ;			
44	2113	013130	005037	005534	CLR ECHOEM ;ENSURE NO ECHOE MODE			
45	2114	013134	004737	005134	JSR PC,TTYOUT ;PRINT ASCII MESSAGE			
46	2115	013140	005037	005530	CLR NCR ;RESET CR RETURN MODE			
47	2116	013144	013103		MOV @ (R1)+,R3 ;GET READY FOR DATA WORD CONVERSION			
48	2117	013146	004737	006754	JSR PC,ASCII ;CONVERT TO ASCII			
49	2118	013152	012737	010574	005526	MOV #OUTBUF,MSGADR ;LOAD OUTPUT ADDRESS		
50	2119	013160	004737	005134	JSR PC,TTYOUT ;OUTPUT DATA WORD			
51	2120	013164	005302		DEC R2 ;DECREMENT MESSAGE COUNTER			
52	2121	013166	001354		BNE PT1 ;GO AGAIN IF MORE			
53	2122	013170	062705	000006	ADD #6,R5 ;UPDATE RETURN			
54	2123	013174	000205		RTS R5 ;AND RETURN NOW			
55	2124							
56	2125							
57	2126							
58	2127							

6	2128								
7	2129								
8	2130								
9	2131								MEMORY POINTERS FOR ERROR PRINTOUT
10	2132								
11	2133								1.CONTROLLER REGISTER IMAGES
12	2134								
13	2135								2.CPU REGISTERS AT ERROR DETECTION
14	2136								
15	2137								
16	2138	013176	035334	EBMSG:	WORD ERRBLK			DCSR ADDRESS	
17	2139	013200	035336		WORD ERRBLK+2			DUSH ADDRESS	
18	2140	013202	035340		WORD ERRBLK+4			DCAR ADDRESS	
19	2141	013204	035342		WORD ERRBLK+6			DWCNT ADDRESS	
20	2142	013206	035344		WORD ERRBLK+10			DCYL ADDRESS	
21	2143	013210	035346		WORD ERRBLK+12			DSTAT ADDRESS	
22	2144	013212	035350		WORD ERRBLK+14			DERR ADDRESS	
23	2145	013214	035352	ECCBB:	WORD ERRBLK+16			ECCPB ADDRESS	
24	2146	013216	035354		WORD ERRBLK+20			ECCPB ADDRESS	
25	2147								
26	2148								
27	2149								
28	2150	013220	002722	ERDATA:	WORD REGO			CPU R0	
29	2151	013222	002724		WORD REGO+2			CPU R1	
30	2152	013224	002726		WORD REGO+4			CPU R2	
31	2153	013226	002730		WORD REGO+6			CPU R3	
32	2154	013230	002732		WORD REGO+10			CPU R4	
33	2155	013232	002734		WORD REGO+12			CPU R5	
34	2156	013234	002736		WORD REGO+14			CPU R6(SP)	
35	2157	013236	002740		WORD REGO+16			CPU R7(PC)	
36	2158								
37	2159								
38	2160								
39	2161								
40	2162								
41	2163								
42	2164								FORMAT COMMAND
43	2165								
44	2166								THIS COMMAND WILL FORMAT ONE DISK UNIT
45	2167								THE COMMAND WILL ASK THE OPERATOR WHICH UNIT
46	2168								HE WISHES TO FORMAT ( 0 THRU 3).
47	2169								
48	2170								A SECOND QUERY WILL BE MADE IF A BAD CHOICE WAS
49	2171								ENTERED. THIS QUESTION WILL BE OF THE FORM:
50	2172								
51	2173								"ARE YOU SURE???? Y OR N
52	2174								
53	2175								
54	2176	013240	004537	015474	FHTDK:	JSR	R5,SAVE		SAVE CPU
55	2177	013244	005037	013450		CLR	DISKTP+2		CLEAR TEMP
56	2178								
57	2179	013250	005037	005532		CLR	REQFLG		RESET REQUEST FLAG
58	2180	013254	005237	005522		INC	CIMODE		SET COMMAND MODE
59	2181								
60	2182	013260	012702	013446	FHTK1:	MOV	DISKTP,R2		POINT TO TEMP DISK UNIT
61	2183	013264	012700	013452		MOV	DUNFT,R0		POINT TO MESSAGE OUT PUT
62	2184	013270	012701	000001		MOV	D1,R1		INCLUDE COUNT

2185	013274	005237	005540			INC	NUMBER		SET NUMBER FLAG
2186	013300	004737	007502			JSR	PC,LOADIN		FETCH DESIRED UNIT TO BE
2187									FORMATTED.
2188	013304	023727	013446	000003		CHP	DISKTP,#3		UNIT OK?
2189	013312	003410				BLE	FMTD1		GO ON IF YES
2190									
2191									
2192	013314	005037	005534			CLR	ECHOEM		RESET ECHO MODE
2193	013320	012737	007060	005526		MOV	#QUEST,MSGADR		POINT TO ? MARK
2194	013326	004737	005134			JSR	PC,TTYOUT		PRINT ?
2195	013332	000752				BR	FMTK1		TRY THIS AGAIN
2196									
2197									
2198	013334	013737	013446	001214	FMTD1:	MOV	DISKTP,STPDSK		LOAD SELECTED UNIT
2199	013342	013737	013446	001216		MOV	DISKTP,STRDSK		
2200									
2201	013350	005037	005540			CLR	NUMBER		ASK IF SURE
2202	013354	012701	000001			MOV	#1,R1		COUNT =1
2203	013360	004737	007502			JSR	PC,LOADIN		FETCH ANSWER
2204	013364	005737	013450			TST	DISKTP+2		OK
2205	013370	001006				BNE	FMTD2		GO ON IF YES
2206	013372	005037	005534			CLR	ECHOEM		RESET ECHO MODE
2207	013376	005037	005522			CLR	CIMODE		RESET COMMANDMODE
2208	013402	000137	004506			JMP	PMG1		GO BACK TO PMGR IF NO
2209									
2210	013406	012737	000045	001212	FMTD2:	MOV	#45,STRTN		LOAD TEST P'S FROM HERE
2211	013414	012737	000045	001210		MOV	#45,STPTN		
2212	013422	005037	001220			CLR	REPFLG		
2213	013426	005037	001222			CLR	NOSTOP		
2214	013432	005037	005522			CLR	CIMODE		RESET COMMAND MODE
2215	013436	005237	005524			INC	TSTACT		SET TEST ACTIVE
2216									
2217									
2218	013442	000137	003044			JMP	TSTART		START OFF NOW
2219									
2220									
2221	013446	000000				DISKTP:	WORD 0		TEMP
2222	013450	000000					WORD 0		
2223	013452	013456				DUNFT:	WORD DFMSG		FORMAT MESSAGE UNIT
2224	013454	013525					WORD ASRMSG		ARE YOU SURE MESSAGE
2225									
2226									
2227	013456	040	040	040	DFMSG:	ASCII /	DISK UNIT TO BE FORMATTED	= 0 /	
	013461	040	040	104					
	013464	111	123	113					
	013467	040	125	116					
	013472	111	124	040					
	013475	124	117	040					
	013500	102	105	040					
	013503	106	117	122					
	013506	115	101	124					
	013511	124	105	104					
	013514	040	040	040					
	013517	075	040	060					
	013522	040	040						
2228	013524	000				BYTE 0			
2229	013525	040	040	040	ASRMSG:	ASCII /	ARE YOU SURE???	Y OR N /	

013530	040	040	101				
013533	122	105	040				
013536	131	117	125				
013541	040	123	125				
013544	122	105	077				
013547	077	077	040				
013552	131	040	117				
013555	122	040	116				
013560	040	040	040				
2230	013563	000			.BYTE 0		
2231					;		
2232					;		
2233					;		
2234					;		
2235					;		
2236					REGISTER READ COMMAND		
2237					;		
2238					THIS COMMAND REDS AND OUPUTS THE PHOENIX 211 REGISTERS		
2239					;		
2240	013564	004537	015474	RGREAD:	JSR R5,SAVE		;SAVE CPU
2241	013570	005037	005532		CLR REOFLG		;RESET REQUEST FLAG
2242	013574	005037	005534		CLR ECHOEM		;RESET ECHO MODE
2243	013600	005237	005522		INC CIMODE		;SET COMMAND MODE
2244					;		
2245					;		
2246	013604	004537	013104		JSR R5,POUT		;PRINT REGISTERS
2247	013610	012560			.WORD DCCMSG		;REGISTER HEADINGS
2248	013612	001000			.WORD DCSR		;REGISTE ADDRESSES
2249	013614	000007			.WORD 7		;COUNT FOR OUPUT
2250					;		
2251	013616	005737	001074		TST ECC		;IS THIS AN ECC CONTROLLER?
2252	013622	001405			BEQ R6R		;EXIT NOW IF NOT
2253					;		
2254	013624	004537	013104		JSR R5,POUT		;DUPUT ECC REGS IF YES
2255	013630	012576			.WORD ECRM5G		;ECC REGISTER HEADING
2256	013632	001016			.WORD ECCPB		;ADDRESS OF REAL REGISTER
2257	013634	000002			.WORD 2		;COUNT FOR REG'S
2258					;		
2259	013636	005037	005522	R6R:	CLR CIMODE		;RESET COMMAND MODE
2260	013642	004537	015510		JSR R5,REST		;BRING BACK CPU
2261					;		
2262					;		
2263	013646	000137	004506		JMP PMGT		;PROMPT
2264					;		
2265					;		
2266					;		
2267					HELP COMMAND		
2268					;		
2269					THIS COMMAND IS A BRIEF DESCRIPTION OF THE		
2270					PHOENIX 211 DIAGNOSTIC MONITOR TO AID THE		
2271					OPERATOR DURING TESTING		
2272	013652	004537	015474	HELP:	JSR R5,SAVE		;SAVE CPU
2273	013656	005237	005522		INC CIMODE		;SET COMMAND MODE
2274	013662	005037	005532		CLR REOFLG		;RESET REQUEST FLAG
2275	013666	005037	005534		CLR ECHOEM		;RESET ECHO MODE
2276					;		
2277	013672	012737	014046	005526	MOV #HLPMSG,MSGADR		;POINT TO MESSAGE ADDRESSES

2278	013700	004737	005134		JSR	PC,TTYOUT		;PRINT IT
2279	013704	012737	005740	005526	MOV	#LF,MSGADR		;ISSUE LINE FEED
2280	013712	004737	005134		JSR	PC,TTYOUT		;
2281								
2282	013716	012702	000004		MOV	#4,R2		;PRINT FIRST INSTRUCTIONS
2283	013722	012703	014004		MOV	#HPMSG,R3		;R3=MESSAGE ADDRESS POINTER
2284	013726	012337	005526	HLP1:	MOV	(R3)+,MSGADR		;LOAD MESSAGE ADDRESS
2285	013732	004737	005134		JSR	PC,TTYOUT		;PRINT IT
2286	013736	005302			DEC	R2		;SEE IF DONE
2287	013740	001372			BNE	HLP1		;GO ON IF NO
2288								;
2289								;
2290	013742	012737	005740	005526	HLP2:	MOV	#LF,MSGADR	;ANOTHER LINE FEED HERE
2291	013750	004737	005134		JSR	PC,TTYOUT		;
2292								;
2293	013754	012702	000015		MOV	#13,R2		;COUNT =13
2294	013760	012337	005526	HLP3:	MOV	(R3)+,MSGADR		;LOAD UP AN ADDRESS
2295	013764	004737	005134		JSR	PC,TTYOUT		;PRINT IT
2296	013770	005302			DEC	R2		;DEC COUNTER
2297	013772	001372			BNE	HLP3		;AND CONTINUE UNTIL DONE
2298	013774	005037	005522		CLR	CIMODE		;RESET COMMAND MODE
2299	014000	000137	004506		JMP	PMG1		;AND PROMPT
2300								;
2301								;
2302	014004	014131		HPMSG:	.WORD	MSG1		;LIST OF MESSAGE FOR HELP COMMAND
2303	014006	014210			.WORD	MSG2		;
2304	014010	014271			.WORD	MSG3		;
2305	014012	014347			.WORD	MSG4		;
2306	014014	014436			.WORD	MSG5		;
2307	014016	014513			.WORD	MSG6		;
2308	014020	014574			.WORD	MSG7		;
2309	014022	014634			.WORD	MSG8		;
2310	014024	014705			.WORD	MSG9		;
2311	014026	014754			.WORD	MSG10		;
2312	014030	015021			.WORD	MSG11		;
2313	014032	015046			.WORD	MSG12		;
2314	014034	015101			.WORD	MSG13		;
2315	014036	015152			.WORD	MSG14		;
2316	014040	015177			.WORD	MSG15		;
2317	014042	015245			.WORD	MSG16		;
2318	014044	015301			.WORD	MSG17		;
2319								;
2320	014046	040	040	040	HLPMSG:	.ASCII /	PHOENIX 211 DIAGNOSTIC MONITOR INSTRUCTIONS/	
	014051	040	040	040				
	014054	040	120	110				
	014057	117	105	116				
	014062	111	130	040				
	014065	062	061	061				
	014070	040	104	111				
	014073	101	107	116				
	014076	117	123	124				
	014101	111	103	040				
	014104	115	117	116				
	014107	111	124	117				
	014112	122	040	111				
	014115	116	123	124				
	014120	122	125	103				

	014123	124	111	117		
	014126	116	123			
2321	014130	000				.BYTE 0
2322						
2323	014131	040	040	040	MSG1:	.ASCII / 1. TYPE A CONTROL C TO ABORT THIS PRINTOUT/
	014134	040	061	056		
	014137	040	124	131		
	014142	120	105	040		
	014145	101	040	103		
	014150	117	116	124		
	014153	122	117	114		
	014156	040	103	040		
	014161	124	117	040		
	014164	101	102	117		
	014167	122	124	040		
	014172	124	110	111		
	014175	123	040	120		
	014200	122	111	116		
	014203	124	117	125		
	014206	124				
2324	014207	000				.BYTE 0
2325	014210	040	040	040	MSG2:	.ASCII / 2. DEFAULT ANSWER FOR YES-NO QUESTIONS IS NO/
	014213	040	062	056		
	014216	040	104	105		
	014221	106	101	125		
	014224	114	124	040		
	014227	101	116	123		
	014232	127	105	122		
	014235	040	106	117		
	014240	122	040	131		
	014243	105	123	055		
	014246	116	117	040		
	014251	121	125	105		
	014254	123	124	111		
	014257	117	116	123		
	014262	040	111	123		
	014265	040	116	117		
2326	014270	000				.BYTE 0
2327	014271	040	040	040	MSG3:	.ASCII / 3. ALL NUMERICAL ANSWERS MUST BE IN OCTAL/
	014274	040	063	056		
	014277	040	101	114		
	014302	114	040	116		
	014305	125	115	105		
	014310	122	111	103		
	014313	101	114	040		
	014316	101	116	123		
	014321	127	105	122		
	014324	123	040	115		
	014327	125	123	124		
	014332	040	102	105		
	014335	040	111	116		
	014340	040	117	103		
	014343	124	101	114		
2328	014346	000				.BYTE 0
2329	014347	040	040	040	MSG4:	.ASCII / 4. TYPING A CONTROL C DURING TESTING CALLS MONITOR/
	014352	040	064	056		
	014355	040	124	131		

	014360	120	111	116		
	014363	107	040	101		
	014366	040	103	117		
1	014371	116	124	122		
2	014374	117	114	040		
3	014377	103	040	104		
4	014402	125	122	111		
5	014405	116	107	040		
6	014410	124	105	123		
7	014413	124	111	116		
8	014416	107	040	103		
9	014421	101	114	114		
10	014424	123	040	115		
11	014427	117	116	111		
12	014432	124	117	122		
13	2330 014435	000			.BYTE 0	
14	2331 014436	040	040	040	MSG5: .ASCII /	5. THE FOLLOWING ARE THE LEGAL COMMANDS:/
15	014441	040	065	056		
16	014444	040	124	110		
17	014447	105	040	106		
18	014452	117	114	114		
19	014455	117	127	111		
20	014460	116	107	040		
21	014463	101	122	105		
22	014466	040	124	110		
23	014471	105	040	114		
24	014474	105	107	101		
25	014477	114	040	103		
26	014502	117	115	115		
27	014505	101	116	104		
28	014510	123	072			
29	2332 014512	000			.BYTE 0	
30	2333 014513	040	040	040	MSG6: .ASCII /	A. G J60 COMMAND -STARTS TEST SEQUENCE/
31	014516	040	040	040		
32	014521	040	101	056		
33	014524	040	107	040		
34	014527	040	040	040		
35	014532	073	107	117		
36	014535	040	103	117		
37	014540	115	115	101		
38	014543	116	104	040		
39	014546	055	123	124		
40	014551	101	122	124		
41	014554	123	040	124		
42	014557	105	123	124		
43	014562	040	123	105		
44	014565	121	125	105		
45	014570	116	103	105		
46	2334 014573	000			.BYTE 0	
47	2335 014574	040	040	040	MSG7: .ASCII /	B. DK JDISK PARAMETERS/
48	014577	040	040	040		
49	014602	040	102	056		
50	014605	040	104	113		
51	014610	040	040	040		
52	014613	073	104	111		
53	014616	123	113	040		
54	014621	120	101	122		



	014624	101	115	105			
	014627	124	105	122			
	014632	123					
1	2336 014633	000				•BYTE 0	
2	2337 014634	040	040	040	MSG8:	•ASCII /	C. TS ;TEST SEQUENCE PARAMETERS/
3	014637	040	040	040			
4	014642	040	103	056			
5	014645	040	124	123			
6	014650	040	040	040			
7	014653	073	124	105			
8	014656	123	124	040			
9	014661	123	105	121			
10	014664	125	105	116			
11	014667	103	105	040			
12	014672	120	101	122			
13	014675	101	115	105			
14	014700	124	105	122			
15	014703	123					
16	2338 014704	000				•BYTE 0	
17	2339 014705	040	040	040	MSG9:	•ASCII /	D. FT ;CONTROLLER PARAMETERS./
18	014710	040	040	040			
19	014713	040	104	056			
20	014716	040	106	124			
21	014721	040	040	040			
22	014724	073	103	117			
23	014727	116	124	122			
24	014732	117	114	114			
25	014735	105	122	040			
26	014740	120	101	122			
27	014743	101	115	105			
28	014746	124	105	122			
29	014751	123	056				
30	2340 014753	000				•BYTE 0	
31	2341 014754	040	040	040	MSG10:	•ASCII /	E. PR ;TEST PROGRESS REPORT/
32	014757	040	040	040			
33	014762	040	105	056			
34	014765	040	120	122			
35	014770	040	040	040			
36	014773	073	124	105			
37	014776	123	124	040			
38	015001	120	122	117			
39	015004	107	122	105			
40	015007	123	123	040			
41	015012	122	105	120			
42	015015	117	122	124			
43	2342 015020	000				•BYTE 0	
44	2343 015021	040	040	040	MSG11:	•ASCII /	F. DA ;DATE/
45	015024	040	040	040			
46	015027	040	106	056			
47	015032	040	104	101			
48	015035	040	040	040			
49	015040	073	104	101			
50	015043	124	105				
51	2344 015045	000				•BYTE 0	
52	2345 015046	040	040	040	MSG12:	•ASCII /	G. SC ;SCOPE LOOP/
53	015051	040	040	040			
54	015054	040	107	056			

1		015057	040	123	103				
2		015062	040	040	040				
3		015065	073	123	103				
4		015070	117	120	105				
5		015073	040	114	117				
6		015076	117	120					
7	2346	015100	000						
8	2347	015101	040	040	040	MSG13:	•BYTE 0	H. RR	•CONTROLLER REGISTER READ/
9		015104	040	040	040		•ASCII /		
10		015107	040	110	056				
11		015112	040	122	122				
12		015115	040	040	040				
13		015120	073	103	117				
14		015123	116	124	122				
15		015126	117	114	114				
16		015131	105	122	040				
17		015134	122	105	107				
18		015137	111	123	124				
19		015142	105	122	040				
20		015145	122	105	101				
21		015150	104						
22	2348	015151	000				•BYTE 0		
23	2349	015152	040	040	040	MSG14:	•ASCII /	I. H	•HELP/
24		015155	040	040	040				
25		015160	040	111	056				
26		015163	040	110	040				
27		015166	040	040	040				
28		015171	073	110	105				
29		015174	114	120					
30	2350	015176	000				•BYTE 0		
31	2351	015177	040	040	040	MSG15:	•ASCII /	J. TE	•TEST ERROR CONDITIONS/
32		015202	040	040	040				
33		015205	040	112	056				
34		015210	040	124	105				
35		015213	040	040	040				
36		015216	073	124	105				
37		015221	123	124	040				
38		015224	105	122	122				
39		015227	117	122	040				
40		015232	103	117	116				
41		015235	104	111	124				
42		015240	111	117	116				
43		015243	123						
44	2352	015244	000				•BYTE 0		
45	2353	015245	040	040	040	MSG16:	•ASCII /	K. FO	•FORMAT DISK/
46		015250	040	040	040				
47		015253	040	113	056				
48		015256	040	106	117				
49		015261	040	040	040				
50		015264	073	106	117				
51		015267	122	115	101				
52		015272	124	040	104				
53		015275	111	123	113				
54	2354	015300	000				•BYTE 0		
55	2355	015301	040	040	040	MSG17:	•ASCII /	L. CO	•CONTINUE TESTING/
56		015304	040	040	040				
57		015307	040	114	056				

1	015312	040	103	117				
2	015315	040	040	040				
3	015320	073	103	117				
4	015323	116	124	111				
5	015326	116	125	105				
6	015331	040	124	105				
7	015334	123	124	111				
8	015337	116	107					
9	2356	015341	000			.BYTE 0		
10	2357					.EVEN		
11	2358							
12	2359							
13	2360							
14	2361							
15	2362							
16	2363					CONTINUE COMMAND		
17	2364							
18	2365					THIS COMMAND IS USED AFTER TESTING HAS BEEN HALTED		
19	2366					AND THE MONITOR HAS BEEN ACTIVATED.		
20	2367					WITH THIS COMMAND TESTING CAN BE STARTED FROM		
21	2368					THE LAST TEST THAT WAS BEING EXECUTED THEREBY		
22	2369					NOT LOSING PREVIOUS PASS COUNTS AND OR PREVIOUS PASSED		
23	2370					TESTS.		
24	2371							
25	2372	015342	012700	005750	CONTU:	MOV	#TSTINT,RO	START FILLING CPU AGAIN
26	2373	015346	005037	005522		CLR	CIMODE	RESET COMMAND MODE
27	2374	015352	005037	001150		CLR	INTFLG	RESER INTERRUPT FLAGS
28	2375	015356	005037	005720		CLR	TTYINT	
29	2376	015362	005237	005524		INC	TSTACT	SET TEST MODE BIT
30	2377	015366	005720			TST	(RO)+	LOOK AT R1 IMAGE
31	2378	015370	012001			MOV	(RO)+,R1	FILL CPU
32	2379	015372	012002			MOV	(RO)+,R2	
33	2380	015374	012003			MOV	(RO)+,R3	
34	2381	015376	012004			MOV	(RO)+,R4	
35	2382	015400	012005			MOV	(RO)+,R5	
36	2383	015402	005046			CLR	-(SP)	ENTER BACK NOW
37	2384	015404	011046			MOV	(RO),-(SP)	LOAD OLD ADDRESS
38	2385	015406	013700	005750		MOV	TSTINT,RO	RESTORE RO LAST
39	2386							
40	2387							
41	2388	015412	000002			RTI		AND EXIT
42	2389							
43	2390							
44	2391							
45	2392							
46	2393	015414	005737	001104	TTYSET:	TST	TTYPUT	KEYBOARD HRER?
47	2394	015420	001406			BEO	TTYSEX	EXIT IF NO
48	2395	015422	012777	000100	170272	MOV	#INTON,#ATKS	ENABLE READER
49	2396	015430	012777	000100	170270	MOV	#INTON,#TPS	ENABLE PRINTER
50	2397	015436	000207			TTYSEX:	RTS	PC
51	2398							
52	2399							
53	2400							
54	2401							
55	2402							
56	2403							
57	2404							

CONTROLLER REGISTER SAVE ROUTINE



```

2462      ;
2463      ;
2464      ; THIS ROUTINE FORMATS THE OUTPUT BUFFER
2465      ; WITH THE RANDOM NUMBER "RAMBLER"
2466      ;
2467 015524 004537 015474      RANBUF: JSR    R5,SAVE      ;SAVE REGISTERS
2468 015530 004537 015564      JSR    R5,RANDOM    ;GENERATE RANDOM NUMBER
2469 015534 013700 001252      MOV    RAMBLER,R0   ;FETCH RANDOM NUMBER
2470 015540 012701 044312      MOV    #0DBUF,R1   ;POINT TO OUTPUT BUFFER
2471 015544 012702 047314      MOV    #IDBUF1,R2  ;POINT R2 TO END OF BUFFER
2472 015550 010021      RANB: MOV    R0,(R1)+ ;ENTER DATA
2473 015552 020102      CHP    R1,R2       ;DONE?
2474 015554 001375      BNE    RANB        ;CONTINUE IF NO
2475 015556 004537 015510      JSR    R5,REST     ;RELOAD REGISTERS
2476 015562 000205      RTS    R5          ;AND EXIT
2477      ;
2478      ;
2479      ;
2480      ;
2481      ;
2482      ;
2483      ;
2484      ;
2485      ;
2486      ;
2487      ;
2488      ;
2489      ;
2490      ;
2491      ;
2492      ;
2493      ;
2494      ;
2495 015564 004537 015474      RANDOM: JSR    R5,SAVE      ;SAVE RO>>>>R4
2496 015570 013704 001252      MOV    RAMBLER,R4  ;FETCH OLD RANDOM
2497 015574 010403      MOV    R4,R3       ;LOAD INTO R3
2498 015576 005001      CLR    R1          ;CLEAR R1
2499 015600 012702 000020      MOV    #20,R2     ;SET UP SHIFT LOOP
2500 015604 043704 001256      BIC    POLY,R4    ;CLEAR XOR BITS
2501 015610 000401      BR     $RN2       ;START RANDOMMING????????
2502 015612 006304      $RN1: ASL    R4    ;SHIFT R4
2503 015614 100001      $RN2: BPL    $RN3 ;MSB NOT SET
2504 015616 005101      COM    R1
2505 015620 005302      $RN3: DEC    R2   ;LAST BITS?
2506 015622 100373      BPL    $RN1      ;CONTINUE IF NO
2507 015624 006303      ASL    R3       ;SHIFT OLD NUMBER
2508 015626 005401      NEG    R1       ;CLEARX XOR
2509 015630 050103      BIS    R1,R3    ;UPDATE LSB OF OLD NUMBER
2510 015632 010337 001252      MOV    R3,RAMBLER ;UPDATE RANDOM NUMBER
2511 015636 004537 015510      JSR    R5,REST     ;RESTORE REGISTERS
2512 015642 000205      RTS    R5        ;GO BACK
2513      ;
2514      ;
2515      ;
2516      ;
2517      ;
2518      ;

```

RANDOM NUMBER GENERATOR  
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THIS ROUTINE WILL GENERATE A 16 BIT  
 RANDOM NUMBER FOR USE AS DATA AND DISK ADDRESS





2633	016154	004537	015564		JSR	R5,RANDOM	;	GET NEW NUMBER
2634	016160	013702	001252		MOV	RAMBLER,R2	;	ENTER INTO R2
2635	016164	000766			BR	RAN5	;	CHECK AGAIN
2636	016166	010210		RAN1:	MOV	R2,(R0)	;	LOAD INTO COMMAND BLOCK
2637	016170	010102			MOV	R1,R2	;	RELOAD RANDOM NUMBER
2638	016172	042702	170177	RAN2:	BIC	#HDMSK,R2	;	EXTRACT SECTOR FIELD
2639	016176	020237	001042		CMP	R2,MAXHD	;	TOO BIG?
2640	016202	003405			BLE	RAN3	;	CONTINUE IF NO
2641	016204	004537	015564		JSR	R5,RANDOM	;	GET NEW NUMBER
2642	016210	013702	001252		MOV	RAMBLER,R2	;	LOAD INTO R2
2643	016214	000766			BR	RAN2	;	CHECK AGAIN
2644	016216	010210		RAN3:	BIS	R2,(R0)	;	AND LOAD INTO COMMAND BLOCK
2645	016220	010102			MOV	R1,R2	;	RELOAD RANDOM NUMBER
2646	016222	042702	176000	RAN8:	BIC	#CYLMSK,R2	;	EXTRACT CYLINDER FIALD
2647	016226	020237	001044		CMP	R2,MAXCYL	;	TOO BIG?
2648	016232	003405			BLE	RAN4	;	CONTINUE IF NO
2649	016234	004537	015564		JSR	R5,RANDOM	;	GET NEW NUMBER
2650	016240	013702	001252		MOV	RAMBLER,R2	;	LOAD INTO R2
2651	016244	000766			BR	RAN8	;	TRY AGAIN
2652	016246	010260	000006	RAN4:	MOV	R2,6(R0)	;	LOAD INTO COMMAND BLOCK
2653	016252	010102			MOV	R1,R2	;	RELOAD RANDOM NUMBER
2654	016254	053702	001270		BIS	MAXTFR,R2	;	MAKE SMALL ENOUGH WORD COUNT
2655	016260	010260	000004		MOV	R2,4(R0)	;	LOAD INTO COMMAND BLOCK
2656	016264	010102			MOV	R1,R2	;	RESTORE RANDOM NUMBER
2657	016266	005737	001106		TST	MORIVE	;	TESTING MULTIPLE DRIVES?
2658	016272	001414			BEQ	RAN10	;	EXIT IF NO
2659	016274	042702	147777	RAN6:	BIC	#UNIMSK,R2	;	EXTRACT UNITS
2660	016300	020237	001214		CMP	R2,STPDSK	;	SEE IF OVER
2661	016304	003405			BLE	RAN7	;	CONTINUE IF NO
2662	016306	004537	015564		JSR	R5,RANDOM	;	GET NEW NUMBER
2663	016312	013702	001252		MOV	RAMBLER,R2	;	LOAD INTO R2
2664	016316	000766			BR	RAN6	;	
2665	016320	010237	001234	RAN7:	MOV	R2,CURDSK	;	FORCE RANDOM DISK ADDRESS
2666	016324	004537	015510	RAN10:	JSR	R5,REST	;	RESTORE REGISTERS
2667	016330	000205			RTS	R5	;	GO BACK
2668					;			
2669					;			
2670					;			
2671					;			
2672					;			
2673					;			
2674					;			
2675					;			
2676					;			
2677					;			
2678	016332	013702	001234	DISKID:	MOV	CURDSK,R2	;	FETCH CURRENT UNIT NUMBER
2679	016336	000302			SWAB	R2	;	MAKE VALID DISK SELECTION BITS
2680	016340	006302			ASL	R2		
2681	016342	006302			ASL	R2		
2682	016344	006302			ASL	R2		
2683	016346	006302			ASL	R2		
2684	016350	000205			RTS	R5	;	AND RETURN TO CALLING PROGRAM
2685					;			
2686					;			
2687					;			
2688					;			
2689					;			

DISK INITIALIZATION ROUTINE

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2691  
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1	2693	016352	013746	001234	DKINIT:	MOV	CURDSK,-(SP)	SAVE CURRENT DISK ID	
2	2694	016356	004537	004066		JSR	R5,SEKTIM	SET UP LOOP FOR SEEK TIME OUT	
3	2695	016362	004537	004276		JSR	R5,ROUEST	SELCT FORMATTER	
4	2696	016366	005002			CLR	R2	USE R2 FOR WORK	
5	2697	016370	004537	016332	DKI1:	JSR	R5,DISKID	FORMAT DISK SLECT BITS	
6	2698	016374	010277	162402		MOV	R2,@DUSH	SELECT DISK	
7	2699	016400	000240			NOP		WAIT FOR DISK READY	
8	2700	016402	000240			NOP			
9	2701	016404	000240			NOP			
10	2702	016406	052777	000022	162364	BIS	#FLTCLR,@DCSR	LOAD FAULT CLEAR COMMAND	
11	2703	016414	005277	162360		INC	@DCSR	SET GO BIT	
12	2704	016420	000240			NOP			
13	2705	016422	012703	000020		MOV	#R2,R3	SET UP WAIT LOOP	
14	2706	016426	105777	162346	DKI3:	TSTB	@DCSR	WAIT FOR DONE	
15	2707	016432	100402			BMI	DKI4	CONTINUE IF DONE	
16	2708	016434	005303			DEC	R3	DECREMENT PROTECT LOOP	
17	2709	016436	001373			BNE	DKI3	CONTINUE IF REASONABLE TIME	
18	2710	016440	042777	000136	162332	DKI4:	BIC	#FUNC,@DCSR	LOSE FUCNTION BITS
19	2711	016446	052777	000024	162324	BIS	#RTZCMD,@DCSR	ENTER RECALIBRATE COMMAND	
20	2712	016454	005277	162320		INC	@DCSR	SET GO	
21	2713	016460	004537	022164		JSR	R5,WAIT1	WAIT DONE	
22	2714	016464	052777	000077	162306	BIS	#NOPCMD,@DCSR	ISSUE NOP FOR SEEK DONE	
23	2715	016472	020227	030000		CMP	R2,#UNIFLD	ALL DONE WITH DISKS?	
24	2716	016476	001403			BEQ	DKI2	CONTINUE IF NO	
25	2717	016500	00237	001234		INC	CURDSK	LOOK AT ANOTHER DISK	
26	2718	016504	000731			BR	DKI1	AND DO ANOTHER DISK	
27	2719	016506	042777	000136	162264	DKI2:	BIC	#FUNC,@DCSR	LOSE FUNCTION BITS
28	2720	016514	012777	000041	162256	MOV	#SYSCLR BIT5,@DCSR	CLEAR ERRORS(DRIVE NOT READY)	
29	2721	016522	012637	001234		MOV	(SP)+,CURDSK	RESTORE CURRENT DISK FLAG	
30	2722	016526	000205			RTS	R5	AND RETURN TO CALLING PROGRAM	
31	2723								
32	2724								
33	2725								
34	2726								
35	2727								
36	2728								
37	2729								
38	2730							INITIALIZATION TEST	
39	2731							-----	
40	2732								
41	2733							THIS TEST VERIFIES THAT INIT CLEARS ALL THE	
42	2734							DISK CONTROLLER REGISTERS	
43	2735								
44	2736	016530	004537	004276	TNO:	JSR	R5,ROUEST	REQUEST FORMATTER	
45	2737	016534	000005			RESET		INITIALIZE ALL HARDWARE	
46	2738	016536	012702	000200		MOV	#FMTRDY,R2	ESTABLISH REFERENCE	
47	2739	016542	004537	004276		JSR	R5,ROUEST	GET FORMATTER AGAIN	
48	2740	016546	005004			CLR	R4	INITIALIZE SUBTEST NUMBER	
49	2741	016550	017703	162224		MOV	@DCSR,R3	WAS CONTROL AND STATUS INITIALIZED?	
50	2742	016554	043703	001102		BIC	#CPU,R3	LOSE REQUEST BIT IF SET	
51	2743	016560	042703	000100		BIC	#INTON,R3	LOSE INTERRUPT REQUEST BIT	
52	2744	016564	020203			CMP	R2,R3	COMPARE THE DCSR IS IT RIGHT	
53	2745	016566	001411			BEQ	TNOA	IF RIGHT CONTINUE	
54	2746	016570	005777	162216		TST	@DSTAT	TEST FORD DRIVE READY	

2747	016574	100454		BMI	TNOERR	);EXIT WITH ERROR IF DRIVE READY
2748	016576	012702	000200	MOV	#FHTRDY,R2	);SET UP NEW REFERENCE WORD
2749	016602	052702	100000	BIS	#BIT15,R2	);ADD ERROR SUMMARY
2750	016606	020203		CMF	R2,R3	);CMPARE AGAIN
2751	016610	001046		BNE	TNOERR	);EXIT WITH ERROR IF REGISRES NOT EQUAL
2752	016612	005204		INC	R4	);SUBTEST NUMBER=1
2753	016614	017703	162164	MOV	@DCAR,R3	);WAS CORE ADDRESS INITIALIZED?
2754	016620	005002		CLR	R2	);SET UP REFERENCE WORD
2755	016622	020203		CMF	R2,R3	);INITIALIZED?
2756	016624	001040		BNE	TNOERR	);EXIT WITH ERROR IF NOT
2757	016626	005204		INC	R4	);SUBTEST NO.=2
2758	016630	017703	162152	MOV	@DWCNT,R3	);WAS WORD COUNT INITIA;IZED?
2759	016634	020203		CMF	R2,R3	);COMPARE
2760	016636	001033		BNE	TNOERR	);EXIT WITH ERROR IF NOT
2761	016640	005204		INC	R4	);SUBTEST NO.=3
2762	016642	017703	162142	MOV	@DCYL,R3	);WAS CYLINDER ADDRESS INITIALIZED?
2763	016646	020203		CMF	R2,R3	);COMPARE
2764	016650	001026		BNE	TNOERR	);EXIT WITH ERROR IF NOT
2765	016652	005204		INC	R4	);SUBTEST NO.=4
2766	016654	017703	162132	MOV	@DSTAT,R3	);FETCH DISK REGISTER
2767	016660	042703	100000	BIC	#BIT15,R3	);LOSE DRIVE READY IF PRESENT
2768	016664	042703	020000	BIC	#BIT13,R3	);AND WRITE PROTECT IF PRESENT
2769	016670	005002		CLR	R2	);SET UP REFERENCE WORD
2770	016672	020203		CMF	R2,R3	);IS THE DATA RIGHT?
2771	016674	001014		BNE	TNOERR	);EXIT IF NOT THE SAME
2772	016676	005204		INC	R4	);SUBTEST NUMBER=5(DISK STATUS OK)
2773	016700	017703	162110	MOV	@DERR,R3	);WAS DISK ERROR INITIALIZED?
2774	016704	005002		CLR	R2	);SET UP REFERENCE
2775	016706	020203		CMF	R2,R3	);RESET?
2776	016710	001006		BNE	TNOERR	);EXIT IF NO
2777	016712	005204		INC	R4	);SUBTEST NUMBER=6
2778	016714	017703	162062	MOV	@DUSH,R3	);WAS UNTI,HEAD SECTOR INIT.?
2779	016720	005002		CLR	R2	);SET UP REFERENCE WORD
2780	016722	020203		CMF	R2,R3	);RESET?
2781	016724	001402		BEQ	TNOOUT	);EXIT IF YES
2782	016726	005237	001322	TNOERR: INC	ERRFLG	);SET ERROR FLAG
2783	016732	004537	003342	TNOOUT: JSR	R5,YSTCTL	);GO TO NEXT TESAT
2784						
2785						
2786				.EOT		);END OF TAPE

\*\*\*\*\* SECTION 1 \*\*\*\*\*

OPERATING INSTRUCTIONS

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\*\*\*\*\*

NOTE: THIS DIAGNOSTIC MUST BE RUN ON A  
FORMATTED DISK PACK AND WILL DESTROY  
ALL DATA ON THE PACK.  
IF IT IS DESIRED TO FORMAT A PACK  
USE THE FORMATTING PROGRAM INCLUDED IN THE  
THE DIAGNOSTIC( TESTS 47 AND 50)

\*\*\*\*\*  
\*\*\*\*\*

1. SET PROGRAM COUNTER (PC) TO "START"  
ADDRESS .

36 000000 003000

WORD START

2. ENTER STARTING TEST NUMBER IN THE MOST SIGNIFICANT  
BYTE OF THE CONSOLE SWITCH REGISTER.

3. ENTER DESIRED END TEST NUMBER IN THE LEAST  
SIGNIFICANT BYTE OF THE CONSOLE SWITCH REGISTER.  
THE FIRST TEST NUMBER IS ZERO.

4. SET THE MOST SIGNIFICANT BIT (BIT 15) OF SWITCH  
REGISTER IF THE TESTS ARE TO BE REPEATED. LEAVE  
RESET IF THE TESTS ARE TO BE EXECUTED ONLY ONCE.

5. DEPRESS "START" SWITCH ON COMPUTER CONSOLE. THE  
COMPUTER WILL START AND THEN HALT.

6. ENTER STARTING DISK DRIVE NUMBER INTO THE MOST  
SIGNIFICANT BYTE OF CONSOLE SWITCH REGISTER.

7. ENTER NUMBER OF THE LAST DISK DRIVE TO BE TESTED IN  
THE LEAST SIGNIFICANT BYTE OF CONSOLE SWITCH REGISTER/  
NOTE THAT THE MAXIMUM DRIVE NUMBER=3(0 THRU 3)

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Line	Address	Label	Code	Comment
1				
2				
3				
4				FORMAT ROUTINE 9/29/75
5				THIS SUBROUTINE FORMATS THE DATA FOR THE
6				OUTPUT BUFFER USED IN ALL DISK WRITE
7				OPERATIONS.THE MESSAGE FORMATTED CONSISTS OF
8				64 WORDS OF AN DECREASING COUNT,
9				64 WORDS OF ALTERNATING 1 AND 0 CHARACTERS,
10				64 WORDS OF ALTERNATING CHECKERBOARD AND
11				REVERSE CHECKERBOARD CHARACTERS, AND 64 WORDS OF ALTERNATING
12				SLIDING ONES AND SLIDING ZERO WORDS
13				
14				AT ENTRY R1 POINTS TO THE BUFFER ORIGIN THAT IS TO BE FORMATTED.
15				
16				
17				
18	016736	010046	FORMAT:	MOV R0,-(SP) ;SAVE REGISTERS
19	016740	010146		MOV R1,-(SP) ;
20	016742	010246		MOV R2,-(SP) ;
21	016744	010346		MOV R3,-(SP) ;
22	016746	010546		MOV R5,-(SP) ;
23	016750	012700	000100	MOV #64,R0 ;GET CHARACTER COUNT
24	016754	010005		MOV R0,R5 ;SAVE IN R5 ALSO
25	016756	010021	F1LP:	MOV R0,(R1)+ ;FORMAT DATA WORD
26	016760	005300		DEC R0 ;DECREMENT CHARACTER COUNT,CHANGE DATA
27	016762	001375		BNE F1LP ;REPEAT IF NOT DONE
28	016764	005002		CLR R2 ;ESTABLISH 0 CHARACTER
29	016766	012703	000377	MOV #377,R3 ;ESTABLISH ALL 1'S CHARACTER
30	016772	010500		MOV R5,R0 ;REINITIALIZE CHARACTER COUNT
31	016774	110221	F2LP:	MOV B R2,(R1)+ ;INITIALIZE 0 CHARACTER
32	016776	110321		MOV B R3,(R1)+ ;INITIALIZE 1'S CHARACTER
33	017000	005300		DEC R0 ;DECREMENT LOOP COUNT
34	017002	001374		BNE F2LP ;REPEAT IF NOT DONE
35	017004	010500		MOV R5,R0 ;GET NEW CHARACTER LOOP COUNT
36	017006	012702	000125	MOV #125,R2 ;ESTABLISH CHECKERBOARD REFERENCE
37	017012	012703	000252	MOV #252,R3 ;ESTABLISH REVERSE LOOP COUNT
38	017016	110221	F3LP:	MOV B R2,(R1)+ ;INITIALIZE CHECKERBOARD CHARACTER
39	017020	110321		MOV B R3,(R1)+ ;INITIALIZE REVERSE CHECKERBOARD CHARACTER
40	017022	005300		DEC R0 ;DECREMENT LOOP COUNT
41	017024	001374		BNE F3LP ;REPEAT IF NOT DONE
42	017026	012705	000002	MOV #2,R5 ;ESTABLISH OUTER LOOP COUNT
43	017032	012700	000020	F0LP:
44	017036	012702	002652	MOV #16,R0 ;ESTABLISH INNER LOOP COUNT
45	017042	012221	F4LP:	MOV (R2)+,(R1)+ ;POINT R2 TO THE ORIGIN OF SLIDING ZERO
46	017044	005300		DEC R0 ;INITIALIZE BUFFER LOCATION
47	017046	001375		DEC R0 ;DECREMENT LOOP COUNT(INNER)
48	017050	012700	000020	BNE F4LP ;REPEAT IF NOT DONE
49	017054	012702	002612	MOV #16,R0 ;REESTABLISH INNER LOOP COUNT
50	017060	012221	F5LP:	MOV #S10RG,R2 ;POINT R2 TO ORIGIN OF SLIDING 1 TABLE
51	017062	005300		MOV (R2)+,(R1)+ ;INITIALIZE LOCATION WITH SLIDING 1 CONSTANT
52	017064	001375		DEC R0 ;DECREMENT LOOP COUNT
53	017066	005305		BNE F5LP ;REPEAT IF NOT DONE
54	017070	001360		DEC R5 ;DECREMENT OUTER LOOP COUNT
55	017072	012605		BNE F0LP ;REPEAT IF NOT DONE
56	017074	0126J3		MOV (SP)+,R5 ;RESTORE REGISTERS
57	017076	012602		MOV (SP)+,R3 ;
				MOV (SP)+,R2 ;

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58 017100 012601      MOV (SP)+,R1  ;
59 017102 012600      MOV (SP)+,R0  ;
60 017104 000205      RTS R5        ;RETURN TO TEST PROGRAM.
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92 017106 010046      DATCMP: MOV RO,-(SP) ;SAVE REGISTERS
93 017110 010146      MOV R1,-(SP)  ;
94 017112 010446      MOV R4,-(SP)  ;
95 017114 005037 001134 CLR CMCNT     ;RESET COMPARISON WORD COUNT
96 017120 013701 001234 MOV CURDSK,R1 ;GET CURRENT DISK NUMBER
97 017124 006301      ASL R1        ;MAKE VALID WORD INDEX
98 017126 016101 001200 MOV IBFTBL(R1),R1 ;GET INPUT BUFFER ORIGIN ADDRESS
99 017132 012704 044312 MOV #0DBUF,R4 ;GET OUTPUT BUFFER ADDRESS
100 017136 012402      DTCMLP: MOV (R4)+,R2 ;GET REFERENCE DATA WORD
101 017140 012103      MOV (R1)+,R3 ;GET ACTUAL DATA WORD
102 017142 020203      CMP R2,R3    ;ARE THEY EQUAL?
103 017144 001012      BNE DTCMER   ;EXIT WITH ERROR IF NOT
104 017146 005237 001134 DCMPA: INC CMCNT ;INCREMENT COMPARISON COUNT
105 017152 005300      DEC RO       ;DECREMENT WORD COUNT
106 017154 001370      BNE DTCMLP   ;REPEAT IF NOT DONE
107 017156 005037 001332 CLR RTRYIN    ;RESET RETRY INDEX
108 017162 012604      DTCMEX: MOV (SP)+,R4 ;RESTORE REGISTERS
109 017164 012601      MOV (SP)+,R1 ;
110 017166 012600      MOV (SP)+,R0 ;
111 017170 000205      RTS R5        ;RETURN
112 017172 005737 001244 DTCMER: TST NONCON ;CONSOLE ACTIVE?
113 017176 001035      BNE ERSET    ;SET ERROR IF NO
114 017200 005737 001104 TST TTYPUT    ;TELETYPE HERE?

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DATA COMPARE SUBROUTINE

THIS SUBROUTINE COMPARES DATA OBTAINED FROM THE DISK DURING ANY DISK READ OPERATION IN THE INPUT DATA BUFFER WITH THE REFERENCE DATA ACTUALLY WRITTEN ONTO THE DISK AND CONTAINED IN THE OUTPUT DATA BUFFER.

AT ENTRY RO CONTAINS THE NUMBER OF WORDS THAT ARE TO BE COMPARED.

IF AN ERROR OCCURS:

1. THE ERROR FLAG IS SET AND CONTROL IS TRANSFERRED BACK TO THE CALLING PROGRAM.
2. THE CMCNT COUNT LOCATION CONTAIN THE NUMBER OF THE COMPARISON AT WHICH THE ERROR WAS DETECTED.

115	017204	001032		BNE	ERSET	;	SET ERROR IF YES
116	017206	005737	177570	TST	CSWR	;	INHIBIT DATA ERROR ON?
117	017212	100027		BPL	ERSET	;	SET ERROR FLAG IF NO
118	017214	005237	001314	INC	ERRCNT	;	INCREMENT ERRCNT IF YES
119	017220	032737	000001 177570	BIT	#1,CSWR	;	ARE WE IN RETRY MODE?
120	017226	001747		BEQ	DCMPA	;	CHECK NEXT WORD IF NOT
121	017230	023727	001332 000020	CMP	RTRYIN,#16.	;	IS REENTRY INDEX LESS THAN 16.
122	017236	002012		BGE	HDERR	;	THIS IS A "HARD ERROR" IF NO
123	017240	013700	001332	MOV	RTRYIN,R0	;	GET ENTRY INDEX
124	017244	005360	001336	DEC	ERRTAB(RO)	;	DECREMENT CURRENT RETRY INDEX COUNT
125	017250	005720		TST	(RO)+	;	INCREMENT INDEX BY TWO
126	017252	010037	001332	MOV	RO,RTRYIN	;	SAVE UPDATED RETRY INDEX
127	017256	005260	001336	INC	ERRTAB(RO)	;	INCREMENT APPROPRIATE RETRY INDEX
128	017262	000737		BR	DTCMEX	;	GO TRY READ OPERATION AGAIN
129	017264	005237	001316	HDERR: INC	HERCNT	;	INCREMENT HARD ERROR COUNT
130	017270	000726		BR	DCMPA	;	GO ON TO NEXT WORD
131	017272	005237	001322	ERSET: INC	ERRFLG	;	SET GENERAL ERROR FLAG
132	017276	005237	001320	INC	DATERR	;	SET DATA ERROR FLAG
133	017302	000727		BR	DTCMEX	;	EXIT
134				;			
135				;			
136				;			
137				;			
138				;			
139				;			
140				;			
141				;			
142				;			
143				;			
144				;			
145				;			
146				;			
147				;			
148				;			
149				;			
150				;			
151				;			
152				;			
153	017304	010246		DSKDN: MOV	R2,-(SP)	;	SAVE R2
154	017306	105777	161500	TSTB	@DSTAT	;	IS THIS A SEEK INTERRUPT?
155	017312	100007		BPL	DKDNEX	;	SET INTERRUPT FLAG IF NO
156	017314	017702	161472	MOV	@DSTAT,R2	;	GET CURRENT STATUS REGISTER
157	017320	042702	177774	BIC	#177774,R2	;	EXTRACT DISK DRIVE IDENTIFICATION BITS
158	017324	006302		ASL	R2	;	MAKE DISK DRIVE NUMBER A VALID WORD INDEX
159	017326	010262	001122	MOV	R2,INTTBL(R2)	;	SAVE IDENT. IN TABLE LOCATION
160	017332	005237	001150	DKDNEX: INC	INTFLG	;	SET GENERAL INTERRUPT FLAG
161	017336	012602		MOV	(SP)+,R2	;	RESTORE R2
162	017340	000002		RTI		;	EXIT FROM INTERRUPT
163				;			
164				;			
165				;			
166				;			
167				;			
168				;			
169				;			
170				;			
171				;			

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WAIT SUBROUTINE

THIS ROUTINE WAITS A MAXIMUM OF APPROX.  
100MILLISECONDS OR UNTIL AN INTERRUPT OCCURS.  
WHICHEVER COMES FIRST CONTROL IS THEN TRANS-  
FERRED TO THE CALLING PROGRAM.

```

172
173
174
175
176 017342 010046      WAIT:  MOV  RD,-(SP)    ;SAVE RD AND R1
177 017344 010146      MOV   R1,-(SP)      ;
178 017346 013700 001510  MOV   TIMPL,R0      ;ESTABLISH OUTER WAIT LOOP
179 017352 012701 177777  WTPLA: MOV   @TIME,R1  ;ESTABLISH WAIT
180 017356 005737 001150  WTPL:  TST   INTFLG   ;HAS INTERRUPT OCCURRED YET?
181 017362 001004      BNE  WTEXTIT       ;EXIT IF YES
182 017364 005301      DEC  R1            ;DECREMENT LOOP COUNT
183 017366 001373      BNE  WTPL         ;REPEAT IF NOT DONE
184 017370 005300      DEC  R0            ;DECREMENT OUTER WAIT LOOP
185 017372 001367      BNE  WTPLA        ;LOOP AGAIN IF NO INTERRUPT
186 017374 012601      WTEXTIT: MOV  (SP)+,R1 ;RESTORE R1 AND R0
187 017376 012600      MOV  (SP)+,R0     ;
188 017400 005046      CLR  -(SP)        ;LOWER CPU HERE
189 017402 012746 017410  MOV   @WTPL1,-(SP) ;
190 017406 000002      RTI              ;
191 017410 000205      WTPL1: RTS       R5      ;RETURN NOW
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208 017412 005004      TN1:  CLR  R4        ;INITIALIZE SUBTEST NUMBER
209 017414 004537 004276  JSR  R5,REQUEST   ;REQUEST 211
210 017420 005000      CLR  R0          ;INITIALIZE REGISTER INDEX
211 017422 004537 017530  JSR  R5,LORD     ;JUMP TO LOAD AND READ ROUTINE
212 017426 005737 001322  TST  ERRFLG     ;ERROR OCCUR?
213 017432 001034      BNE  TN1ERR     ;EXIT IF ERROR
214 017434 005204      TN1A: INC  R4        ;SUBTEST NUMBER=1 (DCSR)
215 017436 022010      CMP  (R0)+,(R0) ;SELECT NEXT REGISTER
216 017440 004537 017530  JSR  R5,LORD     ;JUMP TO LOAD AND READ ROUTINE
217 017444 005737 001322  TST  ERRFLG     ;ANY ERRORS?
218 017450 001025      BNE  TN1ERR     ;EXIT IF ERROR
219 017452 005204      TN1B: INC  R4        ;SUBTEST NUMBER=2 (DCAR)
220 017454 022010      CMP  (R0)+,(R0) ;SELECT NEXT REGISTER
221 017456 004537 017530  JSR  R5,LORD     ;JMP YO LOAD AND READ ROUTINE
222 017462 005737 001322  TST  ERRFLG     ;ANY ERRORS?
223 017466 001016      BNE  TN1ERR     ;EXIT IF ERROR
224 017470 005204      TN1C: INC  R4        ;SUBTEST NUMBER=3 (DWCNT)
225 017472 022010      CMP  (R0)+,(R0) ;SELECT NEXT REGISTER
226 017474 004537 017530  JSR  R5,LORD     ;JUMP TO LOAD AND READ ROUTINE
227 017500 005737 001322  TST  ERRFLG     ;ANY ERRORS?
228 017504 001007      BNE  TN1ERR     ;EXIT IF ERROR
    
```

REGISTER LOAD AND READ TESTS

THIS ROUTINE TESTS THE CAPABILITY OF THE  
 SELECTED FORMATTER REGISTERS TO BE LOAD-  
 ED AND INTERROGATED WITH ANY DATA. EACH REGISTER  
 IS CHECKED WITH FOUR CONSTANTS 100 TIMES.

AT ENTRY, THE REGISTER INDEX IS IN R0.  
 IF AN ERROR IS DETECTED, THE TEST EXITS TO  
 PROGRAM CONTROL WITH THE ERROR FLAG SET.

229	017506	005204		TN1D:	INC R4		;SUBTEST NUMBER=4 (DCYL)
230	017510	022010			CMP (R0)+,(R0)		;SELECT NEXT REGISTER
231	017512	004537	017530		JSR R5,LDRD		;JUMP TO LOAD AND READ ROUTINE
232	017516	005737	001322		TST ERRFLG		;ANY ERRORS?
233	017522	001000			BNE TN1ERR		;EXIT IF ERROR
234	017524	004537	003342	TN1ERR:	JSR R5,TSTCTL		;EXIT TO PROGRAM CONTROL WITH ERROR
235							;FLAG SET IF A JUMP TO THIS INSTRUCTION
236							;WAS FROM LOAD AND READ ROUTINE.
237							;OTHERWISE ,ALL THE REGISTERS ARE CKECKED
238							;AND THE NEXT TEST CAN BE RUN
239							
240							
241							;LOAD AND READ ROUTINE
242							
243							
244	017530	010146		LDRD:	MOV R1,-(SP)		;SAVE REGISTERS,R1,R4,AND R5
245	017532	010446			MOV R4,-(SP)		
246	017534	010546			MOV R5,-(SP)		
247	017536	012704	000004		MOV #4,R4		;ESTABLISH CONSTANT LOOP COUNT
248	017542	012701	002712		MOV #CONST,R1		;POINT R1 TO THE CONSTANT TABLE
249	017546	010005			MOV R0,R5		;PUT THE REGISTER INDEX INTO R5
250	017550	063705	001000		ADD DCSR,R5		;COMPUTE REGISTER I/O ADDRESS
251	017554	012102		LRLP1:	MOV (R1)+,R2		;GET REFERENCE CONSTANT
252	017556	046002	002552		BIC REGHSK(R0),R2		;MASK OUT UNWANTED BITS
253	017562	005700			TST R0		;TEST R0 FOR REGISTER DCSR
254	017564	001006			BNE LRLP3		;CONTINUE IF NOT DCSR
255	017566	053702	001102		BIS MCPU,R2		;ENTER MULTPI
256	017572	042702	000100		BIC #INTON,R2		;AND INTERRUPT ENABLE
257	017576	052702	000200		BIS #FMTRDY,R2		;MASK IN FORMATTER READY
258	017602	012746	000144	LRLP3:	MOV #100,-(SP)		;LOOP COUNT
259	017606	010215		LRLP2:	MOV R2,R5		;LOAD REGISTER WITH CONSTANT
260	017610	011503			MOV R5,R3		;READ REGISTER BACK
261	017612	020203		LRLP4:	CMP R2,R3		;IS THE DATA RIGHT?
262	017614	001014			BNE LRERR		;NO:EXIT TO ERROR ROUTINE
263	017616	005316			DEC RSP		;DECREMENT REPEAT LOOP COUNT
264	017620	001372			BNE LRLP2		;REPEAT IF NOT DONE WITH LOOPS
265	017622	005304			DEC R4		;DECKREMENT CONSTANT LOOP COUNT
266	017624	001403			BEO LREX		;EXIT IF DCNE
267	017626	022606			CMP (SP)+,SP		;FIX UP STACK
268	017630	000137	017554		JMP LRLP1		;REPEAT TEST WITH NEXT CONSTANT
269	017634	022606		LREX:	CMP (SP)+,SP		;FIX UP THE STACK POINTER
270	017636	012605			MOV (SP)+,R5		;RESTORE REGISTERS,R5,R4 AND R1
271	017640	012604			MOV (SP)+,R4		
272	017642	012601			MOV (SP)+,R1		
273	017644	000205			RTS R5		;RETURN TO TEST NUMBER ONE
274	017646	005237	001322	LRERR:	INC ERRFLG		;SET ERROR FLAG
275	017652	000770			BR LREX		;EXIT TO TN1 WITH ERROR FLAG SET
276							
277							SLIDING ONES AND ZEROES TESTS
278							
279							IN THE FOLLOWING TESTS ALL THE CONTROLLER
280							REGISTERS ARE LOADED AND READ BACK WITH 15
281							PATTERNS OF BOTH SINGLE BIT ON AND SINGLE
282							BIT OFF DATA WORDS
283							
284	017654	005004		TN2:	CLR R4		;INITIALIZE SUBTEST NUMBER
285	017656	001537	004276		JSR R5,REQUEST		;REQUEST 211



286	017662	012700	000000		MOV #0,R0	;INITIALIZE REGISTER INDEX NUMBER
287	017666	012701	002612		MOV #S1ORG,R1	;LOAD ADDRESS OF SLIDING ONE TABLE
288	017672	004537	020144	TN2A:	JSR R5,SLIDE	;JUMP TO SLIDE ROUTINE
289	017676	005737	001322		TST ERRFLG	;ANY ERRORS? (CONTROL AND STATUS)
290	017702	001035			BNE TN2ERR	;EXIT IF ERROR
291	017704	005204			INC R4	;SUBTEST NUMBER =1
292	017706	012010			MOV (R0)+,(R0)	;SELECT NEXT REGISTER
293	017710	004537	020144	TN2B:	JSR R5,SLIDE	;JUMP TO SLIDE
294	017714	005737	001322		TST ERRFLG	;ANY ERRORS? (UNIT HEAD AND SECTOR )
295	017720	001026			BNE TN2ERR	;EXIT IF ERPOR
296	017722	005204			INC R4	;SUBTEST NUMBER=2 (CORE ADDR. REG)
297	017724	012010			MOV (R0)+,(R0)	;SELECT NEXT REGISTER
298	017726	004537	020144	TN2C:	JSR R5,SLIDE	;JMP TO SLIDE
299	017732	005737	001322		TST ERRFLG	;ANY ERRORS?
300	017736	001017			BNE TN2ERR	;EXIT IF ERRGRS
301	017740	005204			INC R4	;SUBTEST NUMBER=3 (WORD COUNT REG.)
302	017742	012010			MOV (R0)+,(R0)	;SELECT NEXT REGISTER
303	017744	004537	020144	TN2D:	JSR R5,SLIDE	;JUMP TO SLIDE ROUTINE
304	017750	005737	001322		TST ERRFLG	;ANY ERRORS
305	017754	001010			BNE TN2ERR	;EXIT IF ERROR
306	017756	005204			INC R4	;SUBTEST NUMBER =4 (CYLINDER ADDRESS REG)
307	017760	012010			MOV (R0)+,(R0)	;SELECT NEXT REGISTER
308	017762	004537	020144	TN2E:	JSR R5,SLIDE	;JUMP TOSLIDE ROUTINE
309	017766	005737	001322		TST ERRFLG	;ANY ERRORS?
310	017772	001001			BNE TN2ERR	;EXIT IF ERROR
311	017774	000402			BR TN2OUT	;EXIT TO NEXT TEST
312	017776	005237	001322	TN2ERR:	INC ERRFLG	;SET ERROR FLAG
313	020002	004537	003342	TN2OUT:	JSR R5,TSTCTL	;EXIT TO NEXT TEST
314					;	
315					;	SLIDING ZERO TEST
316					;	
317					;	
318	020006	005004		TN3:	CLR R4	;INITIALIZE SUBTEST NUMBER
319	020010	004537	004276		JSR R5,REQUEST	;REQUEST 211
320	020014	012700	000000		MOV #0,R0	;INITIALIZE REGISTER INDEX
321	020020	012701	002652		MOV #S0ORG,R1	;LOAD ADDRESS OF SLIDING ZERO TABLE
322	020024	004537	020144	TN3A:	JSR R5,SLIDE	;JUMP TOSLIDE ROUTINE
323	020030	005737	001322		TST ERRFLG	;ANY ERRORS? (CONTROL AND STATUS)
324	020034	001402			BEQ #+6	;CONTINUE IF NO
325	020036	000137	020136		JMP TN3ERR	;EXIT IF YES
326	020042	005204			INC R4	;SUBTEST NUMBER =1 (UNIT,HEAD AND SECTOR)
327	020044	012010			MOV (R0)+,(R0)	;SELECT NEXT REGISTER
328	020046	004537	020144	TN3B:	JSR R5,SLIDE	;JUMP TO SLIDE ROUTINE
329	020052	005737	001322		TST ERRFLG	;ANY ERRORS?
330	020056	001027			BNE TN3ERR	;EXIT IF ERROR
331	020060	005204			INC R4	;SUBTEST NUMBER=2 (CORE ADDR. REGISTER)
332	020062	012010			MOV (R0)+,(R0)	;SELECT NEXT REGISTER
333	020064	004537	020144	TN3C:	JSR R5,SLIDE	;JUMP TO SLIDE ROUTINE
334	020070	005737	001322		TST ERRFLG	;ANY ERRORS?
335	020074	001020			BNE TN3ERR	;EXIT IF ERROR
336	020076	005204			INC R4	;SUBTEST NUMBER=3 (WORD COUNT REGISTER)
337	020100	012010			MOV (R0)+,(R0)	;SELECT NEXT REGISTER
338	020102	004537	020144	TN3D:	JSR R5,SLIDE	;JUMP TO SLIDE ROUTINE
339	020106	005737	001322		TST ERRFLG	;ANY ERRORS?
340	020112	001011			BNE TN3ERR	;EXIT IF ERROR
341	020114	005204			INC R4	;SUB TEST NUMBER =4
342	020116	012010			MOV (R0)+,(R0)	;SEL. NEXT REG. (CYLINDER ADDRESS REG)

1	343	020120	004537	020144	TN3E:	JSR R5,SLIDE	;JMP TO SLIDE ROUTINE
2	344	020124	005737	001322		TST ERRFLG	;ANY ERRORS?
3	345	020130	001002			BNE TN3ERR	;EXIT IF ERROR
4	346						
5	347		001004			DBAR=DCAR	;REDEFINE CORE ADDRESS REGISTER FOR THOSE
6	348						PEOPLE WHO CALL IT BUSS ADDRESS REGISTER
7	349						
8	350	020132	004537	003342	TN3OUT:	JSR R5,TSTCTL	;EXIT IF DONE
9	351						
10	352						
11	353						
12	354						
13	355	020136	005237	001322	TN3ERR:	INC ERRFLG	;SET ERROR FLAG
14	356	020142	000773			BR TN3OUT	;AND EXIT
15	357						
16	358						
17	359						
18	360						
19	361						
20	362						
21	363						
22	364						SLIDE ROUTINE
23	365						
24	366						; THIS ROUTINE CONTROLS THE LOADING OF THE
25	367						; SLIDING ZERO AND ONE PATTERNS INTO THE
26	368						; DISK CONTROLLER REGISTERS.
27	369						
28	370	020144	010146		SLIDE:	MOV R1,-(SP)	;SAVE REGISTERS R1,R4,R5
29	371	020146	010446			MOV R4,-(SP)	
30	372	020150	010546			MOV R5,-(SP)	
31	373	020152	012704	000020		MOV #20,R4	;ESTABLISH LOOP COUNT
32	374	020156	010005			MOV R0,R5	;EST REGISTER INDEX INTO R5
33	375	020160	063705	001000		ADD DCSR,R5	;COMPUTE REGISTER I/O ADDRESS
34	376	020164	012102		SL1:	MOV (R1)+,R2	;GET REFERENCE CONSTANT
35	377	020166	046002	002552		BIC REGHSH(R0),R2	;MASK OUT UNWANTED BITS
36	378	020172	005700			TST R0	;IS THIS THE DCSR?
37	379	020174	001006			BNE SLIDE1	;NO CONTINUE
38	380	020176	052702	000200		BIS #FMTRDY,R2	;OR IN FORMATTER READY
39	381	020202	053702	001102		BIS MCPU,R2	;ENTER REQUEST BIT
40	382	020206	042702	000100		BIC #INTON,R2	;LOOSE INTERRUPT ENABLE
41	383	020212	010215		SLIDE1:	MOV R2,R5	;LOAD REGISTER
42	384	020214	011503			MOV @R5,R3	;READ REGISTER BACK
43	385	020216	020203		SLIDE2:	CMP R2,R3	;IS THE DATA CORRECT?
44	386	020220	001006			BNE SLERR	;NO EXIT TO ERROR ROUTINE
45	387	020222	005304			DEC R4	;DECREMENT LOOP COUNT
46	388	020224	001357			BNE SL1	;REPEAT TEST LOOP WITH NEXT CONSTANT
47	389	020226	012605		SLEX:	MOV (SP)+,R5	;RETRIEVE REGISTERS FROM STACK
48	390	020230	012604			MOV (SP)+,R4	
49	391	020232	012601			MOV (SP)+,R1	
50	392	020234	000205			RTS R5	;EXIT TO FETCH ANOTHER REGISTER
51	393	020236	005237	001322	SLERR:	INC ERRFLG	;ERROR OCCURRED SET ERROR FLAG
52	394	020242	000771			BR SLEX	;JUMP TO EXIT ROUTINE
53	395					JERREG•PAL	
54	396						
55	397						
56	398						
57	399						4M•ECC TEST NUMBERS 4>> 7 NOVEMBER-13-77

```

400      ;
401      ;
402      ;
403      ;
404      ;      DISK ERROR AND STATUS REGISTER TESTS
405      ;
406      ;
407      ;      THESE TESTS VERIFY THAT THE NONEXISTANT HEAD,
408      ;      SECTOR AND CYLINDER (TRACK) ERRORS CAN
409      ;      BE SET AND CLEARED PROPERLY.
410      ;
411      ;
412      ;      ALSO TESTED IN THIS TEST IS THE BYTE LOADING
413      ;      CAPABILITY OF THE COMMAND AND STATUS REG (DCSR).
413 020244 004537 004276      TN4: JSR   R5,RQEST      ;FETCH 211
414 020250 000005              RESET          ;RESET I/O BUSS
415 020252 004537 004276      JSR   R5,RQEST      ;GET 211 AGAIN
416 020256 005004              CLR   R4          ;INITIALIZE SUBTEST NUMBER=0
417 020260 004537 021100      JSR   R5,TSTDSK   ;FORMATTER READY? WAIT IF NOT
418 020264 013701 001040      MOV   MAXSEC,R1   ;LOAD ILLEGAL SECTOR NUMBER
419 020270 005201              INC   R1          ;
420 020272 010177 160504      MOV   R1,@DUSH   ;
421 020276 004537 016332      JSR   R5,DISKID   ;SET UP CURRENT DISK SELECT
422 020302 050277 160474      BIS   R2,@DUSH   ;SELECT DISK
423 020306 052777 000077      BIS   @NOPCHD,@DCSR ;ISSUE NOP COMAND
424 020314 004537 021100      JSR   R5,TSTDSK   ;WAIT FORMATTER READY
425 020320 005777 160454      TST   @DCSR      ;ERROR
426 020324 100402              BHI   +6          ;CONTINUE IF YES
427 020326 000137 021020      TN4EX: JMP  TN4ERR      ;NO:GOTO NEXT TEST
428 020332 005204              INC   R4          ;SUBTEST NUMBER=1(ERROR DETECTED)
429 020334 012702 000100      MOV   #100,R2     ;SET UP REFERENCE WORD
430 020340 017703 160450      MOV   @DERR,R3    ;FETCH ERROR REGISTER
431 020344 042703 010000      BIC   #10000,R3   ;CLEAR DRIVE NOT READY IF SET
432 020350 020203              CMP   R2,R3      ;ERROR DETECTED?
433 020352 001365              BNE   TN4EX      ;NOT DETECTED SET ERROR FLAG
434 020354 005204              TN4A: INC  R4      ;SUBTEST NUMBER=2(CLR SECTOR ERROR)
435 020356 004537 021030      JSR   R5,CLRERR   ;JUMP TO CLEAR ERROR
436 020362 005737 001322      TST   ERRFLG     ;ERROR FLAG SET?
437 020366 001402              BEQ   +6          ;NO,CONTINUE
438 020370 000137 021024      JMP   TN4FIN      ;YES:EXIT TO NEXT TEST
439 020374 005204              TN4B: INC  R4      ;SUBTEST NUMBER=3(FORCE HEAD ERROR)
440 020376 013702 001042      MOV   MAXHD,R2   ;LOAD MAXIMUM HEAD ADDRESS
441 020402 062702 000200      ADD   @HDINC,R2  ;MAKE ILLEGAL ADDRESS
442 020406 010277 160370      MOV   R2,@DUSH   ;LOAD INTO DUSH REGISTER
443 020412 004537 016332      JSR   R5,DISKID   ;SET UP CURENT DISK SELECT
444 020416 050277 160360      BIS   R2,@DUSH   ;OR IN SELECT
445 020422 052777 000077      BIS   @NOPCHD,@DCSR ;ISSUE NOP COMMAND
446 020430 004537 021100      JSR   R5,TSTDSK   ;WAIT FORMATTER READY
447 020434 005777 160340      TST   @DCSR      ;ERROR DETECTED?
448 020440 100332              BPL   TN4EX      ;NOT DETECTED GO TO NEXT TEST
449 020442 005204              INC   R4          ;SUBTEST NUMBER=4(ERROR DETECTED)
450 020444 012702 000020      MOV   #20,R2     ;SET UP REFERENCE WORD
451 020450 017703 160340      MOV   @DERR,R3    ;FETCH ERROR REGISTER
452 020454 042703 010000      BIC   #10000,R3   ;CLR DRIVE NOT READY IF SET
453 020460 020203              CMP   R2,R3      ;EQUAL?
454 020462 001321              BNE   TN4EX      ;NOT EQUAL EXIT
455 020464 005204              TN4C: INC  R4      ;SUBTEST NUMBER=5(HEAD ERROR DETECTED)
456 020466 004537 021030      JSR   R5,CLRERR   ;CLEAR ERROR FLAG

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457	020472	005737	001322	TST	ERRFLG		ERROR FLAG CLEARED?
458	020476	001152		BNE	TN4FIN		NOT CLEARED:EXIT TO NEXT TEST
459	020500	005204		TN4D:	INC	R4	SUBTEST NUMBER=6(ERROR CLEARED)
460	020502	004537	016332	JSR	R5,DISKID		SET UP CURRENT DISK SELECT
461	020506	010277	160270	MOV	R2,@DUSH		SELECT DISK
462	020512	013702	001044	MOV	MAXCYL,R2		LOAD ILLEGAL CYLINDER ADDRESS
463	020516	005202		INC	R2		
464	020520	010277	160264	MOV	R2,@DCYL		LOAD INTO CYLINDER ADDRESS REGISTER
465	020524	052777	000077	160246	BIS	#NOPCMD,@DCSR	ISSUE NOP COMMAND
466	020532	004537	021100	JSR	R5,TSTDSK		WAIT FORMATTER READY
467	020536	005777	160236	TST	@DCSR		ERROR DETECTED?
468	020542	100126		BPL	TN4ERR		NOT DETECTED:EXIT TO NEXT TEST
469	020544	005204		INC	R4		SUBTEST NUMBER=7(ERROR DETECTED)
470	020546	012702	000040	MOV	#40,R2		SET UP REFERENCE WORD
471	020552	017703	160236	MOV	@DERR,R3		FETCH ERROR REGISTER
472	020556	042703	010000	BIC	#10000,R3		EXTRACT DRIVE NOT READY
473	020562	020203		CMP	R2,R3		
474	020564	001260		BNE	TN4EX		EXIT IF NOT EQUAL
475	020566	005204		TN4E:	INC	R4	SUBTEST NUMBER=10(NONEX CYL OK)
476	020570	004537	021030	JSR	R5,CLRERR		CLEAR ERROR FLAG
477	020574	005737	001322	TST	ERRFLG		ERROR FLAG CLEARED?
478	020600	001111		BNE	TN4FIN		NOT CLEARED:EXIT TO NEXT TEST
479	020602	005204		TN4F:	INC	R4	SUBTEST NUMBER=15(ERROR CLEARED)
480	020604	013702	001040	MOV	MAXSEC,R2		FORCE ALL THREE NONEXISTANT ERRORS
481	020610	005202		INC	R2		
482	020612	063702	001042	ADD	MAXHD,R2		INCLUDE HEAD
483	020616	062702	000200	ADD	#HDINC,R2		
484	020622	010277	160154	MOV	R2,@DUSH		LOAD INTO DUSH
485	020626	004537	016332	JSR	R5,DISKID		SET UP CURRENT DISK SELECT
486	020632	050277	160144	BIS	R2,@DUSH		OR IT IN
487	020636	013777	001044	160144	MOV	MAXCYL,@DCYL	LOAD ILLEGAL CYLINDER ADDR
488	020644	005277	160140	INC	@DCYL		
489	020650	052777	000077	160122	BIS	#NOPCMD,@DCSR	SEND NOP COMMAND
490	020656	004537	021100	JSR	R5,TSTDSK		WAIT FORMATTER READY
491	020662	005777	160112	TST	@DCSR		ERROR DETECTED?
492	020666	100054		BPL	TN4ERR		NOT DETECTED:EXIT TO NEXT TEST
493	020670	005204		INC	R4		SUBTEST NUMBER=12(ERROR DETECTED)
494	020672	012702	000160	MOV	#160,R2		SET UP REFERENCE WORD
495	020676	017703	160112	MOV	@DERR,R3		FETCH ERROR REGISTER
496	020702	042703	010000	BIC	#10000,R3		CLEAR DRIVE NOT READY
497	020706	020203		CMP	R2,R3		EQUAL?
498	020710	001043		BNE	TN4ERR		EXIT IF NOT
499	020712	005204		TN4G:	INC	R4	SUBTEST NUMBER=13(ERRORS OK)
500	020714	004537	021030	JSR	R5,CLRERR		CLEAR ERROR FLAG
501	020720	005737	001322	TST	ERRFLG		ERROR FLAGS CLEARED?
502	020724	001035		BNE	TN4ERR		EXIT IF NOT CLEARED
503	020726	005204		INC	R4		SUBTEST NUMBER=14(ERRORS CLEARED)
504							CHECK DCSR BYTE LOAD
505	020730	013701	001000	MOV	DCSR,R1		ATTEMPT BYTE LOAD OF DCSR
506	020734	005201		INC	R1		POINT R1 TO DCSR+1
507	020736	012702	000177	MOV	#177,R2		SET UP DATA WORD
508	020742	150211		BISB	R2,(R1)		LOAD I BYTE OF DCSR
509	020744	111103		MOV	(R1),R3		REREAD DCSR+1
510	020746	020203		CMP	R2,R3		READ OK?
511	020750	001023		BNE	TN4ERR		EXIT IF NO
512	020752	005204		INC	R4		SUBTEST NUMBER=15(UPPER BYTE OK)
513	020754	152777	000176	160016	BISB	#176,@DCSR	LOAD LOWER BYTE OF DCSR

514	020762	112702	000176		MOV#176,R2	LOAD R2 WITH REFERENCE
515	020766	117703	160006		MOV# 0DCSR,R3	FETCH DCSR REGISTER
516	020772	042703	177600		BIC #177600,R3	EXTRACT LOWER BITS
517	020776	005737	001076		TST MUCPU	IS THIS A MULTIPLE CPU SET UP?
518	021002	001404			BEQ TN4H	CONTINUE IF NO
519	021004	042702	000040		BIC #BITS,R2	LOOSE BIT 5 IF YES
520	021010	042703	000040		BIC #BITS,R3	IN BOTH WORDS
521	021014	020203		TN4H:	CHP R2,R3	ARE THEY EQUAL?
522	021016	001402			BEQ TN4FIN	EXIT IF YES
523	021020	005237	001322	TN4ERR:	INC ERRFLG	SET ERROR FLAG
524	021024	004537	003342	TN4FIN:	JSR R5,TSTCTL	EXIT TO PROGRAM CONTROL
525						
526						
527						CLEAR ERROR FLAGS
528						
529						
530						THIS ROUTINE CLEARS ERROR FLAGS AND TESTS THAT
531						THEY ARE ACTUALLY CLEARED, THEN RETURNS TO THE
532						ERROR STATUS REGISTER TESTS
533						
534						
535	021030	042777	000136	157742	CLRERR: BIC #FUNC,0DCSR	LOOSE FUNCTION BITS
536	021036	052777	000001	157734	BIS #SYSCLR,0DCSR	ISSUE FORMATTER CLEAR
537	021044	004537	004276		JSR R5,RQUEST	GET 211
538	021050	004537	021100		JSR R5,TSTDSK	WAIT FORMATTER READY
539	021054	005777	157720		TST 0DCSR	ERROR(S) CLEARED?
540	021060	100404			BMI CERR	NOT CLEARED EXIT TO SET ERROR FLAG
541	021062	005777	157726		TST 0DERR	ERROR CLEARED IN DERR?
542	021066	001001			BNE CERR	NO: SET ERROR FLAG
543	021070	000402			BR ++6	EXIT
544	021072	005237	001322	CERR:	INC ERRFLG	SET ERROR FLAG
545	021076	000205			RTS R5	RETURN TO TN4(ERROR REG TEST)
546	021100	105777	157674	TSTDSK:	TSTB 0DCSR	TEST FORMATTER READY?
547	021104	100375			BPL TSTDSK	WAIT
548	021106	000205			RTS R5	JUMP BACK TO TN4
549						UNSEL PAL
550						
551						9/23/75
552						
553						
554						THE UNIT SELECT TESTS VERIFY THAT THE UNIT
555						SELECT LINES ACCESS THE PROPER DISK DRIVES.
556						THIS TESTING IS ACCOMPLISHED BY SELECTING
557						EACH DRIVE AND ISSING A RECALIBRATE.
558						THE DSTAT REGISTER SEEKING FLOPS ARE
559						CHECKED FOR PROPER SEEKING STATUS AND
560						A FORMATTER CLEAR IS THEN GIVEN TO CLEAR THEM.
561						THIS TEST DOES NOT WAIT FOR SEEK DONE.
562						
563						
564						
565	021110	005004		TNST:	CLR R4	INITIALIZE SUBTEST NUMBER
566	021112	004537	004276		JSR R5,RQUEST	GET 211
567	021116	105777	157656		TSTB 0DCSR	FORMATTER READY?
568	021122	100126			BPL TN5ERR	NOEXIT
569	021124	004537	004066		JSR R5,SEKTIH	SET UP WAIT LOOP
570	021130	005737	001322		TST ERRFLG	ERRORS?



```

628      ;
629      ;
630      ;
631 021406 010177 157370      SELECT:  MOV    R1,0DUSH      ;SELECT NEXT UNIT
632 021412 042777 000136 157360      BIC    #FUNC,#DCSR      ;CLEAR FUNCTION BITS
633 021420 052777 000024 157352      BIS    #RTZCMD,#DCSR    ;ISSUE RECALIBRATE
634 021426 005277 157346      INC    #DCSR      ;SET GO
635 021432 012703 000020      MOV    #20,R3      ;INSURE FORMATTER BUSY
636 021436 005303      DEC    R3      ;
637 021440 001376      BNE    #-2      ;
638 021442 105777 157332      TSTB  #DCSR      ;WAIT FORMATTER READY
639 021446 100375      BPL    #-4      ;WAIT
640 021450 017703 157336      MOV    #DSTAT,R3     ;FETCH DISK STATUS REGISTER
641 021454 042703 100000      BIC    #BIT15,R3     ;EXTRACT POSSIBLE DRIVE READY
642 021460 042703 040000      BIC    #BIT14,R3     ;EXTRACT POSSIBLE PORT BUSY
643 021464 042703 020000      BIC    #BIT13,R3     ;AND ALSO POSSIBLE WRITE PROTECT
644 021470 020203      CMP    R2,R3      ;RIGHT FLOP SET?
645 021472 001003      BNE    SELA      ;NO EXIT
646 021474 004537 022164      JSR    R5,WAIT1     ;WAIT FOR SEEK DONE IF DRIVE READY
647 021500 000205      RTS    R5      ;RETURN
648 021502 005237 001322      SELA:  INC    ERRFLG    ;SET ERROR FLAG
649 021506 000205      RTS    R5      ;
650      ;
651      ;
652      ;
653 021510 042777 000136 157262 CLRFR:  BIC    #FUNC,#DCSR    ;LOCSE FUNCTION BITS
654 021516 052777 000001 157254      BIS    #SYSCLR,#DCSR  ;ISSUE SYSCLR
655 021524 004537 004276      JSR    R5,REQUEST    ;GET 211
656 021530 105777 157244      TSTB  #DCSR      ;FORMATTER READY?
657 021534 100402      BMI    #+6      ;EXIT IF YES
658 021536 005237 001322      INC    ERRFLG      ;SET ERROR FLAG IF NO
659 021542 000205      RTS    R5      ;RETURN TO PROGRAM TN5
660      ;SEKST.PAL
661      ;
662      ;
663      ;
664      ;
665      ;
666      ;
667      ;
668      ;
669      ;
670      ;
671      ;
672      ;
673      ;
674 021544 005004      TN6:  CLR    R4      ;INITIALIZE SUBTEST NUMBER
675 021546 004537 004276      JSR    R5,REQUEST    ;GET 211
676 021552 052777 000001 157220      BIS    #SYSCLR,#DCSR  ;ISSUE SYSTEM CLEAR
677 021560 004537 004276      JSR    R5,REQUEST    ;GET IT AGAIN
678 021564 105777 157210      TSTB  #DCSR      ;TEST FORMATTER READY
679 021570 100145      BPL    TN6ERR      ;NOT READY:EXIT
680 021572 005204      INC    R4      ;SUBTEST NUMBER=1
681 021574 004537 016332      JSR    R5,DISKID     ;SET UP UNIT SELECT BIT
682 021600 010201      MOV    R2,R1      ;SAVE IN REG R1
683 021602 013702 002616      MOV    $10R6+4,R2    ;SET UP SEEKING FLOP
684 021606 013700 001234      MOV    CURDSK,R0      ;

```

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SEEKING TESTS

THESE TESTS SEND SEEK COMMANDS (2) TO THE DRIVE UNIT CURRENTLY UNDER TEST AND CHECKS THAT THE PROPER DRIVE HAS DONE A SEEK. THERE IS NO ACTUAL DATA TRANSFER BETWEEN THE PROCESSOR AND THE DISK IN THESE TESTS.





```

742      ;
743      ;
744 022100 004537 003342      TN6OUT: JSR  R5,TSTCTL  ;EXIT TO PROGRAM CONTROL
745 022104 005237 001322      TN6ERR: INC  ERRFLG  ;SET ERROR FLAG
746 022110 000775              BR    TN6OUT    ;EXIT
747      ;
748      ;
749      ;
750 022112 005777 156662      TN6CHK: TST    @DCSR  ;ANY ERRORS?
751 022116 100405              BMI  CHKERR  ;YES:EXIT
752 022120 004537 022164      JSR  R5,WAIT1  ;WAIT
753 022124 105777 156662      TSTB   @DSTAT  ;SEEK DONE?
754 022130 100402              BMI  EXIT6   ;YES:GO BACK TO TN6
755 022132 005237 001322      CHKERR: INC  ERRFLG  ;SET ERROR FLAG
756 022136 000205              EXIT6: RTS  R5    ;RETURN TO TN6
757      ;
758      ;
759      ;
760 022140 017703 156646      T6DONE: MOV   @DSTAT,R3  ;MOVE DISK REG IMAGE INTO R3
761 022144 042703 177703      BIC   #177703,R3  ;EXTRACT SEEK DONE BITS
762 022150 010002              MOV   R0,R2      ;SET UP REFERENCE WORD
763 022152 020203              CMP   R2,R3      ;PROPER DRIVE DONE?
764 022154 001402              BEQ   @+6        ;YES EXIT
765 022156 005237 001322      INC  ERRFLG  ;NO:SET ERROR FLAG
766 022162 000205              RTS  R5        ;RETURN TO TN6
767 022164 010146              WAIT1: MOV  R1,-(SP) ;SAVE REGISTER IN STACK
768 022166 010046              MOV   R0,-(SP);
769 022170 013700 001310      MOV   TIMLP,R0   ;SET OUTER LOOP SIZE
770 022174 012701 177777      WAIT1A: MOV  @TIME,R1 ;LOAD INNER LOOP COUNT
771 022200 005301              DEC  R1          ;DECREMENT LOOP COUNT
772 022202 001376              BNE  @-2        ;DONE?,IF NOT LOOP AGAIN
773 022204 005300              DEC  R0          ;DECREMENT OUTER LOOP
774 022206 001372              BNE  WAIT1A     ;CONTINUE IF NOT DONE
775 022210 012600              MOV  (SP)+,R0;
776 022212 012601              MOV  (SP)+,R1   ;GET R1 BACK
777 022214 000205              RTS  R5        ;RETURN TO PROGRAM
778      ;
779      ;
780      ;
781      ;
782      ;
783      ;
784      ;
785      ;
786      ;
787      ;
788      ;
789      ;
790      ;
791      ;
792      ;
793      ;
794      ;
795      ;
796      ;
797      ;
798      ;

```

9126775

INTERRUPT TESTS

```

; THE INTERRUPT TESTS USE TWO FORMATTER
; COMMANDS,THE RECALIBRATE COMMAND AND THE SEEK
; ONLY COMMAND.AT THIS STAGE OF TESTING THE SEEK
; LOGIC SHOULD BE OPERABLE.
; THE INTERRUPT LOGIC USES THESE COMMANDS TO
; CAUSE THE SEEK DONE IDENTIFICATION BITS FLAG AN
; INTERRUPT.
; IF THE CPU HALTS DURING THIS TEST TO SOME
; MEMORY LOCATION BETWEEN 14 AND 776 THE
; THE INTERRUPT BRANCHED TO A WRONG LOCATION.

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970	022714	005037	001150	CLR	INTFLG	INITIALIZE INTERRUPT FLAG
971	022720	005004		CLR R4		INITIALIZE SUBTEST NUMBER =0
972	022722	105777	156052	TSTB	@DCSR	IS THE CONTROLLER READY?
973	022726	100174		BPL	DTERR	NO, EXIT WITH ERROR
974	022730	005204		INC R4		SUBTEST NUMBER=1(CONTROLLER READY)
975	022732	004537	016332	JSR	R5,DISKID	SET UP DRIVE SELECT
976	022736	010201		MOV	R2,R1	SAVE IN R1
977	022740	042710	030000	BIC	#30000,(R0)	CLEAR PREVIOUS UNIT SELECT
978	022744	050110		BIS	R1,(R0)	OR IN UNIT SELECT INTO USH REGISTER
979	022746	013701	001002	MOV	DUSH,R1	GET UNIT,SECTOR,HEAD REGISTER ADDR.
980	022752	012021		MOV	(R0)+,(R1)+	SELECT DISK DRIVE(AND INIT. SEEK)
981	022754	000240		NOP		
982	022756	023727	001232 000027	CHP	CURTN,#27	DO WE CARE IF DISK READY?
983	022764	001403		BEQ	DXF1	CONTINUE IF NO
984	022766	005777	156020	TST	@DSTAT	DRIVE READY?
985	022772	100152		BPL	DTERR	NO EXIT DRIVE NOT READY
986	022774	005204		INC R4		SUBTEST NUMBER=2(DRIVE READY OR DON'T CARE)
987	022776	012021		MOV	(R0)+,(R1)+	LOAD BUSS ADDRESS REGISTER WITH
988						DATA BUFFER ORIGIN ADDRESS
989	023000	012021		MOV	(R0)+,(R1)+	LOAD WORD COUNT REGISTER
990	023002	012021		MOV	(R0)+,(R1)+	LOAD CYLINDER ADDRESS REGISTER
991	023004	053710	001102	BIS	MCPU,(R0)	LOAD REQUEST BIT IF APPL.
992	023010	011077	155764	MOV	(R0),@DCSR	LOAD COMMAND (NO GO BIT)
993	023014	043710	001102	BIC	MCPU,(R0)	LOOSE REQUEST BIT
994	023020	105777	155754	TSTB	@DCSR	DID THE CONTROLLER GO BUSY?
995	023024	001535		BEQ	DTERR	EXIT WITH ERROR IF YES
996	023026	005204		INC R4		SUBTEST NUMBER=3(NO ERRONEOUS CONT. BUSY)
997	023030	005737	001062	TST	STRCNT	SEE IF STRIP APPLICABLE
998	023034	001403		BEQ	+6	CONTINUE IF NO
999	023036	012777	0000006 155770	MOV	#STRBUF,@DCSR	ENTER STRIP BUFFER ADDRESS
1000	023044	052777	000101 155726	BIS	#INTGO,@DCSR	ENABLE INTERRUPTS AND GO!!!!!!!!!!!!
1001	023052	000240		NOP		
1002	023054	000240		NOP		
1003	023056	000240		NOP		
1004	023060	105777	155714	TSTB	@DCSR	CONTROLLER BUSY?
1005	023064	100515		BMI	DTERR	EXIT WITH ERROR IF NO
1006	023066	005204		INC R4		SUBTEST NUMBER=4(CONTROLLER BUSY)
1007	023070	004537	017342	JSR	R5,WAIT	WAIT FOR INTERRUPT OR TIME OUT
1008	023074	005737	001150	TST	INTFLG	DID AN INTERRUPT OCCUR?
1009	023100	001507		BEQ	DTERR	EXIT WITH ERROR IF NO
1010	023102	005204		INC R4		SUBTEST NUMBER=5
1011	023104	005037	001150	CLR	INTFLG	CLEAR INTERRUPT FLAG IF IT WAS SET
1012	023110	105777	155664	TSTB	@DCSR	IS THE CONTROLLER STILL BUSY?
1013	023114	100101		BPL	DTERR	EXIT WITH ERROR IF YES
1014	023116	005204		INC R4		SUBTEST NUMBER =6
1015	023120	005002		CLR	R2	EST. REFERENCE FOR WORD COUNT
1016	023122	017703	155660	MOV	@WVCNT,R3	GET ACTUAL WORD COUNT REGISTER
1017	023126	020203		CHP	R2,R3	DID WORD COUNT OVERFLOW GO TO ZERO?
1018	023130	001073		BNF	DTERR	EXIT WITH ERROR IF NO
1019	023132	005204		INC R4		SUBTEST NUMBER =7
1020	023134	024040		CHP	-(R0),-(R0)	POINT R5 TO WORD COUNT VALUE
1021	023136	011002		MOV	@RO,R2	GET ORIGINAL WORD COUNT
1022	023140	005402		NEG	R2	FORM POSITIVE VALUE
1023	023142	006302		ASL	R2	MAKE VALID WORD COUNT
1024	023144	064002		ADD	-(R0),R2	COMPUTE REFERENCE ENDING BUS ADDRESS
1025	023146	005720		TST	(R0)+	RESTORE R0 FOR ENDPAR ROUTINE
1026	023150	017703	155630	MOV	@DCAR,R3	GET ACTUAL END BUSS ADDR. VALUE

1027	023154	020203		CMP R2,R3	);IS END BUS ADDRESS CORRECT?
1028	023156	001060		BNE DTERR	);EXIT WITH ERROR IF NO
1029	023160	005204		INC R4	);SUBTEST NUMBER=10
1030	023162	004537	022436	JSR R5,ENDPAR	);COMPUTE END DISK PARAMETERS
1031	023166	013702	001162	MOV ENDSEC,R2	);GET COMPUTED END SECTOR VALUE
1032	023172	017703	155604	MOV @DUSH,R3	);GET UNIT,SECTOR HEAD REG.
1033	023176	010301		MOV R3,R1	);SAVE IN R1 ALSO
1034	023200	042703	177600	BIC #SECHSK,R3	);EXTRACT ACTUAL SECTOR VALUE
1035	023204	020203		CMP R2,R3	);IS THE SECTOR VALUE CORRECT?
1036	023206	001044		BNE DTERR	);EXIT WITH ERROR IF NO
1037	023210	005204		INC R4	);SUBTEST NUMBER=11
1038	023212	013702	001164	MOV ENDHD,R2	);GET COMPUTED END HEAD VALUE
1039	023216	010103		MOV R1,R3	);GET UNIT,SEC,HEAD VALUE AGAIN
1040	023220	042703	170177	BIC #HDMSK,R3	);EXTRACT HEAD FIELD BITS
1041	023224	020203		CMP R2,R3	);IS THE ACTUAL HEAD VALUE CORRECT?
1042	023226	001034		BNE DTERR	);EXIT WITH ERROR IF NO
1043	023230	005204		INC R4	);SUBTEST NUMBER=12
1044	023232	013702	001166	MOV ENDCYL,R2	);GET COMPUTED END CYLINDER ADDRESS
1045	023236	017703	155546	MOV @DCYL,R3	);GET ACTUAL CYLINDER ADDRESS
1046	023242	020203		CMP R2,R3	);IS THE CYLINDER ADDRESS CORRECT?
1047	023244	001025		BNE DTERR	);EXIT WITH ERROR IF NO
1048	023246	005204		INC R4	);SUBTEST NUMBER=13
1049	023250	017703	155524	MOV @DCSR,R3	);TAKE A LOOK AT MEMORY EXTENSION BITS
1050	023254	042703	147777	BIC #147777,R3	);EXTRACT MEMORY EXTENSION BITS
1051	023260	005002		CLR R2	);SET UP REFERENCE WORD
1052	023262	020203		CMP R2,R3	);ANY BITS SET?
1053	023264	001015		BNE DTERR	);EXIT IF YES
1054	023266	005204		INC R4	);SUBTEST NUMBER=14(NO MEMORY EXT. BITS SET)
1055	023270	005777	155504	TST @DCSR	);ANY CONTROLLER ERRORS STILL?
1056	023274	100477		BMI CTLERR	);FIND OUT WHICH ONE IF YES
1057	023276	005037	001132	CLR SOFTRY	);CLEAR REREAD FLAG IF SET
1058	023302	005037	001326	CLR SOFER1	);CLEAR RETRY ATTEMPT COUNTER
1059	023306	012605		DTEXIT: MOV (SP)+,R5	);RESTORE REGISTERS
1060	023310	012604		MOV (SP)+,R4	);
1061	023312	012601		MOV (SP)+,R1	);
1062	023314	012600		MOV (SP)+,R0	);
1063	023316	000205		RTS R5	);EXIT TO CALLING PROGRAM
1064	023320	005777	155454	DTERR: TST @DCSR	);CONTROLLER READY?
1065	023324	100006		BPL DTERRA	);EXIT NORMALLY IF NO
1066	023326	017705	155462	MOV @DERR,R5	);GET ERROR REGISTER IMAGE
1067	023332	042705	175000	BIC #175000,R5	);EXTRACT POSSIBLE SOFT ERROR BITS
1068	023336	005705		TST R5	);ARE THERE ANY ON
1069	023340	001023		BNE DSERR	);RETRY TRANSFER IF YES
1070	023342	005237	001322	DTERRA: INC ERRFLG	);SET GENERAL ERROR FLAG
1071	023346	013700	001000	MOV DCSR,R0	);GET ADDR OF CONTROL AND STATUS REG
1072	023352	012701	035334	MOV #ERRBLK,R1	);GET ERROR BLOCK ADDRESS
1073	023356	012705	000007	MOV #7,R5	);ESTABLISH LOOP COUNT
1074	023362	012021		MOV (R0)+,(R1)+	);SAVE DISK CONT REGISTER IMAGES
1075	023364	005305		DEC R5	);DECREMENT LOOP COUNT
1076	023366	001375		BNE #-4	);REPEAT IF NOT DONE
1077	023370	005737	001074	TST ECC	);IS THIS ECC?
1078	023374	001402		BEO DERECC	);GO NO IF NO
1079				);	
1080	023376	012021		MOV (R0)+,(R1)+	);LOAD ECCPB IF YES
1081	023400	012021		MOV (R0)+,(R1)+	);AND ECCPW ALSO
1082				);	
1083	023402			DERECC:	

1084	023402	010437	001152		MOV R4,DTCNT	SAVE SUBTEST COUNT
1085	023406	000737			BR DTEXT	EXIT
1086	023410	005737	001244	DSERR:	TST NONCON	CONSOLE ACTIVE?
1087	023414	001352			BNE DTERRA	EXIT IF NO
1088	023416	032737	040000 177570		BIT #40000,CSWR	RETRY?
1089	023424	001746			BEO DTERRA	EXIT WITH ERROR IF NO
1090	023426	023727	001326 000004		CHP SOFER1,#4	HAVE WE TRIED 4 TIMES YET?
1091	023434	001412			BEO DSERRA	EXIT IF YES
1092	023436	005237	001326		INC SOFER1	INCREMENT SOFT RETRY COUNTER
1093	023442	005237	001330		INC SOFERR	INCREMENT SOFT ERROR COUNTER
1094	023446	012605			MOV (SP)+,R5	
1095	023450	012604			MOV (SP)+,R4	
1096	023452	012601			MOV (SP)+,R1	
1097	023454	012600			MOV (SP)+,R0	
1098	023456	000137	022700		JMP DXFER	GO RETRY TRANSFER
1099	023462	005037	001326	DSERRA:	CLR SOFER1	CLEAR RETRY COUNTER
1100	023466	005237	001132		INC SOFTK1	SET SOFT RETRY STOP FLAG
1101	023472	000723			BR DTERRA	AND EXIT
1102	023474	004537	023502	CTLERR:	JSR RS,ERRID	SAVE CONTROLLER REGISTERS
1103	023500	000707			BR DTERR	AND GO INTO ERROR ROUTINE
1104						
1105						
1106						
1107						ERROR IDENTIFICATION ROUTINE
1108						
1109						THIS SUBROUTINE EXAMINES THE DISK CONTROLLER
1110						ERROR STATUS REGISTER STARTING WITH THE
1111						FIRST BIT(0),AND STORES THE MASK OF THE FIRST
1112						ERROR BIT ENCOUNTERED THAT IS ACTIVE IN LOCATION
1113						ERRWRD.THE COMPLETE DISK ERROR REGISTER STATE
1114						AT THE TIME OF THE TEST IS STORED IN LOCATION
1115						ERINGE.
1116						
1117						
1118						
1119	023502	010046		ERRID:	MOV R0,-(SP)	SAVE REGISTER R0,R1,R2,R3
1120	023504	010146			MOV R1,-(SP)	
1121	023506	010246			MOV R2,-(SP)	
1122	023510	010346			MOV R3,-(SP)	
1123	023512	017700	155276		MOV @DERR,R0	GET DISK ERROR REG.
1124	023516	010046			MOV R0,-(SP)	SAVE DERR ALSO ON THE STACK
1125	023520	001416			BEO EREXIT+2	EXIT IF TIME OUT ERROR
1126	023522	012703	000020		MOV #16,R3	ESTABLISH LOOP COUNT OF 16
1127	023526	012701	002612		MOV #S10RG,R1	POINT R1 TO SLIDING 1 TBLE
1128	023532	012702	002652		MOV #S00RG,R2	POINT R2 TO SLIDING 0 TBLE
1129	023536	011600		IDLP:	MOV (SP),R0	GET ERROR REGISTER IMAGE
1130	023540	042200			BIC (R2)+,R0	EXTRACT ERROR STATUS BIT
1131	023542	005700			TST R0	IS ERROR BIT SET?
1132	023544	001011			BNE IDERR	FLAG IT IF YES
1133	023546	022101			CHP (R1)+,R1	POINT R1 TO NEXT SLIDING 1 CONSTANT
1134	023550	005303			DEC R3	DECREMENT LOOP CONSTANT
1135	023552	001371			BNE IDLP	REPEAT IF NOT DONE
1136	023554	022616		EREXIT:	CHP (SP)+,(SP)	POP STACK
1137	023556	012603			MOV (SP)+,R3	RESORE REGISTERS
1138	023560	012602			MOV (SP)+,R2	
1139	023562	012601			MOV (SP)+,R1	
1140	023564	012600			MOV (SP)+,R0	









1312	024036	004537	003342		JSR	R5,TSTCTL	GO TO NEXT TEST IF NO ERROR
1313					;		
1314					;		
1315					;		
1316					;		
1317					;		
1318					;		
1319					;		
1320					;		
1321					;		
1322					;		
1323					;		
1324					;		
1325					;		
1326					;		
1327					;		
1328	024042	005004		TN13:	CLR	R4	SUBTEST NUMBER=0
1329	024044	004537	004276		JSR	R5,ROUSET	REQUEST 211
1330	024050	005001			CLR	R1	CLEAR INDEX REGISTER
1331	024052	012705	000016		MOV	#14,R5	ESTABLISH MASTER LOOP COUNT
1332	024056	012700	023610	TN13LP:	MOV	#WRTBLK+6,R0	GET CYL CB ENTRY
1333	024062	005010			CLR	(R0)	CYLINDER=0
1334	024064	016102	002612		MOV	S10RG(R1),R2	GET WORD COUNT (=2 NEXP)
1335	024070	005402			NEG	R2	FORM NEGATIVE VALUE
1336	024072	010240			MOV	R2,-(R0)	SPECIFY WORD COUNT
1337	024074	012740	000000		MOV	#0,-(R0)	BAR=ZERO ADDR. CORE
1338	024100	005040			CLR	-(R0)	DUSH =0
1339	024102	004537	022700		JSR	R5,DXFER	PERFORM SPECIFIED WRITE
1340	024106	005737	001322		TST	R5RFLG	ANY ERRORS?
1341	024112	001004			BNE	TN13EX	EXIT IF YES
1342	024114	005204			INC	R4	INCREMENT SUBTEST NO.
1343	024116	005721			TST	(R1)+	INCREMENT WORD COUNT INDEX
1344	024120	005305			DEC	R5	DECREMENT LOOP COUNT
1345	024122	001355			BNE	TN13LP	REPEAT IF NOT DONE
1346	024124	004537	003342	TN13EX:	JSR	R5,TSTCTL	EXIT
1347					;		
1348					;		
1349					;		
1350					;		
1351					;		
1352					;		
1353					;		
1354					;		
1355					;		
1356					;		
1357					;		
1358					;		
1359					;		
1360					;		
1361					;		
1362					;		
1363					;		
1364					;		
1365	024130	012700	035526	TN14:	MOV	#WRCB+6,R0	GET CYLINDER ENTRY ADDR
1366	024134	004537	004276		JSR	R5,ROUSET	REQUEST 211
1367	024140	013710	001056		MOV	RVCYL,(R0)	SPECIFY CYLINDER ADDRESS
1368	024144	013740	001046		MOV	WPSEC,-(R0)	SPECIFY ONE SECTOR OPERATION

WRITE COUNT TEST

THIS TEST PERFORMS WRITE OPERATIONS WITH AN EVER INCREASING WORD COUNT STARTING WITH 1 AND INCREASING IN POWERS OF 2 TO A MAXIMUM OF 8192 WORDS EACH WRITE OPERATION STARTS A ABSOLUTE 0 DISK ADDRESS.

SUBTEST NUMBER=0  
REQUEST 211

CLEAR INDEX REGISTER  
ESTABLISH MASTER LOOP COUNT

GET CYL CB ENTRY  
CYLINDER=0

GET WORD COUNT (=2 NEXP)  
FORM NEGATIVE VALUE

SPECIFY WORD COUNT  
BAR=ZERO ADDR. CORE

DUSH =0  
PERFORM SPECIFIED WRITE

ANY ERRORS?  
EXIT IF YES

INCREMENT SUBTEST NO.  
INCREMENT WORD COUNT INDEX

DECREMENT LOOP COUNT  
REPEAT IF NOT DONE

EXIT

ONE SECTOR READ,WRITE,COMPARE TEST

THIS TEST WRITES DATA ON ONE SECTOR OF THE DISK, READS IT BACK, AND COMPARES THE DATA OBTAINED WITH THE ORIGINAL DATA WRITTEN.

THE CYLINDER ADDRESS IS SPECIFIED BY RVCYL WHILE THE SECTOR AND HEAD VALUES ARE NORMALLY SUPPLIED BY RVUSH.

OPTIONALLY THE SECTOR AND HEAD DATA MAY BE DYNAMICALLY SUPPLIED FROM THE CONSOLE SWITCH REGISTER IF CSWTCN CONTAINS ANY NON ZERO VALUE.

1369	024150	005740		TST	-(R0)	JSKIP OVER BAR CB ENTRY	
1370	024152	005737	001250	TST	CSWTC	DOES USH DATA COME FROM CSWR?	
1371	024156	001406		BEQ	+14	USE RDUSH DATA IF NO	
1372	024160	013702	177570	MOV	CSWR,R2	GET DESIRED DATA	
1373	024164	042702	100000	BIC	#REPBIT,R2	REMOVE REPEAT BIT IF ON	
1374	024170	010240		MOV	R2,-(R0)	ENTER DUSH VALUE	
1375	024172	000402		BR	+6	CONTINUE	
1376	024174	013740	001054	MOV	RDUSH,-(R0)	PUT MAXIMUM DUSH VALUE IN	
1377	024200	012701	044312	MOV	#DDBUF,R1	GET OUTPUT DATA BUFFER ADDRESS	
1378	024204	004537	016736	JSR	R5,FORMAT	FORMAT BUFFER	
1379	024210	004537	035356	JSR	R5,WRC	PERFORM WRITE,READ AND DATA COMPARISON	
1380	024214	004537	003342	JSR	R5,TSTCTL	GO TO NEXT TEST IF NO ERROR	
1381							
1382							
1383							
1384					READ, WRITE, COMPARE COUNT TEST		
1385							
1386							
1387					THIS TEST PERFORMS WRITE, READ AND DATA COMPARISONS		
1388					WITH AN EVER INCREASING WORD COUNT STARTING WITH ONE AND		
1389					INCREASING BY POWERS OF TWO TO A MAXIMUM OF 512 WORDS.		
1390					EACH DISK OPERATION STARTS AT ABSOLUTE DISH ADDRESS		
1391					ZERO.		
1392					ALL DISK AND DATA PARAMETERS ARE CHECKED DURING THE TEST.		
1393							
1394							
1395							
1396	024220	012701	044312	TN15:	MOV	#DDBUF,R1	GET OUTPUT BUFFER ADDR
1397	024224	004537	004276	JSR	R5,RQUEST	REQUEST 211	
1398	024230	004537	016736	JSR	R5,FORMAT	FORMAT BUFFER	
1399	024234	012705	000011	MOV	#11,R5	ESTABLISH MASTER LOOP	
1400	024240	005001		CLR	R1	CLEAR INDEX REGISTER	
1401	024242	005004		CLR	R4	SUBTEST NUMBER=0	
1402	024244	012700	035526	TN15LP:	MOV	#WRCB+6,R0	GET WRITE/READ CYL ENTRY ADDR
1403	024250	005010		CLR	(R0)	CYLINDER = 0	
1404	024252	016102	002612	MOV	S10RG(R1),R2	GET WORD COUNT =2N (N=EXP)	
1405	024256	005402		NEG	R2	MAKE NEGATIVE	
1406	024260	010240		MOV	R2,-(R0)	PUT IN WORD COUNT ENTRY	
1407	024262	005740		TST	-(R0)	SKIP OVER BAR CB ENTRY	
1408	024264	005040		CLR	-(R0)	DUSH = 0	
1409	024266	004537	035356	JSR	R5,WRC	DO WRITE,READ,DATA COMPARISON	
1410	024272	005737	001322	TST	ERRFLG	ANY ERRORS?	
1411	024276	001004		BNE	T15EX	EXIT IF YES	
1412	024300	005204		INC	R4	INCREMENT SUBTEST COUNT	
1413	024302	005721		TST	(R1)+	INCREMENT WORD COUNT INDEX	
1414	024304	005305		DEC	R5	DECREMENT LOOP COUNT	
1415	024306	001356		BNE	TN15LP	REPEAT IF NOT DONE	
1416	024310	004537	003342	T15EX:	JSR	R5,TSTCTL	EXIT
1417							
1418							
1419							
1420					.ECT		
1421							
1422					WRITE PROTECT TEST		
1423							
1424							
1425					THIS TEST VERIFIES THAT THE CONTROLLER WILL NOT		



1483	024562	001031		BNE	TN16EX	);EXIT IF YES
1484	024564	005204		INC	R4	);SUBTEST NUMBER=4(DATA READ OK)
1485	024566	013700	001050	MOV	POSWP,RO	);SPECIFY 256 WORD COMPARE
1486	024572	004537	017106	JSR	R5,DATCMP	);SEE IF DATA WAS ERRONEOUSLY OVERWRITTEN
1487	024576	005737	001322	TST	ERRFLG	);ANY ERRORS?
1488	024602	001021		BNE	TN16EX	);EXIT IF YES
1489	024604	005204		INC	R4	);SUBTEST NUMBER=5(DATA OK)
1490	024606	005037	044306	CLR	ODBUF-4	);RESTORE NRML HEADER FORMAT
1491	024612	005037	044310	CLR	ODBUF-2	);FOR SECTOR 0
1492	024616	012700	025450	MOV	#ISECFB,RO	);GET FORMAT BLOCK ADDR
1493	024622	005237	001176	INC	SPECMD	);SET SPECIAL TRANSFER COMMAND
1494	024626	004537	022700	JSR	R5,DXFER	);RESTORE ORIGINAL FORMAT TO SECTOR
1495	024632	005037	001176	CLR	SPECMD	);CLEAR SPECIAL TRANSFER FLAG
1496	024636	005737	001322	TST	ERRFLG	);ANY ERRORS?
1497	024642	001001		BNE	TN16EX	);EXIT IF YES
1498	024644	005204		INC	R4	);SUBTEST NUMBER=6(REFORMAT OK)
1499	024646	004537	003342	JSR	R5,TSTCTL	);RETURN
1500						
1501						
1502						
1503					TEST 16	TRANSFER BLOCK
1504						
1505						
1506						
1507	024652	000000		T16WB:	WORD 0	);DUSH =0
1508	024654	044312			WORD ODBUF	);OBAR=ODBUF
1509	024656	177700			WORD 177700	);WORD COUNT LESS THAN ONE SECTOR
1510	024660	000000			WORD 0	);CYLINDER 0
1511	024662	000006			WORD WRTCMD	);WRITE OPERATION
1512		024652			ISECWB=T16WB	
1513						
1514						
1515						
1516						
1517						
1518						
1519						
1520						
1521						
1522						
1523						
1524						
1525					6M•ECC TEST NUMBERS 17>> 21	
1526						
1527						
1528						
1529						
1530						
1531						
1532						
1533						
1534					HEADER OVERRIDE TEST	
1535					*****	
1536						
1537						
1538						
1539						

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1557
1558 024664 005004          TN17: CLR      R4          ;INITIALIZE SUBTEST COUNT
1559 024666 004537 004276   JSR      R5,REQUEST ;REQUEST 211
1560 024672 012701 044306   MOV      #O0BUF-4,R1 ;GET OUTPUT BUFFER ADDRESS
1561 024676 012721 177774   MOV      #177774,(R1)+ ;SET FIRST HEADER TO BE ERRONEOUS
1562 024702 005021          CLR      (R1)+       ;MAKE CYLINDER HEADER WORD VALID
1563 024704 063701 001062   ADD      STRCNT,R1   ;ADJUST BUFFER FOR MCOMPARE
1564 024710 004537 016736   JSR      R5,FORMAT  ;FORMAT OUTPUT BUFFER
1565 024714 012700 025450   MOV      #TN17FB,R0  ;GET FORMAT CONTROL BLOCK ADDRESS
1566 024720 065237 001176   INC      SPECMD      ;SET SPECIAL TRANSFER FLAG
1567 024724 004537 022700   JSR      R5,DXFER    ;WRITE ERRONEOUS HEADER AND DATA
1568 024730 005037 001176   CLR      SPECMD      ;CLEAR SPECIAL TRANSFER FLAG
1569 024734 005737 001322   TST      ERRFLG      ;ANY ERRORS?
1570 024740 001402          BEQ      TN17A       ;CONTINUE IF NO
1571 024742 000137 025416   JMP      TN17EX      ;EXIT IF YES
1572 024746 005204          TN17A: INC      R4          ;SUBTEST NUMBER=1(REFORMAT OK)
1573 024750 012700 025472   MOV      #ISECRB+8,R0 ;GET READ BLOCK ADDR
1574 024754 012710 000004   MOV      #R0CMD,(R0) ;INSURE READ COMMAND PRESENT
1575 024760 005040          CLR      -(R0)       ;CLEAR CYLINDER
1576 024762 013740 001046   MOV      #WPSEC,-(R0) ;SET WORD COUNT TO FULL SECTOR
1577 024766 013701 001234   MOV      #CURDSK,R1  ;GET CURRENT DISK NUMBER
1578 024772 006301          ASL      R1          ;MAKE WORD INDEX
1579 024774 016140 001200   MOV      #IBFTBL(R1),-(R0) ;UCAR=INPUT BUFFER ORIGIN
1580 025000 005040          CLR      -(R0)       ;DUSH=0
1581 025002 004537 022700   JSR      R5,DXFER    ;READ SECTOR WITH BAD HEADER
1582 025006 005737 001322   TST      ERRFLG      ;ANY ERRORS?
1583 025012 001003          BNE      +8          ;CONTINUE IF YES
1584 025014 005237 001322   INC      ERRFLG      ;SET ERROR FLAG IF NO ERROR DETECTED
1585 025020 000576          BR       TN17EX      ;EXIT IF NO ERROR FOUND
1586 025022 017703 153766   MOV      #DERR,R3    ;LOAD ERROR REGISTER
1587 025026 012702 000002   MOV      #2,R2       ;LOAD REFERENCE ERROR WORD
1588 025032 020203          CMP      R2,R3       ;IS THE DERR RIGHT?
1589 025034 001170          BNE      TN17EX      ;EXIT IF NO
1590 025036 005204          INC      R4          ;SUBTEST NUMBER=2(ERROR READ OK)
1591 025040 005037 001322   CLR      ERRFLG      ;RESET ERROR FLAG
1592 025044 012737 000016 025472 MOV      #RVHCHD,ISECRB+8 ;SPECIFY READ WITHOUT HEADER CHECK
1593 025052 012700 025462   MOV      #ISECRB,R0  ;GET READ BLOCK ADDR.
1594 025056 004537 022700   JSR      R5,DXFER    ;READ IGNORING HEADER WORD
1595 025062 005737 001322   TST      ERRFLG      ;ANY ERRORS?
1596 025066 001153          BNE      TN17EX      ;EXIT IF YES

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1654	025342	016001	000004	MOV	4(R0),R1	SET UP FOR DATA COMPARE
1655	025346	010100		MOV	R1,RO	
1656	025350	005400		NEG	RO	
1657	025352	004537	017106	JSR	R5,DATCHP	CHEACL DATA WORDS
1658	025356	005737	001322	TST	ERRFLG	ERRORS?
1659	025362	001015		BNE	TN17EX	EXIT IF YES
1660	025364	005204		INC	R4	SUBTEST NUMBER=10(DATA OK)
1661	025366	012700	025450	MOV	#ISECFB,RO	REFORMAT SECTOR
1662	025372	005037	044306	CLR	ODBUF-4	RESTORE SECTOR
1663	025376	005037	044310	CLR	ODBUF-2	
1664	025402	005237	001176	INC	SPECMD	FLAG ODD TRANSFER
1665	025406	004537	022700	JSR	R5,DXFER	RESTORE SECTOR 0
1666	025412	005037	001176	CLR	SPECMD	CLEAR TRANSFER FLAG
1667	025416	012737	044306	MOV	#ODBUF-4,WHSCCB+2	RELOAD TRANSFER ADDR.
1668	025424	012737	000004	MOV	#RDCHD,ISECRB+8	RELOAD READ COMMAND
1669	025432	004537	003342	JSR	R5,TSTCTL	AND EXIT
1670				EOT		
1671						
1672						
1673						
1674						
1675						
1676						
1677						READ HEADER,HEADER CRC,DATA,DATA CRC BLOCK
1678						*****
1679						
1680						
1681	025436	000000		RDHDBK:	WORD 0	TRANSFER AT SECTOR,HEAD 0
1682	025440	044312			WORD ODBUF	OUTPUT BUFFER
1683	025442	177400			WORD 177400	WORD COUNT VARIABLE
1684	025444	000000			WORD 0	CYLINDER ADDRESS= 0
1685	025446	000012			WORD 12	READ EVERYTHING COMMAND
1686						
1687						
1688						
1689						
1690						TEST 17 FORMAT CONTROL BLOCK
1691						
1692						
1693						
1694	025450	000000		TN17FB:	WORD 0	DUSH=0
1695	025452	044306			WORD ODBUF-4	DBAR=OUTPUT BUFFER
1696	025454	177700			WORD 177700	WORD COUNT LESS ONE SECTORH
1697	025456	000000			WORD 0	CYLINDER =0
1698	025460	000010			WORD FMTCHD	FORMAT OPERATION
1699						
1700						
1701						
1702		025450			ISECFB=TN17FB	
1703						
1704						
1705						
1706						TEST 17 READ CONTROL BLOCK
1707						
1708						
1709						
1710	025462	000000		TN17RB:	WORD 0	DUSH =0



1	1768	025550	001161		BNE	\$TNZ0				);EXIT IF YES
2	1769	025552	005204		INC	R4				);SUBTEST NUMBER=1(WRITE PROTECT WRITE OK )
3	1770	025554	013700	001050	MOV	POSVP,R0				);ONE SECTOR WORD COUNT
4	1771	025560	012701	044312	MOV	#0DBUF,R1				);GET REFERENCE BUFFER ORIGIN
5	1772	025564	005421		NEG	(R1)+				);COMPLEMENT REFERENCE DATA
6	1773	025566	005300		DEC	R0				);DECREMENT WORD COUNT
7	1774	025570	001375		BNE	0-4				);CONTINUE IF NOT ZERO
8	1775	025572	012700	026336	MOV	#WPORCB,R0				);GET OVERRIDE CB ADDRESS
9	1776	025576	013760	001046	MOV	WPSEC,4(RU)	000004			);LOAD ONE SECTOR WORD COUNT
10	1777	025604	004537	022700	JSR	R5,DXFER				);WRITE OVER PROTECTED DATA
11	1778	025610	005737	001322	TST	ERRFLG				);ANY ERRORS?
12	1779	025614	001137		BNE	\$TNZ0				);EXIT IF ERROR
13	1780	025616	005204		INC	R4				);SUBTEST NUMBER=2(OVERRIDE OK 0
14	1781	025620	012700	023622	MOV	#ROBLK+6,R0				);GET CYLINDER ENTRY CB ADDRESS
15	1782	025624	005010		CLR	(R0)				);CYLINDER=0
16	1783	025626	013740	001046	MOV	WPSEC,-(R0)				);ONE SECTOR WORD COUNT
17	1784	025632	013701	001234	MOV	CURDSK,R1				);GET CURRENT DISK DRIVE
18	1785	025636	006301		ASL	R1				);MAKE INDEX WORD
19	1786	025640	016140	001200	MOV	IBFTBL(R1),-(R0)				);SPECIFY INPUT BUFFER ADDRESS
20	1787	025644	005040		CLR	-(R0)				);SECTOR,HEAD=0
21	1788	025646	004537	022700	JSR	R5,DXFER				);READ DATA FROM SECTGR
22	1789	025652	005737	001322	TST	ERRFLG				);ANY ERRORS?
23	1790	025656	001116		BNE	\$TNZ0				);EXIT IF ERROR
24	1791	025660	005204		INC	R4				);SUBTEST NUMBER =3
25	1792	025662	013700	001050	MOV	POSVP,R0				);ONE SECTOR COMPARE COUNT
26	1793	025666	004537	017106	JSR	R5,DATCHP				);COMPARE DATA
27	1794	025672	005737	001322	TST	ERRFLG				);ANY ERRORS?
28	1795	025676	001106		BNE	\$TNZ0				);EXIT IF ERROR
29	1796	025700	005204		INC	R4				);SUBTEST NUMBER=4(DATA OVERRIDE OK)
30	1797	025702	005037	044306	CLR	0DBUF-4				);REFORMAT SECTOR WITH NO WRITE PROTECT
31	1798	025706	005037	044310	CLR	0DBUF-2				);
32	1799	025712	012700	025450	MOV	#ISECFB,R0				);GET ORIGIN ADDRESS OF FORMAT BLOCK
33	1800	025716	005237	001176	INC	SPECMD				);SET SPECIAL TRANSFER FLAG
34	1801	025722	004537	022700	JSR	R5,DXFER				);REFORMAT SECTOR
35	1802	025726	005037	001176	CLR	SPECMD				);RESET SPECIAL TRANSFER FLAG
36	1803	025732	005737	001322	TST	ERRFLG				);ERROT?
37	1804	025736	001066		BNE	\$TNZ0				);EXIT IF ERROR
38	1805	025740	012704	000005	MOV	#5,R4				);SUBTEST NUMBER=5(REFORMAT OK)
39	1806									); THE SUBTEST NUMBER IS FORCED
40	1807									); HERE BECAUSE THIS SECTION IS
41	1808									);USED BY ECC CONTROLLERS
42	1809									);
43	1810	025744	012701	044312	MOV	#0DBUF,R1				);POINT TO DATA BUFFER
44	1811	025750	004537	016736	JSR	R5,FORMAT				);FORMAT DATA BUFFER
45	1812	025754	013702	001050	MOV	POSVP,R2				);COMPUTE LAST SECTOR WORD ADDR
46	1813	025760	006302		ASL	R2				);
47	1814	025762	062702	044312	ADD	#0DBUF,R2				);
48	1815	025766	012742	177777	MOV	#-1,(R2)				);MAKE LAST WORD ALL ONES
49	1816	025772	012737	177777	MOV	#-1,0DBUF	044312			);MAKE FORST WORD ALL ONES
50	1817	026000	012700	023610	MOV	#WRTBLK+6,R0				);POINT TO WRITE BLOCK ADDRESS
51	1818	026004	013710	001056	MOV	RWCY,(R0)				);SPECIFY CYLINDER
52	1819	026010	013740	001046	MOV	WPSEC,-(R0)				);ONE SECTOR WORD COUNT
53	1820	026014	012740	044312	MOV	#0DBUF,-(R0)				);BUFF ADDRESS
54	1821	026020	013740	001054	MOV	R0USH,-(R0)				);DUSH ADDRESS
55	1822	026024	004537	022700	JSR	R5,DXFER				);ISSUE WRITE OPERATION
56	1823	026030	005737	001322	TST	ERRFLG				);ERROR SET?
57	1824	026034	001133		BNE	TN20EX				);EXIT IF YES

1	1825	026036	005204		INC	R4		;SUBTEST NUMBER=6(FIRST WRITE OK)
2	1826	026040	012737	000026	MOV	#WRCHK,WRBLK+8	023612	;LOAD WRITE CHECK COMMAND IN WRITE BLOCK
3	1827	026046	012700	023602	MOV	#WRBLK,R0		;SET UP TO WRITE CHECK
4	1828	026052	004537	022700	JSR	R5,DXFER		;GO WRITE CHECK
5	1829	026056	005737	001322	TST	ERRFLG		;ERROR SET?
6	1830	026062	001120		BNE	TN2OEX		;EXIT IF YES
7	1831	026064	005204		INC	R4		;SUBTEST NUMBER=7(WRITE CHECK OK)
8	1832	026066	005337	044312	DEC	ODBUF		;CHANGE DATA BUFFER (FIRST BIT ONLY)
9	1833							;TO CAUSE WRITE CHECK ERROR
10	1834	026072	012700	023602	MOV	#WRBLK,R0		;SET UP FOR SECOND WRITE CHECK COMMAND
11	1835	026076	004537	022700	JSR	R5,DXFER		;GO WRITE CHECK
12	1836	026102	005737	001322	TST	ERRFLG		;ERROR FLAG SET?
13	1837	026106	001004		BNE	\$TN20A		;CONTINUE IF YES
14	1838	026110	005237	001322	INC	ERRFLG		;SET IT IF NOT
15	1839	026114	000137	026324	JMP	TN2OEX		;AND EXIT
16	1840	026120	005204		INC	R4		;SUBTEST NUMBER=10(ERROR DETECTED)
17	1841	026122	017703	152666	MOV	@DERR,R3		;GET ERROR REG.
18	1842	026126	042703	137777	BIC	#137777,R3		;EXTRACT WRITE CHECK ERROR
19	1843	026132	013702	001302	MOV	SEKINB,R2		;SET UP REFERENCE
20	1844	026136	020203		CMP	R2,R3		;WRITE CHECK ERROR SET?
21	1845	026140	001071		BNE	TN2OEX		;EXIT IF NOT
22	1846	026142	005204		INC	R4		;SUBTEST NUMBER=11(WRITE CHECK ERROR SET)
23	1847	026144	017703	152644	MOV	@DERR,R3		;FETCH ERROR REG AGAIN
24	1848	026150	043703	001302	BIC	SEKINB,R3		;MASK OUT WRITE CHECK ERROR
25	1849	026154	005002		CLR	R2		;SET UP REFERENCE WORD
26	1850	026156	020203		CMP	R2,R3		;ANY OTHER ERRORS SET?
27	1851	026160	001061		BNE	TN2OEX		;EXIT IF YES
28	1852	026162	005204		INC	R4		;SUBTEST NUMBER=12(NO OTHER ERRORS SET)
29	1853	026164	005237	044312	INC	ODBUF		;RESTORE FIRST DATA BIT
30	1854	026170	013702	001050	MOV	POSWP,R2		;COMPUTE LAST CORE WORD LOCATION
31	1855	026174	006302		ASL	R2		
32	1856	026176	062702	044312	ADD	#ODBUF,R2		
33	1857	026202	042742	100000	BIC	#BIT15,-(R2)		;REMOVE LAST BIT OF DATA
34	1858	026206	005037	001322	CLR	ERRFLG		;RESET ERROR FLAG
35	1859	026212	012700	023602	MOV	#WRBLK,R0		;SET UP FOR WRITE CHECK
36	1860	026216	004537	022700	JSR	R5,DXFER		;GO WRITE CHECK!!!!!!!!!!!!!!
37	1861	026222	005737	001322	TST	ERRFLG		;ERROR SET?
38	1862	026226	001003		BNE	\$TN20B		;CONTINUE IF YES
39	1863	026230	005237	001322	INC	ERRFLG		;SET ERROR FLAG
40	1864	026234	000433		BR	TN2OEX		;AND EXIT
41	1865	026236	005204		INC	R4		;SUBTEST NUMBER=13(SECOND ERROR GENERATED)
42	1866	026240	017703	152550	MOV	@DERR,R3		;FETCH ERROR REGISTER
43	1867	026244	013702	001302	MOV	SEKINB,R2		;SET UP REFERENCE WORD
44	1868	026250	030203		BIT	R2,R3		;WRITE CHECK ERROR SET?
45	1869	026252	001424		BEQ	TN2OEX		;EXIT IF NO
46	1870	026254	005204		INC	R4		;SUBTEST NUMBER=14(WRITE CHECK ERROR)
47	1871	026256	005037	001322	CLR	ERRFLG		;RESET ERROR FLAG
48	1872	026262	012701	044312	MOV	#ODBUF,R1		;ENTER BUFFER LOCATION FOR FORMAT
49	1873	026266	013702	001050	MOV	POSWP,R2		;RECOMPUTE LAST DATA WORD LOCATION
50	1874	026272	006302		ASL	R2		
51	1875	026274	062702	044312	ADD	#ODBUF,R2		
52	1876	026300	012742	177777	MOV	#-1,-(R2)		;RESTORE LAST DATA WORD
53	1877	026304	012700	023602	MOV	#WRBLK,R0		;POINT TO COMMAND BLOCK
54	1878	026310	004537	022700	JSR	R5,DXFER		;CHECK COMMAND AGAIN
55	1879	026314	005737	001322	TST	ERRFLG		;ERROR FLAG SET?
56	1880	026320	001001		BNE	TN2OEX		;EXIT IF YES
57	1881	026322	005204		INC	R4		;SUBTEST NUMBER=17(WRITE CHECK OK)

1	1882	026324	012737	000006	023612	TN20EX:	MOV	#WRTCMD, WRTBLK+8,	RESTORE WRITE COMMAND
2	1883	026332	004537	003342			JSR	R5, TSTCTL	EXIT TO TEST CONTROL
3	1884								
4	1885								
5	1886								
6	1887								
7	1888								
8	1889								
9	1890								
10	1891								
11	1892								TEST 20 WRITE PROTECT CONTROL BLOCK
12	1893								
13	1894	026336	000000			WPORCB:	WORD 0	SECTOR, HEAD ADDR=0,0	
14	1895	026340	044312				WORD 0DBUF	DBAR=0DBUF	
15	1896	026342	177400				WORD 177400	WORD COUNT =ONE SECTOR	
16	1897	026344	000000				WORD 0	CYLINDER ADDR=0	
17	1898	026346	000020				WORD WORCMD	WRITE OVERRIDE COMMAND	
18	1899							CDC6.P11	15-FEB-77
19	1900								
20	1901								
21	1902								
22	1903								
23	1904								
24	1905								
25	1906								
26	1907								HEADER WRITE COMMAND TEST
27	1908								
28	1909								
29	1910								THIS TEST VERIFIES THAT THE HEADER CAN BE WRITTEN
30	1911								BY THE WRITE HEADER AND DATA COMMAND,(CRC).
31	1912								THE HEADER IS WRITTEN TO AN ERRONEOUS VALUE
32	1913								USING THE COMMAND AND, THEN A NORMAL READ IS
33	1914								ATTEMPTED AND THE PRESENCE OF THE APPROPRIATE
34	1915								HEADER ERROR BIT(S) IS(CARE) CHECKED.
35	1916								
36	1917								
37	1918								
38	1919								
39	1920	026350	005004			TN21:	CLR	R4	INITIALIZE SUSTEST NUMBER
40	1921	026352	004537	004276			JSR	R5, RQUEST	REQUEST 211
41	1922	026356	012701	044306			MOV	#0DBUF-4, R1	GET DATA BUFFER ORIGIN ADDRESS
42	1923	026362	013702	001040			MOV	#MAXSEC, R2	GENERATE ERRONEOUS HEADER
43	1924	026366	005202				INC	R2	
44	1925	026370	010221				MOV	R2, (R1)+	LOAD INTO BUFFER
45	1926	026372	005021				CLR	(R1)+	MAKE CYLINDER HEADER VALID
46	1927	026374	004537	016736			JSR	R5, FORMAT	FORMAT DATA BUFFER
47	1928	026400	012700	027156			MOV	#VHSCCB, R0	GETWRITE SECTOR, HEAD, CRC, CB
48	1929	026404	013760	001046	000004		MOV	#PSEC, 4(R0)	INCLUDE HEADR/CRC IN FORMAT
49	1930	026412	162760	000004	000004		SUB	#4, 4(R0)	
50	1931	026420	005237	001176			INC	SPECMD	SET SPECIAL TRANSFER FLAG
51	1932	026424	004537	022700			JSR	R5, D,XFER	PERFORM SPECIAL WRITE OPERATION
52	1933	026430	005037	001176			CLR	SPECMD	CLEAR SPECIAL TRANSFER FLAG
53	1934	026434	005737	001322			TST	ERRFLG	ANY ERRORS?
54	1935	026440	001076				BNE	TN21A	EXIT IF YES
55	1936	026442	005204				INC	R4	SUBTEST NUMBER=1(WRITE FUNCTION OK)
56	1937	026444	012700	023622			MOV	#R0BLK+6, R0	GET CYLINDER ENTRY CB ADDRESS
57	1938	026450	005010				CLR	(R0)	CYLINDER=0

6	1939	026452	013740	001046	MOV	WPSEC,-(R0)	ONE SECTOR WORD COUNT
7	1940	026456	013701	001234	MOV	CURDSK,R1	GET CURRENT DISK
8	1941	026462	006301		ASL	R1	MAKE VALID INDEX
9	1942	026464	016140	001200	MOV	IBFTBL(R1),-(R0)	SPECIFY INPUT BUFFER ADDRESS
10	1943	026470	005040		CLR	-(R0)	SECTOR,HEAD=0
11	1944	026472	004537	022700	JSR	R5,DXFER	ATTEMPT TO READ SECTOR ZERO
12	1945	026476	005737	001322	TST	ERRFLG	ANY ERRORS?
13	1946	026502	001004		BNE	+10	CONTINUE IF YES
14	1947	026504	005237	001322	INC	ERRFLG	SET ERROR FLAG
15	1948	026510	000137	027152	JMP	TN21EX	EXIT TO TEST CONTROL
16	1949	026514	017703	152274	MOV	SDERR,R3	GET ERROR REGISTER
17	1950	026520	042703	077774	BIC	#77774,R3	EXTRACT HEADER ERROR BITS
18	1951	026524	012702	000002	MOV	#2,R2	SET UP REFERENCE ERROR WORD
19	1952	026530	020203		CMP	R2,R3	ARE THE ERROR BITS CORRECT
20	1953	026532	001041		BNE	TN21A	EXIT IF NO
21	1954	026534	005204		INC	R4	SUBTEST NUMBER=2(ERROR READ OK)
22	1955	026536	017703	152242	MOV	SDCAR,R3	GET CORE ADDRESS REGISTER
23	1956	026542	013702	023616	MOV	RDBLK+2,R2	GET ORIGINAL ORIGIN ADDRESS
24	1957	026546	020203		CMP	R2,R3	ARE THEY EQUAL
25	1958	026550	001032		BNE	TN21A	EXIT IF NOT
26	1959	026552	005204		INC	R4	SUBTEST NUMBER=3(NO DBAR INCREMENTATION)
27	1960	026554	017703	152226	MOV	SDWCNT,R3	GET WORD COUNT REGISTER
28	1961	026560	013702	023620	MOV	RDBLK+4,R2	GET ORIGINAL WORD COUNT
29	1962	026564	020203		CMP	R2,R3	ARE THEY EQUAL?
30	1963	026566	001171		BNE	TN21EX	EXIT IF NO
31	1964	026570	005037	001322	CLR	ERRFLG	RESET ERROR FLAG
32	1965	026574	005204		INC	R4	SUBTEST NUMBER=4(NO WORD COUNT INCREMENTATION)
33	1966	026576	013702	001042	MOV	MAXHD,R2	NOW GENERATE HEADER USING
34	1967						BAD HEAD ADDRESS
35	1968	026602	062702	000200	ADD	#HDINC,R2	
36	1969	026606	010257	044306	MOV	R2,ODBUF-4	LOAD INTO BUFFER
37	1970	026612	012700	027156	MOV	#WHSCCB,R0	POINT TO WRITE BLOCK
38	1971	026616	005237	001176	INC	SPECMD	SET SPECIAL COMMAND FLAG
39	1972	026622	004537	022700	JSR	R5,DXFER	REFORMAT SECTOR
40	1973	026626	005037	001176	CLR	SPECMD	RESET SPECIAL COMMAND FLAG
41	1974	026632	005737	001322	TST	ERRFLG	ERROR FLAG SET?
42	1975	026636	001145		TN21A: BNE	TN21EX	EXIT IF ERROR SET
43	1976	026640	005204		INC	R4	SUBTEST NUMBER=5(SECOND FORMAT OK)
44	1977	026642	012700	023622	MOV	#RDBLK+6,R0	POINT TO READ BLOCK ADDRESS
45	1978	026646	005010		CLR	(R0)	CLEAR CYLINDER VALUE
46	1979	026650	013740	001046	MOV	WPSEC,-(R0)	ENTER WORD COUNT (ONE SECTOR)
47	1980	026654	013701	001234	MOV	CURDSK,R1	SET UP PROPER BUFFER ADDR.
48	1981	026660	006301		ASL	R1	
49	1982	026662	016140	001200	MOV	IBFTBL(R1),-(R0)	ENTER INTO READ BLOCK
50	1983	026666	005040		CLR	-(R0)	READ SECTOR,HEAD 0
51	1984	026670	004537	022700	JSR	R5,DXFER	EXECUTE READ
52	1985	026674	005737	001322	TST	ERRFLG	ERROR FLAG SET?*
53	1986	026700	001003		BNE	+8	CONTINUE IF YES
54	1987	026702	005237	001322	INC	ERRFLG	SET IT IF NO
55	1988	026706	000521		BR	TN21EX	AND EXIT
56	1989	026710	005204		INC	R4	SUBTEST NUMBER=6(AN ERROR IS DETECTED)*
57	1990	026712	017703	152076	MOV	SDERR,R3	FETCH ERROR REG.
58	1991	026716	042703	177775	BIC	#177775,R3	EXTRACT SECTOR HEADER ERROR
59	1992	026722	012702	000002	MOV	#2,R2	SET UP REFERENCE ERROR WORD
60	1993	026726	020203		CMP	R2,R3	DETECTED?
61	1994	026730	001110		BNE	TN21EX	EXIT IF NOT DETECTED
62	1995	026732	005204		INC	R4	SUBTEST NUMBER=7(HEAD HEADER DETECTED)

1	1996	026734	017703	152054	MOV	0DERR,R3	ERROR REG AGAIN
2	1997	026740	005002		CLR	R2	SET UP REFERENCE WORD
3	1998	026742	042703	000002	BIC	R2,R3	MASK OUT HEADER ERROR
4	1999	026746	020203		CMF	R2,R3	ANY OTHER ERRORS DETECTED?
5	2000	026750	001100		BNE	TN21EX	EXIT IF YES
6	2001	026752	005204		INC	R4	SUBTEST NUMBER=10(NO OTHER ERRORS DETECTED)
7	2002	026754	005037	001322	CLR	ERRFLG	RESET ERROR FLAG
8	2003	026760	005037	044306	CLR	ODBUF-4	MAKE FIRST HEADER VALID
9	2004	026764	013702	001044	MOV	MAXCYL,R2	CONFIGURE ILLEGAL CYLINDER WORD
10	2005	026770	005202		INC	R2	
11	2006	026772	010237	044310	MOV	R2,ODBUF-2	LOAD ILLEGAL CYLINDER WORD
12	2007	026776	012700	027156	MOV	WHSCCB,R0	WRITE NEW FORMAT ONTO DISK
13	2008	027002	005237	001176	INC	SPECMD	SET SPECIAL TRANSFER FLAG
14	2009	027006	004537	022700	JSR	R5,DXFER	
15	2010	027012	005037	001176	CLR	SPECMD	CLEAR SPECIAL TRANSFER FLAG
16	2011	027016	005737	001322	TST	ERRFLG	ERROR FLAG SET?
17	2012	027022	001053		BNE	TN21EX	EXIT IF YES
18	2013	027024	005204		INC	R4	SUBTEST NUMBER=11(REFORMAT CYL HDR OK)
19	2014	027026	012700	023622	MOV	RDBLK+6,R0	GET WRITE BLOCK ADDRESS
20	2015	027032	005010		CLR	(R0)	CLEAR CYLINDER VALUE
21	2016	027034	013740	001046	MOV	WPSEC,-(R0)	WORD COUNT=ONE SECTOR
22	2017	027040	013701	001234	MOV	CURDSK,R1	GET CURRENT DISK DRIVE
23	2018	027044	006301		ASL	R1	MAKE VALID INDEX
24	2019	027046	016140	001200	MOV	IBFTBL(R1),-(R0)	GET OUTPUT BUFFER ADDRESS
25	2020	027052	005040		CLR	-(R0)	SECTOR,HEAD = 0
26	2021	027054	004537	022700	JSR	R5,DXFER	READ SECTOR
27	2022	027060	005737	001322	TST	ERRFLG	ERROR FLAG SET?
28	2023	027064	001003		BNE	+8.	CONTINUE IF YES
29	2024	027066	005237	001322	INC	ERRFLG	SET ERRGR FLAG IF NO
30	2025	027072	000427		BR	TN21EX	AND EXIT TO TEST CONTROL
31	2026	027074	017703	151714	MOV	0DERR,R3	GET ERROR REGISTER
32	2027	027100	042703	177776	BIC	#177776,R3	EXTRACT CYLINDER ERROR BIT
33	2028	027104	012702	000001	MOV	#1,R2	SET UP REFERENCE ERROR
34	2029	027110	020203		CMF	R2,R3	ARE THEY EQUAL?
35	2030	027112	001017		BNE	TN21EX	EXIT IF NO
36	2031	027114	005037	001322	CLR	ERRFLG	CLEAR ERROR FLAG IF YES
37	2032	027120	005204		INC	R4	SUBTEST NUMBER=12(CYL HDR ERROR DETECTED)
38	2033	027122	005037	044310	CLR	ODRUF-2	SET UP CYLINDER HEADER WORD
39	2034	027126	005237	001176	INC	SPECMD	SET SPECIAL TRANSFER FLAG
40	2035	027132	005037	044306	CLR	ODBUF-4	SET UP SECTOR HEAD HEADER WORD
41	2036	027136	012700	025450	MOV	#ISECFB,R0	GET FORMAT BLOCK ORIGIN
42	2037	027142	004537	022700	JSR	R5,DXFER	REWRITE HEADERS
43	2038	027146	005037	001176	CLR	SPECMD	CLEAR SPECIAL TRANSFER FLAG
44	2039	027152	004537	003342	IN21EX JSR	R5,TSTCTL	EXIT TO TEST CONTROL
45	2040						
46	2041						
47	2042						
48	2043						
49	2044						
50	2045						TN21 WRITE HEADER,DATA,SECTOR,CONTROL BLOCK
51	2046						
52	2047						
53	2048	027156	000000		WHSCCB:	WORD 0	DUSH=0
54	2049	027160	044306			WORD 0DBUF-4	DCAR=ODBUF-4
55	2050	027162	177374			WORD 177374	WORD COUNT = ONE SECTOR +4 WORDS
56	2051	027164	000000			WORD 0	CYLINDER 0
57	2052	027166	000014			WORD WHSCRC	WRITE HEADER,SECTOR,CRC COMMAND





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31 027170 005004          TN22: CLR      R4          ;SUBTEST NUMBER=0
32 027172 004537 004276   JSR      R5,REQUEST ;REQUEST 211
33 027176 012701 044312   MOV      #0DBUF,R1  ;LOAD BUFFER ADDRESS
34 027202 004537 016736   JSR      R5,FORMAT  ;FORMAT DATA
35 027206 005037 044306   CLR      0DBUF-4    ;MAKE HEADERS VALID
36 027212 005037 044310   CLR      0DBUF-2    ;
37 027216 005037 044312   CLR      0DBUF      ;CLEAR WORD FOR HEADER CRC CHECK
38 027222 005237 001176   INC      SPECMD     ;SET SPECIAL COMMAND FLAG
39 027226 012700 027156   MOV      #VHSCCB,R0 ;GET TRANSFER BLOCK ADDRESS
40 027232 013760 001046   MOV      WPSEC,4(R0);LOAD WORD COUNT
41 027240 162760 000004 000004 SUB      #4,4(R0)   ;MODIFY FOR HEADERS/CRC
42 027246 004537 022700   JSR      R5,DXFER   ;GO WRITE BAD CRC CHECK
43 027252 005037 001176   CLR      SPECMD    ;CLEAR SPECIAL COMMAND FLAG
44 027256 005737 001322   TST     ERRFLG     ;ANY ERRORS?
45 027262 001067          BNE     TN22A      ;EXIT IF YES
46 027264 005204          INC     R4         ;SUBTEST NUMBER=1(DATA CRC ERRONEOUSLY WRITTEN)
47 027266 012737 000004 025472 MOV      #R0CMD,ISECRB*8. ;PUT READ COMMAND INTO TRANSFER BLK
48 027274 012700 025462   MOV      #ISECRB,R0 ;POINT TO READ BLOCK
49 027300 013760 001046 000004 MOV      WPSEC,4(R0);LOAD WORD COUNT -ONE SECTOR
50 027306 004537 022700   JSR      R5,DXFER   ;GO READ
51 027312 005737 001322   TST     ERRFLG     ;ERROR?
52 027316 001451          BEQ     TN22A      ;EXIT IF NO
53 027320 005204          INC     R4         ;SUBTEST NUMBER=2(ERROR OCCURRED)
54 027322 017703 151466   MOV      #DERR,R3  ;GET ERROR REGISTER
55 027326 042703 177377   BIC     #177377,R3 ;EXTRACT CRC ERROR
56 027332 012702 000400   MOV      #A00,R2   ;SET UP REFERENCE WORD
57 027336 020203          CMP     R2,R3      ;ARE THEY EQUAL?
    
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7M.ECC TEST NUMBERS 22 >> 25 13-NOV-77

CRC AND HEADER COMPARE TESTS

THESE TESTS CHECK THE LOGIC GOVERNING THE DETECTION OF HEADER AND CRC ERRORS.USING THEWRITE HEADER DATA AND CRC COMMAND,ERRONEOUS HEADERS AND CRC CHECKS ARE WRITTEN IN VARIOUS COMBINATIONS.CHECKS ARE THEN MADE FOR PROPER ERROR BIT SETTINGS.





1	172	030116	005037	001322	CLR	ERRFLG	;	RESET ERROR FLAG
2	173	030122	020203		CMP	R2,R3	;	ANY OTHER ERRORS?
3	174	030124	001012		BNE	TN22EX	;	EXIT IF YES
4	175	030126	005237	001176	INC	SPECMD	;	SET SPECMD FLAG
5	176	030132	012700	025450	MOV	#ISFCFB,R0	;	GET FORMAT BLOCK ADDRESS
6	177	030136	004537	022700	JSR	R5,DXFER	;	GO WRIT HEADERS
7	178	030142	005037	001176	CLR	SPECMD	;	CLEAR SPECIAL COMMAND FLAG
8	179	030146	004537	003342	JSR	R5,TSTCTL	;	RETURN TO TEST CONTROL
9	180	030152	005237	001322	TN22EX: INC	ERRFLG	;	SET ERROR FLAG
10	181	030156	000773		BR	.-8.	;	AND RETURN
11	182							
12	183							
13	184							
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31	202							
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33	204							
34	205							
35	206							
36	207							
37	208							
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39	210							
40	211							
41	212							
42	213							
43	214							
44	215							
45	216							
46	217							
47	218							
48	219							
49	220							
50	221							
51	222	030160	005004		TN23: CLR	R4	;	SUBTEST NUMBER=0
52	223	030162	004537	004276	JSR	R5,REQUEST	;	REQUEST 211
53	224	030166	005037	044306	CLR	ODBUF-4	;	MAKE FIRST HEADER VALID
54	225	030172	013737	001276	MOV	BADBIT,ODBUF-2	;	ADD BAD SECTOR ID BITS
55	226	030200	012700	025450	MOV	#ISFCFB,R0	;	GET FORMAT BLOCK ADDRESS
56	227	030204	013760	001046	MOV	WPSEC,4(R0)	;	ADJUST WORD COUNT
57	228	030212	005237	001176	INC	SPECMD	;	FLAG SPECIAL TRANSFER

BAD SECTOR FLAG TESTS

TN23

THIS TEST CHECKS THE BAD SECTOR LOGIC.  
 BAD SECTOR BITS ARE ADDED TO HEADER WORD #1  
 OF SECTOR 0, HEAD 0, TRACK 0 AND A READCOMMAND  
 IS ISSUED. THE FIRST CHECK IS TO SEE IF THE BAD  
 SECTOR BIT IS SET IN THE ERROR REGISTER (DERR)  
 THE DATA IS THEN COMPARED WITH DATA  
 PREVIOUSLY WRITTEN ON SECTOR ONE TO  
 INSURE THAT THE READ TOOK PLACE FROM SECTOR ONE  
 NOT SECTOR ZERO.

229	030216	004537	022700	JSR	R5,DXFER	GO REFORMAT DATA
230	030222	005037	001176	CLR	SPECHD	CLEAR SPECIAL TRANSFER FLAG
231	030226	005737	001322	TST	ERRFLG	ANY ERRORS ON FORMATTING?
232	030232	001027		BNE	TN23A	EXIT IF YES
233	030234	005204		INC	R4	SUBTEST NUMBER=1(REFORMAT OK)
234	030236	012737	000001 024652	MOV	#1,ISECVB	MAKE DUSH =SECTOR ONE
235	030244	013701	001046	MOV	WPSEC,R1	GET WORD COUNT
236	030250	012702	044312	MOV	#00BUF,R2	POINT R2 TO OUTPUT AREA
237	030254	012722	125252	MOV	#125252,(R2)+	FORMAT DATA
238	030260	005201		INC	R1	INCREMENT(DECREMENT) LOOP COUNT
239	030262	001374		BNE	*-6	REPEAT IF NOT DONE
240	030264	012737	044312 024654	MOV	#00BUF,ISECVB+2	LOAD OUTPUT BUFFER
241	030272	012700	024652	MOV	#ISECVB,R0	GET ONE SECTOR WRITE BLOCK ORIGIN
242	030276	004537	022700	JSR	R5,DXFER	GO WRITE KNOWN DATA
243	030302	005037	024652	CLR	ISECVB	REMOVE SECTOR #1 ADDRESS
244	030306	005737	001322	TST	ERRFLG	ERRORS?
245	030312	001104		TN23A: BNE	TN23EX	EXIT IF YES
246	030314	005204		INC	R4	SUBTEST NUMBER=2(WRITE ONE SECTOR ONE OK)
247	030316	012700	025462	MOV	#ISECRB,R0	GET ONE SECTOR READ BLOCK
248	030322	005020		CLR	(R0)+	MAKE DUSH =0
249	030324	013702	001234	MOV	CURDSK,R2	GET CURRENT DISK NUMBER
250	030330	006302		ASL	R2	MAKE VALID INDEX
251	030332	016210	001200	MOV	IBFTBL(R2),(R0)	ENTER PROPER BUFFER ADDRESS
252	030336	005740		TST	-(R0)	RELOCATE POINTER
253	030340	004537	022700	JSR	R5,DXFER	GO ATTEMPT A READ ON SECTOR 0
254	030344	005737	001322	TST	ERRFLG	ERROR?
255	030350	001003		BNE	*+8*	CONTINUE IF NO
256	030352	005237	001322	INC	ERRFLG	SET ERROR FLAG IF NO
257	030356	000462		BR	TN23EX	EXIT
258	030360	005204		INC	R4	SUBTEST NUMBER=3(ERROR OCCURRED)
259	030362	017703	150426	MOV	#DERR,R3	GET ERROR REGISTER
260	030366	042703	157777	BIC	#157777,R3	EXTRACT ERROR BIT
261	030372	012702	020000	MOV	#20000,R2	SET UP ERROR REFERENCE
262	030376	020203		CMP	R2,R3	ARE THEY EQUAL?
263	030400	001051		BNE	TN23EX	EXIT IF NO
264	030402	005204		INC	R4	SUBTEST NUMBER=4(BAD SECTOR FLAGGED)
265	030404	017703	150404	MOV	#DERR,R3	GET ERROR REGISTER AGAIN
266	030410	042703	020000	BIC	#20000,R3	MASK OUT ERROR BIT
267	030414	005002		CLR	R2	SET UP REFERENCE ERROR WORD
268	030416	020203		CMP	R2,R3	ARE THEY EQUAL?
269	030420	001041		BNE	TN23EX	EXIT IF NO
270	030422	005204		INC	R4	SUBTEST NUMBER=5(NO OTHER ERRORS SET)
271	030424	017703	150352	MOV	#DUSH,R3	GET DUSH
272	030430	042703	170000	BIC	#170000,R3	EXTRACT SECTOR AND HEAD ADDRESSES
273	030434	005737	001246	TST	SKPBAD	SKIP OVER BAD SECTOR?
274	030440	001033		BNE	TN23C	LOOK FOR ABORT IF NO
275	030442	012702	000002	MOV	#2,R2	SET UP REFERENCE ERROR WORD
276	030446	020203		CMP	R2,R3	ARE THEY EQUAL?
277	030450	001025		BNE	TN23EX	EXIT IF NO
278	030452	005204		TN23B: INC	R4	SUBTEST NUMBER=6(DUSH OK)
279	030454	005037	001322	CLR	ERRFLG	CLEAR GENERAL ERROR FLAG
280	030460	005037	044306	CLR	ODBUF-4	MAKE BOTH HEADER WORDS VALID
281	030464	005037	044310	CLR	ODBUF-2	
282	030470	012700	025450	MOV	#ISECFB,R0	GET FORMAT TRANSFER BLOCK
283	030474	005237	001176	INC	SPECHD	SET SPECIAL COMMAND FLAG
284	030500	004537	022700	JSR	R5,DXFER	GO REFORMAT SECTOR
285	030504	005037	001176	CLR	SPECHD	CLEAR SPECIAL COMMAND FLAG

6	286	030510	005737	001322	TST	ERRFLG	;	ANY ERRORS?
7	287	030514	001003		BNE	TN23EX	;	EXIT IF YES
8	288	030516	005204		INC	R4	;	SUBTEST NUMBER=7(REWRITE OK)
9	289	030520	005037	024652	CLR	ISECWB	;	MAKE DUSH WRITE BLOCK=0
10	290	030524	004537	003342	TN23EX:	JSR	R5,TSTCTL	EXIT TO TEST CONTROL
11	291				;			
12	292				;			
13	293				;			
14	294				;			
15	295	030530	012702	000001	TN23C:	MOV	#1,R2	SET UP REFERENCE
16	296	030534	020203		CMP	R2,R3	;	OK?
17	297	030536	001372		BNE	TN23EX	;	EXIT IF NO
18	298	030540	000744		BR	TN23B	;	CONTINUE IF YES
19	299				;			
20	300				;			
21	301				;			
22	302				;			
23	303				;			
24	304				;			
25	305				;			
26	306				;			
27	307				;			
28	308				;			
29	309				;			
30	310				;			
31	311				;			
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34	314				;			
35	315				;			
36	316				;			
37	317				;			
38	318				;			
39	319				;			
40	320				;			
41	321				;			
42	322				;		RTZ SEEK TESTS	
43	323				;			
44	324				;			
45	325				;			
46	326				;			
47	327				;		THESE TESTS CHECK THE RTZ COMMAND	
48	328				;		FOR 2 AREAS.THE FIRST SECTION VERIFIES	
49	329				;		THAT THE DRIVE IS INDEED POSITIONED	
50	330				;		ON TRACK 0 AFTER AN RTZ.SECONDLY THE CONDITIONS OF	
51	331				;		THE SEEKING FLIP FLOPS ARE CHECKED (DSTAT) DURING	
52	332				;		AND AFTER THE RTZ COMMAND.	
53	333				;			
54	334				;			
55	335				;			
56	336				;			
57	337				;			
58	338	030542	005004		TN24:	CLR	R4	SUBTEST NUMBER=0
59	339	030544	004537	004276	JSR	R5,ROUSET	;	REQUEST 211
60	340	030550	013777	001044	MOV	MAXCYL,DCYL	;	GET MAX CYLINDER VALUE
61	341	030556	105777	150216	TSTB	@DCSR	;	FORMATTER READY
62	342	030562	100033		BPL	TN24C	;	EXIT IF NO

6	343	030564	005204		INC	R4		JSUBTEST NUMBER=1
7	344	030566	013701	001234	MOV	CURDSK,R1		GET CURRENT DRIVE
8	345	030572	000301		SWAB	R1		MAKE VALID SELECTION WORD
9	346	030574	006301		ASL	R1		
10	347	030576	006301		ASL	R1		
11	348	030600	006301		ASL	R1		
12	349	030602	006301		ASL	R1		
13	350	030604	010177	150172	MOV	R1,0DUSH		SELECT DISK DRIVE
14	351	030610	005777	150176	TST	0DSTAT		DRIVE READY?
15	352	030614	005777	150172	TST	0DSTAT		DEIVE READY?
16	353	030620	052777	000002	BIS	#SEKCMD,0DCSR		ISSUE SEEK COMMAND
17	354	030626	052777	000001	BIS	#GO,0DCSR		SET GO BIT
18	355	030634	105777	150152	TSTB	0DSTAT		WAIT SEEK DONE
19	356	030640	100375		BPL	0-4		WAIT IF NOT
20	357	030642	005204		INC	R4		SUBTEST NUMBER=2(SEEK DONE?)
21	358	030644	005777	150130	TST	0DCSR		ERRORS?
22	359	030650	100002		BPL	0+6		CONTINUE IF NO
23	360	030652	000137	031352	TN24C: JMP	TN24EX		EXIT IF ERROR
24	361	030656	005204		INC	R4		SUBTEST NUMBER=3(NO ERROR)
25	362	030660	010177	150116	MOV	R1,0DUSH		RESELECT DISK DRIVE
26	363	030664	012702	000400	MOV	#400,R2		START REFERENCE WORD
27	364	030670	005005		CLR	R5		START REFERENCE= DRIVE 0
28	365	030672	020537	001234	TN24A: CMP	R5,CURDSK		FOUND IT?
29	366	030676	001403		BEO	TN24B		YES GO ON
30	367	030700	005205		INC	R5		INCREMENT DISK COUNTER
31	368	030702	006302		ASL	R2		REFLECT NEXT DRIVE
32	369	030704	000772		BR	TN24A		TRY NEXT ONE
33	370	030706	010205		TN24B: MOV	R2,R5		GET SEEK DONE COMPARE BIT
34	371	030710	000305		SWAB	R5		PUT IN LOWER BYTE
35	372	030712	006305		ASL	R5		SHIFT FOR REFERENCE
36	373	030714	006305		ASL	R5		
37	374	030716	052702	100000	TN24D: BIS	#BIT15,R2		OR IN DRIVE READY BIT
38	375	030722	053702	001234	BIS	CURDSK,R2		AND SEEK DONE ID BITS
39	376	030726	053705	001234	BIS	CURDSK,R5		OR IN INTERRUPT SEEK DONE ID BITS
40	377	030732	052705	100200	BIS	#100200,R5		R5=DSTAT IMAGE
41	378	030736	010177	150040	MOV	R1,0DUSH		RESELECT DRIVE
42	379	030742	042777	000136	BIC	#FUNC,0DCSR		CLEAR FUNCTION BITS
43	380	030750	052777	000025	BIS	#RECAL,0DCSR		ISSUE RECAL
44	381	030756	105777	150016	TSTB	0DCSR		WAIT FORMATTER READY
45	382	030762	100375		BPL	0-4		
46	383	030764	017703	150022	MOV	0DSTAT,R3		LOAD DISK STATUS REG INTO R3
47	384	030770	042703	020000	BIC	#BIT13,R3		LOSE POSSIBLE WRITE PROTECT
48	385	030774	020203		CMF	R2,R3		ANY SEEKING FLOPS SET?
49	386	030776	001165		BNE	TN24EX		EXIT IF NO
50	387	031000	005204		INC	R4		SUBTEST NUMBER=4(RIGHT SEEKING FLOPS SET)
51	388	031002	032703	000074	BIT	#SKDQNE,R3		CHECK FOR SEEK DONE FLOPS
52	389	031006	001161		BNE	TN24EX		EXIT IF ANY SET
53	390	031010	005204		INC	R4		SUBTEST NUMBER=5(NO OTHER FLOPS SET)
54	391	031012	105777	147774	TSTB	0DSTAT		SEEK DONE?
55	392	031016	100375		BPL	0-4		WAIT UNTIL SEEK DDNE
56	393	031020	010502		MOV	R5,R2		SET UP REFERENCE DATA WORD
57	394	031022	017703	147764	MOV	0DSTAT,R3		GET DISK STATUS REGISTER
58	395	031026	042703	020000	BIC	#BIT13,R3		LOSE POSSIBLE WRITE PROTECT
59	396	031032	042703	007400	BIC	#SKFLOP,R3		REMOVE SEEKING FLOPS IF ANY SET
60	397	031036	020203		CMF	R2,R3		PROPER DISK DONE?
61	398	031040	001144		BNE	TN24EX		EXIT IF NO
62	399	031042	005204		INC	R4		SUBTEST NUMBER=6(SEEK DONE FLOPSET)

6	400	031044	032777	007400	147740	BIT	#SKFLOP,@DSTAT	ANY SEEKING FLOPS SET?
7	401	031052	001137			BNE	TN24EX	EXIT IF YES
8	402	031054	005204			INC	R4	SUBTEST NUMBER=7(NO SEEKING FLOPS SET)
9	403	031056	005077	147726		CLR	@DCYL	LOAD CYLINDER ADDRESS 0 INTO DCYL
10	404	031062	010177	147714		MOV	R1,@DUSH	RESELECT DISK
11	405	031066	042777	000136	147704	BIC	#FUNC,@DCSR	CLEAR FUNCTION BITS
12	406	031074	052777	000004	147676	BIS	#RDCMD,@DCSR	ISSUE READ
13	407	031102	013702	001234		MOV	CURDSK,R2	GET CURRENT DISK AGAIN
14	408	031106	006302			ASL	R2	MAKE VALID INDEX
15	409	031110	016277	001200	147666	MOV	IBFTBL(R2),@DCAR	LOAD INPUT AREA
16	410	031116	013777	001046	147662	MOV	WPSEC,@DWCNT	LOAD ONE SECTOR WORD COUNT
17	411	031124	053777	001302	147646	BIS	SEKINB,@DCSR	SET SEEK INHIBIT BIT
18	412	031132	005277	147642		INC	@DCSR	SET GO BIT
19	413	031136	105777	147636		TSTB	@DCSR	WAIT FORMATTER READY
20	414	031142	100375			BPL	*-4	
21	415	031144	017703	147642		MOV	@DSTAT,R3	LOAD DISK STATUS REGISTER
22	416	031150	042703	170377		BIC	#170377,R3	EXTRACT SEEKING BITS
23	417	031154	005002			CLR	R2	MAKE R2 VALID REFERENCE WORD
24	418	031156	020203			CMP	R2,R3	ANY SEEKING FLOPS SET?
25	419	031160	001074			BNE	TN24EX	EXIT IF YES
26	420	031162	005204			INC	R4	SUBTEST NUMBER=10(SEEK INHIBIT OK)
27	421	031164	005777	147610		TST	@DCSR	ERROR SUMMARY SET?
28	422	031170	100470			BMI	TN24EX	EXIT IF YES
29	423	031172	005204			INC	R4	SUBTEST NUMBER=11(DOES NOT SEEK ON SEEK INHIBIT)
30	424	031174	013702	001044		MOV	MAXCYL,R2	LOAD CYLINDER ADDRESS
31	425	031200	006202			ASR	R2	USE MAXCYL/2
32	426	031202	010277	147602		MOV	R2,@DCYL	LOAD INTO CYLINDER REGISTER
33	427	031206	013702	001234		MOV	CURDSK,R2	GET CURRENT DISK AGAIN
34	428	031212	006302			ASL	R2	MAKE VALID INDEX
35	429	031214	016277	001200	147562	MOV	IBFTBL(R2),@DCAR	INPUT AREA
36	430	031222	042777	000136	147550	BIC	#FUNC,@DCSR	CLEAR FUNCTION BITS
37	431	031230	052777	000004	147542	BIS	#RDCMD,@DCSR	ISSUE READ
38	432	031236	013777	001046	147542	MOV	WPSEC,@DWCNT	LOAD WORD COUNT-ONE SECTOR
39	433	031244	053777	001302	147526	BIS	SEKINB,@DCSR	SET SEEK INHIBIT BIT
40	434	031252	005277	147522		INC	@DCSR	AND SET GO BIT
41	435	031256	105777	147516		TSTB	@DCSR	WAIT FORMATTER READY
42	436	031262	100375			BPL	*-4	
43	437	031264	017703	147522		MOV	@DSTAT,R3	GET DISK STATUS REGISTER
44	438	031270	042703	020000		BIC	#BIT13,R3	LOSE POSSIBLE WRITE PROTECT
45	439	031274	012702	100000		MOV	#100000,R2	SET UP REFERENCE WORD
46	440	031300	053702	001234		BIS	CURDSK,R2	OR IN SEEK INTERRUPT ID BITS
47	441	031304	020203			CMP	R2,R3	SEEK FLOPS SET?
48	442	031306	001021			BNE	TN24EX	EXIT IF YES
49	443	031310	005204			INC	R4	SUBTEST NUMBER=12(NO FLOPS SET)
50	444	031312	005777	147462		TST	@DCSR	ERRORS?
51	445	031316	100015			BPL	TN24EX	EXIT IF NO
52	446	031320	005204			INC	R4	SUBTEST NUMBER=13(ERROR DETECTED)
53	447	031322	032777	000001	147464	BIT	#1,@DERR	TRACK HEADER ERROR?
54	448	031330	001410			BEQ	TN24EX	EXIT IF NO
55	449	031332	042777	000136	147440	BIC	#FUNC,@DCSR	LOSE FUNCTION BITS
56	450	031340	052777	000001	147432	BIS	#SYSCLR,@DCSR	ISSUE FORMATTER CLEAR
57	451	031346	004537	003342		JSR	R5,TSTCTL	EXIT
58	452	031352	005237	001322		TN24EX: INC	ERRFLG	SET ERROR FLAG
59	453	031356	000773			BR	*-8.	AND EXIT
60	454							
61	455							
62	456							



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499 031360 005004
500 031362 004537 004276
501 031366 004537 016332
502 031372 010277 147404
503 031376 000240
504 031400 000240
505 031402 000240
506 031404 005777 147402
507 031410 100126
508 031412 052777 000025 147360
509 031420 105777 147366
510 031424 100375
511 031426 005777 147346
512 031432 100003
513 031434 005237 001322
    
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IMPLIED SEEK TESTS

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THESE TESTS CHECK TWO SEPARATE  
 SEEK ORIENTED FUNCTIONS. FIRST THE IMPLIED  
 TYPE OF A SEEK IS GIVEN IN A READ COMMAND AND  
 A CHECK IS MADE TO SEE THAT THE SEEK DONE FLAG  
 IS NOT SET. SECONDLY, TWO READ COMMANDS ARE GIVEN  
 ONE WITH A PROPER CYLINDER LOCATION AND  
 SEEK INHIBIT SET TO INSURE THE ORIGINAL SEEK WAS  
 TO THE PROPER CYLINDER, AND THE OTHER  
 WITH A ERROEUS CYLINDER ADDRESS AND SEEK INHIBITED  
 TO FORCE A CYLINDER HEADER COMPARE ERROR.

```

TN25: CLR R4 ;SUBTEST NUMBER=0
JSR R5,REQUEST ;REQUEST FORMATTER
JSR R5,DISKID ;60 FORMAT DRIVE SELECTION BITS
MOV R2,ADUSH ;SELECT DISK DRIVE
NOP
NOP
NOP
TST @DSTAT ;DRIVE READY?
BPL TN25EX ;EXIT IF NO
BIS #RECAL,@DCSR ;RECALIBRATE DRIVE
TSTB @DSTAT ;WAIT SEEK DONE
BPL *-4 ;WAIT UNTIL SEEK DONE
TST @DCSR ;ANY ERRORS?
BPL *-8 ;CONTINUE IF NO
INC ERRFLG ;SET ERROR FLAG IF CONTROLLER ERROR
    
```



Line	Address	Content
6	571 031722 000004	WORD RDCMD JDCSR=READ COMMAND
7	572	;
8	573	;
9	574	;
10	575	;
11	576	;
12	577	;
13	578	;
14	579	;
15	580	;
16	581	;
17	582	;
18	583	;
19	584	;
20	585	;
21	586	;
22	587	;
23	588	;
24	589	;
25	590	;
26	591	;
27	592	8M.ECC TEST NUMBERS 26 >> 30 13-NOV-77
28	593	;
29	594	;
30	595	SEEK LOOP TEST
31	596	;
32	597	;
33	598	;
34	599	THIS TEST SENDS THE DISK DRIVE INTO A WORST CASE
35	600	SEEKING LOOP.
36	601	THE SEEKING STARTS AT THE EXTREME ENDS OF THE DISK
37	602	CARTRIDGE(TRACK 0 AND TRACK 823) AND ALTERNATES
38	603	BETWEEN AN INCREASING TRACK ADDRESS AND A DECREASING TRACK
39	604	ADDRESS.THIS PROCESS CONTINUES UNTIL EACH TRACK HAS BEEN
40	605	SOUGHT TWICE.
41	606	;
42	607	;
43	608	DISK ADDRESS TEST
44	609	*****
45	610	;
46	611	;
47	612	THIS SECTION OF TEST 26 CHECKS THE THREE
48	613	DISK ADDRESS FUNCTIONS: SECTOR, HEAD AND CYLINDER.
49	614	STARTING AT DISK ADDRESS 0, A ONE SECTOR
50	615	WRITE READ AND DATA COMPARE IS ISSUED UNTIL
51	616	ALL SECTOR AND HEAD ADDRESSES ARE EXERCISED.
52	617	THE SECOND PART USES A MAXIMUM SECTOR
53	618	AND HEAD ADDRESS AND ISSUES THE SAME TRANSFER
54	619	SEQUENCE ON EACH CYLINDER UNTIL A DISK OVERRUN ERROR
55	620	IS ENCOUNTERED.
56	621	ENDING DISK PARAMETERS ARE CHECKED AFTER EACH TRANSFER.
57	622	;
58	623	;
59	624	;
60	625	;
61	626	;
62	627	;

6	628										
1	629										ERROR CONDITIONS(SEEKING SECTION)
2	630										
3	631										
4	632										R1=DECREASING TRACK ADDRESS
5	633										R2=INCREASING TRACK ADDRESS
6	634										R3=LOOP COUNT ERROR OCCURRED ON
7	635										R5=1 FOR INCREASING ADDRESS
8	636										OR 0 FOR DECREASING ADDR.
9	637										
10	638										
11	639										
12	640										
13	641										
14	642	031724	005004			TN26:	CLR	R4			;SUBTEST NUMBER=0
15	643	031726	004537	004276			JSR	R5,RQUEST			;REQUEST 211
16	644	031732	105777	147042			TSTB	@DCSR			;FORMATTER READY?
17	645	031736	100173				BPL	TN26EX			;EXIT IF NO
18	646	031740	005204				INC	R4			;SUBTEST NUMBER=1
19	647	031742	004537	016332			JSR	R5,DISKID			;FETCH JUSTIFIED DISK ID
20	648	031746	010277	147030			MOV	R2,@DUSH			;SELECT DRIVE
21	649	031752	010200				MOV	R2,R0			;USE R0 FOR SELECTING FROM "0W ON
22	650	031754	000240				NOP				;WAIT READY
23	651	031756	000240				NOP				;
24	652	031760	000240				NOP				;
25	653	031762	000240				NOP				;
26	654	031764	005777	147022			TST	@DSTAT			;DRIVE READY?
27	655	031770	100156				BPL	TN26EX			;EXIT IF NOT READY
28	656	031772	005204				INC	R4			;SUBTEST NUMBER=2
29	657	031774	012703	000001			MOV	#1,R3			;ESTABLISH OUTER LOOP=1
30	658	032000	013704	001044		TN26B:	MOV	MAXCYL,R4			;ESTABLISH MAXIMUM CYLINDER COUNT
31	659	032004	010401				MOV	R4,R1			;PUT LOOP COUNT IN R1
32	660	032006	005002				CLR	R2			;ESTABLISH INCREASING TRACK POINTER
33	661										;
34	662	032010	010177	146774		TN26A:	MOV	R1,@DCYL			;LOAD CYLINDER ADDRESS
35	663	032014	010077	146762			MOV	R0,@DUSH			;SELECT DRIVE
36	664	032020	052777	000002	146752		BIS	#SEKCMD,@DCSR			;LOAD SEEK COMMAND
37	665	032026	052777	000101	146744		BIS	#INTGO,@DCSR			;SET GO AND INTERRUPTS
38	666	032034	004537	017342			JSR	R5,WAIT			;WAIT FOR INTERRUPT
39	667	032040	005737	001150			TST	INTFLG			;INTERRUPT OCCUR?
40	668	032044	001530				BEQ	TN26EX			;EXIT IF NO
41	669	032046	005037	001150			CLR	INTFLG			;INTERRUPT OCCURRED
42	670	032052	105777	146734			TSTB	@DSTAT			;SEEK DONE?
43	671	032056	100123				BPL	TN26EX			;EXIT IF NO
44	672	032060	005777	146714			TST	@DCSR			;ERROR?
45	673	032064	100520				BMI	TN26EX			;EXIT IF YES
46	674	032066	010277	146716			MOV	R2,@DCYL			;LOAD INCREASING CYLINDER ADDR
47	675	032072	010077	146704			MOV	R0,@DUSH			;SELECT DRIVE
48	676	032076	052777	000002	146674		BIS	#SEKCMD,@DCSR			;LOAD SEEK COMMAND
49	677	032104	052777	000101	146666		BIS	#INTGO,@DCSR			;SET GO AND INTERRUPT BITS
50	678	032112	004537	017342			JSR	R5,WAIT			;WAIT FOR INTERRUPT
51	679	032116	005737	001150			TST	INTFLG			;DID WE INTERRUPT?
52	680	032122	001501				BEQ	TN26EX			;EXIT IF NO
53	681	032124	005037	001150			CLR	INTFLG			;RESET INTERRUPT OCCURRENCE FLAG
54	682	032130	105777	146656			TSTB	@DSTAT			;SEEK DONE?
55	683	032134	100074				BPL	TN26EX			;EXIT IF NO
56	684	032136	005777	146636			TST	@DCSR			;ERRORS?

1	685	032142	100471		BMI	TN26EX		);EXIT IF YES'	
2	686	032144	005202		INC	R2		);INCREMENT TRACK ADDRESS	
3	687	032146	005301		DEC	R1		);DECREMENT DECREASING TRACK ADDRESS	
4	688	032150	001317		BNE	TN26A		);REPEAT INNER LOOP IF NOT DONE	
5	689	032152	005303		DEC	R3		);DECREMENT OUTER LOOP	
6	690	032154	001311		BNE	TN26B		);REPEAT OUTER LOOP IF NOT DONE	
7	691				;				
8	692				;				
9	693				;				
10	694				;				
11	695				;				
12	696				;				
13	697				;				
14	698				;				
15	699				;				
16	700				;				
17	701				;				
18	702				;				
19	703				;				
20	704				;				
21	705				;				
22	706				;				
23	707				;				
24	708				;				
25	709				;				
26	710				;				
27	711	032156	012704	000005	TN26C:	MOV	#5,R4	);SET SUBTEST NUMBER=5(STARTING DISK ADDR TEST	
28	712	032162	012700	035520		MOV	#WRCB,R0	);POINT TO WRITE READ BLOCK	
29	713	032166	005010			CLR	(R0)	);START DISK ADDR =0	
30	714	032170	005060	000006		CLR	6(R0)	);CYLINDER ALSO	
31	715	032174	013760	001046	000004	MOV	WPSEC,4(R0)	);WORD COUNT =ONE SECTOR	
32	716	032202	012701	044312		MOV	#0DBUF,R1	);POINT TO OUT PUT BUFFER	
33	717	032206	004537	016736		JSR	R5,FORMAT	);FORMAT DATA BUFFER	
34	718	032212	004537	035356	TN26D:	JSR	R5,WRC	);GO WRITE/READ AND DATA COMPARE	
35	719	032216	005737	001322		TST	ERRFLG	);ERRORS?	
36	720	032222	001027			BNE	TN26F	);EXIT IF YES	
37	721	032224	013710	001162		MOV	ENDSEC,(R0)	);UPDATE DISK ADDRESSES	
38	722	032230	053710	001164		BIS	ENDHD,(R0)	);FIRST SECTOR AND HEAD	
39	723	032234	013760	001166	000006	MOV	ENDCYL,6(R0)	);THEN CYLINDER	
40	724	032242	026027	000006	000001	CHP	6(R0),#1	);HAVE WE REACHED FIRST CYLINDER?	
41	725	032250	001360			BNE	TN26D	);CONTINUE WITH SECTOR - HEAD CHECKOUT IF NO	
42	726	032252	005204			INC	R4	);SUBTEST NUMBER=6(SECTOR HEAD ADDRESS OK)	
43	727	032254	013710	001054		MOV	R0USH,(R0)	);MAKE SECTOR- HEAD ADDR. MAX	
44	728	032260	004537	035356	TN26E:	JSR	R5,WRC	);WRITE READ/ DATA COMPARE ALL CYLINDER ADDR.	
45	729	032264	005737	001322		TST	ERRFLG	);ERRORS?	
46	730	032270	001004			BNE	TN26F	);CHECK OVERRUN ERROR IF YES	
47	731	032272	013760	001166	000006	MOV	ENDCYL,6(R0)	);UPDATE CYLINDER ADDRESS IF NO ERROR	
48	732	032300	000767			BR	TN26E	);AND CONTINUE	
49	733	032302	032777	000040	146504	TN26F:	BIT	#BITS,#DERR	);IS THE ERROR NONEXT CYLINDER
50	734	032310	001404			BEQ	TN26GT	);EXIT IF NOT THAT ERROR	
51	735	032312	000240			NOP			
52	736	032314	000240			NOP			
53	737	032316	005037	001322		CLR	ERRFLG	);CLEAR ERROR FLAG IF YES	
54	738	032322	004537	003342	TN26OT:	JSR	R5,TSTCTL	);EXIT ALL DONE	
55	739	032326	005737	001322	TN26EX:	TST	ERRFLG	);ERROR FLAG SET?	
56	740	032332	001373			BNE	TN26OT	);EXIT IF YES	
57	741	032334	005237	001322		INC	ERRFLG	);SHOULD BE SET-SET IT	

DISK ADDRESS TEST

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6	742	032340	000770		BR	TN260T	JAND EXIT
7	743				;		
8	744				;		
9	745				;		
10	746				;		
11	747				;		
12	748				;		
13	749				;		
14	750				;		
15	751				;		
16	752				;		
17	753				;		
18	754				;		
19	755				;		
20	756				;		
21	757				;	1. OVERRUN TEST	
22	758				;	.....	
23	759				;	THIS TEST CHECKS THE OVERRUN ERROR LOGIC	
24	760				;	BY ATTEMPTING A READ PAST MAXSEC,MAXHD	
25	761				;	AND MAXCYLINDER.	
26	762				;		
27	763				;	2. MEMORY EXTENSION TEST	
28	764				;	.....	
29	765				;	THIS TEST CHECKS THAT THE MEMORY EXTENSION BITS	
30	766				;	ON THE PHOENIX 211 ARE SET WHEN AN INCREMENT IS GENERATED ON	
31	767				;	ON THE BUSS ADDRESS REGISTER AFTER THE REGISTER HAS BEEN	
32	768				;	SET TO 177776.	
33	769				;		
34	770				;		
35	771				;	3. BUSS TIME OUT TEST	
36	772				;	.....	
37	773				;		
38	774				;		
39	775				;	THIS TEST DOES A TRANSFER THAT EXTENDS INTO NON EXISTANT	
40	776				;	CORE FORCING A BUSS TIME OUT ERROR.	
41	777				;		
42	778				;		
43	779				;	*****	
44	780				;		
45	781	032342	000137	033334	\$TN27:	JMP	TN27EX JEXIT JUMP
46	782				;		
47	783				;	*****	
48	784				;		
49	785				;		
50	786				;		
51	787				;		
52	788	032346	005004		TN27:	CLR	R4 JSUBTEST NUMBER=0
53	789	032350	004537	004276		JSR	R5,RQUEST ;REQUEST 211
54	790	032354	012700	033350		MOV	#0VBLK,R0 ;FETCH OVERRUN BLOCK ADDRESS
55	791	032360	013737	001234 044310		MOV	CURDSK,0DBUF-2 ;SAVE CURRENT DISK UNIT
56	792	032366	013710	001054		MOV	KDUSH,(R0) ;LOAD DUSH AS MAXIMUM
57	793	032372	013760	001046 000004		MOV	WPSEC,4(R0) ;LOAD WORD COUNT
58	794	032400	006360	000004		ASL	4(R0) ;MAKE TWO SECTORS
59	795	032404	013760	001044 000006		MOV	MAXCYL,6(R0) ;LOAD LAST CYLINDER ADDRESS
60	796	032412	004537	022700		JSR	R5,DXFER ;ISSUE WRITE COMMAND
61	797	032416	005737	001322		TST	ERRFLG ;ERROR DETECTED?
62	798	032422	001747			BEC	\$TN27 JAND EXIT TO TEST CONTROL

1	799	032424	005204		INC	R4		JSUBTEST NUMBER=1(ERROR DETECTED)
2	800	032426	012702	000010	MOV	#10,R2		JSSET UP REFERENCE ERROR WORD
3	801	032432	017703	146356	MOV	@DERR,R3		JSGET ERROR REGISTER
4	802	032436	042703	177767	BIC	#177767,R3		JSXTRACT OVERRUN BIT
5	803	032442	020203		CMP	R2,R3		JSARE THE RIGHT ERRORS SET?
6	804	032444	001336		BNE	\$TN27		JSEXIT IF NO
7	805	032446	005204		INC	R4		JSUBTEST NUMBER=2(OVERRUN ERROR DETECTED)
8	806	032450	017703	146340	MOV	@DERR,R3		JSFETCH ERROR REGISTER AGAIN
9	807	032454	042703	000010	BIC	#10,R3		JSMASK OUT OVERRUN ERROR
10	808	032460	005002		CLR	R2		JSSET UP REFERENCE ERROR WORD
11	809	032462	020203		CMP	R2,R3		JSANY OTHER ERRORS SET?
12	810	032464	001326		BNE	\$TN27		JSEXIT IF YES
13	811	032466	005204		INC	R4		JSUBTEST NUMBER=3(NO OTHER ERRORS)
14	812	032470	042777	000136	BIC	#FUNC,@DCSR		JSLOSE FUNCTION BITS
15	813	032476	052777	000001	BIS	#SYSCLR,@DCSR	146274	JSISSUE FORMATTER CLEAR
16	814	032504	004537	004276	JSR	R5,REQUEST		JSREQUEST 211
17	815	032510	105777	146264	TSTB	@DCSR		JSWAIT FORMATTER READY
18	816	032514	100375		BPL	-4		JS
19	817	032516	005777	146256	TST	@DCSR		JSERRORS CLEARED?
20	818	032522	100707		BMI	\$TN27		JSEXIT WITH ERROR FLAG SET IF NO
21	819	032524	005204		INC	R4		JSUBTEST NUMBER=4(ERROR CLEARED BY SYS CLEAR)
22	820	032526	005037	001322	CLR	ERRFLG		JSCLR GENERAL ERROR FLAG IF YES
23	821	032532	012700	023610	MOV	#WRTBLK*6,R0	TN27A	JSFETCH WORD COUNT ENTRY OF WRITE BLOCK
24	822	032536	005010		CLR	(R0)		JSENTER CYL
25	823	032540	012740	177777	MOV	#-1,-(R0)		JSENTER WORD COUNT OF ONE
26	824	032544	012740	177776	MOV	#-2,-(R0)		JSENTER MEMORY ADDRESS OF 177776
27	825	032550	005040		CLR	-(R0)		JSMAKE DUSH=0
28	826	032552	004537	022700	JSR	R5,DXFER		JSTRY A WRITE (MAY BE OK DEPENDING ON SIZE OF MEMORY)
29	827	032556	005037	001322	CLR	ERRFLG		JSRESET ERROR FLAG IF SET
30	828	032562	017703	146212	MOV	@DCSR,R3		JSFETCH DCSR REGISTER
31	829	032566	042703	147777	BIC	#147777,R3		JSXTRACT MEMORY EXTENSION BITS
32	830	032572	012702	010000	MOV	#10000,R2		JSSET UP REFERENCE WORD
33	831	032576	020203		CMP	R2,R3		JSDID MEMORY REGISTER INCREMENT?
34	832	032600	001260		BNE	\$TN27		JSEXIT IF NO
35	833	032602	005204		INC	R4		JSUBTEST NUMBER=5(FIRST MEMORY BIT OK)
36	834	032604	005777	146170	TST	@DCSR		JSIS THERE AN ERROR?
37	835	032610	100013		BPL	TN27C		JSCONTINUE IF NO
38	836	032612	042777	000136	BIC	#FUNC,@DCSR	146160	JSLOSE FUNCTION BITS
39	837	032620	052777	000001	BIS	#SYSCLR,@DCSR	146152	JSISSUE SYSTEM CLEAR
40	838	032626	004537	004276	JSR	R5,REQUEST		JSREQUEST 211
41	839	032632	005777	146142	TST	@DCSR		JSRETEST FOR ERROR
42	840	032636	100641		BMI	\$TN27		JSEXIT IF ERROR CONDITION PERSISTS
43	841	032640	052737	020000	BIS	#20000,WRTBLK*8	023612 TN27C	JSOR IN SECOND MEMORY EXTENSION
44	842	032646	012700	023602	MOV	#WRTBLK,R0		JSPOINT R0 TO WRTBLK ADDRESS
45	843	032652	004537	022700	JSR	R5,DXFER		JSATTEMPT ANOTHER WRITE
46	844	032656	005037	001322	CLR	ERRFLG		JSRESET ERROR FLAG IIF SET
47	845	032662	012702	030000	MOV	#30000,R2		JSSET UP REFERENCE WORD
48	846	032666	017703	146106	MOV	@DCSR,R3		JSFETCH DCSR
49	847	032672	042703	147777	BIC	#147777,R3		JSXTRACT MEMORY EXTENSION BITS
50	848	032676	020203		CMP	R2,R3		JSARE THEY EQUAL?
51	849	032700	001220		BNE	\$TN27		JSEXIT IF NO
52	850	032702	005204		INC	R4		JSUBTEST NUMBER=6(SECOND MEMORY BIT OK)
53	851	032704	005777	146070	TST	@DCSR		JSERROR IN DCSR?
54	852	032710	100016		BPL	TN27D		JSCONTINUE IF NO
55	853	032712	042777	000136	BIC	#FUNC,@DCSR	146060	JSLOSE FUNCTION BITS
56	854	032720	052777	000001	BIS	#SYSCLR,@DCSR	146052	JSISSUE SYSTEM CLEAR
57	855	032726	004537	004276	JSR	R5,REQUEST		JSREQUEST 211





1	913	033152	042777	000136	145620	BIC	#FUNC,#DCSR	);LOSE FUNCTION BITS
2	914	033160	052777	000001	145612	BIS	#SYSCLR,#DCSR	);ISSUE SYSTEM CLEAR
3	915	033166	004537	004276		JSR	R5,RQUEST	);REQUEST 211
4	916	033172	105777	145602		TSTB	#DCSR	);WAIT DONE
5	917	033176	100375			BPL	0-4	);
6	918	033200	005777	145574		TST	#DCSR	);TEST FOR ERROR
7	919	033204	100453			BMI	TN27EX	);EXIT IF ERROR PERSISTS
8	920	033206	005037	001322		CLR	EKRFLG	);RESET ERROR FLAG (ALL DONE)
9	921	033212	005204			INC	R4	);SUBTEST NUMBER=13(ERROR CLEARED)
10	922	033214	012700	023604		MOV	#WRTBLK+2,R0	);POINT TO WRITE BLOCK
11	923	033220	012710	160000		MOV	#160000,(R0)	);THIS BUSS ADDRESS WILL DETECT
12	924							POSSIBILITY OF FCO #75 MISSING IN INTERFACE BD'S
13	925							THE INTERFACE BD'S AFFECTED BY THIS FCO
14	926							ARE LEVEL A3 AND UNDER(74177'S > 74271'S).
15	927							
16	928							***** ALL THESE BOARDS ARE WIRE WRAP*****
17	929							
18	930							
19	931							IF THIS FCO IS MISSING CERTAIN ADDRESSES BOUNDARIES
20	932							IN THE 150000 TO 170000 AREA WILL ERRONEOUSLY
21	933							INCREMENT THE BUSS EXTENSION BITS,OPERATING SYSTEMS
22	934							LARGER THAN 28K WILL NOT RUN!!!!!!!!!!!!!!
23	935	033224	042760	030000	000006	BIC	#MEMEX,6(R0)	);CLEAR MEMORY EXT. BITS IF SET
24	936	033232	012700	023602		MOV	#WRTBLK,R0	);LOAD WRITE BLOCK ADDR
25	937	033236	012701	000020		MOV	#20,R1	);LOAD ATTEMPT LOOP COUNT
26	938	033242	004537	022700		JSR	R5,DXFER	);TRY TO GENERATE THIS ERROR
27	939	033246	005037	001322		CLR	ERRFLG	);ERROR FLAG MAY BE SET - DONT CARE
28	940	033252	017703	145522		MOV	#DCSR,R3	);FETCH COMMAND AND STATUS REG
29	941	033256	005002			CLR	R2	);SET UP REFERENCE WORD
30	942	033260	042703	147777		BIC	#147777,R3	);EXTRACT MEMORY EXT.
31	943	033264	020203			CHP	R2,R3	);ANYTHING SET?
32	944	033266	001403			BEQ	TN27G	);CONTINUE IF NO
33	945	033270	005237	001322		INC	ERRFLG	);SET ERROR FLAG IF YES
34	946	033274	000417			BR	TN27EX	);AND EXIT
35	947	033276	005301			DEC R1		);DECREMENT LOOP COUNT
36	948	033300	001360			BNE	TN27H	);AND TRY AGAIN
37	949	033302	000137	033362		JMP	TN27J	);CONTINUE TO MEMORY INC TEST
38	950	033306	042737	030000	023612	TN270I: BIC	#MEMEX,#WRTBLK+8	);CLEAR MEMORY EXTENSION BITS
39	951	033314	042737	030000	024662	BIC	#MEMEX,ISECV8+8	);IN BITH WRITE BLOCKS
40	952	033322	013737	044310	001234	MOV	ODBUF-2,CURDSK	);RELOAD CURRENT DISK
41	953	033330	004537	003342		JSR	R5,TSTCTL	);EXIT TO TEST CONTROL
42	954	033334	005737	001322		TST	ERRFLG	);ERROR FLAG SET?
43	955	033340	001362			BNE	TN27G	);EXIT IF YES
44	956	033342	005237	001322		INC	ERRFLG	);SET IT IF NOT
45	957	033346	000757			BR	TN270T	);AND EXIT
46	958							
47	959							
48	960							OVERRUN RUN COMMAND BLOCK
49	961							
50	962							
51	963							
52	964	033350	000000			OYBLK: .WORD 0		);DUSH IMAGE
53	965	033352	047314			.WORD IOBUF1		);INPUT BUFFER IS IOBUF1
54	966	033354	177000			.WORD 177000		);WORD COUNT IS TWO SECTORS
55	967	033356	000000			.WORD 0		);CYLINDER ADDRESS IS MAXCYL
56	968	033360	000006			.WORD WRTCMD		);COMMAND IS WRITE
57	969							



1	1027	033500	005702		TST	R2		ANY SET?
2	1028	033502	001051		BNE	TN27P		USE DIFFERENT ROUTINE IF YES
3	1029	033504	017703	145270	MOV	@DCSR,R3		IF NOT LETS CHECK THAT THEY DIDN'T
4	1030	033510	042703	147777	BIC	#147777,R3		EXTRACT ENDING DCSR REG
5	1031	033514	020203		CHP	R2,R3		SEE IF BIT SET
6	1032	033516	001306		BNE	TN27EX		EXIT IF SOMTHING SET
7	1033	033520	016002	000002	TN27L: MOV	2(R0),R2		LOAD STARTING BUSS ADDR.
8	1034	033524	062702	000002	ADD	#2,R2		UPDATE
9	1035	033530	017703	145250	TN27M: MOV	@DBAR,R3		FETCH ACTUAL BUSS ADDR. REG
10	1036	033534	020203		CHP	R2,R3		ARE THE EQUAL?
11	1037	033536	001276		BNE	TN27EX		EXIT IF NO
12	1038	033540	000730		BR	TN27K		CONTINUE IF LEGAL
13	1039	033542	005002		TN27M: CLR	R2		SET UP REFERENCE WORD
14	1040	033544	017703	145234	MOV	@DBAR,R3		
15	1041	033550	020203		CHP	R2,R3		EQUAL?
16	1042	033552	001270		BNE	TN27EX		EXIT IF NO
17	1043	033554	016002	000010	MOV	10(R0),R2		LOAD STARTING ADDR AGAIN
18	1044	033560	042702	147777	BIC	#147777,R2		EXTRACT BITS
19	1045	033564	020227	030000	CHP	R2,#30000		OVER FLOW?
20	1046	033570	001427		BEO	TN27R		EXIT IF YES
21	1047	033572	062702	010000	ADD	#10000,R2		UPDATE EXT BIT
22	1048	033576	017703	145176	MOV	@DCSR,R3		FETCH COMMAND REGISTER
23	1049	033602	042703	147777	BIC	#147777,R3		EXTRACT MEM. EXT. BITS
24	1050	033606	020203		CHP	R2,R3		BIT INCREMENT?
25	1051	033610	001251		BNE	TN27EX		EXIT IF NO
26	1052	033612	042760	030000	000010	BIC	#30000,10(R0)	UPDATE STARTING POINT
27	1053	033620	050360	000010	BIS	R3,10(R0)		
28	1054	033624	000676		BR	TN27K		GO ON
29	1055	033626	017703	145146	TN27P: MOV	@DCSR,R3		MEM EXT SHOULD'T HAVE INCREMENTED HERE
30	1056	033632	042703	147777	BIC	#147777,R3		EXTRACT MEM EXT BITS
31	1057	033636	020203		CHP	R2,R3		DID IT INCREMENTED?
32	1058	033640	001235		BNE	TN27EX		EXIT IF YES
33	1059	033642	016002	000002	MOV	2(R0),R2		ASSEMBLE REFERENCE WORD
34	1060	033646	000724		BR	TN27L		NOW CHECK BUSS ADDR.
35	1061	033650	005002		TN27R: CLR	R2		SET UP REFERENCE FOR LAST ADDR.
36	1062	033652	017703	145122	MOV	@DCSR,R3		FETCH COMMANDREG.
37	1063	033656	042703	147777	BIC	#147777,R3		EXTRACT MEM EXT BITS
38	1064	033662	020203		CHP	R2,R3		OVERFLOW?
39	1065	033664	001223		BNE	TN27EX		EXIT IF NO
40	1066	033666	017703	145112	MOV	@DBAR,R3		NOW CHECK BUSS ADDRESS
41	1067	033672	020203		CHP	R2,R3		OVERFLOW?
42	1068	033674	001217		BNE	TN27EX		EXIT IF NO
43	1069	033676	012760	000006	000010	MOV	#VRTCHD,10(R0)	RESTORE COMMAN IN TRANSFER BLOCK
44	1070	033704	005010		CLR	(R0)		RESTORE DUSH ADDRESS
45	1071	033706	000137	033306	JMP	TN270T		AND EXIT
46	1072							
47	1073							
48	1074							
49	1075							
50	1076							
51	1077							
52	1078							
53	1079							
54	1080							
55	1081							
56	1082							
57	1083							

```

6      1084      ;
7      1085      ;
8      1086      ;
9      1087      ;
10     1088      ;
11     1089      ;
12     1090      ;
13     1091      ;
14     1092      ;
15     1093      ;          SEEK/WRITE/DATA COMPARE TEST   TN30
16     1094      ;
17     1095      ;
18     1096      ;
19     1097      ;
20     1098      ;
21     1099      ;          THIS TEST IS A RELIABILITY TEST.
22     1100      ;          THE DRIVE IS MADE TO SEEK IN A WORST CASE
23     1101      ;          PATTERN AND WRITE DATA GENERATED BY A
24     1102      ;          SUBROUTINE,PAIGEN, THAT CREATES A UNIQUE
25     1103      ;          ARRAY OF DATA EACH TIME IT IS CALLED.
26     1104      ;
27     1105      ;
28     1106      ;
29     1107      ;
30     1108      ;
31     1109      ;
32     1110      ;          RANDOM TRANSFER TEST
33     1111      ;          *****
34     1112      ;
35     1113      ;
36     1114      ;
37     1115      ;
38     1116      ;          THE SECOND SECTION OH THIS TEST
39     1117      ;          IS A WRITE/READ DATA COMPARE EXERCISE
40     1118      ;          USING RANDOM DATA AND RANDOM DISK ADDRESSES.
41     1119      ;          THE FOLLOWING IS A LIST OF THE RANDOM PARAMETERS
42     1120      ;
43     1121      ;          1. SECTOR ADDRESS
44     1122      ;          2. HEAD ADDRESS
45     1123      ;          3. TRACK ADDRESS
46     1124      ;          4. UNIT ADDRESS(IF MORE THAN ONE ONLINE)
47     1125      ;          5. TRANSFER SIZE (UP TO 2 SECTORS)
48     1126      ;          6. DATA WORD
49     1127      ;
50     1128      ;
51     1129      ;
52     1130      ;
53     1131      ;
54     1132      ;
55     1133      ;
56     1134      ;
57     1135 033712 013737 001044 034124 TN30:  MOV  MAXCYL,CYLDN  ;LOAD MAXIMUM CYLINDER
58     1136 033720 042737 000001 034124      BIC  #BIT0,CYLDN  ;AVOID ODD ENING CYLINDER NUMBER
59     1137 033726 004537 004276              JSR  R5,RQUEST   ;REQUEST 301
60     1138 033732 012737 000002 036142      MOV  #2,CNTINC   ;MAKE PATTERN GENERATOR INCREMENT=2
61     1139 033740 005037 034122              CLR  CYLUP       ;CLEAR INCREASING CYLINDER COUNTER
62     1140 033744 005004                      TN30A: CLR  R4     ;INITIALIZE SUBTEST NUMBER

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1	1141	033746	012700	035520		MOV	#WRCB,R0	;	GET WRITE/READ BLOCK ADDRESS
2	1142	033752	013710	001054		MOV	RDUSH,(R0)	;	MAKE DUSH MAXIMUM
3	1143	033756	013760	034124	000006	MOV	CYLDN,6(R0)	;	LOAD CYLINDER ADDRESS
4	1144	033764	013701	034124		MOV	CYLDN,R1	;	LOAD CYLINDER ADDRESS FOR PATTERN BIAS
5	1145	033770	004537	036064		JSR	R5,PATGEN	;	FORMAT DATA
6	1146	033774	013760	001046	000004	MOV	WPSEC,4(R0)	;	GO WRITE DISK
7	1147	034002	004537	035356		JSR	R5,WRC	;	GO WRITE READ DATA COMPARE
8	1148	034006	005737	001322		TST	ERRFLG	;	ANY ERRORS?
9	1149	034012	001041			BNE	TN30EX	;	EXIT IF YES
10	1150	034014	005204			INC	R4	;	SUBTEST NUMBER=1,2
11	1151	034016	005337	034124		DEC	CYLDN	;	DECREMENT CYLINDER ADDRESS
12	1152	034022	020427	000002		CMP	R4,#2	;	WRITE 2 CYLINDERS?
13	1153	034026	001347			BNE	TN30A+2	;	DO IT AGAIN IF NO
14	1154	034030	005204			INC	R4	;	SUBTEST NUMBER=3
15	1155	034032	012700	035520	TN30B:	MOV	#WRCB,R0	;	GET TRANSFER BLOCK AGAIN
16	1156	034036	005010			CLR	(R0)	;	MAKE DUSH MINIMUM
17	1157	034040	013760	034122	000006	MOV	CYLUP,6(R0)	;	LOAD INCREASING TRACK ADDRESS
18	1158	034046	013701	034122		MOV	CYLDN,R1	;	USE CYLINDER ADDRESS FOR PATTERN BIAS
19	1159	034052	004537	036064		JSR	R5,PATGEN	;	FORMAT DATA
20	1160	034056	004537	035356		JSR	R5,WRC	;	GO WRITE DISK
21	1161	034062	005737	001322		TST	ERRFLG	;	ANY ERRORS?
22	1162	034066	001013			BNE	TN30EX	;	EXIT IF YES
23	1163	034070	005204			INC	R4	;	SUBTEST NUMBER=4,5
24	1164	034072	005237	034122		INC	CYLUP	;	INCREMENT CYLINDER ADDRESS
25	1165	034076	020427	000005		CMP	R4,#5	;	HAVE WE DONE 2 WRITES?
26	1166	034102	001353			BNE	TN30B	;	WRITE ANOTHER SECTOR IF NO
27	1167	034104	005737	034124		TST	CYLDN	;	HAVE WE DONE WHOLE DISK?
28	1168	034110	001315			BNE	TN30A	;	WRITE 4 MORE SECTIRS IF NOT
29	1169	034112	000137	034126		JMP	TN30E	;	NOW GO USE RANDOM DATA
30	1170	034116	004537	003342	TN30EX:	JSR	R5,TSTCTL	;	EXIT TO PROGRAM CONTROL IF NO
31	1171							;	
32	1172							;	
33	1173							;	
34	1174							;	
35	1175							;	
36	1176							;	
37	1177							;	
38	1178							;	
39	1179							;	
40	1180	034122	000000		CYLUP:	WORD 0		;	INCREASING CYLINDER COUNTER
41	1181	034124	000000		CYLDN:	WORD 0		;	DECREASING CYLINDER COUNTER
42	1182							;	
43	1183							;	
44	1184							;	
45	1185							;	
46	1186							;	
47	1187							;	
48	1188							;	
49	1189							;	
50	1190							;	
51	1191							;	
52	1192							;	
53	1193							;	
54	1194							;	
55	1195							;	
56	1196							;	
57	1197							;	

RANDOM TRANSFER TEST  
\*\*\*\*\*

THIS SECTION OF TEST 30





6	1312	034300	012221			MOV	(R2)+,(R1)+		;WORDS
7	1313	034302	012221			MOV	(R2)+,(R1)+		;
8	1314	034304	011211			MOV	(R2),(R1)		;SAVE CURRENT DISK ADDRESS VALUES
9	1315	034306	012701	044312		MOV	#0DBUF,R1		;POINT R1 TO OUTPUT BUFFER
10	1316	034312	063701	001050		ADD	POSWP,R1		;INCREASE TO SECOND BUFFER OUTPUT
11	1317	034316	063701	001050		ADD	POSWP,R1		
12	1318	034322	013740	001046		MOV	WPSEC,-(R0)		;SET WORD COUNT FOR ONE SECTOR
13	1319	034326	004537	022436		JSR	R5,ENDPAR		;COMPUTE DISK ADDRESS FOR SECOND SECTOR
14	1320	034332	013721	001162		MOV	ENDSEC,(R1)+		;PUT ABSOLUTE DISK ADDRESS IN SECOND BUFFER
15	1321	034336	013721	001164		MOV	ENDHD,(R1)+		;
16	1322	034342	013721	001166		MOV	ENDCYL,(R1)+		;
17	1323	034346	013710	001046		MOV	WPSEC,(R0)		;SET WORD COUNT FOR 2 SECTORS
18	1324	034352	006320			ASL	(R0)+		;
19	1325	034354	004537	035000		JSR	R5,DSKST		;REDUCE WORD COUNT BY 316 IF LAST
20	1326								;WRITE OPERATION ON DISK
21	1327	034360	012700	023602		MOV	#WRTBLK,R0		;POINT R0 TO WRITE BLOCK ORIGIN
22	1328	034364	004537	022700		JSR	R5,DXFER		;PERFORM TWO SECTOR WRITE ON DISK
23	1329	034370	005737	001322		TST	ERRFLG		;ANY ERRORS?
24	1330	034374	001144			BNE	T31EX		;EXIT IF YES
25	1331	034376	005737	001144		TST	DKEND		;ARE WE DONE WRITING?
26	1332	034402	001012			BNE	R0		;CONTINUE WITH NEXT 2 SECTORS IF NOT
27	1333	034404	013737	001162	001136	MOV	ENDSEC,CURSEC		;UPDATE CURRENT SECTOR
28	1334	034412	013737	001166	001142	MOV	ENDCYL,CURCYL		;AND CYLINDER
29	1335	034420	013737	001164	001140	MOV	ENDHD,CURHD		;AND HEAD
30	1336	034426	000705			BR	T31WLP		;GO WRITE AGAIN
31	1337								
32	1338								
33	1339								
34	1340								READ AND COMPARE PROGRAM
35	1341								
36	1342								
37	1343								THIS PROGRAM READS THE COMPLETE DISK SURFACE AND
38	1344								COMPARES THE DATA RECEIVED WITH THEREFERENCE DATA.
39	1345								
40	1346	034430	005204			RD: INC	R4		;SUBTEST+1
41	1347	034432	012737	000001	001136	MOV	#1,CURSEC		;REINITIALIZE DISK ADDRESS PARAMETERS
42	1348	034440	005037	001140		CLR	CURHD		;
43	1349	034444	005037	001144		CLR	DKEND		;CLEAR END OF DISK FLAG
44	1350	034450	005037	001142		CLR	CURCYL		;
45	1351	034454	012701	044312		T31RPL:MOV	#0DBUF,R1		;GET INPUT BUFFER ORIGIN
46	1352	034460	012700	001136		MOV	#CURSEC,R0		;GETCURRENT SECTOR ADDRESS
47	1353	034464	012021			MOV	(R0)+,(R1)+		;PUT ABS DISK ADDRESS IN BUFFER
48	1354	034466	012021			MOV	(R0)+,(R1)+		;
49	1355	034470	011011			MOV	(R0),(R1)		;
50	1356	034472	012700	023614		MOV	#RDBLK,R0		;POINT R0 TO READ BLOCK ORIGIN
51	1357	034476	013710	001136		MOV	CURSEC,(R0)		;FORMAT DUSH WORD
52	1358	034502	053720	001140		BIS	CURHD,(R0)+		;OR IN HEAD FIELD
53	1359	034506	013701	001234		MOV	CURDSK,R1		;GET CURRENT DISK
54	1360	034512	006301			ASL	R1		;MAKE VALID INDEX
55	1361	034514	016120	001200		MOV	IBFTBL(R1),(R0)+		;LOAD INPUT BUFFER AREA
56	1362	034520	013720	001046		MOV	WPSEC,(R0)+		;SPECIFY ONE SECTOR READ
57	1363	034524	013710	001142		MOV	CURCYL,(R0)		;SET DISK CYLINDER
58	1364	034530	005740			TST	-(R0)		;POINT R0 TO WORD COUNT CB ENTRY
59	1365	034532	004537	022436		JSR	R5,ENDPAR		;COMPUTE ENDING DISK ADDRESS
60	1366	034536	012700	001162		MOV	#ENDSEC,R0		;GET CURRENT SECTOR ADDRESS
61	1367	034542	012701	044312		MOV	#0DBUF,R1		;POINT R1 TO BUFFER AREA
62	1368	034546	063701	001050		ADD	POSWP,R1		;ADJUS FOR SECOND SECTOR



6	1369	034552	063701	001050	ADD	POSWP,R1		
7	1370	034556	012021		MOV	(R0)+,(R1)+	PUT DISK ADDRESS IN BUFFER	
8	1371	034560	012021		MOV	(R0)+,(R1)+	;	
9	1372	034562	011011		MOV	(R0),(R1)	;	
10	1373	034564	012700	023620	MOV	#RDBLK+4,R0	POINT R0 TO WORD COUNT CB ENTRY	
11	1374	034570	013710	001046	MOV	WPSEC,(R0)	SET UP FOR TWO SECTOR READ	
12	1375	034574	006320		ASL	(R0)+	;	
13	1376	034576	004537	035000	JSR	R5,DSKTST	REDUCE WORD COUNT BY 316	
14	1377	034602	012700	023614	MOV	#ROBLK,R0	GET READ BLOCK ADDRESS	
15	1378	034606	004537	022700	JSR	R5,DXFER	INITIATE TWO SECTOR READ	
16	1379	034612	005737	001322	TST	ERRFLG	ANY ERRORS?	
17	1380	034616	001033		BNE	T31EX	EXIT IF YES	
18	1381	034620	013700	001050	MOV	POSWP,R0	LOAD WORD COUNT INTO R0 FOR COMPARE	
19	1382	034624	063700	001050	ADD	POSWP,R0	;	
20	1383	034630	005737	001144	TST	DKEND	END OF DISK FLAG SET?	
21	1384	034634	001402		BEO	++6	CONTINUE IF NO	
22	1385	034636	163700	001050	SUB	POSWP,R0	SUBTRACT ONE SECTOR WORD COUNT IF YES	
23	1386	034642	004537	017106	JSR	R5,DATCHP	GO COMPARE DATA	
24	1387	034646	005737	001322	TST	ERRFLG	ERROR FLAG SET?	
25	1388	034652	001015		BNE	T31EX	EXIT IF SET	
26	1389	034654	005737	001144	TST	DKEND	ARE WE DONE READING?	
27	1390	034660	001012		BNE	T31EX	READ 2 MORE SECTORS IF NOT DONE	
28	1391	034662	013737	001162	001136	MOV	ENDSEC,CURSEC	UPDATE DISK ADDRESSES
29	1392	034670	013737	001164	001140	MOV	ENDHD,CURHD	;
30	1393	034676	013737	001166	001142	MOV	ENDCYL,CURCYL	;
31	1394	034704	000663		BR	T31RLP	REPEAT READ OPERATION	
32	1395	034706	004537	003342	T31EX: JSR	R5,TSTCTL	GO ON TO NEXT TEST	
33	1396				;			
34	1397				;			
35	1398				;		DISK ADDRESS SAVE SUBROUTINE	
36	1399				;			
37	1400				;			
38	1401				;		THIS SUBROUTINE SAVES THE CURRENT SECTOR, HEAD AND	
39	1402				;		CYLINDER VALUES AT A TEMPORARY	
40	1403				;		BUFFER, #TMPADR.	
41	1404				;			
42	1405	034712	010046		ADRSAV: MOV	R0,-(SP)	SAVE R0,R1	
43	1406	034714	010146		MOV	R1,-(SP)	;	
44	1407	034716	012700	034772	MOV	#TMPADR,R0	GET TEMPORARY BUF ADDRESS	
45	1408	034722	012701	001136	MOV	#CURSEC,R1	GET CURRENT SECTOR ADDRESS	
46	1409	034726	012120		MOV	(R1)+,(R0)+	SAVE CURRENT SECTOR	
47	1410	034730	012120		MOV	(R1)+,(R0)+	SAVE CURRENT HEAD	
48	1411	034732	012120		MOV	(R1)+,(R0)+	SAVE CURRENT CYLINDER	
49	1412	034734	012601		MOV	(SP)+,R1	RESTORE R1,R0	
50	1413	034736	012600		MOV	(SP)+,R0	;	
51	1414	034740	000205		RTS	R5	RETURN	
52	1415				;			
53	1416				;			
54	1417				;			
55	1418				;		DISK ADDRESS RESTORE SUBROUTINE	
56	1419				;			
57	1420				;			
58	1421				;		THIS SUBROUTINE RESTORES THE DISK ADDRESS SECTOR,	
59	1422				;		HEAD, AND CYLINDER VALUES CONTAINED IN TMPADR.	
60	1423				;			
61	1424				;			
62	1425				;			

6	1426	034742	010046		ADDRST: MOV	RD,-(SP)	;SAVE RO,R1
7	1427	034744	010146		MOV	R1,-(SP)	;
8	1428	034746	012700	034772	MOV	#TMPADR,RO	;GET TEMPORARY BUF ADDRESS
9	1429	034752	012701	001136	MOV	#CURSEC,R1	;GET CURRENT SECTOR ADDRESS
10	1430	034756	012021		MOV	(RO)+,(R1)+	;RESTORE CURRENT SECTOR
11	1431	034760	012021		MOV	(RO)+,(R1)+	;RESTORW CURRENT HEAD
12	1432	034762	011011		MOV	(RO),(R1)	;RESTORE CURRENT CYLINDER
13	1433	034764	012601		MOV	(SP)+,R1	;RESTORE R1,RO
14	1434	034766	012600		MOV	(SP)+,RD	;
15	1435	034770	000205		RTS	R5	;RETURN
16	1436						;
17	1437						;
18	1438	034772	000000		TMPADR: .WORD 0		;CURRENT SECTOR BUFFER
19	1439	034774	000000		.WORD 0		;CURRENT HEAD
20	1440	034776	000000		.WORD 0		;CURRENT CYLINDER
21	1441						;
22	1442						;
23	1443						;
24	1444						DISK END TEST SUBROUTINE
25	1445						;
26	1446						; THIS SUBROUTINE DETERMINES WETHER THE
27	1447						; PHYSICAL END OF DISK MEDIUM WILL BE REACHED
28	1448						; IF THE OPERATION WITH CURRENT WORD COUNT IS RUN
29	1449						;
30	1450						;
31	1451						; IF THE OPERATION EXCEEDS DISK CAPACITY THE WORD
32	1452						; COUNT IS REDUCED BY 316 WORDS OR ON SECTOR
33	1453						;
34	1454						;
35	1455						; AT ENTRY RO POINTS TO THE DISK CYLINDER ADDRESS
36	1456						; IN THE OPERATION CONTROL BLOCK.
37	1457						;
38	1458						;
39	1459						;
40	1460	035000	024000		DSKTST: CMP	-(RO),RO	;POINT RO TO THE WORD COUNT REGISTER
41	1461	035002	004537	022436	JSR	R5,FNOPAR	;COMPUTE ENDING ADDRESS PARAMETERS
42	1462	035006	005737	001144	TST	DKEND	;DID WE REACH END OF DISK?
43	1463	035012	001402		BEO	+6	;EXIT IF NO
44	1464	035014	163710	001046	SUB	WPSEC,(RO)	;REDUCE WORD COUNT BY ONE SECTOR
45	1465	035020	000205		RTS	R5	;RETURN
46	1466						;
47	1467						;
48	1468						;
49	1469						;
50	1470						TEMPORARY PATCH AREA
51	1471						;
52	1472						;
53	1473	035022	000000		PTCH: .WORD 0		
54	1474		035334		. = +200.		
55	1475						;
56	1476						;
57	1477						;
58	1478						;
59	1479						;
60	1480						ERROR IMAGE BLOCK
61	1481						;
62	1482						;

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6      1483      )      THIS BLOCK CONTAINS THE CONTENTS OF ALL OF THE
1      1484      )DISK CONTROLLER REGISTERS AT THE TIME ANY ERROR IS
2      1485      )DETECTED. ERROR INFORMATION IS PLACED IN THE BLOCK
3      1486      )BY THE DXFER SUBROUTINE.
4      1487      )
5      1488      )
6      1489 035334 000000      ERRBLK:  )WORD 0      )CONTROL &STATUS REGISTER IMAGE
7      1490 035336 000000      )WORD 0      )SECTOR,UNIT,HEAD REGISTER
8      1491 035340 000000      )WORD 0      )BUS ADDRESS REGISTER
9      1492 035342 000000      )WORD 0      )WORD COUNT REGISTER
10     1493 035344 000000      )WORD 0      )CYLINDER ADDRESS REGISTER
11     1494 035346 000000      )WORD 0      )DISK STATUS REGISTER
12     1495 035350 000000      )WORD 0      )DISK ERROR REGISTER
13     1496 035352 000000      )WORD 0      )ECC BIT REGISTER
14     1497 035354 000000      )WORD 0      )ECC PATTERN REGISTER
15     1498      )
16     1499      )
17     1500      )
18     1501      )READ,WRITE AND CHECK SUBROUTINE
19     1502      )
20     1503      )      THIS SUBROUTINE WRITES THE SPECIFIED DATA BLOCK
21     1504      )ONTO THE SPECIFIED DEVICE AT THE SPECIFIED ADDRESS.
22     1505      )THE ROUTINE THEN READS THE WRITTEN DATA BACK FROM THE DISK
23     1506      )AND COMPARES THE DATA READ WITH THE ORIGINAL DATA WRITTEN.
24     1507      )
25     1508      )      CALLING SEQUENCE:
26     1509      )
27     1510      )      JSR      R5,WRC
28     1511      )
29     1512      )AT THE TIME OF THE CALL R0 MUST CONTAIN THE ORIGIN ADDRESS
30     1513      )OF THE CONTROL BLOCK DEFINING THE PARAMETERS OF THE
31     1514      )OPERATIONS TO BE PERFORMED.
32     1515      )
33     1516      )REQUIRED CONTROL BLOCK FORMAT IS AS FOLLOWS:
34     1517      )
35     1518      )      ENTRY 1 =DESIRED DUSH IMAGE
36     1519      )      ENTRY 2 = BLANK (USED BY WRC FOR DCAR IMAGE)
37     1520      )      ENTRY 3 = DESIRED DWDCNT IMAGE
38     1521      )      ENTRY 4 = DESIRED DCYL IMAGE
39     1522      )      ENTRY 5 = BLANK (USED BY WRC FOR DCSR CHD IMAGE)
40     1523      )      )RETURN PARAMETERS:
41     1524      )      1.NORMAL RETURN IS WITH GENERAL ERROR FLAG RESET.
42     1525      )      2. IF AN ERROR IS DETECTED DURING ANY OPERATION
43     1526      )CONTROL IS TRANSFERRED TO USER WITH THE ERROR FLAG SET.
44     1527      )      IN THIS CASE ERROR INFORMATION IS CONTAINED IN THE
45     1528      )      DXFER OR DATCMP ERROR FLAGS AS APPROPRIATE.
46     1529      )
47     1530      )
48     1531 035356 010046      WRC:  )MOV      R0,-(SP)      )SAVE REGISTERS
49     1532 035360 010146      )MOV      R1,-(SP)      )
50     1533 035362 010446      )MOV      R4,-(SP)      )
51     1534 035364 010546      )MOV      R5,-(SP)      )
52     1535 035366 012760 044312 000002      )MOV      #0DBUF,2(R0)      )POINT DCAR TO OUTPUT DATA BUF
53     1536 035374 012760 000006 000010      )MOV      #WRTCHD,8*(R0)      )SET UP DCSR FOR WRITE CHD
54     1537 035402 005037 001174      )CLR      WRTFRR      )RESET WRITE ERROR FLAG
55     1538 035406 004537 022700      )JSR      R5,DXFER      )PERFORM SPECIFIED WRITE OPERATION
56     1539 035412 005737 001322      )TST      ERRFLG      )ANY ERRORS?
57

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1	1540	035416	001403		BEQ	+8.	;	CONTINUE IF NO	
2	1541	035420	005237	001174	INC	WRERR	;	SET WRITE ERROR FLAG IF YES	
3	1542	035424	000430		BR	WRCEX	;	EXIT	
4	1543	035426	013701	001234	MOV	CURDSK,R1	;	GET CURRENT DISK NUMBER	
5	1544	035432	006301		ASL	R1	;	MAKE VALID INDEX VALUE	
6	1545	035434	016160	001200	000002	MOV	IBFTBL(R1),2(RD)	;	POINT DCAR TO APPROPRIATE INPUT BUF
7	1546	035442	012760	000004	000010	MOV	#RDCMD,8.(RD)	;	SET UP DCSR FOR READ COMMAND
8	1547	035450	005037	001172	CLR	RDERR	;	RESET READ ERROR FLAG	
9	1548	035454	004537	022700	JSR	R5,DAXFER	;	PERFORM DESIRED READ OPERATION	
10	1549	035460	005737	001322	TST	ERRFLG	;	ANY ERRORS?	
11	1550	035464	001403		BEQ	+8.	;	CONTINUE IF NO	
12	1551	035466	005237	001172	INC	RDERR	;	SET READ ERROR FLAG IF YES	
13	1552	035472	000405		BR	WRCEX	;	EXIT	
14	1553	035474	016000	000004	MOV	4(RD),RO	;	GET SPECIFIED WORD COUNT IN RD	
15	1554	035500	005400		NEG	RO	;	FORM POSITIVE NUMBER	
16	1555	035502	004537	017106	JSR	R5,DATCHP	;	COMPARE READ AND WRITTEN DATA	
17	1556	035506	012605		WRCEX: MOV	(SP)+,R5	;	RESTORE REGISTERS	
18	1557	035510	012604		MOV	(SP)+,R4	;		
19	1558	035512	012601		MOV	(SP)+,R1	;		
20	1559	035514	012600		MOV	(SP)+,RO	;		
21	1560	035516	000205		RTS	R5	;	RETURN	
22	1561				;				
23	1562				;				
24	1563				;				
25	1564				;			READ WRITE CONTROL BLOCK	
26	1565				;				
27	1566				;			THIS CONTROL BLOCK IS USED FOR ALL OPERATIONS	
28	1567				;			INVOLVING THE WRC SUBROUTINE.	
29	1568				;				
30	1569				;				
31	1570	035520	000000		WRCB: ;	WORD 0	;	DUSH IMAGE	
32	1571	035522	000000		;	WORD 0	;	BLANK (DBAR IMAGE)	
33	1572	035524	000000		;	WORD 0	;	DWCNT IMAGE	
34	1573	035526	000000		;	WORD 0	;	DCYL IMAGE	
35	1574	035530	000000		;	WORD 0	;	BLANK (DCSR IMAGE)	
36	1575				;				
37	1576				;				
38	1577				;				
39	1578				;				
40	1579				;				
41	1580				;				
42	1581				;				
43	1582				;				
44	1583				;				
45	1584				;				
46	1585				;				
47	1586				;				
48	1587				;				
49	1588				;				
50	1589				;				
51	1590				;				
52	1591				;				
53	1592				;				
54	1593				;				
55	1594				;				
56	1595				;				
57	1596				;				

	1597	;
1	1598	;
2	1599	;
3	1600	;
4	1601	;
5	1602	;
6	1603	;
7	1604	;
8	1605	;
9	1606	;
10	1607	;
11	1608	;
12	1609	;
13	1610	;
14	1611	;
15	1612	;
16	1613	;
17	1614	;
18	1615	;
19	1616	;
20	1617	;
21	1618	;
22	1619	;
23	1620	;
24	1621	;
25	1622	;
26	1623	;
27	1624	;
28	1625	;
29	1626	;
30	1627	;
31	1628	;
32	1629	;
33	1630	;
34	1631	;
35	1632	;
36	1633	;
37	1634	;
38	1635	;
39	1636	;
40	1637	;
41	1638	;
42	1639	;
43	1640	;
44	1641	;
45	1642	;
46	1643	;
47	1644	;
48	1645	;
49	1646	;
50	1647	;
51	1648	;
52	1649	;
53	1650	;
54	1651	;
55	1652	;
56	1653	;

READ AND COMPARE TEST

-----

THIS PROGRAM READS THE COMPLETE DISK SURFACE AND COMPARES  
DATA RECEIVED WITH REFERENCE DATA.  
BEFORE ENTERING THIS TEST IT IS ASSUMED THAT THE  
ENTIRE DISK AREA HAS BEEN WRITTEN OVER BY TEST 25.  
TEST 32 IS ESSENTIALLY THE READ PORTION OF TEST 25  
MODIFIED TO INCLUDE A DATA ERROR COUNTER FOR USE AS  
RELIABILITY TEST. SETTING SWITCH 7 OF THE  
SWITCH REGISTER UPON ENTERING THE PROGRAM INHIBITS  
PROGRAM HALT WHEN A DATA ERROR IS DETECTED. LOCATION  
ERRCNT IS INCREMENTED EACH TIME AN ERROR IS FOUND.



1	1711	035762	013700	001050	MOV	POSWP,RO	LOAD WORD COUNT		
2	1712	035766	063700	001050	ADD	POSWP,RO			
3	1713	035772	005737	001144	TST	DKEND	END OF DISK FLAG SET?		
4	1714	035776	001402		BEQ	*+6	CONTINUE IF NO		
5	1715	036000	163700	001050	SUB	POSWP,RO	REDUCE COMPARE COUNT IF END OF DISK		
6	1716	036004	004537	017106	JSR	R5,DATCHP	GO COMPARE DATA		
7	1717	036010	005737	001332	TST	RTRYIN	ARE WE IN RETRY MODE?		
8	1718	036014	001267		BNE	TN32LP	YES REREAD THE SAME SECTOR		
9	1719	036016	005737	001322	TST	ERRFLG	ANY ERRORS?		
10	1720	036022	001016		BNE	TN32EX	EXIT IF YES		
11	1721	036024	005004		CLR	R4	REINITIALIZE SUBTEST NUMBER		
12	1722	036026	005737	001144	TST	DKEND	END OF DISK?		
13	1723	036032	001012		BNE	TN32EX	EXIT IF YES		
14	1724	036034	013737	001162	001136	UPD:	MOV	ENDSEC,CURSEC	UPDATE DISK ADDRESSES
15	1725	036042	013737	001164	001140		MOV	ENDHD,CURHD	
16	1726	036050	013737	001166	001142		MOV	ENDCYL,CURCYL	
17	1727	036056	000646				BR	TN32LP	REPEAT READ SEQUENCE
18	1728	036060	004537	003342	TN32EX:	JSR	R5,TSTCTL	EXIT TO TEST CONTROL	
19	1729								
20	1730								
21	1731								
22	1732								
23	1733								
24	1734								
25	1735								
26	1736								
27	1737								
28	1738								
29	1739								
30	1740								
31	1741								
32	1742								
33	1743								
34	1744								
35	1745								
36	1746								
37	1747								
38	1748								
39	1749								
40	1750								
41	1751								
42	1752								
43	1753								
44	1754								
45	1755								
46	1756								
47	1757								
48	1758								
49	1759								
50	1760								
51	1761								
52	1762								
53	1763								
54	1764								
55	1765								
56	1766								
57	1767								

PATTERN GENERATE SUBROUTINE  
-----

THIS SUBROUTINE FORMATS THE OUTPUT DATA FOR  
FOR AN EVER INCREASING BINARY COUNT OR AN EVER  
DECREASING NEGATIVE COUNT DEPENDING ON THE  
STATE OF CNTFLG.  
THE BASE FROM WHICH THE COUNT PROGRESSES IS  
DETERMINED BY THE CONTENTS OF R1 AT THE TIME OF

```

1768 ; ENTRY,THE INCREMENTAL VALUE BETWEEN SUCCESSIVE
1769 ; LOCATIONS IS DETERMINED BY CNTINC,IF CNTINC
1770 ; IS EQUAL TO 0 THE COUNT IS INCREASING ,WHILEIT
1771 ; WILL BE DECREASING IF CNTINC IS EQUAL TO
1772 ; 1.
1773 ; THE CONTENTS OF THE PASS COUNTER IS ALSO ADDED
1774 ; TO THE INITIAL VALUE IN R1 TO CHANGE ALL OF THE
1775 ; DATA PATTERNS. ;
1776 ;
1777 ;
1778 ;
1779 ;
1780 ;
1781 ;
1782 ;
1783 036064 010046 PATGEN: MOV R0,-(SP) ;SAVE REGISTERS R0,R1,R2
1784 036066 010146 MOV R1,-(SP) ;
1785 036070 010246 MOV R2,-(SP) ;
1786 036072 063701 001236 ADD PASCNT,R1 ;CHANGE DATA PATTERN BIAS
1787 036076 005737 036140 TST CNTFLG ;IS PATTERN NEGATIVE
1788 036102 001401 BEQ +4 ;
1789 036104 005401 NEG R1 ;COMPLEMENT BASE VALUE IF NO
1790 036106 012700 044312 MOV #ODBUF,R0 ;GET OUTPUT BUFFER ORIGIN ADDRESS
1791 036112 012702 001000 MOV #512,,R2 ;ESTABLISH LOOP COUNT
1792 036116 010120 MOV R1,(R0)+ ;FORMAT ODBUF LOCATION
1793 036120 063701 036142 ADD CNTINC,R1 ;COMPUTE NEXT DATA WORD
1794 036124 005302 DEC R2 ;DECREMENT LOOP COUNTER
1795 036126 100373 BPL +-8. ;REPEAT IF NOT DONE
1796 036130 012602 MOV (SP)+,R2 ;RESTORE REGISTERS
1797 036132 012601 MOV (SP)+,R1 ;
1798 036134 012600 MOV (SP)+,R0 ;
1799 036136 000205 RTS R5 ;
1800 ;EXIT TO CALLING PROGRAM
1801 ;
1802 036140 000000 CNTFLG: 0WORD 0
1803 036142 000001 CNTINC: 0WORD 1 ;
1804 ;
1805 ;
1806 ;
1807 ;
1808 ;

```





58	036220	004537	016130	JSR	R5,RANBLK	;SET UP DISK ADDRESSES
59	036224	004537	035356	JSR	R5,WRC	;GO WRITE/READ
60	036230	005737	001322	TST	ERRFLG	;ERROR?
61	036234	001762		BEQ	\$3	;CONTINUE IF NO
62	036236	013704	001152	MOV	DTCNT,R4	;FOCRE DXFER SUBCOUNT NUMBER
63	036242	000762		BR	TN33EX	;AND EXIT
64				;		
65				;		
66				;		
67				;		
68				;		
69				;		
70				;		
71				;		
72				;		
73				;		
74				;		
75				;		
76				;		
77				;		
78				;		
79				;		
80				;		
81				;		
82				;		
83				;		
84				;		
85				;		
86				;		
87				;		
88				;		
89				;		
90				;		
91	036244	010046		REQUST: MOV	RO,-(SP)	;SAVE RO
92	036246	005004		CLR	R4	;RESET SUBTEST COUNTER
93	036250	005037	001150	CLR	INTFLG	;RESET INTERRUPT
94	036254	105777	142520	TSTB	@DCSR	;DO WE HAVE ACCESS NOW?
95	036260	100006		BPL	\$R1	;CONTINUE IF NO
96	036262	005237	001322	INC	ERRFLG	;SET ERROR FLAG IF YES
97	036266	017703	142506	MOV	@DCSR,R3	;LOAD R3 WITH ERROR CONDITION
98	036272	005002		CLR	R2	;SET R2 FOR REFERENCE WORD
99	036274	000205		RTS	R5	;AND EXIT
100	036276	005204		\$R1: INC	R4	;SUBTEST NUMBER-1(FORMATTER DEAD)
101	036300	052777	000100 142472	BIS	#INTON,@DCSR	;ENABLE INTERRUPTS AND REQUEST
102	036306	052777	000040 142464	BIS	#BITS,@DCSR	;REQUEST CONTROLLER
103	036314	004537	017342	JSR	R5,WAIT	;WAIT FOR INTERRUPT
104	036320	005737	001150	TST	INTFLG	;DID WE INTERRUPT?(COULD BE 6 SECONDS)
105	036324	001003		BNE	\$R2	;CONTINUE IF YES
106	036326	005237	001322	INC	ERRFLG	;SET ERROR FLAG IF NO
107	036332	000205		RTS	R5	;AND EXIT
108	036334	005204		\$R2: INC	R4	;SUBTEST NUMBER=2(WE DID INTERRUPT)
109	036336	005037	001150	CLR	INTFLG	;RESET INTERRUPT FLAG
110	036342	017703	142432	MOV	@DCSR,R3	;SEE IF READY IS SET
111	036346	012702	000200	MOV	#FMTRDY,R2	;SET UP R2 WITH REFERENCE WORD
112	036352	052702	000100	BIS	#INTON,R2	;INCLUDE INTERRUPT ENABLE
113	036356	052702	000040	BIS	#BITS,R2	;ALSO REQUEST BIT
114	036362	030203		BIT	R2,R3	;ARE THESE BITS SET?

## CONTROLLER REQUEST ROUTINE

\*\*\*\*\*

THIS ROUTINE REQUESTS ACCESS TO THE  
211 CONTROLLER AND WHEN COMMAND IS RECEIVED,  
ISSUES A WRITE AND READ SEQUENCE. THESE COMMANDS  
ARE ALL INTERRUPT DRIVEN AND ERRORS ARE  
CHECKED.

1	115	036364	001003			BNE	SR3		CONTINUE IF YES
2	116	036366	005237	001322		INC	ERRFLG		SET ERROR FLAG IF NO
3	117	036372	000205			RTS	R5		AND EXIT
4	118	036374	005204			SR3: INC	R4		SUBTEST NUMBER=3(READY SET, INTERRUPT
5	119								ENABLE SET AND NO ERRORS.
6	120	036376	012700	035520		MOV	#WRCB,R0		POINT R0 TO WRITE/READ BLOCK
7	121	036402	004537	016042		JSR	R5,FIUNIT		SEARCH FOR ACTIVE DISK DRIVES
8	122	036406	004537	016130		JSR	R5,RANBLK		SET UP DISK ADDRESSES
9	123	036412	004537	035356		JSR	R5,WRC		GO DO SOMETHING
10	124	036416	005737	001322		TST	ERRFLG		ERRORS?
11	125	036422	001001			BNE	SR4		CLEAR REQUEST IF YES
12	126	036424	005204			INC	R4		SUBTEST NUMBER=4(NO ERRORS)
13	127	036426	042777	000040	142344	SR4: BIC	#BITS,@DCSR		LET GO OF CONTROLLER
14	128	036434	042777	000100	142336	BIC	#INTON,@DCSR		DISABLE INTERRUPTS
15	129	036442	017703	142332		MOV	@DCSR,R3		FETCH DCSR
16	130	036446	005062			CLR	R2		SET REFERENCE WORD=0
17	131	036450	020203			CHP	R2,R3		BITS CLEARED?
18	132	036452	001402			BEQ	SR5		EXIT IF YES
19	133	036454	005237	001322		INC	ERRFLG		SET ERROR FLAG IF NO
20	134	036460	012600			SR5: MOV	(SP)+,R0		RESTORE R0
21	135	036462	000205			RTS	R5		AND EXIT
22	136								
23	137								
24	138								
25	139								
26	140								
27	141								
28	142								
29	143								
30	144								
31	145								
32	146								
33	147								
34	148								10M.ECC TEST NUMBERS A16 >> A17 13-NOV-77
35	149								
36	150								
37	151								
38	152								
39	153								
40	154								TNA16.PH -NOV-77
41	155								
42	156								
43	157								
44	158								ECC REGISTER CHECKS
45	159								-----
46	160								
47	161								
48	162								
49	163								THESE TESTS CHECK THE ECC REGISTER (PATTERN)
50	164								FOR LOADING THE ECC INHIBIT BIT AS WELL AS INITIALIZATION
51	165								OF BOTH THE ECC PATTERN REGISTER AND THE ECC BIT COUNT
52	166								REGISTER.
53	167								
54	168								
55	169								
56	170								
57	171	036464	005004			TNA16: CLR	R4		SUBTEST NUMBER=0

172	036466	004537	004276		JSR	R5,RQEST	};REQUEST USE OF THE 211
173	036472	000005			RESET		};ISSUE I/O RESET
174	036474	004537	004276		JSR	R5,RQEST	};FETCH 211 AGAIN
175	036500	005002			CLR	R2	};SET UP REFERENCE WORD
176	036502	017703	142310		MOV	@ECCPB,R3	};FETCH ECC POSITION REGISTER
177	036506	020203			CMP	R2,R3	};CLEARED?
178	036510	001404			BEQ	CECC1	};CONTINUE IF YES
179	036512	005237	001322		INC	ERRFLG	};SET ERROR FLAG IF NO
180	036516	000137	036770		JMP	TNA16EX	};AND EXIT
181	036522	005204		CECC1:	INC	R4	};SUBTEST NUMBER=1(ECCPB OK)
182	036524	017703	142270		MOV	@ECCPW,R3	};FETCH ECC BIT PATTERN REGISTER
183	036530	020203			CMP	R2,R3	};CLEARED?
184	036532	001404			BEQ	CECC2	};CONTINUE IF YES
185	036534	005237	001322		INC	ERRFLG	};SET ERROR FLAG IF NO
186	036540	000137	036770		JMP	TNA16EX	};AND EXIT
187	036544	005204		CECC2:	INC	R4	};SUBTEST NUMBER=(ECC BIT PATTERN OK)
188	036546	012777	100000	142244	MOV	#BIT15,@ECCPW	};LOAD ECC INHIBIT BIT
189	036554	012702	100000		MOV	#BIT15,R2	};LOAD REFERENCE WORD
190	036560	017703	142234		MOV	@ECCPW,R3	};FETCH ECCPW>>R3
191	036564	020203			CMP	R2,R3	};BIT SEY?
192	036566	001404			BEQ	CECC3	};CONTINUE IF YES
193	036570	005237	001322		INC	ERRFLG	};SET ERROR FLAG IF NO
194	036574	000137	036770		JMP	TNA16EX	};AND EXIT
195	036600	005204		CECC3:	INC	R4	};SUBTEST NUMBER=3(BIT 15 OK,ECCPW)
196	036602	005002			CLR	R2	};SET UP REFERENCE WORD
197	036604	005077	142210		CLR	@ECCPW	};ATTEMPT TO CLEAR BIT 15
198	036610	017703	142204		MOV	@ECCPW,R3	};FETCH FOR COMPARE
199	036614	020203			CMP	R2,R3	};BIT CLEARED?
200	036616	001404			BEQ	CECC4	};CONTINUE IF YES
201	036620	005237	001322		INC	ERRFLG	};SET ERROR FLAG IF NO
202	036624	000137	036770		JMP	TNA16EX	};EXIT
203	036630	005204		CECC4:	INC	R4	};SUBTEST NUMBER=4(BIT 15 CLEARED)
204	036632	012777	100000	142160	MOV	#BIT15,@ECCPW	};RELOAD BIT 15
205	036640	052777	000077	142132	BIS	#NOFCMD,@DCSR	};ISSUE NOP COMMAND TO CLEAR BIT
206	036646	017703	142146		MOV	@ECCPW,R3	};SET UP FOR COMPARE
207	036652	012702	100000		MOV	#BIT15,R2	};SET UP REFERENCE IN R2
208	036656	020203			CMP	R2,R3	};BIT NO-OPPED OUT?
209	036660	001404			BEQ	CECC5	};CONTINUE IF NO
210	036662	005237	001322		INC	ERRFLG	};SET ERROR FLAG IF NO
211	036666	000137	036770		JMP	TNA16EX	};AND EXIT
212	036672	005204		CECC5:	INC	R4	};SUBTEST NUMBER=5(60 DOESN'T CLEAR ERROR)
213	036674	012777	100000	142116	MOV	#BIT15,@ECCPW	};LOAD BIT 15 AGAIN
214	036702	012777	000041	142070	MOV	#SYSCLR BIT15,@DCSR	};ISSUE SYSTEM CLEAR
215	036710	004537	004276		JSR	R5,RQEST	};REQUEST 211 AGAIN
216	036714	017703	142100		MOV	@ECCPW,R3	};SET UP FOR COMPARE
217	036720	005002			CLR	R2	};SET UP REFERENCE WORD
218	036722	020203			CMP	R2,R3	};CLEARED?
219	036724	001404			BEQ	CECC6	};CONTINUE IF YES
220	036726	005237	001322		INC	ERRFLG	};SET ERROR FLAG IF NO
221	036732	000137	036770		JMP	TNA16EX	};AND EXIT
222	036736	005204		CECC6:	INC	R4	};SUBTEST NUMBER=6(SYSCLR CLEARS ERROR BIT)
223	036740	012777	100000	142052	MOV	#BIT15,@ECCPW	};LOAD BIT 15 ONE LAST TIME
224	036746	000005			RESET		};ISSUE I/O RESET
225	036750	004537	004276		JSR	R5,RQEST	};REQUEST FORMATTER AGAIN
226	036754	017703	142040		MOV	@ECCPW,R3	};SET UP FOR COMPARE
227	036760	020203			CMP	R2,R3	};CLEARED?
228	036762	001402			BEQ	TNA16EX	};EXIT IF YES

6	229	036764	005237	001322	INC	ERRFLG	SET ERROR FLAG IF NO
1	230	036770	004537	003342	TNA16EX:JSR	R5,TSCTL	JAND EXIT EITHER WAY
2	231						
3	232						
4	233						
5	234						
6	235						
7	236						
8	237						
9	238						
10	239						
11	240						
12	241						
13	242						
14	243						
15	244						
16	245						
17	246						
18	247						
19	248						
20	249						
21	250						
22	251				TNA17,PH	1-NOV-77	
23	252						
24	253						
25	254					ECC/211 HEADER FORMAT	
26	255					*****	
27	256						
28	257						
29	258					THE FOLLOWING DRAWING IS THE HEADER ARRANGEMENT	
30	259					FOR THE PHOENIX 211 CONTROLLER EQUIPTED WITH ECC LOGIC	
31	260					THESE CONTROLLERS HAVE A REDUNDANT SET OF HEADER WORDS	
32	261					ADDED TO THE SECTOR TO INSURE PERFECT DISK PACKS	
33	262					IF THERE IS A BAD SPOT(S) ON A DISK IN THE HEADER FIELD AREA	
34	263					THE CONTROLLER WILL ERROR ONLY IF BOTH HEADERS ARE DETECTED	
35	264					AS BAD.	
36	265						
37	266						
38	267						
39	268						
40	269					*****	
41	270					* WORD1 * WORD2 * CRC1 * CRC2 * WORD3 * WORD4 * CRC1 * CRC2 *	
42	271					* PAIR1 * PAIR1 * PAIR1 * PAIR1 * PAIR2 * PAIR2 * PAIR2 * PAIR2 *	
43	272					*****	
44	273						
45	274						
46	275						
47	276						
48	277						
49	278						
50	279						
51	280						
52	281					ECC/CRC DETECTION TEST	
53	282					-----	
54	283						
55	284					THESE TESTS CHECK THE HEADER CRC	
56	285					DETECTION AS WELL AS THE COMPATIBILITY	
57						OF THE CONTROLLER UNDER TEST.	



1	343	037262	005204			CRC7:	INC	R4		;}SUBTEST NUMBER=7(BUSS ADDR.--NO INCREMENTATION)
2	344	037264	017703	141512			MOV	0DUSH,R3		;}FETCH UNIT-SECTOR-HEAD REGISTER
3	345	037270	011002				MOV	(R0),R2		;}FETCH ORIGINAL VALUE
4	346	037272	042703	030000			BIC	#30000,R3		;}LOOSE UNIT SELECT BITS IN BOTH
5	347	037276	042702	030000			BIC	#30000,R2		;
6	348	037302	005202				INC	R2		;}MAKE R2 REFERENCE(ORIG+1)
7	349	037304	020203				CMF	R2,R3		;}DID SECTOR ADDR BUMP?(SHOULD HAVE)
8	350	037306	001402				BEO	CRC10		;}CONTINUE IF YES
9	351	037310	000137	040614			JMP	CRCXEX		;}EXIT IF NO
10	352	037314	005204			CRC10:	INC	R4		;}SUBTEST=10(SECTOR ADDR =.+1)
11	353	037316	005037	001322			CLR	ERRFLG		;}FINALLY RESET ERROR FLAG
12	354	037322	012700	025450			MOV	#ISECFB,R0		;}POINT R0 TO FORMAT BLOCK
13	355	037326	005010				CLR	(R0)		;}SECTOR,HEAD 0
14	356	037330	005037	044306			CLR	ODBUF-4		;}MAKE VALID HEADER WORDS
15	357	037334	005037	044310			CLR	ODBUF-2		;
16	358	037340	005237	001176			INC	SPECHD		;}SET SPECIAL COMMAND FLAG
17	359	037344	004537	022700			JSR	R5,DXFER		;}REFDRMAT SECTOR 0
18	360	037350	005037	001176			CLR	SPECHD		;}RESET SPECIAL COMMAND FLAG
19	361	037354	005737	001322			TST	ERRFLG		;}ERRORS DURING FORMAT
20	362	037360	001402				BEO	CRC11		;}CONTINUE IF NO
21	363	037362	000137	040614			JMP	CRCXEX		;}EXIT IF YES
22	364	037366	005204			CRC11:	INC	R4		;}SUBTEST NUMBER=11(REFORMAT SECTOR 0 OK)
23	365	037370	005210				INC	(R0)		;}POINT TO SECTOR 1
24	366	037372	004537	004034			JSR	R5,CLRBUF		;}CLEAR BUFFER AREA
25	367	037376	012737	000001	044306		MOV	#1,ODBUF-4		;}MAKE VALID HEADER WORD 1
26	368	037404	012737	000001	044312		MOV	#1,ODBUF		;}MAKE SECOND PAIR VALID
27	369	037412	005037	044310			CLR	ODBUF-2		;
28	370	037416	005237	001176			INC	SPECHD		;}SET SPECIAL COMMAND FLAG
29	371	037422	004537	022700			JSR	R5,DXFER		;}REFORMAT SECTOR
30	372	037426	005037	001176			CLR	SPECHD		;}RESET SPECIAL COMMAND FLAG
31	373	037432	005010				CLR	(R0)		;}SECTOR ADDR BACK TO ZERO
32	374	037434	005737	001322			TST	ERRFLG		;}ERROR?
33	375	037440	001402				BEO	CRC12		;}CONTINUE IF NO
34	376	037442	000137	040614			JMP	CRCXEX		;}EXIT IF YES
35	377	037446	005204			CRC12:	INC	R4		;}SUBTEST NUMBER=12(FORMAT SECTOR 1 OK)
36	378	037450	012700	023614			MOV	#RDBLK,R0		;}POINT TO READ BLOCK
37	379	037454	005210				INC	(R0)		;}MAKE READ FROM SECTOR 0
38	380	037456	004537	022700			JSR	R5,DXFER		;}READ
39	381	037462	005010				CLR	(R0)		;}RESET SECTOR ADDRESS
40	382	037464	005737	001322			TST	ERRFLG		;}ERRORS DURING READ?
41	383	037470	001402				BEO	CRC13		;}CONTINUE IF NO
42	384	037472	000137	040614			JMP	CRCXEX		;}EXIT IF YES
43	385	037476	005204			CRC13:	INC	R4		;}SUBTEST NUMBER=13(READ ON SECTOR 1 OK)
44	386	037500	012700	040632			MOV	#RDCDE,R0		;}POINT TO READ EVERYTHING BLOCK
45	387	037504	005210				INC	(R0)		;}MAKE IT SECTOR 1
46	388	037506	013702	001234			MOV	CURDSK,R2		;}SET UP INPUT FIELD
47	389	037512	006302				ASL	R2		;
48	390	037514	016260	001200	000002		MOV	IBFTBL(R2),2(R0)		;}FOR READ
49	391	037522	013700	001046	000004		MOV	WPSEC,4(R0)		;}ADJUST WORD COUNT
50	392	037530	162760	000012	000004		SUB	#10,4(R0)		;}ADJUST WORD COUNT
51	393	037536	005237	001176			INC	SPECHD		;}SET COMMAND FLAG
52	394	037542	004537	022700			JSR	R5,DXFER		;}READ BALL GAME
53	395	037546	005010				CLR	(R0)		;}RESET SECTOR ADDRESS
54	396	037550	005037	001176			CLR	SPECHD		;}RESET COMMAND FLAG
55	397	037554	005737	001322			TST	ERRFLG		;}ERRORS?
56	398	037560	001402				BEO	CRC14		;}CONTINUE IF NO
57	399	037562	000137	040614			JMP	CRCXEX		;}EXIT IF YES

6	400	037566	005204					CRC14:	INC	R4		;SUBTEST NUMBER=14(READ CRC OK)
7	401	037570	016002	000002					MOV	2(R0),R2		;SET R2 FOR POINTER TO CRC WORD(S)
8	402	037574	016203	000004					MOV	4(R2),R3		;FETCH FIRST CRC WORD
9	403	037600	013702	001260					MOV	HDRC1,R2		;FETCH REFERENCE WORD
10	404	037604	020203						CMP	R2,R3		;COMPATIBLE CRC GENERATION?
11	405	037606	001404						BEO	CRC15		;CONTINUE IF YES
12	406	037610	005237	001322					INC	ERRFLG		;SET ERROR FLAG IF NO
13	407	037614	000137	040614					JMP	CRCXEX		;AND EXIT
14	408	037620	005204					CRC15:	INC	R4		;SUBTEST NUMBER=15(FIRST CRC WORD OK)
15	409	037622	016001	000002					MOV	2(R0),R1		;COMPUTE ADDRESS FOR SECONC CRC WORD
16	410	037626	016103	000006					MOV	6(R1),R3		;LOAD SECOND CRC WORD
17	411	037632	013702	001262					MOV	HDRC2,R2		;FETCH REFERENCE WORD
18	412	037636	020203						CMP	R2,R3		;NEW WORD COMPATIBLE?
19	413	037640	001404						BEO	CRC16		;CONTINUE IF YES
20	414	037642	005237	001322					INC	ERRFLG		;EXIT IF NO
21	415	037646	000137	040614					JMP	CRCXEX		;EXIT WITH ERROR
22	416	037652	005204					CRC16:	INC	R4		;SUBTEST NUMBER=16(SECOND CRC WORD COMPATIBLE
23	417											;THESE LAST TWO SUBTESTS(15+16)
24	418											;ARE USED TO DETERMINE IF THE CRC/ECC
25	419											;GENERATOR ON THE FORMATTER BEING
26	420											;TESTED IS COMPATIBLE WITH ALL OTHER
27	421											;OTHER PHOENIX 211/200 CONTROLLERS.
28	422	037654	016102	000004					MOV	4(R1),R2		;NOW SETUP TO CHECK SECOND PAIR OF HDR CRC'S
29	423	037660	016103	000014					MOV	14(R1),R3		;FOR COMPATIBILITY
30	424	037664	020203						CMP	R2,R3		;SAME VALUE?
31	425	037666	001404						BEO	CRC17		;CONTINUE IF YES
32	426	037670	005237	001322					INC	ERRFLG		;SET ERROR FLAG IF NO
33	427	037674	000137	040614					JMP	CRCXEX		;AND EXIT
34	428	037700	005204					CRC17:	INC	R4		;SUBTEST NUMBER=17(FIRST WORD COMPATIBE)
35	429	037702	016102	000006					MOV	6(R1),R2		;FETCH SECOND CRC WORD
36	430	037706	016103	000016					MOV	16(R1),R3		;FOR SAME
37	431	037712	020203						CMP	R2,R3		;SECOND WORD OK?
38	432	037714	001404						BEO	CRC20		;CONTINUE IF YES
39	433	037716	005237	001322					INC	ERRFLG		;SET ERROR FLAG IF NO
40	434	037722	000137	040614					JMP	CRCXEX		;AND EXIT
41	435	037726	005204					CRC20:	INC	R4		;SUBTEST NUMBER=20(SECOND WORD OK)
42	436	037730	012700	040620					MOV	#ECCWRT,R0		;POINT TO WRITE BLOCK
43	437	037734	005010						CLR	(R0)		;SECTOR ADDR.=0
44	438	037736	016001	000002					MOV	2(R0),R1		;POINT R0 BUFFER AREA
45	439	037742	004537	004034					JSR	R5,CLRBUF		;ZERO BUFFERS
46	440	037746	012761	100000	000004				MOV	#BIT15,4(R1)		;MAKE LAST BIT OF FIRST CRC WORDS A 1
47	441	037754	012761	100000	000014				MOV	#BIT15,14(R1)		;BOTH MUST BE SET TO CAUSE AN ERROR
48	442	037762	013760	001046	000004				MOV	#PSEC,4(R0)		;ADJUST WORD COUNT FOR +ONE SECTOR
49	443	037770	162760	000012	000004				SUB	#10,4(R0)		;INCLUDE HDRS+CRC+ECC WORDS
50	444	037776	005237	001176					INC	SPECMD		;SET SPECIAL COMMAND FLAG
51	445	040002	004537	022700					JSR	R5,DXFER		;WRITE NEW FIELD
52	446	040006	005037	001176					CLR	SPECMD		;CLEAR SPECIAL COMMAND FLAG
53	447	040012	005737	001322					TST	ERRFLG		;ERRORS?
54	448	040016	001402						BEO	CRC21		;CONTINUE IF NO
55	449	040020	000137	040614					JMP	CRCXEX		;EXIT IF YES
56	450	040024	005204					CRC21:	INC	R4		;SUBTEST NUMBER=21(COMPATIBLE)
57	451	040026	012700	023614					MOV	#RDBLK,R0		;POINT TO READ BLOCK
58	452	040032	004537	022700					JSR	R5,DXFER		;ATTEMPT READ ON SECTOR 0
59	453	040036	005737	001322					TST	ERRFLG		;ERRORS?(SHOULD BE)
60	454	040042	001004						BNE	CRC22		;CONTINUE IF YES
61	455	040044	005237	001322					INC	ERRFLG		;SET ERROR FLAG IF NO
62	456	040050	000137	040614					JMP	CRCXEX		;AND EXIT



1	457	040054	005204		CRC22:	INC	R4		);SUBTEST NUMBER=22(ERROR DETECTED)
2	458	040056	017703	140732		MOV	@DERR,R3		);FETCH ERROR REGISTER
3	459	040062	042703	177376		BIC	#177376,R3		);EXTRACT HDR CRC ERROR
4	460	040066	012702	000401		MOV	#BIT8:BIT0,R2		);SET UP REFERENCE WORD
5	461	040072	020203			CHP	R2,R3		);ARE THE EQUAL?
6	462	040074	001402			BEP	CRC23		);CONTINUE IF YES
7	463	040076	000137	040614		JMP	CRCXEX		);EXIT IF NO
8	464	040102	005204		CRC23:	INC	R4		);SUBTEST NUMBER=23(CRCERROR DETECTED)
9	465	040104	005037	001322		CLR	ERRFLG		);RESET ERROR FLAG
10	466	040110	004537	004034		JSR	R5,CLRBUF		);ZERO BUFFERS
11	467	040114	012700	040620		MOV	#ECCWRT,R0		);POINT TO WRITE BLOCK
12	468	040120	016001	000002		MOV	2(R0),R1		);USE R1 TO POINT TO BUFFERS
13	469	040124	012761	000001	000006	MOV	#BIT0:6(R1)		);MAKE FIRST BIT OF SECOND WORDS A 1
14	470	040132	012761	000001	000016	MOV	#BIT0:16(R1)		);BOTH WORDS AGAIN
15	471	040140	005237	001176		INC	SPECHD		);SET SPECIAL COMMAND FLAG
16	472	040144	004537	022700		JSR	R5,DXFER		);REFORMAT
17	473	040150	005037	001176		CLR	SPECHD		);RESET COMMAND FLAG
18	474	040154	005737	001322		TST	ERRFLG		);ERRORS?
19	475	040160	001402			BEO	CRC24		);CONTINUE IF NO
20	476	040162	000137	040614		JMP	CRCXEX		);EXIT IF ERROR
21	477	040166	005204		CRC24:	INC	R4		);SUBTEST NUMBER=24(REWRITE OK)
22	478	040170	012700	023614		MOV	#RDBLK,R0		);POINT TO READ BLOCK ADDRESS
23	479	040174	004537	022700		JSR	R5,DXFER		);READ SECTOR
24	480	040200	005737	001322		TST	ERRFLG		);ERROR?
25	481	040204	001004			BNE	CRC25		);CONTINUE IF YES
26	482	040206	005237	001322		INC	ERRFLG		);SET IT IF NOT
27	483	040212	000137	040614		JMP	CRCXEX		);AND EXIT
28	484	040216	005204		CRC25:	INC	R4		);SUBTEST NUMBER=25(ERROR DETECTED)
29	485	040220	017703	140570		MOV	@DERR,R3		);FETCH ERROR REGISTER
30	486	040224	012702	000401		MOV	#BIT8:BIT0,R2		);SET UP REFERENCE WORD IN R2
31	487	040230	020203			CHP	R2,R3		);CRC ERROR?
32	488	040232	001402			BEO	CRC26		);CONTINUE IF YES
33	489	040234	000137	040614		JMP	CRCXEX		);EXIT IF NOT
34	490	040240	005204		CRC26:	INC	R4		);SUBTEST NUMBER=26(CRC DETECTED)
35	491	040242	005037	001322		CLR	ERRFLG		);RESET ERROR FLAG NOW
36	492	040246	012700	040620		MOV	#ECCWRT,R0		);FETCH WRITE BLOCK ADDR AGAIN
37	493	040252	016001	000002		MOV	2(R0),R1		);USE R1 TO POINT TO WRITE BUFFER
38	494	040256	005061	000004		CLR	4(P1)		);CLEAR FIRST HEADER(VALIDATE)
39	495	040262	005061	000014		CLR	14(R1)		);BOTH SETS
40	496	040266	012761	100000	000006	MOV	#BIT15:6(R1)		);MAKE LAST BIT OF CRC A 1
41	497	040274	012761	100000	000016	MOV	#BIT15:16(R1)		);BOTH SETS
42	498	040302	005237	001176		INC	SPECHD		);SET SPECIAL COMMAND FLAG
43	499	040306	004537	022700		JSR	R5,DXFER		);REWRITE SECTOR
44	500	040312	005037	001176		CLR	SPECHD		);RESET FLAG
45	501	040316	005737	001322		TST	ERRFLG		);ERRORS?
46	502	040322	001402			BEO	CRC27		);CONTINUE IF NO
47	503	040324	000137	040614		JMP	CRCXEX		);EXIT IF YES
48	504	040330	005204		CRC27:	INC	R4		);SUBTEST NUMBER=27(REWRITE OK)
49	505	040332	012700	023614		MOV	#RDBLK,R0		);POINT TO READ BLOCK ADDR
50	506	040336	004537	022700		JSR	R5,DXFER		);ATTEMPT READ
51	507	040342	005737	001322		TST	ERRFLG		);ERRORS?
52	508	040346	001004			BNE	CRC30		);CONTINUE IF YES
53	509	040350	005237	001322		INC	ERRFLG		);SET ERROR FLAG IF NOT
54	510	040354	000137	040614		JMP	CRCXEX		);AND EXIT
55	511	040360	005204		CRC30:	INC	R4		);SUBTEST NUMBER=30(ERROR DETECTED)
56	512	040362	017703	140426		MOV	@DERR,R3		);FETCH ERROR REGISTER
57	513	040366	012702	000401		MOV	#BIT8:BIT0,R2		);SET UP REFERENCE

6	514	040372	020203		CMP	R2,R3	);CONTINUE IF YES
7	515	040374	001402		BEQ	CRC31	);CONTINUE IF YES
8	516	040376	000137	040614	JMP	CRCXEX	);EXIT IF NO
9	517	040402	005204		CRC31: INC	R4	);SUBTEST NUMBER=31(CRC ERROR)
10	518	040404	005037	001322	CLR	ERRFLG	);RESET ERROR FLAG
11	519	040410	012700	025450	MOV	#ISECFB,R0	);POINT TO FORMAT BLOCK
12	520	040414	004537	004034	JSR	R5,CLRBUF	);ZERO BUFFERS
13	521	040420	005237	001176	INC	SPECMD	);SET SPECIAL COMMAND FLAG
14	522	040424	004537	022700	JSR	R5,DXFER	);REFORMAT
15	523	040430	005037	001176	CLR	SPECMD	);RESET COMMAND FLAG
16	524	040434	005737	001322	TST	ERRFLG	);ERROR DURING FORMAT?
17	525	040440	001402		BEQ	CRC32	);CONTINUE IF NO
18	526	040442	000137	040614	JMP	CRCXEX	);EXIT IF YES
19	527	040446	005204		CRC32: INC	R4	);SUBTEST NUMBER=32(REFORMAT OK)
20	528	040450	012700	040632	MOV	#RDCDE,R0	);POINT TO READ BLOCK
21	529	040454	005237	001176	INC	SPECMD	);SET SPECIAL COMMAND FLAG
22	530	040460	004537	022700	JSR	R5,DXFER	);READ SECTOR
23	531	040464	005037	001176	CLR	SPECMD	);RESET COMMAND FLAG
24	532	040470	005737	001322	TST	ERRFLG	);ERRORS?
25	533	040474	001402		BEQ	CRC33	);CONTINUE IF NO
26	534	040476	000137	040614	JMP	CRCXEX	);EXIT IF YES
27	535	040502	005204		CRC33: INC	R4	);SUBTEST NUMBER=33(READ OK)
28	536	040504	016001	000002	MOV	2(R0),R1	);POINT TO BUFFER WITH R1
29	537	040510	016103	000004	MOV	4(R1),R3	);FETCH FIST CRC WORD
30	538	040514	005002		CLR	R2	);SET UP REFERENCE
31	539	040516	020203		CMP	R2,R3	);EQUAL?
32	540	040520	001404		BEQ	CRC34	);CONTINUE IF YES
33	541	040522	005237	001322	INC	ERRFLG	);SET ERROR FLAG IF NO
34	542	040526	000137	040614	JMP	CRCXEX	);AND EXIT
35	543	040532	005204		CRC34: INC	R4	);SUBTEST NUMBER=34(FIRST WORD OK)
36	544	040534	016103	000006	MOV	6(R1),R3	);FETCH SECOND WORD
37	545	040540	020203		CMP	R2,R3	);SECOND WORD OK?
38	546	040542	001404		BEQ	CRC35	);CONTINUE IF YES
39	547	040544	005237	001322	INC	ERRFLG	);SET ERROR FLAG IF NO
40	548	040550	000137	040614	JMP	CRCXEX	);AND EXIT
41	549	040554	005204		CRC35: INC	R4	);SUBTEST NUMBER=35(SECOND WORD OK)
42	550	040556	016103	000014	MOV	14(R1),R3	);FETCH THIRD WORD
43	551	040562	020203		CMP	R2,R3	);OK?
44	552	040564	001404		BEQ	CRC36	);CONTINUE IF YES
45	553	040566	005237	001322	INC	ERRFLG	);SET ERROR FLAG IF NO
46	554	040572	000137	040614	JMP	CRCXEX	);AND EXIT
47	555	040576	005204		CRC36: INC	R4	);SUBTEST NUMBER=36(THIRD WORD OK)
48	556	040600	016103	000016	MOV	16(R1),R3	);FETCH FOURTH WORD
49	557	040604	020203		CMP	R2,R3	);OK?
50	558	040606	001402		BEQ	CRCXEX	);EXIT IF YES
51	559	040610	005237	001322	INC	ERRFLG	);SET ERROR FLAG IF NO
52	560	040614	004537	003342	CRCXEX: JSR	R5,TSTCTL	);EXIT HERE
53	561				;		
54	562				;		
55	563				;		
56	564				;	CRC / ECC TEST COMMAND BLOCKS	
57	565				;	-----	
58	566				;		
59	567				;		
60	568	040620	000000		ECCWRT: .WORD 0		);DUSH=0
61	569	040622	044312		.WORD 0DBUF		);OUTPUT BUFFER=0DBUF
62	570	040624	177400		.WORD 177400		);WORD COUNT -FLEXIBLE

```

571 040626 000000          .WORD 0          ;CYLINDER ADDR=0
572 040630 000014          .WORD VHSCRC      ;WRITE THE BALL GAME COMMAND
573                          ;
574                          ;
575                          ;
576                          ;
577 040632 000000          RDCDE: .WORD 0          ;DUSH=0
578 040634 047314          .WORD IDBUFT      ;INPUT BUFFER-FLEXIBLE
579 040636 1774U0          .WORD 177400      ;WORD COUNT-FLEXIBLE
580 040640 000000          .WORD 0          ;CYLINDER ADDR=0
581 040642 000012          .WORD RDFMT       ;READ BALL GAME COMMAND
582                          ;
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ECC SECTOR FORMAT AND READ ROUTINE

THIS ROUTINE ISSUES 4 DISK COMMANDS DURING THE ECC TEST SEQUENCE. THE GENERAL FUNCTION OF THE EXERCISE IS TO FORCE ECC ERRORS BY DESTROYING A SMALL SECTION OF A SECTOR BY USING THE WRITE HEADER, CRC, DATA AND ECC COMMAND. THE OPERATOR CAN SELECT THE AREA IN THE DATA FIELD WHERE HE DESIRES TO CAUSE THE ERROR. THE STEPS TO ACCOMPLISH THIS ARE AS FOLLOWS:

1. USING THE NORMAL WRITE COMMAND, WRITE A SINGLE SECTOR. EXECUTING THIS COMMAND WILL CAUSE ECC WORDS TO BE GENERATED.
2. READ THE SECTOR USING THE READ FORMAT COMMAND THIS COMMAND READS THE ENTIRE SECTOR, INCLUDING HEADERS, HEADER CRC'S, DATA AND ECC WORDS
3. REWRITE THE SECTOR AFTER CHANGING DESIRED DATA WORD(FROM 1 TO 16 BITS).
4. ISSUE NORMAL READ ON THAT SECTOR TO CAUSE ECC ERROR.
5. EXIT ROUTINE.

CALLING SEQUENCE:

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(X) JSR R5,WRTECC ;PROGRAM CALL
(X+2) .WORD 0 ;DATA PATTERN DESIRED(ENTIRE SECTOR)
(X+4) .WORD 0 ;WORD POSITION(X2)

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6	799	041340	005737	001322	TST	ERRFLG	ERROR SET?
1	800	041344	001402		BEQ	ECCD10	CONTINUE IF NO
2	801	041346	000137	041642	JMP	ECCDEX	EXIT IF YES
3	802	041352	005204		ECCD10: INC	R4	SUBTEST NUMBER=10(NO ERROR ALL ONES)
4	803	041354	004537	040644	JSR	R5,VRTECC	NOW FIRST BIT A ZERO
5	804	041360	177777		.WORD	177777	SECTOR ALL ONES
6	805	041362	000000		.WORD	0	FIRST WORD
7	806	041364	177776		.WORD	177776	LOSE BIT 0
8	807	041366	005737	001322	TST	ERRFLG	ERRORS?
9	808	041372	001002		BNE	ECCD11	CONTINUE IF YES
10	809	041374	000137	041642	JMP	ECCDEX	AND EXIT
11	810	041400	005204		ECCD11: INC	R4	SUBTEST NUMBER=11(PICKED UP FIRST ZERO
12	811	041402	004537	041652	JSR	R5,ECCERR	NOW CHECK ERROR BIT
13	812	041406	005737	001322	TST	ERRFLG	ERROR OK?
14	813	041412	001402		BEQ	ECCD12	CONTINUE IF YES
15	814	041414	000137	041642	JMP	ECCDEX	EXIT IF NO
16	815	041420	005204		ECCD12: INC	R4	SUBTEST NUMBER=12(ERROR BIT OK)
17	816	041422	004537	040644	JSR	R5,VRTECC	NOW TRY LAST BIT
18	817	041426	177777		.WORD	177777	SECTOR ALL ONES
19	818	041430	000776		.WORD	776	LAST WORD
20	819	041432	077777		.WORD	77777	LAST BIT
21	820	041434	005737	001322	TST	ERRFLG	ERROR?
22	821	041440	001002		BNE	ECCD13	CONTINUE IF YES
23	822	041442	000137	041642	JMP	ECCDEX	EXIT IF NO
24	823	041446	005204		ECCD13: INC	R4	SUBTEST NUMBER=13(LAST BIT ERRORED)
25	824	041450	004537	041652	JSR	R5,ECCERR	CHECK ERROR BIT
26	825	041454	005737	001322	TST	ERRFLG	ERRORS OK?
27	826	041460	001402		BEQ	ECCD14	CONTINUE IF YES
28	827	041462	000137	041642	JMP	ECCDEX	EXIT IF NO
29	828	041466	005204		ECCD14: INC	R4	SUBTEST NUMBER=14(ERROR BIT OK)
30	829	041470	004537	040644	JSR	R5,VRTECC	TRY MIDDLE OF SECTOR
31	830	041474	177777		.WORD	177777	SECTOR ALL ONES
32	831	041476	000376		.WORD	376	MIDDLE WORD
33	832	041500	177377		.WORD	177377	LOSE BIT 7
34	833	041502	005737	001322	TST	ERRFLG	ERROR SET?
35	834	041506	001002		BNE	ECCD15	CONTINUE IF YES
36	835	041510	000137	041642	JMP	ECCDEX	EXIT IF NOT
37	836	041514	005204		ECCD15: INC	R4	SUBTEST NUMBER=15(MIDDLE ZERO ERR)
38	837	041516	004537	041652	JSR	R5,ECCERR	CHECK ERROR BIT
39	838	041522	005737	001322	TST	ERRFLG	BIT OK?
40	839	041526	001402		BEQ	ECCD16	GO NO IF YES
41	840	041530	000137	041642	JMP	ECCDEX	LEAVE THIS PLACE IF NOT
42	841	041534	005204		ECCD16: INC	R4	SUBTEST NUMBER=16(CRC BIT AGAIN OK)
43	842	041536	004537	040644	JSR	R5,VRTECC	NOW LET'S FOOL WITH A CHECKER
44	843						BOARD PATTERN.
45	844	041542	125252		.WORD	125252	SECTOR PATTERN(CHECKER BOARD)
46	845	041544	000376		.WORD	376	MIDDLE OF SECTOR
47	846	041546	125052		.WORD	125052	LOSE BIT 7(TRICKY)
48	847	041550	005737	001322	TST	ERRFLG	DID IT ERROR?
49	848	041554	001002		BNE	ECCD17	CONTINUE IF YES
50	849	041556	000137	041642	JMP	ECCDEX	EXIT IF NO
51	850	041562	005204		ECCD17: INC	R4	SUBTEST NUMBER=17(CHECKERBD ERROR)
52	851	041564	004537	041652	JSR	R5,ECCERR	CHECK ECC ERROR BIT
53	852	041570	005737	001322	TST	ERRFLG	ERROR?
54	853	041574	001402		BEQ	ECCD20	CONTINUE IF YES
55	854	041576	000137	041642	JMP	ECCDEX	EXIT IF NOT CORRECT
56	855	041602	005204		ECCD20: INC	R4	SUBTEST NUMBER=20(CRC BIT OK)
57							

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6      856 041604 004537 040644          JSR      R5,VRTECC          ;DO SAME TEST WITH REVERSE CHECKERBD.
7      857 041610 052525          .WORD   052525          ;HERE SI SECTOR PATTERN
8      858 041612 000376          .WORD   376            ;POSITION-MIDDLE OF SECTOR
9      859 041614 052125          .WORD   052125          ;LOSE BIT 8
10     860 041616 005737 001322        TST     ERRFLG          ;ERROR?
11     861 041622 001002          BNE     ECCD21          ;CONTINUE IF YES
12     862 041624 000137 041642        JMP     ECCDEX          ;EXIT IF ERROR
13     863 041630 005204          ECCD21: INC     R4          ;SUBTEST NUMBER=21(SECOND CHECKER OK)
14     864 041632 004537 041652        JSR     R5,ECCERR       ;ERROR BIT OK?
15     865 041636 004537 003362        ECCD22: JSR     R5,TSCTL      ;EXIT TO TEST CONTROL HERE
16     866          ;
17     867          ;
18     868          ;
19     869 041642 012737 000001 001322 ECCDEX: MOV     #1,ERRFLG        ;INSURE ERROR FLAG=1
20     870 041650 000772          BR      ECCD22          ;AND EXIT
21     871          ;
22     872          ;
23     873          ;
24     874          ;
25     875          ;
26     876          ;
27     877          ;
28     878          ;
29     879          ;
30     880          ;
31     881          ;          ECC ERROR BIT CHECK ROUTINE
32     882          ;          *****
33     883          ;
34     884          ;          THIS SHORT SURROUTINE HELPS REDUCE CODE
35     885          ;          WHEN CHECKING ERROR DETECTION OF THE ECC LOGIC
36     886          ;
37     887          ;          AT EXIT R2=REFERENCE ERROR WORD(CRC ERROR BIT)
38     888          ;          R3= ACTUAL ERROR REGISTER
39     889          ;
40     890          ;          AND THE ERROR FLAG "ERRFLG" WILL BE
41     891          ;          SET IF R2 DOES NOT EQUAL R3
42     892          ;
43     893          ;
44     894          ;
45     895 041652 012702 000400          ECCERR: MOV     #BIT8,R2        ;SET UP REFERENCE WORD (CRC ERROR)
46     896 041656 017703 137132        MOV     @DERR,R3        ;FETCH ERROR REGISTER
47     897 041662 020203          CMP     R2,R3          ;EQUAL?
48     898 041664 001002          BNE     ECEROT          ;EXIT IF NO
49     899 041666 005037 001322        CLR     ERRFLG          ;RESET ERROR FLAG IF YES
50     900 041672 000205          ECEROT: RTS     R5          ;AND RETURN
51     901          ;
52     902          ;
53     903          ;
54     904          ;
55     905          ;
56     906          ;
57     907          ;
58     908          ;
59     909          ;
60     910          ;
61     911          ;
62     912          ;

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1	970	041754	005204		ECDC2:	INC	R4		;SUBTEST NUMBER=2(ECC ERROR)
2	971	041756	017703	137024		MOV	@DWCNT,R3		;TRANSFER STOP?
3	972	041762	005002			CLR	R2		;SET UP REFERENCE
4	973	041764	020203			CMF	R2,R3		;WORD COUNT OVERFLOW?
5	974	041766	001002			BNE	ECDC3		;CONTINUE IF NO
6	975	041770	000137	042504		JMP	EDCEX		;EXIT IF OVERFLOWED
7	976	041774	005204		ECDC3:	INC	R4		;SUBTEST NUMBER=3
8	977	041776	017703	137014		MOV	@ECCPB,R3		;FETCH BIT POSITION REGISTER
9	978	042002	005002			CLR	R2		;SET UP REFERENCE WORD
10	979	042004	020203			CMF	R2,R3		;BIT ZEROED?
11	980	042006	001402			BEQ	ECDC4		;CONTINUE IF YES
12	981	042010	000137	042504		JMP	EDCEX		;EXIT IFNO
13	982	042014	005204		ECDC4:	INC	R4		;SUBTEST NUMBER=4(BIT POSITION DIDN'T CHANGE)
14	983	042016	042777	100000	136774	BIC	#BIT15,@ECCPW		;RESET ECC INHIBIT
15	984	042024	004537	040644		JSR	R5,WRTECC		;TRY ECC CORRECTION OF 1 ERROR BIT
16	985	042030	000000			.WORD	0		;PATTERN=0
17	986	042032	000000			.WORD	0		;POSITION 1
18	987	042034	000001			.WORD	1		;FIRST BIT IS BAD
19	988	042036	005737	001322		TST	ERRFLG		;ERROR SET(SHOULD BE)
20	989	042042	001002			BNE	ECDC5		;CONTINUE IF YES
21	990	042044	000137	042504		JMP	EDCEX		;EXIT IF NO ERROR
22	991	042050	005204		ECDC5:	INC	R4		;SUBTEST NUMBER=5(ERROR DETECTED)
23	992	042052	004537	041652		JSR	R5,ECCERR		;CHECK ERROR BIT(CRC)
24	993	042056	005737	001322		TST	ERRFLG		;OK?
25	994	042062	001402			BEQ	ECDC6		;CONTINUE IF YES
26	995	042064	000137	042504		JMP	EDCEX		;EXIT IF NO
27	996	042070	005204		ECDC6:	INC	R4		;SUBTEST NUMBER=6(ECC ERROR DETECTED)
28	997	042072	017703	136720		MOV	@ECCPB,R3		;FETCH ECC BIT POSITION REG
29	998	042076	012702	000001		MOV	#BIT0,R2		;SET UP REFERENCE WORD
30	999	042102	020203			CMF	R2,R3		;BITS SET?
31	1000	042104	001402			BEQ	ECDC7		;CONTINUE IF YES
32	1001	042106	000137	042504		JMP	EDCEX		;EXIT IF NO
33	1002	042112	005204		ECDC7:	INC	R4		;SUBTEST NUMBER=7(COUNT=1)
34	1003	042114	017703	136700		MOV	@ECCPW,R3		;FETCH PATTERN WORD
35	1004	042120	020203			CMF	R2,R3		;SET IF PATTERN WORD OK
36	1005	042122	001402			BEQ	ECDC10		;CONTINUE IF YES
37	1006	042124	000137	042504		JMP	EDCEX		;EXIT IF NO
38	1007	042130	005204		ECDC10:	INC	R4		;SUBTEST NUMBER=10(PATTERN OK)
39	1008	042132	004537	040644		JSR	R5,WRTECC		;TRY 11 BIT ERROR
40	1009	042136	000000			.WORD	0		;FIELD=0
41	1010	042140	000000			.WORD	0		;POSITION=1
42	1011	042142	003777			.WORD	3777		;ERROR IS FIRST 11 BITS
43	1012	042144	005737	001322		TST	ERRFLG		;ERROR?
44	1013	042150	001002			BNE	ECDC11		;CONTINUE IF YES
45	1014	042152	000137	042504		JMP	EDCEX		;EXIT IF NO
46	1015	042156	005204		ECDC11:	INC	R4		;SUBTEST NUMBER=11(ERROR OCCURED)
47	1016	042160	004537	041652		JSR	R5,ECCERR		;CHECK ECC ERROR BIT
48	1017	042164	005737	001322		TST	ERRFLG		;OK?
49	1018	042170	001402			BEQ	ECDC12		;CONTINUE IF YES
50	1019	042172	000137	042504		JMP	EDCEX		;EXIT IF NOT
51	1020	042176	005204		ECDC12:	INC	R4		;SUBTEST NUMBER=12(ERROR BIT OK)
52	1021	042200	012702	000001		MOV	#BIT0,R2		;SET UP REFERENCE FOR BIT POINTER
53	1022	042204	017703	136606		MOV	@ECCPB,R3		;FETCH BIT POSITION REG
54	1023	042210	020203			CMF	R2,R3		;OK?
55	1024	042212	001402			BEQ	ECDC13		;CONTINUE IF YES
56	1025	042214	000137	042504		JMP	EDCEX		;EXIT IF NO
57	1026	042220	005204		ECDC13:	INC	R4		;SUBTEST NUMBER=13(COUNTER OK)

6	1027	042222	017703	136572		MOV	0ECCPW,R3	);FETCH ERROR PATTERN
1	1028	042226	012702	003777		MOV	#3777,R2	);SET UP DESIRED RESULT
2	1029	042232	020203			CMP	R2,R3	);EQUAL?
3	1030	042234	001402			BEQ	ECDC14	);CONTINUE IF YES
4	1031	042236	000137	042504		JMP	EDCEX	);EXIT IF NO
5	1032	042242	005204		ECDC14:	INC	R4	);PATTERN OK(NO HARD ERROR)
6	1033	042244	004537	040644		JSR	R5,VRTECC	);FORCE HARD ERROR #>11
7	1034	042250	000000			.WORD	0	);SECTOR=0
8	1035	042252	000000			.WORD	0	);FIRST WORD
9	1036	042254	007777			.WORD	7777	);12 BIT ERROR
10	1037	042256	005737	001322		TST	ERRFL6	);ERROR SET?
11	1038	042262	001002			BNE	ECDC15	);CONTINUE IF YES
12	1039	042264	000137	042504		JMP	EDCEX	);EXIT IF NO
13	1040	042270	005204		ECDC15:	INC	R4	);SUBTEST NUMBER=15(AN ERROR IS SET)
14	1041	042272	004537	041652		JSR	R5,ECCERR	);CHECK ERROR BIT SET
15	1042	042276	005737	001322		TST	ERRFL6	);OK?
16	1043	042302	001402			BEQ	ECDC16	);CONTINUE IF YES
17	1044	042304	000137	042504		JMP	EDCEX	);EXIT IF NO
18	1045	042310	005204		ECDC16:	INC	R4	);SUBTEST NUMBER=16(ERROR SET)
19	1046	042312	012702	110041		MOV	#110041,R2	);SET UP REFERENCE FOR BIT COUNT
20	1047	042316	017703	136474		MOV	0ECCPB,R3	);FETCH COUNT REGISTER
21	1048	042322	020203			CMP	R2,R3	);EQUAL?
22	1049	042324	001402			BEQ	ECDC17	);CONTINUE IF YES
23	1050	042326	000137	042504		JMP	EDCEX	);EXIT IF NOT
24	1051	042332	005001		ECDC17:	CLR	R1	);SUBTEST NUMBER=17(COUNTER OVERFLOWED)
25	1052							);AND HARD ECC ERROR DETECTED
26	1053	042334	012704	000017		MOV	#17,R4	);FORCE SUBTEST NUMBER=17
27	1054	042340	016137	002612	042362	MOV	S10RG(R1),ECD17	);LOAD BIT PATTERN
28	1055	042346	005721			TST	(R1)+	);UPDATE POINTER
29	1056	042350	010146			MOV	R1,-(SP)	);SAVE R1
30	1057	042352	004537	040644		JSR	R5,VRTECC	);WRITE A SLIDING BIT ERROR
31	1058	042356	000000			.WORD	0	);SECTOR=0
32	1059	042360	000000			.WORD	0	);PCPOSITION =1
33	1060	042362	000001		ECDC17:	.WORD	1	);BIT PATTERN
34	1061	042364	005737	001322		TST	ERRFL6	);ERROR SET?(SHOULD BE)
35	1062	042370	001002			BNE	ECDC20	);CONTINUE IF YES
36	1063	042372	000137	042504		JMP	EDCEX	);EXIT IF NO
37	1064	042376	005204		ECDC20:	INC	R4	);SUBTEST NUMBER=20 ERROR DETECTED
38	1065	042400	013702	042362		MOV	ECD17,R2	);SET UP REFERENCE FOR PATTERN COMPARE
39	1066	042404	017703	136410		MOV	0ECCPW,R3	);FETCH PATTERN WORD
40	1067	042410	004537	041652		JSR	R5,ECCERR	);CHECK ERROR BIT
41	1068	042414	005737	001322		TST	ERRFL6	);ERROR SET?
42	1069	042420	001406			BEQ	ECDC21	);CONTINUE IF YES
43	1070	042422	000137	042504		JMP	EDCEX	);EXIT IF ERROR
44	1071	042426	020203			CMP	R2,R3	);PATTERN OK?
45	1072	042430	001402			BEQ	ECDC21	);CONTINUE IF YES
46	1073	042432	000137	042504		JMP	EDCEX	);EXIT IF NO
47	1074	042436	005204		ECDC21:	INC	R4	);SUBTEST NUMBER=21(PATTERN OK)
48	1075	042440	012702	000001		MOV	#BIT0,R2	);SET UP FOR COUNT CHECK
49	1076							);
50	1077							); NOTE: UNTIL A SINGLE BIT ECC ERROR
51	1078							); PASSES THE 11 BIT POSITION
52	1079							); IN THE SECTOR FIELD,THE COUNT
53	1080							); REGISTER WILL BE THE VALUE 1.
54	1081							);
55	1082	042444	017703	136346		MOV	0ECCPB,R3	);FETCH COUNT REGISTER
56	1083	042450	020203			CMP	R2,R3	);OK?
57								

1	1084	042452	001402			BEO	ECDC22		;CONTINUE IF YES
2	1085	042454	000137	042504		JMP	EDCEX		;EXIT IF NO
3	1086	042460	005204			ECDC22: INC	R4		;SUBTEST NUMBER=22(COUNT OK)
4	1087	042462	012601			MOV	(SP)+,R1		;RESTOR R1
5	1088	042464	010137	042514		MOV	R1,TMPCNT		;SAVE IN TEMP.
6	1089								;AT THIS POINT WE WILL
7	1090								;REUSE THE PRECEEDING CODE ,FROM
8	1091								;SUBTEST 17 TO SUBTEST22, TO
9	1092								;SLIDE THE SINGLE BIT TROUGH 11
10	1093								;POSITIONS,IF AN ERROR SHOULD OCCUR,
11	1094								;LOCATION "TMPCNT" WILL BE A
12	1095								;AN INDEX ON TABLE "S1ORG" TO AID THE
13	1096								;THE TECHNICIAN IN DEBUGGING,ADDING TMPCNT TO
14	1097								;ADDRESS S1ORG WILL POINT TO THE
15	1098								;BIT POSITION FAILING.
16	1099								;
17	1100	042470	027727	136324	002000	CMP	@ECCPW,#BIT10		;SEE IF WE ARE ON LAST BIT
18	1101	042476	002716			BLT	ECDC17+2		;DO NEXT BIT IF LESS THAN
19	1102	042500	004537	003342		ECDC24: JSR	R5,TSTCTL		;GO HOME
20	1103								;
21	1104								;
22	1105	042504	012737	000001	001322	EDCEX: MOV	#1,ERRFLG		;SET ERROR FLG=1
23	1106	042512	000772			BR	ECDC24		;AND EXIT
24	1107								;
25	1108								;
26	1109								;
27	1110								;
28	1111								;
29	1112								;
30	1113	042514	000000			TMPCNT: WORD 0			;TEMPORARY LOCATION
31	1114								;
32	1115								;
33	1116								;
34	1117								;
35	1118								;
36	1119								;
37	1120						TNA23	9-NOV-77	;
38	1121								;
39	1122								;
40	1123								;
41	1124								ECC COMPATIBILITY/EXERCISE TESTS
42	1125								*****
43	1126								;
44	1127								THESE TESTS CHECK THAT THE CONTROLLER
45	1128								UNDER TEST IS GENERATING THE SAME CRC/ECC PATTERNS
46	1129								THAT PREVIOUS 211 CONTROLLERS HAVE GENERATED.
47	1130								;
48	1131								A SECOND PART OF THIS EXERCISE IS TO
49	1132								FORCE CRC ERRORS ON VARIOUS AREAS ON THE DISK
50	1133								AND CHECK THAT THE ECC INFORMATION GENERATED
51	1134								BY THE ECC LOGIC IS CORRECT,TESTS TNA21 AND TNA22
52	1135								DO SIMILAR CHECKS HOWEVER,THOSE TESTS CENTER ON
53	1136								THE FIRST WORD OF THE DATA FIELD.
54	1137								;
55	1138								;
56	1139								;
57	1140	042516	005004			TNA23: CLR	R4		;SUBTEST NUMBER=0

1	1141	042520	004537	004276		JSR	R5,ROUSET	IREQUEST THE FORMATTER
2	1142	042524	012700	024652		MOV	#ISECWB,R0	IUSE ONE SECTOR WRITE BLOCK
3	1143	042530	005010			CLR	(R0)	IINSURE SECTOR ZERO
4	1144	042532	023727	001046	177400	CMP	WPSEC,#177400	I256 WORDS PER SECTOR
5	1145	042540	001402			BEQ	ECCOMH	I60 ON IF YES
6	1146	042542	000137	042752		JMP	ECCOMEX	IEXIT IF NO
7	1147	042546						
8	1148	042546	013760	001046	000004	MOV	WPSEC,4(R0)	IINSURE WORD COUNT
9	1149	042554	004537	004034		JSR	R5,CLRBUF	I CLEAR BUFFER AREA
10	1150	042560	012737	000001	044312	MOV	#1,0DBUF	I MAKE DATA FOR SECTOR=1 BIT
11	1151	042566	004537	022700		JSR	R5,DXFER	I60 WRITE SECTOR
12	1152	042572	005737	001322		TST	ERRFLG	IERRORS?
13	1153	042576	001402			BEQ	ECCO,1	ICONTINUE IF NO
14	1154	042600	000137	042752		JMP	ECCOMEX	IEXIT IF ERROR
15	1155	042604	005204			INC	R4	I SUBTEST NUMBER=1(SECTOR WRITTEN OK)
16	1156	042606	012700	040632		MOV	#RDCDE,R0	I FETCH READ ALL COMMAND
17	1157	042612	013702	001234		MOV	CURDSK,R2	I ENTER PROPER BUFFER AREA
18	1158	042616	006302			ASL	R2	I
19	1159	042620	016260	001200	000002	MOV	IBFTBL(R2),2(R0)	I
20	1160	042626	013760	001046	000004	MOV	WPSEC,4(R0)	ISET UP WORD COUNT
21	1161	042634	162760	000012	000004	SUB	#10,,4(R0)	IINCLUDE HEADERS,CRC'S AND ECC WORDS
22	1162	042642	005237	001176		INC	SPECHD	I FLAG WEIRD TRANSFER
23	1163	042646	004537	022700		JSR	R5,DXFER	I60 READ ECC WORDS
24	1164	042652	005037	001176		CLR	SPECHD	I CLEAR WEIRD XFER FLAG
25	1165	042656	005737	001322		TST	ERRFLG	IERROR SET?
26	1166	042662	001402			BEQ	ECCOM2	ICONTINUE IF NO
27	1167	042664	000137	042752		JMP	ECCOMEX	IEXIT IF ERROR
28	1168	042670	005204			INC	R4	I SUBTEST NUMBER=2(READ SUCCESSFUL)
29	1169	042672	013701	001050		MOV	POSWP,R1	ISET UP POINTER TO LOOK AT ECC WORDS
30	1170	042676	006301			ASL	R1	I MAKE WORDS PER SECTOR AS CORE ADDR
31	1171	042700	016002	000002		MOV	2(R0),R2	I FIND OSTARTING ADDR.
32	1172	042704	060201			ADD	R2,R1	I COMPUTE ECC WORD POSITION
33	1173	042706	062701	000020		ADD	#20,R1	I INCLUDE HEADERS AND HEADER CRC'S
34	1174	042712	011103			MOV	(R1),R3	I FETCH FIRST ECC WORD
35	1175	042714	013702	001264		MOV	ECCW1,R2	I FETCH REFERENCE WORD
36	1176							I THE REFERENCE WORDS USED HERE
37	1177							I WERE READ FROM THE FIRST ECC
38	1178							I211 CONTROLLER AND WERE INCLUDED
39	1179							I IN THIS ASSEMBLY.
40	1180	042720	020203			CMP	R2,R3	I EQUAL?
41	1181	042722	001402			BEQ	ECCOM3	I CONTINUE IF YES
42	1182	042724	000137	042752		JMP	ECCOMEX	I EXIT IF NOT
43	1183	042730	005204			INC	R4	I FIRST ECC WORD COMPATIBLE
44	1184	042732	016103	000002		MOV	2(R1),R3	I FETCH SECOND WORD
45	1185	042736	013702	001266		MOV	ECCW2,R2	I SET UP SECOND REFERENCE
46	1186	042742	020203			CMP	R2,R3	I EQUAL?
47	1187	042744	001002			BNE	ECCOMEX	I
48	1188	042746	004537	003342		JSR	R5,TSCTL	I EXIT HERE
49	1189							I
50	1190							I
51	1191							I
52	1192							I
53	1193	042752	012737	000001	001322	ECCOMEX: MOV	#1,ERRFLG	I SET ERROR FLAG
54	1194	042760	000772			BR	ECCOM4	I AND EXIT
55	1195							I
56	1196							I
57	1197							I



1	1255	043170	013710	001162		MOV	ENDSEC,(R0)	LOAD UP DISK ADDRESS
2	1256	043174	013760	001166	000006	MOV	ENDCYL,6(R0)	
3	1257	043202	053710	001164		BIS	ENDHD,(R0)	
4	1258	043206	005237	001176		INC	SPECMD	SET SPECIAL XFER FLAG
5	1259	043212	004537	022700		JSR	R5,DXFER	GO FORMAT
6	1260	043216	005037	001176		CLR	SPECMD	CLEAR SPECIAL XFER FLAG
7	1261	043222	005737	001322		TST	ERRFLG	ERRORS?
8	1262	043226	001020			BNE	FTEX	EXIT IF YES
9	1263	043230	013702	001044		MOV	MAXCYL,R2	SET UP TO CHECK ALL DONE
10	1264	043234	005202			INC	R2	
11	1265	043236	020237	001166		CMP	R2,ENDCYL	END OF DISK?
12	1266	043242	001415			BEO	FHTOUT	EXIT IF YES
13	1267	043244	013737	001162	001136	MOV	ENDSEC,CURSEC	LOOK TO NEXT RANSFER IF NO
14	1268	043252	013737	001164	001140	MOV	ENDHD,CURHD	
15	1269	043260	013737	001166	001142	MOV	ENDCYL,CURCYL	
16	1270	043266	000661			BR	FT3	AND SET BUFFERS UP AGAIN
17	1271							
18	1272							
19	1273	043270	012737	000001	001322	FTEX: MOV	R1,ERRFLG	SET ERROR FLAG=1
20	1274	043276	004537	003342		FHTOUT: JSR	R5,TSTCTL	EXIT
21	1275							
22	1276							
23	1277							
24	1278	043302	000000			FMTBK: WORD 0		SECTOR HEAD=0
25	1279	043304	044312			WORD 0D8UF		OUTPUT BUFFER
26	1280	043306	177400			WORD 177400		WORD COUNT WILL BE SET
27	1281	043310	000000			WORD 0		CYLINDER ADDR=0
28	1282	043312	000010			WORD FMTCHD		FORMAT COMMAND(NO 60)
29	1283							
30	1284							
31	1285							
32	1286							
33	1287							
34	1288							
35	1289							
36	1290							
37	1291							
38	1292							
39	1293							
40	1294							
41	1295							
42	1296							
43	1297							
44	1298							
45	1299							
46	1300	043314	005004			TN46: CLR	R4	INITIALIZE SUBTEST NUMBER
47	1301	043316	004537	004276		JSR	R5,RQUEST	REQUEST ZIT
48	1302	043322				TN46A:		
49	1303	043322	012700	035530		MOV	#WRCB+8,(R0)	GET COMMAND ENTRY CB ADDRESS
50	1304	043326	012710	000006		MOV	#WRTCHD,(R0)	SPECIFY WRITE COMMAND
51	1305	043332	013740	001142		MOV	CURCYL,(R0)	INITIALIZE CYLINDER
52	1306	043336	013701	001040		MOV	MAXSEC,R1	COMPUTE ONE SURFACE WORD COUNT
53	1307	043342	013702	001050		MOV	POSVP,R2	LOAD R2 WITH WORD COUNT/ONE SECTOR
54	1308	043346	010203			MOV	R2,R3	LOAD INTO R3 ALSO
55	1309	043350	005301			TN46B: DEC	R1	START LOOP
56	1310	043352	100402			BMI	TN46C	EXIT IF DONE
57	1311	043354	060203			ADD	R2,R3	ADD ANOTHER SECTOR COUNT HERE

14M.ECC TEST NUMBERS 46 >> 50 13-NOV-77

FORMAT CHECK TEST

THIS TEST CHECKS THE FORMAT OF ALL THE HEADER WORDS BY COMMANDING A COMPLETE SURFACE WRITE AND USING THE FORMATTERS LOGIC TO CHECK THE HEADER WORDS.

1	1312	043356	000774		BR	TN468		; GO ON
2	1313	043360		TN46C:				
3	1314	043360	005403		NEG	R3		; MAKE 2'S COMPLEMENT FOR WORD COUNT
4	1315	043362	010340		MOV	R3, -(R0)		; ENTER INTO TRANSFER BLOCK
5	1316	043364	012740	036144	MOV	#TN33, -(R0)		; SPECIFY OUTPUT BUFFER
6	1317	043370	013740	001136	MOV	CURSEC, -(R0)		; SPECIFY SECTOR
7	1318	043374	053710	001140	BIS	CURHD, (R0)		; OR IN CURRENT HEAD
8	1319	043400	004537	022700	JSR	R5, DXFER		; READ HEADER
9	1320	043404	005737	001322	TST	ERRFLG		; ANY ERRORS?
10	1321	043410	001031		BNE	TN46EX		; EXIT IF YES
11	1322	043412	012760	000026	000010	MOV	#WRCHK, 10(R0)	; LOAD WRITE CHECK COMMAND
12	1323	043420	004537	022700	JSR	R5, DXFER		; GO WRITE CHECK LAST DATA TRANSFER
13	1324	043424	012760	000006	000010	MOV	#WRTCMD, 10(R0)	; RELOAD WRITE COMMAND
14	1325	043432	005737	001322	TST	ERRFLG		; ERRORS?
15	1326	043436	001016		BNE	TN46EX		; EXIT IF YES
16	1327	043440	005737	001144	TST	DKEND		; ARE WE AT THE END OF THE DISK MEDIUM
17	1328	043444	001013		BNE	TN46EX		; EXIT IF ALL DONE
18	1329	043446	013737	001162	001136	MOV	ENDSEC, CURSEC	; UPDATE DISK ADDRESS
19	1330	043454	013737	001164	001140	MOV	ENDHD, CURHD	
20	1331	043462	013737	001166	001142	MOV	ENDCYL, CURCYL	
21	1332	043470	005204		INC	R4		; UPDATE SUBTEST COUNT
22	1333	043472	000713		BR	TN46A		; GO READ NEXT FORMAT
23	1334	043474	004537	003342	TN46EX:	JSR	R5, TSTCTL	; GO TO TEST CONTROL
24	1335							
25	1336							
26	1337							
27	1338							
28	1339							12M.ECC TEST NUMBER A47 13-NOV-77
29	1340							
30	1341							
31	1342							FORMATTING PROGRAM #2
32	1343							*****
33	1344							
34	1345							
35	1346							
36	1347							
37	1348							THIS PROGRAM FORMATS THE DISK
38	1349							WITHOUT THE OPERATOR ENTERING ANY PARAMETERS.
39	1350							THE NUMBER OF SECTORS AND THE NUMBER OF DATA
40	1351							WORDS IN EACH SECTOR IS SPECIFIED IN THE FIRST PORTION
41	1352							OF THE DIAGNOSTIC. IF THE OPERATOR WISHES TO FORMAT
42	1353							A SECTION OR ONE SECTOR OF THE DISK SURFACE TEST50
43	1354							ALLOWS HIM TO DO SO. (BAD SECTOR BITS, WRITE PROTECT ETC.)
44	1355							
45	1356							
46	1357							
47	1358	043500	000000		FSTHLF:	WORD 0		; REVOLUTION FLAG
48	1359	043502	000000		ESECTA:	WORD 0		; =MAXSEC+1
49	1360	043504	000000		ESECTB:	WORD 0		; =MAXSEC+?
50	1361							
51	1362							
52	1363							
53	1364	043506	005004		TN47:	CLR	R4	; SUBTEST NUMBER=0
54	1365	043510	004537	004276	JSR	R5, RQUEST		; REQUEST 211
55	1366	043514	105777	135260	TSTB	@DCSR		; CONTROLLER READY?
56	1367	043520	100402		BMI	F2T1		; CONTINUE IF YES
57	1368	043522	000137	044176	JMP	F2TEX		; EXIT IF NO



6	1369	043526	005204			F2T1:	INC	R4		;}SUBTEST NUMBER=1(FORMATTER READY)
7	1370	043530	004537	016332			JSR	R5,DISKID		;}POSITION DRIVE SELECT BITS
8	1371	043534	010277	135242			MOV	R2,@DUSH		;}SELECT UNIT
9	1372	043540	010237	044300			MOV	R2,FMTDSK		;}SAVE FOR LATER USE
10	1373	043544	005777	135242			TST	@DSTAT		;}DRIVE READY?
11	1374	043550	100402				BMI	F2T2		;}CONTINUE IF YES
12	1375	043552	000137	044176			JMP	F2TEX		;}EXIT WITH ERROR
13	1376	043556	005204			F2T2:	INC	R4		;}SUBTEST NUMBER=2(DRIVE READY)
14	1377	043560	013737	001040	043502		MOV	MAXSEC,ESECTA		;}SET UP REV FLAG
15	1378	043566	005237	043502			INC	ESECTA		;}
16	1379	043572	005037	043500			CLR	FSTHLF		;}CLEAR REVOLUTION FLAG
17	1380	043576	013703	001050			MOV	POSVP,R3		;}LOAD NUMBER OF WORDS PER SECTOR
18	1381									;}INTO REGISTER R3
19	1382	043602	006303				ASL	R3		;}MULTIPLY BY 2 FOR MEMORY USE
20	1383	043604	062703	000004			ADD	#4,R3		;}INCLUDE HEADERS IN COUNT
21	1384	043610	005737	001074			TST	ECC		;}ECC CONTROLLER?
22	1385	043614	001402				BEQ	F2T3		;}GO NO IF YES
23	1386	043616	062703	000004			ADD	#4,R3		;}ADJUST FOR ECC WORDS
24	1387	043622	062703	044312		F2T3:	ADD	#0DBUF,R3		;}COMPUTE ADDRESS FOR SECOND SET
25	1388	043626	005213				INC	(R3)		;}MAKE FIRST HEADER WORD VALID
26	1389	043630	005203	000004			INC	4(R3)		;}SET SECOND SET(DOESN'T MATTER IF NON ECC
27	1390	043634	012704	044312			MOV	#0DBUF,R4		;}ENTER ADDRESS OF FIRST HEADER
28	1391	043640	013701	001050			MOV	POSVP,R1		;}LOAD R1 WITH #WORDS PER SECTOR
29	1392	043644	062701	000010			ADD	#10,R1		;}INCLUDE HEADERS IN WORD COUNT
30	1393	043650	005401			F2T4:	NEG	R1		;}MAKE 2'S COMP
31	1394	043652	013705	001010		F2T5:	MOV	DCYL,R5		;}SET R5 AS POINTER TO DISK ADDR'S
32	1395	043656	013715	001142			MOV	CURCYL,(R5)		;}LOAD WORD COUNT
33	1396	043662	010145				MOV	R1,-(R5)		;}LOAD WORD COUNT
34	1397	043664	010445				MOV	R4,-(R5)		;}LOAD CORE ADDRESS
35	1398	043666	011445				MOV	(R4),-(R5)		;}LOAD DUSH
36	1399	043670	053715	044300			BIS	FMTDSK,(R5)		;}OR IN UNIT SELECT BITS
37	1400	043674	052777	000010	135076	F2T6:	BIS	#FMTCHD,@DCSR		;}SET DCSR FOR FORMAT
38	1401	043702	052777	000001	135070		BIS	#60,@DCSR		;}SET 60 BIT
39	1402	043710	053737	001302	043676		BIS	SEKINB,F2T6+2		;}SET SEEK INHIBIT BIT
40	1403	043716	062737	000004	001136		ADD	#4,CURSEC		;}INCREMENT SECTOR COUNTER
41	1404	043724	005737	043500			TST	FSTHLF		;}FIRST TIME AROUND
42	1405	043730	001012				BNE	F2T7		;}NO,CHECK IF SURFACE DONE
43	1406	043732	023737	001136	043502		CMP	CURSEC,ESECTA		;}DONE WITH FIRST PASS
44	1407	043740	001057				BNE	F2T10		;}NO GO FORMAT AGAIN
45	1408	043742	005237	043500			INC	FSTHLF		;}YES SET FLAG AND SPIN AGAIN
46	1409	043746	012737	000002	001136		MOV	#2,CURSEC		;}SET CURSEC TO 2
47	1410	043754	000451				BR	F2T10		;}AND GO FORMAT AGAIN
48	1411	043756	023737	001136	001040	F2T7:	CMP	CURSEC,MAXSEC		;}DONE WITH SECOND PASS?
49	1412	043764	002445				BLT	F2T10		;}NO,GO FORMAT AGAIN
50	1413	043766	005037	043500			CLR	FSTHLF		;}RESET PASS COUNTER
51	1414	043772	005037	001136			CLR	CURSEC		;}RESET CURSEC
52	1415	043776	023737	001140	001042		CMP	CURHD,MAXHD		;}DONE WITH SURFACES?
53	1416	044004	001404				BEQ	F2T11		;}YES GO INCREMENT CYLINDER
54	1417	044006	062737	000200	001140		ADD	#HDINC,CURHD		;}INCREMENT HEAD COUNTER
55	1418	044014	000431				BR	F2T10		;}AND FORMAT AGAIN
56	1419	044016	005037	001140		F2T11:	CLR	CURHD		;}RESET HEAD COUNTER
57	1420	044022	105777	134752			TSTB	@DCSR		;}WAIT FORMATTER READY?
58	1421	044026	100375				BPL	-4		;}
59	1422	044030	023737	001142	001044		CMP	CURCYL,MAXCYL		;}END OF DISK
60	1423	044036	001462				BEQ	F2TOUT		;}EXIT IF YES
61	1424	044040	005237	001142			INC	CURCYL		;}INCREMENT TRACK COUNTER IF NO
62	1425	044044	043777	001302	134726		BIC	SEKINB,@DCSR		;}CLEAR SEEK INHIBIT

6	1426	044052	043737	001302	043676	BIC	SEKINB,F2T6+2	;	CLEAR SEEK INHIBIT BIT
1	1427	044060	022324			CMP	(R3)+,(R4)+	;	INDEX POINTERS TO TRACK ADDRESS
2	1428	044062	005213			INC	(R3)	;	INCRENEBT BOTH TRACKS ADDR
3	1429	044064	005214			INC	(R4)	;	
4	1430	044066	005263	000004		INC	4(R3)	;	SET SECOND HEADER WORDS
5	1431	044072	005264	000004		INC	4(R4)	;	
6	1432	044076	024344			CMP	-(R3),-(R4)	;	RESET POINTERS TO FIRST
7	1433							;	HEADER WORD ADDRESS
8	1434	044100	105777	134674		F2T10: TSTB	WDCSR	;	WAIT FORMATTER READY
9	1435	044104	100375			BPL	-4	;	
10	1436	044106	013714	001136		MOV	CURSEC,(R4)	;	ENTER NEW SECTOR NUMBER
11	1437	044112	013764	001136	000004	MOV	CURSEC,4(R4)	;	ENTER NEW SECTOR NUMBER
12	1438	044120	053714	001140		BIS	CURHD,(R4)	;	AND HEAD
13	1439	044124	053764	001140	000004	BIS	CURHD,4(R4)	;	
14	1440	044132	013713	001136		MOV	CURSEC,(R3)	;	
15	1441	044136	013763	001136	000004	MOV	CURSEC,4(R3)	;	
16	1442	044144	053713	001140		BIS	CURHD,(R3)	;	ENTER HEAD
17	1443	044150	053763	001140	000004	BIS	CURHD,4(R3)	;	
18	1444	044156	005213			INC	(R3)	;	INCREMENT SECOND SECTOR
19	1445	044160	005263	000004		INC	4(R3)	;	
20	1446	044164	005777	134610		TST	WDCSR	;	ERRORS?
21	1447	044170	100230			BFL	F2T5	;	CONTINUE IF NO
22	1448	044172	005237	001322		INC	ERRFLG	;	SET ERROR FLAG IF YES
23	1449	044176	012737	000001	001322	F2TEX: MGV	#1,ERRFLG	;	SET ERROR FLAG TO 1
24	1450	044204	004537	003342		F2TOUT: JSR	R5,TSTCTL	;	EXIT HERE
25	1451							;	
26	1452							;	
27	1453							;	
28	1454							;	
29	1455							;	
30	1456							;	
31	1457							;	
32	1458							;	
33	1459							;	
34	1460							;	
35	1461						XOR,PH	;	9-NOV-77
36	1462							;	
37	1463							;	
38	1464							;	
39	1465							;	ECC WORD CORRECTION ROUTINE
40	1466							;	*****
41	1467							;	
42	1468							;	
43	1469							;	
44	1470							;	THIS ROUTINE USES THE ECC PATTERN AREGISTER
45	1471							;	AND ONE ENTRY POINT TO FORM A CORRECTED CORE
46	1472							;	WORD DURING THE ECC TESTS.AT EXIT REGISTER R3 WILL
47	1473							;	CONTAIN THE CORRECTED WORD.
48	1474							;	
49	1475							;	
50	1476						CALL: JSR	;	APCORR,PC
51	1477							;	
52	1478						AT ENTRY	;	4(R5)=CORE WORD TO BE CORRECTED
53	1479							;	
54	1480							;	
55	1481							;	
56	1482	044210	016546	000004		APCORR: MOV	4(R5),-(SP)	;	SAVE CORE IMAGE

1	1483	044214	011603		MOV	(SP),R3	USE R3 FOR WORK
2	1484	044216	017702	134576	MOV	SECCPW,R2	R2=PATTERN WORD
3	1485	044222	032702	000001	APR1:	BIT	#BIT0,R2
4	1486	044226	001002		BNE	APR2	GO ON IF DONE
5	1487	044230	006202		ASR	R2	SHIFT RIGHT IF BIT 0=0
6	1488	044232	000773		BR	APR1	CHECK IT
7	1489	044234	040203	APR2:	BIC	R2,R3	NOT PATTERN WITH DATA
8	1490	044236	042602		BIC	(SP),R2	NOT DATA WITH PATTERN
9	1491	044240	050203		BIS	R2,R3	ROR PATTERN+DATA
10	1492	044242	000207		RTS	PC	LEAVE ALL DONE
11	1493						
12	1494						
13	1495						
14	1496						
15	1497						
16	1498						
17	1499						
18	1500	044244	000000	BSECT:	WORD 0		BEGINNING SECTOR
19	1501	044246	000000	ESECT:	WORD 0		ENDING SECTOR ADDRESS
20	1502	044250	000000	BSURF:	WORD 0		BEGINNING SURFACE
21	1503	044252	000000	ESURF:	WORD 0		ENDING SURFACE NUMBER
22	1504	044254	000000	BTRK:	WORD 0		BEGINNING TRACK
23	1505	044256	000000	ETRK:	WORD 0		ENDING TRACK
24	1506	044260	000000	BDSEC:	WORD 0		BAD SECTOR FLAG
25	1507	044262	000000	WRPT:	WORD 0		WRITE PROTECT FLAG
26	1508	044264	000000	CSECT:	WORD 0		CURRENT SECTOR
27	1509	044266	000000	CSURF:	WORD 0		CURRENT SURFACE
28	1510	044270	000000	CTRK:	WORD 0		CURRENT TRACK
29	1511	044272	000000	WRD1:	WORD 0		HEADER WORD ONE
30	1512	044274	000000	WRD2:	WORD 0		HEADER WORD 2
31	1513	044276	000000	NORM:	WORD 0		NORMAL SECTOR FLAG
32	1514	044300	000000	FHTDSKT	WORD 0		CURRENT DISK DUSH BITS
33	1515						
34	1516						
35	1517						
36	1518						
37	1519						
38	1520						
39	1521						
40	1522						
41	1523						
42	1524						
43	1525						
44	1526						
45	1527						
46	1528						
47	1529						
48	1530						
49	1531						
50	1532						
51	1533						
52	1534						
53	1535	044312	000000	ODBUF:	WORD 0		ORIGIN ADDRESS
54	1536	047314	000000				
55	1537						
56	1538						
57	1539						

OUTPUT DATA BUFFER

THIS BUFFER CONTAINS DATA FOR ALL DISK WRITE OPERATIONS  
THIS BUFFER DATA IS FORMATTED PRIOR TO ANY WRITE OPERATIONS  
AS PART OF THE TESTING SEQUENCE.

BUFFER IS 768. WORDS LONG

```

6      1540      ;
7      1541      ; INPUT BUFFERS
8      1542      ;
9      1543      ;
10     1544      ; THESE DATA BUFFERS ARE ALWAYS USED DURING A READ COMMAND
11     1545      ; AND MAY VARY IN SIZE DEPENDING ON SIZE OF CORE.
12     1546      ;
13     1547      ;
14     1548 047314 000000      IDBUF1: •WORD 0      ;DRIVE 0 INPUT BUFFER AREA
15     1549      050314      •=•+510•      ;EACH AREA IS 512• WORDS LONG
16     1550 050314 000000      IDBUF2: •WORD 0      ;DRIVE 1 INPUT BUFFER AREA
17     1551      051314      •=•+510•      ;
18     1552 051314 000000      IDBUF3: •WORD 0      ;DRIVE 2 INPUT BUFFER AREA
19     1553      052314      •=•+510•      ;
20     1554 052314 000000      IDBUF4: •WORD 0      ;DRIVE 3 INPUT BUFFER AREA
21     1555      053314      •=•+510•      ;
22     1556 053314 000000      IDBUF5: •WORD 0      ;
23     1557      054314      •=•+510•      ;
24     1558      ; 512• WORDS OF BUFFER AREA ARE ASSIGNED TO EACH OF 4 DRIVES
25     1559      ;
26     1560      ;
27     1561      ;
28     1562      ;
29     1563      ;
30     1564      000001'      •END

```

## SYMBOL TABLE

1	ACTMSG 012477	ADR 015666	ADREX 016034
2	ADDRST 034742	ADRSV 034712	ADRSTP 015644
3	ADR1 016004	ADR2 016012	ADR3 016030
4	APCORR 044210	APR1 044222	APR2 044234
5	ASCII 006754	ASMSG 013525	AUTMSG 002241
6	AUTO 001036	AUTSM 001100	BADBIT 001276
7	BADNUM 006750	B0SEC 044260	BIT0 = 000001
8	BIT1 = 000002	BIT10 = 002000	BIT11 = 004000
9	BIT12 = 010000	BIT13 = 020000	BIT14 = 040000
10	BIT15 = 100000	BIT2 = 000004	BIT3 = 000010
11	BIT4 = 000020	BIT5 = 000040	BIT6 = 000100
12	BIT7 = 000200	BIT8 = 000400	BIT9 = 001000
13	BOOT 003500	BSECT 044244	BSURF 044250
14	BTRK 044254	BUFCLR 001300	CASCI 007014
15	CECC1 036522	CECC2 036544	CECC3 036600
16	CECC4 036630	CECC5 036672	CECC6 036736
17	CERP 021072	CEXIT 006740	CHKERR 022132
18	CIMODE 005522	C11 005352	C12 005366
19	C13 005372	C14 005374	C15 005412
20	C16 005414	C17 005420	C18 005424
21	CLI 005346	CLRBUF 004034	CLRB1 004052
22	CLRCNT= 007012	CLRERR 021030	CLRFTR 021510
23	CMDTB 005434	CMPCNT 001134	CMPPL 022510
24	CMSSG 010514	CNSTNT 002712 6	CNTFLG 036140
25	CNTINC 036142	COEX 006734	COCTDN 006716
26	CCCTER 006726	COCTI 006660	COEMSG 007425
27	COMMSG 011456	CONBL 005522	CONC 005732
28	CONTST 001230	CONU 015342	CONU 005734
29	CORE 003010	CRE1 003022	CR = 000015
30	CRCODE 005742	CRCXEX 040614	CRC1 037026
31	CRC10 037314	CRC11 037366	CRC12 037446
32	CRC13 037476	CRC14 037566	CRC15 037620
33	CRC16 037652	CRC17 037700	CRC2 037102
34	CRC20 037726	CRC21 040024	CRC22 040054
35	CRC23 040102	LRC24 040166	CRC25 040216
36	CRC26 040240	CRC27 040330	CRC3 037146
37	CRC30 040360	CRC31 040402	CRC32 040446
38	CRC33 040502	CRC34 040532	CRC35 040554
39	CRC36 040576	CRC4 037174	CRC5 037216
40	CRC6 037240	CRC7 037262	CSECT 044264
41	CSURF 044266	CSWR = 177570	CSVTCH 001250
42	CTLERR 023474	CTRK 044270	CURCYL 001142
43	CURDSK 001234	CURHD 001140	CURSEC 001136
44	CURTN 001232	CYLADR 002542	CYLDN 034124
45	CYLMMSG 001732	CYLSK= 176000	CYLUP 034122
46	CYMSG 011612	DARMSG 012644	DATA 006752
47	DATBUF 011222	DATCHP 017106	DATE 010676
48	DATERR 001320	DATEb 011222	DATMSG 013034
49	DBAR = 001004	DCAR 001004	DCCMSG 012560
50	DCHPA 017146	DCMSG 002066	DCRMSG 012602
51	DCSMSG 002054	DCSR 001000	DCSRA 001070
52	DCYL 001010	DCYMSG 012706	DECGSM 002060
53	DERECC 023402	DERMSG 012750	DERR 001014
54	DFMSG 013456	DISKHD 010032	DISKID 016332
55	DISKIN 007740	DISKP 001642	DISKTP 013446
56	DKDNEX 017332	DKEND 001144	DKINIT 016352
57	DKI1 016370	DKI2 016506	DKI3 016426

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SYMBOL TABLE

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8	DKI4	016440	DSCAR	001034	DSERR	023410
9	DSERRA	023462	DSKDN	017304	DSKMSG	012727
10	DSKSAV	001254	JSKTST	035000	DSTAT	001012
11	DTADR	002024	DTCHER	017172	DTCMEX	017162
12	DTCHLP	017136	DTCNT	001152	DTF	002045
13	DTERR	023320	DTERRA	023342	DTEXT	023306
14	DT1	010716	DT10	011140	DT2	010770
15	DT3	011006	DT4	011024	DT5	011042
16	DT6	011066	DT7	011102	DUMSG	011510
17	DUNF1	013452	DUSH	001002	DUSMSG	012623
18	DLCMSG	012665	DWCNT	001006	DXFER	022700
19	DXF1	022774	EBMSG	013176	ECBMSG	012771
20	ECC	001074	ECCBB	013214	ECCDEX	041642
21	ECCD1	041136	ECCD10	041352	ECCD11	041400
22	ECCD12	041420	ECCD13	041446	ECCD14	041466
23	ECCD15	041514	ECCD16	041534	ECCD17	041562
24	ECCD2	041164	ECCD20	041602	ECCD21	041630
25	ECCD22	041636	ECCD3	041204	ECCD4	041232
26	ECCD5	041252	ECCD6	041304	ECCD7	041324
27	ECCERR	041652	ECCEXT	041044	ECCMSG	002137
28	ECCME	042752	ECCOM1	042604	ECCOM2	042670
29	ECCOM3	042730	ECCOM4	042746	ECCPB	001016
30	ECCPW	001020	ECCWBK	041052	ECCWRT	040620
31	ECCV1	001264	ECCW2	001266	ECDC1	041734
32	ECDC10	042130	ECDC11	042156	ECDC12	042176
33	ECDC13	042220	ECDC14	042242	ECDC15	042270
34	ECDC16	042310	ECDC17	042332	ECDC2	041754
35	ECDC20	042376	ECDC21	042436	ECDC22	042460
36	ECDC24	042500	ECDC3	041774	ECDC4	042014
37	ECDC5	042050	ECDC6	042070	ECDC7	042112
38	ECDC17	042362	ECEROT	041672	ECHOEM	005534
39	ECOPM	042546	ECPMSG	013012	ECRMSG	012576
40	EDCEX	042504	EINMSG	007365	EMULAT	001274
41	ENDCYL	001166	ENDFLG	001146	ENDHD	001164
42	ENDMSG	001456	ENDPAR	022436	ENDSEC	001162
43	ENDTST	022576	ENTMSG	001400	ERCNTM	010544
44	ERDATA	013220	EREXIT	023554	ERIMGE	001170
45	ERMSG	012352	ERPRIN	001226	ERRBLK	035334
46	ERRCNT	001314	ERRFLG	001322	ERRID	023502
47	ERRCR	001324	ERRTAB	001336	ERRWRD	001160
48	ERSET	017272	ESECT	044246	ESECTA	043502
49	ESECTB	043504	ESURF	044252	ETRK	044256
50	EXITE	022136	FDRMSG	012367	FIEXIT	016114
51	FIUNIT	016042	FI1	016056	FI2	016066
52	FLTCLR=	000022	FMTBK	043302	FMTCLR	003614
53	FMTCHD=	000010	FMTDK	013240	FMTDSK	044300
54	FMTD1	013334	FMTD2	013406	FMTK1	013260
55	FMTOUT	043276	FMTROY=	000200	FMTTR	007072
56	FOLP	017032	FORMAT	016736	FSTHLF	043500
57	FTEX	043270	FITMSG	012417	FT1	043002
58	FT2	043030	FT3	043032	FT4	043034
59	FT5	043116	FT6	043154	FUNC	= 000136
60	F1LP	016756	F2LP	016774	F2TEX	044176
61	F2TOUT	044204	F2T1	043526	F2T10	044100
62	F2T11	044016	F2T2	043556	F2T3	043622
63	F2T4	043650	F2T5	043652	F2T6	043674
64	F2T7	043756	F3LP	017016	F4LP	017042



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SYMBOL TABLE

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1	FSLP	017060	GO	=	000001	GOTEST	003676	
2	HALT8	003776	HDERR	017264	HDINC	=	000200	
3	HDMSG	001703	HDMSK	=	170177	HDRC1	001260	
4	HDRC2	001262	HELP	013652	HERCNT	001316		
5	HLMSG	014046	HLP1	013726	HLP2	013742		
6	HLP3	013760	HPMSG	014004	IBFTBL	001200		
7	ICNT	001156	IDBUF1	047314	IDBUF2	050314		
8	IDBUF3	051314	IDBUF4	052314	IDBUF5	053314		
9	IDERK	023570	IDLP	023536	IMPBLK	031712		
10	INCHD	022670	INITLP	003562	INTCAL	=	000125	
11	INTCNT	=	000033	INTFLG	001150	INTGO	=	000101
12	INTMSG	002114	INTON	=	000100	INTSAV	001052	
13	INTTBL	001122	INTVEC	001072	INWAIT	004446		
14	IOERR	005744	IPFLG	001154	ISECFB	=	025450	
15	ISECRB	=	025462	ISECNB	=	024652	LDEX	007630
16	LDRD	017530	LD1	007566	LD1A	007562		
17	LD10	007726	LD2	007604	LD3	007632		
18	LD4	007640	LD5	007660	LD6	007706		
19	LD7	007714	LF	=	000012	LFCODE	005740	
20	LOADIN	007502	LPCNT	001272	LRERR	017646		
21	LREX	017634	LKLP1	017554	LRLP2	017606		
22	LRLP3	017602	LRLP4	017612	LSTTST	003702		
23	MAXCYL	001044	MAXHD	001042	MAXHED	001060		
24	MAXSEC	001040	MAXTFR	001270	MCPU	001102		
25	MDRIVE	001106	MEMEX	=	030000	MICRO	001066	
26	MONTH	011154	MSGADR	005526	MSG1	014131		
27	MSG10	014754	MSG11	015021	MSG12	015046		
28	MSG13	015101	MSG14	015152	MSG15	015177		
29	MSG16	015245	MSG17	015301	MSG2	014210		
30	MSG3	014271	MSG4	014347	MSG5	014436		
31	MSG6	014513	MSG7	014574	MSG8	014634		
32	MSG9	014705	MULCPU	001076	MULMSG	002204		
33	NCR	005530	NINPUT	001242	NONCON	001244		
34	NOPCMD	=	000077	NORM	044276	NOSTOP	001222	
35	NUMBER	005540	OCTAL	006640	ODBUF	044312		
36	OLDHDR	001064	OUTBUF	010574	OVBLK	033350		
37	PARINT	003532	PARMB	005544	PASCNT	001236		
38	PASINC	003720	PASINH	001224	PASMSG	010403		
39	PASS	011640	PATGEN	036064	PINC1	003736		
40	PINMSG	007320	PMGR	004446	PMG1	004506		
41	PM1	004460	PM2	004540	PM3	004544		
42	PM4	004562	PM5	004624	PNTMSG	010334		
43	PGLY	001256	PGSWP	001050	POUT	013104		
44	PPARMB	005546	PRDATA	010306	PRINT	010126		
45	PRMSG	010322	PROMPT	007062	PS	=	177776	
46	PSMSG	012006	PSS1	011766	PSS2	011762		
47	PSS3	012000	PSS4	011744	PSWORD	003032		
48	PTCH	035022	PT1	013120	P2MSG	006424		
49	P3MSG	006603	QDUMY	=	000336	QON	=	000100
50	QPRDY	=	000400	QUEST	007060	RAMBLE	001252	
51	RANB	015550	RANBLK	016130	RANBUF	015524		
52	RANDOM	015564	RAN1	016166	RAN10	016324		
53	RAN2	016172	RAN3	016216	RAN4	016246		
54	RAN5	016142	RAN6	016274	RAN7	016320		
55	RAN8	016222	RD	034430	RDBLK	023614		
56	RDCDE	040632	RDCMD	=	000004	RDECC	041064	
57	RDERR	001172	RDFMT	=	000012	RDHDBK	025436	



6	RDUSH	001054	REBOOT	004020	RECAL =	000025
1	REEPSK	002552	REGSAV	015440	REGO	002722
2	REG1	015460	REPBIT=	100000	REPFLG	001220
3	REPPSG	001536	REOFLG	005532	REQUST	036244
4	RERMSG	001574	REST	015510	RFRMSG	012447
5	RGR	013636	RGREAD	013564	ROEX	004374
6	RGUFST	004276	RQ1	004404	RQ2	004330
7	RQ3	004370	RTRYIN	001352	RTZCHD=	000024
8	RUB	005736	RUN	010064	RUN1	010122
9	RVCYL	001056	RWHCHD=	000016	SAVE	015474
10	SCBLK	011420	SCBLTP	011434	SCOADR	011446
11	SCOPE	011236	SC1	011270	SC2	011312
12	SC2A	011342	SC2B	011354	SC2C	011370
13	SC2D	011400	SC2H	011402	SC5	011406
14	SECINC	022612	SECHSG	001652	SECMSK=	177600
15	SEKBK	004240	SEKCHD=	000002	SEKCHP	001306
16	SEKER	004234	SEKFLP=	000010	SEKINB	001302
17	SEKUT	004172	SEKOU1	004216	SEKOU2	004212
18	SEKTIM	004066	SELA	021502	SELECT	021406
19	SKCNT	001112	SKDON	004260	SKDONE=	000074
20	SKFLOP=	007400	SKIPER	001312	SKLP	004152
21	SKLP1	004144	SKPBAD	001246	SLERR	020236
22	SLEX	020226	SLHMSG	007066	SLIDE	020144
23	SLIDE1	020212	SLIDE2	020216	SL1	020164
24	SOFERR	001330	SOFER1	001326	SOFTRY	001132
25	SPACE =	000040	SPECHD	001176	SREPFL	003330
26	SRTMSG	001426	SRTTN	001210	START	003000
27	STARTA	003072	STCLR	003260	STDMSG	001505
28	STOP	003412	STOP8	003474	STPDSK	001214
29	STPTN	001210	STPTST	003504	STRBUF=	***** GX
30	STRCNT	001062	STRMSG	006507	STRRD =	000032
31	STRTDS	001216	STRTN	001212	SUBMSG	012527
32	SYSCLR=	000001	SOORG	002652 G	STORG	002612 G
33	TDATE	001110	TER1	012042	TER2	012072
34	TER3	012100	TER4	012156	TER5	012210
35	TER6	012346	TER7	012236	TER8	012334
36	TER9	012260	TER9A	012302	TESTP	007176
37	TESTP1	007230	TEXA	031316	TIME =	177777
38	TIHLP	001310	TKB	005724	TKS	005722
39	TMPADR	034772	TMPCNT	042514	TNA16	036464
40	TNA16E	036770	TNA17	036774	TNA20	025740
41	TNA21	041076	TNA22	041674	TNA23	042516
42	TNINT	004006	TNINTA	004000	TNORG	002276
43	TNORGA	002420	TNTST	003516	TNO	016530
44	TNOA	016612	TNOB	016676	TNOC	016712
45	TNOERR	016726	TNOOUT	016732	TN1	017412
46	TN1A	017434	TN1B	017452	TN1C	017470
47	TN1D	017506	TN1ERR	017524	TN10	023626
48	TN11	023670	TN12	023760	TN13	024042
49	TN13EX	024124	TN13LP	024056	TN14	024130
50	TN15	024220	TN15LP	024244	TN16	024314
51	TN16EX	024646	TN17	024664	TN17A	024746
52	TN17EX	025416	TN17FB	025450	TN17RB	025462
53	TN2	017654	TN2A	017672	TN2B	017710
54	TN2C	017726	TN2D	017744	TN2E	017762
55	TN2FRR	017776	TN2OUT	020002	TN20	025474
56	TN2OEX	026324	TN21	026350	TN21A	026636

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6	TN21EX	027152	TN22	027170	TN22A	027442
7	TN22EX	030152	TN23	030160	TN23A	030312
8	TN23B	030452	TN23C	030530	TN23EX	030524
9	TN24	030542	TN24A	030672	TN24B	030706
10	TN24C	030652	TN24D	030716	TN24EX	031352
11	TN25	031360	TN25EX	031666	TN26	031724
12	TN26A	032010	TN26B	032000	TN26C	032156
13	TN26D	032212	TN26E	032260	TN26EX	032326
14	TN26F	032302	TN26OT	032322	TN27	032346
15	TN27A	032532	TN27C	032640	TN27D	032746
16	TN27E	033050	TN27EX	033334	TN27F	033106
17	TN27G	033276	TN27H	033242	TN27J	033362
18	TN27K	033422	TN27L	033520	TN27M	033530
19	TN27N	033542	TN27OT	033306	TN27P	033626
20	TN27R	033650	IN3	020006	TN3A	020024
21	TN3B	020046	TN3C	020064	TN3D	020102
22	TN3E	020120	TN3ERR	020136	TN3OUT	020132
23	TN3O	033712	TN30A	033744	TN30B	034032
24	TN30E	034126	TN30EX	034116	TN30F	034140
25	TN31	034204	TN32	035532	TN32A	035752
26	TN32EX	036060	IN32LP	035574	TN33	036144
27	TN33EX	036210	TN34 =	***** GX	TN35 =	***** GX
28	TN36 =	***** GX	TN37 =	***** GX	TN4	020244
29	TN4A	020354	TN4B	020374	TN4C	020464
30	TN4D	020500	TN4E	020566	TN4ERR	021020
31	TN4EX	020326	TN4F	020602	TN4FIN	021024
32	TN4G	020712	TN4H	021014	TN4O =	***** GX
33	TN4I =	***** GX	TN4J =	***** GX	TN43 =	***** GX
34	TN44 =	***** GX	TN45	042762	TN46	043314
35	TN46A	043322	TN46B	043350	TN46C	043360
36	TN46EX	043474	TN47	043506	TN5	021110
37	TN5A	021200	TN5AA	021146	TN5AB	021156
38	TN5B	021244	TN5C	021302	TN5D	021336
39	TN5ERR	021400	TN5OUT	021374	TN5O =	***** GX
40	TN6	021544	TN6C	021636	TN6CHK	022112
41	TN6D	021660	TN6E	021674	TN6ERR	022104
42	TN6F	021704	TN6J	021764	TN6K	022004
43	TN6OUT	022100	TN7	022216	TN7A	022244
44	TN7B	022304	TN7C	022336	TN7D	022406
45	TN7ERR	022430	TN7OUT	022424	TOS1	006146
46	TCS2	006166	TPB	005730	TPS	005726
47	TRASH	005542	TRSH	006270	TRSH1	006302
48	TSTACT	005524	TSTADR	001356	TSTART	003044
49	TSTBDR	001366	TSTCA	003222	TSTCB	003254
50	TSTCON	003106	TSTCTL	003342	TSTDSK	021100
51	TSTINT	005750	TST1	003404	TST2	003366
52	TST3	003466	TS1	006000	TS2	006026
53	TS3	006030	TS3A	006060	TS4	006112
54	TS5	006120	TTBAD	005336	TTBUF	005550
55	TTERR	012030	TTISEV	005770	TTOINT	005716
56	TTOSEV	006136	TT010	005266	TT011	005274
57	TT012	005302	TT013	005310	TT014	005314
58	TT015	005324	TT02	005150	TT03	005156
59	TT05	005174	TT06	005200	TT07	005210
60	TT08	005226	TT09	005240	TTSTAR	006170
61	TTWORK	005746	TTYACT	005536	TTYIN	004650
62	TTYINT	005720	TTYOUT	005134	TTYPUT	001104

6	TTYSET	015414	TTYSEX	015436	TTZ	004672
7	TTZZ	004710	TT04	005164	TT1	004734
8	TT10	005122	TT2	004760	TT3	004766
9	TT4	005002	TT5	005012	TT6	005014
10	TT6A	005020	TT7	005026	TT8	005104
11	TT9	005114	T1MSG	010434	T15EX	024310
12	T16WB	024652	T2MSG	010464	T31EX	034706
13	T31RLP	034454	T31WLP	034242	T6DONE	022140
14	UNIFLD=	030000	UNIMSK=	147777	UNIT	001240
15	UPD	036034	WAIT	017342	WAIT1	022164
16	WAIT1A	022174	WHSCCB	027156	WHSCRC=	000014
17	WORCHD=	000020	WMSG	001765	WPORCB	026336
18	WPRBIT	001304	WPSEC	001046	WRC	035356
19	WRCB	035520	WRCEX	035506	WRCHK =	000026
20	WRD1	044272	WRD2	044274	WRPT	044262
21	WRTBLK	023602	WRTCHD=	000006	WRTECC	040644
22	WRTERR	001174	WRT1	040662	WSMSG	011550
23	WTEXT	017374	WTPL	017356	WTPLA	017352
24	WTPL1	017410	SRN1	015612	SRN2	015614
25	SRN3	015620	SR1	036276	SR2	036334
26	SR3	036374	SR4	036426	SR5	036460
27	STN20	026114	STN20A	026120	STN20B	026236
28	STN27	032342	STST1	003124	ST61	021612
29	ST62	021622	SSCON =	***** 6	S2	036152
30	S222	036170	S3	036202	S4	036214

• ABS. 054314 000  
000024 001

ERRORS DETECTED: 1  
FREE CORE: 3283. WORDS  
PHOENX,PHOENX<SMD1.P11,SMD2.P11

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XYLOGIC OEM COMPONENTS GROUP, INC.

42 Third Avenue

Burlington, Massachusetts 01803

617-272-8140

Phoenix 200 Disk Controller

User Interface Manual

Dwg. No. 1043-04

Revision B

Date June 3, 1976

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## 1.0 Introduction

It is the intent of this manual to provide the user with sufficient technical information to enable him to successfully design an adapter to interface the Phoenix 200 Disk Formatter to current generation computers with a minimum of difficulty.

The information contained in this manual is principally concerned with the physical, electrical, and timing interface provided to the user by the Phoenix 200 Disk Formatter, and the use thereof by the user in any computer adapter design.

The functional capabilities, performance characteristics, and programming interface of the Phoenix 200 Disk Formatter are explained in great detail in the Phoenix 211 Disk Controller Programming Reference Manual. The user should be equally familiar with the contents of the programming manual, as well as this manual before attempting the detailed design of any computer adapter for the formatter.

This manual will be expanded and updated as required to provide the user with complete, accurate, interfacing information for the Phoenix 200 Formatter.

Any questions relating to the content of this manual should be directed to:

Engineering Department  
Xylogic OEM Component Group, Inc.  
42 Third Avenue  
Burlington, Mass. 01803  
617-272-8140



#### 4.0 User Interface Signal Definitions

Note: All formatter interface signals are low active.

#### 4.1 Data Buss: DBOL-DB15L (Bidirectional)

The 16 Bidirectional DATA lines are used to transmit Register Data and DMA Data from/to the computer Interface Card from/to the Formatter. Data Buss timing is explained in detail in the Timing Diagram Section.

#### 4.2 Register Control: RCO(L) - RC3(L) (to Formatter)

The four Register control lines are used to select a register located in the formatter for purposes of reading or writing. The information on these lines along with the appropriate strobe define which Register will be written or read.

#### 4.3 Word Count Overflow: WCROVFL (to Formatter)

A pulse or a High to Low Transition On Line indicates to the formatter that the Word Count Register in the user interface card has overflowed meaning then the most significant bit of that register has made a TRUE to FALSE transition. DMA Requests will no longer be issued by the 211 formatter when the overflow condition occurs. Refer to DMA timing section.

#### 4.4 Computer Initialize: INIT (L) (to Formatter)

This is a pulse which causes the formatter to revert to the quiescent state; i.e. reset. This line may be used to disable the formatter if the computer power is lost, or to clear the formatter in the case of illegal commands or unusual conditions.

#### 4.5 Direct Memory Data In: DMDATI (L) (to Formatter)

When Active, this signal causes the Formatter to place DMA data on the bidirectional data bus for use by the user computer interface. The data placed on the bus interface is data that the formatter has read from the disk. The user may strobe data 200NS after DMDATI(1) is activated by user. Refer to DMA Timing section.

#### 4.6 Direct Memory Data Out: DM DATO (L) (to Formatter)

This is a pulse which is used by the formatter to strobe data supplied by the computer interface during a DMA write operation. The user puts the DMA data to be read by the formatter on the bus and waits a minimum of 150NS before activating DMDATO(L).

The formatter normally strobes data into one of the internal FIFO memories on the leading edge (High to Low) of DMDATO(L). DMDATO(L) must be a minimum of 100NS wide and maximum frequency is 2.0 to MHZ. Refer to DMA timing section.

4.7 Interrupt Acknowledge: INTRACKL (to Formatter)

This is a pulse which is issued by computer interface to inform the formatter that the host computer has acted upon the Formatter's Interrupt request. This causes the Interrupt Request signal to be cleared. Interrupt Request is also cleared when any new command is issued to the formatter.

4.8 Direct Memory Direction: DMDIRL (from Formatter)

This is a level which when active (Low) indicates that the DMA Transfer taking place is from the formatter to the user Interface, i.e. Read. When this signal is false the direction is defined as computer interface to Formatter, i.e. WRITE. This signal state is defined when any data transfer command is initiated and the formatter becomes "busy."

4.9 Load "Q" Buss Address Register: LDQBAR (L) (from Formatter)

This is a pulse which is used by the user interface to load Data via the Formatter Data Buss into the user Interface Buss address Register. This signal is only used in "Q" mode of operation.

4.10 Load "Q" Memory Extension Register: LDMEX (L) (from Formatter)

This is a pulse which is used by the user interface to load data via the formatter Data Buss into the user interface memory extension of the Command Status Register. This signal is only used in the "Q" mode of operation.

4.11 Load "Q" Word Count Register: LDQWCR (L) (from Formatter)

This is a pulse which is used by the user interface to load data via the formatter Data Buss into the user Interface Word Count Register. This signal is used only in the "Q" mode of operation.

4.12 Data In Strobe: DSDATIL (to Formatter)

This signal gates the register data as defined by the register control lines to the computer interface on the Data Buss. Refer to Register timing section for data validity.

**4.13 Formatter Error Condition: FECOND (L) (to Formatter)**

This is a level from the computer interface signifying that an error condition exists in the computer interface. Any command currently in progress (Read, Write) will be aborted. The general error bit will be set in the formatter and an interrupt generated.

**4.14 Data Out Strobe: DSDATOL (to Formatter)**

This is a pulse which causes the formatter to copy the data from the Data Buss into the register selected by the Register Control lines. Refer to Register timing for further information.

**4.15 Enable MMu Control: ENBMM (L) (to Formatter)**

A pulse (200ns min. 500ns max) on this line causes the "Q" mode control to execute one instruction sequence. This must only be issued if the host computer will not be accessing the formatter or the computer interface for the next 800ns. This includes DMA, Interrupt, Register reading and writing. This signal is used only in Command Queue Mode.

**4.16 System Initialize: SYSINITL (from Formatter)**

This is a pulse generated by the user to initialize all logic within the formatter to a defined quiescent state. This signal is also generated by the Formatter Clear Command.

**4.17 Interrupt Request: INTRL (from Formatter)**

When active this signal informs the computer interface that the formatter has completed the commanded operation. User software should interrogate formatter registers to determine if the commanded operation was performed successfully. This signal, once active, is reset when the leading edge of the user generated Interrupt Acknowledge Signal is generated.

**4.18 Load Low Byte Of Command and Status Register: LDLCSRL (to Formatter)**

This is a pulse which causes the formatter to copy Data from the low order Byte of the Data Bus (DB $\emptyset$ -DB7) into the low order byte (Bits  $\emptyset$ -7) of the Command and Status Register. (Refer to Register Timing Diagram).

**4.19 Load High Byte of Command and Status Register: LDHCSRL (to Formatter)**

This is a pulse which causes the formatter to copy data from the high order Byte of the Data Bus (DB8-DB15) into the high order Byte (Bits 8-15) of the Command and Status Register. (Refer to Register Timing Diagram).

#### 4.20 DMA Request Signal DMR(L) (FROM Formatter)

1. This signal is used by the formatter to initiate DMA transfers via the user interface, DMR(L).
2. DMR(L) is associated with the state of the Formatter internal FIFO memory.
3. In a Write operation the request signal will be active when the controller is busy, the associated FIFO memory buffer is not full, and the Word Count Overflow (WCROVFL) Signal has not been received from the user interface.
4. In a Read operation the request signal will be active when the controller is busy, the associated FIFO memory buffer contains any disk data, and the Word Count Overflow (WCROVFL) Signal has not been received from the user interface.
5. The user interface must sample the state of the DMA request signal.
6. The DMACK(L) signal is utilized to enable the user interface DMA cycle look-a-head capability required for multiple cycle DMA transfers on certain computers.

#### 4.21 DMA Acknowledge Signal: DMACK(L) (To Formatter)

1. This signal acknowledges the current DMA Request.
2. The DMACK(L) Signal is used to detect the state of the formatter's FIFO memory and modify the DMA Request Signal accordingly.
3. DMA Request can be sampled 200ns min. after the leading edge of the DMACK Signal.

## 5.0 Loading and Reading of Internal Formatter Registers

The Phoenix 200 Formatter contains a number of internal 16 bit registers which are necessary to be loaded with parameters or interrogated under direct program control by the user. The following sections are devoted to defining the user procedures to be followed in register addressing, loading and reading program control operations.

Note that some of the internal registers provided in the Phoenix 200 Formatter are applicable only to formatters equipped with special extra cost options.

### 5.1 Phoenix 200 Formatter Register Addressing

- 5.1.1 A register is selected by the user for reading or writing under direct program control by controlling the state of four register select signals [RC0(L) - RC3(L)] provided.
- 5.1.2 Specific internal registers contained in the Phoenix 200 Formatter and the associated assigned register select signal state required to address them are contained in Table 1.

Specific functional read, write capabilities of each register is also indicated, as well as those registers that are applicable to specific optional configurations of the formatter.

### 5.2 Register Loading

#### 5.2.1 Register Load Sequence Overview

Internal registers in the Phoenix 200 Formatter are loaded by:

1. Selecting the register to be loaded by appropriately controlling the states of Register Select Signals RC0(L) - RC3(L).
2. Gating onto the 16 bit formatter data bus (DB0L-DB15L) the data that is to be loaded into the selected register.
3. Supplying a 250NS minimum strobe pulse (DSDATOL) to be used by the formatter to strobe the data on the formatter data bus into the selected register.

The user interface controls completely the register loading operation, and the associated timing. The only timing requirement placed upon the user is to guarantee the validity of the data and register select buss during the DSDATOL strobe pulse.

### 5.2.2 Command & Status Register Loading

The Command and Status Register is loaded by:

1. Gating onto the 16 Bit Formatter data bus (DB0L-DB15L) the data that is to be loaded into the command and status register.
2. Supplying a 250ns minimum strobe pulse (LDLCSRL or LDHCSRL) to be used by the formatter to strobe data into the command and Status Register.
3. The LDLCSRL Signal is used to load the low order byte of the Command and Status Register. The LDHCSRL Signal is used to load the high order byte of the Command and Status Register.
4. The LDLCSRL and LDHCSRL signals may be issued separately or together. The DSDATOL signal should be suppressed when the loading of the Command and Status Register takes place.

TABLE 1  
PHOENIX 200 DISK FORMATTER  
INTERNAL REGISTER SELECT STATE ASSIGNMENTS

RC3 (L)	RC2 (L)	RC1 (L)	RC0 (L)	REGISTER SELECTED	READ/WRITE USAGE
0	0	0	0	Control & Status Register**	:READ ONLY
0	0	0	1	Unit, Select, Head Register	:READ/WRITE
0	0	1	0	Not Used	:READ/WRITE
0	0	1	1	Disk Word Count Register	:WRITE ONLY
0	1	0	0	Cylinder Address Register	:READ/WRITE
0	1	0	1	Disk Status Register	:READ/WRITE
0	1	1	0	Error Register	:READ ONLY
* 0	1	1	1	Queue Mode Control & Status	:READ/WRITE
* 1	0	0	0	Queued Control & Status For Drive N	:READ/WRITE
* 1	0	0	1	Queued Unit, Sector Head Reg. for Drive N	:READ/WRITE
* 1	0	1	1	Queued Word Count Reg. For Drive N	:READ/WRITE
* 1	1	0	0	Queued Cylinder Address Reg. For Drive N	:READ/WRITE
* 1	1	0	1	Spare	:READ/WRITE
* 1	1	1	0	Spare	:READ/WRITE
* 1	1	1	1	Queued Strip Buss Address Reg. For Drive N	:READ/WRITE

\*\*The Control and Status Register is loaded by using the LDLCSRL or LDHCSRL Signals appropriately.

\*Refers to optional features of Formatter.

Note: A logical '1' is defined as active in this table. (Signals at interface are actually active when Low.)

### 5.2.3 Register Load Sequence Timing

A detailed definition of the timing requirements and relationships of all signals involved in a formatter register load operation is given in Figure 5.1.

### 5.3.1 Register Read Sequence Overview

Internal registers in the Phoenix 200 Formatter are interrogated or read by:

1. Selecting the register to be read by appropriately controlling the status of Register Select Signals RCO(L)-RC3(L).
2. Commanding the formatter to gate the contents of the selected register onto the 16 bit data bus (DBOL-DB15L) by enabling the DSDATIL signal.
3. Waiting for the formatter data bus contents to be valid, and then gating the register data into the user interface logic with an internal strobe signal.

In the formatter register read sequence depicted above, the user completely controls the operations and associated timing. Any timing requirements imposed upon the user are only to guarantee register select and data validity.

### 5.3.2 Register Read Sequence Timing

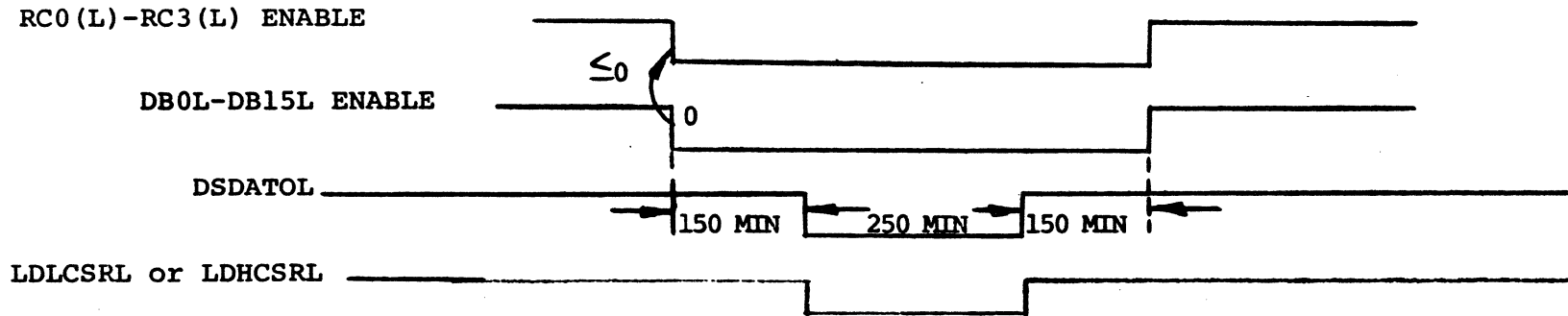
A detailed definition of the timing requirements and relationships of all signals involved in a formatter register read operation is given in Figure 5.2.



FIGURE 5.1

XYLOGIC PHOENIX 200 FORMATTER

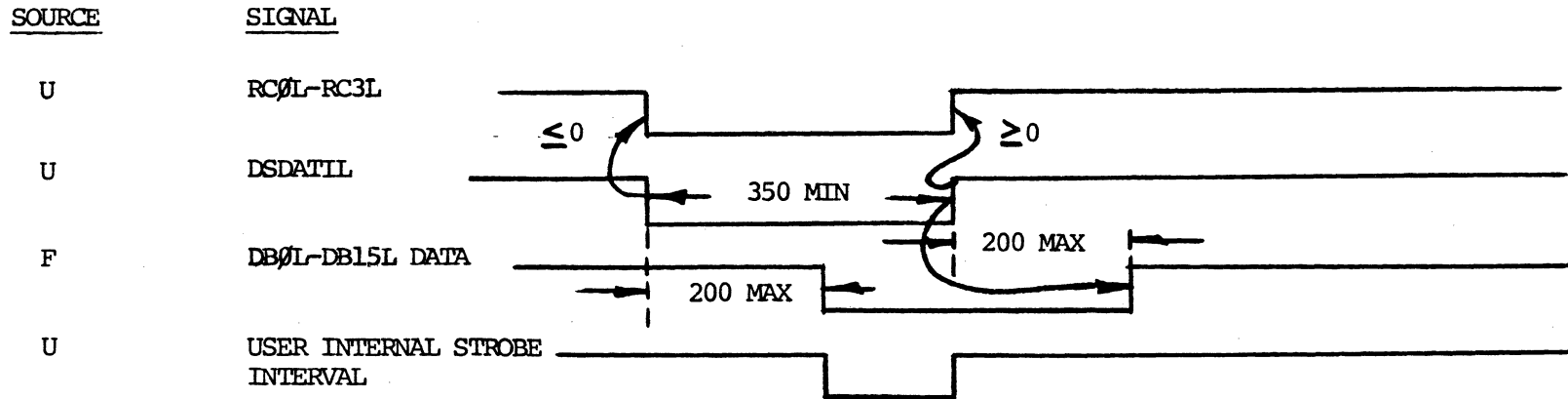
REGISTER LOAD TIMING DIAGRAM



NOTES

1. Timing is at Formatter Interface Connector
2. All signals are active when Low (Negative Logic) at Interface.
3. All times are in nanoseconds.
4. RC0(L) - RC3(L) and DSDATOL not applicable on Command & Status Register Loading.

FIG 3 5.2  
XYLOGIC PHOENIX 200 FORMATTER  
REGISTER READ TIMING DIAGRAM



NOTES:

- 1.) Timing is at Formatter interface connector.
- 2.) All signals are low active (Negative Logic)
- 3.) All times are in nanoseconds.

## 6.0 Interrupt Request Timing Sequence

### 6.1 Interrupt Operation Definition

When the Phoenix 200 Formatter completes any commanded disk operation (except Clear, or Release,) the formatter will generate a signal to the user interface. This signal is normally used by the user interface to generate an interrupt to the operating computer program to enable it to reallocate the disk subsystem resource to some new task.

The interrupt request signal (INTRL) will be generated at the end of a disk operation, independently of whether the operation just completed was completed successfully or not. It is up to user software to test the error summary bit to determine whether an error did occur during the previous commanded operation and to take appropriate action.

### 6.2 Interrupt Timing Reference

All timing given is at the user interface 10' from the Phoenix 200 Formatter.

### 6.3 Interrupt Sequence Overview

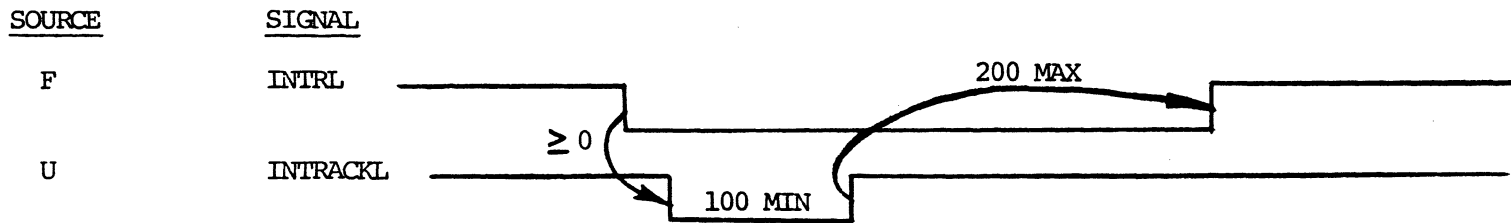
Two signals are involved in the interrupt operation INTRL and INTRACKL. At the end of a commanded disk operation the formatter initiates the interrupt sequence by activating INTRL. The user then completes the sequence by activating the interrupt acknowledge signal INTRACKL.

Upon detection of the INTRACKL Signal the formatter removes the INTRL signal. The only timing requirement imposed by the formatter is that the INTRACKL Signal generated by the user be at least 100NS wide.

### 6.4 Detailed Interrupt Sequence Timing Information

Figure 6.0 shows all applicable interrupt timing relationships and requirements.

FIG 6.0  
XYLOGIC PHOENIX 200 FORMATTER  
INTERRUPT TIMING DIAGRAM



NOTES:

- 1.) Timing is at Formatter interface connector.
- 2.) All signals are active when low (Negative Logic) at interface.
- 3.) Formatter becomes "Ready" during INTRL.
- 4.) All times are in nanoseconds.

## 7.0 Write Direct Memory Access Timing Sequence

### 7.1 Write Operation Definition

A "Write" disk formatter operation, for purposes of this discussion, is defined as being a transfer of 16 bit data words from the user interface to one of the formatter internal FIFO memories and thence to the selected disk drive.

### 7.2 Interface Timing Reference

All timing information given, unless otherwise specifically noted, is at the Formatter cable interface.

### 7.3 Write Operation Initiation

A "Write" operation is initiated by activating the Formatter "Go" bit after properly loading the Formatter registers with appropriate parameters defining the specific operation to be performed.

Note: A complete disk controller consisting of the Phoenix 200 Formatter and a user computer interface actually contains two Word Count Registers, one within the user interface and one within the 200 Formatter.

The user interface Word Count Register controls the number of words transferred between the Phoenix 200 Formatter and computer memory, while the formatter word count register controls the number of words transferred between the formatter and the selected disk drive.

Both Word Count Registers are loaded at the same time.

### 7.4 DMA Direction Establishment by DMDIR

When the write operation is specified, the formatter immediately establishes the direction of all DMA data transfers required by putting formatter signal DMDIR in the inactive (high) state.

This signal will remain at this high level for the duration of any write operation.

## 7.5 DMA Transfer to Formatter FIFO Memory's Overview

1. At the start of a writer operation the internal formatter FIFO memories are empty.
2. The formatter will request data transfers from the user interface to fill the buffer memories before disk synchronization is accomplished.

Once the FIFO buffer memories are full, DMA requests are made only on a demand basis to keep the buffers full until the Word Count Overflow Signal (WCROVFL) is detected.

3. The formatter contains an internal timer which guarantees that the internal FIFO memories have had time to be sufficiently loaded with data before data transfers between the FIFO memories and the disk drive are allowed to begin.

Note: The guaranteed buffer load period is variable and may have to be increased if the maximum DMA data transfer rate possible through the user interface is not fast enough.

The factory and interval setting should be adequate for all current generation computers.

## 7.6 DMA Write Data Transfer Cycle Sequence (Reference Fig.7 .)

- 7.6.1 Each DMA write cycle data transfer is initiated by DMR (L) being active, indicating that the associated buffer is not full and is requesting more data.
- 7.6.2 Upon detection of DMR (L) (and the availability of data from computer) the user should put the data for the next word to be transferred on the formatter bidirectional data bus.
- 7.6.3 A minimum of 150NS. later the user initiates the strobing of the data into one of the internal formatter FIFO memories by activating the DMDATO signal.

(The 150NS delay from data enabling to leading edge of data strobe allows for data skew, propagation, and settling time.)

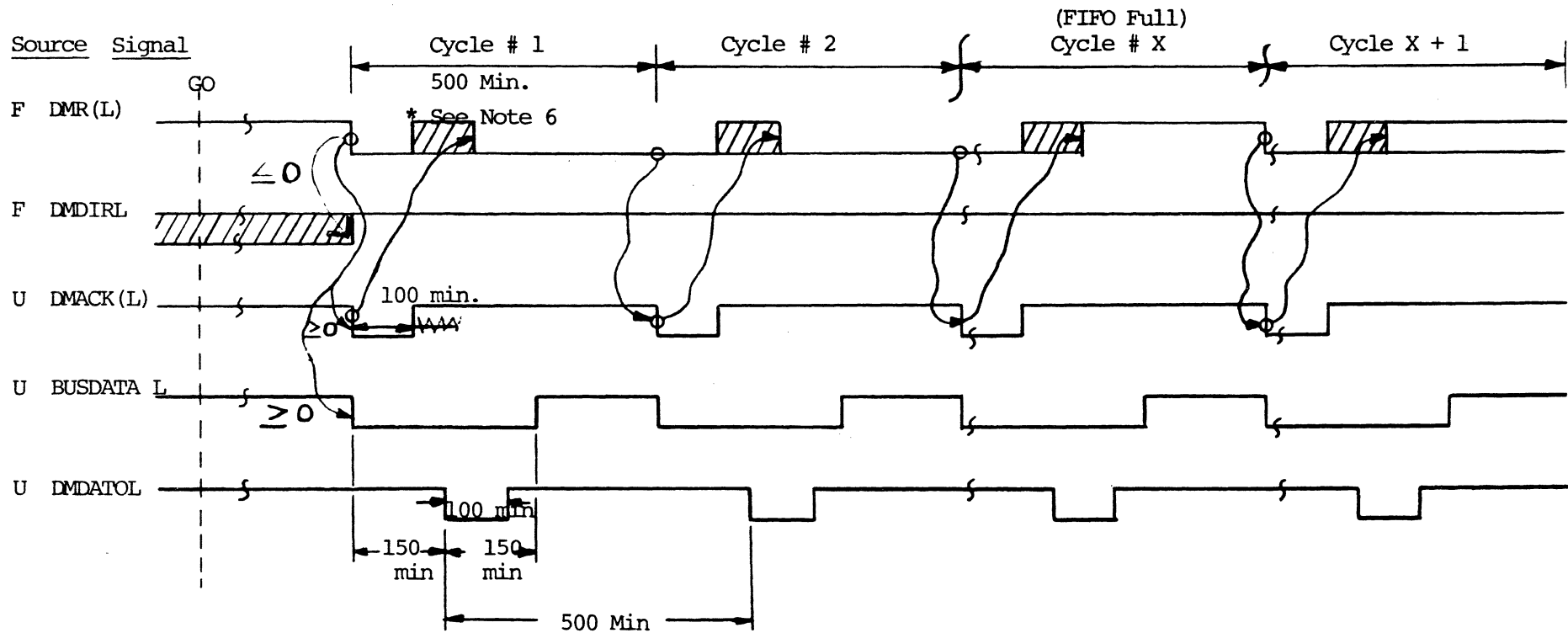
- 7.6.4 The DMACK Signal may be issued at any time during the current cycle or at some convenient time previous to the current cycle. (DMA Look Ahead).
- 7.6.5 The DMDATO Data Strobe Signal should be a minimum of 100NS wide.
- 7.6.6 The user must maintain data on the bus 150NS minimum after the leading edge of the DMDATO Signal.
- 7.6.7 The DMA request signal associated with the FIFO memory loaded by the data transfer will become valid a minimum of 200NS from the leading edge of the DMACK Signal providing the FIFO memory is not yet full.
- 7.6.8 After the data for a given cycle has been transferred per the above, subsequent DMA transfers may take place by repeating the sequence as appropriate.

DMDATA Strobe Signal frequency must not exceed 2.0MHZ (500NS period).

Note: The user effectively controls the Write DMA data transfer rate and timing by controlling the DMDATA and DMACK Signals.

- 7.6.9 The user interface logic should increment the Word Count Register at the beginning of each DMA transfer cycle so that a logic decision to terminate upon Word Count Register Overflow can be reached before the end of the last cycle.
- 7.6.10 Write DMA data transfers from the user interface to the formatter internal FIFO memories terminate when the Word Count Overflow Signal (WCROVFL) is received from the user interface. DMR (L) if active will be returned to the inactive state within 200NS of the leading edge of the WCROVFL Signal.
- 7.6.11 The Word Count Register Overflow Signal generated by the user interface may be either a pulse or a level but must be a minimum of 100NS wide.
- 7.6.12 If the Word Count Overflow Signal is issued prematurely by the user, DMA transfers terminate immediately, but the controller will continue to write alternately the last two words transferred to the FIFO memories onto the selected disk until the formatter internal Word Count Register Overflows and the end of the last addressed sector is reached.

FIGURE  
Phoenix 200 Formatter  
Write DMA Timing Diagram (3 Full Cycles)



Notes:

1. Timing is at Formatter Interface Connector
2. All Signals are active when low (Negative Logic) at Interface
3. Data On Buss is valid during DMDATO Pulse Interval
4. Transfer rate is controlled by user by controlling frequency of DMDATO and DMACK
5. All times are in nanoseconds
6. DMR(L) is not valid until 200 ns min. after leading edge of DMACK(L)



## 8.0 Read Direct Memory Access Timing Diagram

### 8.1 Read Operation Definition

A "Read" disk formatter operation for purposes of this discussion is defined as being a transfer of 16 bit data words from the selected disk to the Phoenix 200 Formatter and thence to the user interface.

### 8.2 Interface Timing Reference

All timing information given, unless otherwise specified, is at the Formatter interface connector.

### 8.3 Read Operation Initiation

A "Read" operation is initiated by activating the formatter "GO" bit after properly initializing the formatter registers with appropriate transfers defining the specific operation to be performed.

### 8.4 DMA Direction Establishment by DMDIR Signal

When the read operation is specified the formatter immediately establishes the direction of all DMA data transfers required by forcing the DMDIR Signal to the active state (low).

This signal will remain at this state for the duration of any read operation.

### 8.5 DMA Transfer from Formatter to User Interface Overview

8.5.1 At the start of a read operation, the formatter internal FIFO memories are empty.

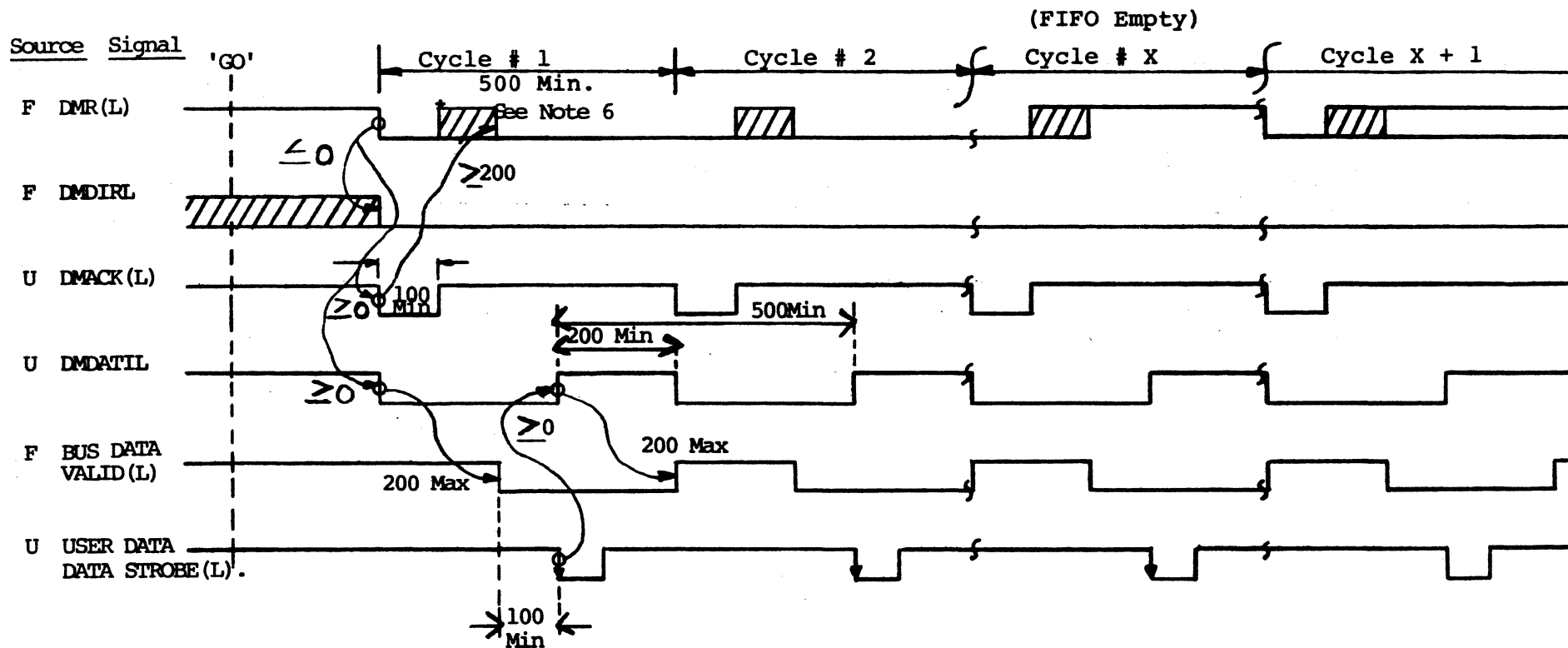
8.5.2 Data transfers from the selected disk to the FIFO memories will begin when the disk is on the correct cylinder and sector.

8.5.3 Words received from the selected disk are alternately temporarily stored in one of the two internal FIFO memories. All odd words are normally stored in FIFO memory #1 while all even words are stored in FIFO memory #2.

8.5.4 DMA Data transfers to the user interface are initiated when data is present in the FIFO memory and will persist until no data is contained in either FIFO memory.

- 8.5.5 Data flow from the selected disk to the FIFO memories terminates when the formatter internal Word Count register overflows.
- 8.5.6 Data flow from the FIFO memories to the user interface terminates when the Word Count Register in the user interface overflows and activates the WCROVFL Signal.
- 8.6 DMA Read Data Transfer Cycle Sequence (Reference Fig. 8)
  - 8.6.1 Each DMA read cycle is initiated by DMR (L) being active, indicating that the associated FIFO memory buffer contains data to be transferred to computer memory via the user interface.
  - 8.6.2 Upon detection of DMR (L) the user, when his interface is ready to accept data, should activate the DMDATI Signal.
  - 8.6.3 The formatter, upon detection of the DMDATI Signal, will put the data to be transferred on the formatter data bus. A maximum of 200NS from the leading edge of a DMDATI pulse, data is guaranteed to be valid at the Formatter interface connector.
  - 8.6.4 The user should strobe data from the bus into the user interface 300ns minimum from the leading edge and during the DMDATI Signal Interval.
  - 8.6.5 The DMDATI Signal pulse must be a minimum of 350NS wide.
  - 8.6.6 The formatter, upon detection of the trailing edge of the DMDATI Signal Pulse, will immediately remove data from the formatter bus. Data, then, is not valid after DMDATI is removed.
  - 8.6.7 The DMDATI Signal, once removed at the end of a read DMA data transfer, must remain inactive for a minimum of 200 NS before it can be activated again for the next read DMA transfer cycle.
  - 8.6.8 The DMACK Signal may be issued at any time during the current cycle or at some convenient time previous to the current cycle. (DMA Look Ahead).
  - 8.6.9 The DMA request signal will become void a minimum of 200NS from the leading edge of the DMACK Signal providing there is another data word available in FIFO memory.

FIGURE 8  
Phoenix 200 Formatter  
Read DMA Timing Diagram (Two Cycles)



**Notes:**

1. Timing is at Formatter Interface Connector.
2. All signals are active when low (negative logic) at interface.
3. Data On Buss is valid 200 ns from leading edge of DMDATI to end of DMDATI Pulse.
4. Transfer rate is controlled by user by controlling frequency of DMDATI and DMACK.
5. All times are in nanoseconds.
6. DMR(L) is not valid until 200 ns min. after leading edge of DMACK(L).

8.6.10 After the read data for a given cycle has been transferred from the formatter to the user interface per above, subsequent read DMA transfers may take place as required by repeating the above sequence.

Note: The user effectively controls the read DMA Data Transfer Timing and data transfer rate by the DMDATI and DMACK Signals.

8.6.11 The user interface should increment the Word Count Register at the beginning of each read DMA data transfer cycle so that a logical decision to terminate upon word count overflow can be reached before the end of the last cycle.

8.6.12 Read DMA data transfers from the formatter to the user interface terminate when the Word Count Register overflow signal (WCROVFL) is activated by the user interface.

DMR (L) if active will be returned to the inactive state within 200NS of the leading edge of the WCROVFL Signal.

8.6.13 The WCROVFL signal may be either a pulse or a level but must be at least a minimum of 100NS wide.

## 9.0 DMA Data Transfer Considerations

- 9.1.1 Two First in First Out (FIFO) memories are contained in the Phoenix 200 Formatter. All data to be transferred to or from disk drives connected to the formatter is buffered in one of the two FIFO memories in the formatter.
- 9.2.1 The two FIFO memories in the formatter are alternately used for temporary data storage on a word basis in order to maximize DMA data transfer throughout rate.  
  
Normally all odd words are buffered in FIFO1 while all even words are buffered in FIFO2.
- 9.3.1 Maximum theoretical DMA transfer 16 bit word transfer rate is 2.0 MHZ which is more than ample for interfacing to current generation computers.
- 9.4.1 The actual DMA transfer rate in a disk subsystem using the Phoenix 200 Formatter is determined by the user.
- 9.5.1 All formatter interface signals are negative active at the user connector.
- 9.6.1 DMA data transfers normally utilize the same 16 bit bidirectional data bus used for direct program control register loading and reading.

DMA data transfers may be optionally made over a separate 16 bit bidirectional data used exclusively for DMA.

Such an interface is available on all printed circuit versions of the Phoenix 200 Formatter and requires a separate cable and associated connectors.

- 9.7.1 If the standard data buss is used for DMA data transfers, the user interface must resolve any formatter bus usage arbitration necessary to insure that no attempt is made to use the formatter bus for DMA and direct program control operations during the same physical bus cycle.
- 9.7.2 The DMACK Signal must be issued only once for each DMA data transfer.

USER INTERFACE CONNECTOR SIGNAL/PIN ASSIGNMENT

PIN #	SIGNAL NAME	DIRECTION
1	GND	-
2	GND	-
3	GND	-
4	DB0L	BI
5	DB1L	BI
6	DB2L	BI
7	DB3L	BI
8	DB4L	BI
9	DB5L	BI
10	DB6L	BI
11	DB7L	BI
12	DB8L	BI
13	DB9L	BI
14	DB10L	BI
15	DB11L	BI
16	DB12L	BI
17	DB13L	BI
18	DB14L	BI
19	DB15L	BI
20	RC0 (L)	TO FORMATTER
21	RC1 (L)	TO FORMATTER
22	RC2 (L)	TO FORMATTER
* 23	RC3 (L)	TO FORMATTER
24	WCROVFL	TO FORMATTER
25	INIT (L)	TO FORMATTER
26	DMDATI (L)	TO FORMATTER
27	DMDATO (L)	TO FORMATTER
28	INTRACKL	TO FORMATTER
29	LDHCSRL	TO FORMATTER
30	DSDATIL	TO FORMATTER
31	FECOND (L)	TO FORMATTER
32	DSDATOL	TO FORMATTER
* 33	ENBMM (L)	TO FORMATTER
34	SYSINITL	FROM FORMATTER
35	INTRL	FROM FORMATTER
36	DMRL	FROM FORMATTER
37	DMDIRL	FROM FORMATTER
* 38	LDQBAR (L)	FROM FORMATTER
* 39	LDMEX (L)	FROM FORMATTER
* 40	LDQWCR (L)	FROM FORMATTER
* 41	ENQDATAL	FROM FORMATTER
42	DMACK (L)	TO FORMATTER
** 43	No Strip (L)	FROM FORMATTER
44	LDLCSRL	TO FORMATTER
45	SPare	-
46	Spare	-
47	Spare	-
48	GND	-
49	GND	-
50	GND	-

CONNECTOR TYPE USED ON BOARD  
1 of FORMATTER:

3M # 3433-1002

## Notes:

1. BI Denotes Bidirectional  
signal

\*\* Used in strip option only

RECOMMENDED INTERFACE

Drivers, Receivers, Termination, and Cable

SIGNAL LEVEL DEFINITION:

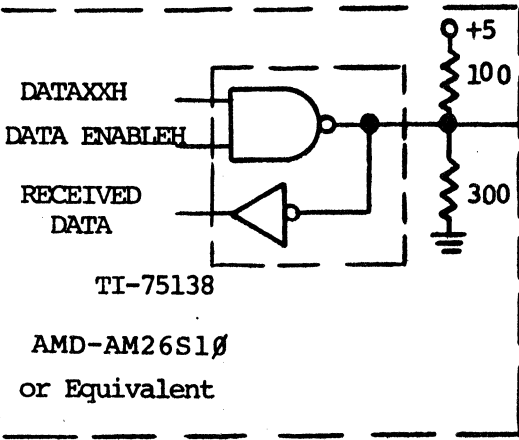
ALL SIGNALS ARE LOW, ACTIVE TRUE

LEVELS: TRUE= LOW= 0.7 VDC @ 100MA

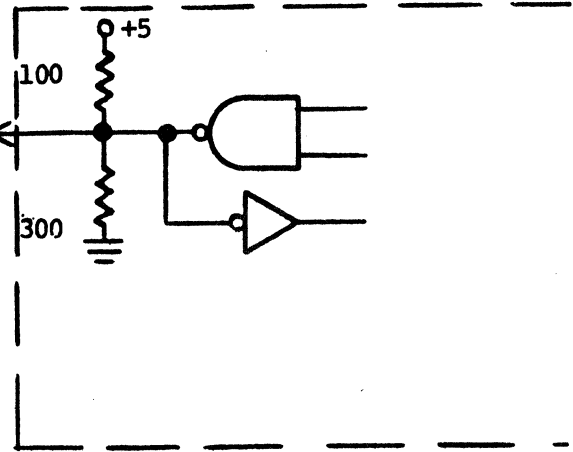
FALSE= HIGH= 3.5VDC

DATA BUS DRIVERS/ RECEIVERS/ TERMINATION (BIDIRECTIONAL)

CUSTOMER INTERFACE

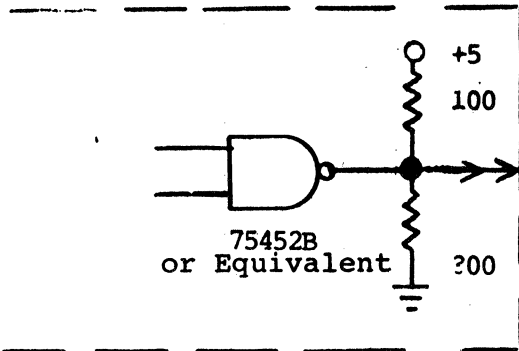


FORMATTER

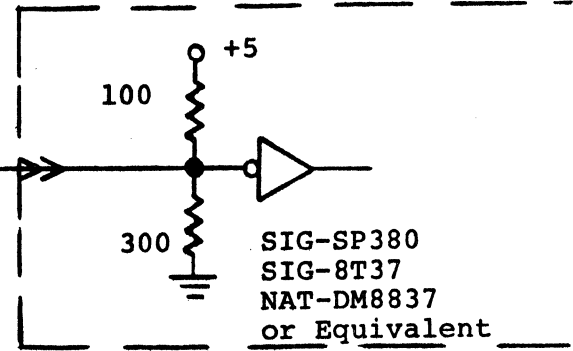


CONTROL SIGNALS DRIVERS/RECEIVERS/TERMINATION

CUSTOMER/FORMATTER



CUSTOMER/FORMATTER



RECOMMENDED CABLE

3M Part No. 3476/50; Flat Cable with Ground Plane and Drain Wire

XYLOGIC OEM COMPONENTS GROUP, INC.

42 Third Avenue

Burlington, Massachusetts 01803

617-272-8140

Phoenix 211 Disk Controller

Optional Data Port

User Interface Manual

Dwg. No. 1043-09

Revision A

Date August 1, 1976



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## 1.0 Introduction

It is the intent of this manual to provide the user with sufficient technical information to successfully interface external equipment to the optional data port interface provided by the Xylogic Phoenix 211 Disk Controller with a minimum of difficulty.

The information contained in this manual is principally concerned with the physical, electrical, and timing interface provided to the user by the optional data port of the Phoenix 211 Disk Controller.

The functional capabilities, performance characteristics, and programming interface of the Phoenix 211 Disk Controller are explained in greater detail in the Phoenix 211 Disk Controller Programming Reference Manual. The user should be equally familiar with the contents of the programming manual, as well as this manual before attempting to interface external equipment to the Phoenix 211 optional data port.

This manual will be expanded and updated as required to provide the user with complete, accurate, interfacing information for the Phoenix 211 Optional Data Port.

Any questions relating to the contents of this manual should be directed to:

Engineering Department  
Xylogic OEM Components Group, Inc.  
42 Third Avenue  
Burlington, Mass. 01803  
617-272-8140

## 2.0 Optional Data Port Description (Reference Figure 1)

### 2.1 General Description

The Optional Data Port provided by the Phoenix 211 Disk Controller enables the user to conduct disk data transfers directly between external equipment and disk drive(s), under control of programs being executed in a PDP11 Computer.

In effect, this option separates the data transfer path from the control and status functions within the Phoenix 200 Formatter. The computer interface is utilized to initiate, control, and monitor the results of disk data transfers, while the actual data transfer takes place between user external equipment and the disk drives, via the Phoenix 200 Formatter.

## 2.2 Physical Description

The Optional Data Port physically is provided by a 50 pin ribbon cable connector located on board 2 of the Phoenix 200 Disk Formatter. This 50 pin ribbon cable connector contains a 16 bit bidirectional data bus over which data is to be transmitted to and received from during disk data transfers, as well as the control signals and ample grounds. Detailed descriptions of the signals provided on this interface are contained in subsequent sections of this manual.

## 3.0 Programming Definition of Optional Data Port

The use of the optional data port interface does not affect the programming of the Phoenix 211 Disk Controller. Operation of a Phoenix 211 disk controller utilizing the optional data port interface is identical to a standard Phoenix 211 disk controller, as defined in the Programmers Reference Manual, except that the data transfer occurs over the optional data port interface.

This assumes, however, that the external equipment will always be ready and able to respond appropriately to disk transfer operations initiated by the controlling computer. Any control signals needed for communication between the controlling computer and the external equipment required to guarantee the validity of this assumption must be provided by the user via some other means.

## 4.0 Optional Data Port Enabling

Any standard Phoenix 211 Disk Controller is equipped with the optional data port interface. The optional data port configuration is achieved by removing staples DØH-D15H and three additional control staples on board 2 of the Phoenix 200 Formatter. Said staples are shown on Logic Drawing D1033-01 sheet 1.

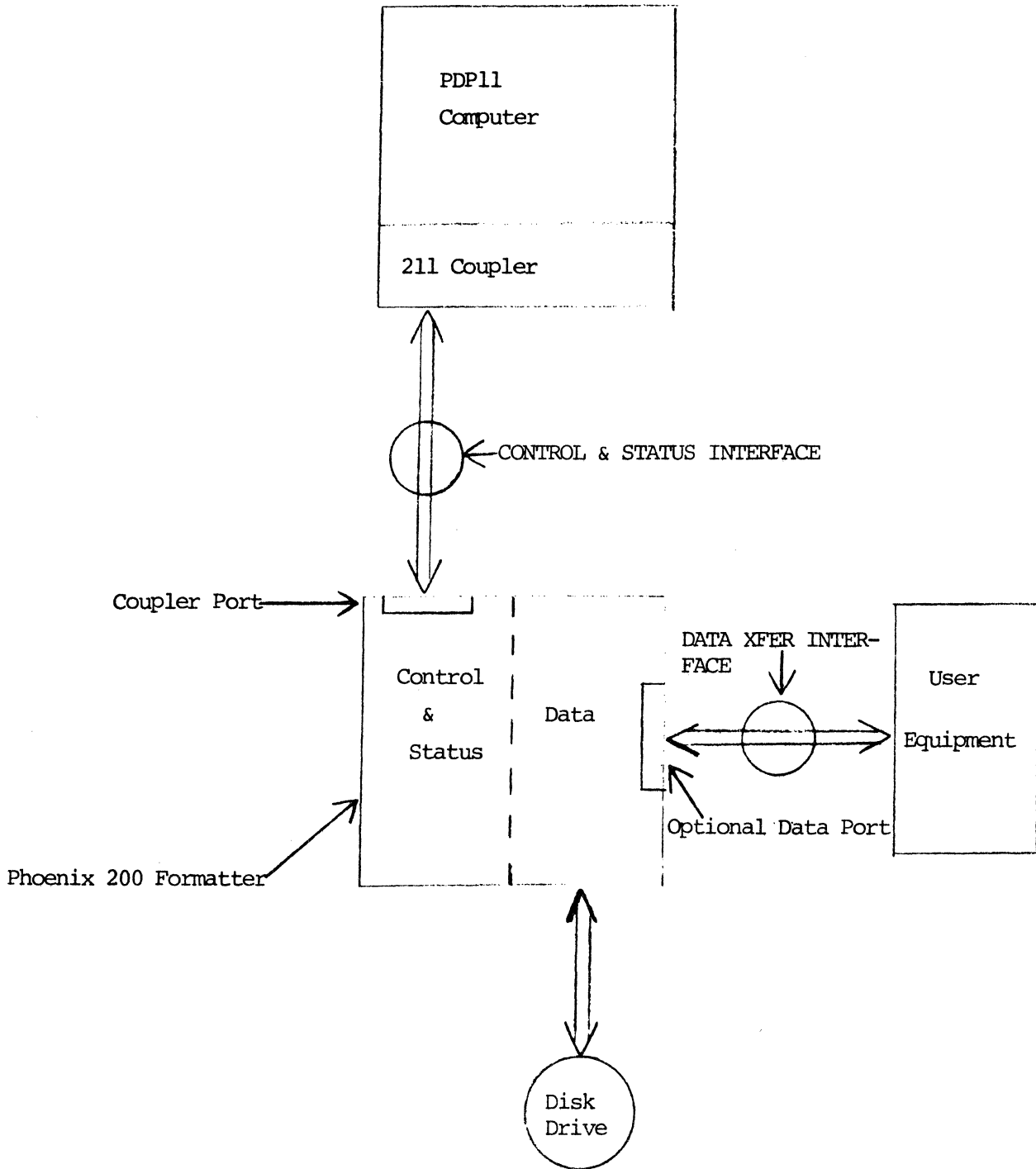
## 5.0 Optional Data Port Interface Testing

The optional data port interface, once enabled may be readily tested by connecting the computer coupler cable to the optional data port interface connector, and to the normal formatter coupler cable connector.

In this configuration data transfers will take place between the computer and disk drive via the optional port interface logic.

FIGURE 1

Phoenix 211 Optional Data Port Configuration



- Note:
1. The optional data port interface connector and coupler connector have the same functional signal/pin assignments to facilitate this operation.
  2. The required coupler cable can be readily configured by adding one additional coupler ribbon cable connector to the coupler cable 6" from the end of the formatter end of the coupler cable.

## 6.0 Data Transfer Mode Switching

Disk transfers may be conducted between the controlling computer and disk or external equipment connected to the optional data port and disk. Switching between these two modes of operation normally requires manual connection of the appropriate coupler or external equipment cable to the optional data port interface connector.

Automatic program controlled mode switching requires the addition of one "Autoswitch" printed circuit board assembly to the disk controller at additional cost.

## 7.0 Optional Data Port User Interface Signal Definitions

Note: All interface signals are low active.

### 7.1 Bidirectional Data Bus = DMDATA0L-DMDATA15L

The 16 bit bidirectional data lines are used to transmit disk data between the internal disk formatter memory and user equipment normally connected to the optional data port interface connector. Timing relationships required in transferring data over the data bus is given in detail in section

### 7.2 Direct Memory Access Direction Control - DMDIRL (From Formatter)

This signal is a level controlled by the Phoenix formatter and sent to the user external equipment to define the direction in which data is to move over the data bus during any disk data transfers.

This signal is active (low) when data is to be transferred from the formatter to the user during any disk read data transfer operations.

This signal is inactive (high) when data is to be transferred from the user to the formatter during a disk write data transfer.

### 7.3 Data Transfer Request - DMREQ(L) (From Formatter)

- .1 This signal is used by the formatter to initiate data transfers between it and user equipment connected to the optional data port.
- .2 The DMREQ(L) signal is associated with the state of the formatter internal FIFO memory.
- .3 In a Disk Write operation the DMREQ(L) signal will be active when the formatter is busy, the internal FIFO memory buffers are not full, and the Word Count Overflow (WCROVFL) Signal has not been received from the user interface.
- .4 In a disk read operation the DMREQ(L) Signal will be active when the formatter is busy, the internal FIFO memory buffer contains any data (is not empty) and the Word Count Overflow (WCROVFL) Signal has not been received from the user interface.
- .5 The user interface must sample the state of the DMA Request Signal.
- .6 The DMACK(L) Signal is utilized to facilitate DMA look-ahead capability for multiple cycle transfers.

### 7.4 Data Transfer Acknowledge Signal - DMACK(L) (To Formatter)

- .1 This signal is issued by the user interface to acknowledge receipt of a DMREQ(L) signal from the formatter.
- .2 Upon receipt of the DMACK(L) signal the formatter interrogates the FIFO memory content and will modify the state of the DMREQ(L) signal accordingly.
- .3 The DMREQ(L) signal may be sampled 200 NS after the leading edge of DMACK signal to facilitate multiple cycle look-ahead transfer implementations.

### 7.5 Write Data Transfer Strobe- DMLDSTB(L) (To Formatter)

This signal is pulsed by the user interface to the formatter during a Write Data Transfer to the formatter when the data on the bidirectional data bus is valid.

This signal is used by the formatter to strobe data from the bidirectional bus into internal FIFO memory, and may be activated a minimum of 150 NS after data is gated onto the bidirectional data bus.

#### 7.6 Read Data Transfer Strobe - DMRDSTB(L) (To Formatter)

1. This signal is activated by the user interface during a read data transfer from the formatter to the user interface, when the user is ready to accept data from the formatter.
2. Upon receipt of the DMRDSTB(L) signal the formatter will put data on the bidirectional data bus.
3. Data will be guaranteed to be valid 150 NS after receipt of DMRDSTB(L) by formatter.
4. User may strobe data from bidirectional data bus any time after the 150 NS period.
5. The DMRDSTB(L) signal may then be removed. User may in fact use the trailing edge of the DMRDSTB(L) signal to strobe data from bus into his own logic.

#### 7.7 Word Count Overflow - WCROVEL (To Formatter)

A pulse or high-to-low transition indicates to the formatter that the word count register in the user interface has overflowed, and that no more data transfers will take place.

#### 7.8 Disk Transfer Done - DSKXFRD(L) (From Formatter)

This signal, when true, signifies that the disk word count register has overflowed and the formatter has reached the End of Sector mark. This signal is reset by issuing a new command to the formatter. The user interface may use this signal to detect data transfer errors. The error conditions are:

WRITE OPERATION: Disk Transfer Done occurs before the user word count overflows.

READ OPERATION: The user word count overflows before Disk Transfer Done is generated.

## 8.0 Disk Write Data Transfer Timing Sequence

### 8.1 Write Operation Definition

A "Write" disk formatter operation, for purposes of this discussion, is defined as being a transfer of 16 bit data words from the user interface to one of the formatter internal FIFO memories and thence to the selected disk drive.

### 8.2 Interface Timing Reference

All timing information given, unless otherwise specifically noted, is at the Formatter cable interface.

### 8.3 Write Operation Initiation

A "Write" operation is initiated by activating the Formatter "Go" bit after properly loading the Formatter registers with appropriate parameters defining the specific operation to be performed.

Note: A complete disk controller consisting of the Phoenix 200 Formatter and a user external equipment interface actually contains two Word Count Registers, one within the user interface and one within the 200 Formatter.

The user interface Word Count Register controls the number of words transferred between the Phoenix 200 Formatter and external equipment, while the formatter word count register controls the number of words transferred between the formatter and the selected disk drive.

Both Word Count Registers should be pre-set to the same count before any data transfer operation is initiated.

### 8.4 Data Transfer Direction Establishment by DMDIR

When the write operation is specified, the formatter immediately establishes the direction of all DMA data transfers required by putting formatter signal DMDIR in the inactive (high) state.

This signal will remain at this high level for the duration of any write operation.



## 8.5 Data Transfer to Formatter FIFO Memory Overview

1. At the start of a writer operation the internal formatter FIFO memories are empty.
2. The formatter will request data transfers from the user interface to fill the buffer memories before disc synchronization is accomplished.

Once the FIFO buffer memories are full, data transfer requests are made only on a demand basis to keep the buffers full until the Word Count Overflow Signal (WCROVFL) is detected.

3. The formatter contains an internal timer which guarantees that the internal FIFO memories have had time to be sufficiently loaded with data before data transfers between the FIFO memories and the disk drive are allowed to begin.

Note: The guaranteed buffer load period is variable and may have to be increased if the maximum data transfer rate possible through the user interface is not fast enough.

The factory interval setting should be adequate for all current generation computers.

## 8.6 Write Data Transfer Cycle Sequence (Reference Fig. 7)

- 8.6.1 Each write cycle data transfer is initiated by DMREQ (L) being active, indicating that the associated buffer is not full and is requesting more data.
- 8.6.2 Upon detection of DMREQ(L) (and the availability of data from user equipment) the user should put the data for the next word to be transferred on the formatter optional data port bidirectional data bus.
- 8.6.3 A minimum of 150NS. later the user initiates the strobing of the data into one of the internal formatter FIFO memories by activating the DMLDSTB(L).

(The 150NS delay from data enabling to leading edge of data strobe allows for data skew, propagation, and settling time.)

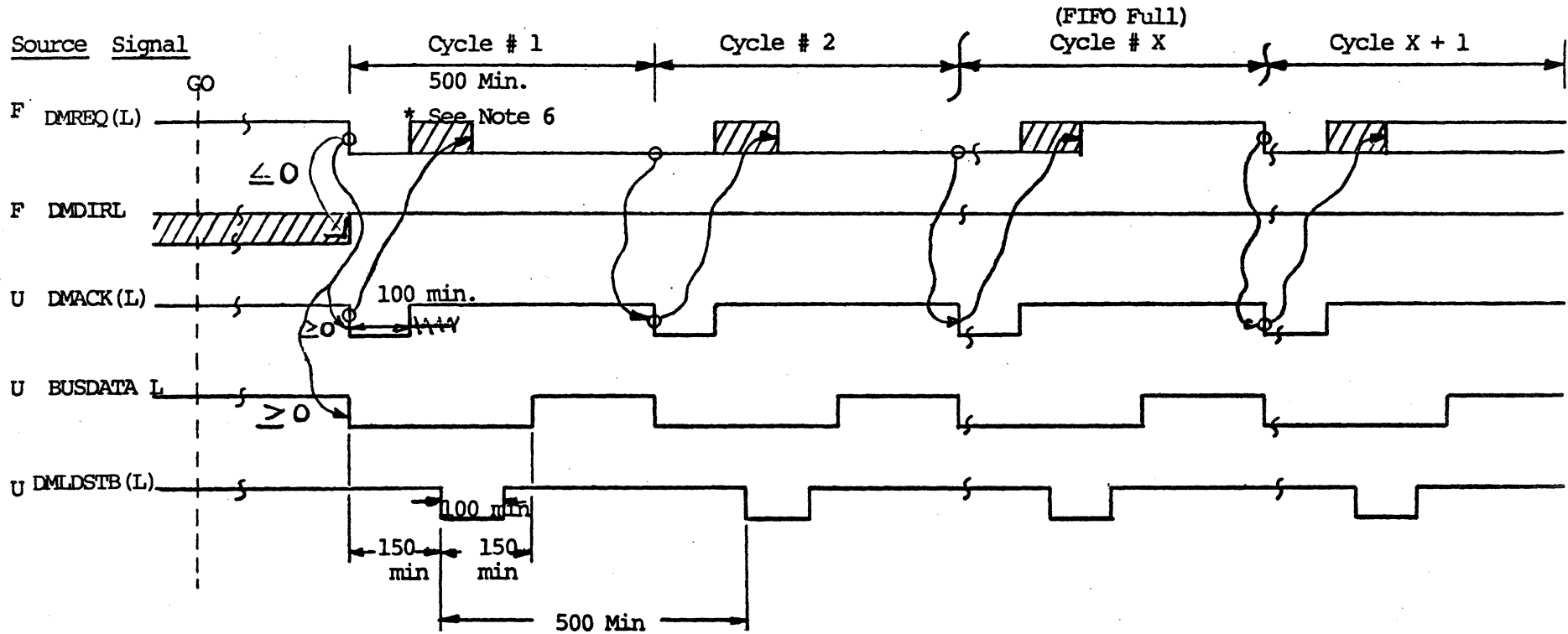
- 8.6.4 The DMACK signal may be issued at any time during the current cycle or at some convenient time previous to the current cycle. (Transfer Look Ahead).
- 8.6.5 The DMLDSTB(L) Data Strobe Signal should be a minimum of 100NS wide.
- 8.6.6 The user must maintain data on the bus 150NS minimum after the leading edge of the DMLDSTB(L) signal.
- 8.6.7 The transfer request signal associated with the FIFO memory loaded by the data transfer will become valid a minimum of 200NS from the leading edge of the DMACK Signal, providing the FIFO memory is not yet full.
- 8.6.8 After the data for a given cycle has been transferred per the above, subsequent data transfers may take place by repeating the sequence as appropriate.

DMLDSTB(L) Strobe Signal frequency must not exceed 2.0MHZ (500NS period).

Note: The user effectively controls the Write DMA data transfer rate and timing by controlling the DMLDSTB(L) and DMACK Signals.

- 8.6.9 The user interface logic should increment the Word Count Register at the beginning of each data transfer cycle so that a logic decision to terminate upon Word Count Register Overflow can be reached before the end of the last cycle.
- 8.6.10 Write DMA data transfers from the user interface to the formatter internal FIFO memories terminate when the Word Count Overflow Signal (WCROVFL) is received from the user interface. DMREQ(L) if active will be returned to the inactive state within 200NS of the leading edge of the SWROVFL Signal.
- 8.6.11 The Word Count Register Overflow Signal generated by the user interface may be either a pulse or a level but must be a minimum of 100NS wide.
- 8.6.12 If the Word Count Overflow Signal is issued prematurely by the user, DMA transfers terminate immediately, but the controller will continue to write alternately the last two words transferred to the FIFO memories onto the selected disk until the formatter internal Word Count Register Overflows and the end of the last addressed sector is reached.

FIGURE 7  
 OPTIONAL DATA PORT  
 PHOENIX 200 FORMATTER  
 WRITE DATA TRANSFER TIMING DIAGRAM (3 FULL CYCLES)



Notes:

1. Timing is at Formatter Interface Connector
2. All Signals are active when low (Negative Logic) at Interface
3. Data On Buss is valid during DMLDSTB(L) Pulse Interval
4. Transfer rate is controlled by user by controlling frequency of DMLDSTB(L) and DMACK
5. All times are in nanoseconds
6. DMREQ(L) is not valid until 200 ns min. after leading edge of DMACK(L)

9.0 Read Data Transfer Timing Diagram

9.1 Read Operation Definition

A "Read" disk formatter operation for purposes of this discussion is defined as being a transfer of 16 bit data words from the selected disk to the Phoenix 200 Formatter and thence to the user interface.

9.2 Interface Timing Reference

All timing information given, unless otherwise specified, is at the Formatter Optional Data Port interface connector.

9.3 Read Operation Initiation

A "Read" operation is initiated by activating the formatter "GO" bit after properly initializing the formatter registers with appropriate transfers defining the specific operation to be performed.

9.4 Data Transfer Direction Establishment by DMDIR Signal

When the read operation is specified the formatter immediately establishes the direction of all data transfers required by forcing the DMDIR Signal to the active state (low).

This signal will remain at this state for the duration of any read operation.

9.5 Data Transfer from Formatter to User Interface Overview

9.5.1 At the start of a read operation, the formatter internal FIFO memories are empty.

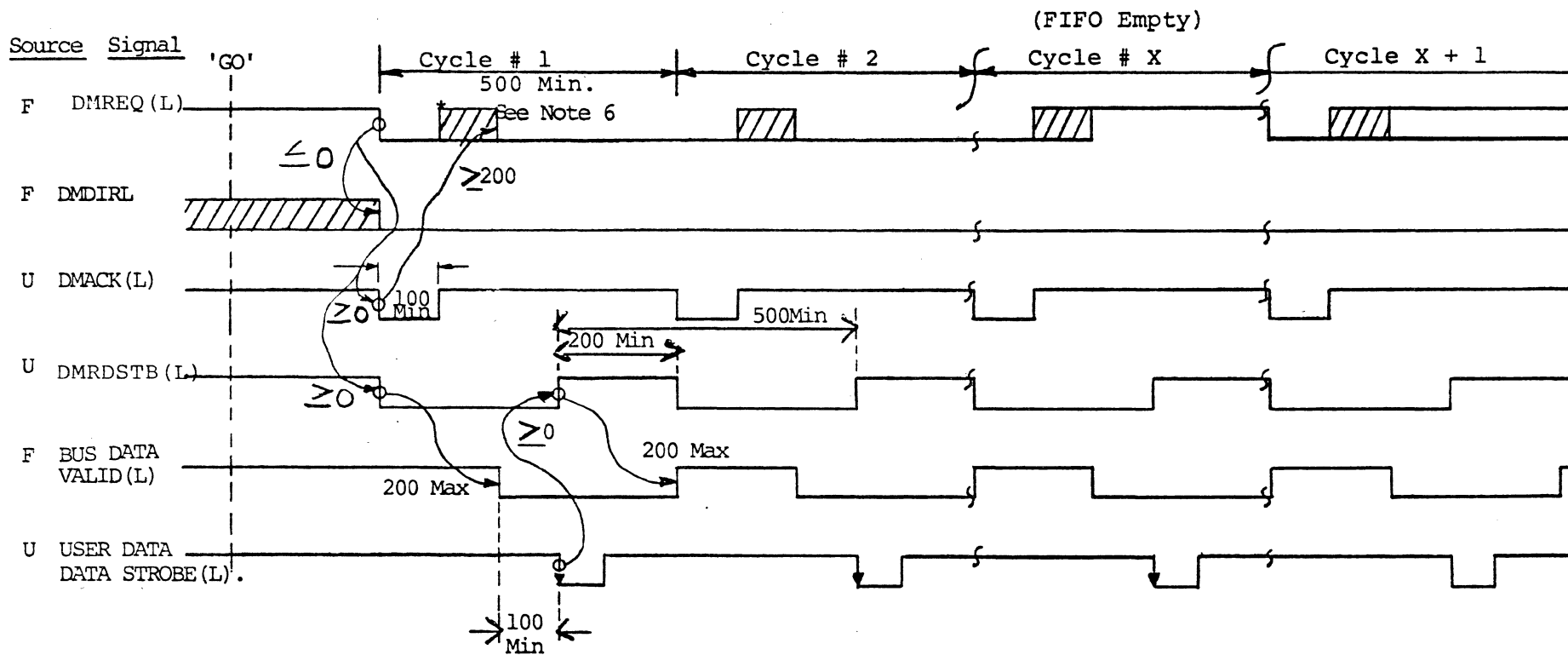
9.5.2 Data transfers from the selected disk to the FIFO memories will begin when the disk is on the correct cylinder and sector.

9.5.3 Words received from the selected disk are alternately temporarily stored in one of the two internal FIFO memories. All odd words are normally stored in FIFO memory #1 while all even words are stored in FIFO memory #2.

9.5.4 Data transfers to the user interface are initiated when data is present in the FIFO memory and will persist until no data is contained in either FIFO memory.

- 9.5.5 Data flow from the selected disk to the FIFO memories terminates when the formatter internal Word Count register overflows.
- 9.5.6 Data flow from the FIFO memories to the user interface terminates when the Word Count Register in the user interface overflows and activates the WCROVFL Signal.
- 9.6 Read Data Transfer Cycle Sequence (Reference Fig. 8)
- 9.6.1 Each read data transfer cycle is initiated by DMREQ(L) being active, indicating that the associated FIFO memory buffer contains data to be transferred to computer memory via the user interface.
- 9.6.2 Upon detection of DMREQ(L) the user, when his interface is ready to accept data, should activate the DMRDSTB(L) Signal.
- 9.6.3 The formatter, upon detection of the DMRDSTB(L) Signal, will put the data to be transferred on the formatter data bus. A maximum of 200 NS from the leading edge of a DMRDSTB(L) pulse, data is guaranteed to be valid at the Formatter interface connector.
- 9.6.4 The user should strobe data from the bus into the user interface 300NS minimum from the leading edge and during the DMRDSTB(L) Signal Interval.
- 9.6.5 The DMRDSTB(L) Signal pulse must be a minimum of 350NW wide.
- 9.6.6 The formatter, upon detection of the trailing edge of the DMRDSTB Signal Pulse, will immediately remove data from the formatter bus. Data, then, is not valid after DMRDSTB(L) is removed.
- 9.6.7 THE DMRDSTB(L) Signal, once removed at the end of a read DMA data transfer, must remain inactive for a minimum of 200 NS before it can be activated again for the next read data transfer cycle.
- 9.6.8 The DMACK Signal may be issued at any time during the current cycle or at some convenient time previous to the current cycle. (Transfer Cycle Look Ahead).
- 9.6.9 The data transfer request signal will become valid a minimum of 200 NS from the leading edge of the DMACK Signal providing there is another data word available in FIFO memory.

FIGURE 8  
Phoenix 200 Formatter  
Read Timing Diagram (Two Cycles)  
Optional Data Port Interface



Notes:

1. Timing is at Formatter Interface Connector.
2. All signals are active when low (negative logic) at interface.
3. Data On Buss is valid 200 ns from leading edge of DMRDSTB(L) to end of DMRDSTB(L) Pulse.
4. Transfer rate is controlled by user by controlling frequency of DMRDSTB(L) & DMACK.
5. All times are in nanoseconds.
6. DMREQ(L) is not valid until 200 ns min. after leading edge of DMACK(L).

9.6.10 After the read data for a given cycle has been transferred from the formatter to the user interface per above, subsequent read data transfers may take place as required by repeating the above sequence.

Note: The user effectively controls the read Data Transfer Timing and data transfer rate by the DMRDSTAB(L) and DMACK Signals.

9.6.11 The user interface should increment the Word Count Register at the beginning of each read data transfer cycle so that a logical decision to terminate upon word count overflow can be reached before the end of the last cycle.

9.6.12 Read data transfers from the formatter to the user interface terminate when the Word Count Register overflow signal (WCROVFL) is activated by the user interface.

DMREQ(L) if active will be returned to the inactive state within 200NS of the leading edge of the WCROVFL Signal.

9.6.13 The WCROVFL signal may be either a pulse or a level but must be at least a minimum of 100NS wide.

## 10.0 Data Transfer Considerations

10.1.1 Two First in First Out (FIFO) memories are contained in the Phoenix 200 Formatter. All data to be transferred to or from disk drives connected to the formatter is buffered in one of the two FIFO memories in the formatter.

10.2.1 The two FIFO memories in the formatter are alternately used for temporary data storage on a word basis in order to maximize data transfer throughout rate.

Normally all odd words are buffered in FIFO1 while all even words are buffered in FIFO2.

10.3.1 Maximum theoretical data transfer (16 bit words) rate is 2.0 MHZ which is more than ample for interfacing to current generation computers and associated peripheral equipment.

10.4.1 The actual data transfer rate in a disk subsystem using the Phoenix 200 Formatter is determined by the user.

10.5.1 All formatter interface signals are negative active at the user connector.

10.6.1 Data transfers normally utilize the same 16 bit bidirectional data bus used for direct program control register loading and reading.

Data transfers may be optionally made over a separate 16 bit bidirectional data used exclusively for data.

The optional data port interface is available on all printed circuit versions of the Phoenix 200 Formatter and requires a separate cable and associated connectors.

10.7.1 If the standard data buss is used for DMA data transfers, the user coupler interface must resolve any formatter bus usage arbitration necessary to insure that no attempt is made to use the formatter bus for DMA and direct program control operations during the same physical bus cycle.

10.7.2 The DMACK signal must be issued only once for each data transfer.



RECOMMENDED INTERFACE  
 OPTIONAL DATA PORT  
 Drivers, Receivers, Termination, and Cable

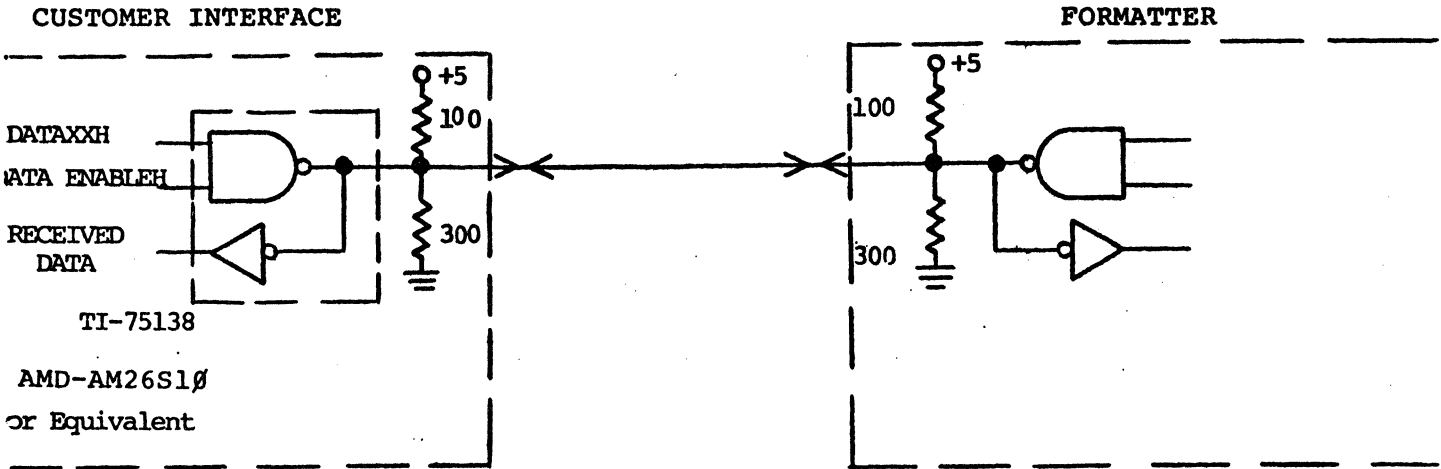
SIGNAL LEVEL DEFINITION:

ALL SIGNALS ARE LOW, ACTIVE TRUE

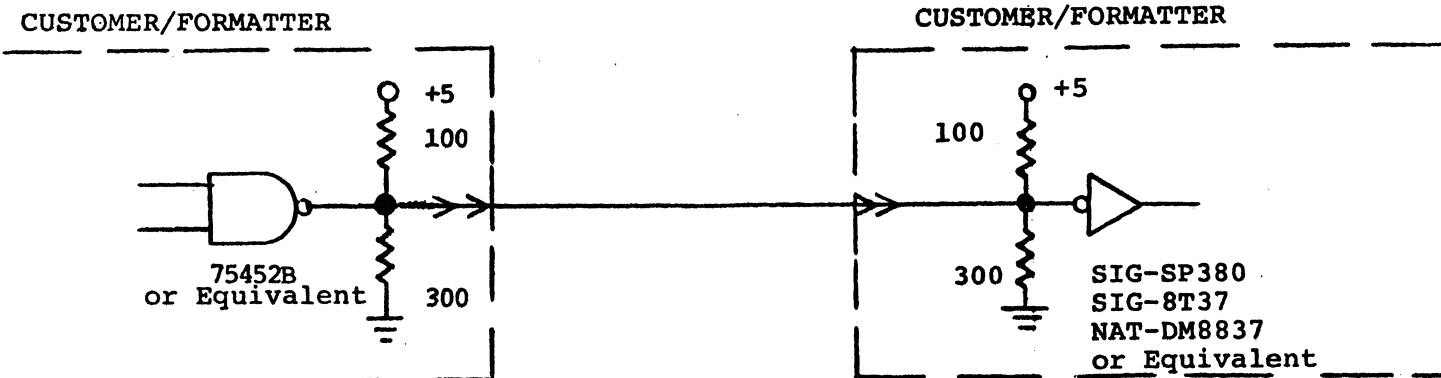
LEVELS: TRUE= LOW= 0.7 VDC @ 100MA

FALSE= HIGH= 3.5VDC

DATA BUS DRIVERS/ RECEIVERS/ TERMINATION (BIDIRECTIONAL)



CONTROL SIGNALS DRIVERS/RECEIVERS/TERMINATION



RECOMMENDED CABLE

3M Part No. 3476/50; Flat Cable with Ground Plane and Drain Wire

PHOENIX 200 FORMATTER

OPTIONAL DATA PORT

USER INTERFACE CONNECTOR SIGNAL/PIN ASSIGNMENT

PIN #	SIGNAL NAME	DIRECTION
1	GND	-
2	GND	-
3	GND	-
4	DBØL	BI
5	DB1L	BI
6	DB2L	BI
7	DB3L	BI
8	DB4L	BI
9	DB5L	BI
10	DB6L	BI
11	DB7L	BI
12	DB8L	BI
13	DB9L	BI
14	DB10L	BI
15	DB11L	BI
16	DB12L	BI
17	DB13L	BI
18	DB14L	BI
19	DB15L	BI
20	-	-
21	-	-
22	-	-
23	-	-
24	WCROVFL	TO FORMATTER
25	-	-
26	DMRDSTB (L)	TO FORMMATER
27	DMLDSTB (L)	TO FORMATTER
28	-	-
29	-	-
30	-	-
31	-	-
32	-	-
33	-	-
34	-	-
35	-	-
36	DMREQ (L)	FROM FORMATTER
37	DMDIRL	FROM FORMATTER
38	-	-
39	-	-
40	-	-
41	-	-
42	DMACK (L)	TO FORMATTER
43	DSKXFRD (L)	FROM FORMATTER
44	-	-
45	-	-
46	-	-
47	-	-
48	GND	-
49	GND	-
50	GND	-

CONNECTOR TYPE USED ON  
BOARD 2 OF FORMATTER:  
3M # 3433 - 1002

NOTE: BI denotes BIDIR-  
ECTIONAL signal



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617-272-8140

Phoenix 211 Disk Controller  
Autoswitch Manual

Dwg. No. 1043-08  
Revision Original  
Date November 1, 1976

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## 1.0 Introduction

This manual is intended to provide the user all of the information necessary to utilize the Autoswitch option to the Phoenix 211 Disk Controller.

## 2.0 Autoswitch Functional Definition/Description

2.1 The Autoswitch Assembly Option is used in conjunction with the Optional Data Port Interface of the Phoenix 211 Disk Controller. (Reference: Phoenix 211 Optional Data Port Manual)

2.2 The Autoswitch option enables the Optional Data Port Interface of the Phoenix 211 Disk Controller to conduct data transfers with either computer memory or user supplied external equipment under direct program control.

2.3 The Autoswitch Option is in effect a programmable digital electronic switch, with two positions; Computer Port Enable and External Port Enable.

2.3.1 Computer Port Mode. When the Autoswitch is in the Computer Port Mode, data transfers can be conducted between the computer memory and the Data Port Interface of the Phoenix 211 Disk Controller.

This permits the user to access data from and store data on any disks connected to the Phoenix 211 Disk Controller.

2.3.2 External Equipment Mode. When the Autoswitch is in the External Equipment Port Mode, data transfers can be set up by the computer program, but all data transfers will take place between the user supplied external equipment and the Data Port Interface of the Phoenix 211 Disk Controller.

This capability maximizes the total system throughput by eliminating the necessity to transfer large amounts of bulk data from user external equipment to computer memory and thence from computer memory to the disk drive(s).

### 2.3.3 Switch Position Control

2.3.3.1 Program Control. The position or mode of the Autoswitch is programmable and may be changed by the execution of one computer instruction. (See Section 4. )

2.3.3.2 Manual Control. A Manual Control Switch is physically provided on each Autoswitch Assembly to permit direct manual control of the Autoswitch position or mode.

### 3.0 General Specifications

#### 3.1 Physical Size = 8½" X 15" Standard

- 1.) 8½ X 15" Standard Hex Printed Circuit Board with Notch cut at connector locations A & B to permit board to be mounted in outside slots (1 & 4) of standard DEC DD11 Systems Unit Assembly.

#### 3.2 Weight: 1.5 Lbs. excluding cables

#### 3.3 Power Requirements: 2.0 amps +5V+10% VDC (Supplied by computer or systems unit backplane)

#### 3.4 Environmental: Temperature and humidity tolerances exceed those required by the host computer system.

### 3.5 Connector Cabling Requirements

3.5.1 External Equipment Port = Connector J2

3.5.2 Computer Data Port = Connector J1

3.5.3 Phoenix 211 Data Port = Connector J3

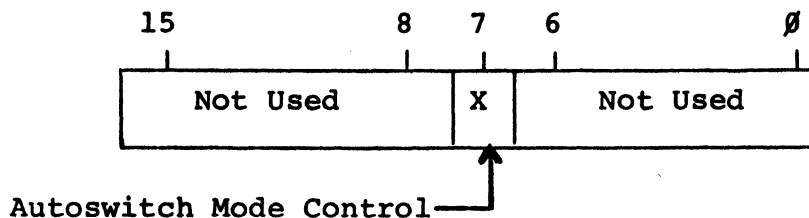
### 4.0 Programming Interface

#### 4.1 General

The programming of the Autoswitch is as simple as possible. One bit is provided, the state of which is controlled directly by the programmer, and which also determines the mode of the Autoswitch.

This bit can be both loaded and read. Further specifics are given in the following subsections.

#### 4.2 Autoswitch Control Register (Typical Address - 164600)



#### 4.2.2. Register Format Explanation

4.2.2.1 The Autoswitch Mode Control (Bit 07) is the only bit used in the word. All other bits when the register is read will be zeros.

4.2.2.2 The state of the Autoswitch Mode Control Bit directly determines the state of the Autoswitch Mode per the following:

<u>Autoswitch Mode Control Bit State</u>	<u>Autoswitch Mode Selected</u>
0	Computer Port
1	External Equipment Port

4.2.3 Initialization Mode. The Autoswitch Mode Control bit is initialized to the reset or Computer Port Mode state at system initialization.

#### 4.3 Timing Considerations - None

The Autoswitch switches mode immediately upon command.

#### 5.0 Autoswitch Register Address Selection (Reference Drawing D1-016-02A, Sheet 2)

5.1 The address of the Autoswitch Mode Control Register is completely manually selectable by staples at component locations D8 and D9 on the Autoswitch printed circuit board assembly.

5.2 These staples are labeled A0-A12 and shown on Sheet 2 of logic drawing D1016-02A.

5.3 The nominal staple settings shown represent a base address of 164600.

5.4 Table 1 shows the staples used to control the Autoswitch Register address and the corresponding assigned address bits.

5.5 Appendix A shows the block of addresses to be used for multiple Autoswitch Assignments.



TABLE 1

Phoenix 211 Autoswitch

Mode Control Register Address Selection

(Reference D1016-02A Sheet 2)

<u>Address Bit</u>	<u>Controlling Staple Designation</u>
A12	A12
A11	A11
A10	A10
A09	A09
A09	A09
A08	A07
A06	A06
A05	A05
A04	A04
A03	A03
A02	A02
A01	A01

NOTE:

- 1.) Staple Removed = logic 1
- 2.) Staple Inserted = logic 0

## 6.0 Manual Mode Control of Autoswitch Mode

- 6.1 A manually controlled switch is provided at the top left hand side of the Autoswitch printed circuit board assembly.

This switch is provided to facilitate debugging and maintenance of the Autoswitch by enabling an operator to manually force the Autoswitch into the External Equipment Port Mode.

## 6.2 External Equipment Switch Position

When the mode control switch is in the External Equipment position, data will be transferred between external equipment supplied by the user and the Optional Data Port Interface on Board 2 of the Phoenix 200 Formatter irrespective of program commands.

This is accomplished by unconditionally forcing control element C11 shown on Sheet 2 of D1016-01B to the set or External Equipment state.

## 6.3 Computer Port Switch Position

When the mode control switch is in the Computer Port Position, data will normally be transferred between the computer memory and the Optional Data Port Interface on Board 2 of the Phoenix 200 Formatter, unless the Autoswitch is specifically commanded to the External Equipment via a user program.

In effect the Computer Port Switch position is the "normal" switch position and enables the Autoswitch mode to be controlled via user program commands.

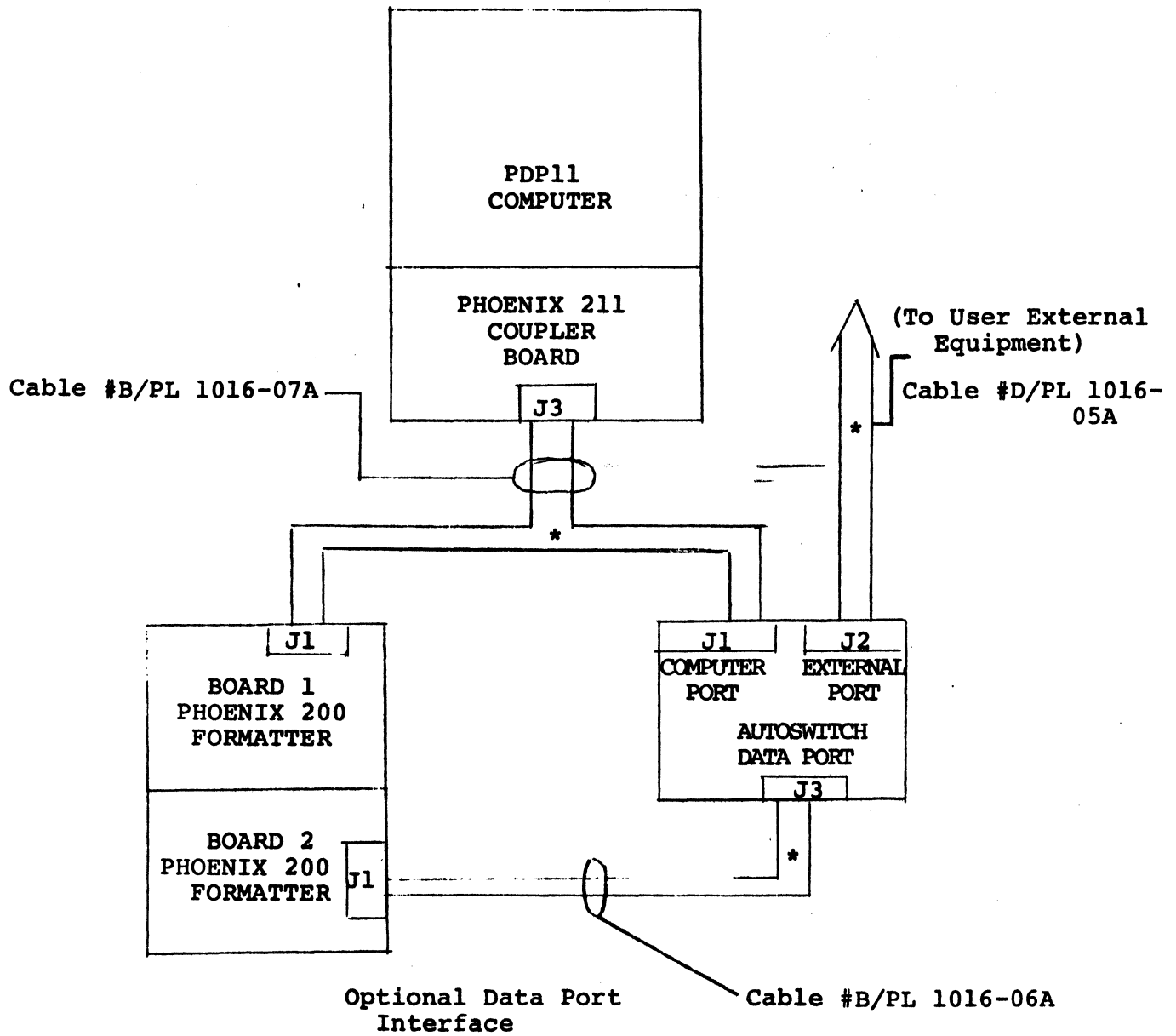
### NOTE:

If the Autoswitch Mode Control Switch is put into the "External Equipment Port" position and is then returned to the "Computer Port" position, the Autoswitch will remain in the External Equipment Port Position until a initialization Signal is issued by the host computer or the Autoswitch is specifically commanded to the "Computer Port" position via a user program.

## 7.0 Phoenix 211 Autoswitch System Configuration and Installation (Reference Figure 1)

Figure 1 shows the physical relationship between the Autoswitch and other elements of a Phoenix 211 disk subsystem.

**FIGURE 1**  
**AUTOSWITCH SYSTEM CONFIGURATION**



\* Shielded Ribbon Cable

# Phoenix 211 Autoswitch Manual

## Appendix B

### Computer Port Connector (J1) Signal/Pin Assignment

PIN #	SIGNAL NAME	DIRECTION
J1	GND	-
J2	GND	-
J3	GND	-
J4	DB0L	BI
J5	DB1L	BI
J6	DB2L	BI
J7	DB3L	BI
J8	DB4L	BI
J9	DB5L	BI
J10	DB6L	BI
J11	DB7L	BI
J12	DB8L	BI
J13	DB9L	BI
J14	DB10L	BI
J15	DB11L	BI
J16	DB12L	BI
J17	DB13L	BI
J18	DB14L	BI
J19	DB15L	BI
J20	-	-
J21	-	-
J22	-	-
J23	-	-
J24	WCROVFL	TO FORMATTER
J25	-	-
J26	DMRDSTB (L)	TO FORMATTER
J27	DMLDSTB (L)	TO FORMATTER
J28	-	-
J29	-	-
J30	-	-
J31	-	-
J32	-	-
J33	-	-
J34	-	-
J35	-	-
J36	DMREQ (L)	FROM FORMATTER
J37	DMDIRL	FROM FORMATTER
J38	-	-
J39	-	-
J40	-	-
J41	-	-
J42	DMACK (L)	TO FORMATTER
J43	DSKXFRD (L)	FROM FORMATTER
J44	-	-
J45	-	-
J46	-	-
J47	-	-
J48	GND	-
J49	GND	-
J50	GND	-

NOTE: BI denotes  
BIDIRECTIONAL  
signal

Phoenix 211 Autoswitch Manual

Appendix C

Data Port Connector (J3) Signal/Pin Assignment

PIN #	SIGNAL NAME	DIRECTION
J3-1	GND	-
J3-2	GND	-
J3-3	GND	-
J3-4	DBØL	-
J3-5	DB1L	BI
J3-6	DB2L	BI
J3-7	DB3L	BI
J3-8	DB4L	BI
J3-9	DB5L	BI
J3-10	DB6L	BI
J3-11	DB7L	BI
J3-12	DB8L 1	BI
J3-13	DB9L	BI
J3-14	DB10L	BI
J3-15	DB11L	BI
J3-16	DB12L	BI
J3-17	DB13L	BI
J3-18	DB14L	BI
J3-19	DB15L	BI
J3-20	-	-
J3-21	-	-
J3-22	-	-
J3-23	-	-
J3-24	WCROVFL	TO FORMATTER
J3-25	-	-
J3-26	DMRDSTB (L)	TO FORMATTER
J3-27	DMLDSTB (L)	TO FORMATTER
J3-28	-	-
J3-29	-	-
J3-30	-	-
J3-31	-	-
J3-32	-	-
J3-33	-	-
J3-34	-	-
J3-35	-	-
J3-36	DMREQ (L)	FROM FORMATTER
J3-37	DMDIRL	FROM FORMATTER
J3-38	-	-
J3-39	-	-
J3-40	-	-
J3-41	-	-
J3-42	DMACK (L)	TO FORMATTER
J3-43	DSKXFRD (L)	FROM FORMATTER
J3-44	-	-
J3-45	-	-
J3-46	-	-
J3-47	-	-
J3-48	GND	-
J3-49	GND	-
J3-50	GND	-

NOTE: BI denotes BIDI-  
RECTIONAL signal

Phoenix 211 Autoswitch Manual

Appendix D

External Equipment Connector (J2) Signal/Pin Assignment

PIN #	SIGNAL NAME	DIRECTION
J2-1	GND	-
J2-2	GND	-
J2-3	GND	-
J2-4	DBØL	BI
J2-5	DB1L	BI
J2-6	DB2L	BI
J2-7	DB3L	BI
J2-8	DB4L	BI
J2-9	DB5L	BI
J2-10	DB6L	BI
J2-11	DB7L	BI
J2-12	DB8L	BI
J2-13	DB9L	BI
J2-14	DB10L	BI
J2-15	DB11L	BI
J2-16	DB12L	BI
J2-17	DB13L	BI
J2-18	DB14L	BI
J2-19	DB15L	BI
J2-20	-	-
J2-21	-	-
J2-22	-	-
J2-23	-	-
J2-24	WCROVFL	TO FORMATTER
J2-25	-	-
J2-26	DMRDSTB (L)	TO FORMATTER
J2-27	DMLDSTB (L)	TO FORMATTER
J2-28	-	-
J2-29	-	-
J2-30	-	-
J2-31	-	-
J2-32	-	-
J2-33	-	-
J2-34	-	-
J2-35	-	-
J2-36	DMREQ (L)	FROM FORMATTER
J2-37	DMDIRL	FROM FORMATTER
J2-38	-	-
J2-39	-	-
J2-40	-	-
J2-41	-	-
J2-42	DMACK (L)	TO FORMATTER
J2-43	DSKXFRD (L)	FROM FORMATTER
J2-44	-	-
J2-45	-	-
J2-46	-	-
J2-47	-	-
J2-48	GND	-
J2-49	GND	-
J2-50	GND	-

NOTE:

- 1.) CONNECTOR USED ON AUTOSWITCH IS BERG 65268-011.
- 2.) REQUIRED USER MATCHING CONNECTOR IS 3M3433-1002 OR EQUIVALENT.
- 3.) BI denotes BIDI-RECTIONAL signal

Appendix E

External Equipment Port Required User Specifications

RECOMMENDED INTERFACE

OPTIONAL DATA PORT  
Drivers, Receivers, Termination, and Cable

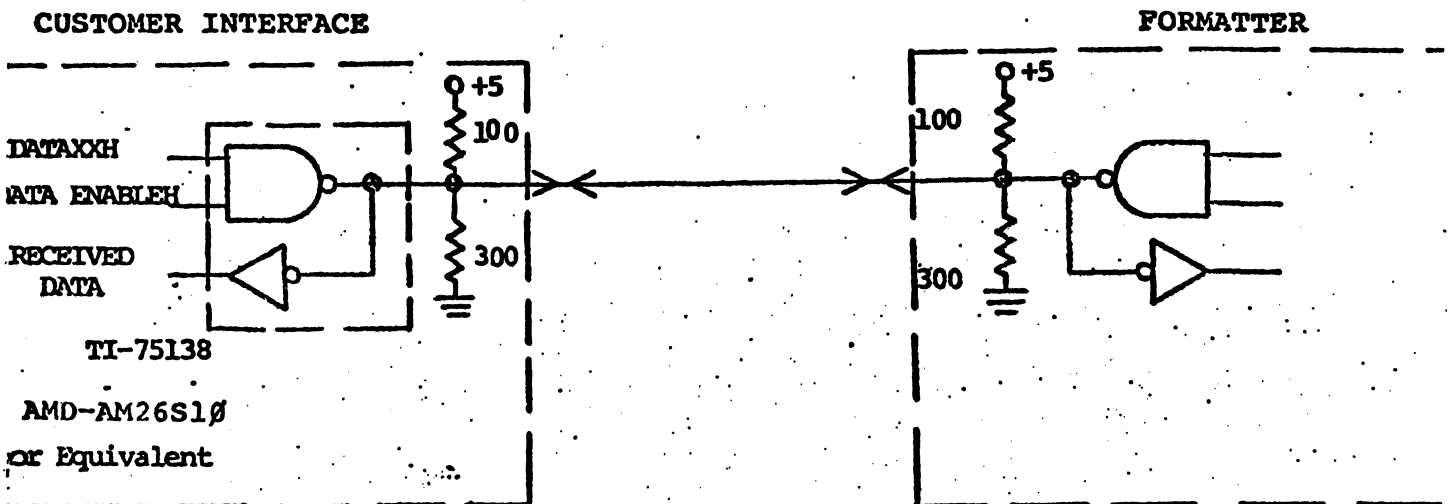
SIGNAL LEVEL DEFINITION:

ALL SIGNALS ARE LOW, ACTIVE TRUE

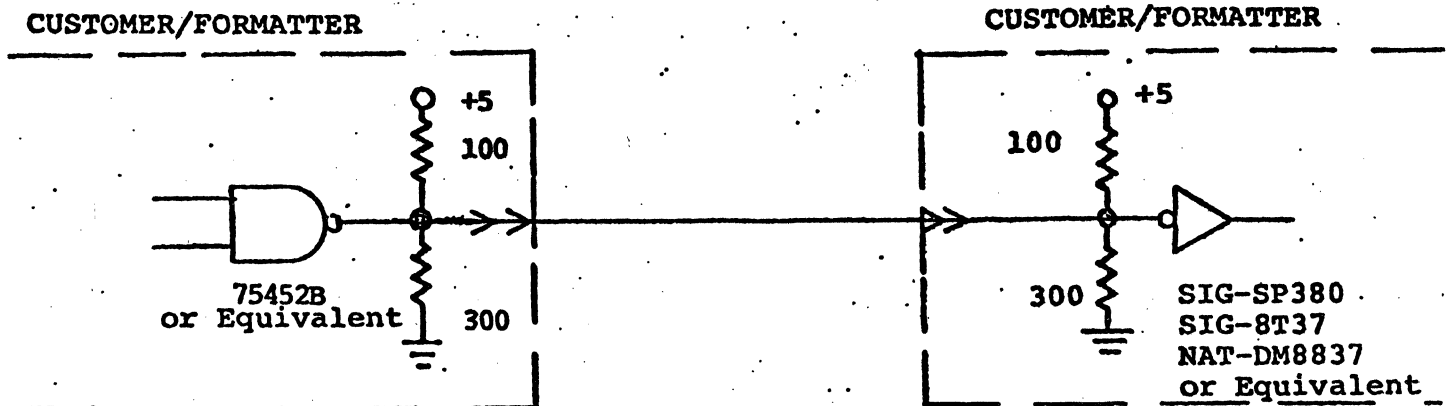
LEVELS: TRUE= LOW= 0.7 VDC @ 100MA

FALSE= HIGH= 3.5VDC

DATA BUS DRIVERS/ RECEIVERS/ TERMINATION (BIDIRECTIONAL)



CONTROL SIGNALS DRIVERS/RECEIVERS/TERMINATION



RECOMMENDED CABLE

3M Part No. 3476/50; Flat Cable with Ground Plane and Drain Wire

## 7.1 Autoswitch Board Installation

The Autoswitch Board is physically a standard "hex" printed circuit board with a notch in the A & B connector section. The board may be physically plugged into a standard small peripheral controller slot (SPC) in any PDP11 computer or BALLK Expansion Box backplane. Installation of the Autoswitch Board simply consists of physically plugging it in to any available backplane slot after having first determined the mode control register address via staple selection as outlined in Section 5.

## 7.2 Computer Port Cabling (J1)

- 7.2.1 The Computer Port on the Autoswitch is physically provided by connector J1 on the Autoswitch Board. (Connector J1 is the rightmost connector on the top of the board. Reference Assembly Drawing D1016-03)
- 7.2.2 J1, the Computer Port Connector is physically cabled to J3 of the Phoenix 211 Coupler Board and J1 of board 1 of the Phoenix 200 Board 1 as shown on Figure 1., via Cable B/PL 1016-07A.
- 7.2.3 Installation of the Computer Port Cable is accomplished by simply plugging the labelled cable connectors into the matching connector receptables on the Autoswitch Board, 211 Coupler Board and Board 1 of the formatter.

## 7.3 Data Port Cabling (J3)

- 7.3.1 The common Data Port Interface of the Autoswitch is physically provided by connector J3 on the Autoswitch Board. (Connector J3 is the leftmost connector on the top of the board. Reference Assembly Drawing D1016-03)
- 7.3.2 J3, the Data Port Connector is physically cabled to J1 of board 2 of the Phoenix 200 Formatter as shown on Figure 1 via cable
- 7.3.3 Installation of the Data Port Cable is accomplished by simply plugging the labelled cable connectors into the matching connector receptacles located on the Autoswitch and board 2 of the Phoenix 200 Formatter.

## 7.4 External Equipment Port Cabling (J2)

- 7.4.1 The user External Equipment Port of the Autoswitch is physically provided by connector J2 on the Autoswitch Board. (Connector J2 is the center connector on the top of the board. Reference Assembly Drawing D1016-03)



- 7.4.2 J2, the External Equipment Connector is to be physically connected to user supplied external equipment as shown on Figure 1.

NOTE:

- 1.) The user designed external equipment interface logic must conform to the Phoenix 211 Optional Data Port Interface electrical and signal timing specifications as outlined in the Phoenix 211 Optional Data Port Interface Manual.
- 2.) Appendix D defines the required physical connector, cable and signal pin assignments of user equipment to be connected to this interface.

8.0 Autoswitch Testing (Reference Figure 2)

The Autoswitch may be tested completely using the standard supplied Phoenix 211 Disk Diagnostics and two cabling configurations as shown in Figure 2.

8.1 Test Position 1 - Computer Port Data Path Test

- 8.1.1 In the Computer Port Data Path Test, the Coupler cable is connected to the Autoswitch Computer Port Connector and the Autoswitch is electrically switched to the Computer Port position.

NOTE:

This is the default mode of the Autoswitch.

- 8.1.2 All data transferred between the disk and the computer is thus constrained to flow through the Computer Port of the Autoswitch and the Optional Data Port Interface of the Phoenix 200 Formatter.
- 8.1.3 The integrity of the Autoswitch Computer Port Data Path is verified by running Diagnostic Tests 0 - 25 as a single group.

8.2 Test Position 2 - External Port Data Path Test

- 8.2.1 In the External Data Path Test the coupler cable is connected to the Autoswitch External Port Connector and the Autoswitch is electrically switched to the External Port position under direct program control.

NOTE:

- 1.) The Autoswitch may be forced to the External Equipment Mode by putting the Manual Mode Control Switch located on the top of the Autoswitch Board to the External Equipment Position.

2.) The Autoswitch may be switched to the External Equipment Mode under control of the supplied Phoenix 211 Diagnostic Program by depositing 1 in location AUTOSW of the program.

8.2.2 All data transferred between the disk and the computer is thus constrained to flow through the External Port of the Autoswitch and the Optional Data Port Interface of the Phoenix 200 Formatter.

8.2.3 The integrity of the Autoswitch External Port Data Path is verified by running Diagnostic Tests 0 - 25 as a single group.

8.2.4 The Autoswitch External Port position is selected by depositing a "1" into the "Autoswitch" control memory location of the diagnostic program prior to initiating the test.

Phoenix 211 Autoswitch Manual

Appendix A

Autoswitch Unibus Address Assignments

<u>Autoswitch Unit No.</u>	<u>Assigned Base Address</u>
1	164600
2	164602
3	164604
4	164606
5	164610
6	164612
7	164614
8	164616
9	164620
10	164622
11	164624
12	164626
13	164630
14	164632
15	164634
16	164636
17	164640
18	164642
20	164646
21	164650
22	164652
23	164654
24	164656

XYLOGIC OEM COMPONENTS GROUP, INC.  
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PHOENIX 211 DISK CONTROLLER

MULTIPLE COMPUTER PORT OPTION SPECIFICATION

Revision B

October 15, 1977



Phoenix 211 Disk Controller  
Multiple Computer Port Option

1. Purpose

The multiple computer port option enables up to four PDP11 Computers to retrieve data from and store data on common storage module type disk drives connected to one Phoenix 200 Disk Formatter. Access to the common formatter is provided on a selectable equal priority or controlled priority basis.

2. Overview - (Reference Figure 1)

Each PDP11 Computer in a multiple computer disk subsystem contains a Phoenix 211 Coupler Board which physically interfaces the computer to the common formatter bus.

The common formatter bus is "daisy-chained" from the formatter to each of the 211 couplers associated with each computer to be included in the disk system. The formatter interface is terminated at the last 211 coupler board.

Arbitration logic is contained within the formatter to insure that the common formatter resource is allocated to the connected computers on a request basis with failsafe timeout provisions.

3.0 Operation

3.1 General

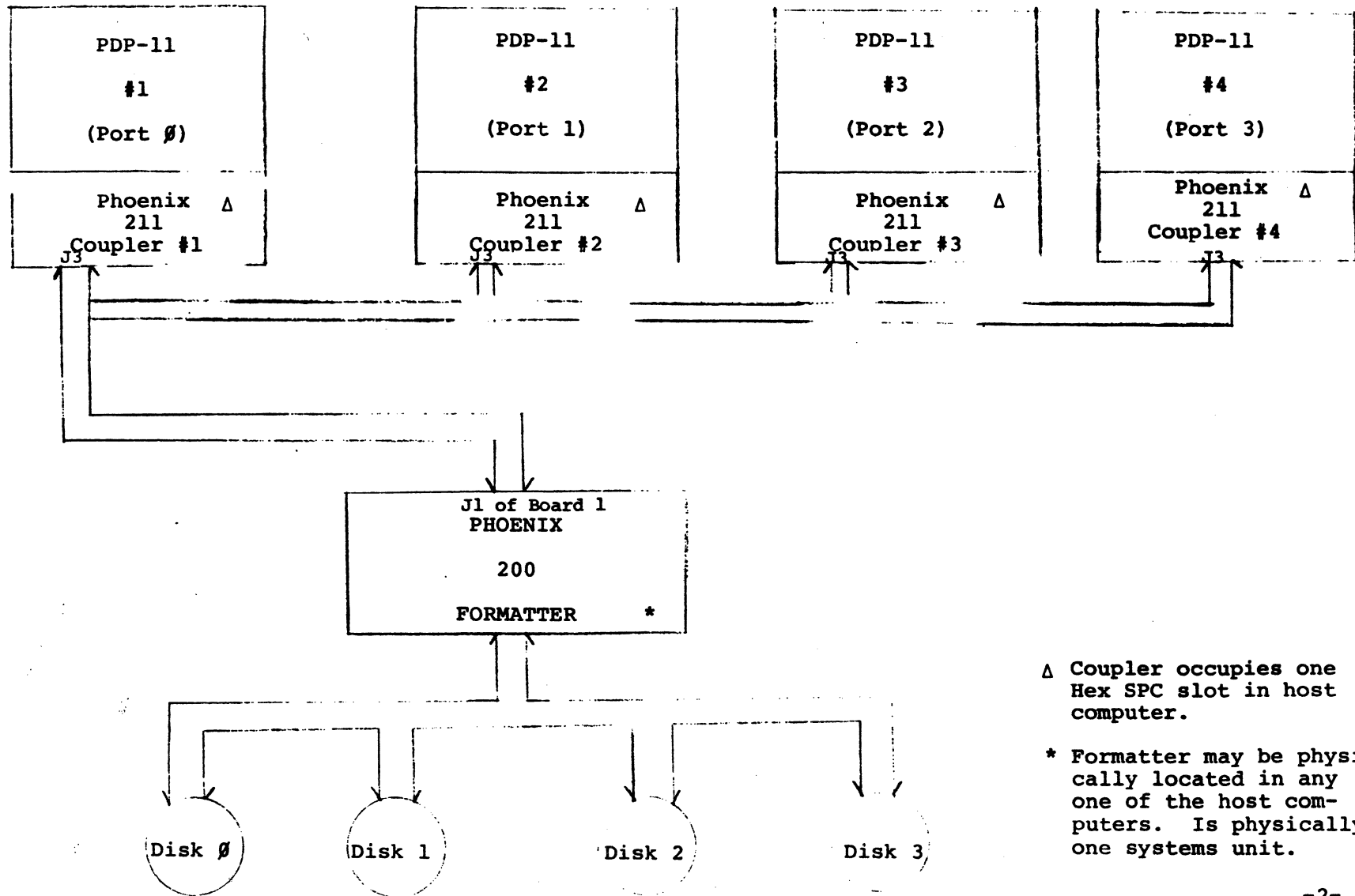
The common formatter is "shared" between all computers in the system on a mutual exclusive basis. Requests are made to the computer port arbitrator by each of the computers whenever disk operations are to be performed.

The arbitrator fields all requests for the use of the formatter and assigns the formatter to the requesting computer ports on a equal or selectable controlled priority basis.

Once the formatter has been assigned to a given port, the associated computer may use the formatter to conduct as many disk operations as desired. When the formatter is so assigned to one computer port in the system all

Figure 1

XYLOGIC PHOENIX MULTIPLE PDP-11 COMPUTER DISK SYSTEM CONFIGURATION



other computer ports are prohibited from using the formatter.

The formatter is normally released for use by other ports when the current assigned computer port removes its "request" signal at the conclusion of its disk operations.

However, the arbitrator also monitors actual formatter usage and will automatically reassign the formatter to another port if no activity is detected on the currently assigned port within a selectable, predefined time interval.

When the formatter is assigned to a requesting computer port by the arbitrator an interrupt is automatically generated to the associated computer by the 211 coupler board to facilitate system software.

### 3.2 Detailed Operation

#### 3.2.1 Formatter Request Bit (Bit 5 of the 211 DCSR)

Requests for use of the formatter by any computer port are initiated by setting the "Formatter Request" Bit.

This Bit sets an internal control memory element which sends a unique request signal to the arbitrator.

No further action can be taken by the programmer until the arbitrator assigns the formatter to his port, at which time the controller becomes ready and will generate an interrupt, if enabled.

The Formatter Request bit must be set and the port be assigned as per above before any disk operations can be initiated.

#### 3.2.2 Computer Port Assignment

1. The arbitrator utilizes a four state scanner and associated control logic to allocate the common formatter to the maximum of four computer ports.
2. When the formatter is unassigned, the arbitrator sequentially scans the request signals from the computer ports. When a request signal is detected the scanner is stopped and the binary state is issued to all computer ports over two signal interfaces.
3. Each computer port is assigned a strappable port number. (0-3). See Appendix A for staple selection.

When the assigned port number is issued by the arbitrator, all requesting ports automatically compare this value with the associated preassigned physical port number.



The requesting port associated with the matching preassigned port number then becomes ready, generates an interrupt to the host computer, and is free to initiate any and all appropriate disk transfers via the formatter.

### 3.2.3 Formatter Release

When all desired disk operations have been completed by the current assigned computer port, the formatter is released for use by other computer ports by resetting the Formatter request bit.

This removes the associated port request signal to the formatter arbitrator, and causes the arbitrator to reassign the formatter to some other requesting computer port.

### 3.2.4 Formatter Reassignment Priority Options

Computer Port Formatter Requests may be serviced on a selectable equal priority or a controlled priority basis.

If the equal priority option is chosen, the arbitrator scanner will always sequentially scan all of the computer ports for formatter requests. Hence, all computer ports have an equal opportunity to obtain formatter access.

If the controlled priority option is selected, the arbitrator scanner will always be reset to state  $\emptyset$  when released, and then sequentially scan the associated ports for new requests.

Hence, this option assigns the highest priority to port  $\emptyset$  and the least priority to port 3.

### 3.2.5 Automatic Timeout Port Reassignment

The arbitrator contains a automatic timeout feature which will automatically reassign the formatter to another requesting port if no activity is detected on the currently assigned port within a selectable, predefined interval.

#### 4.0 Physical Configuration

##### 4.1 Phoenix 211 PDP11 Coupler

One Phoenix 211 PDP11 Coupler Board is required for each PDP11 Computer that is to utilize the Phoenix 200 Formatter.

##### 4.2 Phoenix 200 Formatter

The common Phoenix 200 Formatter is packaged in one PDP11 systems unit and may reside in any one of the system PDP11 computers.

The formatter physically interfaces to the system disk drives.

##### 4.3 Coupler Cabling

A shielded ribbon cable is required between the formatter and each cpu coupler card.

## APPENDIX A

### MULTIPLE CPU STAPLE SELECTION

1) To enable the Multi-CPU option

- A) Install W36 on Phoenix 200 Board 1
- B) Remove W22 on Phoenix 211 coupler card

2) 211 Coupler Port Selection

Port	W54	W55	W56	W57	W36	W37	W38	W39
∅	IN	OUT	OUT	OUT	IN	OUT	OUT	OUT
1	OUT	IN	OUT	OUT	OUT	IN	OUT	OUT
2	OUT	OUT	IN	OUT	OUT	OUT	IN	OUT
3	OUT	OUT	OUT	IN	OUT	OUT	OUT	IN

NOTE: On a given system each coupler must be assigned a different port number.

3) To enable the controlled priority option install W41 on Phoenix 200 Board 1.

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PHOENIX 211 ECC SPECIFICATION

Rev. c

November 30, 1977

## 1. Introduction

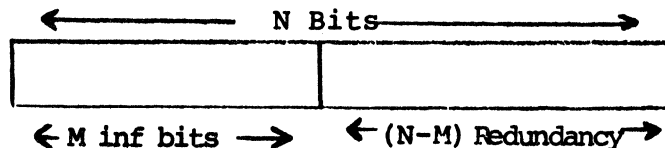
Storage Module media is not as perfect as Disk Drive Vendors would like it to be. The bit recording density of about 6000 bpi is state of the art and requires a head flying height and coating thickness of about 20 micro-inches. (The figure for 2314 type packs is 60 micro-inches.)

Practical testing has revealed that 100% of all unrecoverable errors are one, two or three bit bursts. Disk Drive Vendors specify that a track shall not have more than one burst error and it, in turn, shall be no longer than 11 bits long. Cylinder 0 (heads 0 and 1) shall have no errors. Also, there shall be no more than 30 correctable error tracks per 80 MB pack.

Based on the above, a Storage Module Disk System has the ability to either bypass bad tracks or to perform error correction on them. One solution to the potential problem is an error correction scheme.

## 2. Principles of Error Detection

A checkword is appended to the message (data field) when the information is written on the disk. The checkword is obtained as the remainder when the message is divided by a carefully chosen number known as the generator polynomial.



The above figure shows a message of M information bits having added to it (N-M) redundancy bits. The redundancy bits are achieved as follows:

Let  $M(X)$  equal the message polynomial.  
Let  $P(X)$  equal the generator polynomial.

Hence,  $M(X) = Q(X) + R(X)$  where  $Q(X)$  and  $R(X)$  are respectively the quotient and remainder following division. The quotient has no real significance and is discarded but  $R(X)$  becomes the (N-M) redundancy bits shown above. Hence, the total message (information plus redundancy) can be expressed as:

$$\begin{aligned} N(X) &= X^{(N-M)} M(X) + R(X) \\ &= Q(X) P(X) \end{aligned}$$

If the received message can be divided by the polynomial  $P(X)$  without a remainder, then it has been received correctly and further action is not needed.

### 3. Choice of Polynomial

The strength or weakness of a redundancy scheme is intimately tied to the choice of polynomial and this depends on the type of errors to be expected. Data transmission suffers from long burst errors. High-speed solid-state memories suffer from isolated single-bit errors. Rotating magnetic memories compromise between these two extremes and suffer from short bursts (1-3 bits). The polynomial chosen was a Fire Code and thus is of the following form:

$$P(X) = P_1(X) (X^C + 1)$$

Where  $P(X)$  is the generator polynomial for a Fire Code; this must have two properties. (1)  $P_1(X)$  is a primitive (irreducible) polynomial of degree  $M$  and order  $E$ . (Note, the degree of a polynomial is defined to be the greatest power of  $X$  in which the coefficient is non-zero and  $E$  is defined to be  $(2^M - 1)$ ). (2) The parameter  $C$  must not be divisible by  $E$ .

The above Fire code polynomial will have the following properties: (1) The length of the code,  $N$ , is equal to the least common multiple of  $E$  and  $C$ . This works out to be  $(2^M - 1)C$ . (2) The number of redundancy bits is equal to  $(M + C)$ . (3) The number of information bits,  $M$ , is equal to  $(2^M - 1)C - (M + C)$ .

The polynomial chosen for the Phoenix 211 Disk Controller is as follows:

$$P(X) = (X^{11} + X^2 + 1) (X^{21} + 1)$$

The degree of the  $P_1(X)$  portion is 11 and  $E$  is therefore equal to  $(2^{11} - 1)$  or 2047. The length of the code is equal to  $(E - C)$  where  $C$  equals 21. Hence, code length equals  $(2047 - 21)$  bits. The number of redundancy bits is equal to  $(M + C)$  or  $(11 + 21)$ .

In summary, the above polynomial will support a record length up to 2680 words and each record will be followed by a 32 bit checkword.

### 4. Error Detection and Correction Performance

$$\begin{aligned} \text{The polynomial chosen was } P(X) &= (X^{11} + X^2 + 1) (X^{21} + 1) \\ &= X^{32} + X^{23} + X^{21} + X^{11} + X^2 + 1 \end{aligned}$$

This will detect two error burst of combined length 22, one error burst of length 32 and any odd number of errors. This will correct any single burst up to 11 bits long.

## 5. Programming Details

The Phoenix 211 has an ECC (error correction code) capability which will detect and correct an error by reconstructing a portion of the data within the specified code word length, which is fixed. The burst ECC code will correct an error which must fall within the specified length of the burst. The actual location of the burst within the code word (data field of a sector) is irrelevant.

Any errors outside the specified burst length will be detected but not corrected. The ECC hardware, in this case, will yield an ECC uncorrectable error. The Phoenix 211 logic contains the hardware to find the burst within which the read error is included and determine the exact location of the burst within the data field.

The ECC pattern register contains the actual error burst and the ECC position register contains the address for determining the actual location of the error burst within the data field.

**NOTE:** The actual correction of the data field is done by the software with the help of the ECC position and ECC position and ECC pattern registers.

## 6. ECC Register Formats

### (A) ECC Bit Position Register (764016)

UCERR	0	0	BPR 4096	BPR 2048	BPR 1024	BPR 512	BPR 256	BPR 128	BPR 64	BPR 32	BPR 16	BPR 8	BPR 4	BPR 2	BPR 1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

<u>Bit</u>	<u>Name</u>	<u>Function</u>
0-12	Bit Position Address (Read Only)	Contains the exact location of the error burst within the data field following the completion of the error correction procedure. Upon completion of the ECC process the formatter will load this register with the physical location of the <u>firstbit</u> of the 11-bit error burst. The position register will only be loaded if the ECC logic is enabled by having the ECC Inhibit Bit reset.

<u>Bit</u>	<u>Name</u>	<u>Function</u>
13-14	Not Used (Read Only)	Always zeros
15	Uncorrectable ECC Error (Read Only)	Set when the conclusion of the error correction procedure indicates that the error was an uncorrectable ECC error. Cleared by UNIBUS INIT, Formatter Clear, or a "GO" Bit.

(B) ECC Pattern Register (764020)

ECC INHIB	Ø	Ø	Ø	Ø	ECC PAT	ECC PAT	ECC PAT	ECC PAT	ECC PAT	ECC PAT	ECC PAT	ECC PAT	ECC PAT	ECC PAT	ECC PAT
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø

<u>Bit</u>	<u>Name</u>	<u>Function</u>
0-10	ECC Pattern (Read Only)	Contains the actual error burst available at the completion of the ECC internal to the formatter logic error correction process. These bits will be exclusive OR'd with the eleven bits in error by software. The software will use the contents of the ECC Position Register to find the actual location of the error burst in the data field, then the error burst itself will determine the bits in error within the 11-bit field.
11-14	Not Used (Read Only)	Always Zeros
15	ECC Inhibit (Read/Write)	Set when the software desires to inhibit error correction. If ECC Inhibit is set, error correction code is disallowed; if ECC Inhibit is reset, the error correction process is allowed. Cleared by Unibus INIT, formatter clear, or by writing a zero.

If a data error is detected at the end of the data transmission in the read mode with the ECC Inhibit Bit reset, the formatter will immediately go into the ECC correction process. Prior to beginning the correction process, the formatter will also set the CRC Error



Function(Cont'd.)

Bit (Bit 8 of the Error Status Register), which will remain set until a UNIBUS Init, formatter Clear, or a "GO" Bit is received.

APPENDIX A

ECC DUAL HEADER FOR CDC SMD'S 9760, 9762, 9764, 9766

Preamble #1 240 Bits	HDR SYNC 2 Bits	HDR 1 32 Bits	HDR 1 CRC 32 Bits	GAP 16 Zeros	HDR 2 32 Bits	HDR 2 CRC 32 Bits	Preamble #2 96 Bits	Data Sync 2Bits	DATA 4096 Bits	DATA ECC (CRC) 32 Bits	POSTAMBLE 428 Bits
-------------------------	--------------------	------------------	----------------------	--------------	------------------	----------------------	------------------------	--------------------	-------------------	---------------------------	-----------------------

APPENDIX B

ECC Board I Switch Settings (300-031-90X)

Normal Operation

K7-1 ON  
K7-8 ON  
K7-2 ON  
K7-3 ON  
K7-7 ON

E5-3 ON  
E5-7 ON  
E5-4 ON  
E5-5 ON

All other switches OFF

---

For Normal Operation with ECC with 256 Words/Sector

K7-1 ON  
K7-8 ON  
K7-2 ON  
K7-3 ON  
K7-7 ON

E5-3 ON  
E5-4 ON  
E5-5 ON  
E5-8 ON  
E5-6 ON

C2-1 ON  
C2-7 ON

D6-2 ON  
D6-5 ON  
D6-7 ON  
D6-8 ON

D7-1 ON  
D7-3 ON  
D7-4 ON  
D7-5 ON  
D7-8 ON

All other switches OFF

---

XYLOGIC OEM COMPONENTS GROUP, INC.

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ROM Bootstrap Board

&

Phoenix 211 Disk Controller Bootstrap Program

1. General Description

The Xylogic ROM Bootstrap Board is a quad sized printed circuit board which may be plugged into any standard small peripheral controller (SPC) I/O slots in any standard PDP11 Unibus backplane.

The ROM Bootstrap Board contains sockets to accommodate up to a maximum of 512 words of PROM program storage.

2. Phoenix 211 Disk Controller Bootstrap Program

- 2.1 The Bootstrap Program for the Phoenix 211 Disk Controller is contained in two 32 x 8 Proms on the bootstrap printed circuit board.
- 2.2 The Phoenix 211 Disk Controller Program starting address is 173700.
- 2.3 The boot program utilizes disk drive unit 0 of a Phoenix 211 Disk Drive Subsystem.
- 2.4 The program reads data absolute from sectors 0 and 1 (sector 0, head 0, cylinder 0) of unit 0 and transfers data obtained to computer memory starting at absolute memory location zero.
- 2.5 When the boot operation is successfully completed program control is transferred to absolute memory location 0.
- 2.6 If an error is detected, the operation will be repeated.

3. Phoenix 211 Disk Controller Bootstrap Program Installation Procedure

- 3.1 Plug the XYLOGIC ROM Bootstrap Board Assembly into any available standard small peripheral controller I/O slot in the PDP11 computer or Expansion Box.

Caution: Insure that all system power is off before plugging or removing any boards in system.

- 3.2 Turn power on system.
- 3.3 Verify proper operation of Bootstrap Board by checking proper ROM content via computer console.
  - 3.3.1 Set 173700 in Console Switch Register
  - 3.3.2 Momentarily Depress the Console "Load Address" Register Switch
  - 3.3.3 Momentarily depress the "Examine" Console Switch
  - 3.3.4 Observe that the contents of the Phoenix 211 ROM Bootstrap Program memory location is the same as that specified on the Phoenix 211 Bootstrap Program Listing.
  - 3.3.5 Repeat steps 3.3.3 and 3.3.4 until all of bootstrap memory locations have been verified for proper content.

#### 4. Phoenix 211 Disk Controller Bootstrap Program Operating Procedures

- 4.1 Insure that disk drive unit 0 contains proper operating system disk pack, has power applied, and is enabled for use.
- 4.2 Set 173700 in Console Switch Register
- 4.3 Put Console "Enable/Halt" Switch in "Enable" position
- 4.4 Momentarily depress the console "Load Address" Switch
- 4.5 Momentarily depress the console "Start" Switch
- 4.6 Absolute Sectors 0 and 1 of disk drive 0 will then be read, transferred to memory, and control transferred to absolute memory location zero.



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Phoenix 211 Disk Controller

Maintenance Manual

Dwg. No. 900-006-301

Revision A

Date March 10, 1977



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## Phoenix 211 Disk Controller

### 1.0 MAINTENANCE PHILOSOPHY

The maintenance philosophy for the Phoenix 211 Disk Controller that appears to make the most sense for Xylogics and the majority of its customers is:

1. Troubleshoot to the printed circuit board level
2. Swap out any defective boards
3. Have any defective boards repaired at the factory for a nominal charge.

Execution of such a maintenance philosophy should result in minimizing customer down time and facilitate third party or customer service of equipment in the field. Accordingly all Xylogic documentation is geared towards isolation of any problems to the board level.

## 2.0 PHOENIX 211 DISK SUBSYSTEM USER MAINTENANCE ALTERNATIVES

### 2.1.0 GENERAL

A Phoenix 211 Disk Subsystem consists of the Phoenix 211 Disk Controller and at least one disk drive. The disk controller is solid state and requires no preventitive maintenance, while the disk drive requires regularly scheduled preventitive maintenance in order to keep it operating.

Three options are open to the user with respect to maintenance of a Phoenix 211 Disk Subsystem.

- . Contracted Third Party Maintenance (ICE)
- . On Call Maintenance (ICE/XYLOGICS)
- . User Maintenance

### 2.1.1 THIRD PARTY MAINTENANCE

Third Party Maintenance of a Phoenix 211 Disk Subsystem is normally available through Iomec Customer Engineering, Incorporated (ICE). ICE has offices nationwide, and can provide service on a reasonable monthly contract basis for both the Phoenix 211 Disk Controller and associated disk drives. Typically, a maintenance contract with ICE covers scheduled preventitive maintenance calls and parts and labor on repair calls. Third Party Maintenance is strongly recommended for small OEM and end users. Response time for contract maintenance is less than 8 hours.

### 2.1.2 ON CALL MAINTENANCE

On Call Maintenance is sometimes opted in lieu of contracted maintenance. On Call Maintenance can be obtained according to the following groundrules.

#### 1. Response Time:

On Call Maintenance requests for service to ICE will be honored only after all outstanding requests for contracted service have been taken care of. On Call Maintenance requests for service to Xylogics will be honored only in the event that service from ICE is not available in the customer area. Such service will be scheduled at Xylogic's convenience. A user opting for On Call Maintenance must be willing to live with possible response times of 24-96 hours, since he is at the bottom of ICE and Xylogic priority.

#### 2. Charges:

Charges for On Call Maintenance visits are based on a time, materials, and expense basis. Hence, a customer will pay for all material, any and all travel expenses, and direct labor at a predefined rate. A Purchase Order number, to cover all such charges, will be obtained from any user prior to making the service visit.

### 2.3 Considerations:

A user who chooses to utilize On Call Maintenance, rather than Contract Maintenance is effectively betting that the equipment will be reliable to the point that the On Call costs will be less than the Contract Maintenance costs.

Such a user must be willing to live with the slow response time and be willing to take the risk that it may cost him more if a catastrophic disk drive failure occurs.

Thirdly, such a user must also assume the responsibility for seeing that the proper disk drive preventative maintenance procedures are followed or he can be guaranteed of a catastrophic disk drive failure.

#### 2.1.3 USER MAINTENANCE

In User Maintenance the user assumes complete maintenance responsibility for the Phoenix 211 Disk Subsystem. To perform maintenance properly, the user must have both capable trained personnel and proper maintenance equipment.

##### 2.1.3.1 SPARES AND MAINTENANCE EQUIPMENT REQUIREMENTS

A list of the required equipment necessary for the maintenance of both the Phoenix 211 Disk Controller and a Control Data Corp. 9762, 80 Megabyte Disk Drive are listed in Appendix A. Note that the capital outlay for spare parts and maintenance equipment is in excess of \$8000.00.

##### 2.1.3.2 TRAINED PERSONNEL REQUIREMENTS

The most important ingredient in a user maintenance program is the availability of capable personnel who have a systematic approach to problem solving, and who have been properly trained on, and are familiar with both the Phoenix 211 Disk Controller and user associated disk drives.

Training of personnel on the disk controller and associated disk drives requires two weeks, with one week being spent on each. Use of untrained user personnel, no matter how capable, to maintain a Phoenix 211 Disk Subsystem is not recommended. Such individuals will not be able to get the job done properly, even if provided with a 100% complement of spares and maintenance equipment, and are likely to induce failures into a subsystem, by abusing the equipment physically, and/or electrically. An untrained field service engineer is worse than no field service engineer. We are all too familiar with the true war stories of personnel who are "experts" at taking apart equipment, but who, under no circumstances can put it back together again and make it work.

### 2.1.3.3 CONSIDERATIONS

Assumption of maintenance responsibility by the user is not to be taken lightly or without serious consideration of the economics involved. If the field service engineer were to be dedicated to Phoenix 211 Subsystems, it would take a total of 12 Disk Drives and 6 Phoenix 211 Disk Drives to break even, in terms of paying for labor, parts, and equipment.

## PHOENIX 211 DISK CONTROLLER

### 3.0 MAINTENANCE TOOLS

#### 3.1 Disk Diagnostic Program

The chief maintenance tool provided by Xylogics is the Phoenix 211 Disk Diagnostic Program. This program is designed with the Philosophy that nothing in the disk controller operates properly, and it attempts to prove just that.

The Disk Diagnostic initially exercises the smallest amount of disk controller logic possible to determine proper operation. Once proper operation has been verified, this logic is then used to exercise additional logic. This process is then repeated until all of the disk controller logic has been tested.

A natural byproduct of this approach is that the logic being exercised in any test or subtest can usually be readily identified.

#### 3.2 Disk Diagnostic Program Manual

The Phoenix 211 Disk Diagnostic Program Manual provides the user with complete instructions on how to operate the Phoenix 211 Disk Diagnostic Program in addition to specific details on what functional logic is being exercised by each test, and on what board(s) the logic is physically contained on are provided.

The intent is to enable the user to determine what functional logic is inoperative, and what board(s) are suspect by running the diagnostic program and noting what specific test and subtest an error occurs on.

#### 3.3 Functional Logic Partitioning Guide

For those users who desire to become involved in troubleshooting to the component level a functional logic partitioning guide is provided which identifies each functional logic block by name, physical board where it is located, and a drawing sheet reference.

#### 3.4 Documentation Conventions Glossary

A documentation convention glossary is also provided, which explains in detail all documentation conventions and symbology utilized by Xylogics in the Phoenix 211 logic drawings.

This glossary should go a long way towards minimizing the amount of user time required to familiarize himself with the hardware for maintenance purposes.

### 3. 5. Hardware Documentation Package

A complete hardware documentation package is supplied with each Phoenix 211 Disk Controller. This hardware documentation package includes:

- . Logic Drawings
- . Assembly Drawings
- . Parts Lists
- . Wiring Lists
- . Drawing Directory

Care has been taken to maximize the amount of information provided to the user by functionally partitioning, labeling, and adding notes wherever appropriate to all logic drawings.

### 3. 6. Operators Manual

An operator's manual is provided which covers all topics from physical unpacking, installation, and checkout to providing detailed descriptions of each user defined parameter, and instructions on how to change such parameters.

The operator's manual provides an insight into the myriad of options provided by the Phoenix 211 Disk Controller to the user, as well as an insight into how the parameters are logically implemented in the disk controller.

The Phoenix 211 operator's manual is recommended reading for those users intending to perform their own component level maintenance.

### 3. 7. Phoenix 200 Formatter Interface Manual

The Phoenix 211 Disk Controller physically consists of the Phoenix 200 Disk Formatter and the Phoenix 211 Interface Board.

The Phoenix 200 Disk Formatter is equipped with a standard interface which is adapted to the PDP-11 Unibus by the Phoenix 211 Interface Board. (The Phoenix 200 Formatter has been interfaced to many other computers as well)

The Phoenix 200 Formatter Interface Manual describes in detail the signal, electrical, and timing relationships required to cause the Phoenix 200 Disk Formatter to perform the required disk data transfer operations.

This manual is likewise, recommended reading material for those users interested in performing their own component level maintenance.

#### 4.0 PHOENIX 211 DISK SUBSYSTEM MAINTENANCE DON'TS

1. Do not touch any hardware associated with the disk controller or disk drive without first analyzing fault symptom, as defined by supplied diagnostic program.
2. Do not remove any printed circuit board of disk controller or disk drive without first turning power off.
3. Do not, under any circumstances, take down another working system in order to attempt to isolate a fault in a defective system. More often than not, two defective systems will result.
4. Do not, under any circumstances, randomly substitute spare boards into a defective system. More often than not defective system will not be fixed and disposition of spare boards will be compromised.
5. Do not substitute more than one spare board at a time into a Phoenix 211 Disk Subsystem. Changing more than one board at a time does not facilitate fault isolation to the board level and increases the probability of inducing additional faults into the system, by inserting boards into the wrong backplane locations (particularly on the disk drives).
6. Do not attempt to diagnose a disk subsystem problem using any type of operating system or with any valued data pack on any of the disk drives connected to the disk controller. Use of any data pack on a suspect disk subsystem will more likely than not, result in the loss of data contained on any such pack, and will not provide any useful diagnostic information.
7. Do not call Xylogics for assistance if a disk subsystem problem occurs, until after the supplied disk diagnostic program has been run and the following information can be supplied to Xylogics personnel.
  - . Failing Test Number
  - . Failing Subtest Number
  - . Actual Erroneous Test Data Obtained
  - . Reference Test Data
  - . Failing Program Count Value
  - . System Configuration
    - . Computer Model
    - . Memory Capacity
    - . Other peripherals on System
    - . Position on Bus of Phoenix 211 Interface Board
  - . Disk Drive Type and Model
  - . Number of Disk Drives

Telephone calls indicating such system failure symptoms as "FAILED TO BOOT", "HOME BLOCK READ ERROR", etc. have no significance to Xylogics personnel and are a waste of time and money.



## Phoenix 211 Disk Controller

### Maintenance Manual

#### 5.0 Controller Physical Organization and Logic Partitioning

##### 5.10 General

The Phoenix 211 Disk Controller physically consists of a total of five hex 8½" x 15" printed circuit boards compatible with any standard DEC backplane assembly.

##### 5.20 Phoenix 200 Formatter

- 5.2.1 Four of the printed circuit boards are mounted in a supplied four slot systems unit type backplane assembly.
- 5.2.2 The systems unit backplane assembly can be mounted directly in any standard computer or BALLK Expansion Chassis which physically has room.
- 5.2.3 Power for the backplane assembly and associated printed circuit boards is provided by the host computer or expansion box, and a power harness to connect to the power distribution connector of the host is also supplied.
- 5.2.4 The four boards and backplane assembly constitute the Phoenix 200 Formatter which is also sold as a separate product by Xylogics.
- 5.2.5 The four printed circuit boards comprising the Phoenix 200 Formatter are identified as simply "Phoenix 200 Formatter Board 1,2, 3, or 4" in all associated documentation.
- 5.2.6 The Phoenix 200 Formatter is not physically tied to the host PDP11 Computer Unibus.
- 5.2.7 Each pin of all connectors on a given I/O slot of formatter backplane assembly is bussed to the same pin on all of the other three I/O slots of the backplane assembly.

Hence any Formatter board can be plugged into any I/O slot of the backplane assembly to facilitate maintenance operations.

##### 5.30 Phoenix 211 Coupler (PDP11 Interface Board)

- 5.3.1 The fifth printed circuit board assembly, the Phoenix 211 Coupler, is used to interface the Phoenix 200 Formatter to the PDP11 Unibus.
- 5.3.2 The Phoenix 211 Coupler Board occupies one standard hex Small Peripheral Controller (SPC) I/O slot available in any DEC PDP11 computer or expansion chassis, and is connected to the Unibus or said computer.

5. 3.3 The hex I/O slot used for the Phoenix 211 Coupler Board must be altered to allow the DMA Non Processor Grant Signal to pass serially through the board as specified in the installation instructions.

NOTE: In most cases the alteration consists of cutting one wire on the I/O slot backplane.

- 5.3.4 The Phoenix 211 Coupler Board is physically connected to the Phoenix 200 Formatter via a 50 conductor shielded ribbon cable provided for that purpose.

#### 5.4.0 Physical Logic Partitioning

The total logic of the disk controller has been physically partitioned on a functional basis to achieve modularity and flexibility.

The following sheets provide a tabulation of the functional logic blocks contained on each of the five controller printed circuit board assemblies, as well as logic drawing sheet reference to facilitate controller maintenance.

Phoenix 211 Disk Controller  
Physical Logic Partitioning  
Phoenix 211 PDP11 Interface Board

The following functional logic blocks are physically contained on the Phoenix 211 PDP11 Interface Board. (Reference Logic Drawing D1025)

<u>Functional Logic Block</u>	<u>Drawing Sheet Reference</u>
1) Unibus Data Bus Buffering Logic	1
2) Unibus Address Bus Buffering Logic	1
3) Interrupt Vector Logic	1
4) Interrupt Priority Selection Logic	1
5) Unibus Control Signal Buffering Logic	1
6) Unibus DMA Control Logic	2
7) Unibus Interrupt Control Logic	2
8) DMA Throttle Logic	2
9) Main Bus Address Register	3
10) Strip Option Address Register	3
11) Strip Control Logic	3
12) DMA Word Count Register	4
13) Register Address Decode Logic	4
14) Formatter Interface Logic	5

Phoenix 211 Disk Controller  
Physical Logic Partitioning  
Phoenix 200 Formatter Board 1  
(Non Queue)

The following functional logic blocks are physically contained on Board 1 of the Pheonix 200 Formatter. (Reference Logic Drawing D1032)

Functional Logic Block	<u>Drawing Sheet Reference</u>
1) Formatter Coupler Interface Logic	1
2) Formatter Register Address Control Logic	1
3) Formatter Interrupt Request Logic	1
4) Command & Status Register	2
5) General Error Logic	2
6) Error Register	2
7) Multiple Computer Arbitration Logic	3

Phoenix 211 Disk Controller  
Physical Logic Partitioning  
Phoenix 200 Formatter Board 2

The following functional logic blocks are physically contained on the Phoenix 200 Formatter Board 2. (Reference Logic Drawing D1033-01)

<u>Functional Logic Block</u>	<u>Drawing Sheet Reference</u>
1) Seek Logic	3
2) Disk Status Register	4
3) FIFO Transfer Request Delay Logic	4
4) Data Late Error Detection Logic	4
5) DMA Request Control Logic	4
6) Even, Odd FIFO Memories	5
7) Optional Data Port Interface	1
8) FIFO Read Data Multiplexing Logic	1
9) FIFO Write Data Multiplexing Logic	1
10) FIFO Write/Read Control Logic	1
11) Serial to Parallel Data Conversion	2
a.) Data Shift Register #1	
b.) Data Shift Register #2	
c.) Shift Register Data Multiplexer	
12) Data Shift Register Control Logic	2
13) Write Check Error Logic	2

Phoenix 211 Disk Controller

Physical Logic Partitioning

Phoenix 200 Formatter Board 3

The following functional logic blocks are physically contained on the Phoenix 200 Formatter Board 3. (Reference Logic Drawing D1034-01)

<u>Functional Logic Block</u>	<u>Drawing Sheet Reference</u>
1) CRC Generation & Check Logic	1
2) Self Test Logic	1
3) Bad Sector Ident Detect & Skip Logic	1
4) Sector Write Protect Logic	1
5) Header Check Logic	1
6) Disk Sequencer Logic	3
7) Disk Word Count Register	4
8) Sequencer Word Count Logic	4
9) Controller Busy/Done Logic	4
10) Seek Start Logic	4
11) Servo Offset Done Delay Logic	4
12) Linkage Strip Word Count Logic	4
13) Unit, Sector, Head Register	5
14) Maximum Sector Detect Logic	5
15) Maximum Head Detect Logic	5
16) Head and Cylinder Incrementation Logic	5
17) Command Decode Logic	2
18) End of Sequence Control Logic	2
19) Sector Coincidence Enable Logic	2
20) Maintenance Panel Switch Write Protect Logic	2
21) Maintenance Panel Indicator Logic	2

Phoenix 211 Disk Controller

Physical Logic Partitioning

Phoenix 200 Formatter Control Data Corp. Compatible Board 4

The following functional Logic Blocks are physically contained on Board 4 of the Phoenix 200 Formatter. (Reference Logic Drawing D1035)

<u>Functional Logic Block</u>	<u>Drawing Sheet Reference</u>
1) Power Fail Detect Logic	1
2) Disk Control Bus Logic	1
a.) Control Data Bus Drivers	
b.) Tag Bus Drivers	
c.) Cylinder Tag Logic	
d.) Head Tag Logic	
e.) Control Tag Logic	
f.) Tag Timing Logic	
3) Miscellaneous A Cable Disk Interface Logic	1
a.) Fault	
b.) Seek Error	
c.) On Cylinder	
d.) Unit Ready	
e.) Unit Select $\emptyset$ , 1	
f.) Port Busy	
4) Physical Port $\emptyset$ Radial Cable Disk Interface	2
5) Physical Port 1 Radial Cable Disk Interface	2
6) Physical Port 2 Radial Cable Disk Interface	2
7) Physical Port 3 Radial Cable Disk Interface	2
8) Sector Coincidence Detector	3
9) Cylinder Address Register	4
10) Maximum Cylinder Detect Logic	4
11) Header Control Logic	4
12) Port $\emptyset$ -3 Sector Count Logic	5
13) Sector Count Multiplexing Logic	5
14) Sector Interleaving Logic	5
15) Data and Clock Multiplexing Logic	5

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6.0 Documentation Standards and Conventions

6.1.0 General



Standard documentation standards are utilized on all of the logic drawings provided in this manual in order to convey as much information as possible to the user.

The following sections of this document are devoted to defining the standards used.

6.2.0 Backplane Signal Identification Symbol

6.2.1 All logic signals coming from or going from a printed circuit board to the backplane assembly via any of edge connectors are identified on the logic drawings with diamond symbol (<>).

6.2.2 The connector and pin number by which any such signal is to be interfaced to the backplane assembly is contained above the diamond symbol enclosed in square brackets.

Example:  Example:  Connector and pin No.

6.3.0 Ribbon Cable Connector Identification Symbol

6.3.1 Ribbon Cable Connectors, if used, are normally contained on the top of a printed circuit board assembly.

6.3.2 If more than one such connector is used on a printed circuit board, the rightmost connector (when viewing the board from the component side) is labeled J1. Subsequent connectors moving to the left are labeled J2, J3, etc.

6.3.3 Pin 1 of any ribbon cable connector is located on the left side of the connector when viewed from the component side of the board.

6.3.4 Any signal going to or coming from a ribbon cable connector is identified by the symbols >>, >, or << in conjunction with the connector number, pin number, and signal name.



An example of a signal going to a ribbon cable connector is as follows:

>> J3-34 READH

- 6.3.4.1 If a ribbon cable edge connector is the source of a signal, the connector symbol, connector number, pin number and signal name will appear to the left of the point where it is used.
- 6.3.4.2 If a ribbon cable edge connector is a load for a signal generated on a board, the connector symbol, connector number, pin number, and signal name will appear to the right of the source for the signal.

#### 6.4.0 Signal Name Conventions

##### 6.4.1 Signal Active State Designation

The active state of any named signal appearing on any supplied logic drawings may be readily determined by examining the signal name associated with the signal.

The last character of the signal indicates the active state of the signal per following:

##### 6.4.1.1 Case 1 - Signal Source is Non Memory Logic Element

If the source of a signal is a gating logic element the last character of the signal name will be an H or L depending on whether the signal is active when in the logic 1 state or logic  $\emptyset$  state respectively.

##### 6.4.1.2 Case 2 - Signal Source is Memory Logic Element

If the source of a signal is a memory element such as a flip flop, the last character of the signal name will be (1) or ( $\emptyset$ ) depending on whether the signal is active when the memory element is set or reset respectively.

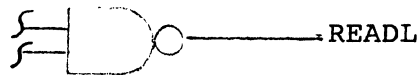
##### 6.4.2 Signal Name Philosophy

- 6.4.2.1 A signal will normally be named if it is used on more than one sheet of logic drawings, or if it is used so many times on one sheet such that it cannot be interconnected without "cluttering up" the drawing.
- 6.4.2.2 Signal names, when used, will normally be limited to 7 characters or less, and will reflect as close as possible, the operation or function of the associated signal.

### 6.5.0 Signal Sheet Cross Referencing

Signals appearing on the supplied logic drawings fit into three categories not previously discussed. By noting the conventions used in signal cross referencing, the user may quickly determine whether a signal has additional loads on the same or other sheets of the logic drawings.

- 6.5.1 If a signal is used elsewhere on the same sheet, the signal name is appended to the end of a straight line at the signal source. An example of this is:



- 6.5.2 If a signal is not used anywhere else on the current logic sheet, but is used on other sheets, a circle is appended to the end of a line at the right of signal source, and all other sheets where the signal is used are identified in parenthesis immediately above the circle.

An example of this signal cross reference is:



READL is not used anywhere else on sheet, but is used on sheets 4 & 5.

- 6.5.3 If a signal is used elsewhere on the same sheet, and also used on other sheets, a solid circle is appended to the end of a line at the right of the signal source, and all other sheets where the signal is used are identified in parenthesis immediately above the solid circle.

An example of this signal cross reference is:



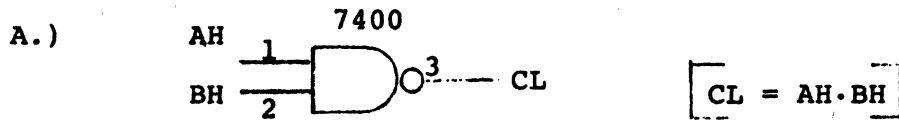
READL is used elsewhere on logic sheet as well as on sheets 4 & 5.

### 6.6.0 Logic Symbology

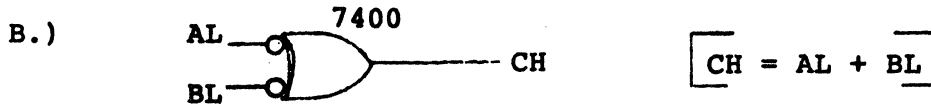
- 6.6.1 Logic symbols used in all supplied documentation are industry standard and are used in a manner conducive to making the logic prints easy to understand.

#### 6.6.2 AND/OR Interpretation

Logic elements, particularly gating elements may be drawn as either an "AND" or as an "OR" function. In all supplied documentation, a gating element will be drawn as either an "AND" or "OR" function as appropriate, to best convey the logical function being implemented. Hence a standard 7400 NAND Gate may be drawn as:



or



L = Active State = Logic 0

H = Active State = Logic 1

### 6.6.3 MSI, LSI Symbology

Medium scale and large scale integrated circuit devices used are symbolically shown as a rectangular box with the suppliers functional notation inside the box next to the associated circuit pin.

### 6.6.4 Manufacturer's Part Number Listing

The common manufacturer's part number is located prominently inside or outside any logical device used to facilitate cross referencing and user understanding of any questionable device function.

### 6.7.0 Printed Circuit Board Component Orientation

Integrated circuit components for most boards supplied are organized on a grid basis.

6.7.1 The component grid supplied consists of both rows and columns.

6.7.2 A component is assigned a grid address based on the row column coordinates associated with its location per the following:

#### 6.7.2.1 Row Coordinate

The integrated circuit components are normally organized horizontally into 10 rows on a hex sized printed circuit board. These rows are assigned A,B,C,D,E,F,G,H,J,& K with the "A" row being just above and covering the six backplane edge connectors.

#### 6.7.2.2 Column Coordinate

The integrated circuit components are normally organized vertically into 12 columns on a hex sized printed circuit board identified as 1-12. The columns are assigned consecutively right to left with column 1 being at the right hand side of the board when viewing the component side of the board with the board vertical and resting on the backplane edge connectors.

### 6.7.2.3 Component Location Designation

The location designation of any component appearing on all documentation is determined by the row coordinate followed by the column designation.

Hence, the location designation of the component appearing on the extreme lower right hand corner of printed circuit board is "A1" while the location designation of the component at the extreme top left hand corner of the printed circuit board is "K12".

## Phoenix 211 Disk Controller

### Maintenance Manual

#### 7.0 Required Test Equipment

The following equipment is required to test and maintain the Phoenix 211 Disk Controller.

<u>Item</u>	<u>Quantity</u>	<u>Equipment Description</u>
1	1	PDP11 Computer with a minimum of 8192 words of memory
2	1	DEC W984 Quad Extended Height Extender Board
3	1	DEC W987 Double Extended Height Extender Board
4	3	Pomona 3916 Dip Clip - 16 pin dual inline integrated circuit test clip or equivalent
5	1	Tektronix 453 Dual Channel Oscilloscope with external trigger, X10 Probes, or equivalent
6	1	WTCPN Weller Controller Temperature Soldering Iron or equivalent
7	1	"Micro-Shear" 175 Flush Safety Cutter or equivalent
8	1	Xcelite 41CG Needle Nose Pliers or equivalent
9	1	Precista T-2C Solder Removal Tool or equivalent
10	A/R	Alpha 815 Flux or equivalent
11	A/R	Service Chemical D-Sol F-13 Defluxer or equivalent
12	1	Solder Removal Co. Insertic #880 Insertion Tool or equivalent
13	A/R	Solder, 63/37 Rosin Core

PHOENIX 211 DISK CONTROLLER

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8.0 RECOMMENDED SPARES

8.1.0 PHOENIX 211 SPARES LIST

PRICE

Interface	\$1000
Board 1 Standard	1150
Board 1 with Command Queue	2000
128 Word Buffer Board 2	1000
512 Word Buffer Board 2	1300
Board 3	1000
CDC Board 4	1200
Calcomp Board 4	1200
Cables & Terminator	500

8.2.0 CDC 9762 DISK DRIVE SPARES LIST

Field Exerciser for Disk Unit	3200
First Level Spares for CDC 9762 1 head, 1 set of boards, tools	3500
Alignment Pack	1750

## PHOENIX 200 DISK CONTROLLER

### 9.0 MBTF Prediction Calculations

#### 9.1 Reference Used

Reliability calculations were made using the MIL-HDBK 217B, Parts Count Prediction Method.

#### 9.2 Reliability Prediction Formula

The formula used to predict reliability MBTF is:

$$\lambda_{\text{Equip}} = \sum_{i=1}^{i=n} N_i (\lambda_G \eta_Q)^i$$

Where:  $\lambda_{\text{Equip}}$  = Total rate of failure ( /10<sup>6</sup> hr)

$\lambda_G$  = Generic failure rate for ith part

$\eta_Q$  = Quality factor for ith part

$N_i$  = Quantity of ith part

$n$  = Number of categories

NOTE: Only Failures which cause non-operation were included.

#### 9.3 Disk Controller Configuration

The Phoenix 211 Disk Controller configuration used in the reliability prediction calculations was as follows:

- . Phoenix 211 Interface Board
- . Phoenix 200 Board 1
- . Phoenix 200 Board 2
- . Phoenix 200 Board 3
- . Phoenix 200 Board 4
- . Phoenix 211 Autoswitch Board

#### 9.4 Calculation Summary

For the 211, with interface and autoswitch, the calculations are as follows:

9.4.1	Component Failures	F/10 <sup>6</sup> hours
9.4.2	Integrated Circuits	88.98
9.4.3	Capacitors	12.48
9.4.4	Resistors	.85
9.4.5	Connectors, edge	3.13
9.4.6	Connectors, right angle	.625
9.4.7	Other	<u>.509</u>
	Total:	106.074
		Failures/10 <sup>6</sup> hours

#### 9.5 Predicted MBTF

The net result is a predicted MTBF of 9500 hours.



## Phoenix 211 Disk Controller

### Maintenance Manual

#### 10.0 Data Flow Sequence

##### 10.1.0 Normal Disk Write Sequence

- 10.1.1 When write operation is initiated data is transferred a word at a time via DMA through 2:1 Multiplexer into Latch register preceding FIFO memories.
- 10.1.2 All odd data words are transferred from the latch register into FIFO Memory #1.
- 10.1.3 All even data words are transferred from the latch register into FIFO Memory #2.

Such DMA transfers will continue until both FIFO memories are full or until the DMA Word Counter overflows.

- 10.1.4 When disk controller is in synchronism with the disk drive and the beginning of the sector data field is reached, data is transferred in parallel from the two FIFO memories to one of the two shift registers.
- 10.1.5 Data is then shifted serially from one of the shift registers to the disk.
- 10.1.6 Data Words are alternately loaded into Shift Register #1 and then Shift Register #2.
- 10.1.7 When the contents of one shift register are being transferred to the disk, the other shift register is loaded from the FIFO memories with the next word to be transferred.
- 10.1.8 The Disk Word Count Register is incremented once for each word transferred to the disk.

##### 10.2.0 Normal Disk Read Sequence

- 10.2.1 Data is received serially from the disk drive and into one of the two serial shift registers.
- 10.2.2 When a 16 bit data word has been accumulated, the serial data bit stream is diverted to the other shift register and the data word collected is transferred in parallel to one of the two FIFO Memories.

The Disk Word Count Register is incremented once for each word that is received from the disk.

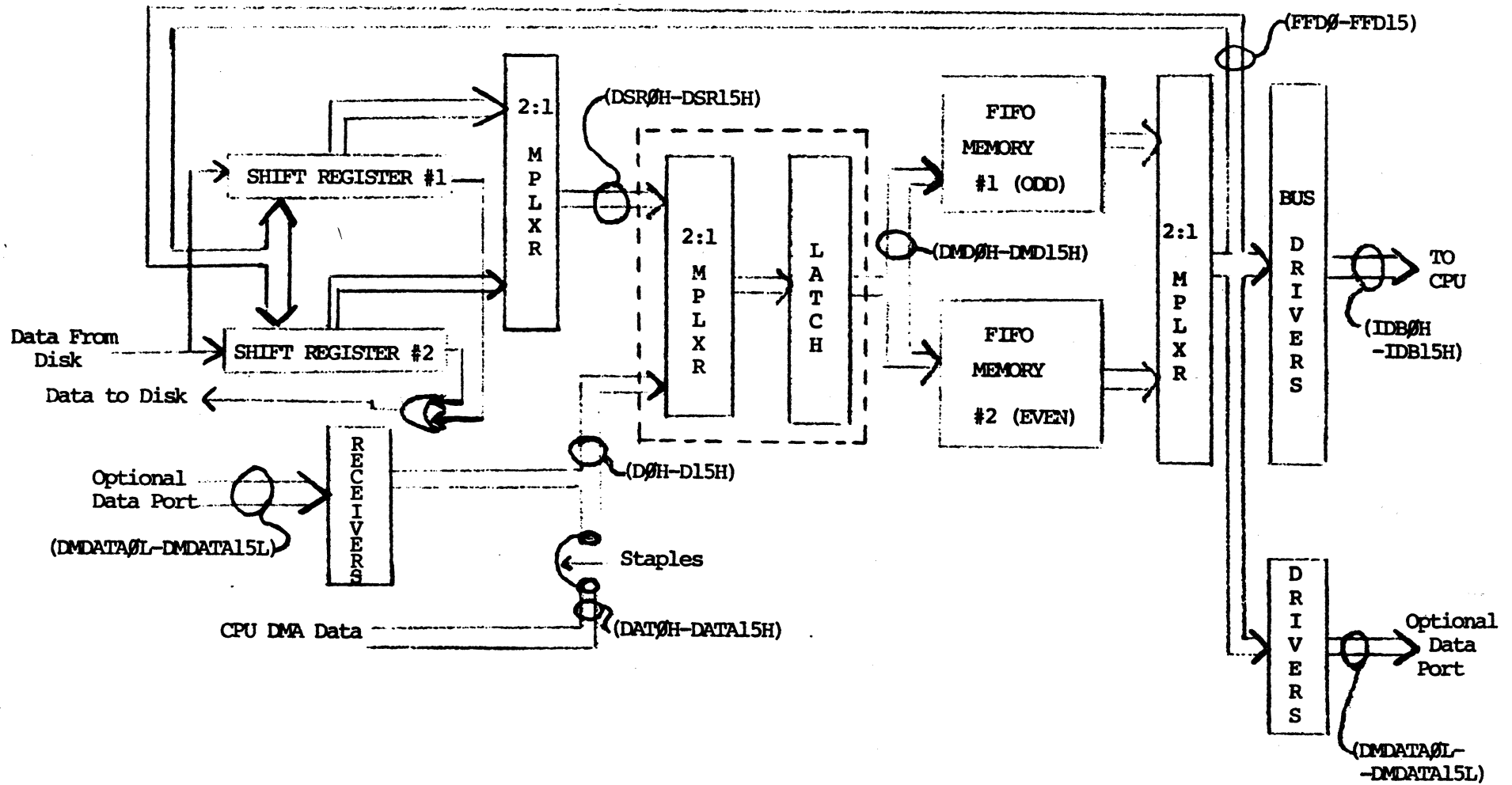
- 10.2.3 Normally all odd data words are formed in Shift Register #1 and stored temporarily in FIFO Memory #1 while all even data words are formed in Shift Register #2 and stored temporarily in FIFO Memory #2.
- 10.2.4 When the presence of data is detected in either FIFO, DMA requests are initiated to the host computer.

Data Words are extracted alternately from the two FIFO memories until either the DMA word Count Register overflows or the FIFO memories are empty of all disk data.

PHOENIX 211 DISK CONTROLLER

Data Paths Block Diagram

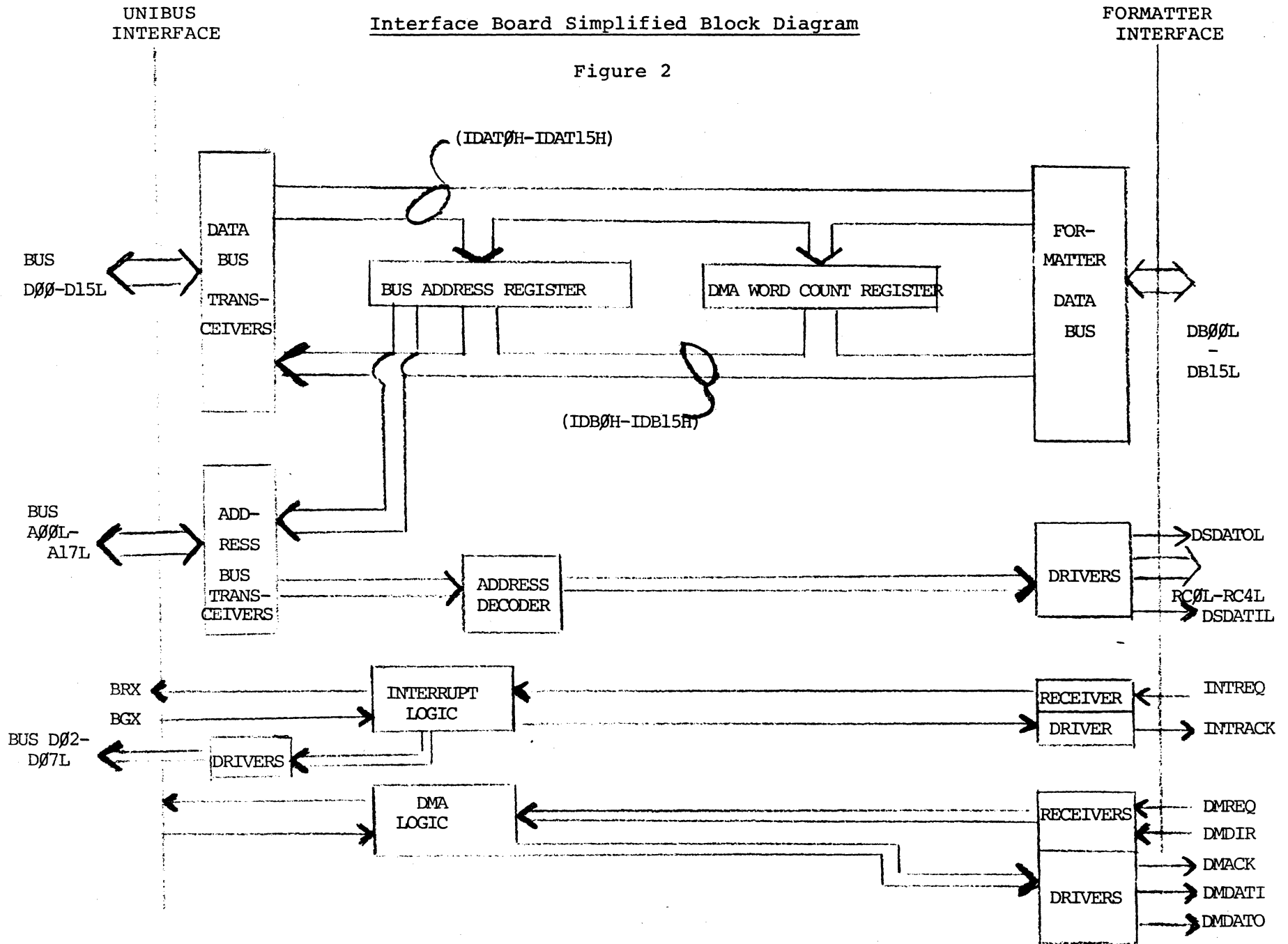
Figure 1



Phoenix 211 Disk Controller

Interface Board Simplified Block Diagram

Figure 2



## 11.0 Hardware Documentation

11.1 The following sections of this manual contain all of the hardware documentation for the Phoenix 211 Disk Controller. For each major Phoenix 211 Sub Assembly the following documentation is provided:

- . Parts List
- . Assembly Drawing
- . Wiring Lists\*
- . Logic Drawings\*

\* Where appropriate.

11.2 The first section contains an overall drawing Directory or "Phoenix 211 Family Tree", for the Phoenix 211 Disk Controller.

11.3 The major Phoenix 211 Subassemblies organized in order of presented in this manual are as follows:

1. Phoenix 211 Interface Board
2. Phoenix 200 Board 1
3. Phoenix 200 Board 2
4. Phoenix 200 Board 3
5. Phoenix 200 Board 4
6. Phoenix 200 Systems Unit
7. Phoenix 211 Interconnect Cable
8. Disk Drive A Cable
9. Disk Drive B Cable
10. Phoenix 211 Autoswitch Board

## ECC LOGIC DESCRIPTION

### I Error Correction Code Logic Block Diagram Discussion

Figure 1 is a block diagram of the circuits used to implement error correction processing within the Formatter. The circuits on this diagram can be looked at as performing three separate functions, all related to error correction code processing.

1. Generation of a 32-bit ECC redundancy code during write operations. This information is written serially on the disk immediately following the 256 word data field (Figure 2).
2. Checkout of the ECC redundancy field during read operations to detect the possible presence of a data check error. The check is made by ANDing together the low order 21 bits of the ECC register and looking for a zero status.
3. Entry into the error correction process on detection of a data check error indicated by the fact that the low order 21 bits of the ECC register are not zeros. This has two immediate effects with respect to the Phoenix 211 Interface lines:
  - . The DONE (INTRL) signal normally inserted at the end of a transfer is inhibited or delayed until completing error correction processing.
  - . The CRC error (CRCERR) bit in the Error Register is set causing the setting of the composite error bit in the control and status register.

Following the error correction process, the Formatter detects one of two conditions:

1. Detects the 11-bit error burst and its position (physical location within the data field). The burst pattern and position information are supplied to the software operating system via the appropriate registers.
2. Determines that the error is non-correctable and sets the error correction hard error bit in the ECC Bit Location Count Register.

II Generating and Writing the ECC Field (Write Operation) - Generating and writing the ECC redundancy code in the ECC field (Figure 1) occurs when the Formatter executes either of the write commands. The code is formed within the ECC shift register during the time that the data field is written onto the disk. Each bit shifted from the shift register (for transfer to the disk) is also entered into the ECC shift register. This is accomplished as follows:

- a. Signal (WGH) WRITE GATE H (applied to the ECC register feedback control logic) is asserted since a write operation is in progress.
- b. At the start of the data field, signal (WCCGH) WRITE CHECK CHARACTER GATE is negated. This in turn causes A7-6 to switch high and enable the ECC register feedback gating.

ONES and ZEROS coming from the shift register (signal DATAOUTL) now enter the ECC shift register throughout the data field transfer. In this way, the ECC redundancy code (to be written onto the disk following the data field) is formed. At the end of the data field, signal WCCGH asserts because it is now time to write the ECC field associated with the data just written. Signal WCCGH inhibits the ECC Register feedback at A6-2, the ECC Register is now shifted to the NRØ data latch (on Board 2 SH2 of logics) where the serial pulse train of write data is generated (DATAOUT)

III Checkout of the ECC Redundancy Code (Read Operation) - During read operations, the ECC redundancy code is formed again by applying each data field bit read from the disk to the ECC shift register. When reading from the disk, the enabling of the ECC register feedback gating is effected in the following way:

- a. With a read operation undertaken, signal (RDGATEH) READ GATE (applied to the ECC register feedback control logic) is asserted.
- b. At the end of the Preamble #2, signal DATAH asserts to define the start of the data field.
- c. Signal WCCGH is negated to enable the ECC register feedback gating and thereby allows each bit coming from the disk (READDATAH) to enter the ECC register.

Applying each bit read from the disk to the ECC register (with the feedback loop enabled) reconstructs the same code that was attached to the ECC field when the data was written.

When the end of the data field is reached, signal DATAH negates; however, signal WCCGH is negated to maintain signal A7-6 at the asserted level allowing the ECC field bits coming from the disk (READDATAH) to enter the ECC register while the feedback loops are still enabled.

When the ECC redundancy code read from the disk and clocked into the ECC register matches that developed (in the ECC register) at the close of reading the ECC field (Signal RCCGATE - read check character gate) then the 21 low order bits of the ECC register all contain zeros. This means that the data field has checked out OK. As a result, signal E1-4 (zero's detect) asserts and sector processing is terminated normally by raising the EOSH signal.

NOTE

The 21 low order bits of the ECC pattern register are ANDed together. When all bits are zeros, signal E1-4 (zero detect) asserts.

When the 21 low order bits of the ECC register fail to contain all zeros, it means that there is an error in the data read from the disk. The actual location and the nature (soft or hard) of that error is not known at this time. The Formatter now enters the error correction process (provided it is not inhibited from doing so) as described in the subsequent paragraphs.

IV Error Correction Processing - When signal E1-4 (zero detect) fails to assert at the end of the ECC envelope, the data check error detect logic issues three outputs that are used as follows:

1. Signal ECCERROR (1) asserts to set bit 8 (data check error) in the Error Register.
2. Signal CRCERR (1) asserts. This is used in the Busy/Done logic to inhibit generation of the DONE (Formatter Ready) signal.

NOTE

If the Error Correction Inhibit (ECI) bit in the ECC pattern register is set, INTRL signal is sent to the Interface. The error correction process in this case, is inhibited

3. CRCERR (1) is applied to enable the ECC correction enable logic. The latter circuit now asserts A9-5 (correction enable) provided that the error correction enable signal (ECCENB (1) is asserted.

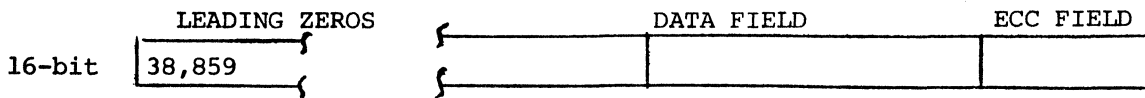
Assertion of A9-5 together with CRCERR (1) begins the error correction process and has two immediate effects:

1. It negates signal A4-8 via the ECC register feedback control logic to force zero's as data. (This is essential for the error correction process).
2. Enables clocking of the leading zero's word counter to maintain a count of each bit serially shifted within the ECC register.

NOTE

The polynomial used for the error correction process is capable of accommodating a field much larger than the 256 word data field of each sector. For this reason, the Formatter goes through a process of shifting leading zeros within the ECC register and feedback paths. The zero's word counter maintains a count of the leading zeros. This is done so the time at which error correction code processing enters the data field can be decoded and the task of detecting the 11-bit error burst can begin.

The number of leading zeros shifted within the pattern register depends on the Data Field format that is being used. The leading zero value is shown below: for a data field of 256, 16 bit words.



When the applicable number of leading zeros has been counted, the data field entry detect logic asserts signal B5-9 (Leading zero's counter overflow.) This acts as an enabling signal to the position register shift lock enable gating. The position register keeps a count of data field bits shifted (in the ECC register) until such time as the 11-bit error burst is located. A second use of signal B5-9 is its application to the error burst detect clock circuits. Here it acts as an enabling signal (i.e., in an anticipation of detecting the 11-bit error burst) because the shifting of bits is now within the data field. Conditions are now set up for detecting the presence of the error burst in the 11 high order bits of the ECC register. That portion of the ECC register is also called the "ECC pattern" register. Design is such that the location of the 11 bit error burst is detected as being identified when the 21 low order bits all contain zeros (i.e., as a result of the continuous shifting/feedback process). An all zero condition is sampled in the zero detect gating and asserts signal zero ( $\emptyset$ ). On application to the ECC correction enable logic, signal Zero ( $\emptyset$ ) produces the following results:

- a. Inhibits the position register shift clock enable gating to stop the count of the position register at that point in the data field (or ECC field). The count stored in the "ECC position" register identifies the physical location within the data field, of the first bit of the 11-bit error burst.
- b. Causes the error burst detect logic to assert signal ECCABOL. This, in turn, has a double effect:



1. Inhibits the ECC register shift clock enable gating so that no further shifting of bits occurs in the ECC register. This is necessary because the 11 high order bits ("ECC pattern" containing the error burst) must now be sent to the central processor.
2. Forces the DONE generation logic to send an INTR signal to the Interface. This is done to indicate that error correction processing is complete and that the CPU may now take the contents of the ECC position and pattern registers.

c. Inhibits further counting by the leading zero's word counter.

This completes Formatter error correction processing for those cases where the location of the error burst is detected within the data field and the error is correctable. If the error correction logic fails to detect an error burst within the data (or ECC) field, the Formatter notifies the CPU of a "hard error" condition. This condition is indicated to the logic by the fact that the Bit Location counter has exceeded the maximum size of the entire ECC code length without having found an all zeros condition in the low order 21 flip-flops of the ECC register.

#### NOTE

By definition, "hard error" means that the Formatter failed to detect a correctable error burst within the data or ECC fields.

The error correction logic keeps a count of the bits being shifted in the pattern register after the shifting process enters the data field. Consequently, when the Bit Location counter reaches a value of 4128<sub>10</sub> bits\* (following entry into the data field) it means that no error burst has been detected and the uncorrectable error bit must be set in the bit location count register. This occurs when the data field entry/hard error detect logic determines that the count from the Bit Location counter has gone past the ECC field and asserts signal UNCORDER (1).