file: MesaMu.Log   Mesa Microcode Log
Add entries at front

August 1, 1978; version 34; Fix bugs in stack underflow detection in MDpop and Dpop dispatches. Fix BL
**TC to remember even/odd alignment. [2 free words left] RL

July 26, 1978; version 33; Correct constant at Jscale from 100000 to 77777. [3 free words left] RJ

July 5, 1978; version 32; Fix signed comparison bytecodes to handle overflow correctly (Suzuki's algori
**thm). Add BLTC bytecode. Eliminate 1 instruction each in nextXB logic and FetchAB. Eliminate 3 ins
**tructions by combining JEQ and JNE logic. Miscellaneous corrections to comments and some predefs. [
**3 free words left] RL

March 6, 1978; version 31b; Ensure DISP non-zero at KFCr. Add RFC. [3 free words left] RJ & RL

March 2, 1978; version 31a; Entry conditions for all trap handlers changed: trap parameters now passed
**in registers, and interrupts never disabled. AV, SD, GFT now bound to fixed addresses. RR and WR ch
**anged appropriately, and additional RR added for real-time clock. Xfer traps implemented. BITBLT/in
**terrupts disabled bug fixed, ADD01 implemented. Miscellaneous optimizations to free space (RIL0, Jev
**en, SHIFT). [6 free words left] RL

February 14, 1978; version 30c; Fix bug in BITBLT (TASK error when interrupts pending but disabled). [
**8 free words left] RL

February 9, 1978; version 30b; Fix bug in EFCB (missing pre-def for EFCdoGetlink). [8 free words left]
** RL

January 20, 1978; version 30a; Global frame overhead reduced to 3 words. GP diddled to point at global
** 1 instead of 2 (because -6 not available in constants ROM). Links in either code segment or global
**frame supported. LLKB bytecode added. TASK violations on stack overflow fixed. [8 free words left]
** RL

January 16, 1978; version 29; Splitalpha uses dispatch instead of ShiftSub. ShiftSub moved to Mesad.mu
**. DESCB and DESCBS added. CVT and BLK removed. Symbolic names for frame offsets substituted for co
**nstants throughout. [22 free words left] RL

January 5, 1978; version 28; Miscellaneous cleanup. Replace 'verytemp' by 'saveret'. Change definitio
**n of 'mx' to free an R-register. Extend uses of 'taskhole'. Prepare for elimination of BLK and poss
**ibly CVT. [36 free words left] RL

January 3, 1978; version 27; Replace ABORT by REQUEUE. Change MRE to 2 parameters and ME to 1 paramete
**r. RJ

December 21, 1977; version 26; Move NovaDV to 25. Change MRE to 3 parameters. RJ

December 1, 1977; version 25; AllocTrap from ALLOC instruction must go through KFCr instead of directly
** to Mtrap. RJ

November 22, 1977; version 24; Complete rewrite of microcode, many new conventions and semantics. See
**separate documentation. RL

July 25, 1977; version 23a; Fixup code at alloc1z because -T-1 will not load T from ALU output. Requir
**ed extra instruction. Might want to try to optomize better later. RJ

July 24, 1977; version 22a; Change to single parameter alloc trap. Use double memory fetch at xferg. RJ
**

July 13, 1977; version 21a; Update RSTR and WSTR instructions to take offset from alpha instead of assu
**ming 4. RJ

July 7, 1977; version 20c; Tweak Mesa.bcpl. RJ

July 7, 1977; version 20b; Change Mesa.bcpl so that it does not skip the first item in Com.Cm if it has
** a .image extension. This is in anticipation of having the Executive "do the right thing" for runnin
**g Image files. RJ

June 20, 1977; version 20a; At DWDC1+3 change T←MD OR T to L←MD OR T. RJ

June 1, 1977; version 19b; New value of sGoingAway in mesa.bcpl and take out enableinterrupts jsr code
**in mesa-nova.asm. RJ

May 27, 1977; version 19a; New Format Procedure Descriptor. RJ

May 18, 1977; version 18a; No room for TASK at LFCxxx; deleted. New instructions IWDC and DWDC along w
**ith wdc register and shuffling of other registers to make room. Loadstate subroutine modified becaus
**e of interrupt change. RJ

April, 1977; version 17b; Implement Clark/Sproull/Johnsson convention for testing for presence of ROM1.
** RJ

March 23, 1977; version 17a; Had to move TASK at LFCn to after store of 0 into mx at LFCxxx+1. Also ta
**ke out loading of RAM to initialize registers. RJ

March 18, 1977; version 16d; Trouble with trap before PUSHX, frame alloc or code swap will change mx.
**This change fixed frame trap by pushing mx instead of my. The trap handler can now get my from the s
**tate (see 16c). When frame trap sees destination of 2MOD4 it will put the new frame back on the list
** and retry the xfer. Interrupts will remain off through PUSHX. In addition the compiler will not al
**low nexted procedures with large frames. RJ

March 9, 1977; version 16c; Can't disturb stack on BRK; instead get DST to save my by extra call to sav
**sub at DSTr1. RJ

March 8, 1977; version 16b; Move Mstopc to 777 for standard ROM1 check (convention developed with D. Cl
**ark). Change semantics of BRK: pass current L as parameter of trap and don't backup pc. RJ

February 18, 1977; version 16a; Changes before blowing PROMs. (1) Free up R14 for use by Trident code
**by moving my to S51. (2) Delete extra IR← in call of alloc since only one caller. (3) Implement LRU
** word in code segment at lgc. (4) Fix use of M across TASK at xfer2 and BLT. (5) Move Mgo to 420 so
** SWMODE from ROM0 will go to ROM1. (6) Add JRAM opcode (#366) to do SWMODE to address on stack. Mov
**e nxtib to 400 for return. RJ

February 18, 1977; version 15c; Make MUL, DIV and LDIV be unsigned. RJ

February 18, 1977; version 15b; Fix bug in bitmasks for unsigned compares. RJ

February 3, 1977; version 15a; Change opcode numbers to make room for
unsigned jumps. Add unsigned jumps, remove RBIT0, RBIT1. RJ