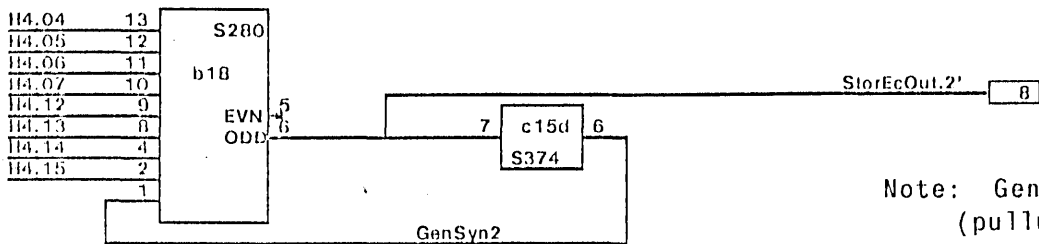
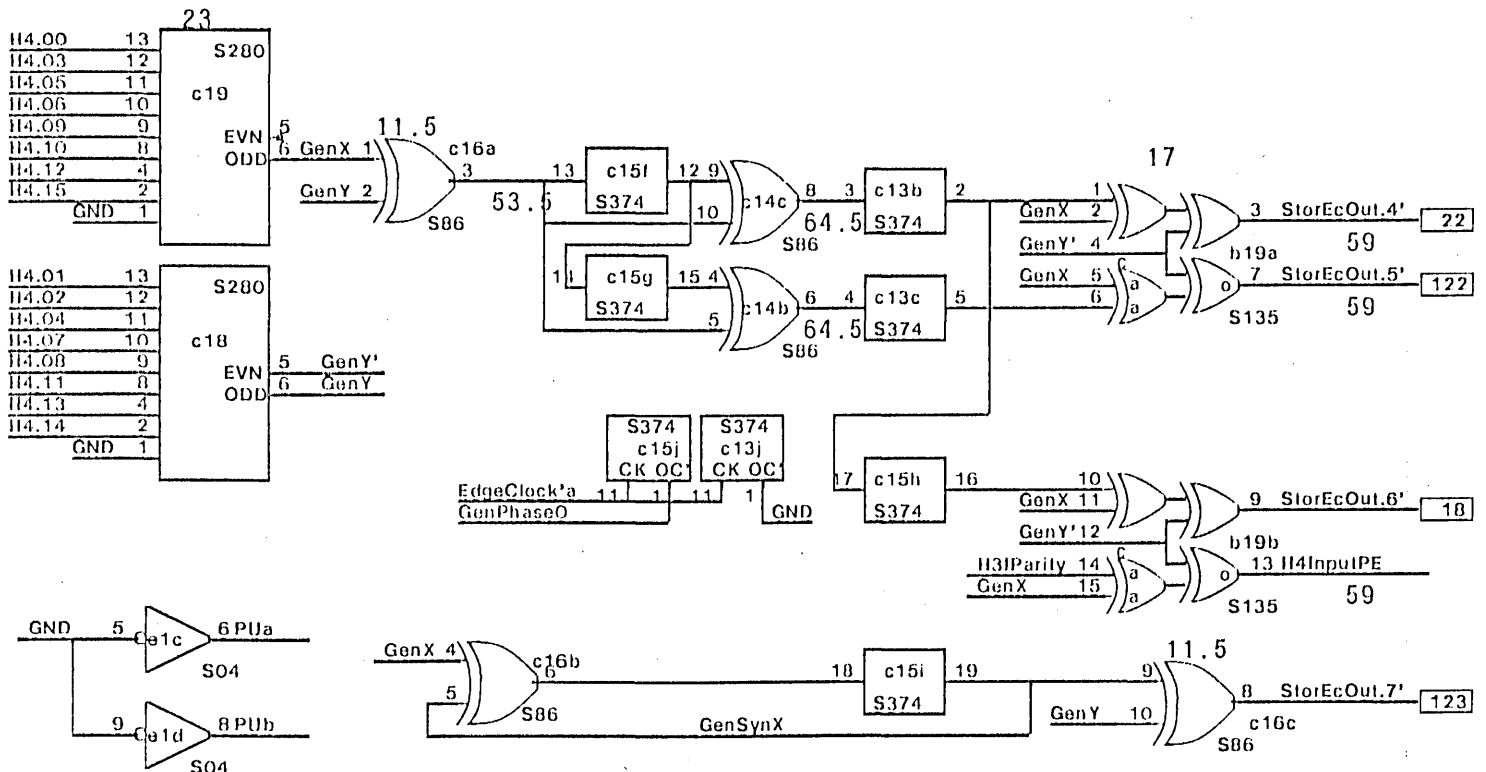
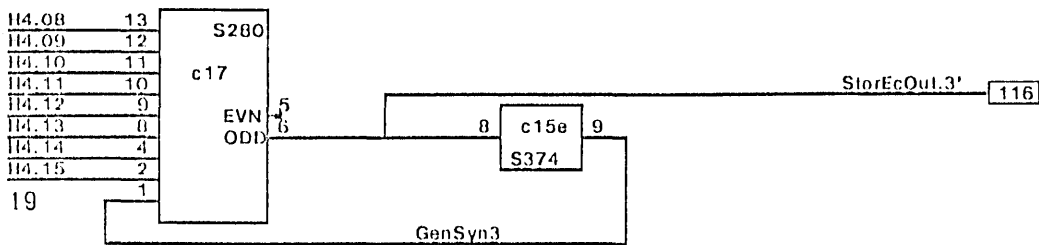
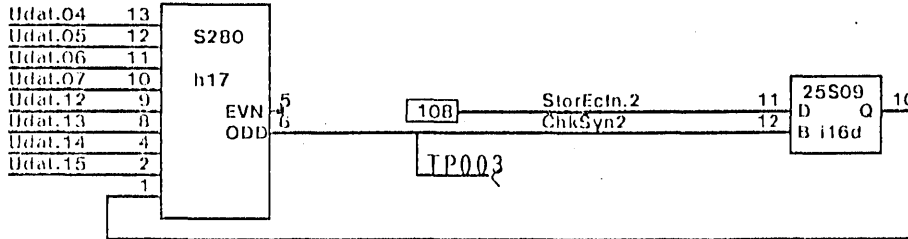
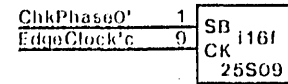
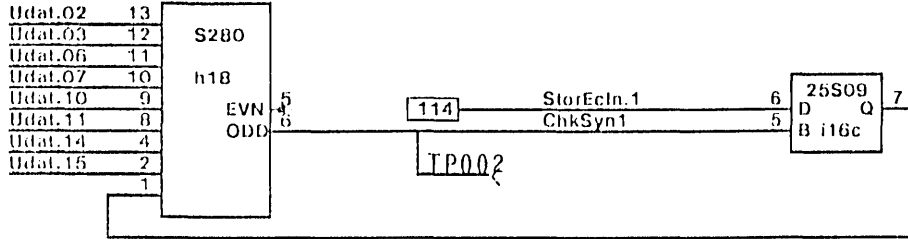
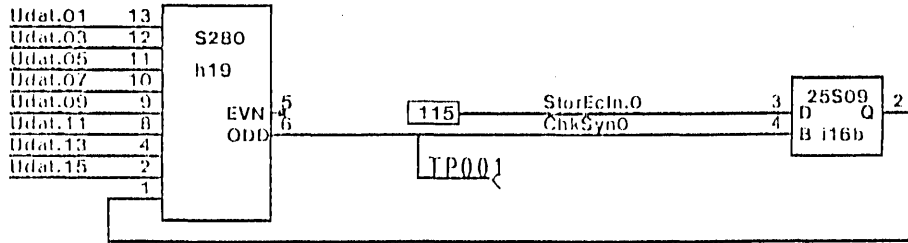


Note: Storage card inverts data and check bits.

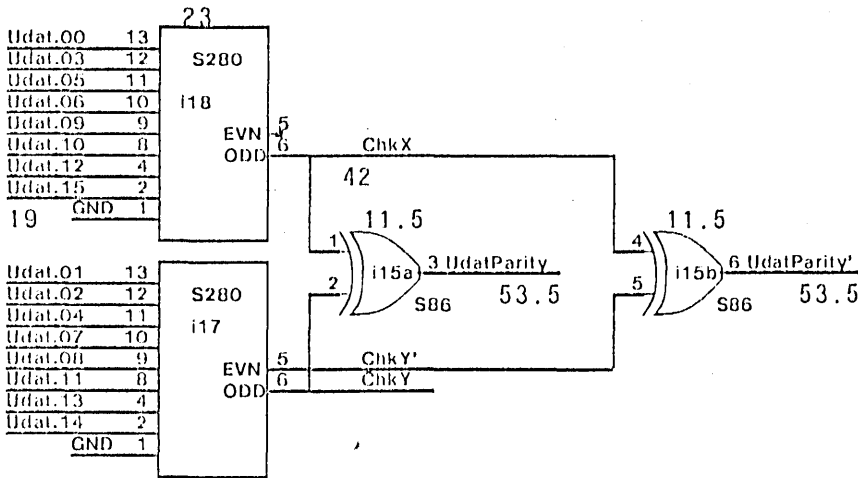
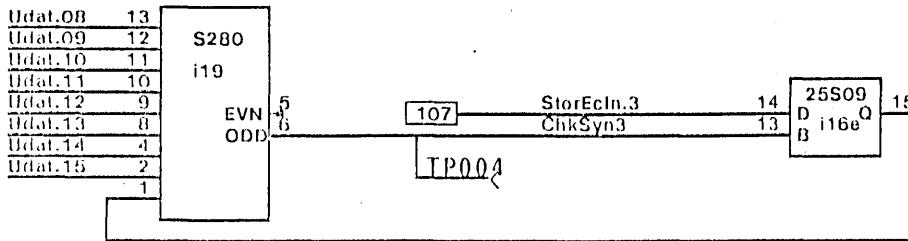


Note: GenPhase0 => GenSyn0,1,2,3,X = (pullups on page 12)

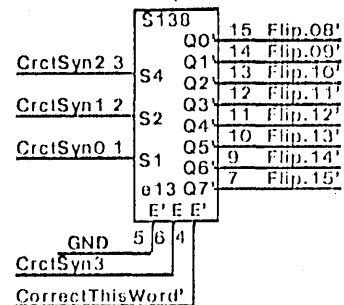
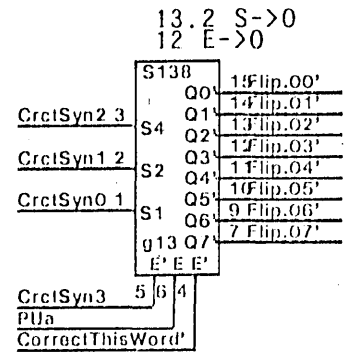


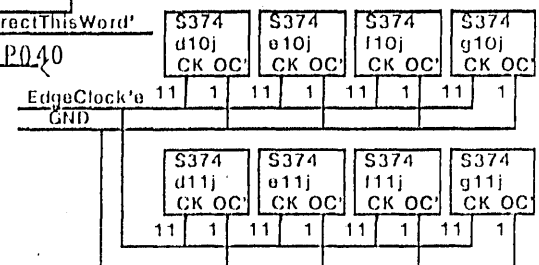
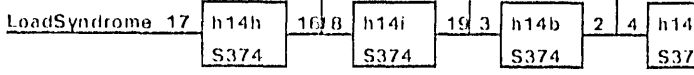
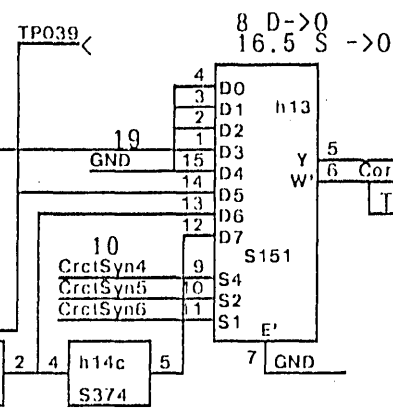
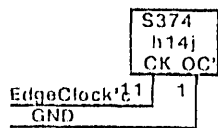
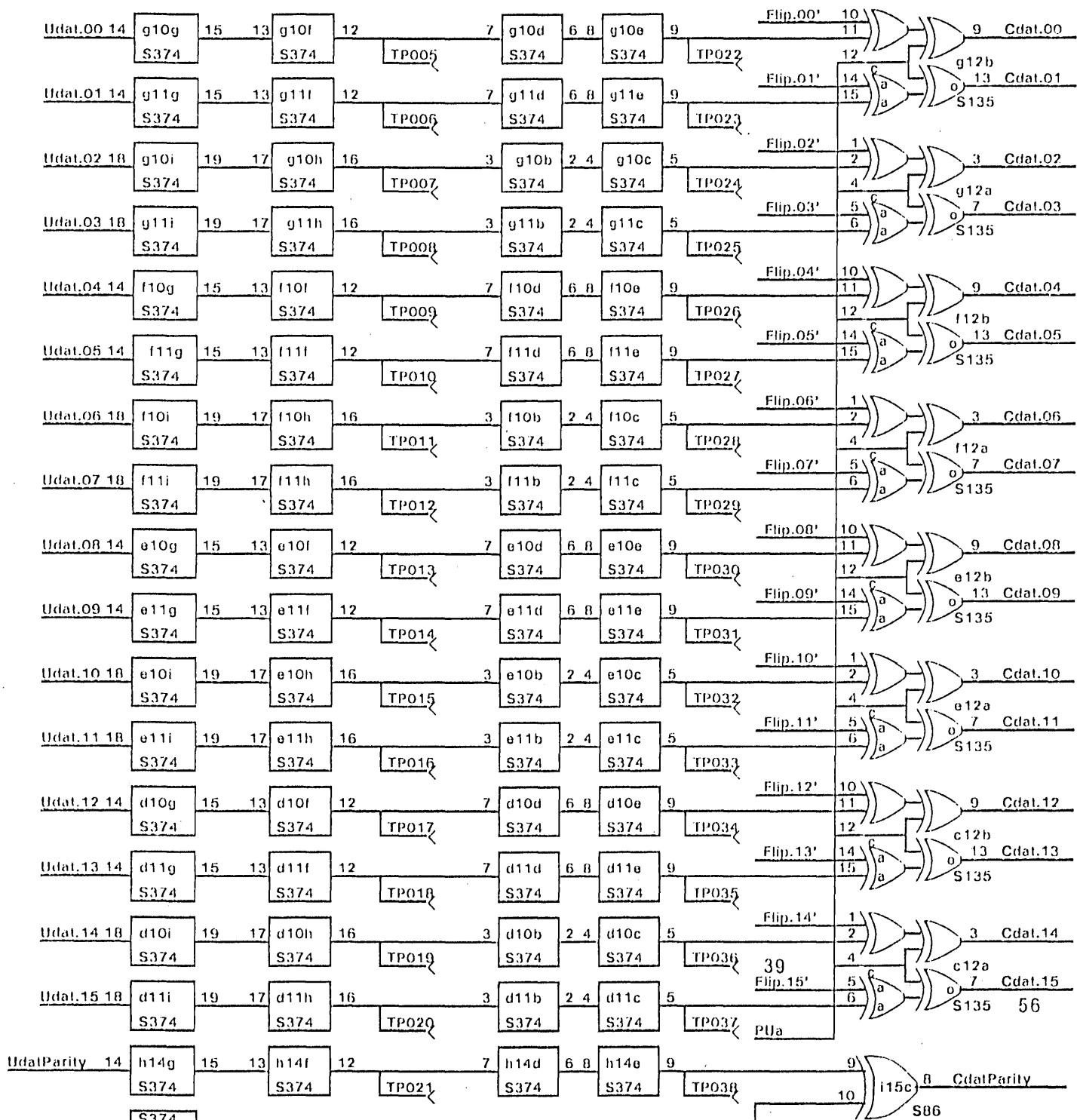


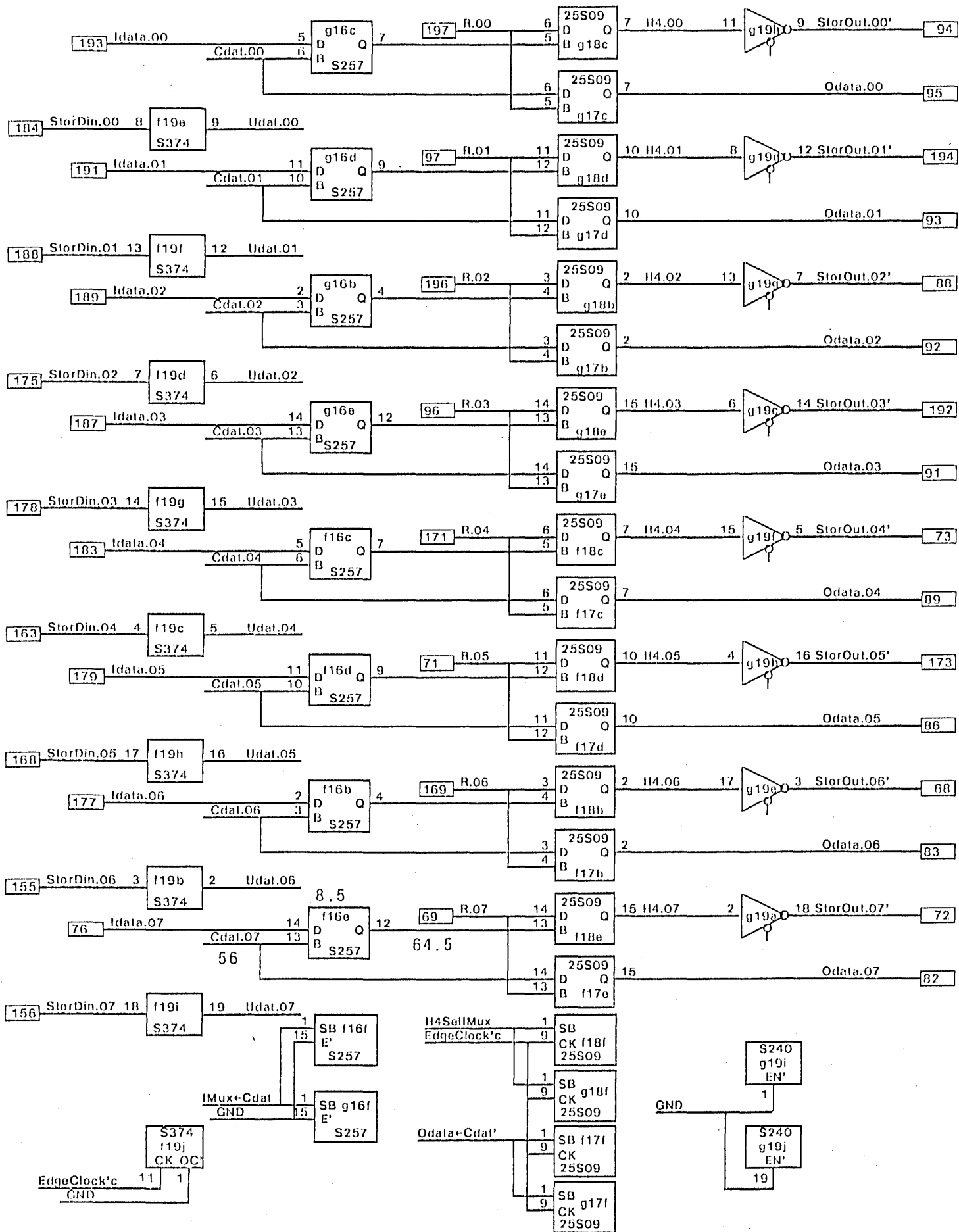
Note: Storage card inverts data and check bits

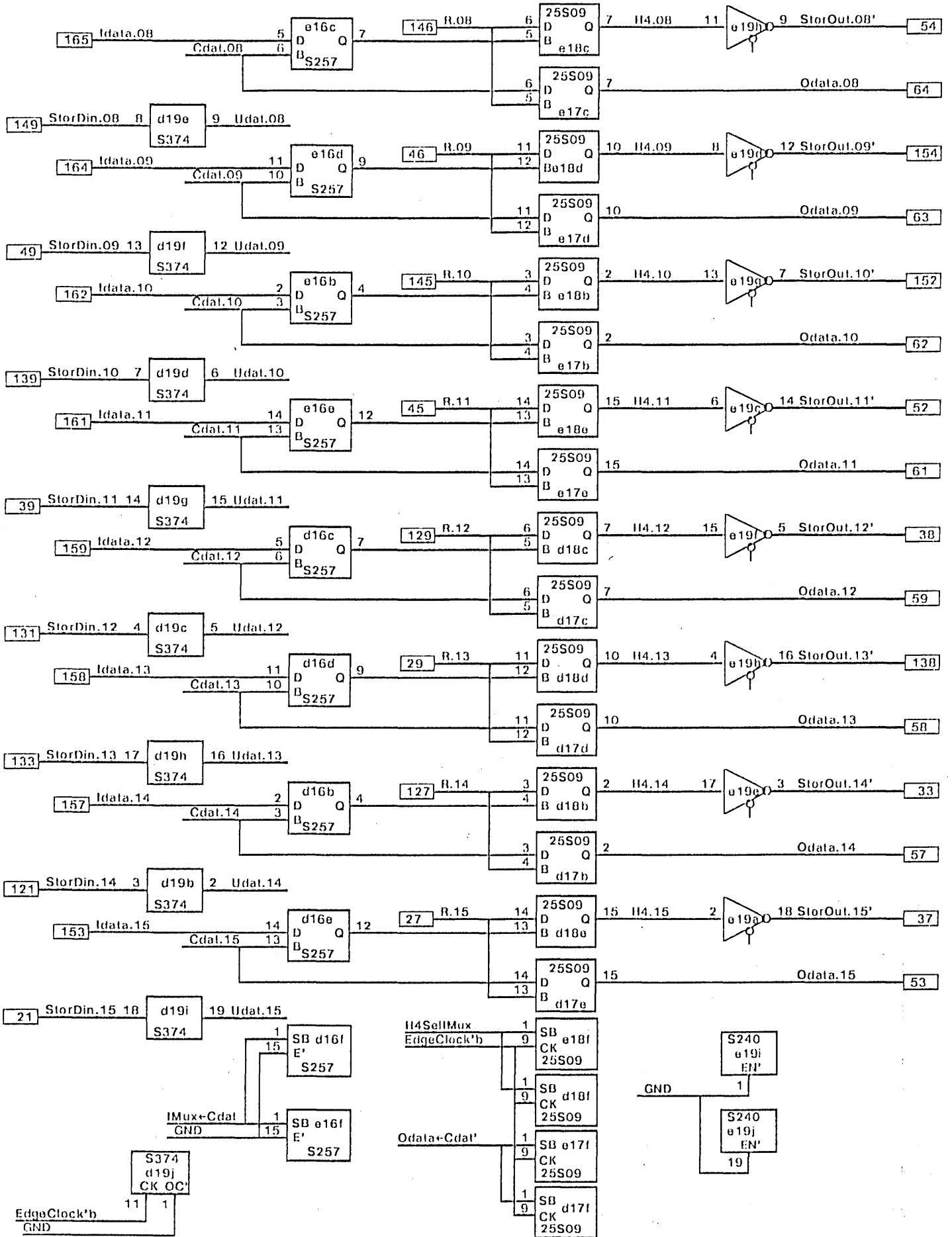


Note: Balance of checker is on pg. 6

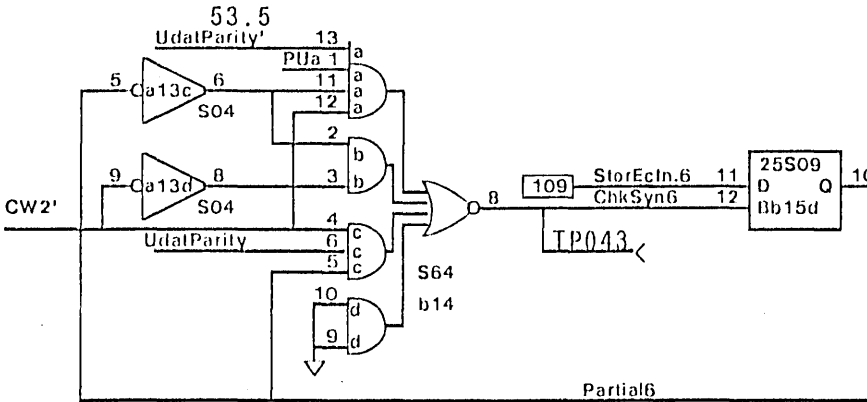
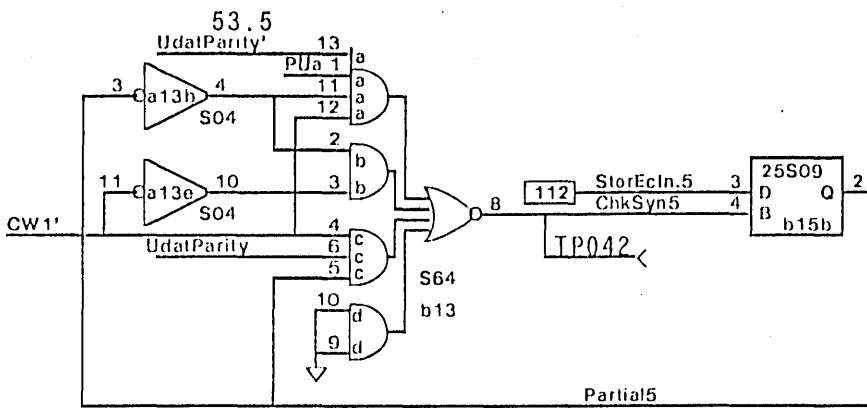
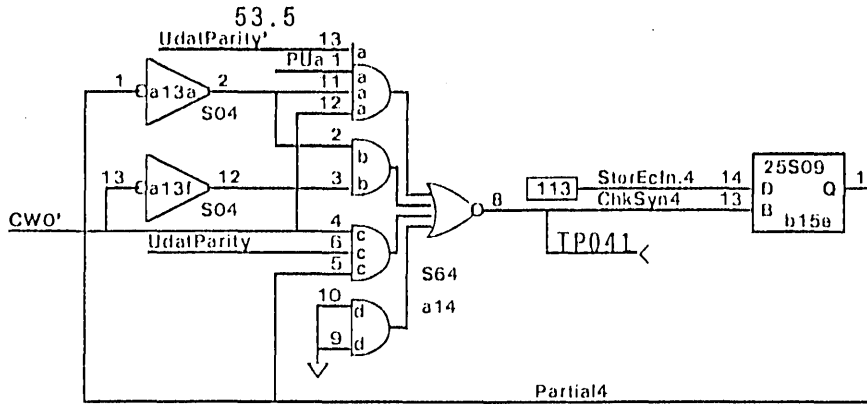








Note: Storage card inverts data and check bits

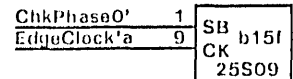
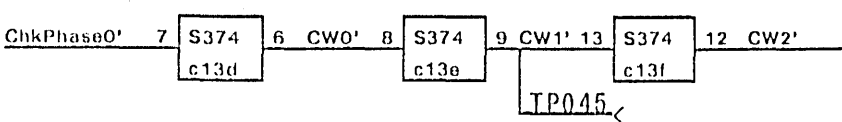
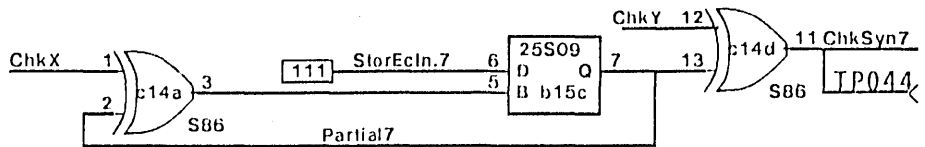


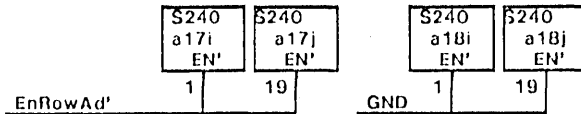
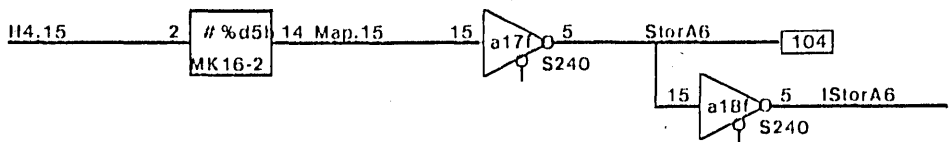
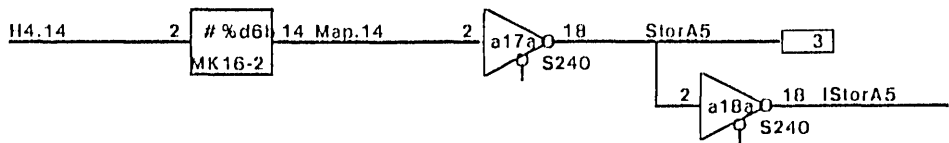
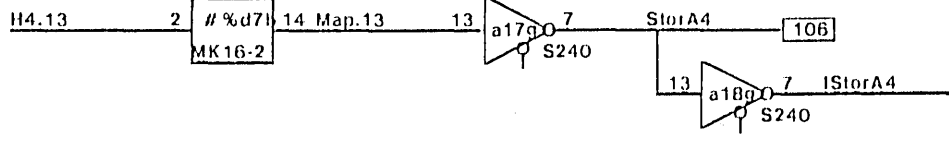
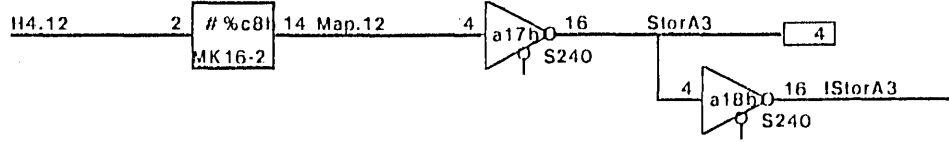
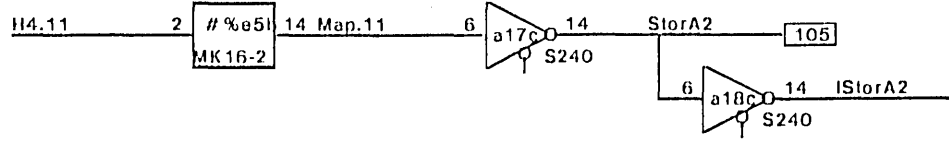
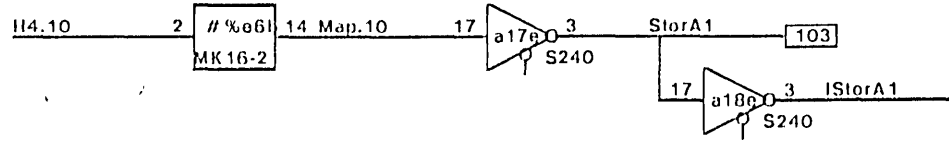
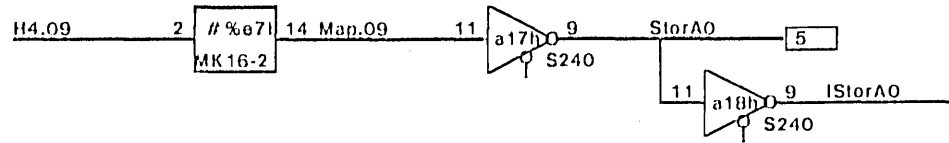
CW' = 1:

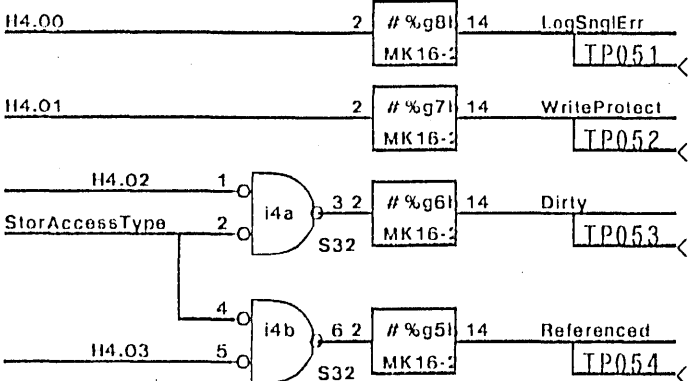
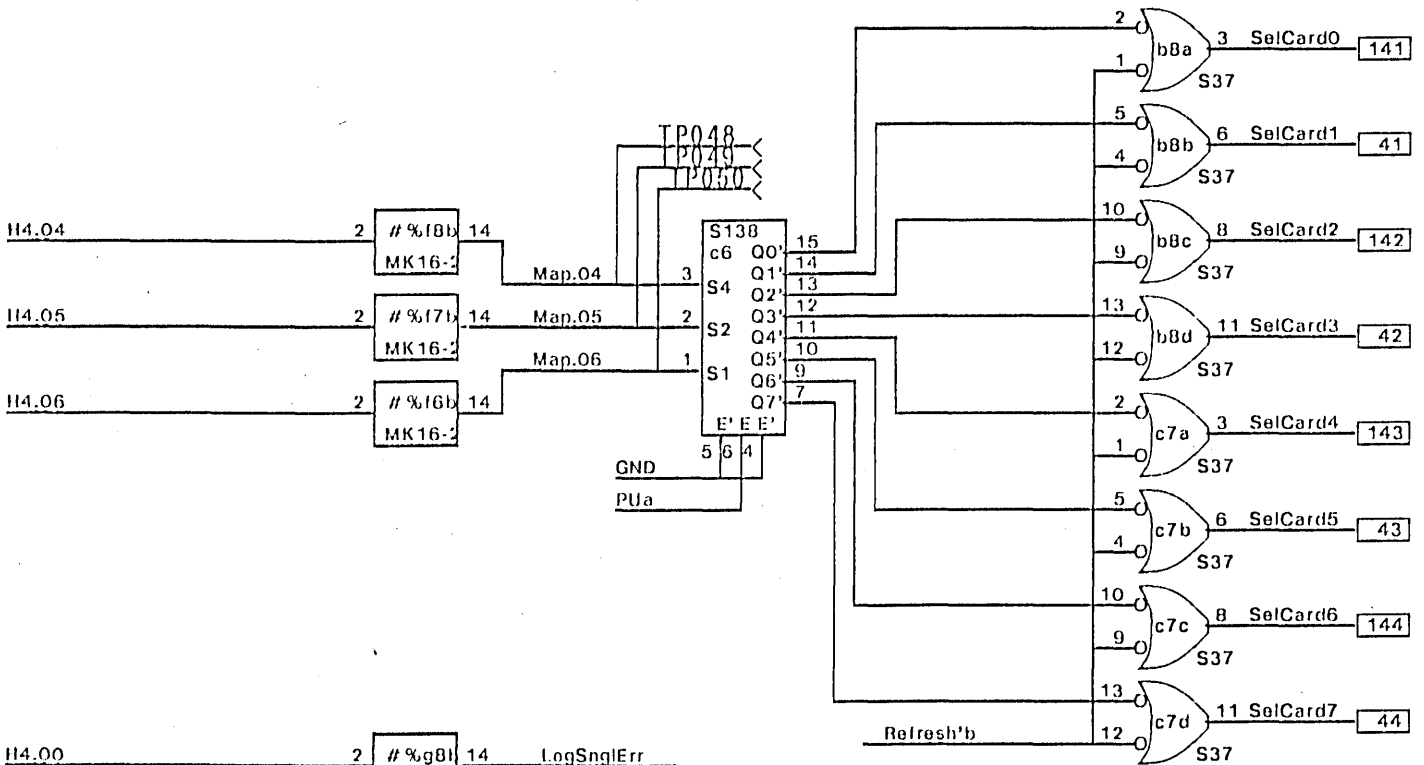
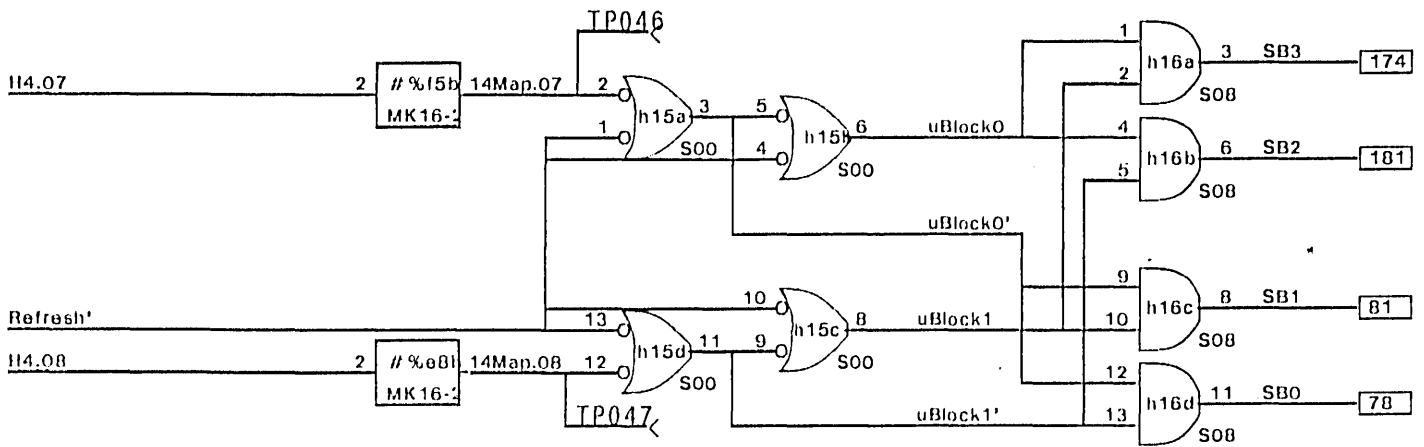
UdatParity	Partial4	ChkSyn4
0	0	0
0	1	1
1	0	1
1	1	0

CW' = 0

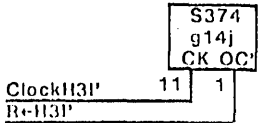
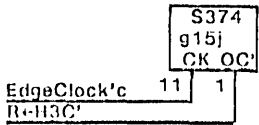
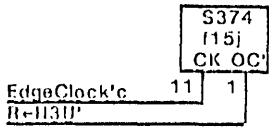
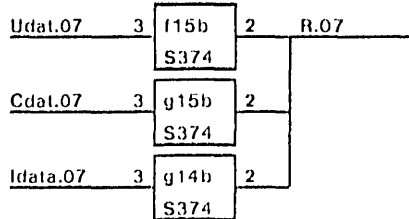
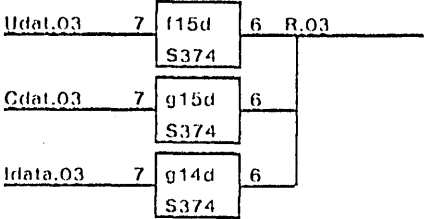
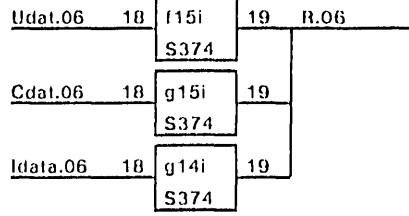
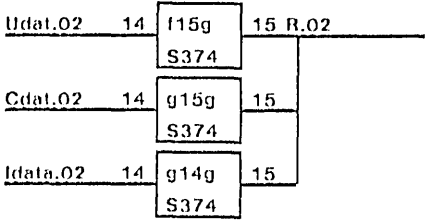
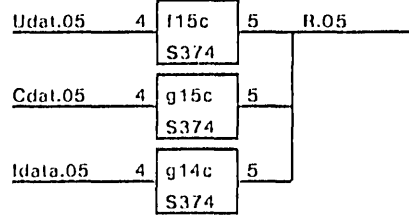
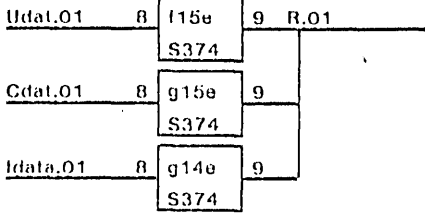
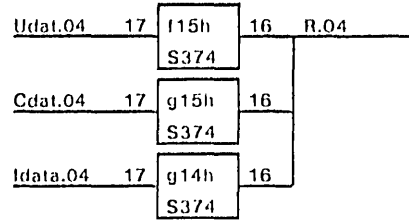
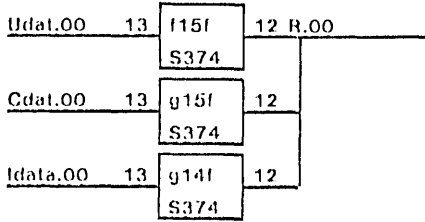
Partial5	ChkSyn5
0	0
1	1

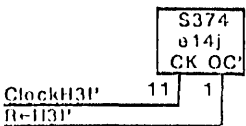
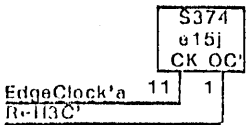
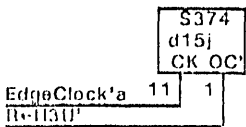
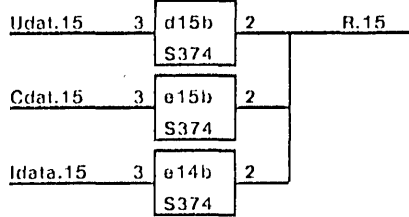
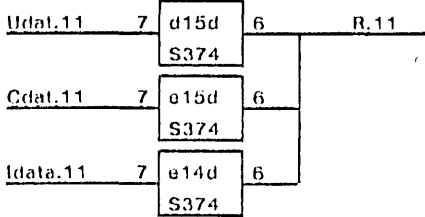
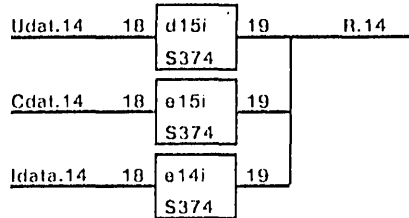
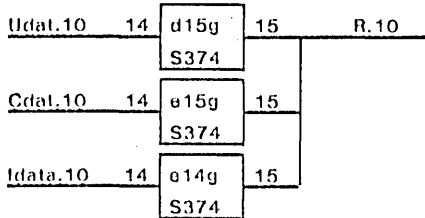
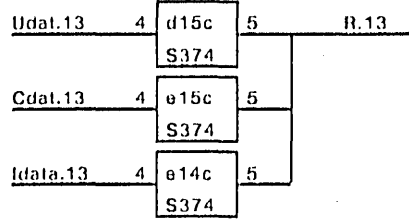
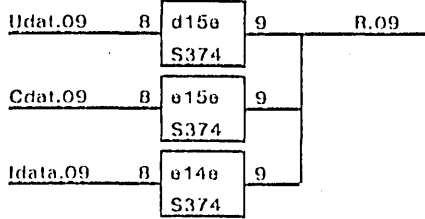
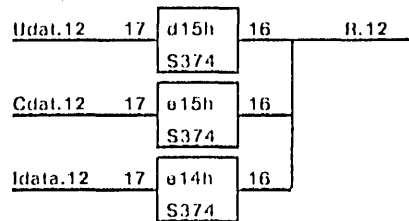
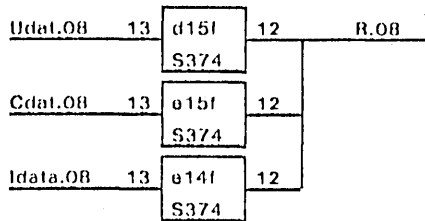




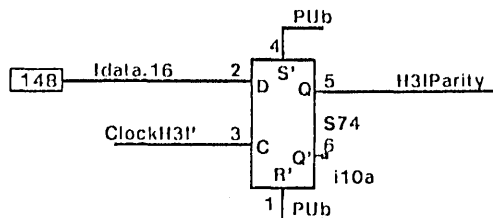
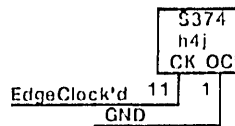
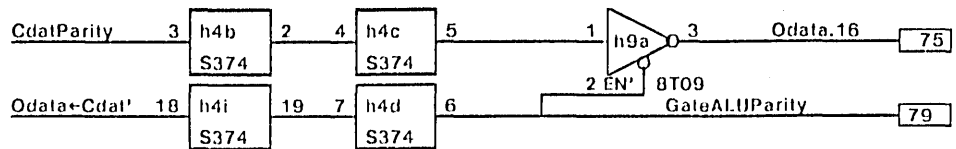


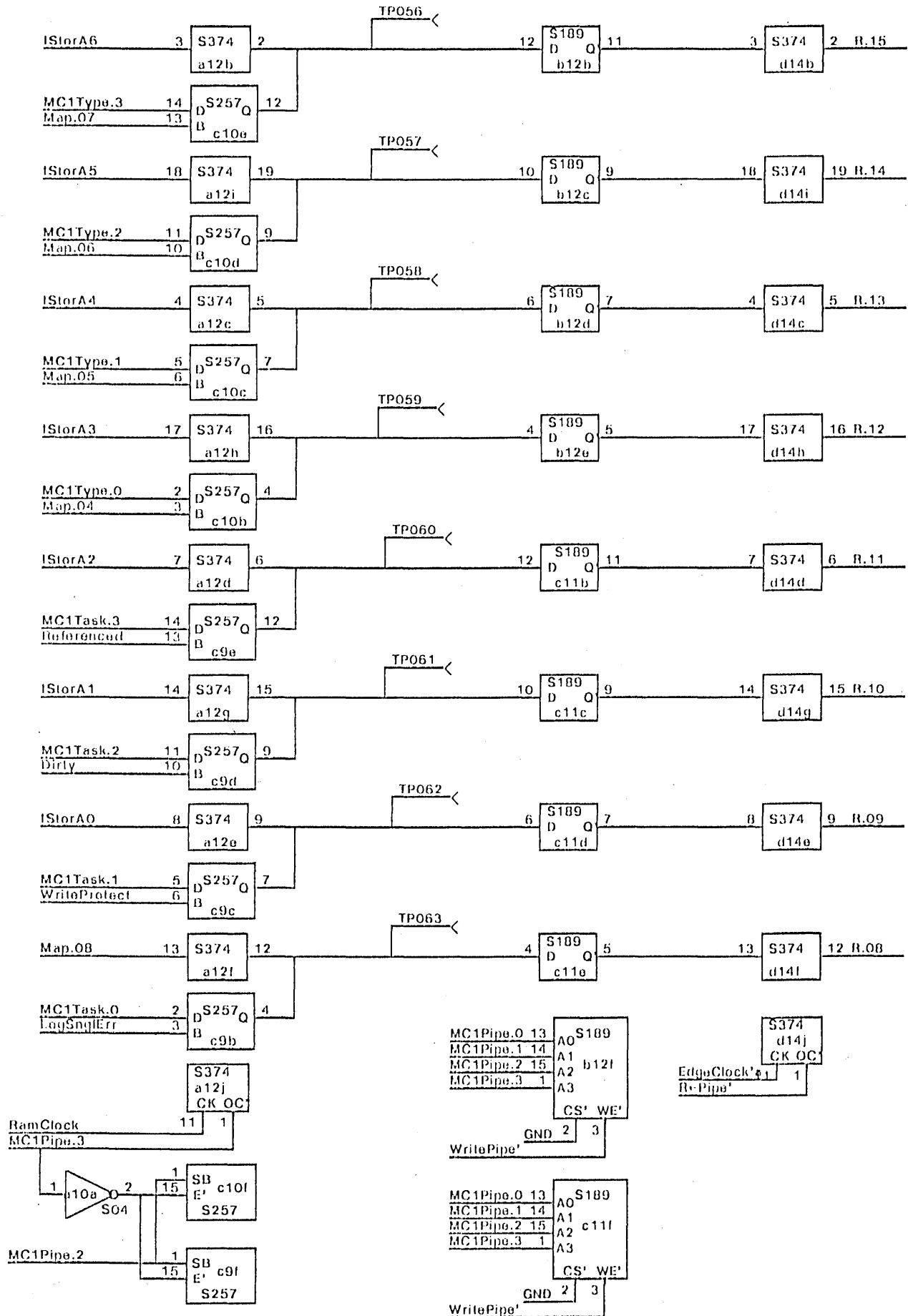






ALU Card supplies parity on OUTPUT

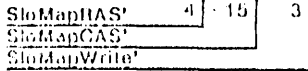




Dirty Bit

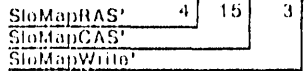
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	
SloMapA.3	12	A3	##%e5c
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



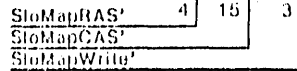
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	
SloMapA.3	12	A3	##%f6c
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



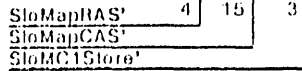
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%g8c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%g6c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

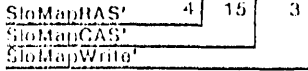
RAS' CAS' WE'



Ref Bit

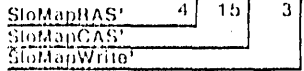
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%c8c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



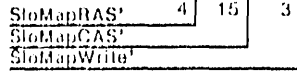
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%f5c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



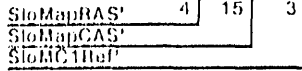
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%g7c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%g5c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

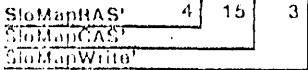
RAS' CAS' WE'



.1uF FICAPS, 16 pF

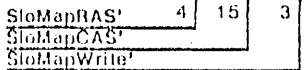
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%d7c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



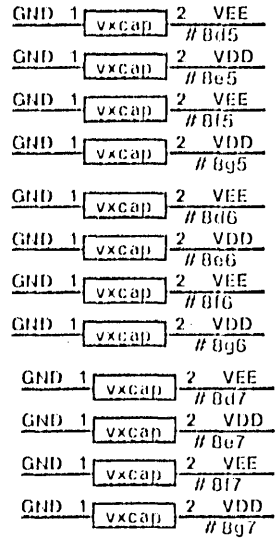
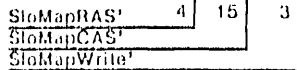
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%e8c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



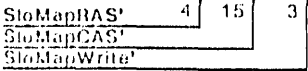
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%f8c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



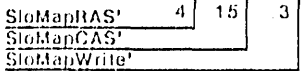
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%d6c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



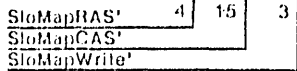
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%e7c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



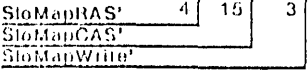
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%f7c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



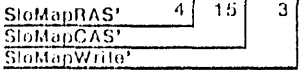
SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%d5c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'

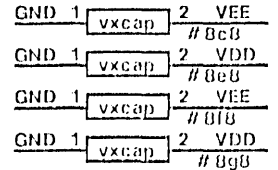


SloMapA.0	5	A0	MK4116-2
SloMapA.1	7	A1	
SloMapA.2	6	A2	##%e6c
SloMapA.3	12	A3	
SloMapA.4	11	A4	
SloMapA.5	10	A5	
SloMapA.6	13	A6	

RAS' CAS' WE'



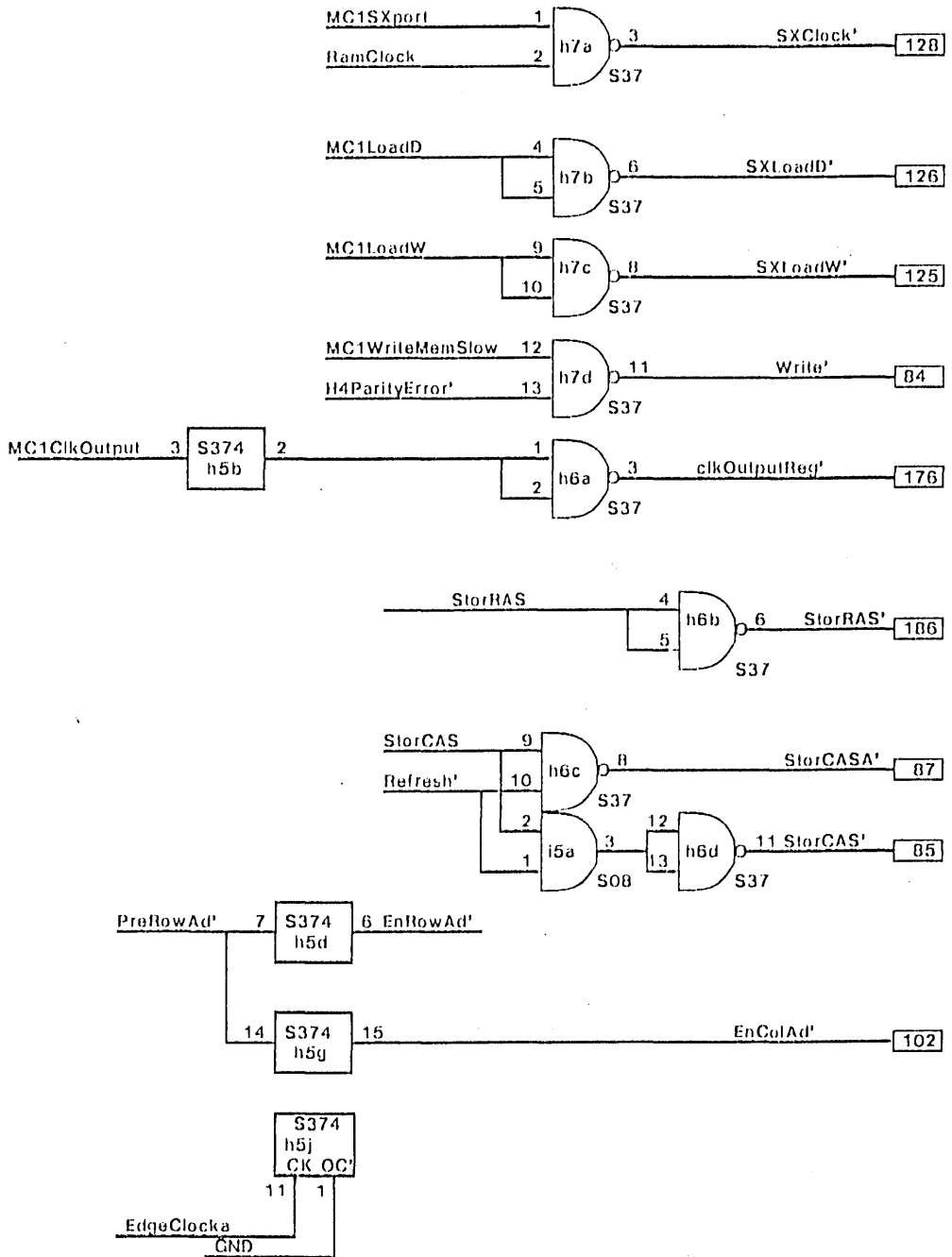
DisableMC2	1	P1	P20	FPLAT	20	VCC
DisableMC1	3	P2	P19	19	Disablee2	
Disablef14	4	P3	P18	18	Disableb9	
	5	P4	P17	17	Disablef7	
	6	P5	P16	16	Disableh2	
GND	7	P6	P15	15		
MC1Rel'	8	P7	P14	14	StoMC1Rel'	
GND	9	P8	P13	13		
MC1Store'	10	P9	P12	12	StoMC1Store'	
		P10	P11	11		

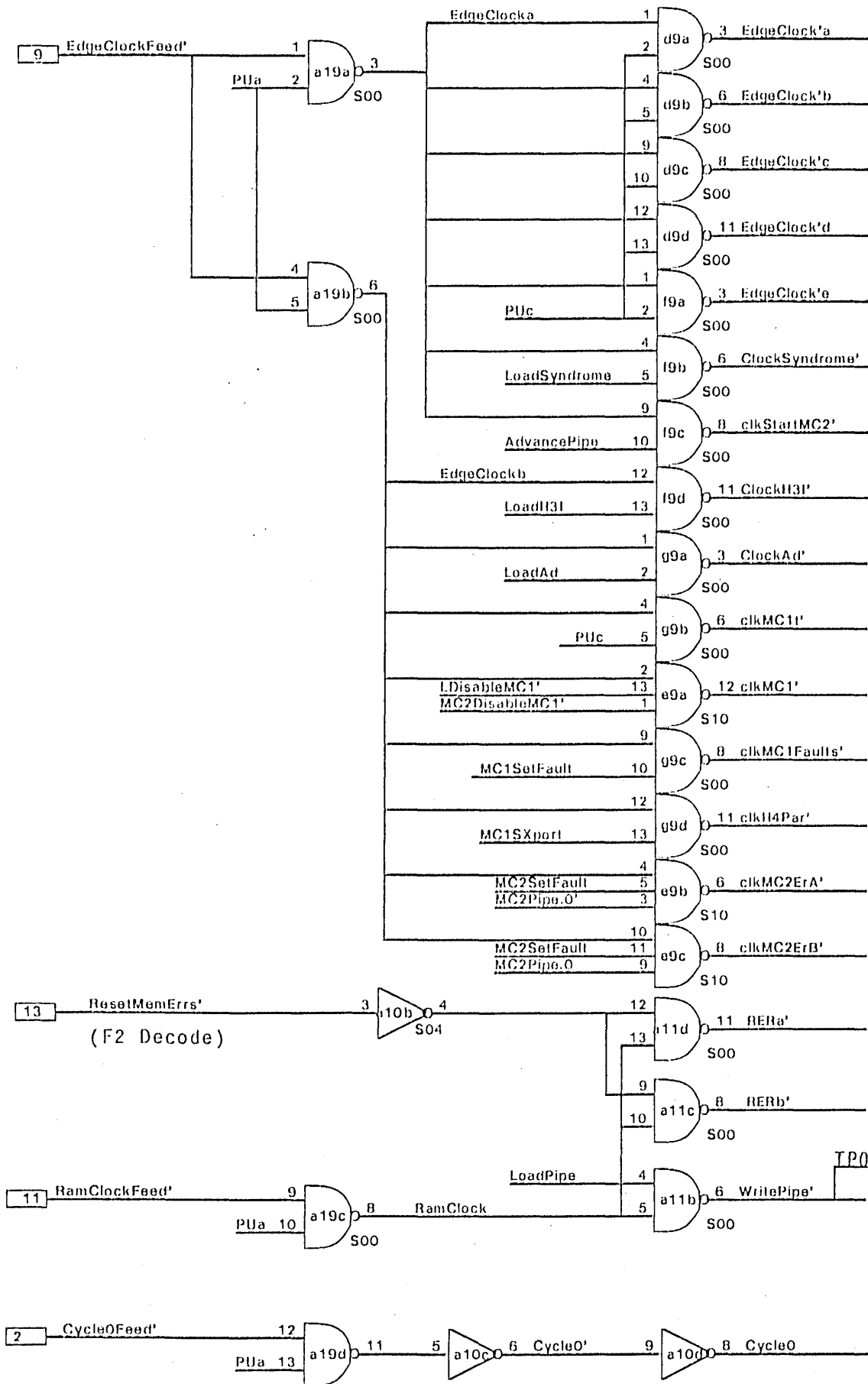


MapRAS'	1	P1	P20	FPLAT	20	VCC
MapCAS'	2	P2	P19	19	StoMapRAS'	
MapWrite'	3	P3	P18	18	StoMapCAS'	
VCC	4	P4	P17	17	StoMapWrite'	
	5	P5	P16	16	GenSyn0	
	6	P6	P15	15	GenSyn1	
	7	P7	P14	14	GenSyn2	
	8	P8	P13	13	GenSyn3	
	9	P9	P12	12	GenSynX	
GND	10	P10	P11	11		

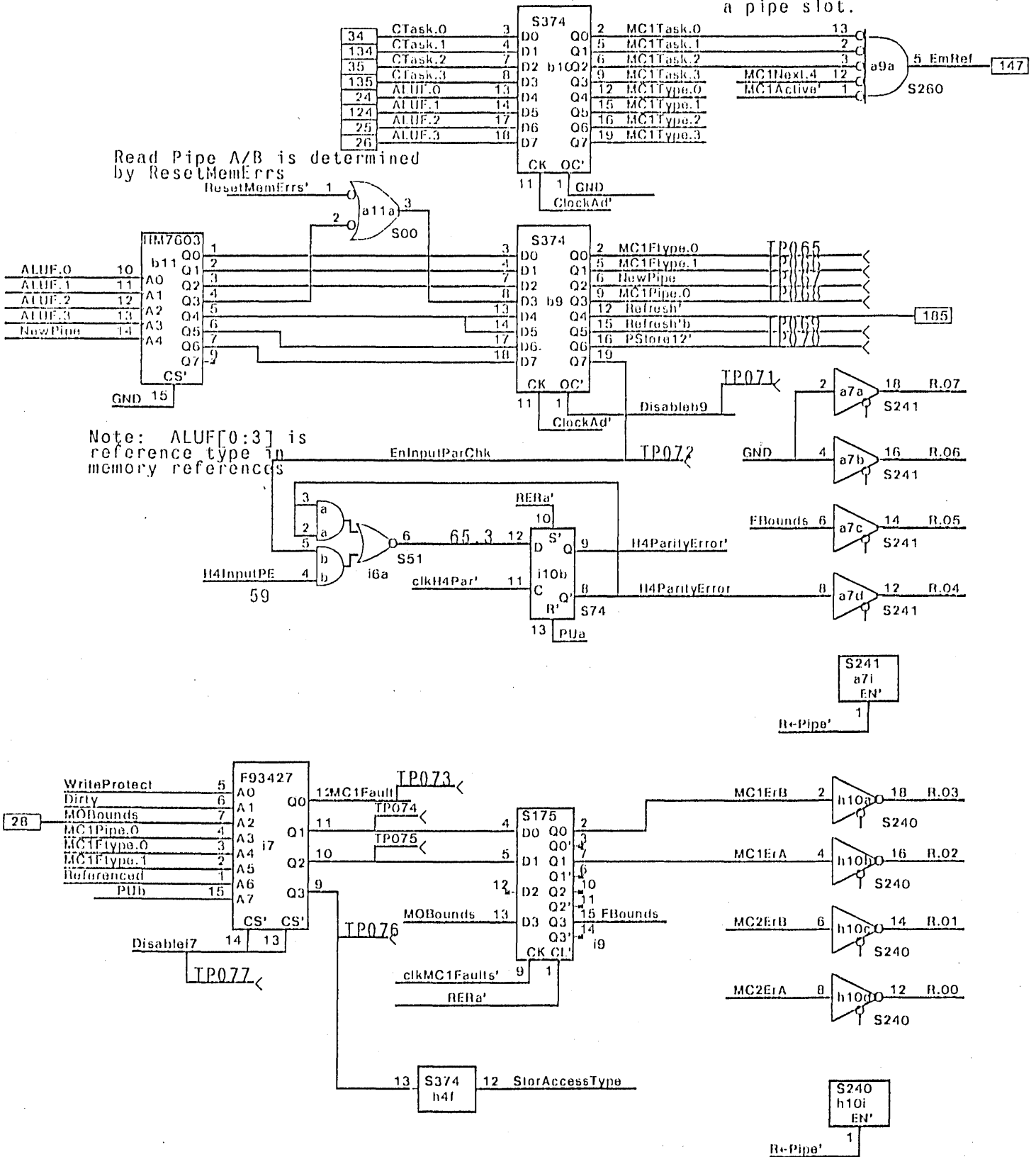
SloMapA.0	2	P1	P20	FPLAT	20	VCC
SloMapA.1	3	P2	P19	19	IStorA0	
SloMapA.2	4	P3	P18	18	IStorA1	
SloMapA.3	5	P4	P17	17	IStorA2	
SloMapA.4	6	P5	P16	16	IStorA3	
SloMapA.5	7	P6	P15	15	IStorA4	
SloMapA.6	8	P7	P14	14	IStorA5	
MC1WriteMem	9	P8	P13	13	IStorA6	
GND	10	P9	P12	12	MC1WriteMemSlow	
		P10	P11	11		

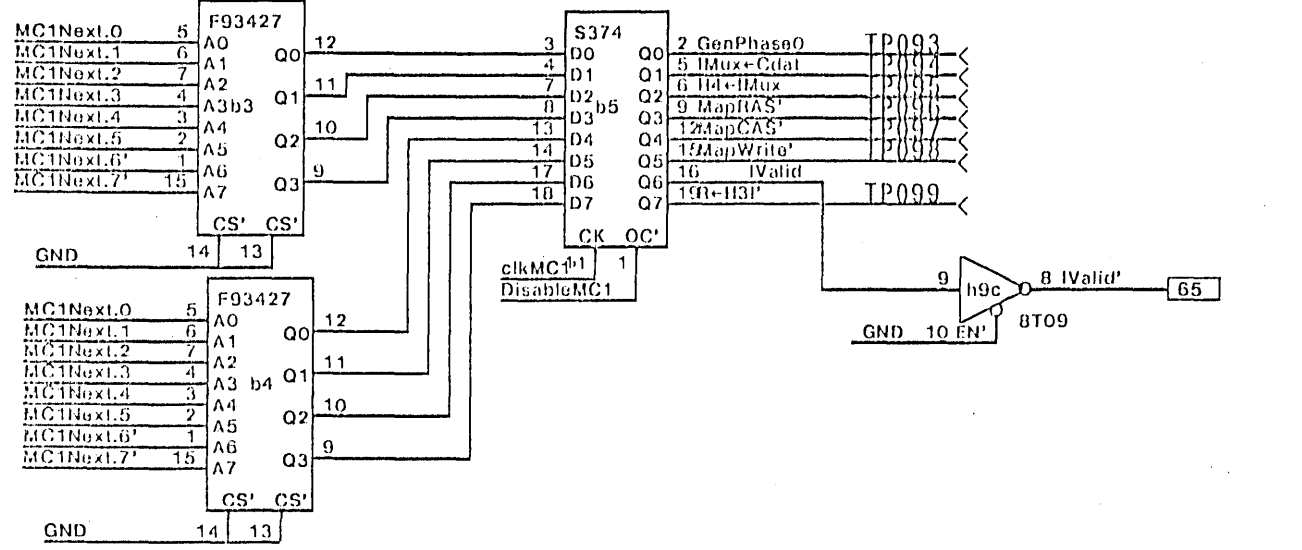
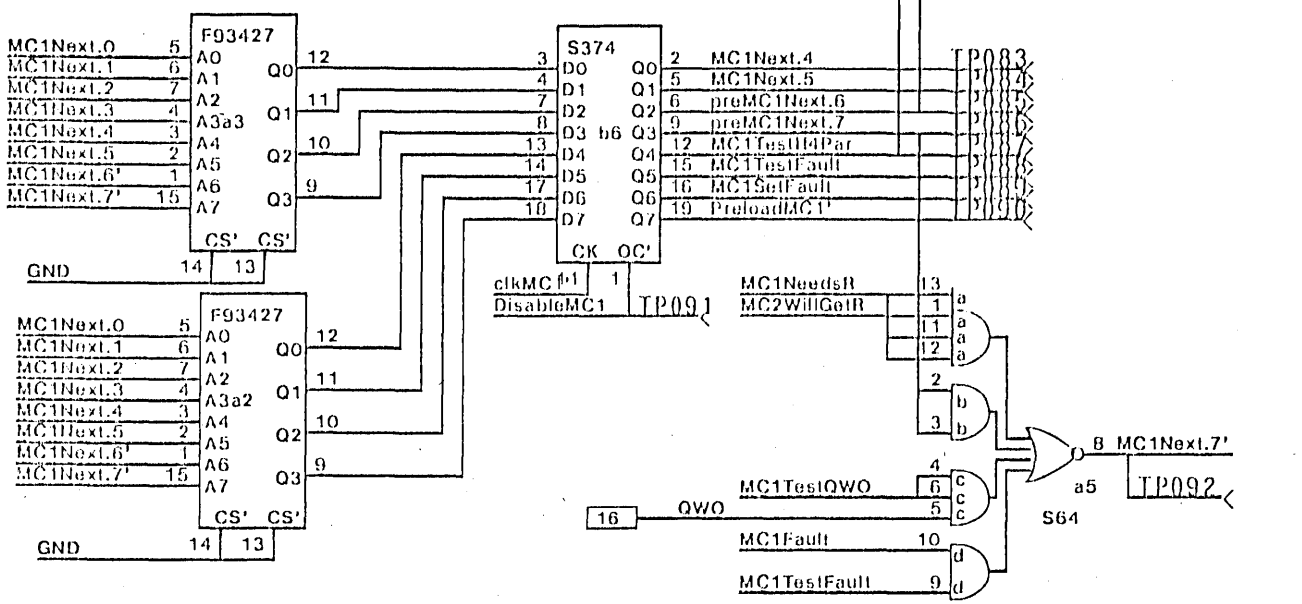
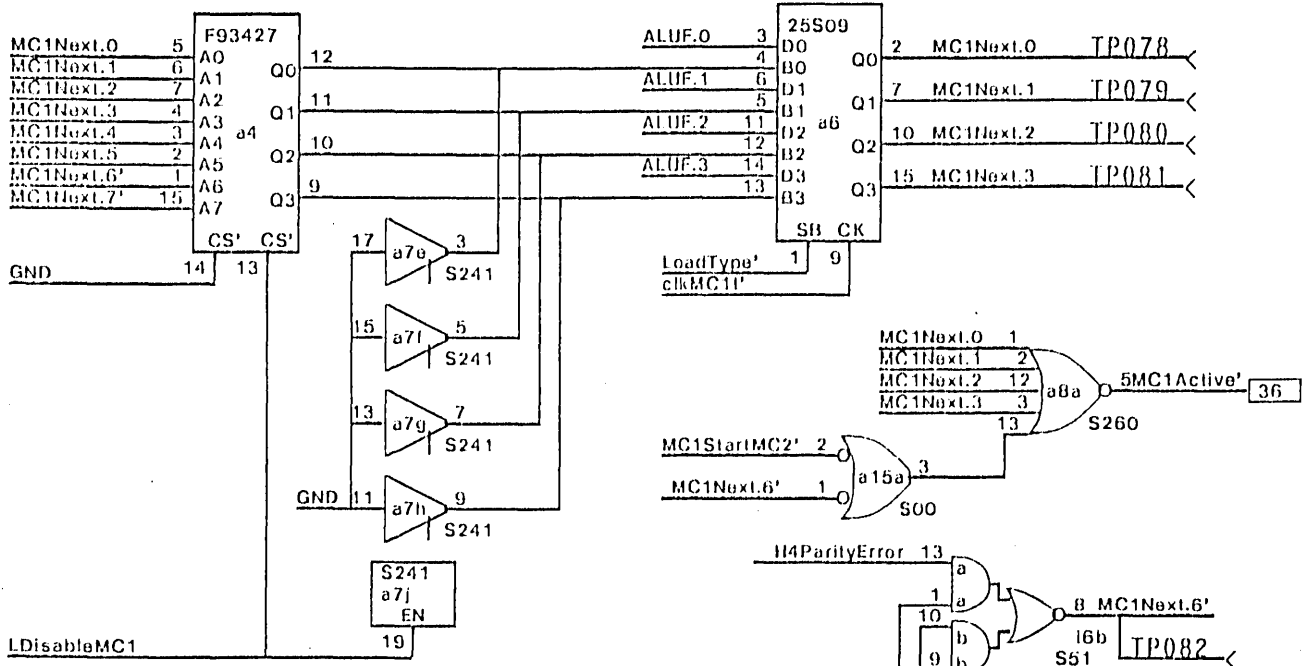
Filter cap. near receiver (GND 1 vxcap 2 MC1WriteMemSlow #Bh7)



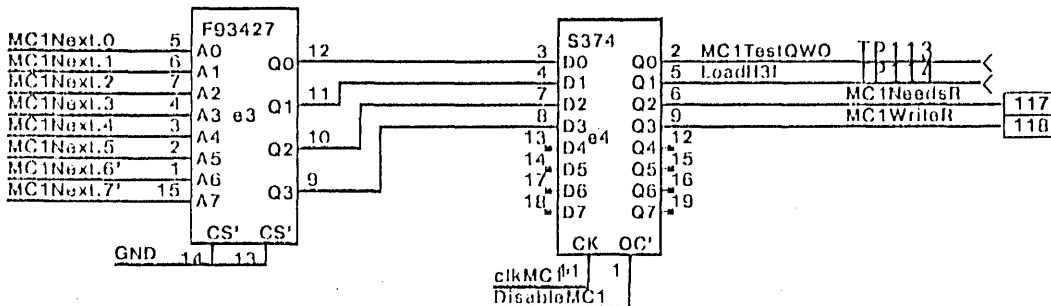
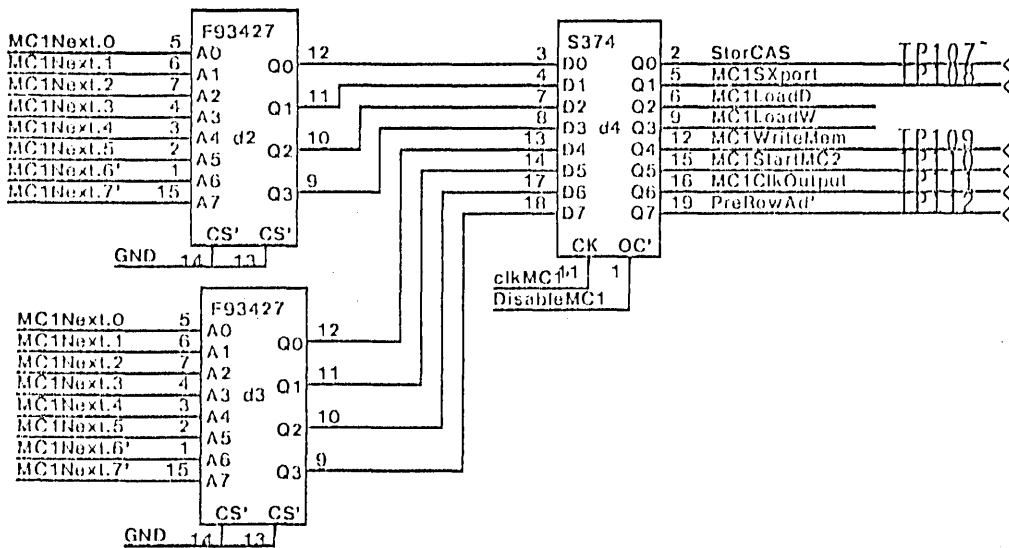
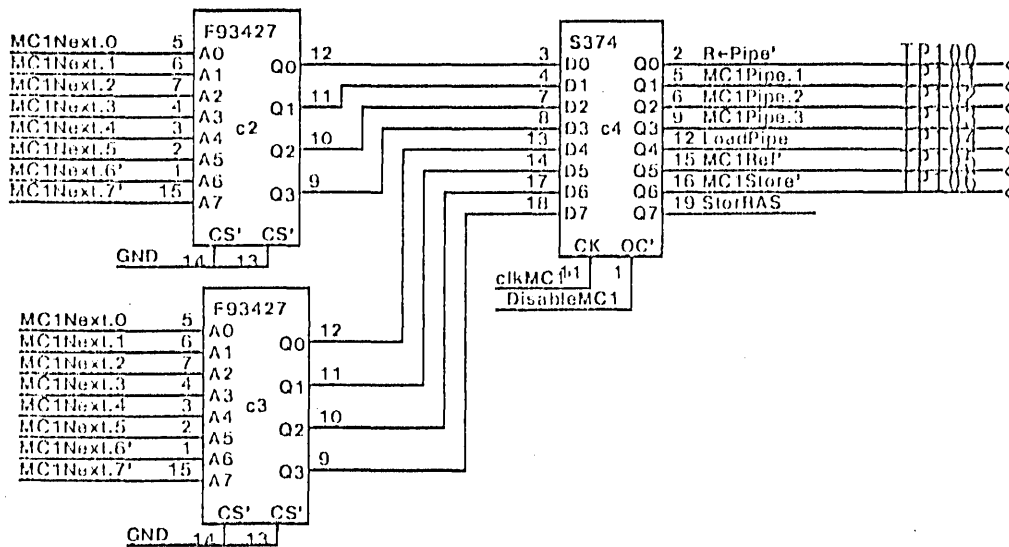


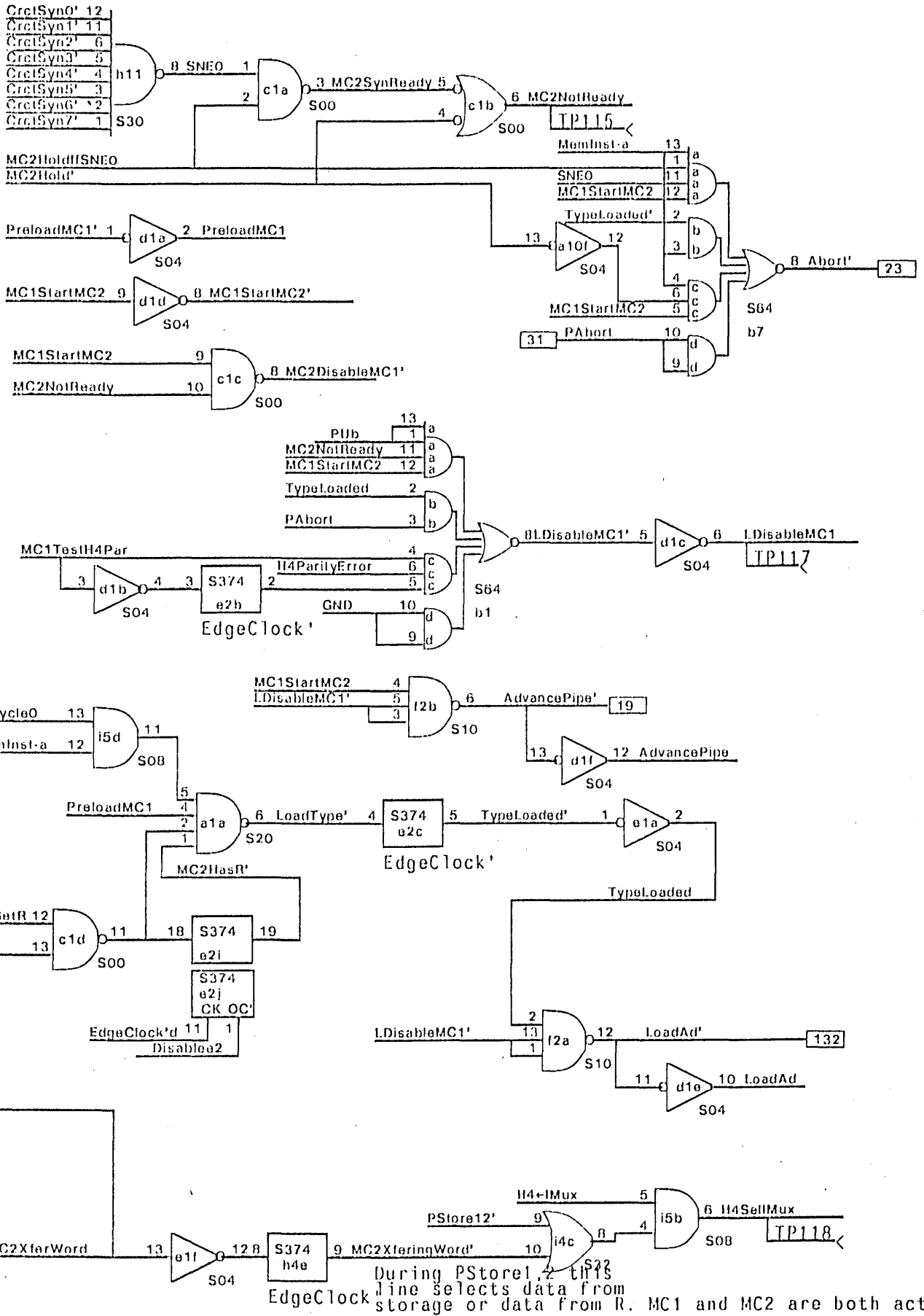
Ftype classifies references according to the types of faults they can cause: Non-memory/Fetch/Store  
 References are also classified as to whether or not they use a pipe slot.



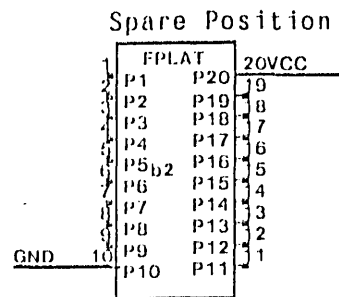
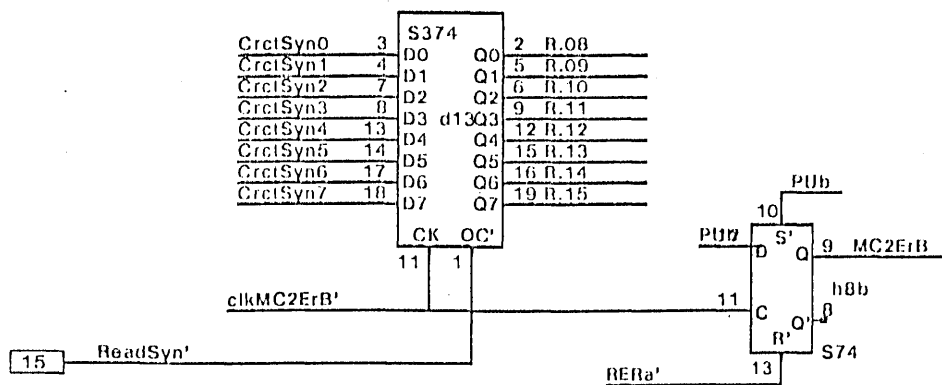
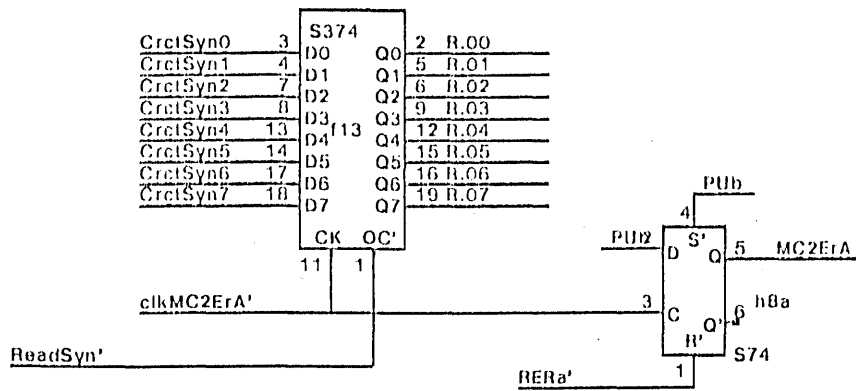
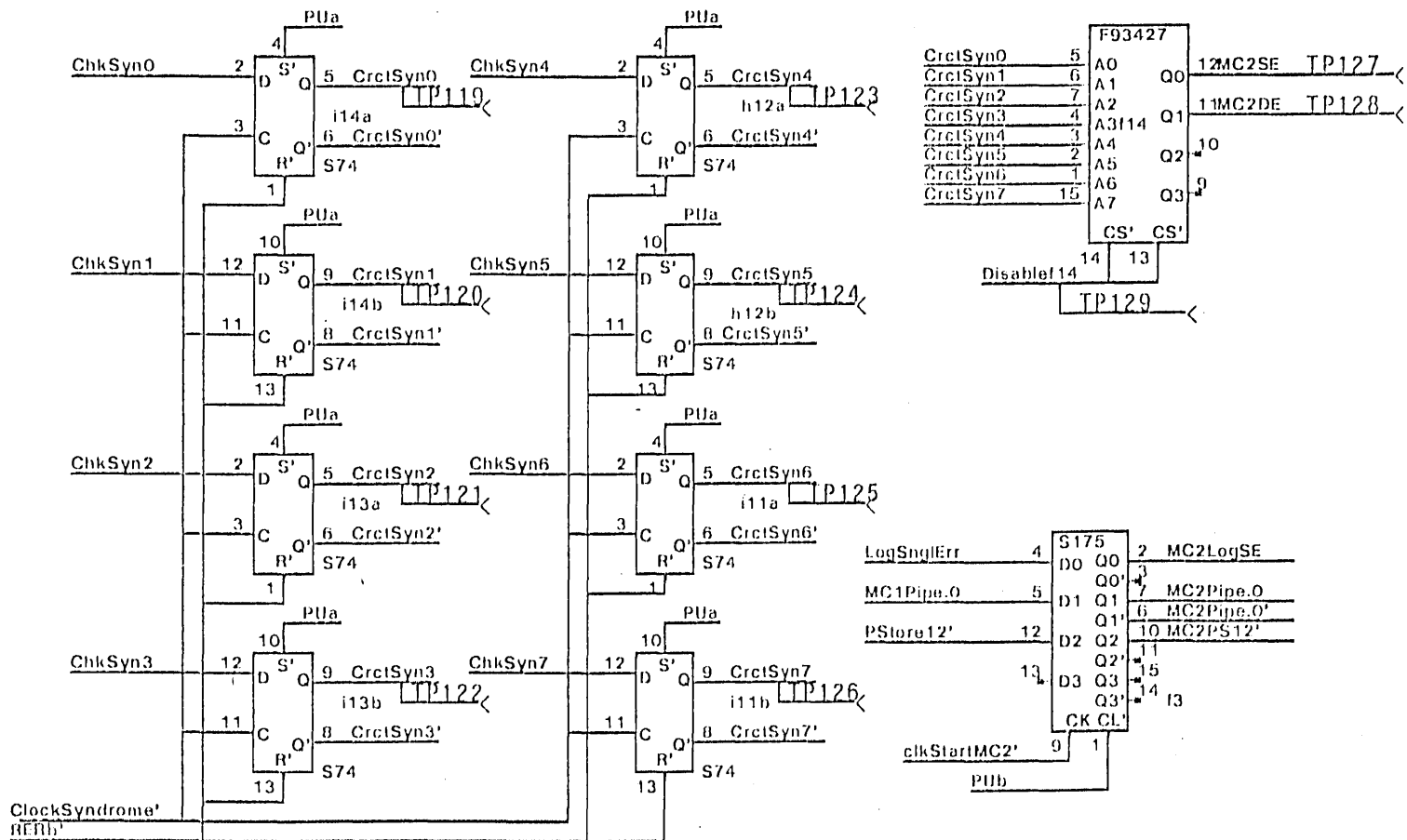


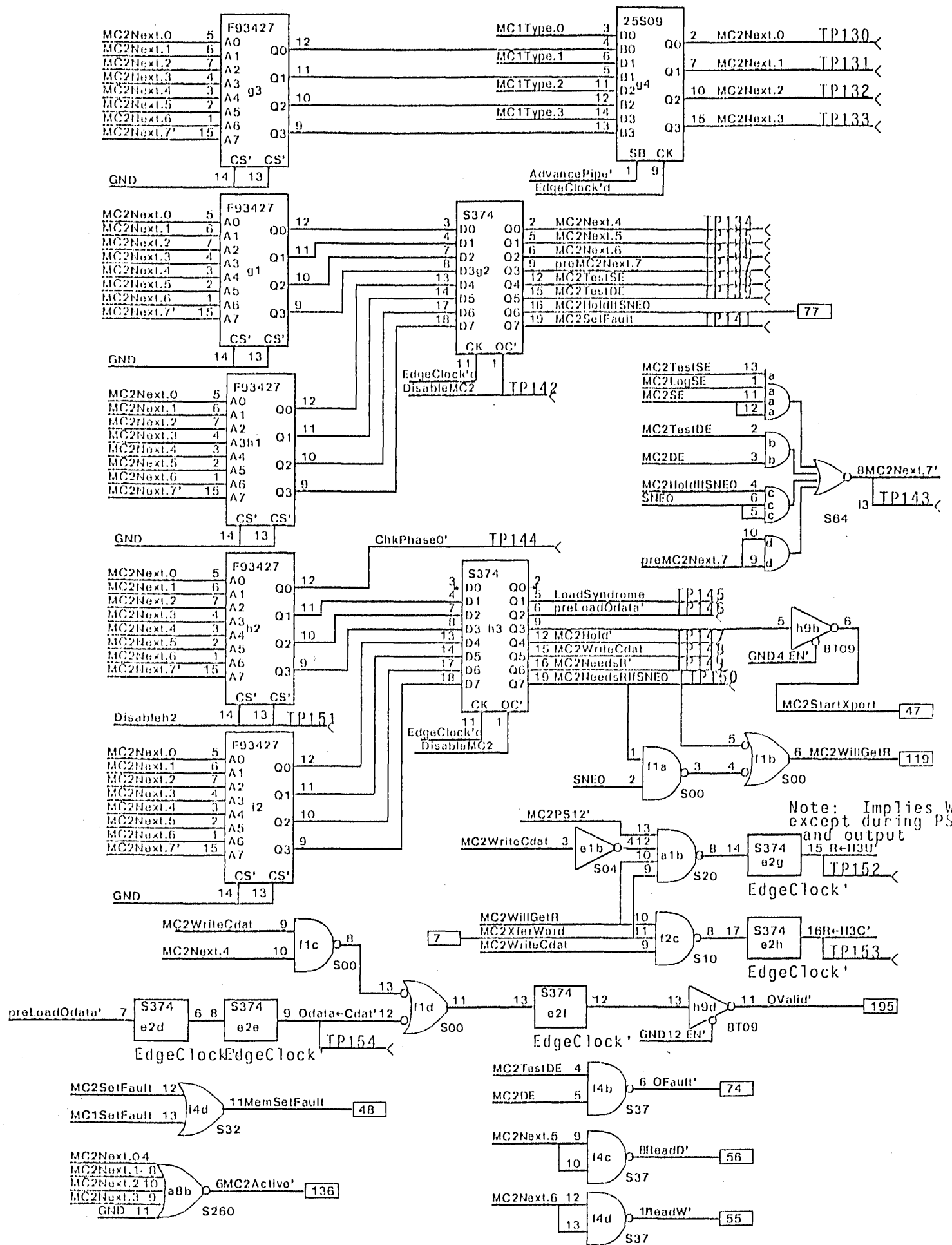


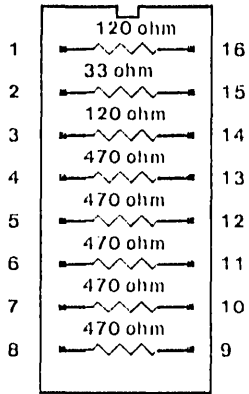




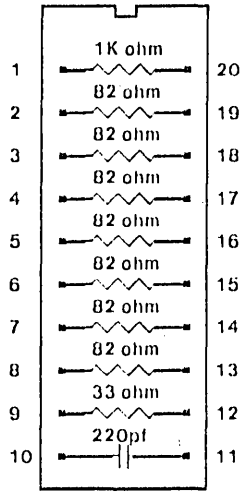
During PStore12, the  
 EdgeClock line selects data from  
 storage or data from R. MC1 and MC2 are both active.



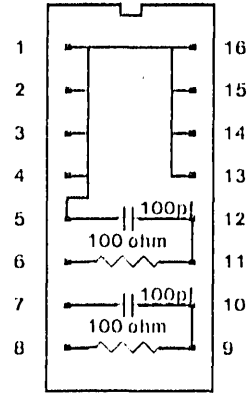




Position c5



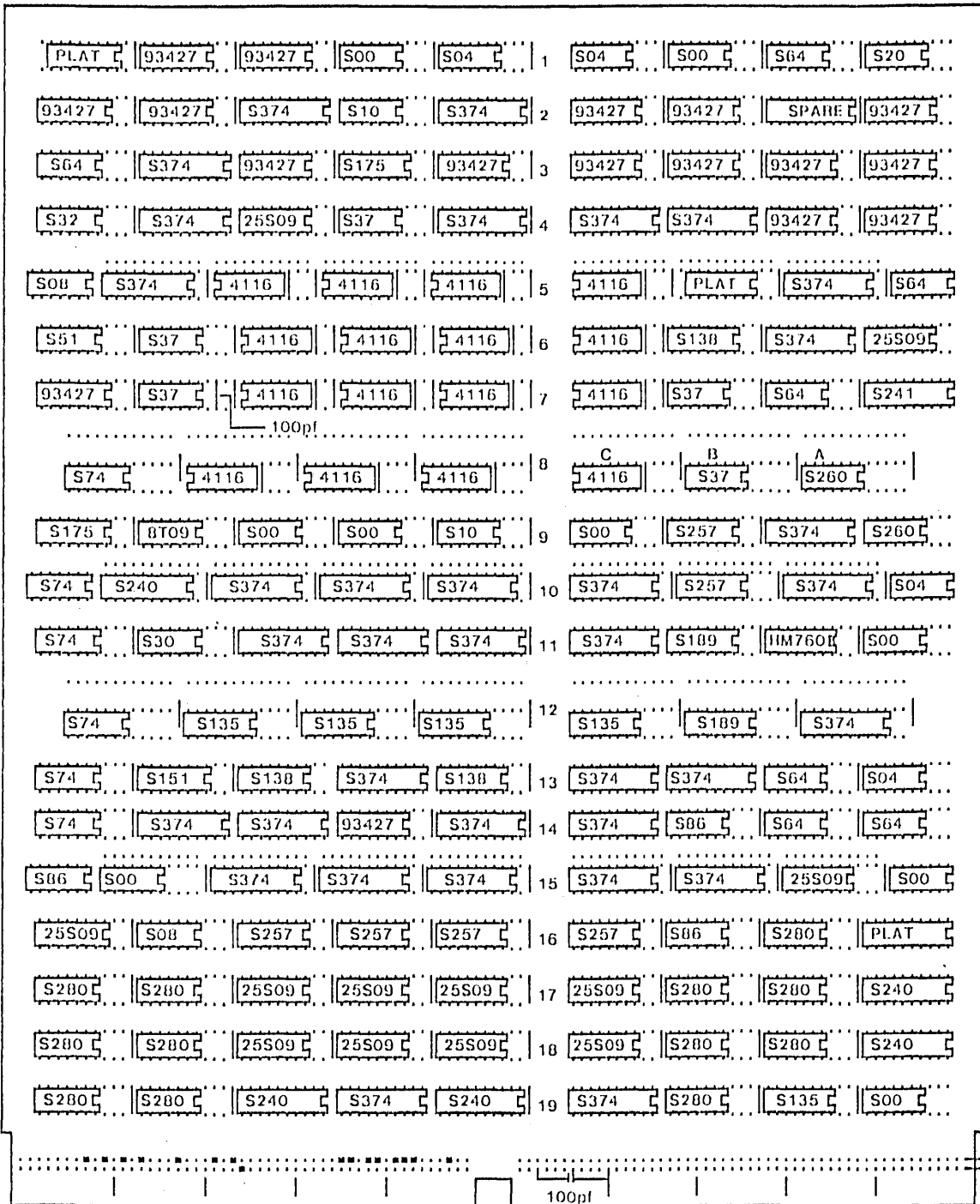
Position a16



Position i1

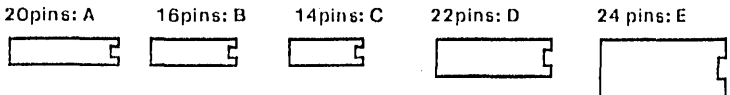
XEROX E0D	Project D0	Memory Control PLATFORMS	File D0MemPLATFORMS.sil	Designer Thacker	Rev Gb	Date 7/18/80
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I H G F E D C B A



101-200  
1-100

Note: Pinx marked with ■ have 470ohm pullup resistors to +5v.



Note: The short vertical lines indicate filler capacitor locations.

(143 Places)

16pins REVERSED!!!  
typical of MK4116: F



Changes from Rev E to Rev F:

- 1) Added the signal Disableh2 (pg 20,12) for test
- 2) Removed 'H4ParityError' from the term that forms Abort' (gate at a15 now free, inverter at e1a moved).  
Note: This change deletes IC a15.

Changes from Rev F to Rev G:

- 1) b11.15 (pg 1) ← GenX, not GenX' (this was wrong in .nl file, ok on dwg.)
- 2) h13.9 ← CrctSyn4, h13.11 ← CrctSyn6 (pg. 3)

Changes from Rev G to Rev H:

- 1) (pg 13) Change c1.13 from RamClock to EdgeClocka
- 2) (pg 13,15) Changed i9 from S74 to S175. Relocated i9's functions to i10. Added MOBounds as R.05 during R+Pipe operation.
- 3) (pg 16) Deleted S04 at a10b. Replaced with S00 a15a, and added MC1StartMC2' as input to MC1Active.
- 4) Added MC2PS12' by replacing i3 (S74) with S175 (pg 19). MC1PS12' is used instead of PStore12' at a1.13 (pg 20).

Changes from Rev H to Rev I (5/9/78)

- 1) (pg 20) h3.9 was MC2HoldHSNEO, is now MC2StartXport' after passing through the 8T09 at h9b (used as a driver).
- 2) Renamed signal MC2TestSNEO to MC2HoldHSNEO (essentially, these two signals have been coalesced into one).
- 3) Added test points.
- 4) Added comments on Vee bypass and -10V supply changes to D0memplatforms.sil

Changes from Rev I to Rev J (8/12/78 - C. Thacker)

- 1) Renamed signal TP055 GateALUParity, and connected it to E079 (pg 10)
- 2) Latched signal StorAccessType in S374 at h4f (pg 15)
- 3) Removed MC2XferWord and MC1XferWord from a5.11 and a5.12. Connected a5.11 and a5.12 to a5.13 (pg 16). Note that signal MC1XferWord is no longer used on this card, so E006 is free.
- 4) Removed -10V supply components on D0memplatforms.sil

Changes from Rev J to Rev K (10/8/78 - C. Thacker)

- 1) Changed h7.12 from MC1WriteMem to MC1WriteMemSlow (pg13). This signal is generated at platform a16 (pg12).
- 2) Changed platform a16 to 20pins to make room for MC1WriteMemSlow (pg12).
- 3) Added capacitors on SloMapRAS' and SloMapWrite' (platform c5, page 12).
- 4) Changed a9.12 from MC1Task.3 to MC1Next.4 (pg15).
- 5) Changed i7.1 from PUB to Referenced (pg15). This requires changing PROM i7 to revision E.

Changes from Rev K to Rev L (11/1/78 - C. Thacker)

- 1) Signal clkOutputReg is now clkOutputReg' by removing S37 at h6a (now free) page 13.
  - 2) b10.1 (pg15) was Disableb10, is now GND. Also removed Disableb10 from SPLAT i1 (pg 12).
- There are no prom changes in this revision.

Changes from Rev L to Rev M (12/9/78 - C. Thacker)

- 1) Changed platforms c5 and i1 - removed capacitors and changed values.
  - 2) Changed the generation of clkOutputReg' (pg 13). This signal is now one cycle wide, rather than being a qualified EdgeClock.
  - 3) The input to h5g (pg 13) is PreRovAd', not EnRovAd'. This board requires an ALU board of rev M for proper operation.
- There are no prom changes in this revision.

Note: Rev M = Rev Ga

Changes from rev Ga to rev Gb (7/18/80 - CPT).

- 1) Added 16 FICAPS for MK4116 chips (VDD and VEE)
- 2) Added glitch suppression capacitor adjacent to h7 (on MC1WriteMemSlow - 100pf).
- 3) Changed interlock logic on page 18.

Current PROM Revisions:

a4, a3, a2, b3, b4, c2, c3, d2, d3, e3 (MC1 Sequencer): E  
g3, g1, h1, h2, i2 (MC2 Sequencer): D  
i7 (Fault): E  
b11 (Ftype, Pipe): D  
i14 (Single/Double errors)D

XEROX EOD	Project D0	Memory Control Changes	File d0memchanges.sil	Designer Thacker	Rev Gb	Date 7/18/80
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