

DICENTRA SCHEMATICS

Central Processor

Table of contents

<u>TITLE</u>	<u>PAGE</u>
Arithmetic Logic Units _____	1
ALU Carry & Shift Ends _____	2
U Registers _____	3
RH & StackP Registers _____	4
Rotator & Constants _____	5
Instruction Buffer _____	6
Raw MIR _____	7
Decoded MIR _____	8
Branching & Link Register _____	9
Next Address Register _____	10
Prom Control Store _____	11
Traps & Interrupts _____	12
Multibus Control _____	13
Multibus Data & Address _____	14
Clocks & Debugger _____	15
Odds & Ends _____	16
Connectors _____	17
Bypass Capacitors _____	18
Interrupt PALs _____	19
Multibus Timing & States _____	20
Parts List _____	21
Fabrication Drawing _____	23
Assembly Drawing _____	24

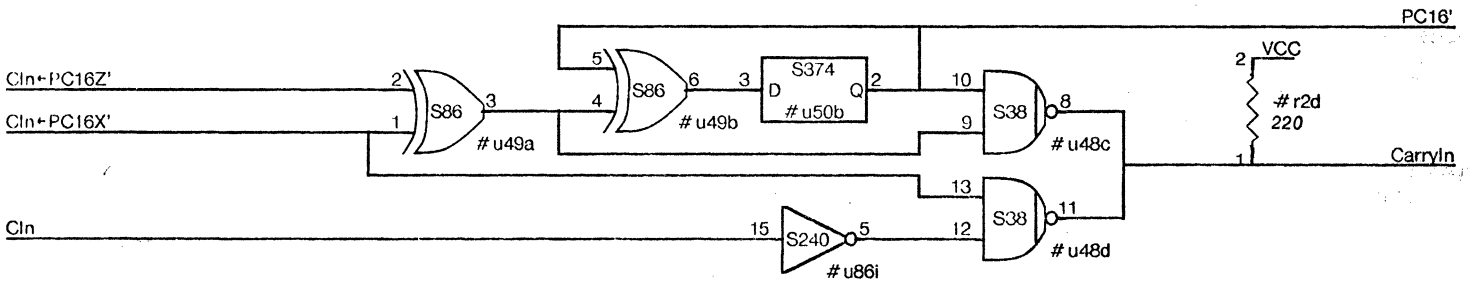
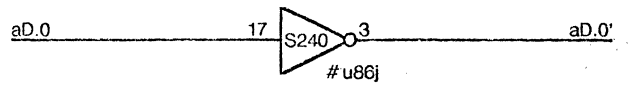
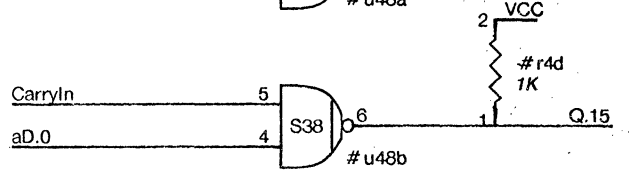
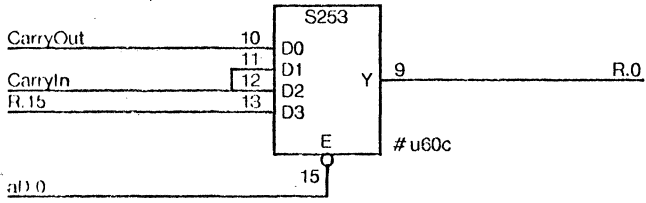
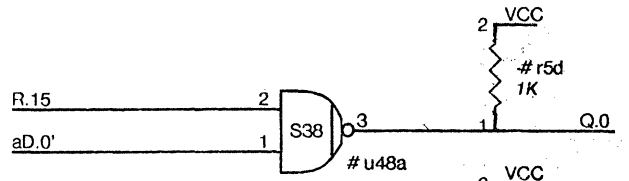
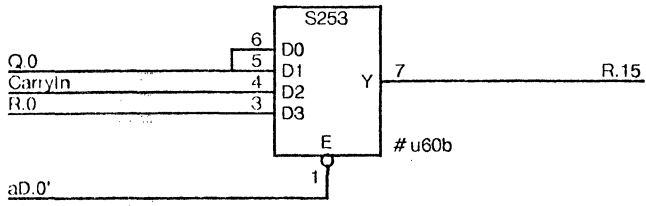
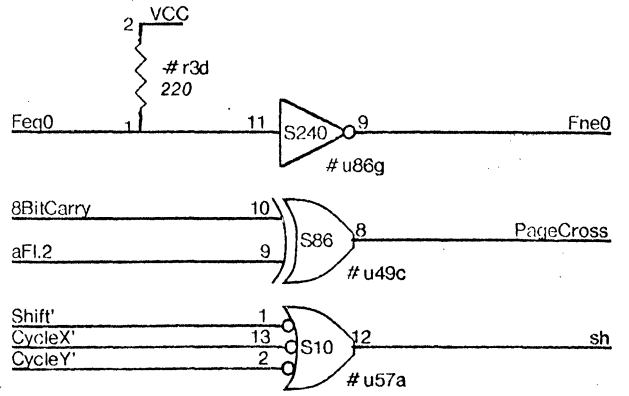
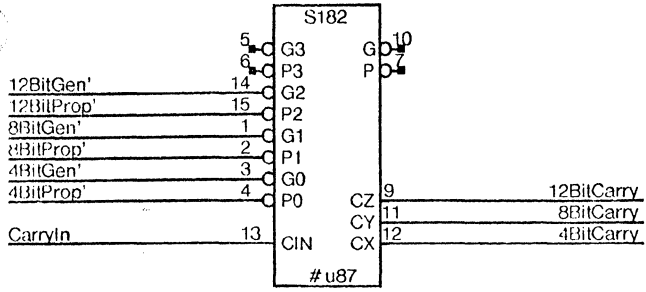
Butler Lampson designed this Mesa processor and named it WILDFLOWER.
 Robert Garner implemented a version for Star and named it DANDELION.
 David Boggs repackaged it minus tasking plus a Multibus and named it DICENTRA.

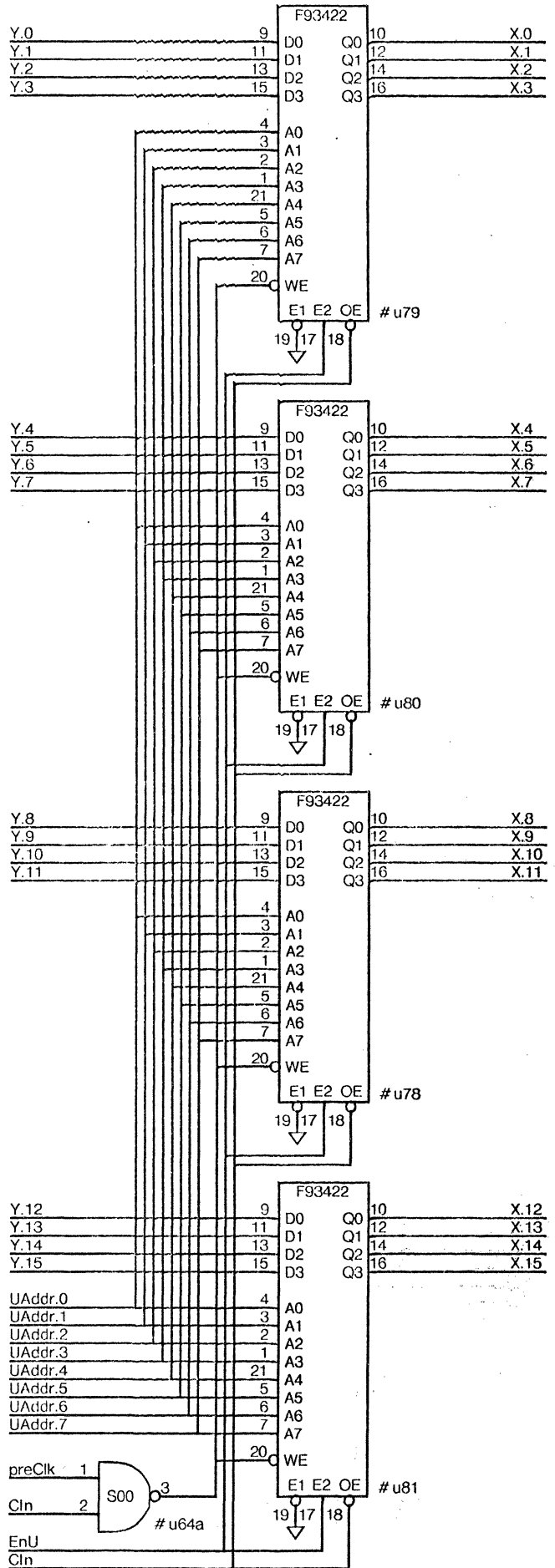
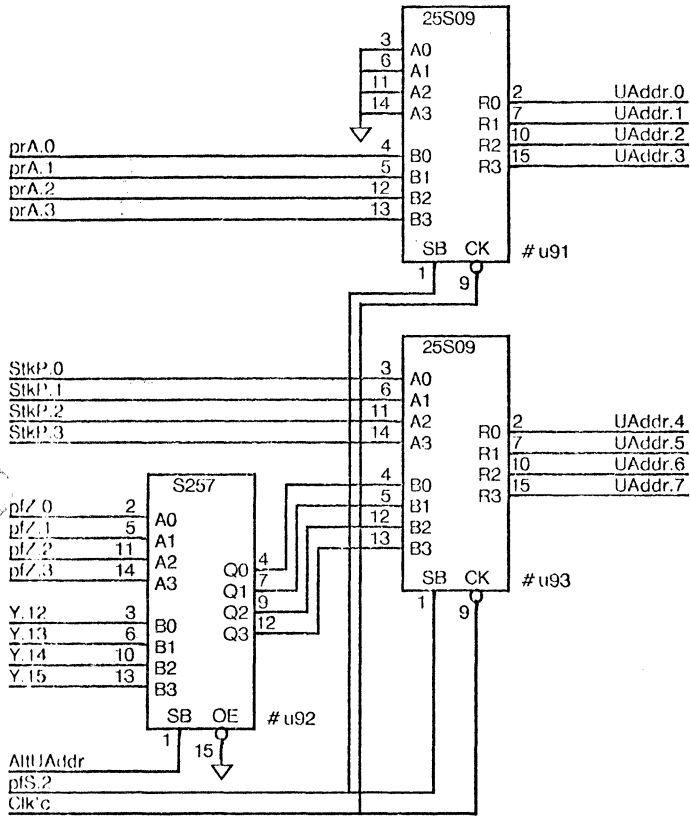
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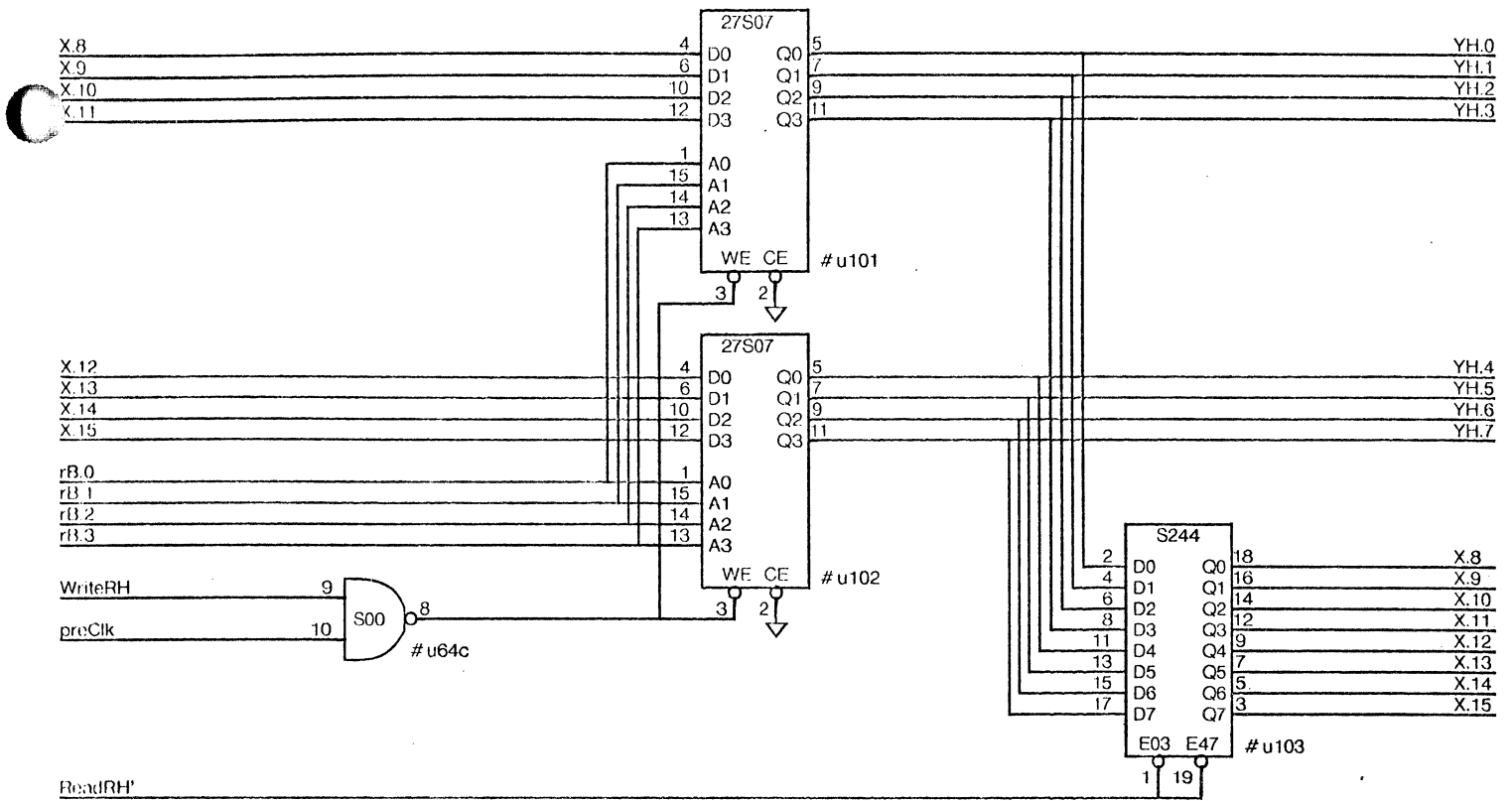
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 2: Template64
 3: Gates32
 5: Dicentra.lb5
 6: Dicentra.lb6
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 8: Dicentra.lb8
 A: Dicentra.Analyze
 Y: 712

All files are kept on [Indigo]<Dicentra>

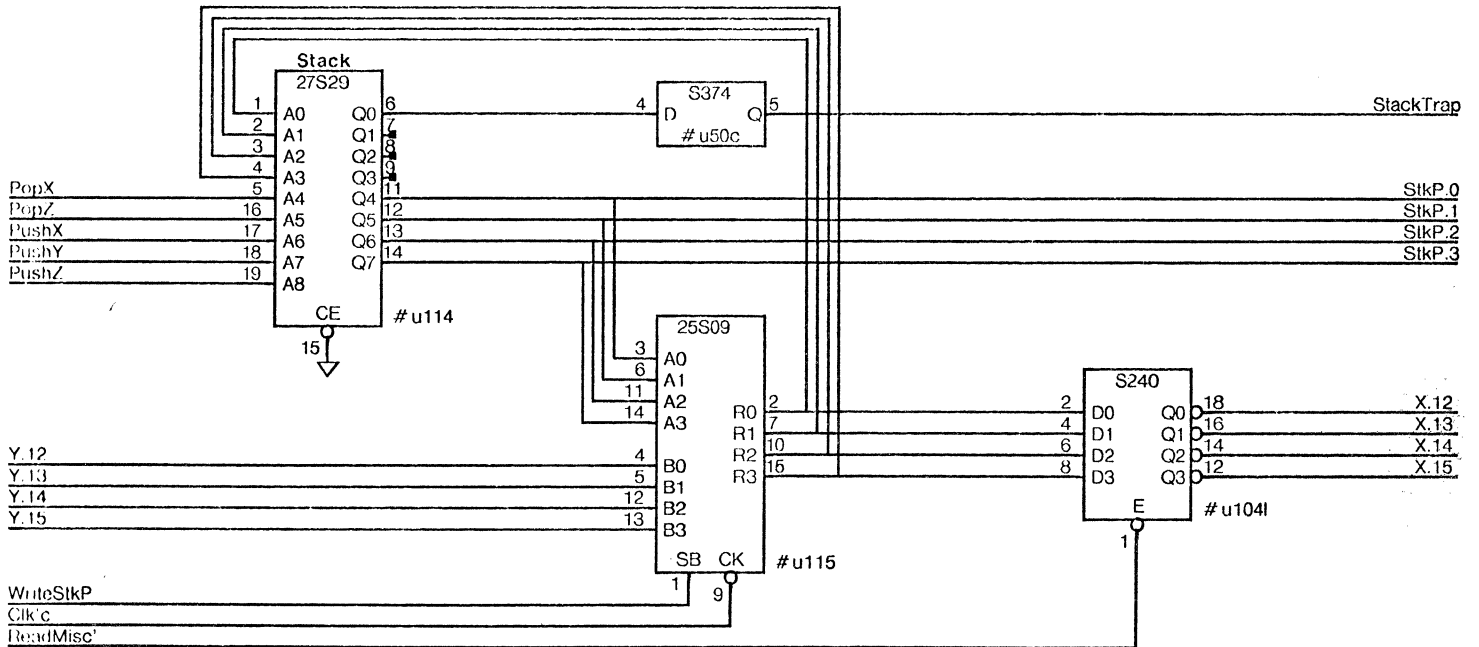
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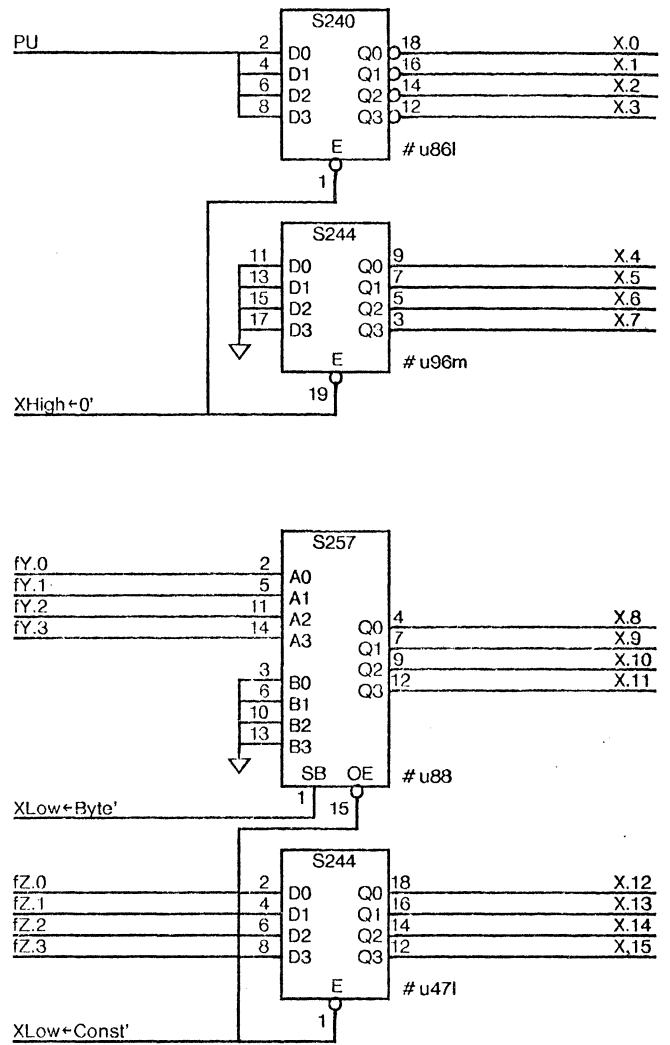
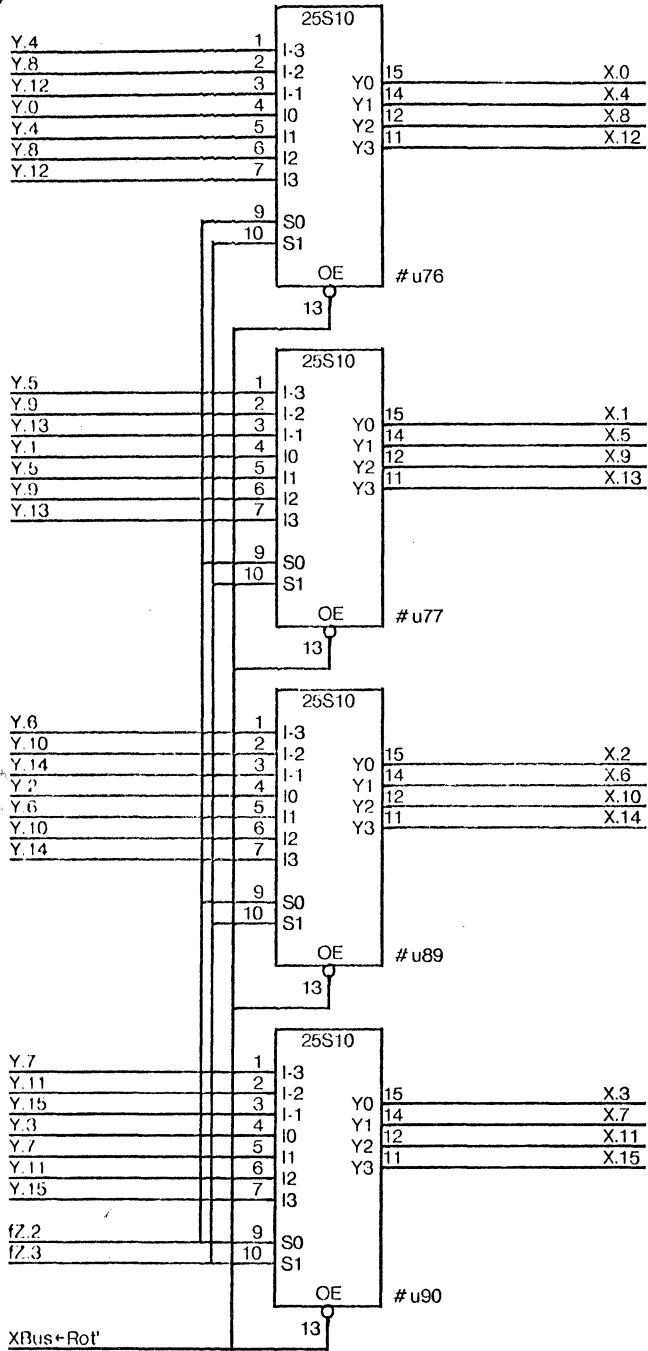


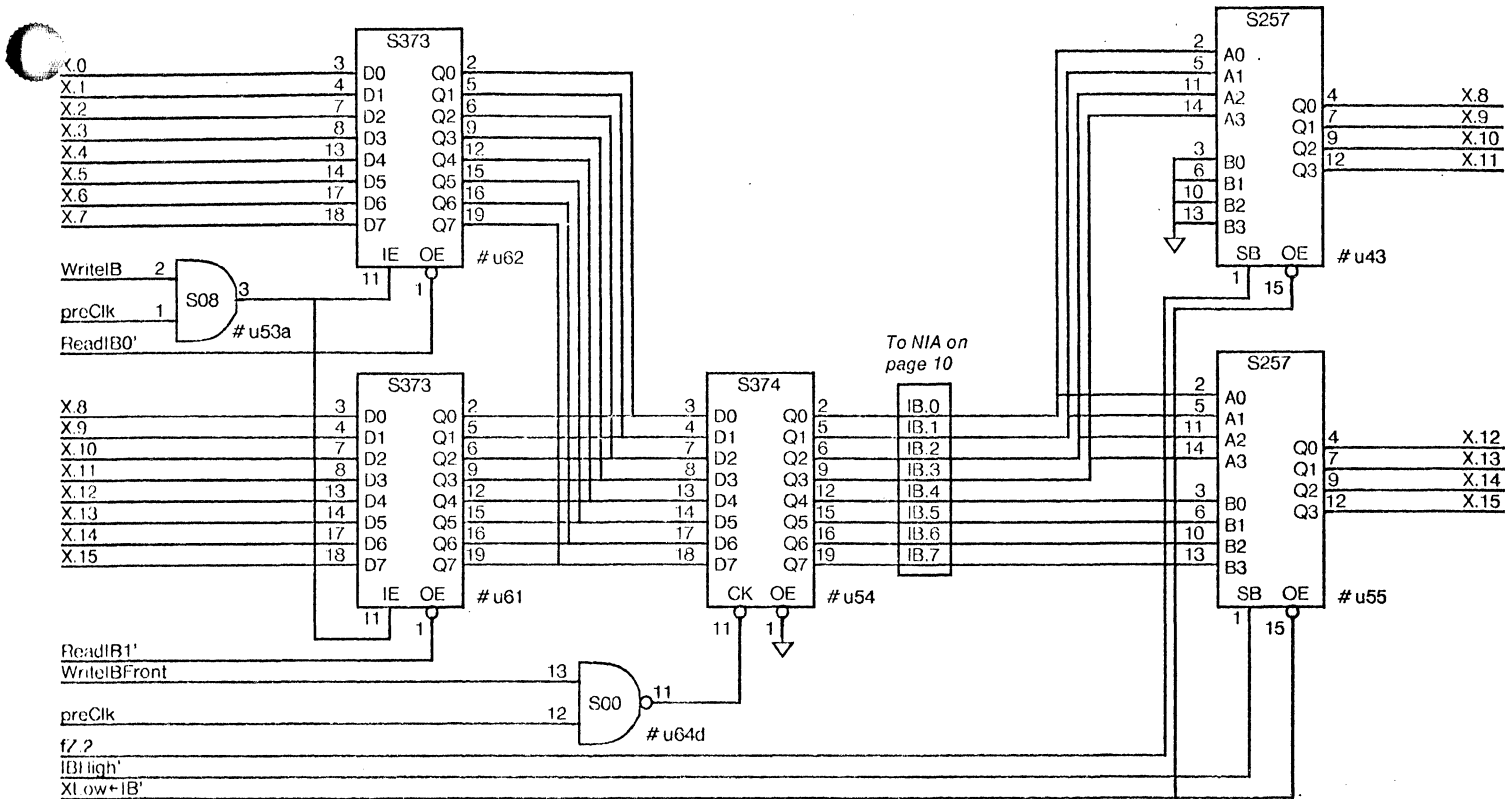




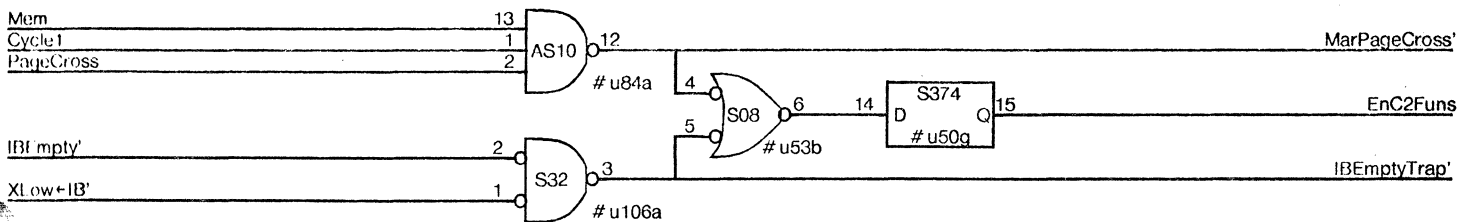
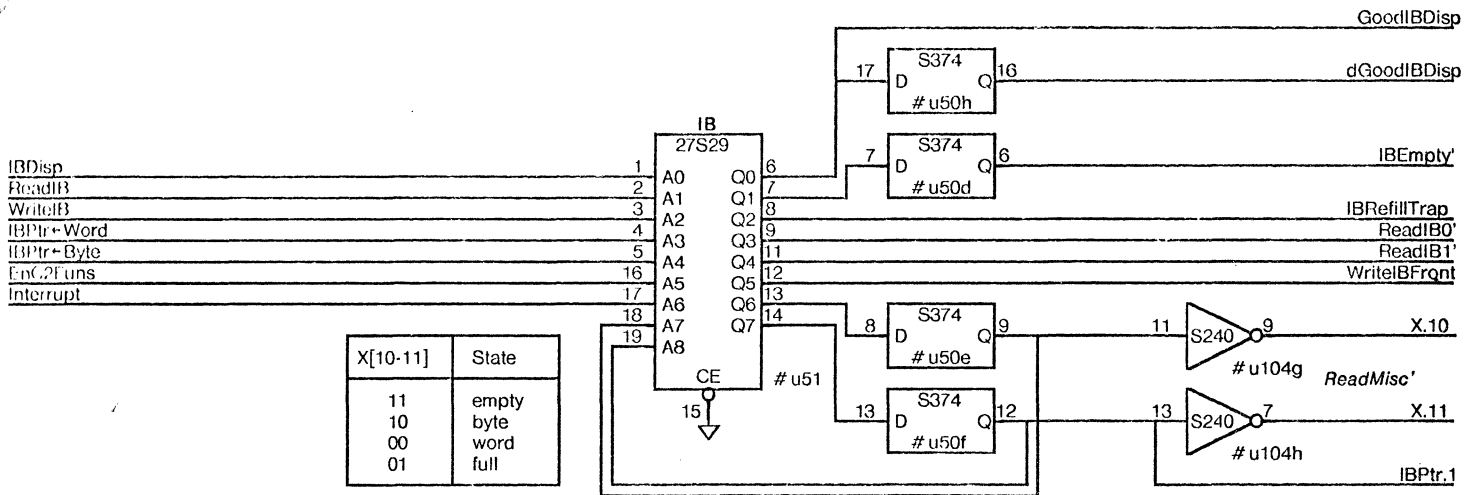
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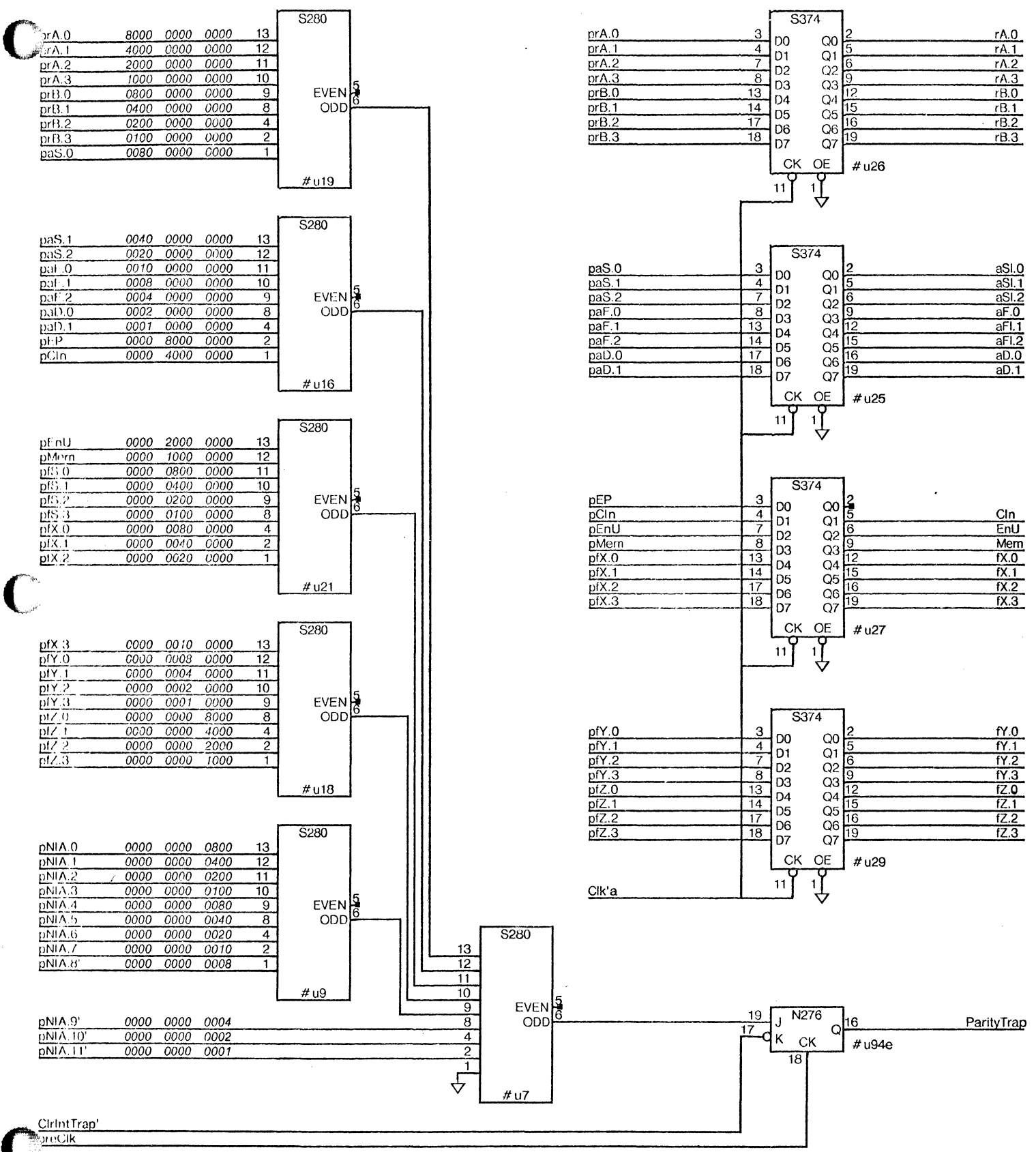


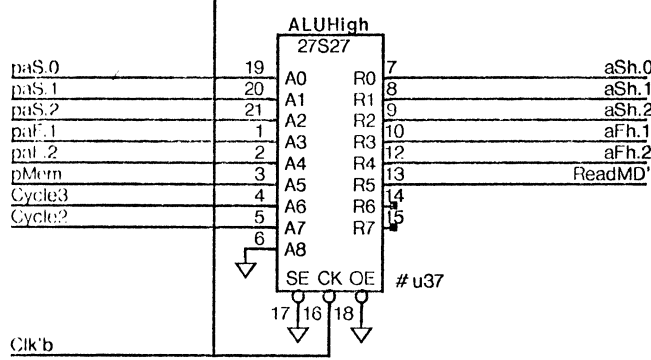
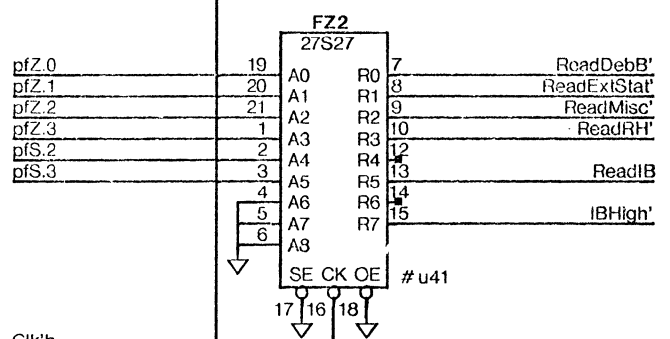
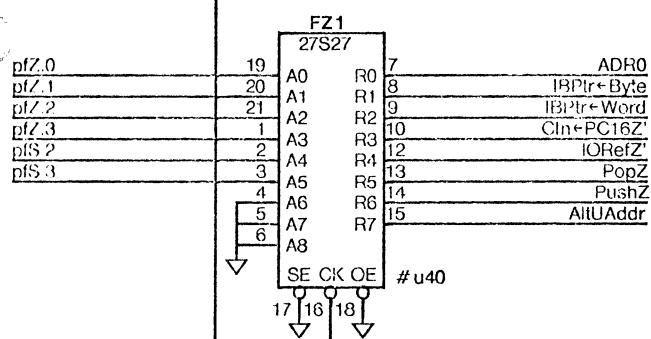
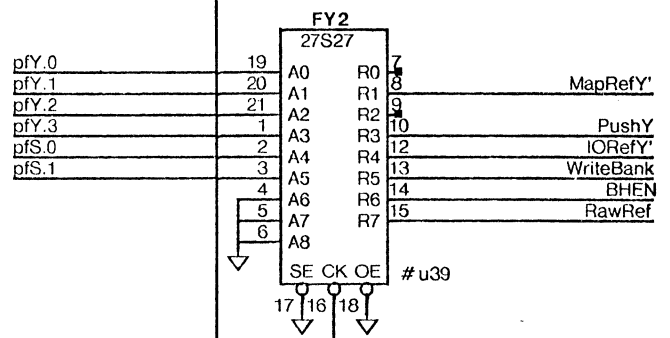
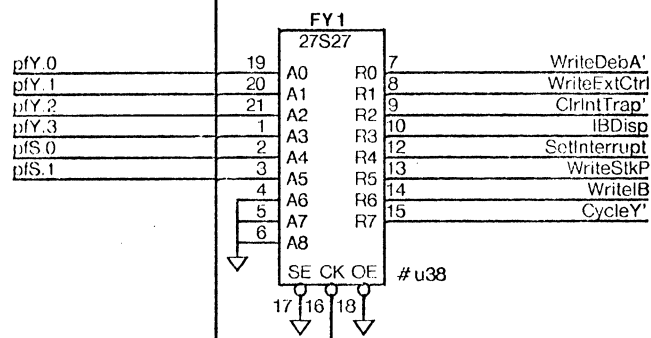
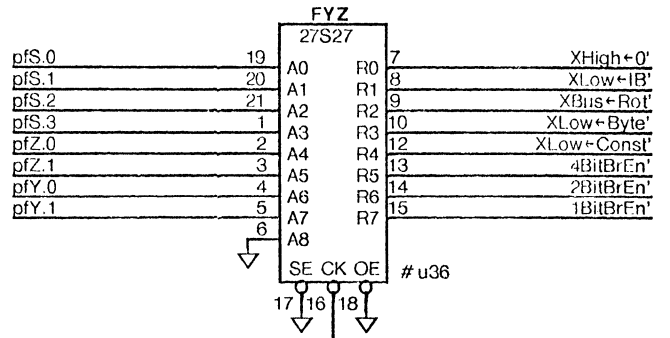
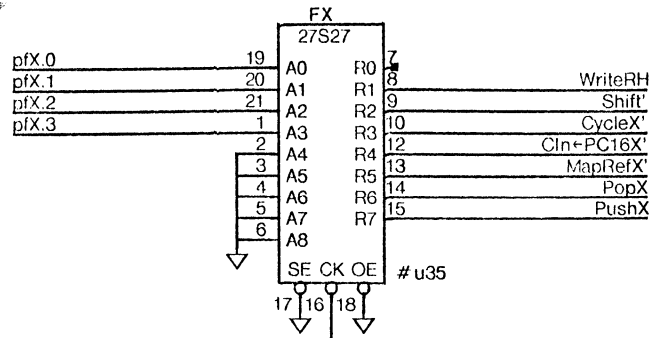


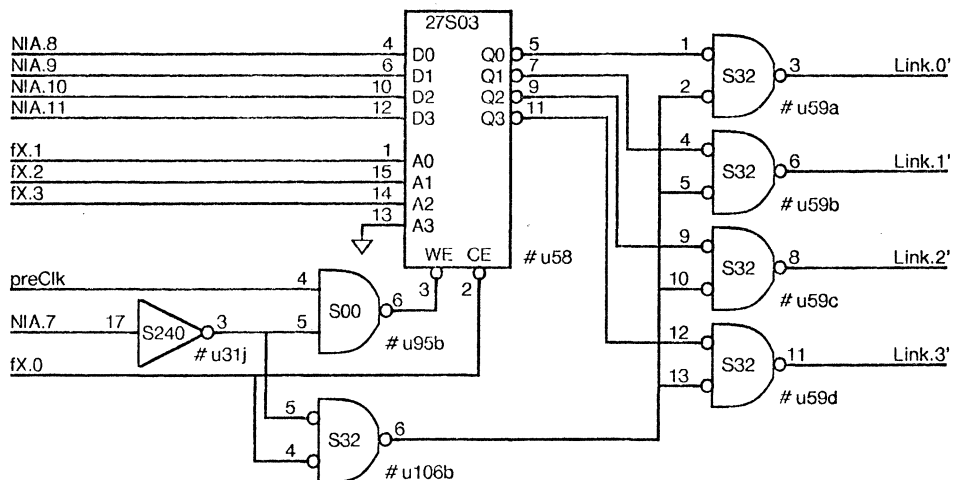
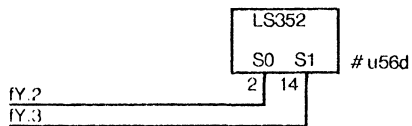
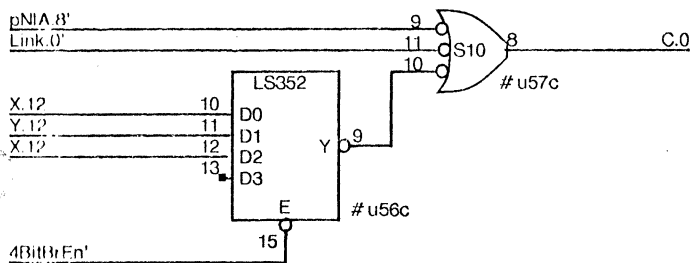
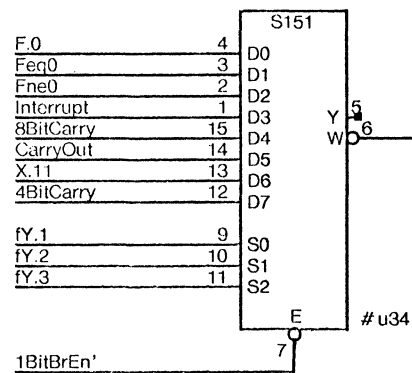
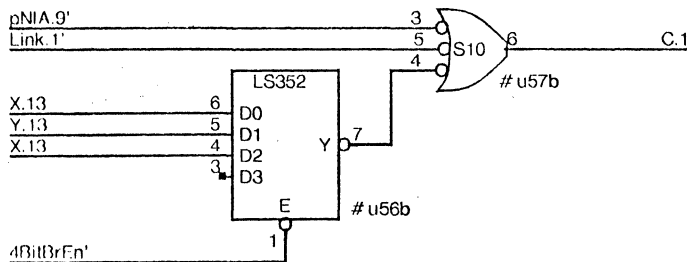
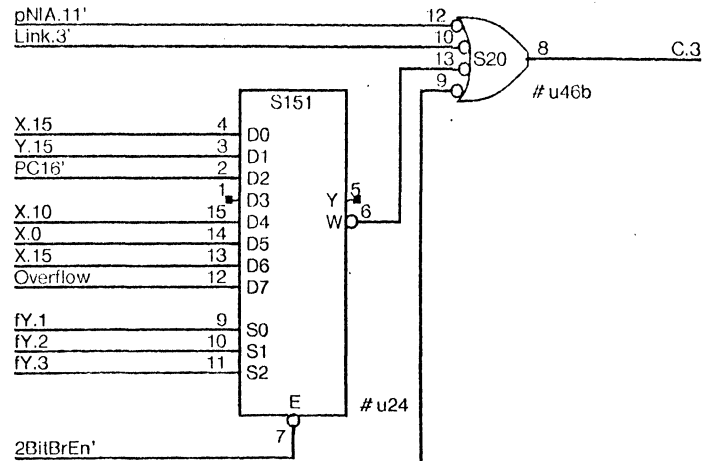
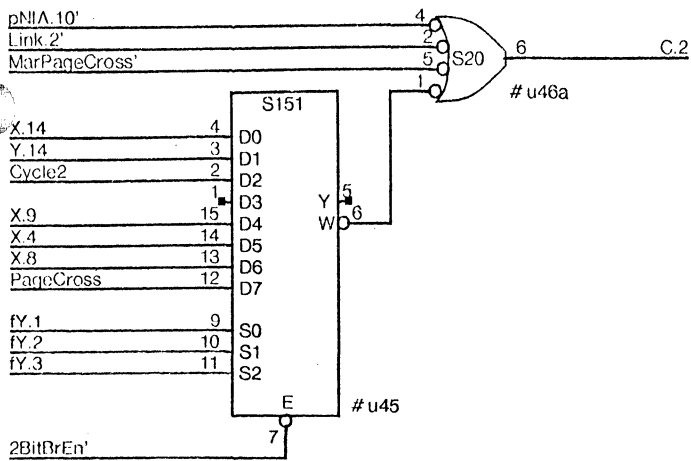


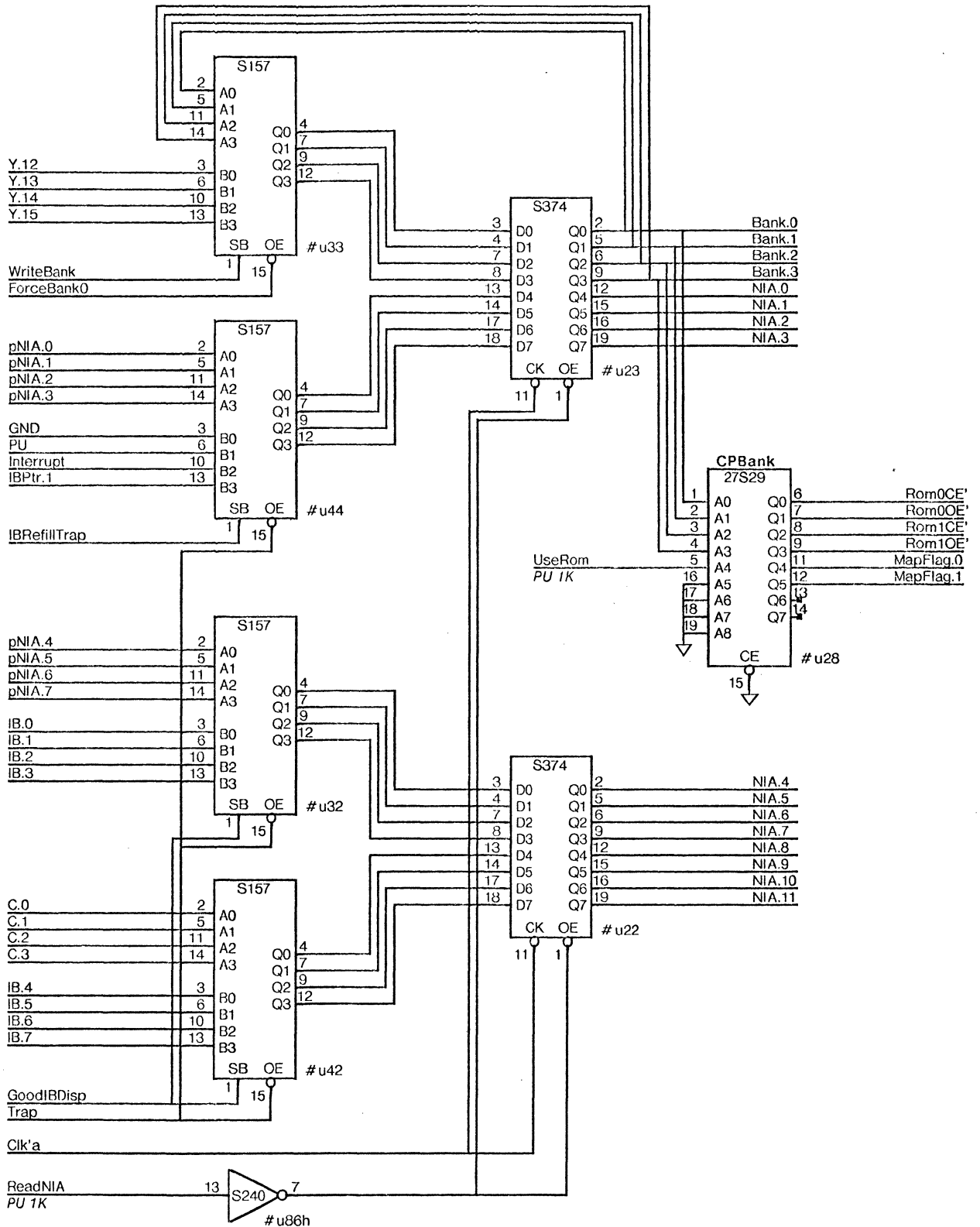
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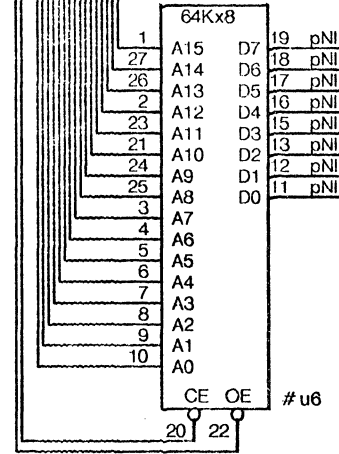
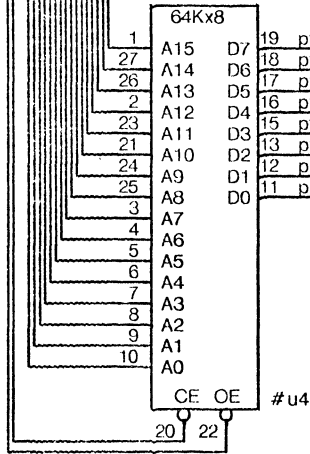
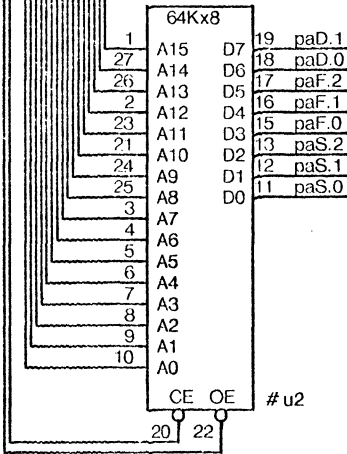
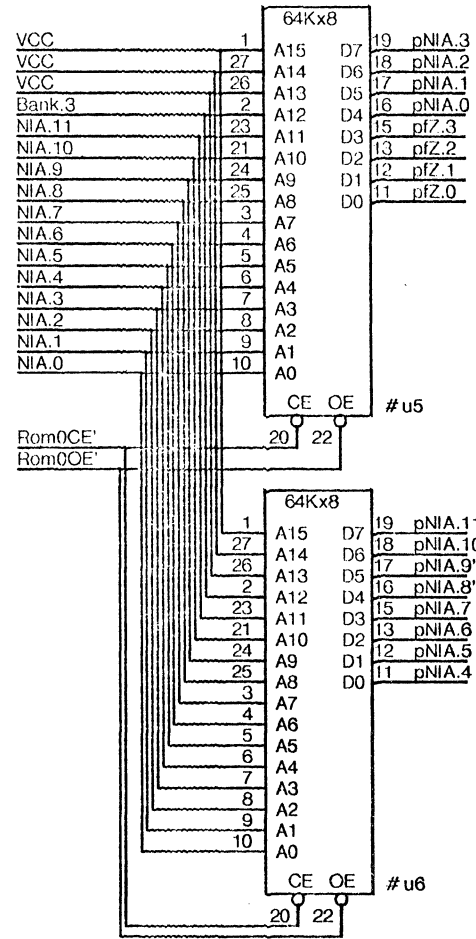
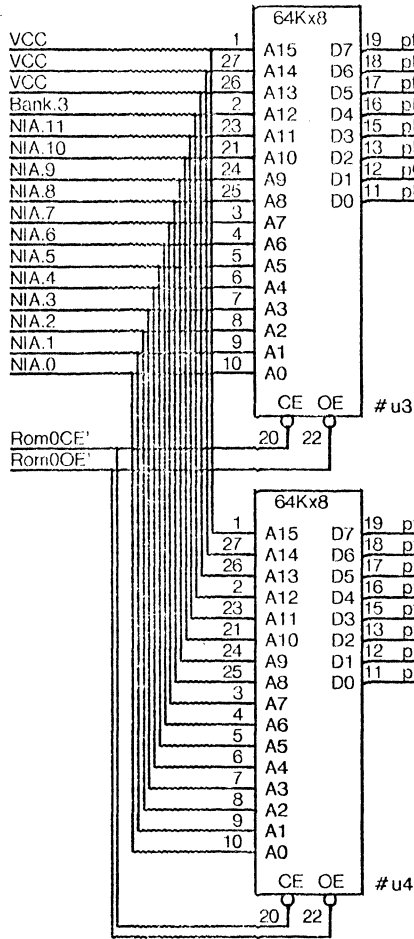
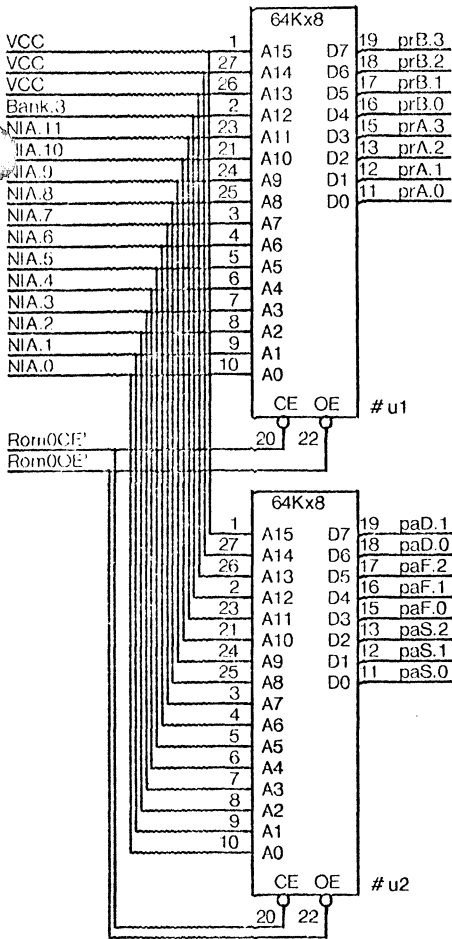




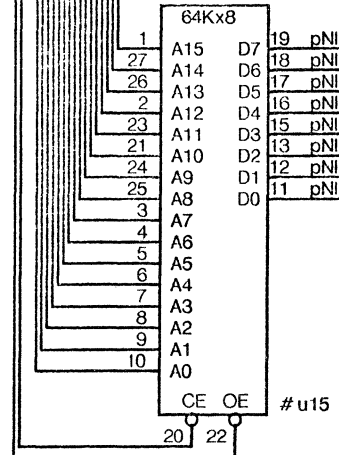
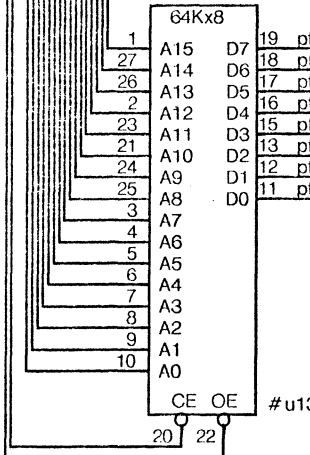
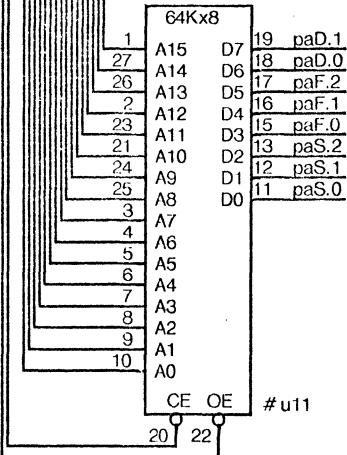
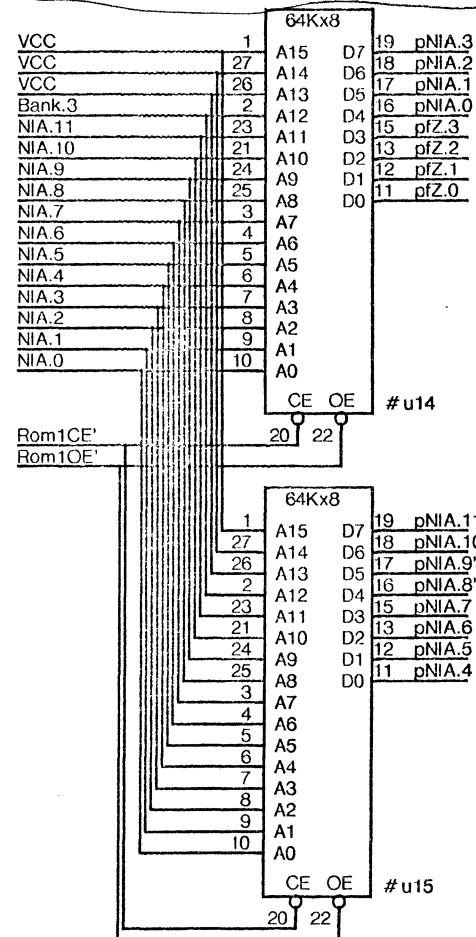
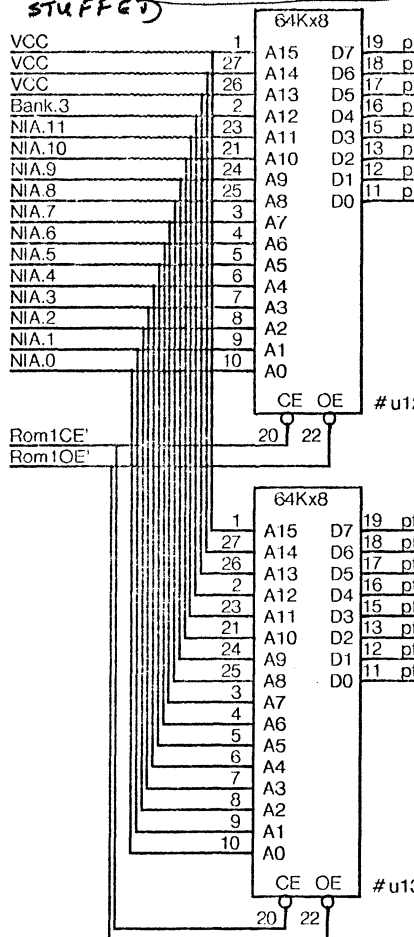
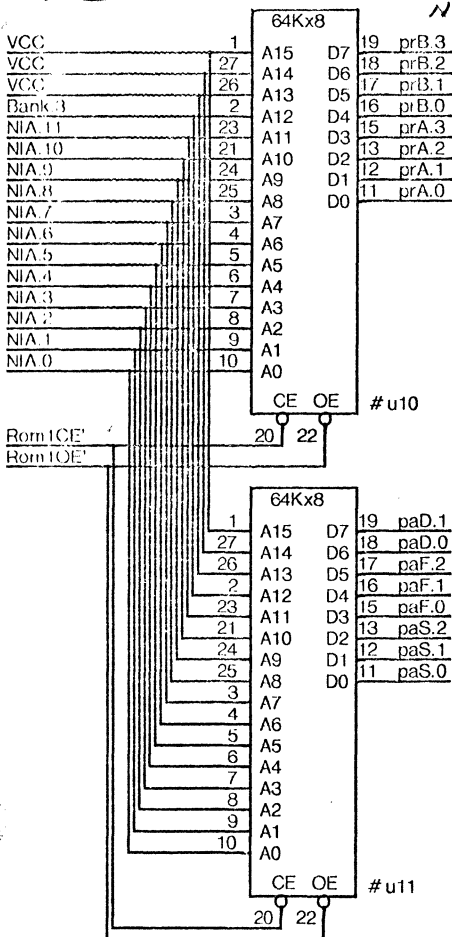


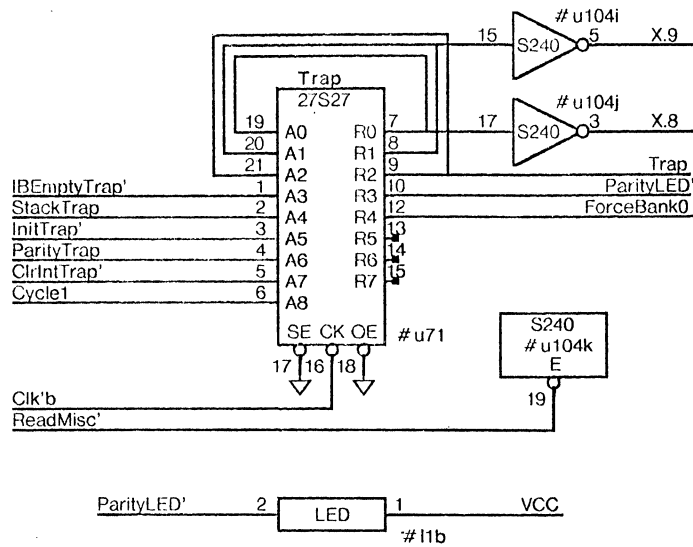




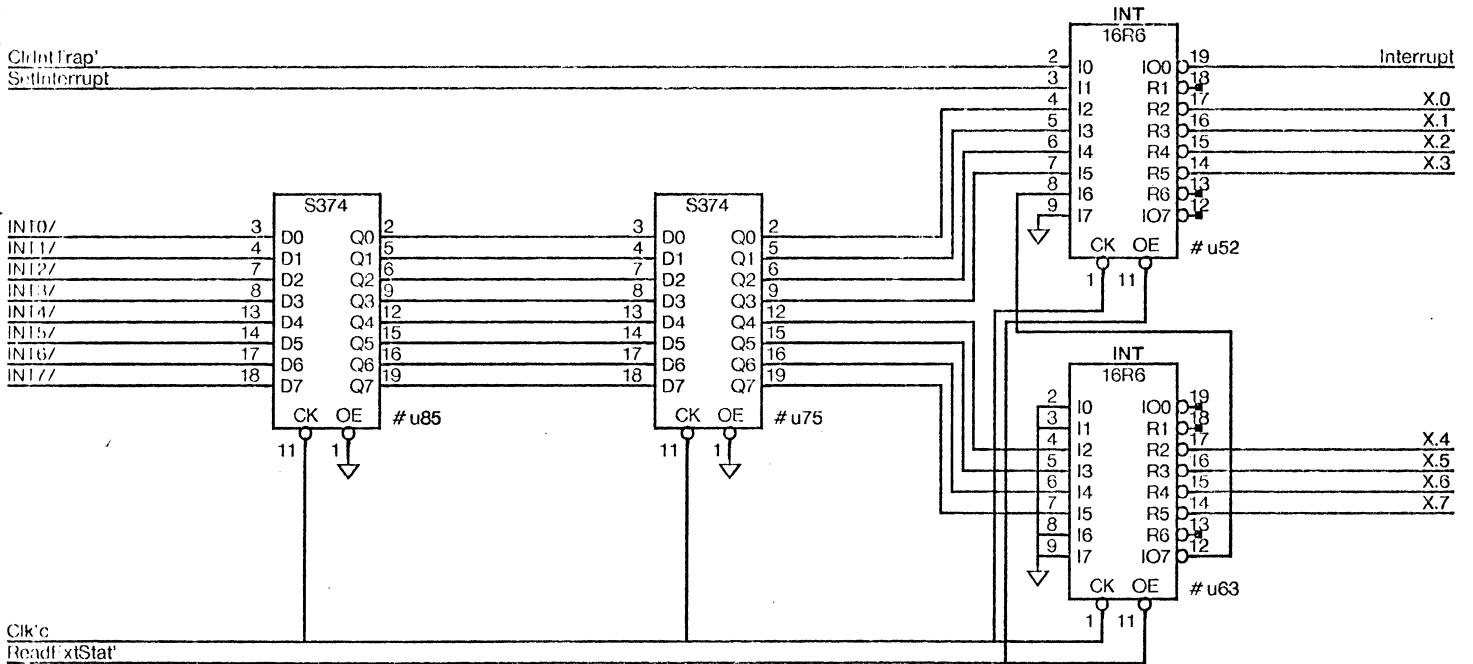


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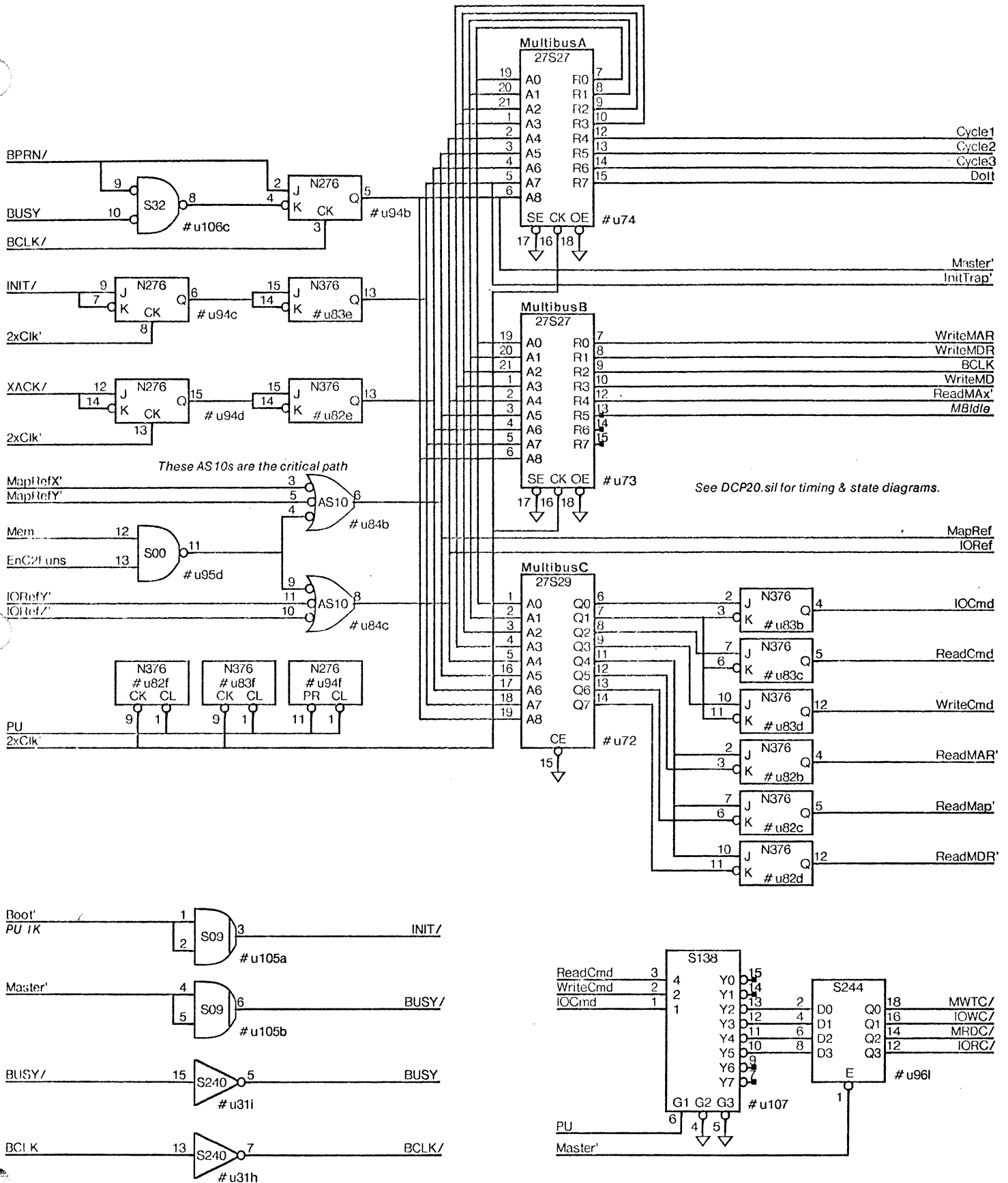


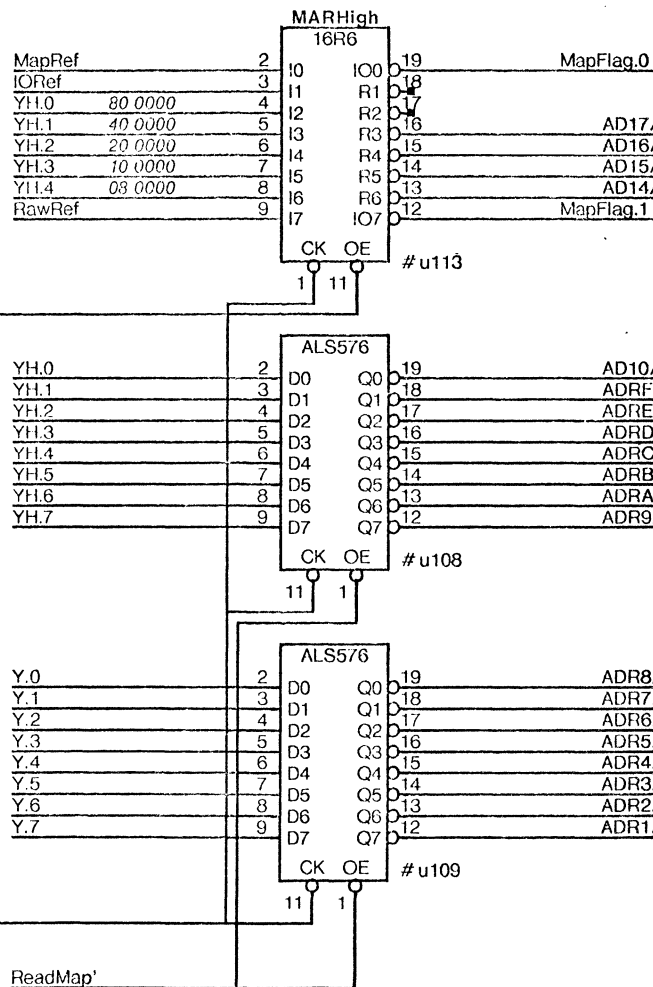
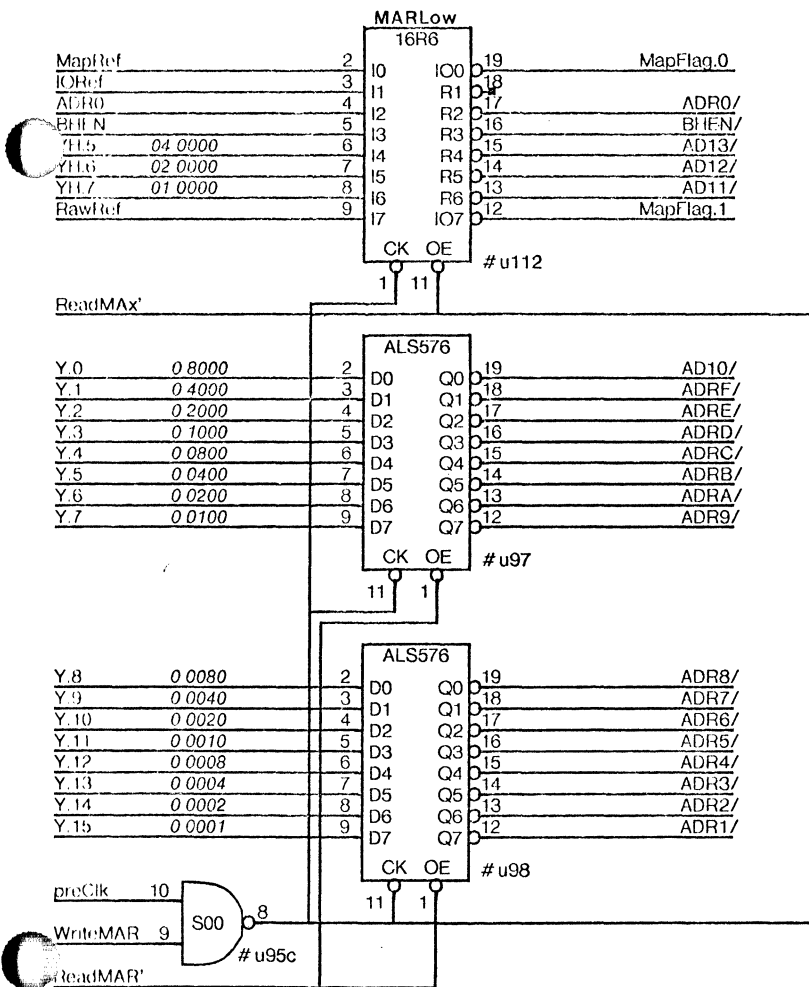
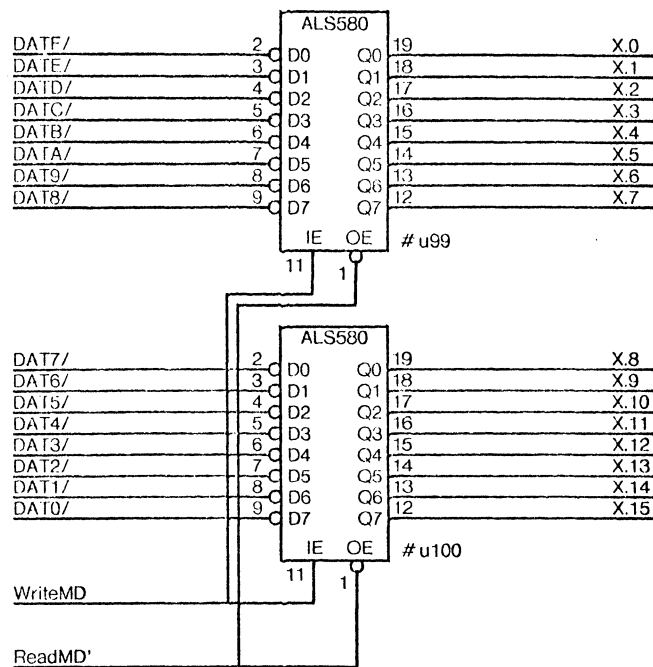
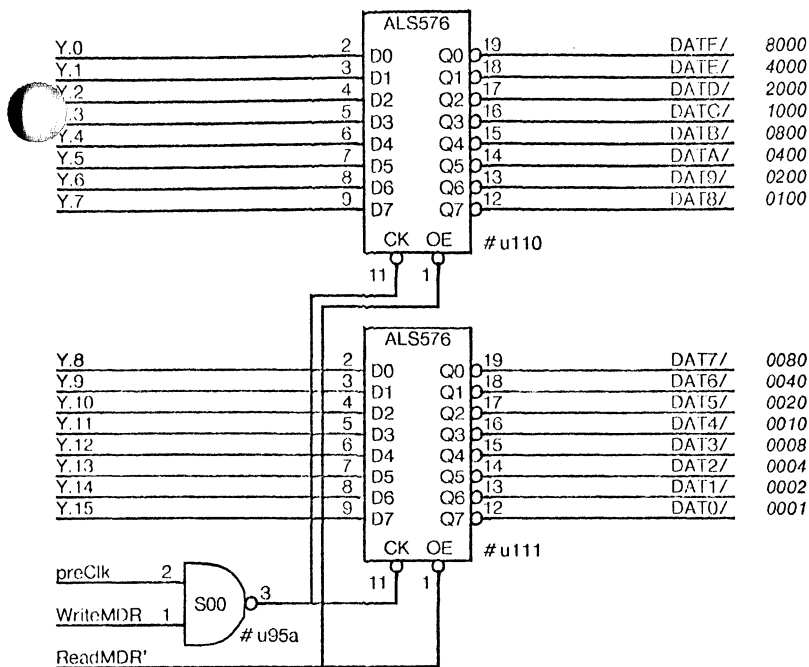
X[8-9]	Trap
0	CSParity
1	Init
2	Stack
3	IBEmpy

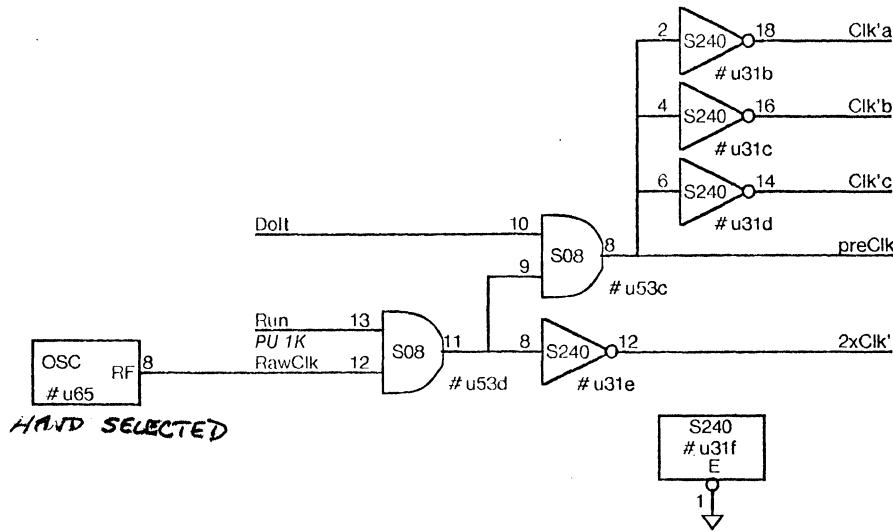


See DCP19.sil for PAL contents

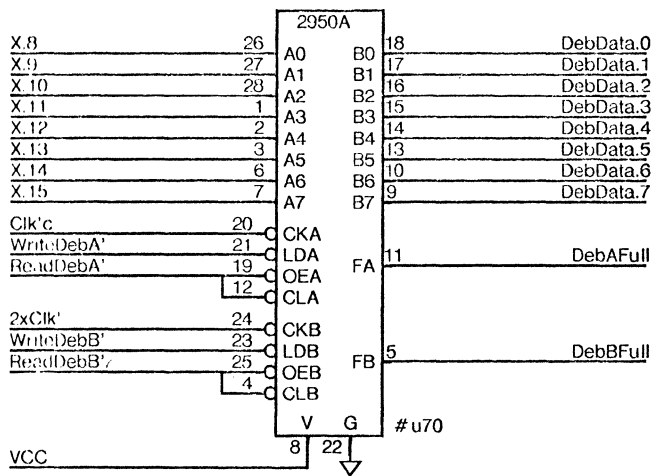
Beware: These PROMs are running way over specs



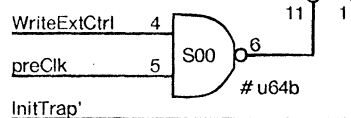
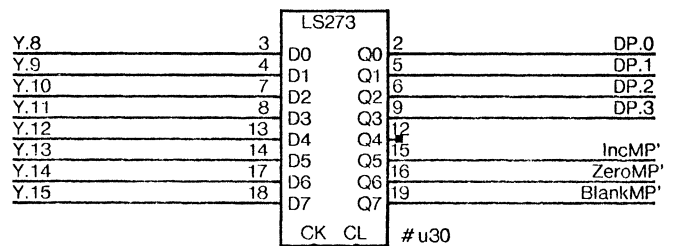
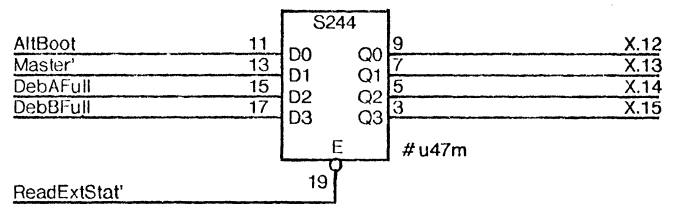


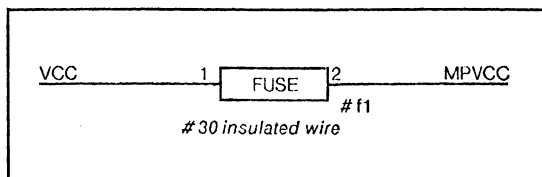
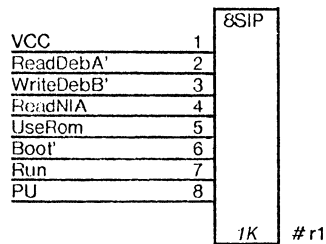


HAND SELECTED

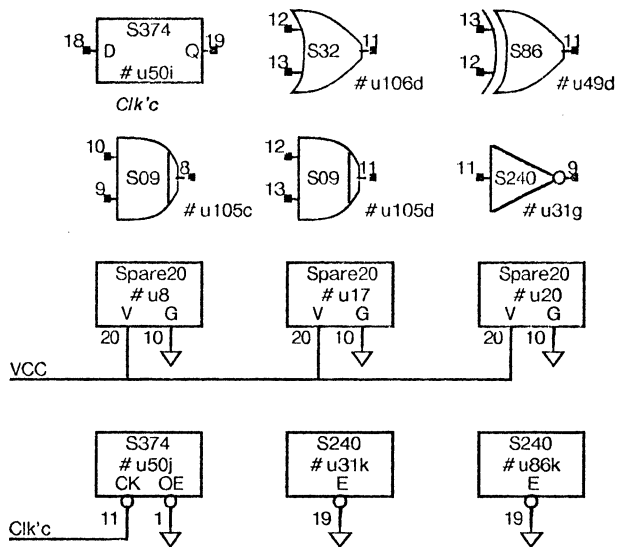


CP writes A and reads B





Add this in Rev J



GND	101	GND	102
VCC	103	VCC	104
VCC	105	VCC	106
GND	111	GND	112
BCLK/	113	INIT/	114
BPRN/	115		
BUSY/	117		
MRDC/	119	MWTC/	120
IORC/	121	IOWC/	122
XACK/	123		
BHEN/	127	AD10/	128
		AD11/	130
		AD12/	132
		AD13/	134
INT6/	135	INT7/	136
INT4/	137	INT5/	138
INT2/	139	INT3/	140
INT0/	141	INT1/	142
ADRE/	143	ADRF/	144
ADRC/	145	ADRD/	146
ADRA/	147	ADRB/	148
ADR8/	149	ADR9/	150
ADR6/	151	ADR7/	152
ADR4/	153	ADR5/	154
ADR2/	155	ADR3/	156
ADR0/	157	ADR1/	158
DATE/	159	DATE/	160
DATC/	161	DATD/	162
DATA/	163	DATB/	164
DAT8/	165	DAT9/	166
DAT6/	167	DAT7/	168
DAT4/	169	DAT5/	170
DAT2/	171	DAT3/	172
DAT0/	173	DAT1/	174
GND	175	GND	176
VCC	181	VCC	182
VCC	183	VCC	184
GND	185	GND	186

P1

AD16/	255	AD17/	256
AD14/	257	AD15/	258

Component side **P2** Solder Side

GND	301	GND	302
Bank.0	303	Bank.1	304
Bank.2	305	Bank.3	306
NIA.0	307	NIA.1	308
NIA.2	309	NIA.3	310
NIA.4	311	NIA.5	312
NIA.6	313	NIA.7	314
NIA.8	315	NIA.9	316
NIA.10	317	NIA.11	318
prA.0	319	prA.1	320
prA.2	321	prA.3	322
prB.0	323	prB.1	324
GND	325	GND	326
prB.2	327	prB.3	328
paS.0	329	paS.1	330
paS.2	331	paF.0	332
paF.1	333	paF.2	334
paD.0	335	paD.1	336
pEP	337	pCIn	338
pEnU	339	pMem	340
pfS.0	341	pfS.1	342
pfS.2	343	pfS.3	344
pfX.0	345	pfX.1	346
pfX.2	347	pfX.3	348
GND	349	GND	350

Component side **J1** Solder Side

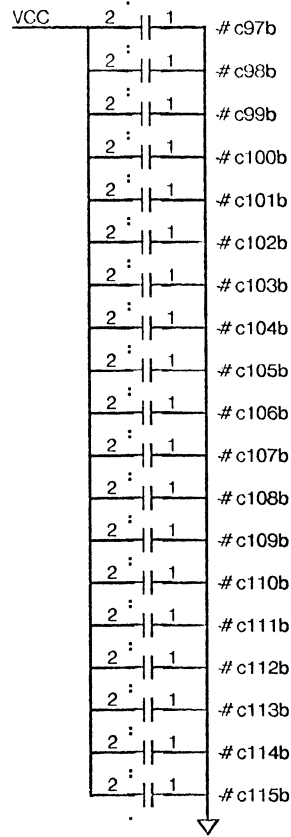
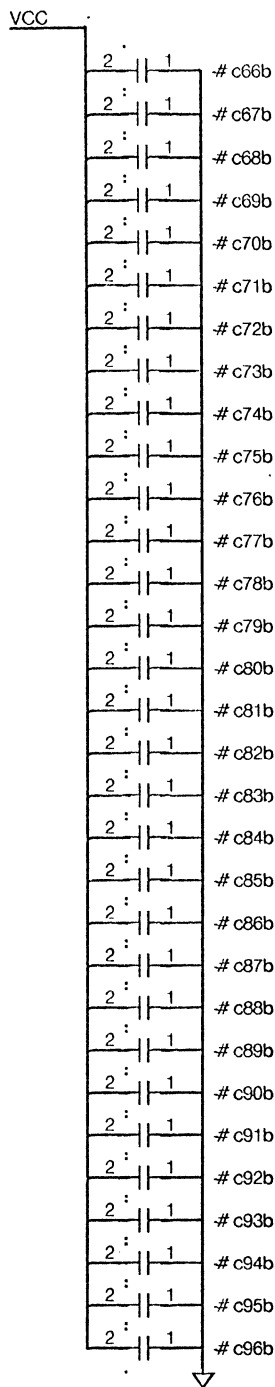
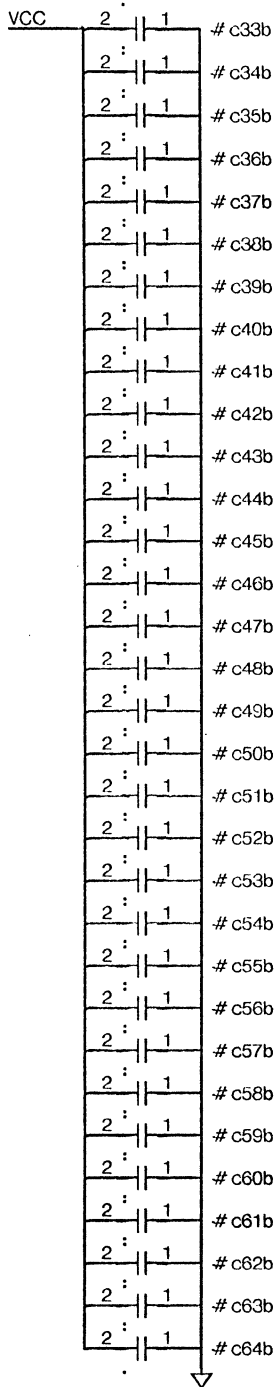
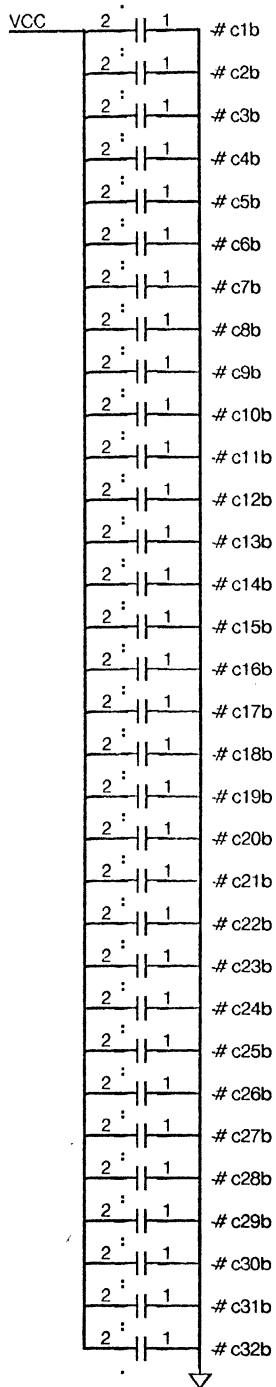
GND	501	DP.0	506
AltBoot	505	DP.1	508
Boot'	507	DP.2	510
BlankMP'	511	DP.3	512
ZeroMP'	513	VCC	516
IncMP'	515		

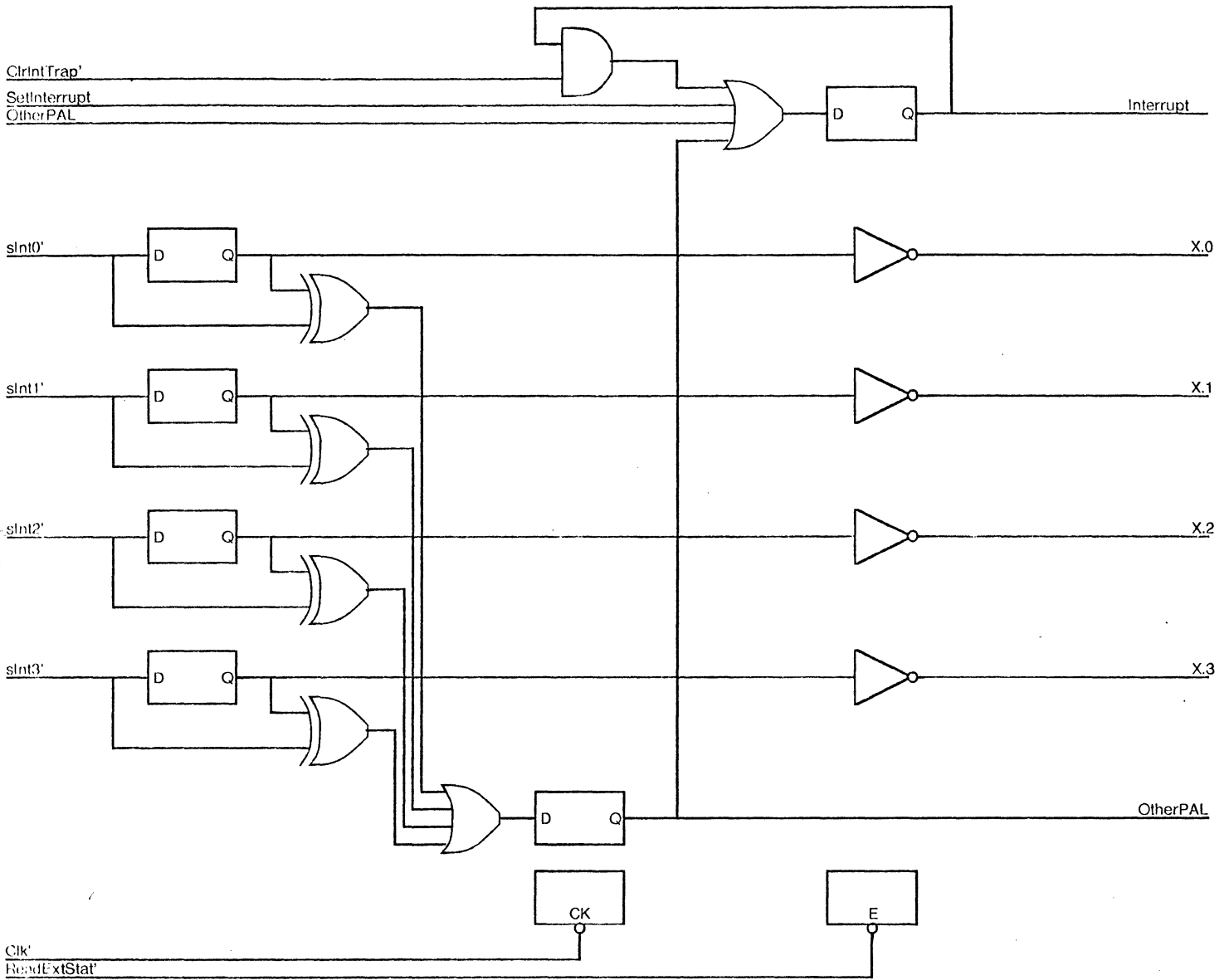
Component side **J3** Solder Side

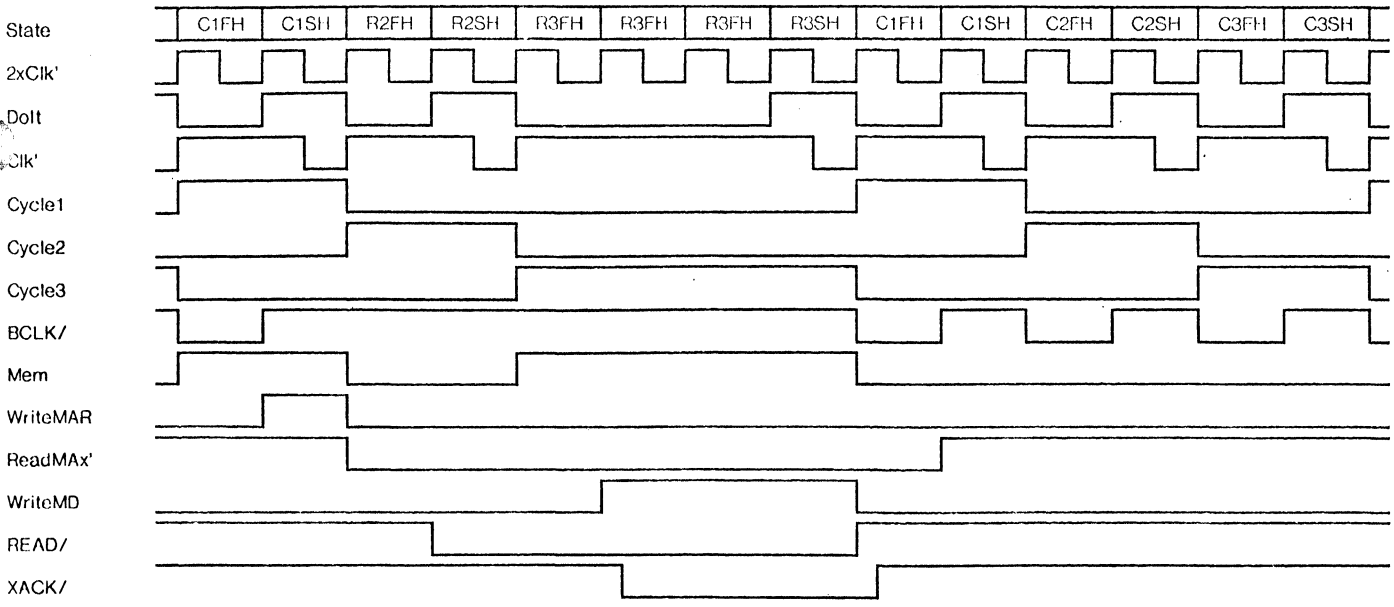
GND	401	GND	402
pfY.0	403	pfY.1	404
pfY.2	405	pfY.3	406
pfZ.0	407	pfZ.1	408
pfZ.2	409	pfZ.3	410
pNIA.0	411	pNIA.1	412
pNIA.2	413	pNIA.3	414
pNIA.4	415	pNIA.5	416
pNIA.6	417	pNIA.7	418
pNIA.8'	419	pNIA.9'	420
pNIA.10'	421	pNIA.11'	422
MBIdle	423	dGoodIBDisp	424
GND	425	GND	426
DebData.0	427	DebData.1	428
DebData.2	429	DebData.3	430
DebData.4	431	DebData.5	432
DebData.6	433	DebData.7	434
DebAFull	435	DebBFull	436
WriteDebB'	437	ReadDebA'	438
MapRef	439	IORef	440
UserRom	441	ReadNIA	442
Run	443	Dolt	444
Cycle2	445	Cycle1	446
RawClk	447	Cycle3	448
GND	449	GND	450

Component side **J2** Solder Side

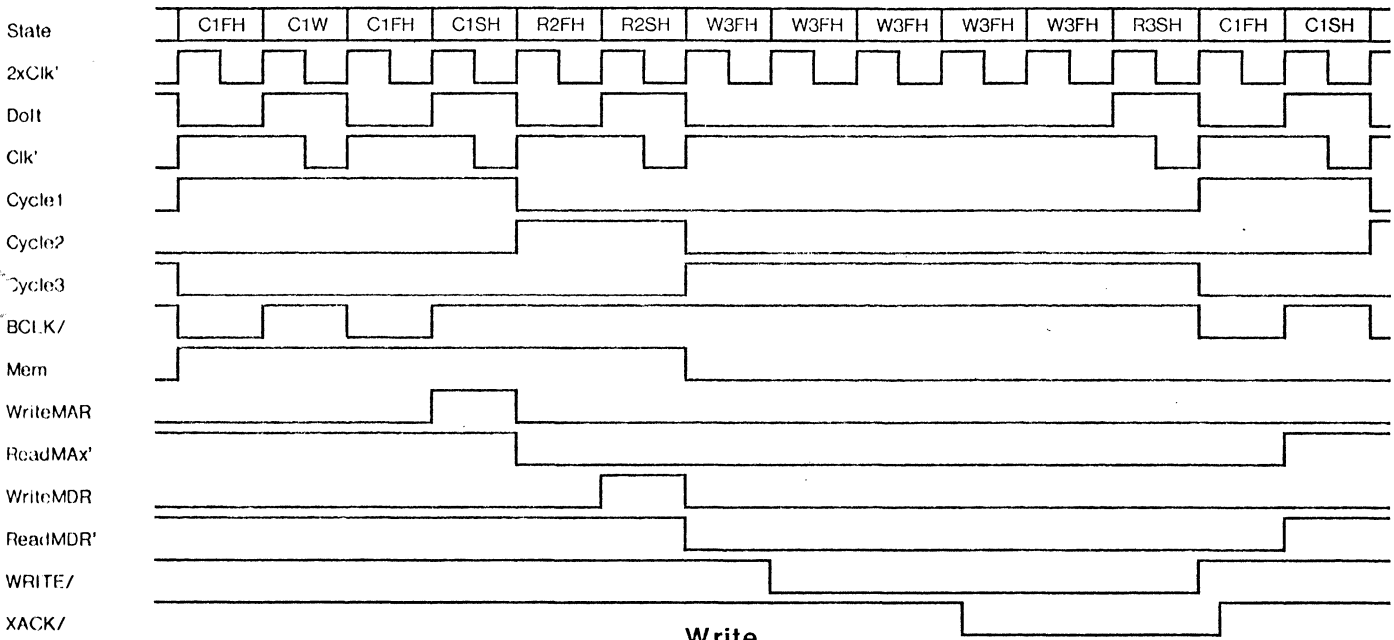
NB: The pin numbers on J1, J2, and J3 correspond to the Multibus specs. The numbers on the 3M connectors are top/bottom reversed. The numbers on the StitchWeld boards are top/bottom reversed.



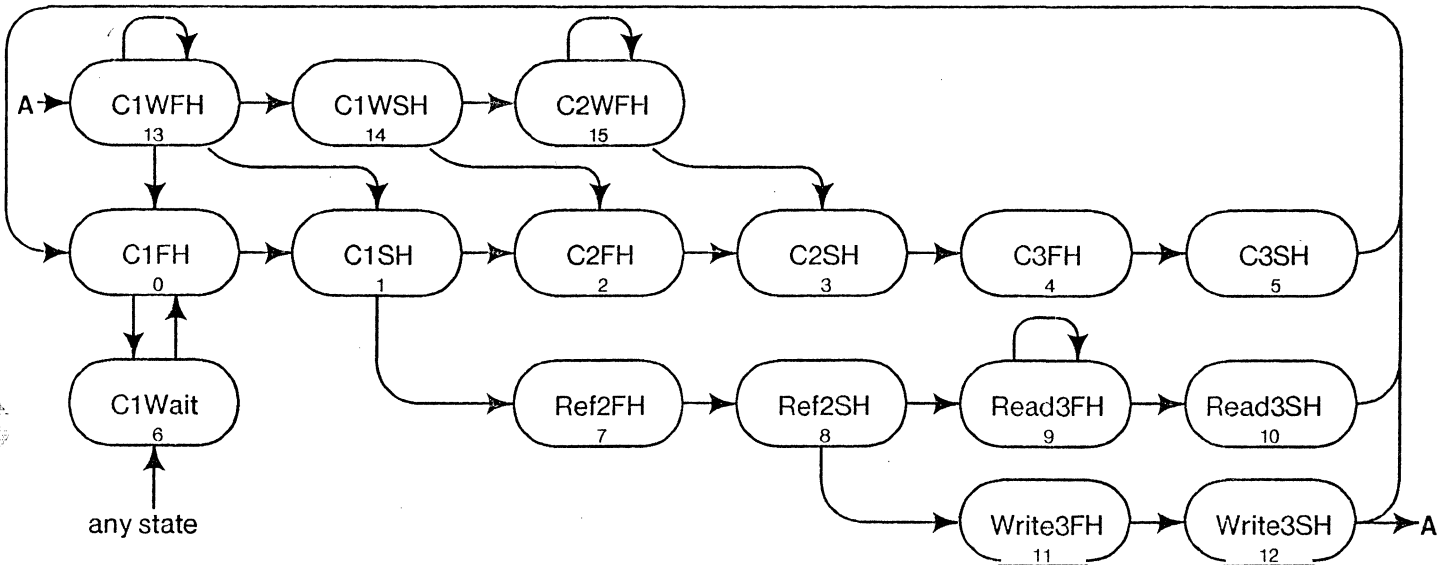


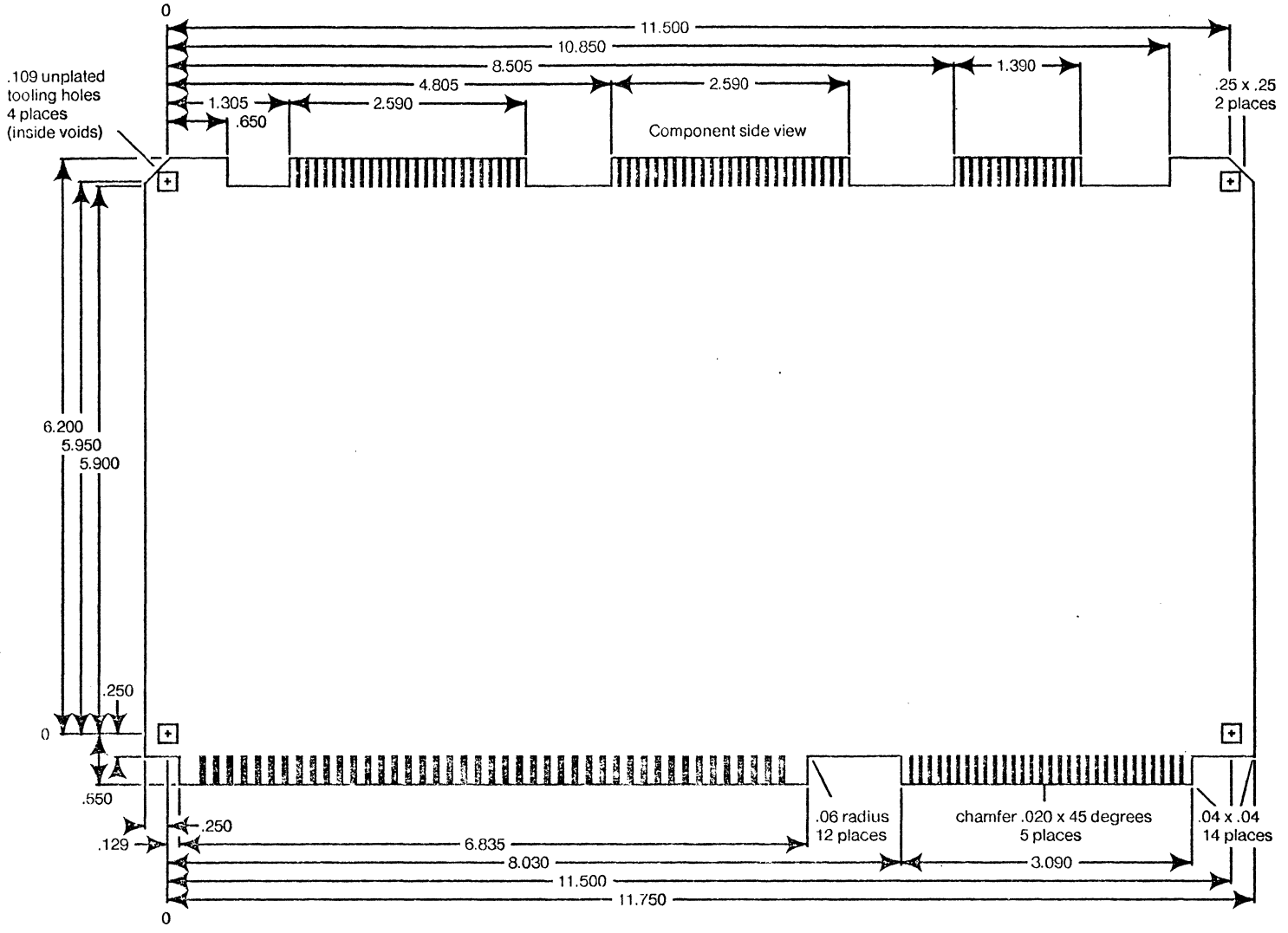


Read



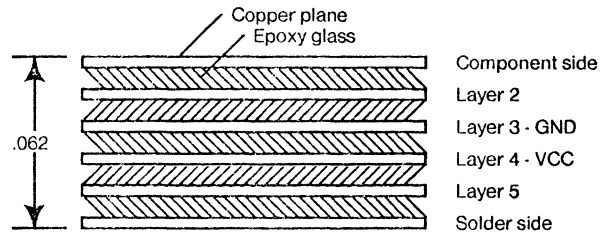
Write



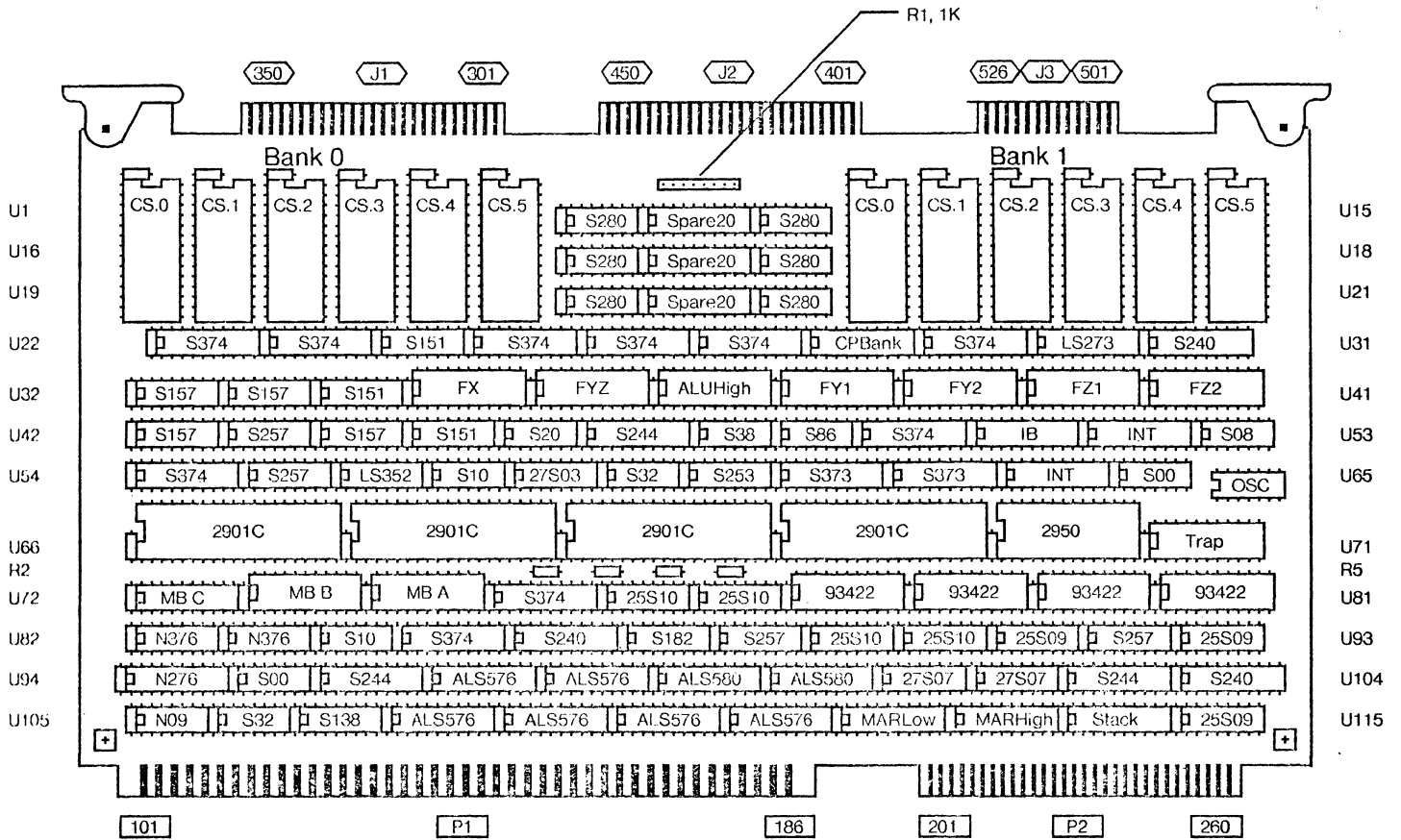


NOTES

- ① All dimensions are in inches; drawing is not to scale.
X.XXX is + .005; X.XX is + .01.
- ② Except as noted, this printed board shall be made in accordance with IPC-ML-910 Class II.
- ③ Acceptability of the finished board will be judged in accordance with IPC-A-600.
- ④ Base material: 1 oz Cu on FR4 in accordance with IPC-L-130.
- ⑤ Bonding agent: prepreg B-stage in accordance with IPC-L-110.
- ⑥ Solder mask: green epoxy in accordance with IPC-SM-840.
- ⑦ Silk screen: none
- ⑧ Plating: .000050 Au over .000200 Ni on contact fingers.
.0003 Sn-Pb over .0010 Cu in holes and on traces.
- ⑨ Holes: tooling holes finished diameter .109.
component & connector holes finished diameter .031.
feedthru holes finished diameter .018.
- ⑩ Pads: components & connectors .050, feedthrus .030.
- ⑪ Conductors: .010 wide, .010 spacing.



XEROX	Project	Reference	File	Drawn by	Rev	Date	Page
PARC	Dicentra	Fabrication Drawing	DCP23.sil	David Boggs	I	4/22/84	23



R2, R3: 220
R4, R5: 1K

Proms, pals, and oscillator are socketed.
Odd numbered edge pins are on the component side
Even numbered edge pins are on the solder side
NB: The pin numbers on J1, J2, and J3 correspond to the Multibus specs.
The numbers on the 3M connectors are top/bottom reversed.
The numbers on the StitchWeld boards are top/bottom reversed.

Rework:
Add MB1dle from J2.23 to U73.13

Proms & Pals					
Position	Type	Name	Position	Type	Name
U28	27S29	CPBank	U52	16R6	INT
U35	27S27	FX	U63	16R6	INT
U36	27S27	FYZ	U71	27S27	Trap
U37	27S27	ALUHigh	U72	27S29	MultibusC
U38	27S27	FY1	U73	27S27	MultibusB
U39	27S27	FY2	U74	27S27	MultibusA
U40	27S27	FZ1	U112	16R6	MARLow
U41	27S27	FZ2	U113	16R6	MARHigh
U51	27S29	IB	U114	27S29	Stack

```
// DCP-Multibus.bcp1 -- Multibus FSM Roms for Dicentra Central Processor
// Loaded with DCP-Proms.bcp1
// Last modified October 28, 1983 1:22 AM by Boggs
```

```
external Multibus
```

```
manifest [ high = 1; low = 0 ]
```

```
//-----
let Multibus(addr, data) be
```

```
//-----
```

```
[
```

```
manifest
```

```
[
  // FSM states
  C1FH = 0
  C1SH = 1
  C2FH = 2
  C2SH = 3
  C3FH = 4
  C3SH = 5
  C1Wait = 6
  Ref2FH = 7
  Ref2SH = 8
  Read3FH = 9
  Read3SH = 10
  Write3FH = 11
  Write3SH = 12
  C1WFH = 13
  C1WSH = 14
  C2WFH = 15
]
```

```
structure Addr:
```

```
[
  blank bit 7
  CurState bit 4
  IORef bit
  MapRef bit
  XACK bit //low true
  InitTrap bit //low true
  Master bit //low true
]
```

```
structure Data:
```

```
[
  NextState bit 4
  Cycle1 bit
  Cycle2 bit
  Cycle3 bit
  DoIt bit
  WriteMar bit
  WriteMDR bit
  BCLK bit
  WriteMD bit //low true
  ReadMAX bit
  MBIdle bit
  bTANK bit 2
  IOCmd bit
  ClearCmd bit //low true
  ReadCmd bit
  WriteCmd bit
  ClearAD bit
  ReadMar bit //low true
  ReadMap bit //low true
  ReadMDR bit //low true
  blank bit 8
]
```

```

let CurrentState = addr<<Addr.CurState
let IORef = addr<<Addr.IORef eq high
let MapRef = addr<<Addr.MapRef eq high
let XACK = addr<<Addr.XACK eq low
let InitTrap = addr<<Addr.InitTrap eq low
let Master = addr<<Addr.Master eq low

let NextState = nil
let Cycle1, Cycle2, Cycle3, DoIt = false, false, false, false
let WriteMar, WriteMDR, BCLK, WriteMD = false, false, nil, false
let ReadMAX, MBIdle = false, false
let IOCmd, ReadCmd, WriteCmd, ClearCmd = false, false, false, false
let ReadMar, ReadMap, ReadMDR, ClearAD = false, false, false, false

if InitTrap & CurrentState ne C1FH then CurrentState = C1Wait

switchon CurrentState into
[
  case C1FH:
    [
      Cycle1 = true
      ClearAD = true
      BCLK = low
      test InitTrap
      ifso
      [
        DoIt = true
        NextState = C1Wait
      ]
      ifnot test IORef % MapRef
      ifnot
      [
        DoIt = true
        NextState = C1SH
      ]
      ifso test Master
      ifso
      [
        WriteMar = true
        DoIt = true
        NextState = C1SH
      ]
      ifnot NextState = C1Wait
    ]
  ]
  case C1Wait:
    [
      Cycle1 = true
      BCLK = high
      ClearCmd = true
      NextState = C1FH
    ]
  ]
  case C1SH:
    [
      Cycle2 = true
      test IORef % MapRef
      ifnot
      [
        ClearAD = true
        BCLK = high
        NextState = C2FH
      ]
      ifso
      [
        BCLK = low
        IOCmd = IORef & not MapRef
        test MapRef & not IORef
        ifso ReadMap = true
        ifnot ReadMar = true
        ReadMAX = true
        NextState = Ref2FH
      ]
    ]
  ]
endcase
]

```

```
case Ref2FH:
[
  Cycle2 = true
  BCLK = low
  test IORef & MapRef
    ifnot ReadCmd = true
    ifso WriteMDR = true
  ReadMAX = true
  DoIt = true
  NextState = Ref2SH
endcase
]
case Ref2SH:
[
  Cycle3 = true
  BCLK = low
  ReadMAX = true
  test IORef & MapRef
    ifnot NextState = Read3FH
    ifso
      [
        ReadMDR = true
        NextState = Write3FH
      ]
    endcase
  ]
case Read3FH:
[
  Cycle3 = true
  BCLK = low
  WriteMD = true
  ReadMAX = true
  test XACK
    ifnot NextState = Read3FH
    ifso
      [
        DoIt = true
        NextState = Read3SH
      ]
    endcase
  ]
case Read3SH:
[
  Cycle1 = true
  BCLK = high
  ReadMAX = true
  ClearCmd = true
  NextState = C1FH
endcase
]
```

```
case Write3FH:
[
  Cycle3 = true
  BCLK = low
  WriteMD = true
  ReadMAX = true
  unless IORef & MapRef do WriteCmd = true
  DoIt = true
  NextState = Write3SH
endcase
]
case Write3SH:
[
  Cycle1 = true
  ReadMAX = true
  if IORef & MapRef then XACK = true
  test XACK
  ifnot
  [
    BCLK = low
    NextState = C1WFH
  ]
  ifso
  [
    ClearCmd = true
    BCLK = high
    NextState = C1FH
  ]
endcase
]
```

```
case C1WFH:
[
  Cycle1 = true
  ReadMAX = true
  BCLK = low
  test XACK
  ifnot test IORef % MapRef
  ifnot
  [
    DoIt = true
    NextState = C1WSH
  ]
  ifso NextState = C1WFH
  ifso
  [
    ClearCmd = true
    test IORef % MapRef
    ifso
    [
      BCLK = high
      NextState = C1FH
    ]
    ifnot
    [
      DoIt = true
      NextState = C1SH
    ]
  ]
]
endcase
]
case C1WSH:
[
  Cycle2 = true
  ReadMAX = true
  test XACK
  ifso
  [
    BCLK = high
    ClearCmd = true
    NextState = C2FH
  ]
  ifnot
  [
    BCLK = low
    NextState = C2WFH
  ]
]
endcase
]
case C2WFH:
[
  Cycle2 = true
  ReadMAX = true
  BCLK = low
  test XACK
  ifso
  [
    DoIt = true
    ClearCmd = true
    NextState = C2SH
  ]
  ifnot NextState = C2WFH
endcase
]
```

```
case C2FH:
[
  DoIt = true
  Cycle2 = true
  ClearAD = true
  BCLK = low
  NextState = C2SH
endcase
]
case C2SH:
[
  Cycle3 = true
  MBIdle = true
  ClearAD = true
  BCLK = high
  NextState = C3FH
endcase
]
case C3FH:
[
  DoIt = true
  Cycle3 = true
  BCLK = low
  NextState = C3SH
endcase
]
case C3SH:
[
  Cycle1 = true
  BCLK = high
  NextState = C1FH
endcase
]
]

data>>Data.NextState = high? NextState, not NextState
data>>Data.Cycle1 = Cycle1? high, low
data>>Data.Cycle2 = Cycle2? high, low
data>>Data.Cycle3 = Cycle3? high, low
data>>Data.DoIt = DoIt? high, low
data>>Data.WriteMar = WriteMar? high, low
data>>Data.WriteMDR = WriteMDR? high, low
data>>Data.BCLK = BCLK
data>>Data.WriteMD = WriteMD? high, low
data>>Data.ReadMAX = ReadMAX? low, high
data>>Data.MBIdle = MBIdle? high, low
data>>Data.IOCmd = IOCmd? high, low
data>>Data.ClearCmd = ClearCmd? low, high
data>>Data.ReadCmd = ReadCmd? high, low
data>>Data.WriteCmd = WriteCmd? high, low
data>>Data.ClearAD = ClearAD? high, low
data>>Data.ReadMar = ReadMar? low, high
data>>Data.ReadMap = ReadMap? low, high
data>>Data.ReadMDR = ReadMDR? low, high
]
```

```

// DCP-Proms.bcp1 -- Dicentra Central Processor Proms
// Loaded with DCP-Multibus.bcp1
// Last modified October 23, 1983 7:40 PM by Boggs

external [ Ws; OpenFile; Puts; Closes; Allocate; Free; sysZone; Multibus ]

static [ memory; mbFile ]

structure String [ length byte; char+1,1 byte ]

manifest [ high = 1; low = 0 ]

-----
let DCPProms() be
-----
[
mbFile = OpenFile("DCP-Proms.mb")

DoMemory("Stack", 512, 8, Stack)
DoMemory("IB", 512, 8, IB)
DoMemory("ALUHigh", 512, 8, ALUHigh)
DoMemory("FX", 512, 8, FX)
DoMemory("FYZ", 512, 8, FYZ)
DoMemory("FY1", 512, 8, FY1)
DoMemory("FY2", 512, 8, FY2)
DoMemory("FZ1", 512, 8, FZ1)
DoMemory("FZ2", 512, 8, FZ2)
DoMemory("CPBank3632", 512, 8, CPBank3632)
DoMemory("CPBank2732", 512, 8, CPBank2732)
DoMemory("Trap", 512, 8, Trap)
DoMemory("Multibus", 512, 24, Multibus)

Puts(mbFile, 0) //0 = end of file
Closes(mbFile)
]

-----
and DoMemory(name, nAddr, nData, Proc) be
-----
// nAddr is number of addresses
// nData is number of output bits
[
Ws("**N"); Ws(name)

Puts(mbFile, 4) //4 = define memory
memory = memory + 1
Puts(mbFile, memory)
Puts(mbFile, nData)
if name>>String.length gr 1 then
  for i = 1 to name>>String.length-1 by 2 do
    Puts(mbFile, name>>String.char+i lshift 8 + name>>String.char+(i+1))
Puts(mbFile, (name>>String.length & 1) eq 0? 0,
  name>>String.char+(name>>String.length) lshift 8)

Puts(mbFile, 2) //2 = set current memory
Puts(mbFile, memory)
Puts(mbFile, 0) //location counter (not used)

let data = Allocate(sysZone, (nData+15)/16)
for addr = 0 to nAddr-1 do
  [
Puts(mbFile, 1) //1 = memory contents
Puts(mbFile, 0) //source line number (not used)
Proc(addr, data)
for i = 0 to (nData+15)/16 - 1 do Puts(mbFile, data+i)
  ]
Free(sysZone, data)
]

```



```
//-----  
and Stack(addr, data) be  
//-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    StackP bit 4  
    PopX bit  
    PopZ bit  
    PushX bit  
    PushY bit  
    PushZ bit  
  ]  
  
  structure Data:  
  [  
    StackTrap bit  
    blank bit 3  
    StackP bit 4  
    blank bit 8  
  ]  
  
  let PopX = addr<<Addr.PopX eq high  
  let PopZ = addr<<Addr.PopZ eq high  
  let PushX = addr<<Addr.PushX eq high  
  let PushY = addr<<Addr.PushY eq high  
  let PushZ = addr<<Addr.PushZ eq high  
  let StackP = addr<<Addr.StackP  
  
  let Pop = PopX % PopZ  
  let Push = PushX % PushY % PushZ  
  
  let StackTrap = Pop & StackP eq 0 %  
  Push & StackP eq 15 %  
  PopX & Push & StackP eq 0 %  
  Push & PopZ & StackP eq 15 %  
  PopX & PopZ & (StackP eq 0 % StackP eq 1) %  
  PopX & PopZ & Push & (StackP eq 0 % StackP eq 1)  
  
  if Pop then StackP = StackP -1  
  if Push then StackP = StackP +1  
  
  data>>Data.StackP = StackP  
  data>>Data.StackTrap = StackTrap? high, low  
]
```

```
-----
and IB(addr, data) be
-----
[
manifest
[
// instruction buffer states
ibEmpty = 0
ibByte = 1
ibFull = 2
ibWord = 3
]

structure Addr:
[
blank bit 7
IBDisp bit
ReadIB bit
WriteIB bit
IBPtrGetsWord bit
IBPtrGetsByte bit
EnC2Funs bit
Interrupt bit
InIBPtr bit 2
unused bit
]

structure Data:
[
GoodIBDisp bit
IBEmpty bit //low true
IBRefillTrap bit
ReadIB0 bit //low true
ReadIB1 bit //low true
WriteIBFront bit
OutIBPtr bit 2
blank bit 8
]

let IBDisp = addr<<Addr.IBDisp eq high
let ReadIB = addr<<Addr.ReadIB eq high
let WriteIB = addr<<Addr.WriteIB eq high
let IBPtrGetsWord = addr<<Addr.IBPtrGetsWord eq high
let IBPtrGetsByte = addr<<Addr.IBPtrGetsByte eq high
let EnC2Funs = addr<<Addr.EnC2Funs eq high
let Interrupt = addr<<Addr.Interrupt eq high
let InIBPtr = addr<<Addr.InIBPtr

let IBEmpty = false
let IBRefillTrap = false
let GoodIBDisp = false
let ReadIB0 = false
let ReadIB1 = false
let WriteIBFront = false
let OutIBPtr = InIBPtr

let advance = false
```

```

// IBSrefillTrap causes a trap to one of four locations executed in Cycle 1:
// 3400b or 3000b Interrupt
// 2400b IB refill; IB not empty
// 2000b IB refill; IB is empty
if IBDisp & EnC2Funs & not ReadIB & not WriteIB & not IBPtrGetsWord then
  test (Interrupt % InIBPtr ne ibFull) & not IBPtrGetsByte
  ifso IBSrefillTrap = true
  ifnot [ GoodIBDisp = true; advance = true ]

// ReadIB puts IBFront onto the X bus and advances IBPtr.
// Since there are always at least 2 bytes in the buffer when we begin
// executing a Mesa instruction, ReadIB can't trap.
// Note that "ReadIB, IBDisp" is not legal (its a Noop).
if ReadIB & not IBDisp & not WriteIB & not IBPtrGetsWord & not IBPtrGetsByte then
  advance = true

if advance then
  [
  WriteIBFront = true
  ReadIB0 = (InIBPtr & 1) eq 0 //ReadIB0 is the inverse of IBPtr.1
  ReadIB1 = not ReadIB0
  OutIBPtr = selecton InIBPtr into
  [
  case ibFull: ibWord
  case ibWord: ibByte
  case ibByte: ibEmpty
  case ibEmpty: ibEmpty
  ]
  ]

// Unless we are refilling due to a jump instruction, IBPtr will be ibByte or ibEmpty.
// If it's ibEmpty then we need to write IBFront from IB0.
// If it's ibByte then we shouldn't write IBFront.
// If we are refilling due to a jump instruction, IBPtr value is unknown.
// It will be specified by a IBPtr- in this cycle or the next.
// Note that "WriteIB, ReadIB" is not legal (it's a Noop).
if WriteIB & not IBDisp & not ReadIB test InIBPtr eq ibEmpty
  ifso
  [
  WriteIBFront = true
  test IBPtrGetsByte
  ifso [ ReadIB1 = true; OutIBPtr = ibByte ]
  ifnot [ ReadIB0 = true; OutIBPtr = ibWord ]
  ]
  ifnot OutIBPtr = ibFull

// IBPtr-byte or IBPtr-word always come in cycle 1 immediately after a WriteIB.
// They load IBFront with the even or odd dest byte and set up IBPtr.
if IBPtrGetsWord & not IBDisp & not ReadIB & not WriteIB & not IBPtrGetsByte then
  [
  WriteIBFront = true
  ReadIB0 = true
  OutIBPtr = ibWord
  ]
if IBPtrGetsByte & not IBDisp & not ReadIB & not WriteIB & not IBPtrGetsWord then
  [
  WriteIBFront = true
  ReadIB1 = true
  OutIBPtr = ibByte
  ]

data>>Data.IBEmpty = OutIBPtr eq ibEmpty? low, high
data>>Data.IBSrefillTrap = IBSrefillTrap? high, low
data>>Data.GoodIBDisp = GoodIBDisp? high, low
data>>Data.ReadIB0 = ReadIB0? low, high
data>>Data.ReadIB1 = ReadIB1? low, high
data>>Data.WriteIBFront = WriteIBFront? high, low
data>>Data.OutIBPtr = OutIBPtr
]

```

```
-----  
and ALUHigh(addr, data) be  
-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    paS0 bit  
    paS1 bit  
    paS2 bit  
    paF1 bit  
    paF2 bit  
    pMem bit  
    Cycle3 bit  
    Cycle2 bit  
    blank bit  
  ]  
  
  structure Data:  
  [  
    aSh0 bit  
    aSh1 bit  
    aSh2 bit  
    aFh1 bit  
    aFh2 bit  
    ReadMD bit           //low true  
    blank bit 2  
    blank bit 8  
  ]  
  
  let paS0 = addr<<Addr.paS0 eq high  
  let paS1 = addr<<Addr.paS1 eq high  
  let paS2 = addr<<Addr.paS2 eq high  
  let paF1 = addr<<Addr.paF1 eq high  
  let paF2 = addr<<Addr.paF2 eq high  
  let pMem = addr<<Addr.pMem eq high  
  let Cycle3 = addr<<Addr.Cycle3 eq high  
  let Cycle2 = addr<<Addr.Cycle2 eq high  
  
  data>>Data.aSh0 = (pMem & Cycle3? false, paS0)? high, low  
  data>>Data.aSh1 = (pMem & Cycle3? true, paS1)? high, low  
  data>>Data.aSh2 = (pMem & Cycle3? true, paS2)? high, low  
  data>>Data.aFh1 = (pMem & Cycle3? true, paF1)? high, low  
  data>>Data.aFh2 = (pMem & Cycle3? true, paF2)? high, low  
  data>>Data.ReadMD = pMem & Cycle2? low, high  
  ]
```

```
-----  
and FX(addr, data) be  
-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    pFX bit 4  
    blank bit 5  
  ]  
  
  structure Data:  
  [  
    blank bit  
    WriteRH bit  
    Shift bit           //low true  
    CycleX bit         //low true  
    CinGetsPC16X bit   //low true  
    MapRefX bit        //low true  
    PopX bit  
    PushX bit  
    blank bit 8  
  ]  
  
  let FX = addr<<Addr.pFX  
  
  data>>Data.WriteRH = FX eq 9? high, low  
  data>>Data.Shift = FX eq 10? low, high  
  data>>Data.CycleX = FX eq 11? low, high  
  data>>Data.CinGetsPC16X = FX eq 12? low, high  
  data>>Data.MapRefX = FX eq 13? low, high  
  data>>Data.PopX = FX eq 14? high, low  
  data>>Data.PushX = FX eq 15? high, low  
  ]
```

```
//-----  
and FYZ(addr, data) be  
//-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    pFS01 bit 2  
    pFS23 bit 2  
    pfZ01 bit 2 =  
    [  
      pfZ0 bit  
      pfZ1 bit  
    ]  
    pfY0 bit  
    pfY1 bit  
    blank bit  
  ]  
  
  structure Data:  
  [  
    Zero bit           //low true  
    IB bit             //low true  
    Rot bit            //low true  
    Byte bit           //low true  
    Const bit          //low true  
    FourBitBr bit      //low true  
    TwoBitBr bit       //low true  
    OneBitBr bit       //low true  
    blank bit 8  
  ]  
  
  let pFS01 = addr<<Addr.pFS01  
  let pFS23 = addr<<Addr.pFS23  
  let pfZ01 = addr<<Addr.pfZ01  
  let pfZ0 = addr<<Addr.pfZ0 eq high  
  let pfY0 = addr<<Addr.pfY0 eq high  
  let pfY1 = addr<<Addr.pfY1 eq high  
  
  data>>Data.Zero = (pFS23 eq 1 % (pFS23 eq 3 & pfZ0))? low, high  
  data>>Data.IB = (pFS23 eq 3 & pfZ01 eq 3)? low, high  
  data>>Data.Rot = (pFS23 eq 0 & pfZ01 eq 3)? low, high  
  data>>Data.Byte = pFS01 eq 3? low, high  
  data>>Data.Const = pFS23 eq 1? low, high  
  data>>Data.FourBitBr = (pFS01 eq 0 & pfY0 & not pfY1)? low, high  
  data>>Data.TwoBitBr = (pFS01 eq 0 & pfY0)? low, high  
  data>>Data.OneBitBr = (pFS01 eq 0 & not pfY0)? low, high  
  ]
```

```
-----  
and FY1(addr, data) be  
-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    pfY bit 4  
    pfs01 bit 2  
    blank bit 3  
  ]  
  
  structure Data:  
  [  
    WriteDebA bit          //low true  
    WriteExtCtrl bit  
    ClrIntTrap bit        //low true  
    IBDisp bit  
    SetInterrupt bit  
    WriteStkP bit  
    WriteIB bit  
    CycleY bit            //low true  
    blank bit 8  
  ]  
  
  let pfY = addr<<Addr.pfY  
  let pfs01 = addr<<Addr.pfs01  
  
  data>>Data.WriteDebA = (pfs01 eq 2 & pfY eq 0)? low, high  
  data>>Data.WriteExtCtrl = (pfs01 eq 2 & pfY eq 1)? high, low  
  data>>Data.ClrIntTrap = (pfs01 eq 1 & pfY eq 2)? low, high  
  data>>Data.IBDisp = (pfs01 eq 1 & pfY eq 3)? high, low  
  data>>Data.SetInterrupt = (pfs01 eq 1 & pfY eq 4)? high, low  
  data>>Data.WriteStkP = (pfs01 eq 1 & pfY eq 5)? high, low  
  data>>Data.WriteIB = (pfs01 eq 1 & pfY eq 6)? high, low  
  data>>Data.CycleY = (pfs01 eq 1 & pfY eq 7)? low, high  
]
```

```
-----  
and FY2(addr, data) be  
-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    pfY bit 4  
    pfS01 bit 2  
    blank bit 3  
  ]  
  
  structure Data:  
  [  
    blank bit  
    MapRefY bit          //low true  
    blank bit  
    PushY bit  
    IORefY bit          //low true  
    WriteBank bit  
    BHEN bit  
    RawRef bit  
    blank bit 8  
  ]  
  
  let pfY = addr<<Addr.pfY  
  let pfS01 = addr<<Addr.pfS01  
  
  data>>Data.MapRefY = (pfS01 eq 1 & pfY eq 9)? low, high  
  data>>Data.PushY = (pfS01 eq 1 & pfY eq 11)? high, low  
  data>>Data.IORefY = ((pfS01 eq 1 % pfS01 eq 2) & pfY eq 12)? low, high  
  data>>Data.WriteBank = (pfS01 eq 1 & pfY eq 13)? high, low  
  data>>Data.BHEN = (pfS01 eq 2 & (pfY eq 12 % pfY eq 14 % pfY eq 15))? low, high  
  data>>Data.RawRef = ((pfS01 eq 1 % pfS01 eq 2) & pfY eq 14)? high, low  
]
```



```
//-----  
and FZ1(addr, data) be  
//-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    pfZ bit 4  
    pfs23 bit 2  
    blank bit 3  
  ]  
  
  structure Data:  
  [  
    ADRO bit  
    IBPtrGetsByte bit  
    IBPtrGetsWord bit  
    CInGetsPC16Z bit      //low true  
    IORefZ bit           //low true  
    PopZ bit  
    PushZ bit  
    AltUAddr bit  
    blank bit 8  
  ]  
  
  let pfZ = addr<<Addr.pfZ  
  let pfs23 = addr<<Addr.pfs23  
  
  data>>Data.ADRO = (pfs23 eq 3 & pfZ eq 0)? high, low  
  data>>Data.IBPtrGetsByte = (pfs23 eq 0 & pfZ eq 1)? high, low  
  data>>Data.IBPtrGetsWord = (pfs23 eq 0 & pfZ eq 2)? high, low  
  data>>Data.CInGetsPC16Z = (pfs23 eq 0 & pfZ eq 3)? low, high  
  data>>Data.IORefZ = (pfs23 eq 3 & pfZ eq 7)? low, high  
  data>>Data.PopZ = (pfs23 eq 0 & pfZ eq 5)? high, low  
  data>>Data.PushZ = (pfs23 eq 0 & pfZ eq 6)? high, low  
  data>>Data.AltUAddr = (pfs23 eq 0 & pfZ eq 7)? high, low  
]
```

```
//-----  
and FZ2(addr, data) be  
//-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    pfZ bit 4  
    pfS23 bit 2  
    blank bit 3  
  ]  
  
  structure Data:  
  [  
    ReadDebB bit          //low true  
    ReadExtStat bit       //low true  
    ReadMisc bit          //low true  
    ReadRH bit            //low true  
    blank bit  
    ReadIB bit  
    blank bit  
    IBHigh bit           //low true  
    blank bit 8  
  ]  
  
  let pfZ = addr<<Addr.pfZ  
  let pfS23 = addr<<Addr.pfS23  
  
  data>>Data.ReadDebB = (pfS23 eq 3 & pfZ eq 8)? low, high  
  data>>Data.ReadExtStat = (pfS23 eq 3 & pfZ eq 6)? low, high  
  data>>Data.ReadMisc = (pfS23 eq 3 & pfZ eq 10)? low, high  
  data>>Data.ReadRH = (pfS23 eq 3 & pfZ eq 11)? low, high  
  data>>Data.ReadIB = (pfS23 eq 3 & pfZ eq 13)? high, low  
  data>>Data.IBHigh = (pfS23 eq 3 & pfZ eq 15)? low, high  
]
```

```
-----  
and CPBank3632(addr, data) be  
-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    Bank bit 4  
    UseRom bit  
    blank bit 4  
  ]  
  
  structure Data:  
  [  
    Rom0CE bit          //high true, aka CS2  
    Rom0OE bit          //low true, aka CS1  
    Rom1CE bit          //high true, aka CS2  
    Rom1OE bit          //low true, aka CS1  
    MapFlags bit 2  
    blank bit 2  
    blank bit 8  
  ]  
  
  let Bank = addr<<Addr.Bank  
  let UseRom = addr<<Addr.UseRom  
  
  let Rom0CE, Rom0OE = false, false  
  let Rom1CE, Rom1OE = false, false  
  let MapFlags = 0  
  
  if UseRom then  
  [  
    if Bank eq 0 then Rom0CE, Rom0OE = true, true  
    if Bank eq 1 then Rom1CE, Rom1OE = true, true  
  ]  
  
  data>>Data.Rom0CE = Rom0CE? high, low  
  data>>Data.Rom0OE = Rom0OE? low, high  
  data>>Data.Rom1CE = Rom1CE? high, low  
  data>>Data.Rom1OE = Rom1OE? low, high  
  data>>Data.MapFlags = MapFlags  
]
```

```
//-----  
and CPBank2732(addr, data) be  
//-----  
[  
  structure Addr:  
  [  
    blank bit 7  
    Bank bit 4  
    UseRom bit  
    blank bit 4  
  ]  
  
  structure Data:  
  [  
    Rom0CE bit          //low true  
    Rom0OE bit          //low true  
    Rom1CE bit          //low true  
    Rom1OE bit          //low true  
    MapFlags bit 2  
    blank bit 2  
    blank bit 8  
  ]  
  
  let Bank = addr<<Addr.Bank  
  let UseRom = addr<<Addr.UseRom  
  
  let Rom0CE, Rom0OE = false, false  
  let Rom1CE, Rom1OE = false, false  
  let MapFlags = 0  
  
  if UseRom then  
  [  
    if Bank eq 0 then Rom0CE, Rom0OE = true, true  
    if Bank eq 1 then Rom1CE, Rom1OE = true, true  
  ]  
  
  data>>Data.Rom0CE = Rom0CE? low, high  
  data>>Data.Rom0OE = Rom0OE? low, high  
  data>>Data.Rom1CE = Rom1CE? low, high  
  data>>Data.Rom1OE = Rom1OE? low, high  
  data>>Data.MapFlags = MapFlags  
]
```

```
-----  
and Trap(addr, data) be  
-----  
[  
manifest  
  [   
    // These bits appear inverted on X[8-9] when fZ = XLow+Misc.  
    // If X[8-9] = zero then a control store parity error occurred.  
    stateIBEmpty = 0  
    stateStack = 1  
    stateInit = 2  
    stateNoTrap = 3  
    stateParity = 3  
  ]  
  
  structure Addr:  
  [   
    blank bit 7  
    CurrentState bit 2  
    TrapIn bit  
    IBEmptyTrap bit //low true  
    StackTrap bit  
    InitTrap bit //low true  
    ParityTrap bit  
    ClrIntTrap bit //low true  
    Cycle1 bit  
  ]  
  
  structure Data:  
  [   
    NextState bit 2  
    Trap bit  
    ParityLED bit //low true  
    ForceBank0 bit  
    blank bit 3  
    blank bit 8  
  ]  
  
  let CurrentState = addr<<Addr.CurrentState  
  let IBEmptyTrap = addr<<Addr.IBEmptyTrap eq low  
  let StackTrap = addr<<Addr.StackTrap eq high  
  let InitTrap = addr<<Addr.InitTrap eq low  
  let ParityTrap = addr<<Addr.ParityTrap eq high  
  let ClrIntTrap = addr<<Addr.ClrIntTrap eq low  
  let Cycle1 = addr<<Addr.Cycle1 eq high  
  let TrapIn = addr<<Addr.TrapIn eq high  
  
  let NextState = CurrentState  
  let Trap = false
```

```
// The Trap machine only remembers one trap. If multiple traps occur,
// only one of them is reported. The priority of reporting is:
//   InitTrap - highest priority
//   ParityTrap
//   StackTrap
//   IBEEmptyTrap - lowest priority
// If a trap occurs in an instruction which clears traps, the new trap still takes.
// The instruction at location 0 must read the trap type (XBus+Misc) and
// clear the trap (ClrIntTrap), or else another trap will occur.

// InitTrap causes a continuous Trap regardless of the cycle.
// The CP repeatedly executes the instruction at location 0.
// The Multibus FSM loops in Cycle 1.
// The control store bank is forced to 0.
// When InitTrap goes away, the processor takes off from location 0 in cycle 1.

// The instruction at location 0, which the CP repeatedly executes while
// Init is asserted, contains FY = ClrIntTrap. Unless inhibited, this will
// cause the trap machine to forget its mission 3 cycles before the processor
// is finally released from its chains. TrapIn detects this peculiar
// combination and remembers it long enough to inhibit ClrIntTrap until the last
// time that that magic instruction at location 0 is executed.

if ClrIntTrap & CurrentState eq stateInit & (TrapIn % not Cycle1) then ClrIntTrap = false

if ClrIntTrap then NextState = stateNoTrap
if IBEEmptyTrap & CurrentState eq stateNoTrap then NextState = stateIBEmpty
if StackTrap & (CurrentState eq stateNoTrap % CurrentState eq stateIBEmpty) then
  NextState = stateStack
if ParityTrap & CurrentState ne stateInit then NextState = stateParity
if InitTrap then NextState = stateInit

// Trap must be asserted during Cycle 2, so we must decide to assert it during Cycle 1.
// A Trap causes the address loaded into NIA at the end of cycle 2 to be zero.
// The instruction at location 0 is fetched in cycle 3 and executed in cycle 1.

if Cycle1 & (NextState ne stateNoTrap % ParityTrap) then Trap = true

// ParityTrap is a level (JK-FF) rather than a 1-cycle pulse like the rest of the traps.
// This is fortunate since the trap mechanism has only 2 state bits but has 5 states:
//   NoTrap, IBEEmpty, Stack, Parity, Init.

// InitTraps and ParityTraps go to location 0 in bank 0.
// All other traps go to location 0 in the current bank.
// This trap handler might just pass control to the trap handler in bank 0.

data>>Data.NextState = NextState
data>>Data.ParityLED = ParityTrap? low, high
data>>Data.ForceBank0 = (Trap & ParityTrap) % InitTrap? high, low
data>>Data.Trap = Trap? high, low
]
```

DCP-Ints.pa1
Last modified October 14, 1982 3:54 PM by Boggs

PALType 16R6

PinDefs

CK
/ClrIntTrap SetInterrupt In0 In1 In2 In3 OtherIn Low
GND /ReadInts
OtherOut /Trans /Out3 /Out2 /Out1 /Out0 /IFF Interrupt
PWR

BEGIN

Out0 + In0;
Out1 + In1;
Out2 + In2;
Out3 + In3;

Trans + In0 /Out0 + /In0 Out0 +
In1 /Out1 + /In1 Out1 +
In2 /Out2 + /In2 Out2 +
In3 /Out3 + /In3 Out3;

IF /Low THEN /OtherOut + /Trans;

IFF + /ClrIntTrap IFF + SetInterrupt + OtherIn + Trans;

IF /Low THEN /Interrupt + /IFF;

END

DCP-MarHigh.pal
Last modified February 21, 1983 6:45 PM by Boggs

PALType 16R6

PinDefs

CK
MapRef IORef YH0 YH1 YH2 YH3 YH4 RawRef
GND /ReadMax
MapFlag1 /AD14 /AD15 /AD16 /AD17 SpareOut1 SpareOut2 MapFlag0
PWR

BEGIN

AD14 + IORef YH4;
AD15 + RawRef YH3 + IORef /MapRef YH3;
AD16 + RawRef YH2 + IORef /MapRef YH2;
AD17 + RawRef YH1 + IORef /MapRef YH1;

END

DCP-MarLow.pa1
Last modified February 21, 1983 6:45 PM by Boggs

PALType 16R6

PinDefs

CK
MapRef IORef ADROin BHENin YH5 YH6 YH7 RawRef
GND /ReadMAX
MapFlag1 /AD11 /AD12 /AD13 /BHEN /ADRO SpareOut MapFlag0
PWR

BEGIN

AD11 † IORef YH7 † /IORef MapRef;
AD12 † IORef YH6;
AD13 † IORef YH5;
BHEN † BHENin;
ADRO † ADROin;

END

Page Numbers: Yes First Page: 1
 Columns: 2 Edge Margin: .8" Between Columns: .0"
 Heading:
 DCP-Rev-I.ps
 COMPONENTS:

--:	2	12	18			
16R6:	12	14				
26S09:	3	4				
26S10:	5					
27S03:	9					
27S07:	4					
27S27:	8	12	13			
27S29:	4	6	10	13		
2901C:	1					
2950A:	15					
64Kx8:	11					
851P:	16					
ALS576:	14					
ALS580:	14					
F93422:	3					
LS273:	15					
LS352:	9					
N276:	7	13				
N376:	13					
OSC:	15					
S00:	3	4	6	9	13	14
	15					
S08:	6	15				
S09:	13	16				
S10:	2	6	9	13		
S138:	13					
S151:	9					
S157:	10					
S182:	2					
S20:	9					
S240:	2	4	5	6	9	10
	12	13	15	16		
S244:	4	6	13	15		
S253:	2					
S257:	3	5	6			
S280:	7					
S32:	6	9	13	16		
S373:	6					
S374:	2	4	6	7	10	12
	16					
S38:	2					
S86:	2	16				
Spare20:	16					

SIGNAL NAMES:

+:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
12BitCarry:	1(1)	2(1)				
12BitGen':	1(1)	2(1)				
12BitProp':	1(1)	2(1)				
18BitBrEn':	8(1)	9(1)				
28BitBrEn':	8(1)	9(2)				
2xC1k':	13(3)	15(2)				
48BitBrEn':	8(1)	9(2)				
48BitCarry:	1(1)	2(1)	9(1)			
48BitGen':	1(1)	2(1)				
48BitProp':	1(1)	2(1)				
88BitCarry:	1(1)	2(2)	9(1)			
88BitGen':	1(1)	2(1)				
88BitProp':	1(1)	2(1)				
aD.0:	1(4)	2(3)	7(1)			
aD.0':	2(3)					
aD.1:	1(4)	2(1)	7(1)			
AD10/:	14(2)	17(1)				
AD11/:	14(1)	17(1)				
AD12/:	14(1)	17(1)				
AD13/:	14(1)	17(1)				
AD14/:	14(1)	17(1)				
AD15/:	14(1)	17(1)				
AD16/:	14(1)	17(1)				
AD17/:	14(1)	17(1)				
ADR0:	8(1)	14(1)				
ADR0/:	14(1)	17(1)				
ADR1/:	14(2)	17(1)				
ADR2/:	14(2)	17(1)				
ADR3/:	14(2)	17(1)				
ADR4/:	14(2)	17(1)				
ADR5/:	14(2)	17(1)				
ADR6/:	14(2)	17(1)				
ADR7/:	14(2)	17(1)				
ADR8/:	14(2)	17(1)				
ADR9/:	14(2)	17(1)				
ADRA/:	14(2)	17(1)				
ADRB/:	14(2)	17(1)				
ADRC/:	14(2)	17(1)				
ADRD/:	14(2)	17(1)				
ADRE/:	14(2)	17(1)				
ADRF/:	14(2)	17(1)				
aF.0:	1(4)	7(1)				
aFh.1:	1(2)	8(1)				
aFh.2:	1(2)	8(1)				
aFT.1:	1(2)	7(1)				

aF1.2:	1(2)	2(1)	7(1)				
AltBoot:	15(1)	17(1)					
AltUAddr:	3(1)	8(1)					
aSh.0:	1(2)	8(1)					
aSh.1:	1(2)	8(1)					
aSh.2:	1(2)	8(1)					
aS1.0:	1(2)	7(1)					
aS1.1:	1(2)	7(1)					
aS1.2:	1(2)	7(1)					
Bank.0:	10(1)	17(1)					
Bank.1:	10(1)	17(1)					
Bank.2:	10(1)	17(1)					
Bank.3:	10(1)	11(6)	17(1)				
BCLK:	13(2)						
BCLK/:	13(2)	17(1)					
BHEN:	8(1)	14(1)					
BHEN/:	14(1)	17(1)					
BlankMP':	15(1)	17(1)					
Boot':	13(1)	16(1)	17(1)				
BPRN/:	13(1)	17(1)					
BUSY:	13(2)						
BUSY/:	13(2)	17(1)					
C.0:	9(1)	10(1)					
C.1:	9(1)	10(1)					
C.2:	9(1)	10(1)					
C.3:	9(1)	10(1)					
CarryIn:	1(1)	2(5)					
CarryOut:	1(1)	2(1)	9(1)				
CIn:	2(1)	3(2)	7(1)				
CIn+PC16X':	2(1)	8(1)					
CIn+PC16Z':	2(1)	8(1)					
Clk'a:	1(4)	7(1)	10(1)	15(1)			
Clk'b:	8(2)	12(1)	15(1)				
Clk'c:	3(1)	4(1)	12(1)	15(2)	16(1)		
ClrIntTrap':	7(1)	8(1)	12(2)				
Cycle1:	6(1)	12(1)	13(1)	17(1)			
Cycle2:	8(1)	9(1)	13(1)	17(1)			
Cycle3:	8(1)	13(1)	17(1)				
CycleX':	2(1)	8(1)					
CycleY':	2(1)	8(1)					
DAT0/:	14(2)	17(1)					
DAT1/:	14(2)	17(1)					
DAT2/:	14(2)	17(1)					
DAT3/:	14(2)	17(1)					
DAT4/:	14(2)	17(1)					
DAT5/:	14(2)	17(1)					
DAT6/:	14(2)	17(1)					
DAT7/:	14(2)	17(1)					
DAT8/:	14(2)	17(1)					
DAT9/:	14(2)	17(1)					
DATA/:	14(2)	17(1)					
DATB/:	14(2)	17(1)					
DATC/:	14(2)	17(1)					
DATD/:	14(2)	17(1)					
DATE/:	14(2)	17(1)					
DATF/:	14(2)	17(1)					
DebAFull:	15(2)	17(1)					
DebBFull:	15(2)	17(1)					
DebData.0:	15(1)	17(1)					
DebData.1:	15(1)	17(1)					
DebData.2:	15(1)	17(1)					
DebData.3:	15(1)	17(1)					
DebData.4:	15(1)	17(1)					
DebData.5:	15(1)	17(1)					
DebData.6:	15(1)	17(1)					
DebData.7:	15(1)	17(1)					
dGoodIBDisp:	6(1)	17(1)					
DoIt:	13(1)	15(1)	17(1)				
DP.0:	15(1)	17(1)					
DP.1:	15(1)	17(1)					
DP.2:	15(1)	17(1)					
DP.3:	15(1)	17(1)					
EnC2Funs:	6(2)	13(1)					
EnU:	3(1)	7(1)					
F.0:	1(1)	9(1)					
Feq0:	1(4)	2(1)	9(1)				
Fne0:	2(1)	9(1)					
ForceBank0:	10(1)	12(1)					
fX.0:	7(1)	9(1)					
fX.1:	7(1)	9(1)					
fX.2:	7(1)	9(1)					
fX.3:	7(1)	9(1)					
fY.0:	5(1)	7(1)					
fY.1:	5(1)	7(1)	9(3)				
fY.2:	5(1)	7(1)	9(4)				
fY.3:	5(1)	7(1)	9(4)				
fZ.0:	5(1)	7(1)					
fZ.1:	5(1)	7(1)					
fZ.2:	5(2)	6(1)	7(1)				
fZ.3:	5(2)	7(1)					
Gnd:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)	
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)	
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)	
GND:	10(1)	17(21)					
GoodIBDisp:	6(1)	10(1)					
IB.0:	6(1)	10(1)					
IB.1:	6(1)	10(1)					
IB.2:	6(1)	10(1)					
IB.3:	6(1)	10(1)					
IB.4:	6(1)	10(1)					
IB.5:	6(1)	10(1)					

IB.6:	6(1)	10(1)		
IB.7:	6(1)	10(1)		
IBDisp:	6(1)	8(1)		
IBEmpty':	6(2)			
IBEmptyTrap':	6(1)	12(1)		
IBHigh':	6(1)	8(1)		
IBPtr.1:	6(1)	10(1)		
IBPtr+Byte:	6(1)	8(1)		
IBPtr+Word:	6(1)	8(1)		
IBRefillTrap:	6(1)	10(1)		
IncMP':	15(1)	17(1)		
INIT/:	13(2)	17(1)		
InitTrap':	12(1)	13(1)	15(1)	
INT0/:	12(1)	17(1)		
INT1/:	12(1)	17(1)		
INT2/:	12(1)	17(1)		
INT3/:	12(1)	17(1)		
INT4/:	12(1)	17(1)		
INT5/:	12(1)	17(1)		
INT6/:	12(1)	17(1)		
INT7/:	12(1)	17(1)		
Interrupt:	6(1)	9(1)	10(1)	12(1)
IOCmd:	13(2)			
IORC/:	13(1)	17(1)		
IORef:	13(1)	14(2)		
IORefY':	8(1)	13(1)		
IORefZ':	8(1)	13(1)		
IOWC/:	13(1)	17(1)		
Link.0':	9(2)			
Link.1':	9(2)			
Link.2':	9(2)			
Link.3':	9(2)			
MapFlag.0:	10(1)	14(2)		
MapFlag.1:	10(1)	14(2)		
MapRef:	13(1)	14(2)		
MapRefX':	8(1)	13(1)		
MapRefY':	8(1)	13(1)		
MapPageCross':	6(1)	9(1)		
Master':	13(3)	15(1)		
Mem:	6(1)	7(1)	13(1)	
MRDC/:	13(1)	17(1)		
MWTC/:	13(1)	17(1)		
NIA.0:	10(1)	11(6)	17(1)	
NIA.1:	10(1)	11(6)	17(1)	
NIA.10:	9(1)	10(1)	11(6)	17(1)
NIA.11:	9(1)	10(1)	11(6)	17(1)
NIA.2:	10(1)	11(6)	17(1)	
NIA.3:	10(1)	11(6)	17(1)	
NIA.4:	10(1)	11(6)	17(1)	
NIA.5:	10(1)	11(6)	17(1)	
NIA.6:	10(1)	11(6)	17(1)	
NIA.7:	9(1)	10(1)	11(6)	17(1)
NIA.8:	9(1)	10(1)	11(6)	17(1)
NIA.9:	9(1)	10(1)	11(6)	17(1)
Overflow:	1(1)	9(1)		
paD.0:	7(2)	11(2)	17(1)	
paD.1:	7(2)	11(2)	17(1)	
paF.0:	7(2)	11(2)	17(1)	
paF.1:	7(2)	8(1)	11(2)	17(1)
paF.2:	7(2)	8(1)	11(2)	17(1)
PageCross:	2(1)	6(1)	9(1)	
ParityLED':	12(2)			
ParityTrap:	7(1)	12(1)		
paS.0:	7(2)	8(1)	11(2)	17(1)
paS.1:	7(2)	8(1)	11(2)	17(1)
paS.2:	7(2)	8(1)	11(2)	17(1)
PC16':	2(1)	9(1)		
pCIn:	7(2)	11(2)	17(1)	
pEnU:	7(2)	11(2)	17(1)	
pEP:	7(2)	11(2)	17(1)	
pfS.0:	7(1)	8(3)	11(2)	17(1)
pfS.1:	7(1)	8(3)	11(2)	17(1)
pfS.2:	3(1)	7(1)	8(3)	11(2)
pfS.3:	7(1)	8(3)	11(2)	17(1)
pfX.0:	7(2)	8(1)	11(2)	17(1)
pfX.1:	7(2)	8(1)	11(2)	17(1)
pfX.2:	7(2)	8(1)	11(2)	17(1)
pfX.3:	7(2)	8(1)	11(2)	17(1)
pfY.0:	7(2)	8(3)	11(2)	17(1)
pfY.1:	7(2)	8(3)	11(2)	17(1)
pfY.2:	7(2)	8(2)	11(2)	17(1)
pfY.3:	7(2)	8(2)	11(2)	17(1)
pfZ.0:	3(1)	7(2)	8(3)	11(2)
pfZ.1:	3(1)	7(2)	8(3)	11(2)
pfZ.2:	3(1)	7(2)	8(2)	11(2)
pfZ.3:	3(1)	7(2)	8(2)	11(2)
pMem:	7(2)	8(1)	11(2)	17(1)
pNIA.0:	7(1)	10(1)	11(2)	17(1)
pNIA.1:	7(1)	10(1)	11(2)	17(1)
pNIA.10':	7(1)	9(1)	11(2)	17(1)
pNIA.11':	7(1)	9(1)	11(2)	17(1)
pNIA.2:	7(1)	10(1)	11(2)	17(1)
pNIA.3:	7(1)	10(1)	11(2)	17(1)
pNIA.4:	7(1)	10(1)	11(2)	17(1)
pNIA.5:	7(1)	10(1)	11(2)	17(1)
pNIA.6:	7(1)	10(1)	11(2)	17(1)
pNIA.7:	7(1)	10(1)	11(2)	17(1)
pNIA.8':	7(1)	9(1)	11(2)	17(1)
pNIA.9':	7(1)	9(1)	11(2)	17(1)
PopX:	4(1)	8(1)		
PopZ:	4(1)	8(1)		

prA.0:	3(1)	7(2)	11(2)	17(1)			
prA.1:	3(1)	7(2)	11(2)	17(1)			
prA.2:	3(1)	7(2)	11(2)	17(1)			
prA.3:	3(1)	7(2)	11(2)	17(1)			
prB.0:	7(2)	11(2)	17(1)				
prB.1:	7(2)	11(2)	17(1)				
prB.2:	7(2)	11(2)	17(1)				
prB.3:	7(2)	11(2)	17(1)				
preC1k:	3(1)	4(1)	6(2)	7(1)	9(1)	14(2)	
	15(2)						
PU:	5(1)	10(1)	13(2)	16(1)			
PushX:	4(1)	8(1)					
PushY:	4(1)	8(1)					
PushZ:	4(1)	8(1)					
Q.0:	1(1)	2(2)					
Q.15:	1(1)	2(1)					
Q.7:	1(2)						
R.0:	1(1)	2(2)					
R.15:	1(1)	2(3)					
R.7:	1(2)						
rA.0:	1(4)	7(1)					
rA.1:	1(4)	7(1)					
rA.2:	1(4)	7(1)					
rA.3:	1(4)	7(1)					
RawC1k:	15(1)	17(1)					
RawRef:	8(1)	14(2)					
rB.0:	1(4)	4(1)	7(1)				
rB.1:	1(4)	4(1)	7(1)				
rB.2:	1(4)	4(1)	7(1)				
rB.3:	1(4)	4(1)	7(1)				
ReadCmd:	13(2)						
ReadDebA':	15(1)	16(1)	17(1)				
ReadDebB':	8(1)	15(1)					
ReadExtStat':	8(1)	12(1)	15(1)				
ReadIB:	6(1)	8(1)					
ReadIB0':	6(2)						
ReadIB1':	6(2)						
ReadMap':	13(1)	14(1)					
ReadMAR':	13(1)	14(1)					
ReadMax':	13(1)	14(1)					
ReadMD':	8(1)	14(1)					
ReadMDR':	13(1)	14(1)					
ReadMisc':	4(1)	8(1)	12(1)				
ReadNIA:	10(1)	16(1)	17(1)				
ReadRH':	4(1)	8(1)					
RomOCE':	10(1)	11(3)					
RomOOE':	10(1)	11(3)					
RomICE':	10(1)	11(3)					
RomIOE':	10(1)	11(3)					
Run:	15(1)	16(1)	17(1)				
SetInterrupt:	8(1)	12(1)					
sn:	1(4)	2(1)					
Shift':	2(2)	8(1)					
StackTrap:	4(1)	12(1)					
StkP.0:	3(1)	4(1)					
StkP.1:	3(1)	4(1)					
StkP.2:	3(1)	4(1)					
StkP.3:	3(1)	4(1)					
Trap:	10(1)	12(1)					
UAddr.0:	3(2)						
UAddr.1:	3(2)						
UAddr.2:	3(2)						
UAddr.3:	3(2)						
UAddr.4:	3(2)						
UAddr.5:	3(2)						
UAddr.6:	3(2)						
UAddr.7:	3(2)						
UseRom:	10(1)	16(1)	17(1)				
VCC:	1(4)	2(4)	11(18)	12(1)	15(1)	16(2)	
	17(9)	18(4)					
WriteBank:	8(1)	10(1)					
WriteCmd:	13(2)						
WriteDebA':	8(1)	15(1)					
WriteDebB':	15(1)	16(1)	17(1)				
WriteExtCtrl:	8(1)	15(1)					
WriteIB:	6(2)	8(1)					
WriteIBFront:	6(2)						
WriteMAR:	13(1)	14(1)					
WriteMD:	13(1)	14(1)					
WriteMDR:	13(1)	14(1)					
WriteRH:	4(1)	8(1)					
WriteStkP:	4(1)	8(1)					
X.0:	1(1)	3(1)	5(2)	6(1)	9(1)	12(1)	
	14(1)						
X.1:	1(1)	3(1)	5(2)	6(1)	12(1)	14(1)	
X.10:	1(1)	3(1)	4(2)	5(2)	6(3)	9(1)	
	14(1)	15(1)					
X.11:	1(1)	3(1)	4(2)	5(2)	6(3)	9(1)	
	14(1)	15(1)					
X.12:	1(1)	3(1)	4(3)	5(2)	6(2)	9(2)	
	14(1)	15(2)					
X.13:	1(1)	3(1)	4(3)	5(2)	6(2)	9(2)	
	14(1)	15(2)					
X.14:	1(1)	3(1)	4(3)	5(2)	6(2)	9(1)	
	14(1)	15(2)					
X.15:	1(1)	3(1)	4(3)	5(2)	6(2)	9(2)	
	14(1)	15(2)					
X.2:	1(1)	3(1)	5(2)	6(1)	12(1)	14(1)	
X.3:	1(1)	3(1)	5(2)	6(1)	12(1)	14(1)	
X.4:	1(1)	3(1)	5(2)	6(1)	9(1)	12(1)	
	14(1)						

X.5:	1(1)	3(1)	5(2)	6(1)	12(1)	14(1)
X.6:	1(1)	3(1)	5(2)	6(1)	12(1)	14(1)
X.7:	1(1)	3(1)	5(2)	6(1)	12(1)	14(1)
X.8:	1(1)	3(1)	4(2)	5(2)	6(2)	9(1)
	12(1)	14(1)	15(1)			
X.9:	1(1)	3(1)	4(2)	5(2)	6(2)	9(1)
	12(1)	14(1)	15(1)			
XACK/:	13(1)	17(1)				
XBus+Rot':	5(1)	8(1)				
XHigh+0':	5(1)	8(1)				
XLow+Byte':	5(1)	8(1)				
XLow+Const':	5(1)	8(1)				
XLow+IB':	6(2)	8(1)				
Y.0:	1(1)	3(1)	5(1)	14(3)		
Y.1:	1(1)	3(1)	5(1)	14(3)		
Y.10:	1(1)	3(1)	5(2)	14(2)	15(1)	
Y.11:	1(1)	3(1)	5(2)	14(2)	15(1)	
Y.12:	1(1)	3(2)	4(1)	5(2)	9(1)	10(1)
	14(2)	15(1)				
Y.13:	1(1)	3(2)	4(1)	5(2)	9(1)	10(1)
	14(2)	15(1)				
Y.14:	1(1)	3(2)	4(1)	5(2)	9(1)	10(1)
	14(2)	15(1)				
Y.15:	1(1)	3(2)	4(1)	5(2)	9(1)	10(1)
	14(2)	15(1)				
Y.2:	1(1)	3(1)	5(1)	14(3)		
Y.3:	1(1)	3(1)	5(1)	14(3)		
Y.4:	1(1)	3(1)	5(2)	14(3)		
Y.5:	1(1)	3(1)	5(2)	14(3)		
Y.6:	1(1)	3(1)	5(2)	14(3)		
Y.7:	1(1)	3(1)	5(2)	14(3)		
Y.8:	1(1)	3(1)	5(2)	14(2)	15(1)	
Y.9:	1(1)	3(1)	5(2)	14(2)	15(1)	
YH.0:	4(1)	14(2)				
YH.1:	4(1)	14(2)				
YH.2:	4(1)	14(2)				
YH.3:	4(1)	14(2)				
YH.4:	4(1)	14(2)				
YH.5:	4(1)	14(2)				
YH.6:	4(1)	14(2)				
YH.7:	4(1)	14(2)				
ZeroMP':	15(1)	17(1)				

-/2/J:

#c1	#c10	#c100	#c101	#c102	#c103	#c104	#c105
#c106	#c107	#c108	#c109	#c11	#c110	#c111	#c112
#c113	#c114	#c115	#c12	#c13	#c14	#c15	#c16
#c17	#c18	#c19	#c2	#c20	#c21	#c22	#c23
#c24	#c25	#c26	#c27	#c28	#c29	#c3	#c30
#c31	#c32	#c33	#c34	#c35	#c36	#c37	#c38
#c39	#c4	#c40	#c41	#c42	#c43	#c44	#c45
#c46	#c47	#c48	#c49	#c5	#c50	#c51	#c52
#c53	#c54	#c55	#c56	#c57	#c58	#c59	#c6
#c60	#c61	#c62	#c63	#c64	#c66	#c67	#c68
#c69	#c7	#c70	#c71	#c72	#c73	#c74	#c75
#c76	#c77	#c78	#c79	#c8	#c80	#c81	#c82
#c83	#c84	#c85	#c86	#c87	#c88	#c89	#c9
#c90	#c91	#c92	#c93	#c94	#c95	#c96	#c97
#c98	#c99	#11	#r2	#r3	#r4	#r5	

16R6/20/N:

#u112	#u113	#u52	#u63
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64Kx8/28/N6W:

#u1	#u10	#u11	#u12	#u13	#u14	#u15	#u2
#u3	#u4	#u5	#u6				

74276/20/N:

#u94

74376/16/N:

#u82	#u83
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74ALS576/20/N:

#u108	#u109	#u110	#u111	#u97	#u98
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74ALS580/20/N:

#u100	#u99
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74LS273/20/N:

#u30

74LS352/16/N:

#u56

74S00/14/N:

#u64	#u95
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74S08/14/N:

#u53

74S09/14/N:

#u105

74S10/14/N:

#u57	#u84
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74S138/16/N:

#u107

74S151/16/N:

#u24	#u34	#u45
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74S157/16/N:

#u32	#u33	#u42	#u44
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74S182/16/N:

#u87

74S20/14/N:

#u46

74S240/20/N:

#u104	#u31	#u86
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74S244/20/N:

#u103	#u47	#u96
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74S253/16/N:

#u60

74S257/16/N:

#u43 #u55 #u88 #u92
74S280/14/N:
#u16 #u18 #u19 #u21 #u7 #u9
74S32/14/N:
#u106 #u59
74S373/20/N:
#u61 #u62
74S374/20/N:
#u22 #u23 #u25 #u26 #u27 #u29 #u50 #u54
#u75 #u85
74S38/14/N:
#u48
74S86/14/N:
#u49
8SIP/8/J1W:
#r1
93422/22/F4W:
#u78 #u79 #u80 #u81
AMD25S09/16/N:
#u115 #u91 #u93
AMD25S10/16/N:
#u76 #u77 #u89 #u90
AMD27S03/16/N:
#u58
AMD27S07/16/N:
#u101 #u102
AMD27S27/22/N4W:
#u35 #u36 #u37 #u38 #u39 #u40 #u41 #u71
#u73 #u74
AMD27S29/20/N:
#u114 #u28 #u51 #u72
AMD2901C/40/J6W:
#u66 #u67 #u68 #u69
AMD2950/28/J6W:
#u70
OSCILLATOR/14/N:
#u65
Spare20/20/J:
#u17 #u20 #u8

Universal
;File=DCP-Rev-I.sil Rev=I Date=10/15/84 Page=00 Reference -MARKED BUILT-
;File=DCP01.sil Rev=I Date=4/22/84 Page=01 -MARKED BUILT-
;File=DCP02.sil Rev=I Date=4/22/84 Page=02 -MARKED BUILT-
;File=DCP03.sil Rev=I Date=6/20/83 Page=03 -MARKED BUILT-
;File=DCP04.sil Rev=I Date=6/29/83 Page=04 -MARKED BUILT-
;File=DCP05.sil Rev=I Date=6/20/83 Page=05 -MARKED BUILT-
;File=DCP06.sil Rev=I Date=6/20/83 Page=06 -MARKED BUILT-
;File=DCP07.sil Rev=I Date=4/22/84 Page=07 -MARKED BUILT-
;File=DCP08.sil Rev=I Date=6/29/83 Page=08 -MARKED BUILT-
;File=DCP09.sil Rev=I Date=4/22/84 Page=09 -MARKED BUILT-
;File=DCP10.sil Rev=I Date=4/22/84 Page=10 -MARKED BUILT-
;File=DCP11.sil Rev=I Date=4/22/84 Page=11 -MARKED BUILT-
;File=DCP12.sil Rev=I Date=10/15/84 Page=12 -MARKED BUILT-
;File=DCP13.sil Rev=I Date=10/15/84 Page=13 -MARKED BUILT-
;File=DCP14.sil Rev=I Date=4/22/84 Page=14 -MARKED BUILT-
;File=DCP15.sil Rev=I Date=4/22/84 Page=15 -MARKED BUILT-
;File=DCP16.sil Rev=I Date=10/15/84 Page=16 MARKED BUILT
;File=DCP17.sil Rev=I Date=10/15/84 Page=17 -MARKED BUILT-
;File=DCP18.sil Rev=I Date=4/22/84 Page=18 -MARKED BUILT-
;File=DCP19.sil Rev=I Date=6/29/83 Page=19 Reference -MARKED BUILT-
;File=DCP20.sil Rev=I Date=4/22/84 Page=20 Reference -MARKED BUILT-
;File=DCP21.sil Rev=I Date=10/15/84 Page=21 Reference -MARKED BUILT-
;File=DCP22.sil Rev=I Date=10/15/84 Page=22 Reference -MARKED BUILT-
;File=DCP23.sil Rev=I Date=4/22/84 Page=23 Reference -MARKED BUILT-
; Implicitly generated wiring ...

#c1: (-/2/J) ;
#c10: (-/2/J) ;
#c100: (-/2/J) ;
#c101: (-/2/J) ;
#c102: (-/2/J) ;
#c103: (-/2/J) ;
#c104: (-/2/J) ;
#c105: (-/2/J) ;
#c106: (-/2/J) ;
#c107: (-/2/J) ;
#c108: (-/2/J) ;
#c109: (-/2/J) ;
#c11: (-/2/J) ;
#c110: (-/2/J) ;
#c111: (-/2/J) ;
#c112: (-/2/J) ;
#c113: (-/2/J) ;
#c114: (-/2/J) ;
#c115: (-/2/J) ;
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#c17: (-/2/J) ;
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#c20: (-/2/J) ;
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#c6: (-/2/J) ;
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#c61: (-/2/J) ;

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#c63: (-/2/J) ;
#c64: (-/2/J) ;
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#c92: (-/2/J) ;
#c93: (-/2/J) ;
#c94: (-/2/J) ;
#c95: (-/2/J) ;
#c96: (-/2/J) ;
#c97: (-/2/J) ;
#c98: (-/2/J) ;
#c99: (-/2/J) ;
#r1: (8SIP8/J1W) ;
#r2: (-/2/J) ;
#r3: (-/2/J) ;
#r4: (-/2/J) ;
#r5: (-/2/J) ;
#u1: (64Kx8/28/N6W) ;
#u10: (64Kx8/28/N6W) ;
#u100: (74ALS589/20/N) ;
#u101: (AMD27S07/16/N) ;
#u102: (AMD27S07/16/N) ;
#u103: (74S244/20/N) ;
#u104: (74S240/20/N) ;
#u105: (74S09/14/N) ; 8,9,10,11,12,13
#u106: (74S32/14/N) ; 11,12,13
#u107: (74S138/16/N) ; 7,9,14,15
#u108: (74ALS576/20/N) ;
#u109: (74ALS576/20/N) ;
#u11: (64Kx8/28/N6W) ;
#u110: (74ALS576/20/N) ;
#u111: (74ALS576/20/N) ;
#u112: (16R6/20/N) ; 18
#u113: (16R6/20/N) ; 17,18
#u114: (AMD27S29/20/N) ; 7,8,9
#u115: (AMD25S09/16/N) ;
#u12: (64Kx8/28/N6W) ;
#u13: (64Kx8/28/N6W) ;
#u14: (64Kx8/28/N6W) ;
#u15: (64Kx8/28/N6W) ;
#u16: (74S280/14/N) ; 3,5
#u17: (Spare20/20/J) ; 1,2,3,4,5,6,7,8,9,11,12,13,14,15,16,17,18,19
#u18: (74S280/14/N) ; 3,5
#u19: (74S280/14/N) ; 3,5
#u2: (64Kx8/28/N6W) ;
#u20: (Spare20/20/J) ; 1,2,3,4,5,6,7,8,9,11,12,13,14,15,16,17,18,19
#u21: (74S280/14/N) ; 3,5
#u22: (74S374/20/N) ;
#u23: (74S374/20/N) ;
#u24: (74S151/16/N) ; 1,5
#u25: (74S374/20/N) ;
#u26: (74S374/20/N) ;
#u27: (74S374/20/N) ; 2
#u28: (AMD27S29/20/N) ; 13,14
#u29: (74S374/20/N) ;
#u3: (64Kx8/28/N6W) ;
#u30: (74LS273/20/N) ; 12
#u31: (74S240/20/N) ; 9,11
#u32: (74S157/16/N) ;
#u33: (74S157/16/N) ;
#u34: (74S151/16/N) ; 5
#u35: (AMD27S27/22/N4W) ; 7
#u36: (AMD27S27/22/N4W) ;
#u37: (AMD27S27/22/N4W) ; 14,15
#u38: (AMD27S27/22/N4W) ;
#u39: (AMD27S27/22/N4W) ; 7,9
#u4: (64Kx8/28/N6W) ;
#u40: (AMD27S27/22/N4W) ;
#u41: (AMD27S27/22/N4W) ; 12,14
#u42: (74S157/16/N) ;
#u43: (74S257/16/N) ;
#u44: (74S157/16/N) ;

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#u45: (74S151/16/N) ; 1,5
#u46: (74S20/14/N) ; 3,11
#u47: (74S244/20/N) ;
#u43: (74S38/14/N) ;
#u49: (74S86/14/N) ; 11,12,13
#u5: (64Kx8/28/NGW) ;
#u50: (74S374/20/N) ; 18,19
#u51: (AMD27S29/20/N) ;
#u52: (16R6/20/N) ; 12,13,18
#u53: (74S08/14/N) ;
#u54: (74S374/20/N) ;
#u55: (74S257/16/N) ;
#u56: (74LS352/16/N) ; 3,13
#u57: (74S10/14/N) ;
#u58: (AMD27S03/16/N) ;
#u59: (74S32/14/N) ;
#u6: (64Kx8/28/NGW) ;
#u60: (74S253/16/N) ;
#u61: (74S373/20/N) ;
#u62: (74S373/20/N) ;
#u63: (16R6/20/N) ; 13,18,19
#u64: (74S00/14/N) ;
#u65: (OSCILLATOR/14/N) ; 1,2,3,4,5,6,9,10,11,12,13
#u66: (AMD2901C/40/J6W) ; 31,33,34
#u67: (AMD2901C/40/J6W) ; 31,33,34
#u68: (AMD2901C/40/J6W) ; 32,35
#u69: (AMD2901C/40/J6W) ; 31,33,34
#u7: (74S280/14/N) ; 3,5
#u70: (AMD2950/28/J6W) ;
#u71: (AMD27S27/22/N4W) ; 13,14,15
#u72: (AMD27S29/20/N) ;
#u73: (AMD27S27/22/N4W) ; 13,14,15
#u74: (AMD27S27/22/N4W) ;
#u75: (74S374/20/N) ;
#u76: (AMD25S10/16/N) ;
#u77: (AMD25S10/16/N) ;
#u78: (93422/22/F4W) ;
#u79: (93422/22/F4W) ;
#u8: (Spare20/20/J) ; 1,2,3,4,5,6,7,8,9,11,12,13,14,15,16,17,18,19
#u80: (93422/22/F4W) ;
#u81: (93422/22/F4W) ;
#u82: (74376/16/N) ;
#u83: (74376/16/N) ;
#u84: (74S10/14/N) ;
#u85: (74S374/20/N) ;
#u86: (74S240/20/N) ;
#u87: (74S182/16/N) ; 5,6,7,10
#u88: (74S257/16/N) ;
#u89: (AMD25S10/16/N) ;
#u9: (74S280/14/N) ; 3,5
#u90: (AMD25S10/16/N) ;
#u91: (AMD25S09/16/N) ;
#u92: (74S257/16/N) ;
#u93: (AMD25S09/16/N) ;
#u94: (74276/20/N) ;
#u95: (74S00/14/N) ;
#u96: (74S244/20/N) ;
#u97: (74ALS576/20/N) ;
#u98: (74ALS576/20/N) ;
#u99: (74ALS580/20/N) ;
@

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CALIBRATE: <1> ; INSTALL welder nose, board wiring side up ...
#TopRight {0,0} #TopLeft {0,0} #? {0,0} #? {0,0}

12BitCarry: <382> (196)
#u87.9o {204,92} #u68.29i {24,108}

12BitGen': <364> (148)
#u87.14i {204,72} #u67.32o {80,96}

12BitProp': <337> (140)
#u87.15i {204,68} #u67.35o {80,84}

1BitBrEn': <324> (100)
#u34.7i {220,168} #u36.15o {124,172}

2BitBrEn': <44> (88)
#u36.14o {124,176} #u45.7i {188,168} #u24.7i {204,168}

2xClk': <31> (1052)
#u73.16i {916,168} #u74.16i {896,168} #u31.12o {280,176} #u70.24i {296,216}
#u82.9i {44,228} #u83.9i {28,228} #u94.8i {32,172} #u94.13i {44,172}

4BitBrEn': <53> (228)
#u56.15i {312,148} #u56.1i {300,144} #u36.13o {124,180}

4BitCarry: <328> (288)
#u66.29i {52,108} #u87.12o {204,80} #u34.12i {232,160}

4BitGen': <326> (108)
#u87.3i {192,72} #u69.32o {108,96}

4BitProp': <318> (92)
#u87.4i {192,76} #u69.35o {108,84}

8BitCarry: <299> (248)
#u67.29i {80,108} #u49.10i {124,80} #u87.11o {204,84} #u34.15i {232,148}

8BitGen': <371> (172)
#u87.1i {192,64} #u66.32o {52,96}

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8BitProp': <366> (156)
 #u87.2i {192,68} #u66.35o {52,84}

aD.0: <165> (844)
 #u68.7i {0,88} #u66.7i {28,88} #u67.7i {56,88} #u69.7i {84,88}
 #u86.17i {140,76} #u48.4i {176,76} #u60.15i {220,68} #u25.16o {812,80}

aD.0': <179> (88)
 #u86.3o {128,72} #u48.1i {176,64} #u60.1i {208,64}

aD.1: <164> (824)
 #u68.5i {0,80} #u66.5i {28,80} #u67.5i {56,80} #u69.5i {84,80}
 #u60.2i {208,68} #u25.19o {812,68}

AD10/: <198> (388)
 #u108.19o {188,204} #u97.19o {156,204} E128 {0,4}

AD11/: <418> (340)
 E130 {8,4} #u112.13o {124,228}

AD12/: <417> (328)
 E132 {16,4} #u112.14o {124,224}

AD13/: <410> (316)
 E134 {24,4} #u112.15o {124,220}

AD14/: <422> (356)
 E257 {4,8} #u113.13o {140,228}

AD15/: <420> (348)
 E258 {8,8} #u113.14o {140,224}

AD16/: <450> (584)
 E255 {508,4} #u113.15o {140,220}

AD17/: <421> (348)
 E256 {0,8} #u113.16o {140,216}

ADR0: <327> (108)
 #u112.4i {112,212} #u40.7o {48,168}

ADR0/: <387> (216)
 E157 {116,4} #u112.17o {124,212}

ADR1/: <183> (312)
 #u109.12o {204,232} #u98.12o {172,232} E158 {120,4}

ADR2/: <187> (320)
 #u109.13o {204,228} #u98.13o {172,228} E155 {108,4}

ADR3/: <184> (312)
 #u109.14o {204,224} #u98.14o {172,224} E156 {112,4}

ADR4/: <188> (320)
 #u109.15o {204,220} #u98.15o {172,220} E153 {100,4}

ADR5/: <185> (312)
 #u109.16o {204,216} #u98.16o {172,216} E154 {104,4}

ADR6/: <189> (320)
 #u109.17o {204,212} #u98.17o {172,212} E151 {92,4}

ADR7/: <186> (312)
 #u109.18o {204,208} #u98.18o {172,208} E152 {96,4}

ADR8/: <190> (320)
 #u109.19o {204,204} #u98.19o {172,204} E149 {84,4}

ADR9/: <193> (328)
 #u108.12o {188,232} #u97.12o {156,232} E150 {88,4}

ADRA/: <196> (336)
 #u108.13o {188,228} #u97.13o {156,228} E147 {76,4}

ADRB/: <194> (328)
 #u108.14o {188,224} #u97.14o {156,224} E148 {80,4}

ADRC/: <197> (336)
 #u108.15o {188,220} #u97.15o {156,220} E145 {68,4}

ADRD/: <191> (328)
 #u108.16o {188,216} #u97.16o {156,216} E146 {72,4}

ADRE/: <195> (336)
 #u108.17o {188,212} #u97.17o {156,212} E143 {60,4}

ADRF/: <192> (328)
 #u108.18o {188,208} #u97.18o {156,208} E144 {64,4}

aF.0: <160> (796)
 #u68.27i {24,116} #u66.27i {52,116} #u67.27i {80,116} #u69.27i {108,116}
 #u25.9o {800,96}

aFh.1: <258> (212)
 #u68.28i {24,112} #u67.28i {80,112} #u37.10o {168,180}

aFh.2: <260> (224)
 #u68.26i {24,120} #u67.26i {80,120} #u37.12o {184,184}

aF1.1: <264> (776)

#u66.28i {52,112}	#u69.28i {108,112}	#u25.12o {812,96}	
aFl.2: <248> (796) #u66.26i {52,120}	#u69.26i {108,120}	#u49.9i {124,84}	#u25.15o {812,84}
AltBoot: <332> (128) C505 {484,44}	#u47.11i {556,100}		
AltUAddr: <419> (348) #u40.15o {64,172}	#u92.1i {304,64}		
aSh.0: <259> (220) #u68.14i {0,116}	#u67.14i {56,116}	#u37.7o {168,168}	
aSh.1: <261> (228) #u63.13i {0,112}	#u67.13i {56,112}	#u37.8o {168,172}	
aSh.2: <262> (236) #u68.12i {0,108}	#u67.12i {56,108}	#u37.9o {168,176}	
aSl.0: <269> (820) #u66.14i {28,116}	#u69.14i {84,116}	#u25.2o {800,68}	
aSl.1: <267> (804) #u66.13i {28,112}	#u69.13i {84,112}	#u25.5o {800,80}	
aSl.2: <265> (796) #u66.12i {28,108}	#u69.12i {84,108}	#u25.6o {800,84}	
Bank.0: <210> (352) #u28.1i {428,144}	#u23.2o {396,148}	#u33.2i {332,148}	C303 {188,40}
Bank.1: <233> (368) #u28.2i {428,148}	#u23.5o {396,160}	#u33.5i {332,160}	C304 {192,40}
Bank.2: <232> (368) #u28.3i {428,152}	#u23.6o {396,164}	#u33.11i {344,164}	C305 {196,40}
Bank.3: <133> (716) #u10.2i {752,148} #u13.2i {640,148} #u5.2i {528,148} #u28.4i {428,156}	#u11.2i {724,148} #u15.2i {612,148} #u3.2i {500,148} #u23.9o {396,176}	#u12.2i {696,148} #u6.2i {584,148} #u2.2i {472,148} #u33.14i {344,152}	#u14.2i {668,148} #u4.2i {556,148} #u1.2i {444,148} C306 {200,40}
BCLK: <456> (624) #u31.13i {280,172}	#u73.9o {900,176}		
BCLK/: <394> (604) #u94.3i {32,152}	#u31.7o {268,168}	E113 {452,0}	
BHEN: <297> (72) #u112.5i {112,216}	#u39.14o {144,176}		
BHEN/: <452> (600) E127 {508,0}	#u112.16o {124,216}		
BlankMP': <428> (416) C511 {608,44}	#u30.19o {252,204}		
Boot': <7> (624) #u105.1i {64,200}	#u105.2i {64,204}	#r1.6i {300,220}	C507 {492,44}
BPRN/: <423> (932) #u94.2i {32,148}	E115 {460,0}	#u106.9i {732,84}	
BUSY: <446> (544) #u31.5o {268,160}	#u106.10i {732,80}		
BUSY/: <400> (624) #u105.6o {64,220}	#u31.15i {280,164}	E117 {468,0}	
C.0: <398> (268) #u42.2i {380,148}	#u57.8o {172,88}		
C.1: <404> (296) #u42.5i {380,160}	#u57.6o {160,84}		
C.2: <338> (140) #u42.11i {392,164}	#u46.6o {252,164}		
C.3: <361> (144) #u42.14i {392,152}	#u46.8o {264,168}		
CarryIn: <5> (208) #u60.11i {220,84} #u87.13i {204,76} #u69.29i {108,108}	#u60.12i {220,80} #u48.8o {188,88}	#r2.1o {224,64} #u48.11o {188,76}	#u60.4i {208,76} #u48.5i {176,80}
CarryOut: <305> (276) #u68.33o {24,92}	#u60.10i {220,88}	#u34.14i {232,152}	
CIn: <120> (704) #u86.15i {140,84} #u78.18i {408,80}	#u64.2i {288,68} #u81.18i {428,80}	#u79.18i {368,80} #u27.5o {816,80}	#u80.18i {388,80}
CIn+PC16X': <309> (208) #u48.13i {188,68}	#u49.1i {112,64}	#u35.12o {104,184}	
CIn+PC16Z': <372> (176) #u40.10o {48,180}	#u49.2i {112,68}		

Clk'a: <89> (984)
 #u29.11i {844,100} #u27.11i {828,100} #u25.11i {812,100} #u26.11i {796,100}
 #u22.11i {424,180} #u23.11i {408,180} #u31.18o {280,152} #u69.15i {84,120}
 #u67.15i {56,120} #u66.15i {28,120} #u68.15i {0,120}

Clk'b: <121> (748)
 #u71.16i {796,168} #u31.16o {280,160} #u37.16i {184,168} #u41.16i {164,168}
 #u39.16i {144,168} #u36.16i {124,168} #u35.16i {104,168} #u38.16i {84,168}
 #u40.16i {64,168}

Clk'c: <91> (1088)
 #u70.20i {296,232} #u31.14o {280,168} #u50.11i {156,100} #u93.9i {332,92}
 #u91.9i {348,92} #u115.9i {444,92} #u52.1i {800,144} #u63.1i {816,144}
 #u75.11i {860,180} #u85.11i {876,180}

ClrIntTrap': <199> (804)
 #u94.17i {44,156} #u38.9o {68,176} #u71.5i {780,160} #u52.2i {800,148}

Cycle1: <334> (788)
 #u74.12o {896,184} #u71.6i {780,164} #u84.1i {640,64} C446 {248,44}

Cycle2: <204> (940)
 #u74.13o {896,180} #u37.5i {168,160} #u45.2i {188,148} C446 {244,44}

Cycle3: <385> (948)
 #u74.14o {896,176} #u37.4i {168,156} C448 {256,44}

CycleX': <383> (196)
 #u35.10o {88,180} #u57.13i {172,68}

CycleY': <373> (180)
 #u38.15o {84,172} #u57.2i {160,68}

DAT0/: <350> (408)
 #u100.9i {80,232} #u111.12o {220,232} E173 {180,4}

DAT1/: <344> (400)
 #u100.8i {80,228} #u111.13o {220,228} E174 {184,4}

DAT2/: <351> (408)
 #u100.7i {80,224} #u111.14o {220,224} E171 {172,4}

DAT3/: <345> (400)
 #u100.6i {80,220} #u111.15o {220,220} E172 {176,4}

DAT4/: <352> (408)
 #u100.5i {80,216} #u111.16o {220,216} E169 {164,4}

DAT5/: <346> (400)
 #u100.4i {80,212} #u111.17o {220,212} E170 {168,4}

DAT6/: <353> (408)
 #u100.3i {80,208} #u111.18o {220,208} E167 {156,4}

DAT7/: <347> (400)
 #u100.2i {80,204} #u111.19o {220,204} E168 {160,4}

DAT8/: <354> (420)
 #u110.12o {236,232} #u99.9i {96,232} E165 {148,4}

DAT9/: <355> (420)
 #u110.13o {236,228} #u99.8i {96,228} E166 {152,4}

DATA/: <348> (404)
 #u110.14o {236,224} #u99.7i {96,224} E163 {140,4}

DATB/: <349> (404)
 #u110.15o {236,220} #u99.6i {96,220} E164 {144,4}

DATC/: <342> (388)
 #u110.16o {236,216} #u99.5i {96,216} E161 {132,4}

DATD/: <343> (388)
 #u110.17o {236,212} #u99.4i {96,212} E162 {136,4}

DATE/: <339> (372)
 #u110.18o {236,208} #u99.3i {96,208} E159 {124,4}

DATF/: <340> (372)
 #u110.19o {236,204} #u99.2i {96,204} E160 {128,4}

DCP01.si1+1: <236> (48)
 #u67.16i {56,124} #u68.21o {24,140}

DCP01.si1+2: <272> (60)
 #u67.8i {56,92} #u68.9o {0,96}

DCP01.si1+3: <271> (60)
 #u69.8i {84,92} #u66.9o {28,96}

DCP01.si1+4: <237> (48)
 #u69.16i {84,124} #u66.21o {52,140}

DCP02.si1+1: <4> (88)
 #u49.3o {112,72} #u49.4i {112,76} #u48.9i {188,84}

DCP02.si1+2: <223> (44)
 #u50.3i {144,72} #u49.6o {112,84}

DCP02.si1+3: <290> (68)
 #u48.12i {188,72} #u86.5o {128,80}

DCP03.sil+1: <35> (16)
#u92.4o {304,76} #u93.4i {320,76}

DCP03.sil+2: <129> (24)
#u92.7o {304,88} #u93.5i {320,80}

DCP03.sil+3: <135> (28)
#u92.9o {316,92} #u93.12i {332,80}

DCP03.sil+4: <97> (20)
#u92.12o {316,80} #u93.13i {332,76}

DCP03.sil+5: <116> (140)
#u81.20i {428,72} #u78.20i {408,72} #u80.20i {388,72} #u79.20i {368,72}
#u64.3o {288,72}

DCP04.sil+1: <51> (196)
#u101.3i {480,72} #u102.3i {464,72} #u64.8o {300,88}

DCP04.sil+2: <110> (88)
#u104.2i {512,68} #u114.1i {448,64} #u115.2o {432,68}

DCP04.sil+3: <209> (108)
#u104.4i {512,76} #u114.2i {448,68} #u115.7o {432,88}

DCP04.sil+4: <112> (92)
#u104.6i {512,84} #u115.10o {444,88} #u114.3i {448,72}

DCP04.sil+5: <27> (92)
#u104.8i {512,92} #u114.4i {448,76} #u115.15o {444,68}

DCP04.sil+6: <408> (312)
#u50.4i {144,76} #u114.6o {448,84}

DCP06.sil+1: <39> (36)
#u54.3i {736,72} #u62.2o {752,68} #u61.2o {768,68}

DCP06.sil+10: <437> (472)
#u64.11o {300,76} #u54.11i {748,100}

DCP06.sil+11: <443> (532)
#u50.13i {156,92} #u51.14o {684,88}

DCP06.sil+12: <445> (540)
#u50.8i {144,92} #u51.13o {684,92}

DCP06.sil+13: <380> (572)
#u51.18i {684,72} #u104.11i {524,100} #u50.9o {144,96}

DCP06.sil+14: <442> (528)
#u51.7o {672,88} #u50.7i {144,88}

DCP06.sil+15: <441> (504)
#u50.14i {156,88} #u53.6o {656,84}

DCP06.sil+2: <38> (36)
#u54.4i {736,76} #u62.5o {752,80} #u61.5o {768,80}

DCP06.sil+3: <37> (36)
#u54.7i {736,88} #u62.6o {752,84} #u61.6o {768,84}

DCP06.sil+4: <36> (36)
#u54.8i {736,92} #u62.9o {752,96} #u61.9o {768,96}

DCP06.sil+5: <43> (36)
#u54.13i {748,92} #u62.12o {764,96} #u61.12o {780,96}

DCP06.sil+6: <42> (36)
#u54.14i {748,88} #u62.15o {764,84} #u61.15o {780,84}

DCP06.sil+7: <41> (36)
#u54.17i {748,76} #u62.16o {764,80} #u61.16o {780,80}

DCP06.sil+8: <40> (36)
#u54.18i {748,72} #u62.19o {764,68} #u61.19o {780,68}

DCP06.sil+9: <49> (152)
#u61.11i {780,100} #u62.11i {764,100} #u53.3o {656,72}

DCP07.sil+1: <473> (884)
#u7.13i {28,148} #u19.6o {848,84}

DCP07.sil+2: <474> (904)
#u7.12i {28,152} #u16.6o {864,84}

DCP07.sil+3: <475> (924)
#u7.11i {28,156} #u21.6o {880,84}

DCP07.sil+4: <476> (944)
#u7.10i {28,160} #u18.6o {896,84}

DCP07.sil+5: <136> (28)
#u7.9i {28,164} #u9.6o {0,164}

DCP07.sil+6: <224> (44)
#u94.19i {44,148} #u7.6o {16,164}

DCP09.sil+1: <312> (84)
#u45.6o {188,164} #u46.1i {252,144}

DCP09.sil+10: <389> (232)
#u56.7o {300,168} #u57.4i {160,76}

DCP09.sil+11: <390> (232)
#u56.9o {312,172} #u57.10i {172,80}

DCP09.sil+12: <239> (48)
#u59.1i {284,144} #u58.5o {316,160}

DCP09.sil+2: <302> (76)
#u24.6o {204,164} #u46.13i {264,148}

DCP09.sil+3: <227> (44)
#u34.6o {220,164} #u46.9i {264,164}

DCP09.sil+4: <319> (92)
#u95.6o {236,164} #u58.3i {316,152}

DCP09.sil+5: <30> (536)
#u59.5i {284,160} #u59.2i {284,148} #u59.13i {296,148} #u59.10i {296,160}
#u106.6o {720,84}

DCP09.sil+6: <226> (44)
#u59.4i {284,156} #u58.7o {316,168}

DCP09.sil+7: <213> (40)
#u59.9i {296,164} #u58.9o {328,172}

DCP09.sil+8: <225> (44)
#u59.12i {296,152} #u58.11o {328,164}

DCP09.sil+9: <222> (564)
#u95.5i {236,160} #u31.3o {268,152} #u106.5i {720,80}

DCP10.sil+1: <238> (48)
#u22.8i {412,172} #u32.12o {376,160}

DCP10.sil+10: <253> (56)
#u23.7i {396,168} #u33.9o {344,172}

DCP10.sil+11: <303> (76)
#u23.4i {396,156} #u33.7o {332,168}

DCP10.sil+12: <291> (68)
#u23.3i {396,152} #u33.4o {332,156}

DCP10.sil+13: <274> (60)
#u42.4o {380,156} #u22.13i {424,172}

DCP10.sil+14: <228> (44)
#u42.7o {380,168} #u22.14i {424,168}

DCP10.sil+15: <240> (48)
#u42.9o {392,172} #u22.17i {424,156}

DCP10.sil+16: <215> (40)
#u42.12o {392,160} #u22.18i {424,152}

DCP10.sil+17: <58> (340)
#u22.1i {412,144} #u23.1i {396,144} #u86.7o {128,88}

DCP10.sil+2: <214> (40)
#u22.7i {412,168} #u32.9o {376,172}

DCP10.sil+3: <273> (60)
#u22.4i {412,156} #u32.7o {364,168}

DCP10.sil+4: <247> (52)
#u22.3i {412,152} #u32.4o {364,156}

DCP10.sil+5: <254> (56)
#u44.12o {360,160} #u23.18i {408,152}

DCP10.sil+6: <284> (64)
#u44.9o {360,172} #u23.17i {408,156}

DCP10.sil+7: <275> (60)
#u44.7o {348,168} #u23.14i {408,168}

DCP10.sil+8: <304> (76)
#u44.4o {348,156} #u23.13i {408,172}

DCP10.sil+9: <283> (64)
#u23.8i {396,172} #u33.12o {344,160}

DCP12.sil+1: <143> (376)
#u104.17i {524,76} #u71.7o {780,168} #u71.19i {796,156}

DCP12.sil+10: <285> (64)
#u63.7i {816,168} #u75.19o {860,148}

DCP12.sil+11: <177> (32)
#u63.12o {828,176} #u52.8i {800,172}

DCP12.sil+12: <105> (20)
#u75.3i {848,152} #u85.2o {864,148}

DCP12.sil+13: <104> (20)
#u75.4i {848,156} #u85.5o {864,160}

DCP12.sil+14: <103> (20)

#u75.7i {848,168}	#u85.6o {864,164}		
DCP12.sil+15: <102> (20)	#u75.8i {848,172}	#u85.9o {864,176}	
DCP12.sil+16: <101> (20)	#u75.13i {860,172}	#u85.12o {876,176}	
DCP12.sil+17: <100> (20)	#u75.14i {860,168}	#u85.15o {876,164}	
DCP12.sil+18: <99> (20)	#u75.17i {860,156}	#u85.16o {876,160}	
DCP12.sil+19: <98> (20)	#u75.18i {860,152}	#u85.19o {876,148}	
DCP12.sil+2: <211> (376)	#u104.15i {524,84}	#u71.20i {796,152}	#u71.8o {780,172}
DCP12.sil+3: <256> (56)	#u75.9o {848,176}	#u52.7i {800,168}	
DCP12.sil+4: <242> (48)	#u75.6o {848,164}	#u52.6i {800,164}	
DCP12.sil+5: <241> (48)	#u75.5o {848,160}	#u52.5i {800,160}	
DCP12.sil+6: <255> (56)	#u75.2o {848,148}	#u52.4i {800,156}	
DCP12.sil+7: <286> (64)	#u63.4i {816,156}	#u75.12o {860,176}	
DCP12.sil+8: <244> (48)	#u63.5i {816,160}	#u75.15o {860,164}	
DCP12.sil+9: <243> (48)	#u63.6i {816,164}	#u75.16o {860,160}	
DCP13.sil+1: <127> (976)	#u73.21i {916,148}	#u74.21i {896,148}	#u74.9o {880,176} #u72.3i {0,208}
DCP13.sil+10: <207> (36)	#u83.10i {28,224}	#u72.9o {0,232}	
DCP13.sil+11: <125> (968)	#u72.4i {0,212}	#u74.10o {880,180}	#u74.1i {880,144} #u73.1i {900,144}
DCP13.sil+12: <3> (48)	#u94.6o {32,164}	#u83.15i {28,204}	#u83.14i {28,208}
DCP13.sil+13: <118> (492)	#u95.11o {248,156}	#u84.4i {640,76}	#u84.9i {652,84}
DCP13.sil+14: <26> (76)	#u72.11o {12,236}	#u82.7i {32,224}	#u82.10i {44,224} #u82.2i {32,204}
DCP13.sil+15: <25> (56)	#u72.7o {0,224}	#u83.6i {16,220}	#u83.3i {16,208} #u83.11i {28,220}
DCP13.sil+16: <178> (32)	#u83.2i {16,204}	#u72.6o {0,220}	
DCP13.sil+17: <472> (768)	#u94.4i {32,156}	#u106.8o {732,88}	
DCP13.sil+18: <461> (644)	#u96.2i {560,68}	#u107.13o {60,212}	
DCP13.sil+19: <469> (640)	#u96.4i {560,76}	#u107.12o {60,216}	
DCP13.sil+2: <126> (968)	#u73.20i {916,152}	#u74.20i {896,152}	#u74.8o {880,172} #u72.2i {0,204}
DCP13.sil+20: <458> (636)	#u96.6i {560,84}	#u107.11o {60,220}	
DCP13.sil+21: <457> (632)	#u96.8i {560,92}	#u107.10o {60,224}	
DCP13.sil+3: <124> (960)	#u73.19i {916,156}	#u74.19i {896,156}	#u74.7o {880,168} #u72.1i {0,200}
DCP13.sil+4: <229> (44)	#u82.3i {32,208}	#u72.12o {12,232}	
DCP13.sil+5: <137> (28)	#u82.6i {32,220}	#u72.13o {12,228}	
DCP13.sil+6: <208> (36)	#u82.11i {44,220}	#u72.14o {12,224}	
DCP13.sil+7: <2> (44)	#u94.15o {44,164}	#u82.15i {44,204}	#u82.14i {44,208}
DCP13.sil+8: <122> (944)	#u73.4i {900,156}	#u74.4i {880,156}	#u82.13o {44,212} #u72.17i {12,212}

DCP13.sil+9: <106> (20)
 #u83.7i {16,224} #u72.8o {0,228}

DCP14.sil+1: <46> (100)
 #u111.11i {220,236} #u110.11i {236,236} #u95.3o {236,152}

DCP14.sil+2: <54> (240)
 #u95.8o {248,168} #u109.11i {204,236} #u108.11i {188,236} #u98.11i {172,236}
 #u97.11i {156,236} #u113.1i {128,200} #u112.1i {112,200}

DCP15.sil+1: <16> (496)
 #u31.8i {268,172} #u53.9i {668,84} #u53.11o {668,76}

DCP15.sil+2: <379> (188)
 #u64.6o {288,84} #u30.11i {252,236}

DebAFu11: <397> (656)
 #u47.15i {556,84} C435 {204,44} #u70.11o {272,240}

DebBFu11: <391> (616)
 #u47.17i {556,76} C436 {208,44} #u70.5o {272,216}

DebData.0: <414> (320)
 C427 {172,44} #u70.18o {296,240}

DebData.1: <413> (320)
 C428 {176,44} #u70.17o {296,244}

DebData.2: <412> (320)
 C429 {180,44} #u70.16o {296,248}

DebData.3: <411> (320)
 C430 {184,44} #u70.15o {296,252}

DebData.4: <403> (292)
 C431 {188,44} #u70.14o {272,252}

DebData.5: <401> (284)
 C432 {192,44} #u70.13o {272,248}

DebData.6: <399> (268)
 C433 {196,44} #u70.10o {272,236}

DebData.7: <395> (260)
 C434 {200,44} #u70.9o {272,232}

dGoodIBDisp: <212> (40)
 C424 {160,44} #u50.16o {156,80}

DoIt: <415> (784)
 #u74.15o {896,172} #u53.10i {668,80} C444 {240,44}

DP.0: <425> (408)
 C506 {488,44} #u30.2o {240,204}

DP.1: <431> (428)
 C508 {496,44} #u30.5o {240,216}

DP.2: <434> (440)
 C510 {504,44} #u30.6o {240,220}

DP.3: <430> (424)
 C512 {0,48} #u30.9o {240,232}

EnC2Funs: <367> (660)
 #u51.16i {684,80} #u95.13i {248,148} #u50.15o {156,84}

EnU: <117> (448)
 #u79.17i {368,84} #u80.17i {388,84} #u78.17i {408,84} #u81.17i {428,84}
 #u27.6o {816,84}

F.0: <393> (252)
 #u34.4i {220,156} #u68.31o {24,100}

Feq0: <144> (416)
 #r3.1o {272,64} #u34.3i {220,152} #u86.11i {140,100} #u69.11o {84,104}
 #u67.11o {56,104} #u66.11o {28,104} #u68.11o {0,104}

Fne0: <360> (144)
 #u34.2i {220,148} #u86.9o {128,96}

ForceBank0: <438> (488)
 #u71.12o {796,184} #u33.15i {344,148}

fX.0: <333> (604)
 #u27.12o {828,96} #u106.4i {720,76} #u58.2i {316,148}

fX.1: <448> (572)
 #u58.1i {316,144} #u27.15o {828,84}

fX.2: <447> (568)
 #u58.15i {328,148} #u27.16o {828,80}

fX.3: <449> (584)
 #u58.14i {328,152} #u27.19o {828,68}

fY.0: <406> (304)
 #u29.2o {832,68} #u88.2i {528,68}

fY.1: <71> (724)
 #u45.9i {200,172} #u24.9i {216,172} #u34.9i {232,172} #u88.5i {528,80}

#u29.5o {832,80}

FY.2: <70> {716}
 #u45.10i {200,168} #u24.10i {216,168} #u34.10i {232,168} #u56.2i {300,148}
 #u88.11i {540,84} #u29.6o {832,84}

FY.3: <72> {748}
 #u45.11i {200,164} #u24.11i {216,164} #u34.11i {232,164} #u56.14i {312,152}
 #u88.14i {540,72} #u29.9o {832,96}

FZ.0: <416> {328}
 #u29.12o {844,96} #u47.2i {544,68}

FZ.1: <407> {308}
 #u29.15o {844,84} #u47.4i {544,76}

FZ.2: <59> {352}
 #u47.6i {544,84} #u76.9i {588,92} #u77.9i {604,92} #u89.9i {620,92}
 #u90.9i {636,92} #u43.1i {688,64} #u29.16o {844,80}

FZ.3: <56> {324}
 #u47.8i {544,92} #u76.10i {588,88} #u77.10i {604,88} #u89.10i {620,88}
 #u90.10i {636,88} #u29.19o {844,68}

GND: <13> {22312}

#u65.7i {256,224}	#u30.10i {240,236}	#u110.10i {224,236}	#u111.10i {208,236}
#u109.10i {192,236}	#u108.10i {176,236}	#u98.10i {160,236}	#u97.10i {144,236}
#u113.10i {128,236}	#u112.10i {112,236}	#u99.10i {96,236}	#u100.10i {80,236}
#u105.7i {64,224}	#u107.8i {48,228}	#u82.8i {32,228}	#u83.8i {16,228}
#u72.10i {0,236}	#u73.11i {900,184}	#u74.11i {880,184}	#u85.10i {864,180}
#u75.10i {848,180}	#u63.10i {816,180}	#u52.10i {800,180}	#u71.11i {780,184}
#u10.14i {752,196}	#u11.14i {724,196}	#u12.14i {696,196}	#u14.14i {668,196}
#u13.14i {640,196}	#u15.14i {612,196}	#u6.14i {584,196}	#u4.14i {556,196}
#u5.14i {528,196}	#u3.14i {500,196}	#u2.14i {472,196}	#u1.14i {444,196}
#u28.10i {428,180}	#u22.10i {412,180}	#u23.10i {396,180}	#u42.8i {380,172}
#u32.8i {364,172}	#u44.8i {348,172}	#u33.8i {332,172}	#u58.8i {316,172}
#u56.8i {300,172}	#u59.7i {284,168}	#u31.10i {268,180}	#u46.7i {252,168}
#u95.7i {236,168}	#u34.8i {220,172}	#u24.8i {204,172}	#u45.8i {188,172}
#u37.11i {168,184}	#u41.11i {148,184}	#u39.11i {128,184}	#u36.11i {108,184}
#u35.11i {88,184}	#u38.11i {68,184}	#u40.11i {48,184}	#u94.10i {32,180}
#u7.7i {16,168}	#u9.7i {0,168}	#u18.7i {896,88}	#u21.7i {880,88}
#u16.7i {864,88}	#u19.7i {848,88}	#u29.10i {832,100}	#u27.10i {816,100}
#u25.10i {800,100}	#u26.10i {784,100}	#u61.10i {768,100}	#u62.10i {752,100}
#u54.10i {736,100}	#u106.7i {720,88}	#u55.8i {704,92}	#u43.8i {688,92}
#u51.10i {672,100}	#u53.7i {656,88}	#u84.7i {640,88}	#u90.8i {624,92}
#u89.8i {608,92}	#u77.8i {592,92}	#u76.8i {576,92}	#u96.10i {560,100}
#u47.10i {544,100}	#u88.8i {528,92}	#u104.10i {512,100}	#u103.10i {496,100}
#u101.8i {480,92}	#u102.8i {464,92}	#u114.10i {448,100}	#u115.8i {432,92}
#u81.8i {412,92}	#u78.8i {392,92}	#u80.8i {372,92}	#u79.8i {352,92}
#u91.8i {336,92}	#u93.8i {320,92}	#u92.8i {304,92}	#u64.7i {288,88}
#u60.8i {208,92}	#u87.8i {192,92}	#u48.7i {176,88}	#u57.7i {160,88}
#u50.10i {144,100}	#u86.10i {128,100}	#u49.7i {112,88}	#c97.1o {336,260}
#c98.1o {320,260}	#c99.1o {304,260}	#c100.1o {272,260}	#c101.1o {288,260}
#c102.1o {256,260}	#c103.1o {240,260}	#c104.1o {208,260}	#c105.1o {224,260}
#c106.1o {192,260}	#c107.1o {176,260}	#c108.1o {144,260}	#c109.1o {160,260}
#c110.1o {128,260}	#c111.1o {112,260}	#c112.1o {96,260}	#c113.1o {48,260}
#c114.1o {64,260}	#c115.1o {80,260}	#c66.1o {464,256}	#c67.1o {480,256}
#c68.1o {512,256}	#c69.1o {496,256}	#c70.1o {528,256}	#c71.1o {544,256}
#c72.1o {576,256}	#c73.1o {560,256}	#c74.1o {592,256}	#c75.1o {608,256}
#c76.1o {640,256}	#c77.1o {624,256}	#c78.1o {656,256}	#c79.1o {672,256}
#c80.1o {688,256}	#c81.1o {32,260}	#c82.1o {16,260}	#c83.1o {0,260}
#c84.1o {880,256}	#c85.1o {896,256}	#c86.1o {864,256}	#c87.1o {848,256}
#c88.1o {816,256}	#c89.1o {832,256}	#c90.1o {800,256}	#c91.1o {784,256}
#c92.1o {752,256}	#c93.1o {768,256}	#c94.1o {736,256}	#c95.1o {720,256}
#c96.1o {704,256}	#c33.1o {448,256}	#c34.1o {432,256}	#c35.1o {416,256}
#c36.1o {384,256}	#c37.1o {400,256}	#c38.1o {368,256}	#c39.1o {352,256}
#c40.1o {320,256}	#c41.1o {336,256}	#c42.1o {304,256}	#c43.1o {288,256}
#c44.1o {256,256}	#c45.1o {272,256}	#c46.1o {240,256}	#c47.1o {224,256}
#c48.1o {208,256}	#c49.1o {864,200}	#c50.1o {880,200}	#c51.1o {896,200}
#c52.1o {16,256}	#c53.1o {0,256}	#c54.1o {32,256}	#c55.1o {48,256}
#c56.1o {80,256}	#c57.1o {64,256}	#c58.1o {96,256}	#c59.1o {112,256}
#c60.1o {144,256}	#c61.1o {128,256}	#c62.1o {160,256}	#c63.1o {176,256}
#c64.1o {192,256}	#c1.1o {352,200}	#c2.1o {368,200}	#c3.1o {384,200}
#c4.1o {416,200}	#c5.1o {400,200}	#c6.1o {432,200}	#c7.1o {448,200}
#c8.1o {480,200}	#c9.1o {464,200}	#c10.1o {496,200}	#c11.1o {512,200}
#c12.1o {544,200}	#c13.1o {528,200}	#c14.1o {560,200}	#c15.1o {576,200}
#c16.1o {592,200}	#c17.1o {848,200}	#c18.1o {832,200}	#c19.1o {816,200}
#c20.1o {784,200}	#c21.1o {800,200}	#c22.1o {768,200}	#c23.1o {752,200}
#c24.1o {720,200}	#c25.1o {736,200}	#c26.1o {704,200}	#c27.1o {688,200}
#c28.1o {656,200}	#c29.1o {672,200}	#c30.1o {640,200}	#c31.1o {624,200}
#c32.1o {608,200}	E185 {228,4}	E186 {232,4}	E176 {192,4}
E175 {188,4}	E112 {448,0}	E111 {444,0}	E102 {408,0}
E101 {404,0}	C501 {468,44}	C450 {264,44}	C449 {260,44}
C350 {376,40}	C349 {372,40}	C325 {276,40}	C326 {280,40}
C425 {164,44}	C426 {168,44}	C402 {72,44}	C401 {68,44}
C302 {184,40}	C301 {180,40}	#u8.10i {320,236}	#u17.10i {336,236}
#u20.10i {304,236}	#u86.19i {140,68}	#u31.19i {280,148}	#u50.1i {144,64}
#u31.1i {268,144}	#u70.22i {296,224}	#u107.4i {48,212}	#u107.5i {48,216}
#u74.17i {896,164}	#u72.15i {12,220}	#u73.17i {916,164}	#u73.18i {916,160}
#u74.18i {896,160}	#u52.9i {800,176}	#u63.2i {816,148}	#u63.3i {816,152}
#u63.8i {816,172}	#u63.9i {816,176}	#u71.18i {796,160}	#u75.1i {848,144}
#u85.1i {864,144}	#u71.17i {796,164}	#u28.15i {440,164}	#u28.16i {440,160}
#u28.17i {440,156}	#u28.18i {440,152}	#u28.19i {440,148}	#u44.3i {348,152}
#u58.13i {328,156}	#u37.6i {168,164}	#u37.18i {184,160}	#u37.17i {184,164}
#u36.6i {108,164}	#u41.17i {164,164}	#u39.17i {144,164}	#u36.17i {124,164}
#u35.17i {104,164}	#u38.17i {84,164}	#u40.17i {64,164}	#u39.18i {144,160}
#u39.4i {128,156}	#u39.5i {128,160}	#u39.6i {128,164}	#u40.18i {64,160}
#u40.4i {48,156}	#u40.5i {48,160}	#u40.6i {48,164}	#u41.4i {148,156}
#u41.5i {148,160}	#u41.6i {148,164}	#u38.4i {68,156}	#u38.5i {68,160}
#u38.6i {68,164}	#u35.2i {88,148}	#u35.3i {88,152}	#u35.4i {88,156}
#u35.5i {88,160}	#u35.6i {88,164}	#u35.18i {104,160}	#u36.18i {124,160}

#u38.18i {84,160}	#u41.18i {164,160}	#u7.1i {16,144}	#u29.1i {832,64}
#u27.1i {816,64}	#u25.1i {800,64}	#u26.1i {784,64}	#u43.3i {688,72}
#u43.6i {688,84}	#u43.10i {700,88}	#u43.13i {700,76}	#u51.15i {634,84}
#u54.1i {736,64}	#u96.11i {572,100}	#u96.13i {572,92}	#u96.15i {572,84}
#u96.17i {572,76}	#u88.3i {528,72}	#u88.6i {528,84}	#u88.10i {540,88}
#u88.13i {540,76}	#u102.2i {464,68}	#u101.2i {480,68}	#u114.15i {460,84}
#u81.19i {428,76}	#u78.19i {408,76}	#u80.19i {388,76}	#u79.19i {368,76}
#u92.15i {316,68}	#u91.3i {336,72}	#u91.6i {336,84}	#u91.11i {348,84}
#u91.14i {348,72}	#u69.30o {108,104}	#u66.40i {52,64}	#u66.30o {52,104}
#u68.40i {24,64}	#u67.30o {80,104}	#u68.30o {24,104}	#u69.40i {108,64}
#u67.40i {80,64}			
GoodIBDisp: <69> (644)			
#u51.6o {672,84}	#u42.1i {380,144}	#u32.1i {364,144}	#u50.17i {156,76}
IB.0: <63> (456)			
#u54.2o {736,68}	#u55.2i {704,68}	#u43.2i {688,68}	#u32.3i {364,152}
IB.1: <62> (456)			
#u54.5o {736,80}	#u55.5i {704,80}	#u43.5i {688,80}	#u32.6i {364,164}
IB.2: <61> (444)			
#u54.6o {736,84}	#u55.11i {716,84}	#u43.11i {700,84}	#u32.10i {376,168}
IB.3: <64> (468)			
#u54.9o {736,96}	#u55.14i {716,72}	#u43.14i {700,72}	#u32.13i {376,156}
IB.4: <293> (472)			
#u54.12o {748,96}	#u55.3i {704,72}	#u42.3i {380,152}	
IB.5: <234> (448)			
#u54.15o {748,84}	#u55.6i {704,84}	#u42.6i {380,164}	
IB.6: <219> (444)			
#u54.16o {748,80}	#u55.10i {716,88}	#u42.10i {392,168}	
IB.7: <218> (444)			
#u54.19o {748,68}	#u55.13i {716,76}	#u42.13i {392,156}	
IBDisp: <468> (720)			
#u38.10o {68,180}	#u51.1i {672,64}		
IBEmpty': <451> (592)			
#u50.6o {144,84}	#u106.2i {720,68}		
IBEmptyTrap': <298> (204)			
#u53.5i {656,80}	#u106.3o {720,72}	#u71.1i {780,144}	
IBHigh': <462> (648)			
#u41.15o {164,172}	#u55.1i {704,64}		
IBPtr.1: <377> (676)			
#u50.12o {156,96}	#u44.13i {360,156}	#u104.13i {524,92}	#u51.19i {684,68}
IBPtr+Byte: <467> (716)			
#u40.8o {48,172}	#u51.5i {672,80}		
IBPtr+Word: <469> (724)			
#u40.9o {48,176}	#u51.4i {672,76}		
IBRefillTrap: <424> (376)			
#u44.1i {348,144}	#u51.8o {672,92}		
IncMP': <427> (412)			
C515 {12,48}	#u30.15o {252,220}		
INIT/: <19> (664)			
#u105.3o {64,208}	#u94.9i {32,176}	#u94.7i {32,168}	E114 {456,0}
InitTrap': <123> (960)			
#u72.18i {12,208}	#u83.13o {28,212}	#u30.1i {240,200}	#u71.3i {780,152}
#u74.5i {880,160}	#u73.5i {900,160}		
INT0/: <478> (960)			
E141 {52,4}	#u85.3i {864,152}		
INT1/: <477> (960)			
E142 {56,4}	#u85.4i {864,156}		
INT2/: <480> (984)			
E139 {44,4}	#u85.7i {864,168}		
INT3/: <479> (984)			
E140 {48,4}	#u85.8i {864,172}		
INT4/: <484> (1008)			
E137 {36,4}	#u85.13i {876,172}		
INT5/: <483> (1000)			
E138 {40,4}	#u85.14i {876,168}		
INT6/: <482> (1000)			
E135 {28,4}	#u85.17i {876,156}		
INT7/: <481> (992)			
E136 {32,4}	#u85.18i {876,152}		
Interrupt: <370> (780)			
#u34.1i {220,144}	#u44.10i {360,168}	#u51.17i {684,76}	#u52.19o {812,148}
IOCmd: <230> (44)			

#u83.4o {16,212}	#u107.1i {48,200}		
IORC/: <374> (184) E121 {484,0}	#u96.12o {572,96}		
IORef: <92> (1088) #u72.5i {0,216} #u74.2i {880,148}	#u112.3i {112,208} #u73.2i {900,148}	#u113.3i {128,208}	#u84.8o {652,88}
IORefY': <454> (616) #u84.11i {652,76}	#u39.12o {144,184}		
IORefZ': <464> (692) #u84.10i {652,80}	#u40.12o {64,184}		
IOWC/: <368> (164) E122 {488,0}	#u96.16o {572,80}		
Link.0': <378> (188) #u59.3o {284,152}	#u57.11i {172,76}		
Link.1': <386> (208) #u57.5i {160,80}	#u59.6o {284,164}		
Link.2': <282> (64) #u46.2i {252,148}	#u59.8o {296,168}		
Link.3': <206> (36) #u46.10i {264,160}	#u59.11o {296,156}		
MapFlag.0: <57> (340) #u28.11o {440,180}	#u113.19o {140,204}	#u112.19o {124,204}	
MapFlag.1: <60> (372) #u28.12o {440,176}	#u113.12o {140,232}	#u112.12o {124,232}	
MapRef: <93> (1088) #u73.3i {900,152} #u112.2i {112,204}	#u74.3i {880,152} #u72.16i {12,216}	#u84.6o {640,84}	#u113.2i {128,204}
MapRefX': <460> (644) #u84.3i {640,72}	#u35.13o {104,180}		
MapRefY': <453> (604) #u84.5i {640,80}	#u39.8o {128,172}		
MarPageCross': <15> (496) #u53.4i {656,76}	#u84.12o {652,72}	#u46.5i {252,160}	
Master': <11> (1576) #u105.5i {64,216} #u47.13i {556,92}	#u105.4i {64,212} #u74.6i {880,164}	#u72.19i {12,204} #u73.6i {900,164}	#u94.5o {32,160} #u96.1i {560,64}
Mem: <381> (680) #u27.9o {816,96}	#u84.13i {652,68}	#u95.12i {248,152}	
MRDC/: <375> (184) E119 {476,0}	#u96.14o {572,88}		
MWTC/: <369> (164) E120 {480,0}	#u96.18o {572,72}		
NIA.0: <157> (688) #u10.10i {752,180} #u13.10i {640,180} #u5.10i {528,180} #u23.12o {408,176}	#u11.10i {724,180} #u15.10i {612,180} #u3.10i {500,180} C307 {204,40}	#u12.10i {696,180} #u6.10i {584,180} #u2.10i {472,180}	#u14.10i {668,180} #u4.10i {556,180} #u1.10i {444,180}
NIA.1: <156> (680) #u10.9i {752,176} #u13.9i {640,176} #u5.9i {528,176} #u23.15o {408,164}	#u11.9i {724,176} #u15.9i {612,176} #u3.9i {500,176} C308 {208,40}	#u12.9i {696,176} #u6.9i {584,176} #u2.9i {472,176}	#u14.9i {668,176} #u4.9i {556,176} #u1.9i {444,176}
NIA.10: <155> (680) #u10.21i {776,172} #u13.21i {664,172} #u5.21i {552,172} #u22.16o {424,160}	#u11.21i {748,172} #u15.21i {636,172} #u3.21i {524,172} #u58.10i {328,168}	#u12.21i {720,172} #u6.21i {608,172} #u2.21i {496,172} C317 {244,40}	#u14.21i {692,172} #u4.21i {580,172} #u1.21i {468,172}
NIA.11: <153> (676) #u10.23i {776,164} #u13.23i {664,164} #u5.23i {552,164} #u22.19o {424,148}	#u11.23i {748,164} #u15.23i {636,164} #u3.23i {524,164} #u58.12i {328,160}	#u12.23i {720,164} #u6.23i {608,164} #u2.23i {496,164} C318 {248,40}	#u14.23i {692,164} #u4.23i {580,164} #u1.23i {468,164}
NIA.2: <152> (672) #u10.8i {752,172} #u13.8i {640,172} #u5.8i {528,172} #u23.16o {408,160}	#u11.8i {724,172} #u15.8i {612,172} #u3.8i {500,172} C309 {212,40}	#u12.8i {696,172} #u6.8i {584,172} #u2.8i {472,172}	#u14.8i {668,172} #u4.8i {556,172} #u1.8i {444,172}
NIA.3: <151> (664) #u10.7i {752,168} #u13.7i {640,168} #u5.7i {528,168} #u23.19o {408,148}	#u11.7i {724,168} #u15.7i {612,168} #u3.7i {500,168} C310 {216,40}	#u12.7i {696,168} #u6.7i {584,168} #u2.7i {472,168}	#u14.7i {668,168} #u4.7i {556,168} #u1.7i {444,168}
NIA.4: <149> (656) #u10.6i {752,164} #u13.6i {640,164}	#u11.6i {724,164} #u15.6i {612,164}	#u12.6i {696,164} #u6.6i {584,164}	#u14.6i {668,164} #u4.6i {556,164}

#u5.6i {528,164}	#u3.6i {500,164}	#u2.6i {472,164}	#u1.6i {444,164}
#u22.2o {412,148}	C311 {220,40}		
NIA.5: <147> (648)			
#u10.5i {752,160}	#u11.5i {724,160}	#u12.5i {696,160}	#u14.5i {668,160}
#u13.5i {640,150}	#u15.5i {612,160}	#u6.5i {584,160}	#u4.5i {556,160}
#u5.5i {528,160}	#u3.5i {500,160}	#u2.5i {472,160}	#u1.5i {444,160}
#u22.5o {412,160}	C312 {224,40}		
NIA.6: <148> (656)			
#u10.4i {752,156}	#u11.4i {724,156}	#u12.4i {696,156}	#u14.4i {668,156}
#u13.4i {640,156}	#u15.4i {612,156}	#u6.4i {584,156}	#u4.4i {556,156}
#u5.4i {528,156}	#u3.4i {500,156}	#u2.4i {472,156}	#u1.4i {444,156}
#u22.6o {412,164}	C313 {228,40}		
NIA.7: <154> (680)			
#u10.3i {752,152}	#u11.3i {724,152}	#u12.3i {696,152}	#u14.3i {668,152}
#u13.3i {640,152}	#u15.3i {612,152}	#u6.3i {584,152}	#u4.3i {556,152}
#u5.3i {528,152}	#u3.3i {500,152}	#u2.3i {472,152}	#u1.3i {444,152}
#u22.9o {412,176}	#u31.17i {280,156}	C314 {232,40}	
NIA.8: <158> (696)			
#u10.25i {776,156}	#u11.25i {748,156}	#u12.25i {720,156}	#u14.25i {692,156}
#u13.25i {664,156}	#u15.25i {636,156}	#u6.25i {608,156}	#u4.25i {580,156}
#u5.25i {552,156}	#u3.25i {524,156}	#u2.25i {496,156}	#u1.25i {468,156}
#u22.12o {424,176}	#u58.4i {316,156}	C315 {236,40}	
NIA.9: <150> (664)			
#u10.24i {776,160}	#u11.24i {748,160}	#u12.24i {720,160}	#u14.24i {692,160}
#u13.24i {664,160}	#u15.24i {636,160}	#u6.24i {608,160}	#u4.24i {580,160}
#u5.24i {552,160}	#u3.24i {524,160}	#u2.24i {496,160}	#u1.24i {468,160}
#u22.15o {424,164}	#u58.6i {316,164}	C316 {240,40}	
Overflow: <396> (264)			
#u24.12i {216,160}	#u68.34o {24,88}		
paD.0: <306> (824)			
#u16.8i {876,88}	#u25.17i {812,76}	#u11.18o {748,184}	#u2.18o {496,184}
C335 {316,40}			
paD.1: <266> (796)			
#u16.4i {864,76}	#u25.18i {812,72}	#u11.19o {748,180}	#u2.19o {496,180}
C336 {320,40}			
paF.0: <320> (848)			
#u16.11i {876,76}	#u25.8i {800,92}	#u11.15o {748,196}	#u2.15o {496,196}
C332 {304,40}			
paF.1: <308> (1076)			
#u37.1i {168,144}	C333 {308,40}	#u2.16o {496,192}	#u11.16o {748,192}
#u25.13i {812,92}	#u16.10i {876,80}		
paF.2: <295> (1068)			
#u37.2i {168,148}	C334 {312,40}	#u2.17o {496,188}	#u11.17o {748,188}
#u25.14i {812,88}	#u16.9i {876,84}		
PageCross: <365> (680)			
#u84.2i {640,68}	#u45.12i {200,160}	#u49.8o {124,88}	
ParityLED': <325> (100)			
#11.2i {844,144}	#u71.10o {780,180}		
ParityTrap: <470> (740)			
#u71.4i {780,156}	#u94.16o {44,160}		
paS.0: <270> (1036)			
#u19.1i {848,64}	#u25.3i {800,72}	#u11.11o {724,184}	#u2.11o {472,184}
#u37.19i {184,156}	C329 {292,40}		
paS.1: <314> (1072)			
#u37.20i {184,152}	C330 {296,40}	#u2.12o {472,188}	#u11.12o {724,188}
#u25.4i {800,76}	#u16.13i {876,68}		
paS.2: <321> (1072)			
#u37.21i {184,148}	C331 {300,40}	#u2.13o {472,192}	#u11.13o {724,192}
#u25.7i {800,88}	#u16.12i {876,72}		
PC16': <231> (184)			
#u49.5i {112,80}	#u50.2o {144,68}	#u48.10i {188,80}	#u24.2i {204,148}
pCIn: <276> (808)			
#u16.1i {864,64}	#u27.4i {816,76}	#u12.12o {696,188}	#u3.12o {500,188}
C338 {328,40}			
pEnU: <322> (836)			
#u21.13i {892,68}	#u27.7i {816,88}	#u12.13o {696,192}	#u3.13o {500,192}
C339 {332,40}			
pEP: <249> (800)			
#u16.2i {864,68}	#u27.3i {816,72}	#u12.11o {696,184}	#u3.11o {500,184}
C337 {324,40}			
pfS.0: <34> (1216)			
#u38.2i {68,148}	#u36.19i {124,156}	#u39.2i {128,148}	C341 {340,40}
#u3.16o {524,192}	#u12.16o {720,192}	#u21.11i {892,76}	
pfS.1: <10> (1192)			
#u38.3i {68,152}	#u36.20i {124,152}	#u39.3i {128,152}	C342 {344,40}
#u3.17o {524,188}	#u12.17o {720,188}	#u21.10i {892,80}	
pfS.2: <96> (1352)			

#u21.9i {892,84}	#u12.18o {720,184}	#u3.18o {524,184}	#u91.1i {336,64}
#u93.1i {320,64}	C343 {348,40}	#u40.2i {48,148}	#u36.21i {124,148}
#u41.2i {148,148}			
pFS.3: <246> (1204)			
#u40.3i {48,152}	#u36.1i {108,144}	#u41.3i {148,152}	C344 {352,40}
#u3.19o {524,180}	#u12.19o {720,180}	#u21.8i {892,88}	
pFX.0: <296> (1144)			
#u35.19i {104,156}	C345 {356,40}	#u4.11o {556,184}	#u13.11o {640,184}
#u27.13i {828,92}	#u21.4i {880,76}		
pFX.1: <301> (1156)			
#u35.20i {104,152}	C346 {360,40}	#u4.12o {556,188}	#u13.12o {640,188}
#u27.14i {828,88}	#u21.2i {880,68}		
pFX.2: <288> (1164)			
#u35.21i {104,148}	C347 {364,40}	#u4.13o {556,192}	#u13.13o {640,192}
#u27.17i {828,76}	#u21.1i {880,64}		
pFX.3: <315> (1208)			
#u35.1i {88,144}	C348 {368,40}	#u4.15o {580,196}	#u13.15o {664,196}
#u27.18i {828,72}	#u18.13i {908,68}		
pFY.0: <134> (1100)			
#u18.12i {908,72}	#u29.3i {832,72}	#u13.16o {664,192}	#u4.16o {580,192}
#u39.19i {144,156}	#u36.4i {108,156}	#u38.19i {84,156}	C403 {76,44}
pFY.1: <205> (1100)			
#u18.11i {908,76}	#u29.4i {832,76}	#u13.17o {664,188}	#u4.17o {580,188}
#u39.20i {144,152}	#u36.5i {108,160}	#u38.20i {84,152}	C404 {80,44}
pFY.2: <278> (1068)			
#u18.10i {908,80}	#u29.7i {832,88}	#u13.18o {664,184}	#u4.18o {580,184}
#u39.21i {144,148}	#u38.21i {84,148}	C405 {84,44}	
pFY.3: <279> (1092)			
#u18.9i {908,84}	#u29.8i {832,92}	#u13.19o {664,180}	#u4.19o {580,180}
#u39.1i {128,144}	#u38.1i {68,144}	C406 {88,44}	
pFZ.0: <252> (1300)			
C407 {92,44}	#u40.19i {64,156}	#u36.2i {108,148}	#u41.19i {164,156}
#u92.2i {304,68}	#u5.11o {528,184}	#u14.11o {668,184}	#u29.13i {844,92}
#u18.8i {908,88}			
pFZ.1: <235> (1264)			
C408 {96,44}	#u40.20i {64,152}	#u36.3i {108,152}	#u41.20i {164,152}
#u92.5i {304,80}	#u5.12o {528,188}	#u14.12o {668,188}	#u29.14i {844,88}
#u18.4i {896,76}			
pFZ.2: <280> (1268)			
#u18.2i {896,68}	#u29.17i {844,76}	#u14.13o {668,192}	#u5.13o {528,192}
#u92.11i {316,84}	#u41.21i {164,148}	#u40.21i {64,148}	C409 {100,44}
pFZ.3: <281> (1320)			
#u40.1i {48,144}	#u41.1i {148,144}	C410 {104,44}	#u92.14i {316,72}
#u5.15o {552,196}	#u14.15o {692,196}	#u29.18i {844,72}	#u18.1i {896,64}
pMem: <323> (1116)			
#u37.3i {168,152}	C340 {336,40}	#u3.15o {524,196}	#u12.15o {720,196}
#u27.8i {816,92}	#u21.12i {892,72}		
pNIA.0: <358> (924)			
#u14.16o {692,192}	#u5.16o {552,192}	#u44.2i {348,148}	#u9.13i {12,148}
C411 {108,44}			
pNIA.1: <357> (924)			
#u14.17o {692,188}	#u5.17o {552,188}	#u44.5i {348,160}	#u9.12i {12,152}
C412 {112,44}			
pNIA.10': <169> (872)			
#u7.4i {16,156}	C421 {148,44}	#u46.4i {252,156}	#u6.18o {608,184}
#u15.18o {636,184}			
pNIA.11': <166> (860)			
#u15.19o {636,180}	#u6.19o {608,180}	#u46.12i {264,152}	C422 {152,44}
#u7.2i {16,148}			
pNIA.2: <356> (924)			
#u14.18o {692,184}	#u5.18o {552,184}	#u44.11i {360,164}	#u9.11i {12,156}
C413 {116,44}			
pNIA.3: <359> (932)			
#u14.19o {692,180}	#u5.19o {552,180}	#u44.14i {360,152}	C414 {120,44}
#u9.10i {12,160}			
pNIA.4: <167> (860)			
#u15.11o {612,184}	#u6.11o {584,184}	#u32.2i {364,148}	C415 {124,44}
#u9.9i {12,164}			
pNIA.5: <168> (868)			
#u15.12o {612,188}	#u6.12o {584,188}	#u32.5i {364,160}	C416 {128,44}
#u9.8i {12,168}			
pNIA.6: <170> (872)			
#u15.13o {612,192}	#u6.13o {584,192}	#u32.11i {376,164}	C417 {132,44}
#u9.4i {0,156}			
pNIA.7: <172> (892)			
#u15.15o {636,196}	#u6.15o {608,196}	#u32.14i {376,152}	C418 {136,44}
#u9.2i {0,148}			

pNIA.8': <171> (884)
 #u15.16o {636,192} #u6.16o {608,192} #u57.9i {172,84} C419 {140,44}
 #u9.1i {0,144}

pNIA.9': <173> (900)
 #u15.17o {636,188} #u6.17o {608,188} #u7.8i {28,168} #u57.3i {160,72}
 C420 {144,44}

PopX: <433> (440)
 #u35.14o {104,176} #u114.5i {448,80}

PopZ: <439> (496)
 #u40.13o {64,180} #u114.16i {460,80}

prA.0: <311> (868)
 #u19.13i {860,68} #u26.3i {784,72} #u10.11o {752,184} #u1.11o {444,184}
 #u91.4i {336,76} C319 {252,40}

prA.1: <310> (868)
 #u19.12i {860,72} #u26.4i {784,76} #u10.12o {752,188} #u1.12o {444,188}
 #u91.5i {336,80} C320 {256,40}

prA.2: <317> (868)
 #u19.11i {860,76} #u26.7i {784,88} #u10.13o {752,192} #u1.13o {444,192}
 #u91.12i {348,80} C321 {260,40}

prA.3: <316> (868)
 #u19.10i {860,80} #u26.8i {784,92} #u10.15o {776,196} #u1.15o {468,196}
 #u91.13i {348,76} C322 {264,40}

prB.0: <300> (852)
 #u19.9i {860,84} #u26.13i {796,92} #u10.16o {776,192} #u1.16o {468,192}
 C323 {268,40}

prB.1: <287> (836)
 #u19.8i {860,88} #u26.14i {796,88} #u10.17o {776,188} #u1.17o {468,188}
 C324 {272,40}

prB.2: <250> (816)
 #u19.4i {848,76} #u26.17i {796,76} #u10.18o {776,184} #u1.18o {468,184}
 C327 {284,40}

prB.3: <268> (812)
 #u19.2i {848,68} #u26.18i {796,72} #u10.19o {776,180} #u1.19o {468,180}
 C328 {288,40}

preClk: <23> (1028)
 #u53.8o {668,88} #u53.1i {656,64} #u64.12i {300,72} #u64.10i {300,80}
 #u64.5i {288,80} #u64.1i {288,64} #u31.2i {268,148} #u31.4i {268,156}
 #u95.10i {248,160} #u95.4i {236,156} #u94.18i {44,152} #u95.2i {236,148}
 #u31.6i {268,164}

PU: <21> (888)
 #u94.11i {44,180} #u94.1i {32,144} #u86.8i {128,92} #u86.6i {128,84}
 #u86.4i {128,76} #u86.2i {128,68} #u83.1i {16,200} #u82.1i {32,200}
 #u107.6i {48,220} #r1.8i {300,228} #u44.6i {348,164}

PushX: <435> (452)
 #u35.15o {104,172} #u114.17i {460,76}

PushY: <432> (440)
 #u39.10o {128,180} #u114.18i {460,72}

PushZ: <440> (504)
 #u40.14o {64,176} #u114.19i {460,68}

Q.0: <6> (340)
 #r5.1o {256,64} #u60.5i {208,80} #u60.6i {208,84} #u48.3o {176,72}
 #u68.16i {0,124}

Q.15: <313> (208)
 #r4.1o {240,64} #u48.6o {176,84} #u69.21o {108,140}

Q.7: <289> (68)
 #u66.16i {28,124} #u67.21o {80,140}

R.0: <181> (252)
 #u60.3i {208,72} #u60.9o {220,92} #u68.8i {0,92}

R.15: <132> (196)
 #u60.13i {220,76} #u60.7o {208,88} #u48.2i {176,68} #u69.9o {84,96}

R.7: <175> (32)
 #u66.8i {28,92} #u67.9o {56,96}

rA.0: <159> (788)
 #u68.1i {0,64} #u66.1i {28,64} #u67.1i {56,64} #u69.1i {84,64}
 #u26.2o {784,68}

rA.1: <162> (796)
 #u68.2i {0,68} #u66.2i {28,68} #u67.2i {56,68} #u69.2i {84,68}
 #u26.5o {784,80}

rA.2: <161> (796)
 #u68.3i {0,72} #u66.3i {28,72} #u67.3i {56,72} #u69.3i {84,72}
 #u26.6o {784,84}

rA.3: <163> (804)
 #u68.4i {0,76} #u66.4i {28,76} #u67.4i {56,76} #u69.4i {84,76}
 #u26.9o {784,96}


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RawCk: <384> (640)
#u53.12i {668,72} C447 {252,44} #u65.8o {268,224}

RawRef: <45> (92)
#u112.9i {112,232} #u113.9i {128,232} #u39.15o {144,172}

rB.0: <87> (904)
#u68.20i {0,140} #u66.20i {28,140} #u67.20i {56,140} #u69.20i {84,140}
#u102.1i {464,64} #u101.1i {480,64} #u26.12o {796,96}

rB.1: <84> (880)
#u68.19i {0,136} #u66.19i {28,136} #u67.19i {56,136} #u69.19i {84,136}
#u102.15i {476,68} #u101.15i {492,68} #u26.15o {796,84}

rB.2: <81> (864)
#u68.18i {0,132} #u66.18i {28,132} #u67.18i {56,132} #u69.18i {84,132}
#u102.14i {476,72} #u101.14i {492,72} #u26.16o {796,80}

rB.3: <79> (856)
#u68.17i {0,128} #u66.17i {28,128} #u67.17i {56,128} #u69.17i {84,128}
#u102.13i {476,76} #u101.13i {492,76} #u26.19o {796,68}

ReadCmd: <216> (40)
#u107.3i {48,208} #u83.5o {16,216}

ReadDebA': <182> (312)
#u70.12i {272,244} #u70.19i {296,236} #r1.2i {300,204} C438 {216,44}

ReadDebB': <131> (192)
#u41.7o {148,168} #u70.4i {272,212} #u70.25i {296,212}

ReadExtStat': <86> (896)
#u63.11i {828,180} #u52.11i {812,180} #u47.19i {556,68} #u41.8o {148,172}

ReadIB: <455> (620)
#u41.13o {164,180} #u51.2i {672,68}

ReadIB0': <329> (112)
#u62.1i {752,64} #u51.9o {672,96}

ReadIB1': <330> (120)
#u61.1i {768,64} #u51.11o {684,100}

ReadMap': <50> (176)
#u82.5o {32,216} #u108.1i {176,200} #u109.1i {192,200}

ReadMAR': <48> (140)
#u82.4o {32,212} #u97.1i {144,200} #u98.1i {160,200}

ReadMax': <78> (844)
#u112.11i {124,236} #u113.11i {140,236} #u73.12o {916,184}

ReadMD': <47> (124)
#u37.13o {184,180} #u99.1i {96,200} #u100.1i {80,200}

ReadMDR': <52> (196)
#u110.1i {224,200} #u111.1i {208,200} #u82.12o {44,216}

ReadMisc': <67> (492)
#u41.9o {148,176} #u104.1i {512,64} #u104.19i {524,68}

ReadNIA: <341> (376)
#r1.4i {300,212} C442 {232,44} #u86.13i {140,92}

ReadRH': <65> (480)
#u103.19i {508,68} #u103.1i {496,64} #u41.10o {148,180}

RomOCE': <140> (192)
#u6.20i {608,176} #u4.20i {580,176} #u5.20i {552,176} #u3.20i {524,176}
#u2.20i {496,176} #u1.20i {468,176} #u28.6o {428,164}

RomOOE': <138> (180)
#u6.22i {608,168} #u4.22i {580,168} #u5.22i {552,168} #u3.22i {524,168}
#u2.22i {496,168} #u1.22i {468,168} #u28.7o {428,168}

RomICE': <141> (352)
#u10.20i {776,176} #u11.20i {748,176} #u12.20i {720,176} #u14.20i {692,176}
#u13.20i {664,176} #u15.20i {636,176} #u28.8o {428,172}

RomIOE': <142> (356)
#u10.22i {776,168} #u11.22i {748,168} #u12.22i {720,168} #u14.22i {692,168}
#u13.22i {664,168} #u15.22i {636,168} #u28.9o {428,176}

Run: <392> (700)
#r1.7i {300,224} C443 {236,44} #u53.13i {668,68}

SetInterrupt: <471> (748)
#u52.3i {800,152} #u38.12o {84,184}

sh: <139> (184)
#u68.6i {0,84} #u66.6i {28,84} #u67.6i {56,84} #u69.6i {84,84}
#u57.12o {172,72}

Shift': <292> (252)
#u60.14i {220,72} #u57.1i {160,64} #u35.9o {88,176}

StackTrap: <466> (704)
#u71.2i {780,148} #u50.5o {144,80}

StkP.0: <257> (168)

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#u93.3i {320,72}	#u115.3i {432,72}	#u114.11o {460,100}	
StkP.1: <217> {152}			
#u93.6i {320,84}	#u115.6i {432,84}	#u114.12o {460,96}	
StkP.2: <130> {136}			
#u93.11i {332,84}	#u115.11i {444,84}	#u114.13o {460,92}	
StkP.3: <180> {144}			
#u93.14i {332,72}	#u115.14i {444,72}	#u114.14o {460,88}	
Trap: <66> {480}			
#u44.15i {360,148}	#u32.15i {376,148}	#u42.15i {392,148}	#u71.21i {796,148}
#u71.9o {780,176}			
UAddr.0: <109> {84}			
#u91.2o {336,68}	#u79.4i {352,76}	#u80.4i {372,76}	#u78.4i {392,76}
#u81.4i {412,76}			
UAddr.1: <111> {92}			
#u91.7o {336,88}	#u79.3i {352,72}	#u80.3i {372,72}	#u78.3i {392,72}
#u81.3i {412,72}			
UAddr.2: <108> {84}			
#u91.10o {348,88}	#u79.2i {352,68}	#u80.2i {372,68}	#u78.2i {392,68}
#u81.2i {412,68}			
UAddr.3: <14> {68}			
#u91.15o {348,68}	#u79.1i {352,64}	#u80.1i {372,64}	#u78.1i {392,64}
#u81.1i {412,64}			
UAddr.4: <115> {108}			
#u93.2o {320,68}	#u79.21i {368,68}	#u80.21i {388,68}	#u78.21i {408,68}
#u81.21i {428,68}			
UAddr.5: <114> {100}			
#u93.7o {320,88}	#u79.5i {352,80}	#u80.5i {372,80}	#u78.5i {392,80}
#u81.5i {412,80}			
UAddr.6: <107> {84}			
#u93.10o {332,88}	#u79.6i {352,84}	#u80.6i {372,84}	#u78.6i {392,84}
#u81.6i {412,84}			
UAddr.7: <113> {100}			
#u93.15o {332,68}	#u79.7i {352,88}	#u80.7i {372,88}	#u78.7i {392,88}
#u81.7i {412,88}			
UseRom: <376> {428}			
#u28.5i {428,160}	#r1.5i {300,216}	C441 {228,44}	
VCC: <12> {16640}			
#u65.14i {268,200}	#u30.20i {252,200}	#u110.20i {236,200}	#u111.20i {220,200}
#u109.20i {204,200}	#u108.20i {188,200}	#u98.20i {172,200}	#u97.20i {156,200}
#u113.20i {140,200}	#u112.20i {124,200}	#u99.20i {108,200}	#u100.20i {92,200}
#u105.14i {76,200}	#u107.16i {60,200}	#u82.16i {44,200}	#u83.16i {28,200}
#u72.20i {12,200}	#u73.22i {915,144}	#u74.22i {896,144}	#u85.20i {876,144}
#u75.20i {860,144}	#u63.20i {828,144}	#u52.20i {812,144}	#u71.22i {796,144}
#u10.28i {776,144}	#u11.28i {748,144}	#u12.28i {720,144}	#u14.28i {692,144}
#u13.28i {664,144}	#u15.28i {636,144}	#u6.28i {608,144}	#u4.28i {580,144}
#u5.28i {552,144}	#u3.28i {524,144}	#u2.28i {496,144}	#u1.28i {468,144}
#u28.20i {440,144}	#u22.20i {424,144}	#u23.20i {408,144}	#u42.16i {392,144}
#u32.16i {376,144}	#u44.16i {360,144}	#u33.16i {344,144}	#u58.16i {328,144}
#u56.16i {312,144}	#u59.14i {296,144}	#u31.20i {280,144}	#u46.14i {264,144}
#u95.14i {248,144}	#u34.16i {232,144}	#u24.16i {216,144}	#u45.16i {200,144}
#u37.22i {184,144}	#u41.22i {164,144}	#u39.22i {144,144}	#u36.22i {124,144}
#u35.22i {104,144}	#u38.22i {84,144}	#u40.22i {64,144}	#u94.20i {44,144}
#u7.14i {28,144}	#u9.14i {12,144}	#u18.14i {908,64}	#u21.14i {892,64}
#u16.14i {876,64}	#u19.14i {860,64}	#u29.20i {844,64}	#u27.20i {828,64}
#u25.20i {812,64}	#u26.20i {796,64}	#u61.20i {780,64}	#u62.20i {764,64}
#u54.20i {748,64}	#u106.14i {732,64}	#u55.16i {716,64}	#u43.16i {700,64}
#u51.20i {684,64}	#u53.14i {668,64}	#u84.14i {652,64}	#u90.16i {636,64}
#u89.16i {620,64}	#u77.16i {604,64}	#u76.16i {588,64}	#u96.20i {572,64}
#u47.20i {556,64}	#u88.16i {540,64}	#u104.20i {524,64}	#u103.20i {508,64}
#u101.16i {492,64}	#u102.16i {476,64}	#u114.20i {460,64}	#u115.16i {444,64}
#u81.22i {428,64}	#u78.22i {408,64}	#u80.22i {388,64}	#u79.22i {368,64}
#u91.16i {348,64}	#u93.16i {332,64}	#u92.16i {316,64}	#u64.14i {300,64}
#u60.16i {220,64}	#u87.16i {204,64}	#u48.14i {188,64}	#u57.14i {172,64}
#u50.20i {156,64}	#u86.20i {140,64}	#u49.14i {124,64}	#c97.2i {348,260}
#c115.2i {92,260}	#c114.2i {76,260}	#c113.2i {60,260}	#c112.2i {108,260}
#c111.2i {124,260}	#c110.2i {140,260}	#c109.2i {172,260}	#c108.2i {156,260}
#c107.2i {188,260}	#c106.2i {204,260}	#c105.2i {236,260}	#c104.2i {220,260}
#c103.2i {252,260}	#c102.2i {268,260}	#c101.2i {300,260}	#c100.2i {284,260}
#c99.2i {316,260}	#c98.2i {332,260}	#c96.2i {716,256}	#c95.2i {732,256}
#c94.2i {748,256}	#c93.2i {780,256}	#c92.2i {764,256}	#c91.2i {796,256}
#c90.2i {812,256}	#c89.2i {844,256}	#c88.2i {828,256}	#c87.2i {860,256}
#c86.2i {876,256}	#c85.2i {908,256}	#c84.2i {892,256}	#c83.2i {12,260}
#c82.2i {28,260}	#c81.2i {44,260}	#c80.2i {700,256}	#c79.2i {684,256}
#c78.2i {668,256}	#c77.2i {636,256}	#c76.2i {652,256}	#c75.2i {620,256}
#c74.2i {604,256}	#c73.2i {572,256}	#c72.2i {588,256}	#c71.2i {556,256}
#c70.2i {540,256}	#c69.2i {508,256}	#c68.2i {524,256}	#c67.2i {492,256}
#c66.2i {476,256}	#c63.2i {460,256}	#c64.2i {204,256}	#c63.2i {188,256}
#c62.2i {172,256}	#c61.2i {140,256}	#c60.2i {156,256}	#c59.2i {124,256}
#c58.2i {108,256}	#c57.2i {76,256}	#c56.2i {92,256}	#c55.2i {60,256}
#c54.2i {44,256}	#c53.2i {12,256}	#c52.2i {28,256}	#c51.2i {908,200}
#c50.2i {892,200}	#c49.2i {876,200}	#c48.2i {220,256}	#c47.2i {236,256}
#c46.2i {252,256}	#c45.2i {284,256}	#c44.2i {268,256}	#c43.2i {300,256}
#c42.2i {316,256}	#c41.2i {348,256}	#c40.2i {332,256}	#c39.2i {364,256}
#c38.2i {380,256}	#c37.2i {412,256}	#c36.2i {396,256}	#c35.2i {428,256}
#c34.2i {444,256}	#c1.2i {364,200}	#c32.2i {620,200}	#c31.2i {636,200}
#c30.2i {652,200}	#c29.2i {684,200}	#c28.2i {668,200}	#c27.2i {700,200}
#c26.2i {716,200}	#c25.2i {748,200}	#c24.2i {732,200}	#c23.2i {764,200}

#c22.2i {780,200}	#c21.2i {812,200}	#c20.2i {796,200}	#c19.2i {828,200}
#c18.2i {844,200}	#c17.2i {860,200}	#c16.2i {604,200}	#c15.2i {588,200}
#c14.2i {572,200}	#c13.2i {540,200}	#c12.2i {556,200}	#c11.2i {524,200}
#c10.2i {508,200}	#c9.2i {476,200}	#c8.2i {492,200}	#c7.2i {460,200}
#c6.2i {444,200}	#c5.2i {412,200}	#c4.2i {428,200}	#c3.2i {396,200}
#c2.2i {380,200}	C516 {16,48}	E184 {224,4}	E182 {216,4}
E181 {212,4}	E183 {220,4}	E105 {420,0}	E106 {424,0}
E104 {416,0}	E103 {412,0}	#u20.20i {316,200}	#u8.20i {332,200}
#u17.20i {348,200}	#r1.1i {300,200}	#u70.8i {272,228}	#11.10 {832,144}
#u1.26i {468,152}	#u2.26i {496,152}	#u1.27i {468,148}	#u2.27i {496,148}
#u1.1i {444,144}	#u2.1i {472,144}	#u3.1i {500,144}	#u4.1i {556,144}
#u3.27i {524,148}	#u4.27i {580,148}	#u3.26i {524,152}	#u4.26i {580,152}
#u5.26i {552,152}	#u6.26i {608,152}	#u5.27i {552,148}	#u6.27i {608,148}
#u5.1i {528,144}	#u6.1i {584,144}	#u14.1i {668,144}	#u15.1i {612,144}
#u14.27i {692,148}	#u15.27i {636,148}	#u14.26i {692,152}	#u15.26i {636,152}
#u12.26i {720,152}	#u13.26i {664,152}	#u12.27i {720,148}	#u13.27i {664,148}
#u12.1i {696,144}	#u13.1i {640,144}	#u10.1i {752,144}	#u11.1i {724,144}
#u10.27i {776,148}	#u11.27i {748,148}	#u10.26i {776,152}	#u11.26i {748,152}
#r3.2i {284,64}	#r2.2i {236,64}	#r4.2i {252,64}	#r5.2i {268,64}
#u69.10o {84,100}	#u68.10o {0,100}	#u66.10o {28,100}	#u67.10o {56,100}
WriteBank: <388> (224)			
#u33.1i {332,144}	#u39.13o {144,180}		
WriteCmd: <176> (32)			
#u107.2i {48,204}	#u83.12o {28,216}		
WriteDebA': <402> (288)			
#u70.21i {296,228}	#u38.7o {68,168}		
WriteDebB': <55> (268)			
#u70.23i {296,220}	#r1.3i {300,208}	C437 {212,44}	
WriteExtCtrl: <409> (316)			
#u64.4i {288,76}	#u38.8o {68,172}		
WriteIB: <119> (700)			
#u51.3i {672,72}	#u53.2i {656,68}	#u38.14o {84,176}	
WriteIBFront: <426> (412)			
#u51.12o {684,96}	#u64.13i {300,68}		
WriteMAR: <463> (656)			
#u95.9i {248,164}	#u73.7o {900,168}		
WriteMD: <83> (864)			
#u73.10o {900,180}	#u99.11i {108,236}	#u100.11i {92,236}	
WriteMDR: <465> (692)			
#u95.1i {236,144}	#u73.8o {900,172}		
WriteRH: <405> (300)			
#u35.8o {88,172}	#u64.9i {300,84}		
WriteStkP: <436> (464)			
#u38.13o {84,180}	#u115.1i {432,64}		
X.0: <363> (1240)			
#u52.17o {812,156}	#u62.3i {752,72}	#u76.15o {588,68}	#u79.10o {352,100}
#u24.14i {216,152}	#u86.18o {140,72}	#u99.19o {108,204}	#u68.22i {24,136}
X.1: <362> (1144)			
#u52.16o {812,160}	#u62.4i {752,76}	#u77.15o {604,68}	#u79.12o {368,104}
#u86.16o {140,80}	#u99.18o {108,208}	#u68.23i {24,132}	
X.10: <32> (1064)			
#u100.17o {92,212}	#u66.24i {52,128}	#u24.15i {216,148}	#u70.28i {296,200}
#u78.14o {408,96}	#u101.10i {492,88}	#u103.14o {508,88}	#u104.9o {512,96}
#u88.9o {540,92}	#u89.12o {620,80}	#u43.9o {700,92}	#u61.7i {768,88}
X.11: <174> (1268)			
#u68.25i {52,124}	#u100.16o {92,216}	#u70.1i {272,200}	#u34.13i {232,156}
#u78.16o {408,88}	#u101.12i {492,80}	#u104.7o {512,88}	#u88.12o {540,80}
#u103.12o {508,96}	#u61.8i {768,92}	#u43.12o {700,80}	#u90.12o {636,80}
X.12: <24> (1052)			
#u61.13i {780,92}	#u55.4o {704,76}	#u76.11o {588,84}	#u47.18o {556,72}
#u104.18o {524,72}	#u47.9o {544,96}	#u103.9o {496,96}	#u102.4i {464,76}
#u81.10o {412,100}	#u56.12i {312,160}	#u56.10i {312,168}	#u70.2i {272,204}
#u100.15o {92,220}	#u69.22i {108,136}		
X.13: <22> (972)			
#u61.14i {780,88}	#u55.7o {704,88}	#u77.11o {604,84}	#u47.16o {556,80}
#u47.7o {544,88}	#u104.16o {524,80}	#u103.7o {496,88}	#u102.6i {464,84}
#u81.12o {428,104}	#u56.4i {300,156}	#u56.6i {300,164}	#u70.3i {272,208}
#u100.14o {92,224}	#u69.23i {108,132}		
X.14: <128> (1072)			
#u100.13o {92,228}	#u69.24i {108,128}	#u45.4i {188,156}	#u70.6i {272,220}
#u81.14o {428,96}	#u102.10i {476,88}	#u103.5o {496,80}	#u104.14o {524,88}
#u47.5o {544,80}	#u47.14o {556,88}	#u89.11o {620,84}	#u55.9o {716,92}
#u61.17i {780,76}			
X.15: <33> (1212)			
#u61.18i {780,72}	#u55.12o {716,80}	#u90.11o {636,84}	#u104.12o {524,96}
#u47.12o {556,96}	#u47.3o {544,72}	#u103.3o {496,72}	#u102.12i {476,80}
#u81.16o {428,88}	#u24.13i {216,156}	#u24.4i {204,156}	#u69.25i {108,124}
#u100.12o {92,232}	#u70.7i {272,224}		
X.2: <336> (1128)			
#u52.15o {812,164}	#u62.7i {752,88}	#u89.15o {620,68}	#u79.14o {368,96}

#u86.14o {140,88}	#u68.24i {24,128}	#u99.17o {108,212}	
X.3: <335> (1120)			
#u52.14o {812,168}	#u62.8i {752,92}	#u90.15o {636,68}	#u79.16o {368,88}
#u86.12o {140,96}	#u68.25i {24,124}	#u99.16o {108,216}	
X.4: <251> (1040)			
#u63.17o {828,156}	#u62.13i {764,92}	#u76.14o {588,72}	#u96.9o {560,96}
#u80.10o {372,100}	#u45.14i {200,152}	#u67.22i {80,136}	#u99.15o {108,220}
X.5: <277> (1016)			
#u63.16o {828,160}	#u62.14i {764,88}	#u77.14o {604,72}	#u96.7o {560,88}
#u80.12o {388,104}	#u67.23i {80,132}	#u99.14o {108,224}	
X.6: <294> (1024)			
#u63.15o {828,164}	#u62.17i {764,76}	#u89.14o {620,72}	#u96.5o {560,80}
#u80.14o {388,96}	#u67.24i {80,128}	#u99.13o {108,228}	
X.7: <307> (1032)			
#u63.14o {828,168}	#u62.18i {764,72}	#u90.14o {636,72}	#u96.3o {560,72}
#u80.16o {388,88}	#u67.25i {80,124}	#u99.12o {108,232}	
X.8: <8> (1036)			
#u61.3i {768,72}	#u43.4o {688,76}	#u76.12o {588,80}	#u88.4o {528,76}
#u104.3o {512,72}	#u103.18o {508,72}	#u101.4i {480,76}	#u78.10o {392,100}
#u70.26i {296,208}	#u45.13i {200,156}	#u100.19o {92,204}	#u66.22i {52,136}
X.9: <9> (1064)			
#u100.18o {92,208}	#u66.23i {52,132}	#u45.15i {200,148}	#u70.27i {296,204}
#u78.12o {408,104}	#u101.6i {480,84}	#u103.16o {508,80}	#u104.5o {512,80}
#u88.7o {528,88}	#u77.12o {604,80}	#u43.7o {688,88}	#u61.4i {768,76}
XACK/: <18> (624)			
#u94.12i {44,176}	#u94.14i {44,168}	E123 {492,0}	
XBus+Rot': <68> (628)			
#u90.13i {636,76}	#u89.13i {620,76}	#u77.13i {604,76}	#u76.13i {588,76}
#u36.9o {108,176}			
XHigh=0': <331> (572)			
#u96.19i {572,68}	#u86.1i {128,64}	#u36.7o {108,168}	
XLow+Byte': <444> (536)			
#u36.10o {108,180}	#u88.1i {528,64}		
XLow+Const': <17> (540)			
#u47.1i {544,64}	#u88.15i {540,68}	#u36.12o {124,184}	
XLow+IB': <20> (720)			
#u106.1i {720,64}	#u55.15i {716,68}	#u43.15i {700,68}	#u36.8o {108,172}
Y.0: <200> (816)			
#u76.4i {576,76}	#u79.9i {352,96}	#u110.2i {224,204}	#u109.2i {192,204}
#u97.2i {144,204}	#u68.39o {24,68}		
Y.1: <201> (836)			
#u77.4i {592,76}	#u79.11i {352,104}	#u110.3i {224,208}	#u109.3i {192,208}
#u97.3i {144,208}	#u68.38o {24,72}		
Y.10: <80> (860)			
#u89.2i {608,68}	#u89.6i {608,84}	#u78.13i {408,100}	#u30.7i {240,224}
#u111.4i {208,212}	#u98.4i {160,212}	#u66.37o {52,76}	
Y.11: <85> (880)			
#u90.2i {624,68}	#u90.6i {624,84}	#u78.15i {408,92}	#u30.8i {240,228}
#u111.5i {208,216}	#u98.5i {160,216}	#u66.36o {52,80}	
Y.12: <94> (1096)			
#u30.13i {252,228}	#u111.6i {208,220}	#u98.6i {160,220}	#u69.39o {108,68}
#u92.3i {304,72}	#u33.3i {332,152}	#u66.11i {312,164}	#u115.4i {432,76}
#u81.9i {412,96}	#u76.3i {576,72}	#u76.7i {576,88}	
Y.13: <88> (908)			
#u77.3i {592,72}	#u77.7i {592,88}	#u115.5i {432,80}	#u81.11i {412,104}
#u92.6i {304,84}	#u56.5i {300,160}	#u33.6i {332,164}	#u30.14i {252,224}
#u111.7i {208,224}	#u98.7i {160,224}	#u69.38o {108,72}	
Y.14: <90> (1060)			
#u45.3i {188,152}	#u69.37o {108,76}	#u98.8i {160,228}	#u111.8i {208,228}
#u30.17i {252,212}	#u33.10i {344,168}	#u92.10i {316,88}	#u81.13i {428,100}
#u115.12i {444,80}	#u89.7i {608,88}	#u89.3i {608,72}	
Y.15: <95> (1168)			
#u98.9i {160,232}	#u69.36o {108,80}	#u24.3i {204,152}	#u111.9i {208,232}
#u30.18i {252,208}	#u33.13i {344,156}	#u92.13i {316,76}	#u115.13i {444,76}
#u81.15i {428,92}	#u90.3i {624,72}	#u90.7i {624,88}	
Y.2: <202> (856)			
#u89.4i {608,76}	#u79.13i {368,100}	#u110.4i {224,212}	#u109.4i {192,212}
#u97.4i {144,212}	#u68.37o {24,76}		
Y.3: <203> (876)			
#u90.4i {624,76}	#u79.15i {368,92}	#u110.5i {224,216}	#u109.5i {192,216}
#u97.5i {144,216}	#u68.36o {24,80}		
Y.4: <73> (804)			
#u76.1i {576,64}	#u76.5i {576,80}	#u80.9i {372,96}	#u110.6i {224,220}
#u109.6i {192,220}	#u97.6i {144,220}	#u67.39o {80,68}	
Y.5: <75> (824)			
#u77.1i {592,64}	#u77.5i {592,80}	#u80.11i {372,104}	#u110.7i {224,224}

	#u109.7i {192,224}	#u97.7i {144,224}	#u67.38o {80,72}	
Y.6: <77> (844)	#u89.1i {608,64}	#u89.5i {608,80}	#u80.13i {388,100}	#u110.8i {224,228}
	#u109.8i {192,228}	#u97.8i {144,228}	#u67.37o {80,76}	
Y.7: <82> (864)	#u90.1i {624,64}	#u90.5i {624,80}	#u80.15i {388,92}	#u110.9i {224,232}
	#u109.9i {192,232}	#u97.9i {144,232}	#u67.36o {80,80}	
Y.8: <74> (804)	#u76.2i {576,68}	#u76.6i {576,84}	#u78.9i {392,96}	#u30.3i {240,208}
	#u111.2i {208,204}	#u98.2i {160,204}	#u66.39o {52,68}	
Y.9: <76> (824)	#u77.2i {592,68}	#u77.6i {592,84}	#u78.11i {392,104}	#u30.4i {240,212}
	#u111.3i {208,208}	#u98.3i {160,208}	#u66.38o {52,72}	
YH.0: <146> (512)	#u103.2i {496,68}	#u101.5o {480,80}	#u108.2i {176,204}	#u113.4i {128,212}
YH.1: <145> (508)	#u103.4i {496,76}	#u101.7o {480,88}	#u103.3i {176,208}	#u113.5i {128,216}
YH.2: <28> (504)	#u103.6i {496,84}	#u101.9o {492,92}	#u108.4i {176,212}	#u113.6i {128,220}
YH.3: <29> (512)	#u101.11o {492,84}	#u103.8i {496,92}	#u108.5i {176,216}	#u113.7i {128,224}
YH.4: <263> (548)	#u103.11i {508,100}	#u102.5o {464,80}	#u108.6i {176,220}	#u113.8i {128,228}
YH.5: <245> (540)	#u103.13i {508,92}	#u102.7o {464,88}	#u108.7i {176,224}	#u112.6i {112,220}
YH.6: <220> (544)	#u103.15i {508,84}	#u102.9o {476,92}	#u108.8i {176,228}	#u112.7i {112,224}
YH.7: <221> (556)	#u103.17i {508,76}	#u102.11o {476,84}	#u108.9i {176,232}	#u112.8i {112,228}
ZeroMP: <429> (416)				
	C513 {4,48}	#u30.16o {252,216}		