WANG

6200

VS I/O STRUCTURE AND THE IOP MOTHERBOARD

Models:

209-7110
209-7810

Customer Engineering
Product Maintenance Manual

741-0824

PREFACE

Every I/O interface on a VS 80, 85, 90 or 100 system consists of an IOP Motherboard (IOPMB) as a motherboard and a Device Adapter (DA) as a daughterboard. This manual covers the way in which the operating system and the peripheral device communicate with each other. Information about specific DA daughterboards is not provided here.

There are several other publications related to this document. The VS Data Processing Field Guide, part number 729-1265-A, is a handbook summarizing the operating system information which is covered here in chapter 2. The VS 80 Reference Guide, part number 741-0716, is a handbook containing IOP part numbers for VS 80 machines. The VS Service Handbook, part number 729-1098-A, is a handbook containing part number information for VS 85, 90 and 100 IOPs.

This manual obsoletes 729-0824 and its update 729-0941.

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DIAGNOSTICS HANDBOOK

VS I/O STRUCTURE AND THE IOP MOTHERBOARD

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TABLE OF CONTENTS

VS I/O STRUCTURE AND THE IOP MOTHERBOARD

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VS I/O STRUCURE AND THE IOP MOTHERBOARD
741-0824

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CHAPTER 1
OVERVIEW

INTRODUCTION

The operating system of a computer is the entity which manages system resources and assigns those resources to the programs and applications running under it. One of the resources controlled by the operating system is the I/O subsystem. The I/O subsystem consists of all the devices attached to the system, of their interfaces and controllers, and of the manner in which they communicate.

This manual was written to help CE understand the the I/O subsystem in both intermediate and large VS systems. It explains the protocol used in communications between the CP and the I/O devices. It also provides an overview of the hardware involved in this information exchange. By discussing both software and hardware issues, this manual attempts to show a complete picture of I/O operations.

Chapter 1 introduces the manual itself and provides an I/O overview.

Chapter 2 describes how the operating system communicates with the I/O Processors (IOPs).

Chapter 3 provides a block diagram description of the IOP Motherboard (IOPMB).

Chapter 4 describes how the IOPMB communicates via each of its three interfaces.

Appendix A provides the instruction set used in the PROMs on the IOP.

Appendix B provides schematics for the two IOPMBs covered by this manual.

ACRONYMS

The following acronyms are used for elements of the I/O subsystem of VS machines.

Acronym	Definition
IOPMB	IOP Motherboard.
CIO	Control I/O instruction (privileged).
CP	Central Processor.
CP3	Central Processor of a VS 80 system.
CP4	Central Processor of a VS 85, 90 or 100 system.
CP5	Central Processor of a VS 15, 25 or 45 system.
DA	Device Adapter.
DLI	Device-Level Interface.
DLP	Device-Level Processor, i.e., the microprocessor which is the intelligence of the device itself (often a Z80), not the IOPMB's Microprocessor logic.
IOCA	I/O Command Area or I/O Command Address.
IOCT	I/O Command Table.
IOCW	I/O Command Word.
IOP	I/O Processor, a two-board assembly consisting of an IOP Motherboard and a Device Adapter.
IOPMB	I/O Processor Motherboard.
IOSW	I/O Status Word.
HIO	Halt I/O instruction (privileged).
PCB	Processor Communications Bus.
SIO	Start I/O instruction (privileged).
XIO	Execute I/O instruction.

IOP FUNCTIONS

Input/Output Processors are used to control input/output requests to both serial and parallel devices in intermediate and large VS computer systems (VS 80/85/90/100). The position occupied by the IOP in the systems is shown in Figures 1-1 and 1-2.

The operating system executing in the central processor (CP) starts an IOP's functions, but, once started, the IOP is able to perform the operation independently of the CP. Meanwhile, the CP places the program requiring I/O on hold and executes some other program. In this manner, the IOP and the CP perform concurrent processing.

Every IOP consists of a IOP Motherboard as a motherboard and a Device Adapter as a daughterboard. The IOPMB interfaces to the system buses and translates CP commands into functions for the DA. The DA furnishes the direct link to any attached devices.

There are two types of motherboards used in IOPs. The first model is the 209-7110 board. The second model is the 209-7810 board.

The difference between IOPMB models is in how many addresses each can handle. Both IOPMB boards handle up to 16 devices. On the 7110 IOPMB, these 16 devices may have only 16 different addresses. On the 7810 IOPMB, however, these 16 devices may have up to 32 addresses. This means that the 7810 may handle devices like archiving workstations which have separate addresses for the floppy disk drive and the workstation itself. The 7110 can handle only regular workstations which do not need a second address.

Figure 1-1
Printed Circuit Boards in a VS 80

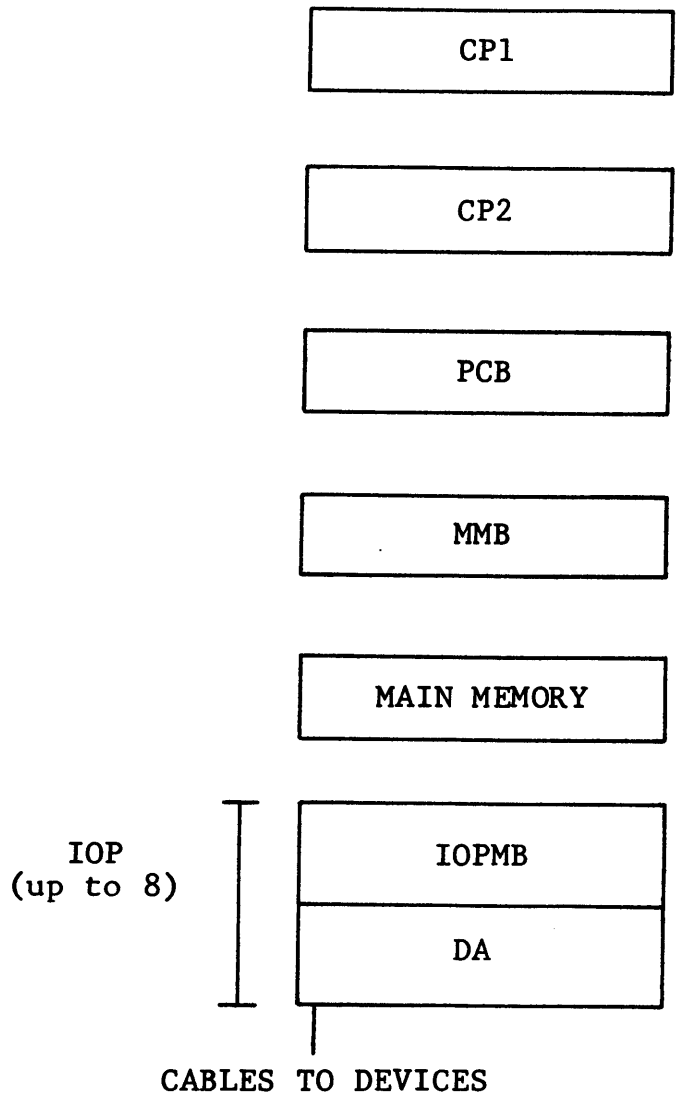
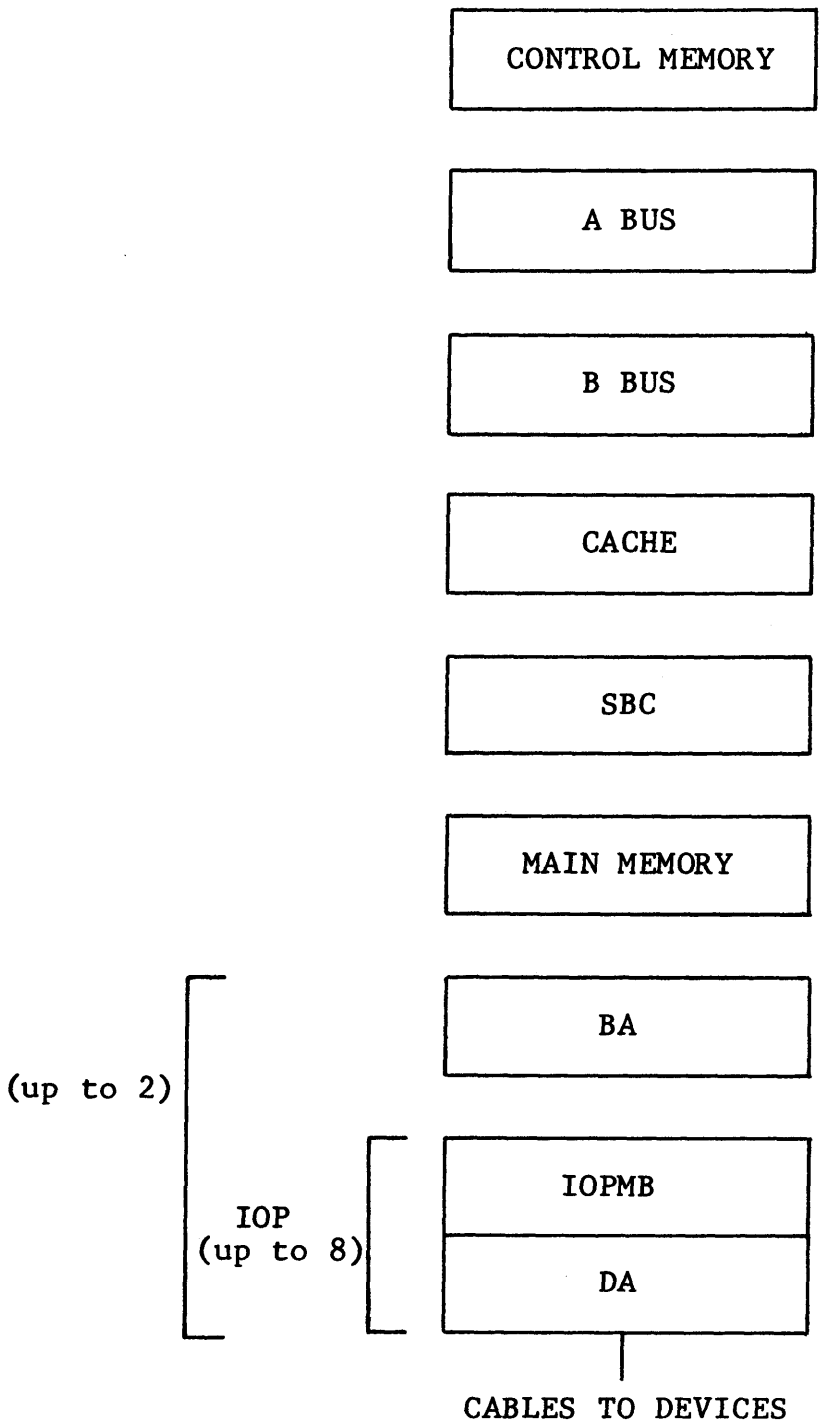


Figure 1-2
Printed Circuit Boards in a VS 100



CHAPTER 2
I/O PROTOCOL

OVERVIEW

The protocol of the I/O subsystem consists of two things:

- the format in which commands and responses are communicated and
- the order in which operations are performed.

This chapter concentrates on the format in which commands and responses are communicated. Chapter 4 discusses the order in which I/O operations are performed.

The protocol established between the VS operating system and the IOPs hinges on the I/O Command Word (IOCW) and the I/O Status Word (IOSW). The CP and all IOPs in the system use the same IOCW/IOSW structure when executing the I/O instructions.

This chapter discusses:

- the format of the IOCWs,
- the format of the IOSWs, and
- the privileged I/O instructions.

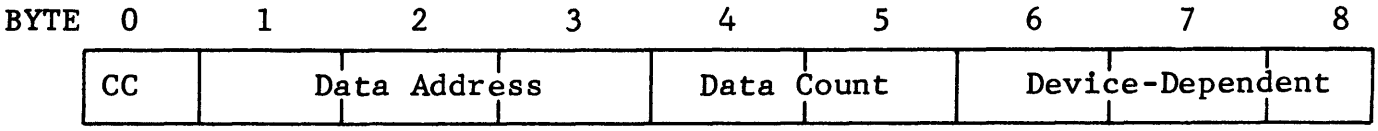
REFERENCE DOCUMENTATION

- VS Principles of Operation, part number 800-1100PO-04, describes the SIO, CIO and HIO instructions and the algorithms for memory addressing. (RR addressing is used.)
- The VS Data Processing Field Guide, part number 729-1265-A, is a small handbook summarizing the operating system.

IOCW

IOCW Contents: The IOCW is generated by the VS operating system to communicate to the IOP specific information about the requested I/O operation. This information consists of four fields of data. The four data fields are:

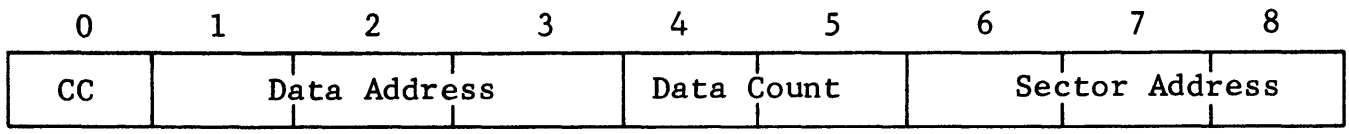
- o Command Code: the type of operation to be performed.
- o Data Address: the starting address for main memory data.
- o Data Count Field: the number of bytes of data to be transferred.
- o Device-Dependent Section: various types of information, depending on the device.



IOCW Storage: Once the operating system has generated an IOCW, it places the IOCW in main memory. To aid the IOP in locating the IOCW, the operating system then leaves this storage address at another place in main memory. This place is called the I/O Command Area or the I/O Command Address. Both are abbreviated as the IOCA.

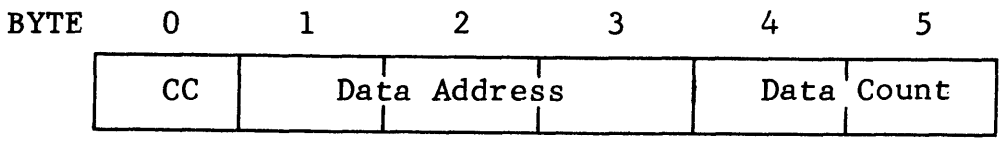
The address of this address storage place is known to the IOP involved: it is a function of the device address. The IOP goes to this preliminary address to find the pointer to the actual I/O Command Word. The particular protocol about where to store the storage address depends on the CP in which the operating system is executing.

DISK IOCW FORMAT



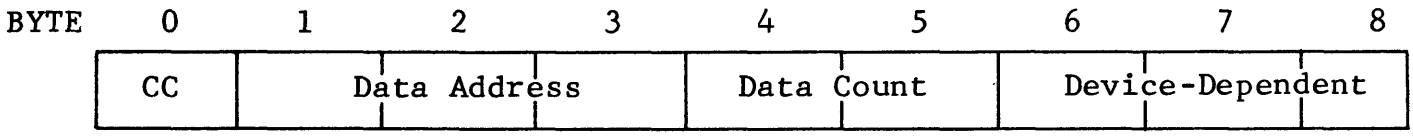
Byte	Hex Value	Description
0	Command Code:	
	00	Fixed platter.
	01	Removable platter.
	02	Indirect addressing is used in the Data Address field.
	04	Suppress retry on errors.
	08	Use Diagnostic Mode.
	40	Read.
	80	Write.
	A0	Write/verify.
	C0	Seek.
	E0	Format.
1-3	Data Address:	
	0-512K	Main memory physical address of data area. If indirect addressing is in use, this contains the address of the start of the Indirect Address List.
4-5	Data Count:	
		Number of bytes to be transferred (in hexadecimal), depends on the type of disk:
	100	Ten-Meg drives, floppy drives.
	800	75/288 Meg drives, 30/60/90 Meg drives.
6-8	Device-Dependent: Sector Address	
		Sector at which transfer starts, ranges from 0 to maximum for that particular disk.

TAPE IOCW FORMAT



Byte	Hex Value	Description
0	Command Code:	
	01	Selects low increment values. Can be added to other values below.
	02	Selects indirect addressing for Data Address Field. Can be added to other values below.
	40	Read data.
	80	Write data.
	C0	Sense.
	D0	Erase.
	D4	Write tape mark.
	D8	Forward space block.
	DC	Forward space file.
	E0	Rewind.
	E4	Rewind and unload.
	E8	Back space block.
	EC	Back space file.
	F0	Kennedy: Set density high. Telex: Set PE mode.
	F4	Kennedy: Set density low. Telex: Set NRZI mode.
	F8	Kennedy: Set parity odd. Telex: Set GCR mode.
	FC	Kennedy: Set parity even. Telex: Set drive-selected mode.
1-3	Data Address:	
	0-512K	Main memory physical address of data area. If indirect addressing is in use, this contains the address of the start of the Indirect Address List.
4-5	Data Count:	
		Number of bytes to be transferred.
6-8	Device-Dependent: Not used for tapes.	

SERIAL IOCW FORMATS



Byte	Hex Value	Description
0		Command Code:
		Interpretation of this area by the IOP depends on whether it is passed to the IOP under an SIO or a CIO instruction. The two possibilities are listed separately below.
0 for SIO:		
	40	Read data from the device.
	44	Read the tab settings.
	48	Read the diagnostic code.
	4C	7810 IOPs: Interrogate.
	50	Read altered.
	80	Write data to the device.
	84	Write the tab settings.
	90	Write selected.
	C0	Control device. When this command is issued, the rest of the IOCW is passed on to the device for use as an immediate operand. Do not use any DMA operations when using the C0 option.
0 for CIO:		
	40	Read the Device Routing Table from the Device-Level Processor to main memory. 1024 bytes total.
	60	Read the device's microcode.
	80	Load the Device Configuration Table from main memory into the Device-Level Processor. 64 bytes total.
	90	Load the Device-Level Processor microcode. This microcode resides not on the IOP but in the peripheral itself.
	A0	Load device microcode.
	A8	Read the Device Routing Table from the Device-Level Processor to main memory. 1024 bytes total.

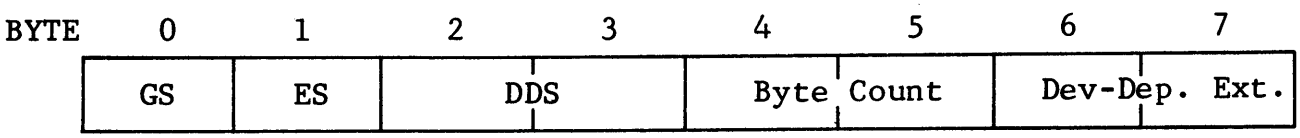
Serial IOCWs, continued

Byte	Hex Value	Description
0	Command Code for CIO, continued:	
	C0	Reinitialize the Device-Level Processor and restart the IOP.
	D0	Restart the Device-Level Processor.
	E0	Restart the Device Processor.
	F0	Control resources.
1-3	Data Address:	
	0-512K	Main memory physical address of data area. If indirect addressing is in use, this contains the address of the start of the Indirect Address List.
4-5	Data Count:	
		Size of the valid data buffer for this I/O request. The device is allowed an unlimited number of accesses to this buffer. The only requirement is that it stay within the boundaries defined by this field and the Data Address field.
6-8	Device-Dependent:	
	For SIO commands:	passed unaltered to device. Can be used as anything desired.
	For CIO commands:	Device RAM Address.

IOSW

IOSW Contents: The IOP generates an IOSW to communicate to the CP the outcome of the I/O operation. Each IOSW can have up to 8 bytes of information. This information consists of five fields of data as follows:

- o General Status Byte: indicates whether the operation was successfully completed or if a hard or soft error occured.
- o Error Status Byte: indicates the type of error which occured.
- o Device-Dependent Status Bytes: vary according to device type.
- o Residual Byte Count: tells the operating system how much of the job remained to be done at the time the IOSW was logged.
- o Device-Dependent Extension: varies both in length and in meaning by device type.

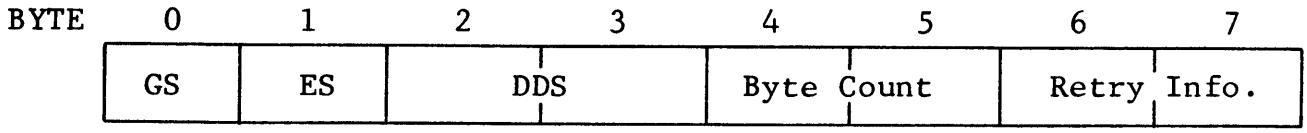


IOSW Storage: Once the operation is complete, the IOP stores the IOSW in main memory. The address at which it is stored depends on the type of CP in which the operating system is executing.

For a CP3-based system, the IOSW is written into main memory beginning at location 0000 0000.

For a CP4-based system, the IOSW is written into an operating system table. Then, as soon as the IOP notifies the operating system that the operation is completed, the operating system re-writes this IOSW into location 0000 0000.

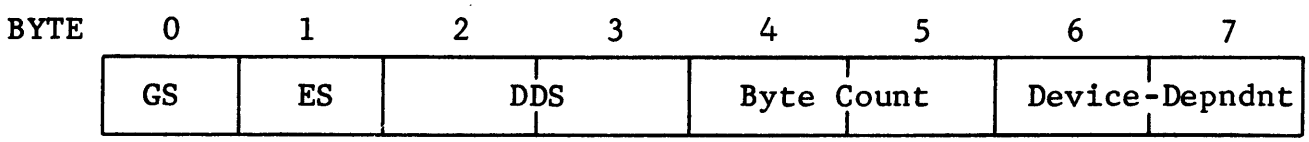
DISK IOSW FORMAT



Byte	Hex Value	Description
0		General Status:
	80	IRQ: Intervention required.
	40	NC: Normal completion.
	20	EC: Error Completion. When both NC and EC are set, a soft error occured. When only EC is set, the error was a hard error.
	10	U: Unsolicited interrupt.
	08	PC: IOP/DLP now ready.
	04, 02, 01	Reserved for future use by the operating system.
1		Error Status:
	80	IC: Invalid command.
	40	MPE: Memory parity error.
	20	MAE: Memory address error.
	10	DM: Device malfunction.
	08	DAM: Device memory error, or device damaged.
	04, 02, 01	Reserved for future use by the operating system.
2-3		Device-Dependent Status Information:
2	80	HDF: Header reformatted.
	40	HDS: Header skipped.
	20	DIA: Diagnostic mode.
	10	OPT: Optimization was used.
	08	IDA: Invalid disk address.
	04	IDC: Invalid data count.
	02	SO: Sector overrun.
	01	SI: Seek incomplete.

Byte	Hex Value	Description
2-3		Device-Dependent Status Information continued
3	80	WP: Write-protected.
	40	NRO: Disk not ready.
	20	ST: Sector time-out.
	10	DCE: Data compare error.
	08	HDE: Header check.
	04	CRC: Cyclical redundancy check.
	02	O: Memory overrun.
	01	ISP: Short sector.
4-5		Residual Byte Count:
		When there is an error completion, these two bytes contain the number of bytes of data that remain to be transferred.
6		Retry Information:
		First digit describes the retry set-up and second digit (n) shows the error count.
	0n	Normal.
	1n	Data strobe early.
	2n	Data strobe late.
	3n	Offset minus.
	4n	Offset plus.
	5n	Data strobe early and offset plus.
	6n	Data strobe late and offset plus.
	7n	Data strobe early and offset minus.
	8n	Data strobe late and offset minus.
	9n	ECC used.

TAPE IOSW FORMAT

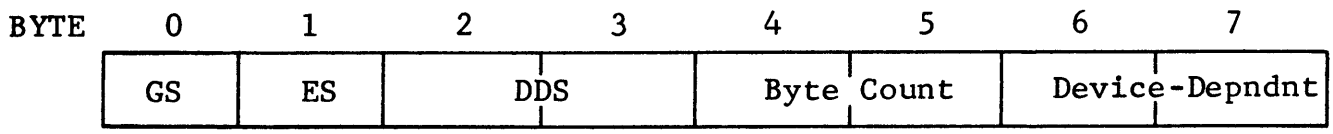


Byte	Hex Value	Description
0		General Status:
	80	IRQ: Intervention required.
	40	NC: Normal completion.
	20	EC: Error Completion. When both NC and EC are set, a soft error occured. When only EC is set, the error was a hard error.
	10	U: Unsolicited interrupt.
	08	PC: IOP/DLP now ready.
	04, 02, 01	Reserved for future use by the operating system.
1		Error Status:
	80	IC: Invalid command.
	40	MPE: Memory parity error.
	20	MAE: Memory address error.
	10	DM: Device malfunction.
	08	DAM: Device memory error, or device damaged.
	04	IL: Incorrect length.
	02, 01	Reserved for future use by the operating system.
2-3		Device-Dependent Status Information:
2	80	VRC: Vertical redundancy check.
	40	LRC: Longitudinal redundancy check.
	20	CRC: Cyclical redundancy check.
	10	On write only: SC: Skew check. On read only: NB: Noise block.
	08	IMODE: Incorrect mode.
	04	PHASE: PE ID burst indicator detected.

Tape IOSW formats, continued

Byte	Hex Value	Description
2-3		Device-Dependent Status Information continued
2	02	Kennedy: DS1: Drive type (0 is for 9-track drives and 1 is for 7-track drives). Telex: 0.
	01	Kennedy 7-Track only: DS2: Even Parity. All others: 0.
1	80	FP: File is write-protected.
	40*	Kennedy: DS3: Recording mode (0 is for PE and 1 is for NRZI). Telex: see below.
	20*	Kennedy: DS4: Density (0 is for high and 1 is for low). Telex: see below.
	10	LP: Load point.
	08	TM: Tape mark detected.
	04	EOT: End of tape detected.
	02	O: FIFO overflow or underflow.
	01	OFF: Offline.
	*Telex: bits 40 and 20 00 PE. 01 NRZI. 10 GCR. 11 Drive selected mode.	
4-5		Residual Byte Count: When there is an error completion, these two bytes contain the number of bytes of data that remain to be transferred.
6		Error Retry Count: Number of times IOP attempted unsuccessfully to complete the I/O operation normally.
7		Reserved for future use of the operating system.

SERIAL IOSW FORMAT



Byte	Hex Value	Description
0		General Status:
	80	IRQ: Intervention required.
	40	NC: Normal completion.
	20	EC: Error Completion.
	10	U: Unsolicited interrupt.
	08	PC: IOP/DLP now ready.
	04	DAR: Data area early released. Means that the page in main memory is now released for use by other programs.
	02, 01	Reserved for later use by the operating system.
1		Error Status:
	80	IC: Invalid command.
	40	MPE: Memory parity error.
	20	MAE: Memory address error.
	10	DM: Device malfunction.
	08	DAM: Device memory error, or device damaged.
	04	IL: Incorrect length.
	02	PP: Peripheral processor (Device-Level Processor) needs microcode.
	01	DP: Device Processor needs microcode.
2-3		Device-Dependent Status Information:
2	All values	Used by telecommunications controllers as the AID character.

Serial IOSW Formats, continued

Byte	Hex Value	Description
3		Device Information:
	x0	Value of first digit represents device type.
		Note that the second digit is zero for telecommunications controllers.
	0x	For non-TC controllers, the following apply:
	01	DNR: Device Processor not running or halted. IPL requested.
	02	DCE: Device cable error.
	04	DPE: Device parity error.
	08	DPO: Device is powered-on.
4-5		Residual Byte Count:
		When there is an error completion, these two bytes contain the number of bytes of data that remain to be transferred.
		In 22V27 SIOPs operating in VS 100 machines, if byte 4 is 00, byte 5 can contain any of the following error codes:
	00	Invalid BA command.
	01	BCC error.
	02	Memory address error.
	03	IOP/BA parity error.
6-7		Device-Dependent: Extended Error Codes
		Used with telecommunications controllers. For serial controllers, these two bytes pass unaltered between the IOP and main memory.

I/O INSTRUCTIONS

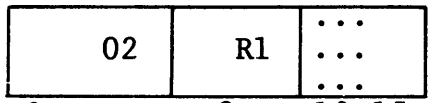
Whenever a program requires I/O, it calls on the operating system using the XIO instruction. It is the operating system which then actually orders the IOP to perform the I/O. The three instructions the operating system uses are privileged, i.e., only the operating system may use these three instructions. This means that the CP must be in supervisor state.

- Start I/O (SIO) is the privileged instruction which institutes I/O operation.
- Control I/O (CIO) is the privileged instruction which performs different types of operations with the device's intelligence.
- Halt I/O (HIO) is the privileged instruction which immediately terminates an I/O operation.

All instructions use the RR addressing capabilities.

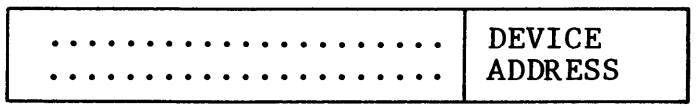
START I/O

SIO R1



The operating system uses the SIO command to initiate an I/O operation for the I/O device whose address is in R1. The instruction START I/O is executed only when the system is in the supervisor state.

The register specified by R1 contains the I/O device address in the following format.



Before the SIO instruction is issued, the operating system stores the IOCW in memory then loads the pointer to the IOCW at the correct main memory address for the device in question.

After the SIO instruction is issued, the I/O operation will take place provided the addressed device and the IOP are available. Under any of the following conditions, the I/O operation will not take place:

- The IOP is not connected or operational.
- The IOP is busy.
- The device is busy with a previous IOCW.

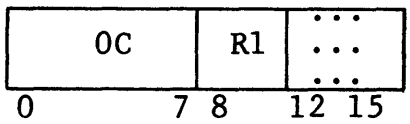
After the SIO instruction is executed, the operating system cannot change the IOCW until the completion interrupt is received from the IOP.

When the IOP receives the IOCW, it returns a condition code. The various condition codes which can result from this operation are:

0 SIO instruction is accepted by IOP and operation is proceeding.
1 The device is busy with a previous operation.
2 IOP BUSY is true.
3 The IOP is not operational.

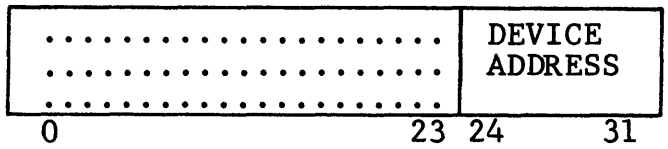
CONTROL I/O

CIO R1



CIO commands the IOP to perform its control function. In most cases, this means that the IOP loads microcode for the Device-Level Processor.

The register specified by R1 contains the I/O device address in the following format.



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- The IOP is not connected or operational.
- The IOP is busy.
- The device is busy with a previous IOCW.

Not all devices support CIO. When issued for a device for which control is not accepted, the 0 condition code is returned and program execution continues.

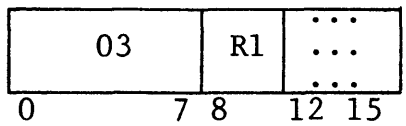
The various condition codes which can result from this operation are:

0 Means one of two things:
  - CIO instruction is accepted by IOP and operation is proceeding.
  - This device cannot accept a CIO instruction.

1 The device is busy with a previous operation.
2 IOP BUSY is true.
3 The IOP is not operational.

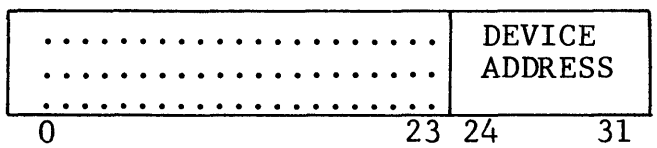
HALT I/O

HIO R1



HIO commands the IOP to immediately terminate activities in the addressed device.

The register specified by R1 contains the I/O device address in the following format.



Not all devices support HIO. When issued for a device for which control is not accepted, the 0 condition code is returned and program execution continues.

HIO clears all interrupts that may be pending for the device. In addition, if any I/O operations are currently going on, HIO terminates them as well. If a current operation is terminated, a completion interrupt will be generated. The IOSW that the IOP places in main memory may or may not have the Error Completion and Incorrect Length bits set to 1.

The various condition codes which can result from this operation are:

0 Means one of two things:

- o HIO instruction is accepted by IOP and operation is proceeding.
- o This device cannot support the HIO instruction.

1 The device is busy with a previous operation.

2 IOP BUSY is true.

3 The IOP is not operational.

CHAPTER 3
IOPMB BLOCK DIAGRAM

INTRODUCTION

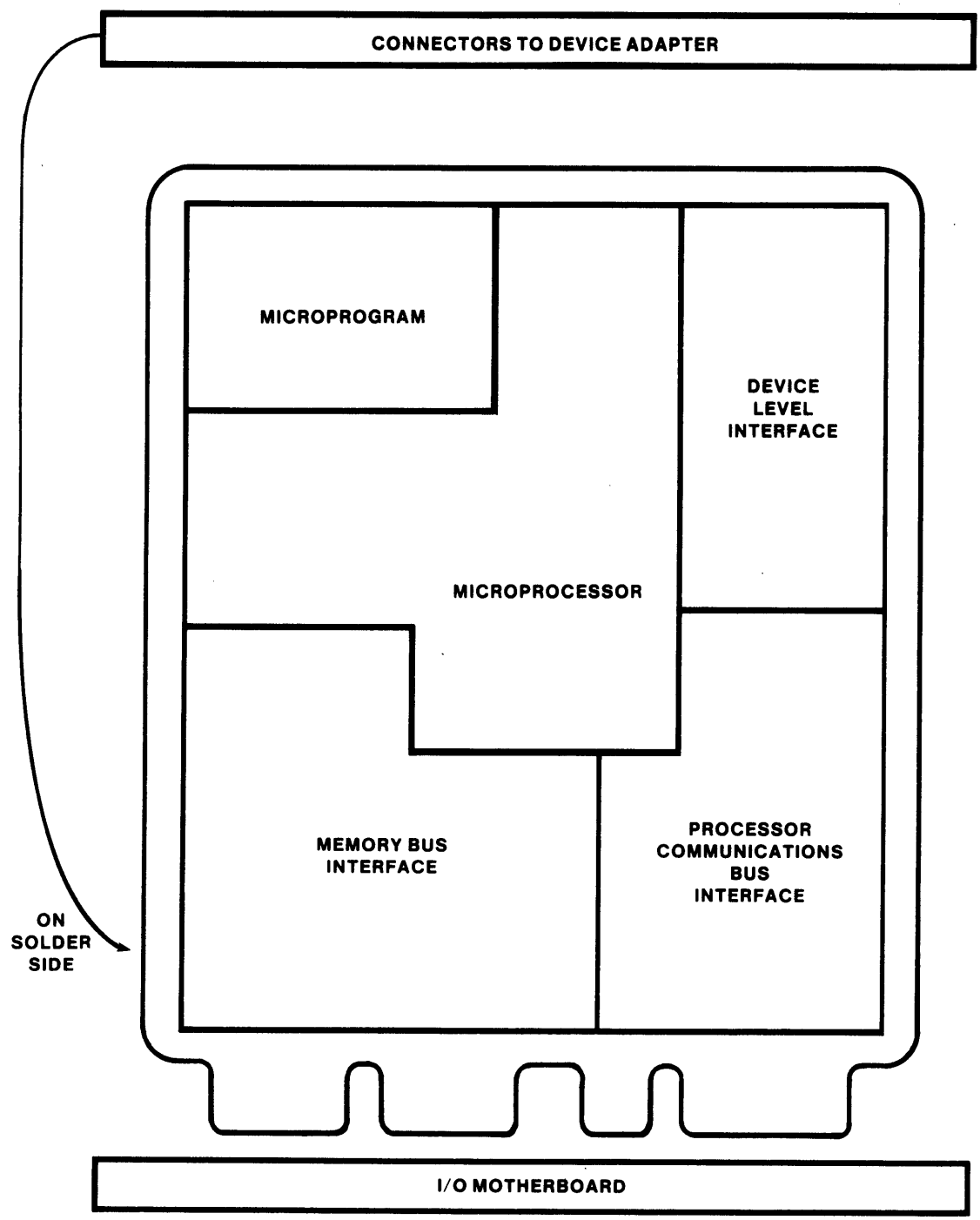
This chapter provides a block diagram of the IOPMB portion of an IOP assembly. The block diagram presents the logic at the functional level. Block diagrams for the DA portion are covered in the pertinent Product Maintenance Manuals.

Overall, there are five major functional areas on the IOP Motherboard.

- o Intelligence:
  - Microprogram
  - Microprocessor
- o Interfaces:
  - Memory Bus Interface
  - Processor Communications Bus Interface
  - Device Level Interface

Figure 3-1 presents a simple view of a IOP Motherboard. Each of these five functional blocks are discussed separately below.

Figure 3-1
Simple Block Diagram of IOPMB



MICROPROGRAM

The Microprogram section of the IOPMB is diagrammed in detail in Figure 3-2. This function of the IOPMB consists of the Control Memory which stores the IOPMB microcode and of the Parity Testing Circuit which checks this microcode for errors.

The Control Memory consists of PROMs. The PROMs vary from one IOP to the next. Each set of PROMs contains the particular microcode program which drives the IOPMB for use in a specific environment. One set of PROMs makes the IOPMB run large disks; another set makes the IOPMB run workstations and printers.

Control Memory has 4 kilowords of 16 bits. It is the Microprocessor section which addresses the PROMs and latches the control word output.

The Parity Testing Circuit includes both a parity storage PROM and a parity generation chip. As each control word is read into the Microprocessor section, the parity generator creates the correct parity bit for the word. This bit is then checked against the stored parity bit from the PROM. If the two bits do not match, the Parity Testing Circuit generates an error signal called PED for Parity Error Detect.