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2

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LIST OF ILLUSTRATIONS

LIST OF TABLES

This chapter contains block level theory of operation discussions for the subassemblies of the 4230/05 Workstations. The equipment is covered in the subsections of this chapter as listed below.

Section 2.1 Monitor
Section 2.2 Keyboard
Section 2.3 Electronics Base
Section 2.4 4230 TC Option
Section 2.5 4230/05 Arabic WS

2.1 MONITOR

The Monitor unit (figure 2-1) contains a 12-inch green-on-black CRT with a Monitor PCA to process video and synchronization signals. The CRT screen has a capacity of 25 lines with 80 characters per line for a total of 2000 characters displayed.

The Monitor PCA receives +12 Vdc from the switching power supply in the Electronics Base via one lead of the Monitor power cable assembly. The +12 Vdc directly supplies the higher current horizontal deflection circuitry and the CRT filament. A series regulator is used to derive a +5 Vdc supply from the +12 Vdc input for the logic devices on the Monitor PCA.

Input signals to the Monitor PCA include VIDEO, HSYNC, VSYNC and INTEN which are generated in the Electronics Base of the particular model Workstation. These signals are applied to the Monitor PCA via the eight-pin monitor video cable, buffered and then presented to the appropriate circuits on the PCA.

2.1 MONITOR (Continued)

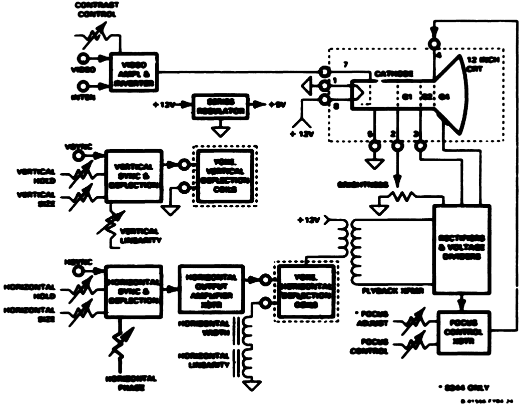

Figure 2-1. Monitor PCA Block Diagram

2.1 MONITOR (Continued)

The VIDEO input is applied to a common-emitter stage in the video amplifier and inverter which provides amplification and inversion of the incoming video signal. The amplified and inverted video drives the cathode of the 12-inch (diagonal) CRT. A special portion of the video amplifier and inverter receives the INTEN signal, which is used to intensify or highlight selected characters on the CRT screen. The INTEN signal causes the CRT cathode voltage to decrease, causing an increase in intensity for the instant that the INTEN sig- nal is present. The front-panel contrast control adjusts the extent to which the circuit reacts to the INTEN signal.

The horizontal sync (HSYNC) input is applied to the horizontal sync and deflection circuitry, comprising a horizontal processor device followed by a driver and, finally, the horizontal output amplifier. The horizontal phase and horizontal hold adjustments are inputs to the horizontal sync and deflection device and provide for a phase and frequency-stable horizontal deflection ramp to be fed to the output stage.

The horizontal output transistor feeds the horizontal deflection coils of the yoke with a sawtooth-type deflection waveform. The current in the yoke windings develops an electro-magnetic field for deflecting the CRT electron beam in the horizontal direction. Adjustments for horizontal width and horizontal linearity form part of the total horizontal deflection coil load.

2.1 MONITOR (Continued)

At horizontal retrace (flyback), the current field in the horizontal deflection coils of the yoke collapses and the resultant energy is stepped up by the flyback transformer. On the secondary side of the flyback transformer are separate windings which feed diode rectifiers and associated voltage divider circuits. Anode operating potential, focus (G4), G1 and G2 voltages are all derived from these rectifier and voltage divider circuits.

The vertical sync (VSYNC) input is applied to the vertical sync and deflection circuitry. Vertical processing is performed wholly by a vertical processor device which develops the final vertical sawtooth waveform that drives the vertical deflection coils of the yoke. Vertical hold, vertical size and vertical linearity adjustments are all inputs to the vertical sync and deflection device.

2.2 KEYBOARD

This section provides an overview of Keyboard operations as well as a functional block diagram level of theory discussion.

2.2.1 KEYBOARD OVERVIEW

The detached Keyboard contains a dedicated 8031 microprocessor that accepts commands from the Z-80 in the Electronics Base while sending both Keyboard status data and keystroke data back to the Z-80. This communication occurs between the serial I/O port of the 8031 in the Keyboard and another 8031 located in the Electronics Base. The Keyboard communicates in a full-duplex mode.

Pressing a key causes the Keyboard to send a 7-bit keystroke code to the Z-80 in the Electronics Base. Every key has its own unique keystroke code, which is arbitrary and bears no relationship to any of the various character codes. In addition to the keystroke codes produced when they are pressed, the left and right SHIFT keys also generate different codes, called release codes, when they are released.

The release code for any key is identical to its keystroke code, but with high-order bit 7 set (i.e., keystroke code plus '80'). Special Keyboard commands establish release codes for up to five other designated keys or, alternately, for all of the keys on the Keyboard.

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

The LOCK and SHIFT keys have transmittable codes that allow maximum flexibilty at the host system. The LOCK key has an LED (bit 0) for a visual indication that the key is engaged. The host system decodes the LOCK key transmittal code and returns a code back to the Keyboard through the 8031 to light the LOCK LED.

The left and right SHIFT keys have make and break codes in the Keyboard default scheme. When either SHIFT key is depressed, it will transmit its own X/Y code (make code). When the SHIFT key is released, a break code will be transmitted. When a shift condition is sensed, the host system will append an '80' bit to all keys until it sees the break code for the shift key.

Any key on the Keyboard is a potential repeat key. If the Keyboard is programmed to generate a release code for a particular key, the Z-80 in the Electronics Base can assume that the key remains down (or pressed) between the time it receives the keystroke code and the time it receives the corresponding release code. Therefore, when a program that is monitoring the Keyboard recognizes a pressed key in this way, it can decide whether the key will repeat, and at what rate.

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

Figure 2-2 shows keystroke code assignments for the standard Keyboard. There are some possible keystroke codes and their corresponding release codes that are not produced by any key.

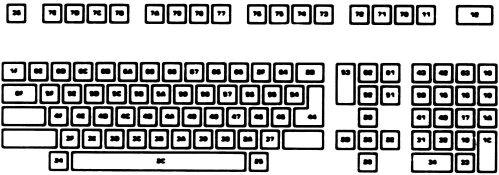

Figure 2-2. Keycode Assignments

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD OVERVIEW (Continued)

One of these, code '01', is used as a query response byte, which is always followed by one or more status bytes. When the Z-80 makes an inquiry by sending one of the query control byte sequences, it continues accepting Keyboard input until it receives the '01' query response byte and then accepts the appropriate number of status bytes before resuming normal Keyboard input.

A 4-conductor cable fitted with a 4-pin DIN connector carries power and interface signals between the Keyboard interface and the detached Keyboard. The Keyboard connector and 4-pin DIN connector signals are shown below.

CONNECTOR PIN NO.	DIN PLUG PIN NO.	SIGNAL
1	N/C	Negative lead to speaker
2		Positive lead to speaker
3	1	Ground
4	2	Data output to Keyboard
5	4	5 Vdc power
6	3	Data input from Keyboard

LED control commands are used to turn on individual LEDs as well as turn on and turn off all LEDs. The Keyboard LEDs are used to indicate diagnostic errors. The LED status command allows the host system to read the LED status at any time. The Keyboard is initialized with all LEDs off.

2.2.1 KEYBOARD OVERVIEW (Continued)

N-key rollover exists between all encoded keys on the Keyboard. Therefore, when a key is depressed while other keys are held down, the Keyboard will be able to output the latest keycode. Two 8-bit switchbanks on the Keyboard identify the particular Keyboard configuration.

The Keyboard interface in the Electronics Base is designed around an 8031 microprocessor with a full duplex serial port UART operating at 62.5k baud. On power-up or system reset, hardware initializes the 8031 to transmit and receive serial protocol that consists of one start bit (cleared to zero), an 8-bit data word (least significant bit first), and two stop bits (set to one), without parity.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION

Refer to Figure 2-3 for the following discussion.

Figure 2-3. Low-Profile Serial Keyboard Block Diagram

2.2 KEYBOARD (Continued)

2.2.1 KEYBOARD THEORY OF OPERATION (Continued)

The 8031 device is a single-component 8-bit microprocessor that contains 128 x 8-bit internal RAM memory, an internal oscillator and timing circuit for data synchronization, and a full duplex serial port (UART). The 8031 device requires one supply voltage (+5 volts) for operation. Keyboard data is either sent or received across the full-duplex Keyboard interface.

A 4 MHz crystal-generated clock is used for the synchronization of the 8031 to the various other components located on the board. This clock is necessary since only power and data are transmitted from the Electronics Base.

The 8031 uses its port zero lines as both the data and the address bus in a multiplexed bus scheme. Lines D0 - D7 identify the shared bus. Signal ALE (address latch enable) enables the address latch when the bus is in the address mode, thus storing an address in the latch. The address latch addresses the EPROM while signal PSEN (program store enable) enables the EPROM to read the instruction at that address onto the bus, which is now in the data mode. The EPROM stores the operational routines for the 8031.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

At power-up, the reset circuit sets the 8031 program counter to zero and the 8031 starts executing its initialization code from the EPROM. The initialization routine performs the following tasks:

1. Configure internal UART to 62.5k baud
2. Configure line protocol (1 start bit, 8 data bits, 2 stop bits)
3. Load zeros to sound generator
4. Clear LEDs
5. Set up two internal timers

After initialization, the 8031 starts its X axis scan routine, continuously polling port 1 for an input from the X/Y matrix. The Keyboard keys are laid out in a 16 x 8 X/Y matrix for a total of 128 possible configurations. Not all possible configurations are used. The 8031 supplies three scan lines (A8, A9, A10) to the two 3-to-8 decoders. The three scan lines count in binary from zero to 7 for each of the two decoders, thus causing a strobe to occur sequentially from X_0 to X_{15}.

The Y lines in the matrix are the return lines to the 908 device. When a key is pressed, the capacitive reactance is sensed by the 908 device and the device translates the sense to a TTL level for the 8031. Upon receipt of the input from the 908, the 8031 reads the 908 input again to confirm the original read.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

The 8031 now looks in an internal table for the keycode that matches the Y location from the 908 device and the X location from the 3-to-8 decoders.

The keycode is then sent to the 8031's internal UART where it is serialized. A start bit and two stop bits are added and the serial stream is transmitted to the Electronics Base. After transmission of the last bit in the stream, the 8031 UART generates an internal interrupt which causes the 8031 to resume its X axis scanning routine.

The X portion of the X/Y matrix also serves to read the settings of the two on-board switchbanks. One side of each switch is connected to one of the X lines. Each X line is normally pulled up to 5V. The other side of each switch is connected to one common transistor. When an X line is strobed (brought low) and its switch is closed, the strobe is coupled through the switch to the transistor and the transistor changes state.

This pulse is applied to the 8031 as an interrupt at P3.2, and the 8031 registers the switch closure in an internal register dedicated to holding the switch settings. When an X line is strobed (brought low) and its switch is open, the transistor is unaffected and no interrupt occurs.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

The switch setting scan routine occurs after each X/Y matrix read routine. The switch settings can be read from the 8031's internal register anytime the Z-80 in the Elec- tronics Base issues a query command.

Communication from the Z-80 in the Electronics Base to the 8031 in the Keyboard occurs as follows. The command to the Keyboard is received by the 8031's internal UART, the start and stop bits are stripped and the command is looked up in a table in the 8031. The starting address of the routine associated with that command is put on the address bus, and the 8031 executes code from the EPROM to satisfy the particular routine.

The six LEDs located on the Keyboard PCB are under the control of the Z-80 CPU in the Electronics Base. The Z-80 CPU sends LED data serially to the 8031 in the Keyboard. The 8031 strips the start and stop bits and converts the serial data to parallel data. The LED data is then placed on port zero lines P0.0 - P0.7 and latched in the tri-state LED latch. The 8031 enables the LED latch, thus driving the LEDs with the data from the Z 80 in the Electronics Base. Any low output from the LED latch will illuminate the associated LED.

A programmable sound generator device provides the Keyboard with its beep and click sounds.

2.2 KEYBOARD (Continued)

2.2.2 KEYBOARD THEORY OF OPERATION (Continued)

Upon receipt of a beep or click command from the Z-80 in the Electronics Base, the associated routine is called from the EPROM.

The 8031 receives the appropriate data for the sound generator from the EPROM. This includes the data required to load the sound generator's attenuation and frequency registers to produce the desired sound. The data is latched from the data bus and then applied to the sound generator. A common operational amplifier is used to drive the speaker.

2.3 4230/4205 ELECTRONICS BASE

The standard 4230/4205 Electronics Base with no options houses one PCA which carries out all logic functions of the workstation. This PCA is referred to as the 4230 Workstation Electronics PCA, part number 210-8287, or the 4205 Workstation Electronics PCA, part number 210-8287-1. These PCAs are referred to in this section simply as the 8287 PCA. The information contained in this section is applicable to both the 4230 and the 4205 workstation Electronics PCA except where specifically noted.

Figure 2-4 is a functional representation of the single PCA workstation.

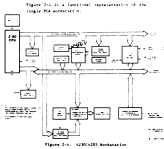

Figure 2-4. 4230/4205 Workstation Functional Block Diagram

2.3 4230/4205 ELECTRONICS BASE (Continued)

2.3.1 210-8287 CPU PCA

The 8287 CPU PCA contains three LSI (large scale integration) devices and their support logic, thus providing all logic required for workstation operation on a single board. The LSI devices are a Z-80 CPU, an 8031 microprocessor for the serial keyboard interface and a WL-2001 device which provides all the functions of a standard Wang 928 data link in a single LSI device.

Support logic for these main LSI devices includes 64k bytes of main memory with parity, a 4k PROM containing the Built-In Test (BIT) power-up diagnostic, and CRT RAM including 4k of character RAM, 4k of attribute RAM and 8k of font RAM. (The 4205 has only 4K of font RAM.) Another 4k PROM stores the operating program for the 8031 microprocessor.

The connector header mounted on the rear of the PCA contains the DATA LINK BNC/TNC connectors for cable connection to the host CPU as well as the connectors for the Monitor and Keyboard.

2.3.1.1 Z-80 Central Processor Unit (CPU)

Bus operations are controlled by the Z-80A CPU. The CPU receives sequential instructions from main memory over the data bus. It assigns device access and tasks based on these instructions and communicates with workstation logic through the data, address, and control buses.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.1 Z-80 Central Processor Unit (CPU) (Continued)

CPU signals are sequenced according to both its internal instruction set and instructions received from main memory over the data bus. The CPU requires a single, +5 Vdc supply and employs a 4 MHz clock as its time base.

Bidirectional data flow is accomplished by an 8-bit, tri-state data bus. The CPU transmits address information over a 16-bit, tri-state address bus. A reset line initializes the CPU and the six control-output lines. The six control-output lines are:

M1, CPU Fetch Cycle: This line is active during the first cycle (fetch cycle) of each instruction-request cycle, and during the special interrupt cycles.

MREQ, Memory Request: Active when the address bus holds a valid address for a memory read or write operation.

IORQ, Input/Output Request: Active when the lower half of the address bus holds a valid I/O address for an I/O read or write operation. Also becomes active for the interrupt acknowledge cycle.

RD, Read: When active, indicates that the CPU will input data while performing a memory-access or I/O instruction.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.1 Z-80 Central Processor Unit (CPU) (Continued)

WR, Write: When active, indicates that the CPU will output data while performing a memory-access or I/O instruction.

RFSH, Refresh: During an M1 (memory period 1) cycle, the CPU outputs an address for memory refresh. RFSH confirms the active presence of that address.

In addition to the control-output lines, there are three CPU input control lines. These lines are:

BUSRQ, Bus Request: An outside device can request bus access by asserting this signal. BUSRQ input causes the CPU to switch its address, data, and status lines into a high-impedance state to accommodate the outside device.

BUSAK, Bus Acknowledge: Becomes active to indicate that the CPU has complied with a BUSRQ.

WAIT: An outside device can request the CPU to extend the current memory access or I/O cycle by asserting this signal. The CPU waits as long as the signal remains asserted.

2.3.1.2 CPU Interrupts

The workstation employs Z-80 interrupt mode 0. In this mode, the CPU receives its next instruction from the interrupting device.

2.3.1.2 CPU Interrupts (Continued)

The workstation employs Z-80 interrupt mode 0. In this mode, the CPU receives its next instruction from the interrupting device. In the 4230/4205 Workstation, interrupts are received from the 8031 processor used for the Keyboard interface. The interrupt notifies the CPU that a keystroke has been received and is ready for processing.

Two interrupt inputs to the CPU are provided, maskable (INT) and nonmaskable (NMI). Keystroke interrupts are of the maskable type, while a non-maskable interrupt (unconditional entrance to the program) occurs only for a detected memory parity error.

2.3.1.3 Main Memory

Main memory consists of 64k bytes of dynamic RAM with one bit of parity for each byte of memory. Physically, memory is implemented with nine 64k x 1-bit devices. Main RAM can be accessed by both the CPU and the data link. (The data link is a DMA path.) The DRAM controller is responsible for generating row address strobe (RAS) and column address strobe (CAS) logic to address main memory. RAS and CAS lines enable 16-bit addresses to be processed in 8-bit, half-address form, permitting 16-bit main memory addresses to dynamic RAM devices with only eight address input pins.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.3 Main Memory (Continued)

RAS/CAS logic transfers high and low-order address bits through the same device pins at different times.

RAS/CAS cycles are required any time main memory is addressed. Main memory is addressed during these operations: CPU instruction fetch/refresh cycle, CPU data read, CPU data write and DMA transfer

2.3.1.4 Main Memory Parity Checking

Memory parity logic is one of two parity generation/detection circuits. The other circuit is part of the Data Link. Memory parity logic generates and then tests for even parity on all data transfers leaving or entering the CPU through the data bus. During a CPU write, each parity bit is calculated and stored in main memory.

The parity line is checked on each CPU read. If a memory parity error is detected, the diagnostic PROM is enabled and the CPU receives a non-maskable interrupt which causes it to jump to location '0066'. At that location in PROM is the main memory parity error routine which causes the contents of the CRT screen to be underlined, thus informing the operator of the error.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.4 Main Memory Parity Checking (Continued)

The underlining condition can be cleared only through a Z-80 RESET. In the 4230/4205, a RESET can be accomplished by cycling ac power to the workstation or, in some cases, by the host CPU.

Following workstation reset (restart), the diagnostic built-in test (BIT) runs and the usual power-up checks ensue. If the memory parity error was a soft error, the workstation will pass the BIT and be ready for operation again. During diagnostics, the parity detection circuitry itself is tested by forcing bad parity to be written and then reading back the same data location.

2.3.1.5 Address Assignments and Page Select Logic

The Z-80 CPU, with its 16 address lines, is capable of addressing up to 65,536 (64k) different memory locations. Many of the programs available on a host VS/OIS CPU require the full 64k of main memory within the 4230 workstation in order to run. Nevertheless, character, attribute and font memories comprise another large segment of memory that must be addressed as directed by CRT controlling routines within the workstation.
To overcome the limit placed upon the number of available addresses by the 16-bit address bus, a method of memory address assignments called page selection is used in the 4230/4205 Workstation.

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select Logic (Continued)

Page selection allows the same addresses to be assigned to more than one physical memory device. Thus, while both the main and CRT memories see the address lines from the CPU, only the memory that is enabled at the time responds to the current address on the bus.

Figure 2-5 is a simplified representation of the hardware used to implement the page select scheme. The central element in the page select hardware is the block memory decode PAL (programmable array of logic). The PAL is programmed to output the appropriate memory enables for the combination of inputs it receives. In the 4205, this PAL is programmed to inhibit main RAM addresses above 32k.

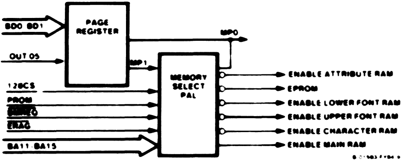

Figure 2-5. 4230/4205 Workstation Memory Page Select Logic

2.3.1 210-8287 CPU PCA (Continued)

2.3.1.5 Address Assignments and Page Select Logic (Continued)

The available addresses are assigned differently for each of three pages available to the CPU for selection. The three pages and their address assignments are shown in Figure 2-6.

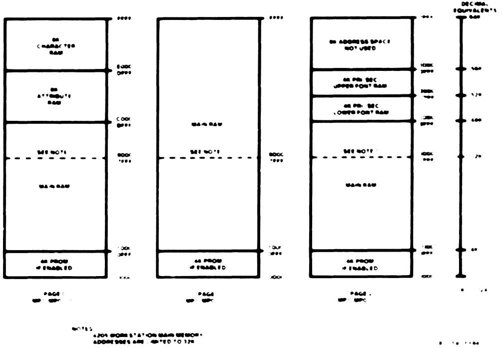

Figure 2-6. 4230/4205 Workstation Memory Addressing Assignments