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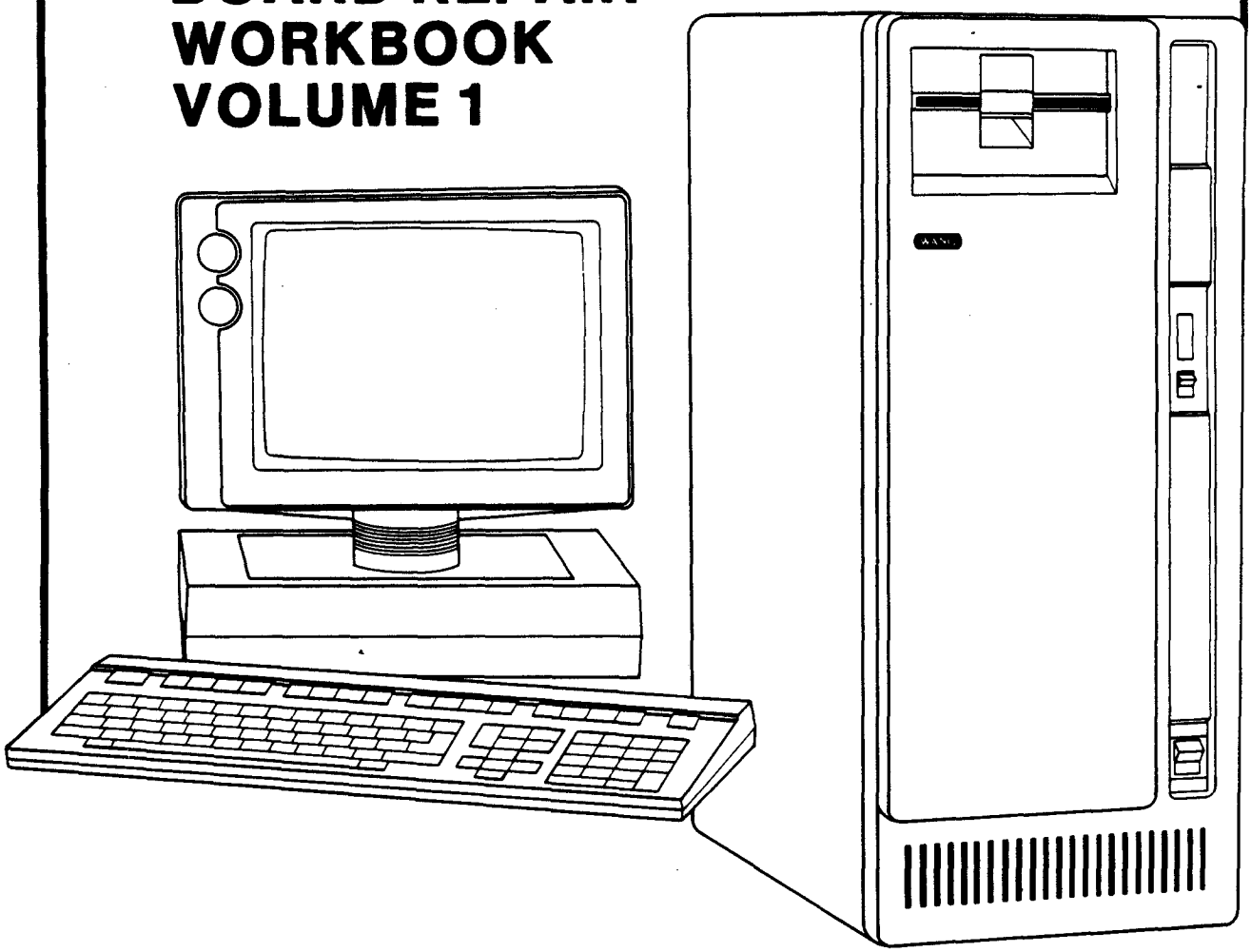
OIS 40/50/60

BOARD REPAIR WORKBOOK VOLUME 1



CUSTOMER ENGINEERING
TRAINING AND DOCUMENTATION

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WANG

CUSTOMER ENGINEERING TRAINING CENTER

OIS 40/50/60
BOARD REPAIR WORKBOOK VOLUME 1

PREFACE

This document is intended to be used for TRAINING PURPOSES only. The material contained in this document, while accurate during the developement of this workbook, may not reflect the latest developments or changes to the OIS 40/50/60 system.

TECHNICAL SUPPORT DOCUMENTS

OIS 50 INTERNAL PRINTER CONTROLLER HARDWARE SPECIFICATIONS HM-60
OIS 40/50 RESOURCE MANAGEMENT UNIT THEORY OF OPERATION 751-0902
OIS 40/50 RESOURCE CONTROL UNIT THEORY OF OPERATION 751-0911
OIS 40/50 IWS FULL MATRIX CONTROLLER SPECIFICATION HM-67
WL-2630 OIS/VS COLLECTIVE GATE ARRAY SPECIFICATION HM-37
OIS-50 INTERNAL WISE SPECIFICATION REVISION 3 HM-85
OFFICE INFORMATION SYSTEMS OIS 40/50/60 741-1267
OIS SYSTEM ADMINISTRATION GUIDE 700-5562E

First Edition - December, 1985

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SECTION I
INTRODUCTION

SECTION 1

OIS 40/50/60 WORKBOOK INTRODUCTION

This board repair workbook is comprized of two volumes. In the first volume the overall system will be covered in general. Then the reader will be presented with theory of operation for the three main circuit boards within the system, the Resource Management Unit (RMU), the Resource Control Unit (RCU), and the Internal Workstation Controller (IWS). Each of these sections will include a detailed description of the circuit board with limited bit chasing. The reader will be referred to Figures and Tables, along with references to the schematics to help him or her understand the operation of the unit. At the end of each section there is a quiz covering the information that was presented. After answering the questions in the quiz the reader can check his or her answers by referring to the answers in Appendix G.

In the second volume the reader will be presented with a detailed description of the theory of operation for the Internal Printer Controller (IPC), and the Internal WISE Controller (IWISE) circuit boards. The organization of the second volume is similar to that of the first as far as type of content and objectives.

Both volumes contain Appendices that provide relitive infromation about the circuit boards within that volume. Also located in the rear of the each volume is a master index that covers both volumes, this should provide the reader with a quick reference to just about any circuit operation.

If after you read this book you have any further questions or are interrested in learning more about the operation of the system, a list of reference books is provided in Appendix A of volume 1.

If while you are reading this workbook you come accross any errors that you feel need correcting, fill out the form provided at the back of the book and subbmit it to you supervisior. This feed back will help us improve the quality of the books that we produce and improve the quality of training that you receive.

1.1 OIS 40/50/60 SYSTEM INTRODUCTION

The OIS 40/50/60 system is a smaller version of the OIS 140 system that is contained in one package. The OIS 50 is capable of supporting up to four non-intelligent workstations and one or two non-intelligent printers. The logic providing the intelligence of these workstations and printers resides within the OIS 50 Master Processor. In addition the system will support up to four OIS 928 type serial devices, including intelligent workstations, image printers, phototypesetters, and telecommunication devices. The OIS 50 may be connected in a network configuration to more powerful Office Information Systems through the use of a Wang Inter-System Exchange Unit (WISE).

The OSI 40 is essentially a subset of the more versitile OIS 50. It was designed to be used as a stand alone system, capable of supporting one non-intelligent workstation along with one non-intelligent printer. As an option the OIS 40 may be configured to support one 928 type serial intelligent workstation or device. Like the OIS 50, it may be connected in an office system network via WISE, and has optional telecommunications capability.

The OIS 60 system represents the latest design in the OIS family of WANG Office Information Systems. In addition to the features of the OIS 40/50 configurations the OIS 60 provides four additional standard 928-type serial data link ports enabling the system to support a total of 12 peripheral devices, eight of these could be workstations. To support the additional ports the Resource Management Unit (RMU) and the Resource Control Unit (RCU) PCA's have been modified. The applicable theory and maintenance information (differences) for each will be covered as the RMU and RCU boards are discussed.

All three system contain an onboard 5 1/4 inch floppy archive drive, and either a 10 Meg or 30 Meg Winchester disk drive. The OIS 40 and 50 contain 10 Meg Winchester drives while the OIS 60 has a 30 Meg Winchester drive. In addition the OIS 60 has a hinged rear panel for easier access to the internal cabling for troubleshooting purposes.

The front panel of each of the units contains a rocker switch used for selecting which drive the unit will IPL from, (i.e. the Winchester or the Floppy). Directly above the IPL switch is located a LED status display. When the system is first powered on the unit will run an onboard BIT diagnostic. If an error is detected during the BIT test the status display will reflect the type of problem found. Refer to Appendix zzz for a complete list of error codes and their meaning.

1.2 SYSTEM OPERATION

In the OIS 40/50/60 system there are six printed circuit board that reside in the Master Processor, they are:

BOARD #	DESCRIPTION	SYSTEM
210-8266-A	Resource Management Unit (RMU)	((OIS 40/50))
210-8490-A	Resource Management Unit (RMU)	((OIS 60))
210-8267-A	Resource Control Unit (RCU)	((OIS 40/50))
210-8267-B	Resource Control Unit (RCU)	((OIS 60))
210-8274-A	Internal Workstation Controller (IWS)	((OIS 40/50/60))
210-8280-A	Internal Printer Controller (IPC)	((OIS 40/50/60))
210-8270-A	Internal WISE Controller (IWISE)	((OIS 40/50/60))
210-8269	OIS 50 Motherboard	((OIS 40/50/60))

The OIS motherboard is designed to hold a total of seven printed circuits boards, two of these boards must be the RMU and RCU boards. These two board contain all the Central Processing Logic for the Master unit. The five remaining slots accommodate the different peripheral controller boards in various combinations. Four of these slot may contain Internal Workstation Controllers (IWS), while the last slot may contain either an Internal WISE Controller (IWISE) or Internal Printer Controller (IPC). Depending on the system configuration, an additional IPC board may be substituted for one of the IWS controllers. FIGURE 1-1 shows a simplified block diagram of the OIS 40/50/60 system depicting the RMU, RCU, IWS,IPC and IWISE controllers, floppy and Winchester storage, and various peripheral devices. The flow of information between the various devices and PC boards occurs on the 50BUS. This bus is comprised of 40 signals representing address, data, select, and control information.

All of the Central Processing Logic for the OIS 40/50/60 is contained on the Resource Management Unit (RMU) and the Resource Control Unit (RCU) circuits boards. The Resource Management Unit (RMU) as its name implies, is responsible for the overall management of system operations. It runs the Operating System code and contains the system's main memory. The Resource Control Unit (RCU) shares the processing burden by controlling some of the more cumbersome tasks. In this way the RCU relieves the RMU of certain time-consuming operations, thus freeing the RMU to concentrate on overall system management. The net result is a system that runs faster and more efficiently than single-processor systems.

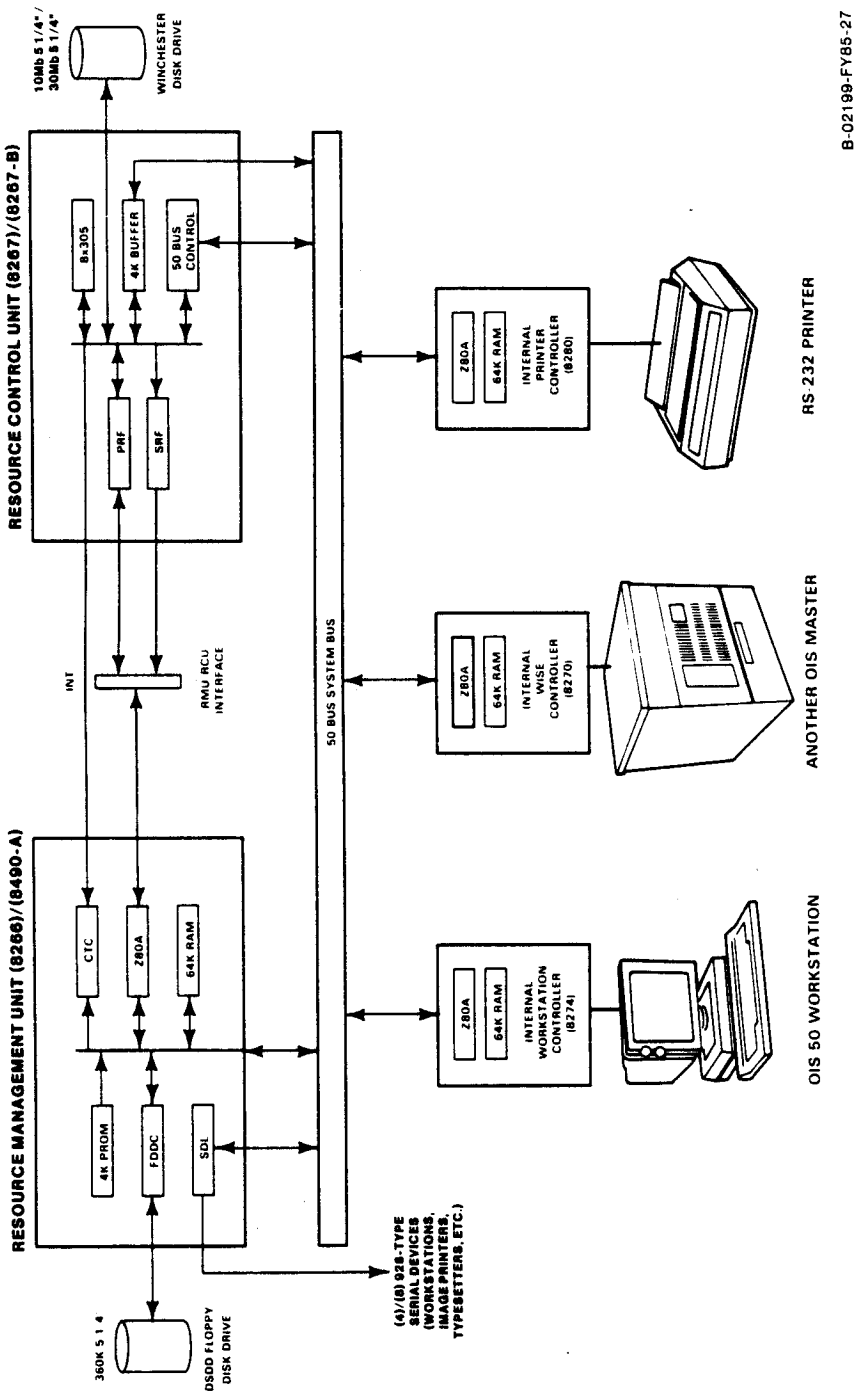


FIGURE 1-1
OIS 40/50/60 Simplified Block Diagram

1.2.1 Resource Management Unit (RMU)

The RMU contains a Z80 microprocessor that executes the system operating code, also on the RMU is located 64K of RAM overlayed by 4K of PROM memory. The RAM functions as main memory for the system, while the PROM contains the BIT power-up diagnostics and bootstrap loader code. The upper 256 bytes of memory is reserved Memory Mapped I/O. A Z80 Counter/Timer Chip (CTC) handles the various interrupts that the Z80 must respond to. The RMU is also responsible for controlling all operation involving the system's mini-floppy disk drive. An LSI Floppy Disk Controller chip (FDDC) resides on the RMU for this purpose. Finally, the RMU also contains all transmit and receive logic for all the external Serial Data Link (SDL) ports that connect the OIS 40/50/60 to 928-type serial peripherals. Although this SDL logic resides on the RMU board the RCU is actually responsible for its control.

1.2.2 Resource Control Unit (RCU)

The RCU board is designed around a Signetics 8X305 Microcontroller chip. It relieves the RMU's Z80 of a good deal of overhead by assuming the processing duties in four main areas:

1. Control and execution of all operations involving the 5 1/4" Winchester Disk Drive.

2. Execution of all block data transfers.

3. Control and arbitration of the 50BUS System Bus.

4. Control and execution of the Serial Data Link (SDL).

The 8X305 Microcontroller is the heart of the RCU board, and operates from instructions stored in firmware. A 4K Data Buffer is located on the RCU, and is involved in any operation that requires the transfer of block data. Logic on the RCU board generates commands and control signals that governs the operation of the 50BUS. Finally, all Serial Data Link (SDL) operations are under direct control of the 8X305 Microcontroller and additional support logic, even though the actual SDL transmit and receive circuitry is on the RMU.

In a multi-processor system such as this, communication between the two microprocessors is an important aspect of the system design. The RMU's Z80A and the RCU's 8X305 Microcontroller communicate with one another through the use of shared memory and interrupt signals. Two special memory areas are present on the RCU board. Both the Z80A and the 8X305 Microcontroller can access these locations. One area is called the Parameter Register File (PRF) while the other is labeled the Status Register File (SRF). When the Z80A of the RMU encounters and instruction that is the responsibility of the RCU, it will instruct the RCU to perform the task. To do this the RMU will write commands and parameter information into the Parameter Register File. The RCU then reads the (PRF) and interprets and executes the commands. When the RCU completes the task it writes status information into the Status Register File. The RMU reads the status information from the (SRF) to determine the outcome of the operation. For lengthy RCU operations such as block transfers the RMU will attend to other management duties while the RCU carries out the operation. When the RCU completes the task it will generate an interrupt to the Z80A indicating that the operation is complete.

As mentioned earlier, the 50BUS is the system's internal bus network comprised of 40 signals representing address, data, select, and control information. All information exchanged between the OIS 40/50/60 Central Processing Logic (RMU, RCU) and the various peripheral controllers (IWS, IPC, IWIS) travel on the 50BUS. The RCU initiates and governs all 50BUS transactions. Via the 50BUS the RCU is able to exchange information with a total of eight logical devices, called 50BUS Devices. Three of these logical devices reside on the RMU board:

1. Main Memory
2. The Floppy disk drive controller
3. The Serial Data Link transmit and receive logic

The remaining five logical devices correspond to the five Motherboard slots which house the various peripheral controller boards (IWS, IPC, IWISE).

A typical 50BUS transaction between the RCU and a 50BUS Device usually involves the transfer of block data. Consider the following example: While running the operating system, the RMU determine that it needs to read a portion of the workstations memory. Since the operation involves use of the 50BUS, and the RCU is responsible for operation of the 50BUS then the RMU instruct the RCU to perform the task and supplies the RCU with the particulars (which IWS, what portion of memory to read from, etc.) by writing to the (PRF). The RMU then goes about doing other housekeeping duties while the RCU performs the task. Using the 50BUS, the RCU selects the desired slave and places the slaves Z80A into a Bus-Request state so a DMA operation can take place. Then the RCU reads the desired slaves memory and transfers it byte for byte into the 4K Data Buffer on the RCU board via the 50BUS. When the operation is complete the RCU notifies the RMU by an interrupt. The RMU will then read the (SRF) to determine the results of the operation.

Three type of peripheral controller boards may be included in an OIS 40/50/60 system. They are; the Internal Workstation Controller (IWS), Internal Printer Controller (IPC), and the Internal WISE Controller (IWISE). Each of these controller boards contain a Z80A microprocessor along with 64K bytes of RAM used as slave memory. The following paragraphs contain a brief description of each board's responsibilities.

1.2.3 The Internal Workstation Controller (IWS)

The OIS 40/50/60 Master is capable of supporting up to four OIS 40/50/60 non-intelligent display terminals. The workstation is termed non-intelligent because the hardware and software that control the logical functions reside within the OIS 40/50/60 Master, on an (IWS) Controller board. The IWS Controller is responsible for providing:

1. The interface signals to the monitor electronics.
2. The interface logic to the serial keyboard.
3. The CRT, font, and main memory storage.
4. Interface logic required to communicate with the 50BUS.

1.2.4 The Internal Printer Controller (IPC)

The Internal Printer Controller (IPC) is designed to control a single RS-232C printer. The IPC receives commands and data from the RCU board via the 50BUS and communicates with the printer through an RS-232C serial interface. It is designed around a Z80A microprocessor running at 4 Mhz, and contains:

1. 50BUS interface logic.
2. RS-232C interface logic.
3. Printer control interface logic.
4. 64K of Dynamic RAM

1.2.5 The Internal WISE Controller (IWISE)

The internal WISE board provides a high speed communication path between the OIS 40/50/60 and any other WANG system that employs the standard 928-type Serial Data Link. The IWISE enables the OIS 40/50/60 to be used as clustered system, providing a communication link to a higher level Master Processor, such as the OIS 145 shown in FIGURE 1-1. Like the other controller devices attached to the 50BUS, the IWISE board depends on a Z80A running at 4 Mhz, and also contains:

1. Serial Data Link protocol logic.
2. 50BUS protocol logic.
3. 64K of Dynamic RAM and memory access arbitration logic.
4. DMA logic.

A complete theory of operation, and detailed circuit description for each of the circuit boards in the OIS 40/50/60 system is discussed in the following sections. Appendix A gives a complete list of all related documents for the OIS 40/50/60 system.

SECTION 1 QUIZ

1) What are the major differences between an OIS 50 and an OIS 60?

2) Name the five PCA assemblies that can reside in the main unit of either of the systems?

3) What two controller circuits reside on the RMU but are primarily controlled by the RCU?

4) In what four main areas does the RCU assume processing duties for the RMU?

5) What two memory areas do the Z80A and the 8X305 use to communicate with each other?

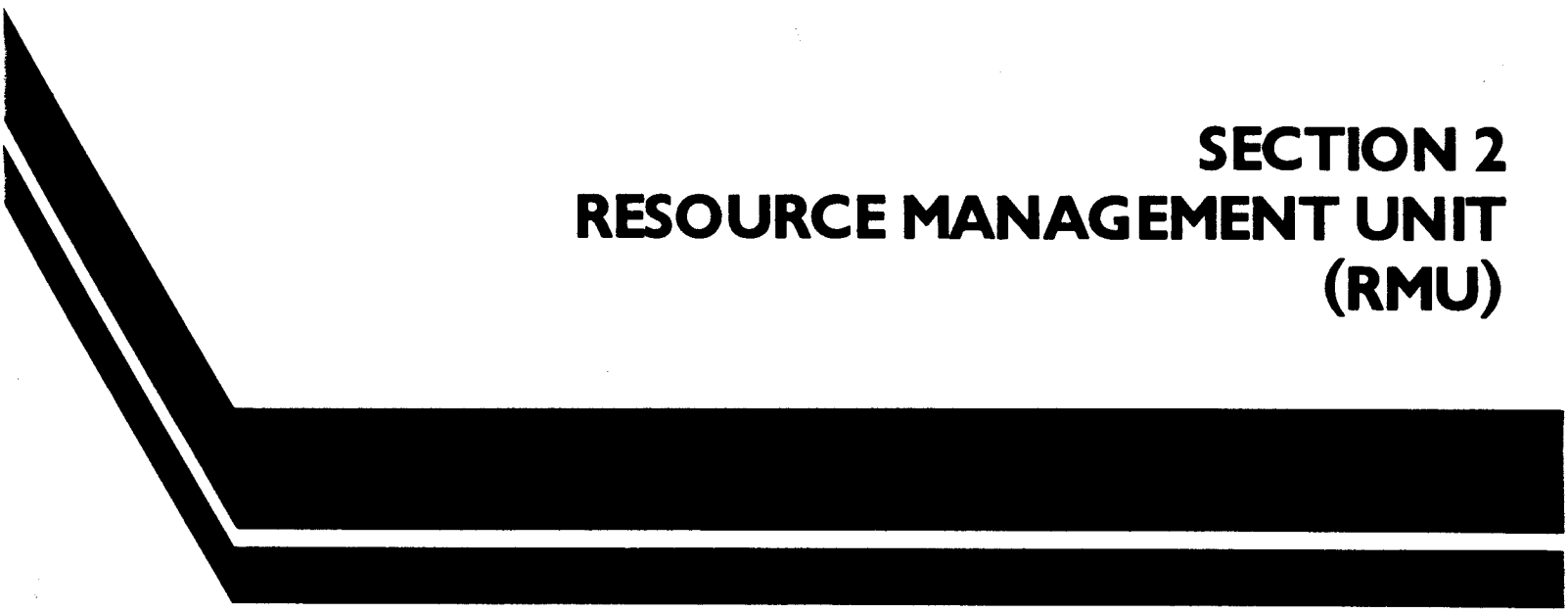
6) Who initiates and governs all 50BUS transactions?

7) What four items is the Internal Workstation Controller (IWS) responsible for?

8) How many printers can be connected to an Internal Printer Controller (IPC)?

9) What type of interface does the Internal WISE Controller (IWISE) require to communicate with other units?

10) Which Appendix contains a listing of reference materials that may be read to provide a better understanding of the OIS 40/50/60 system.



SECTION 2
RESOURCE MANAGEMENT UNIT (RMU)

SECTION 2

Resource Management Unit (RMU)

2.1 Resource Management Unit (RMU)

In this section we will discuss the theory of operation and circuit description for the Resource Management Unit (RMU). In lue of the fact that the RMU can not operate completely by itself, parts of the RCU circuits will also be discussed throughout this section.

While reading this section you should refer to the schematics in Appendix E so that you can follow along with the descriptions given. All circuit components will be referred to by their chip number and schematic location; Example L4 (1B2) indicates chip L4 located on sheet 1 row B column 2. If you are unfamiliar with a pectular type of chip that is being discussed you should refer to either the manufactures specification sheet or to the TTL Data Book by Texas Instruments. A quick reference of all the chips in the OIS 40/50/60 system is located in appendix C, each chip is listed by number and a brief description of its operation in the circuit is given. This Appendix is divided into parts representing each of the circuit boards located in the OIS 40/50/60. I recommend that you turn to Appendix C now and take a quick look at the listings.

Throughout the description of the circuits I will be using mnemonics to describe different signals that are generated. A complete listing of the meaning of these mnemonics are given in Appendix B. Any mnemonics that are active low and are indicated in the schematics by having a bar over the top will be prefixed in this document be an ampersand (&). Some signal have dual functions, such a R/W which when active low indicates a read operation and when active high indicates a write operation. To indicate which part of the mnemonic is active low I will place an additional ampersand next to the portion of the mnemonic that is active low, (i.e. &&R/W will represent the above description whereas R/W&& would indicate the reverse situation).

The 8266 Resource Management Unit used in the OIS 40/50/60 processor-based data processing system contains the 4-MHz Z80A Processor; the Counter Timer Chip, which generates interrupts and acts as a time-of-day clock; and the NEC765 Floppy Disk Controller (FDC), which manages operations involving the system's Floppy Disk Drive (FDD). (The 8X305 Microcontroller, the second processor of the OIS 50 multiprocessor system, is located on the 210-8267 Resource Control Unit board.) FIGURE 2.1-1 is a block diagram of the Resource Management Unit, and FIGURE 2.1-2 illustrates the Resource Management Unit's relation to the OIS 40/50/60 system.

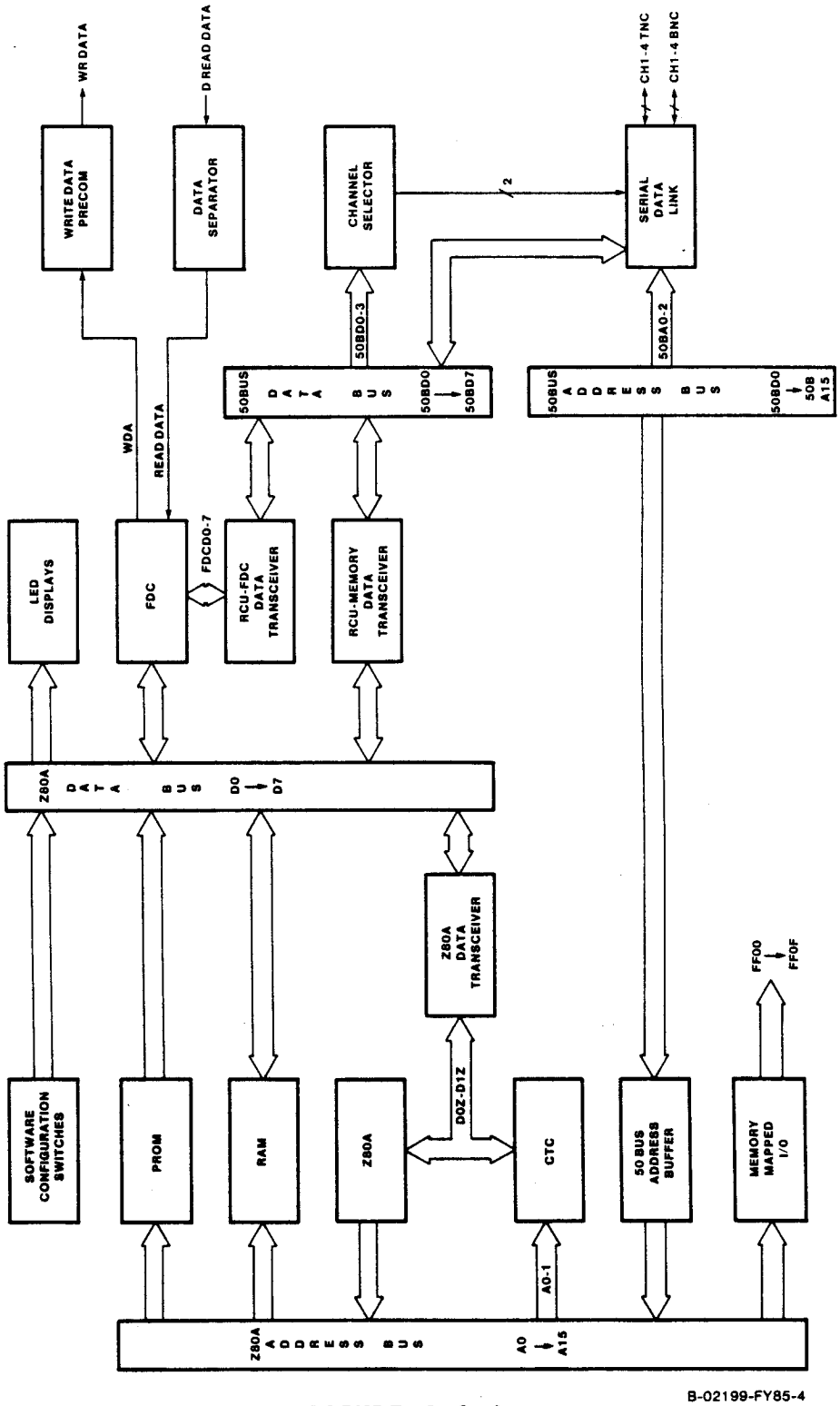


FIGURE 2.1-1
Block Diagram of the Resource Management Unit

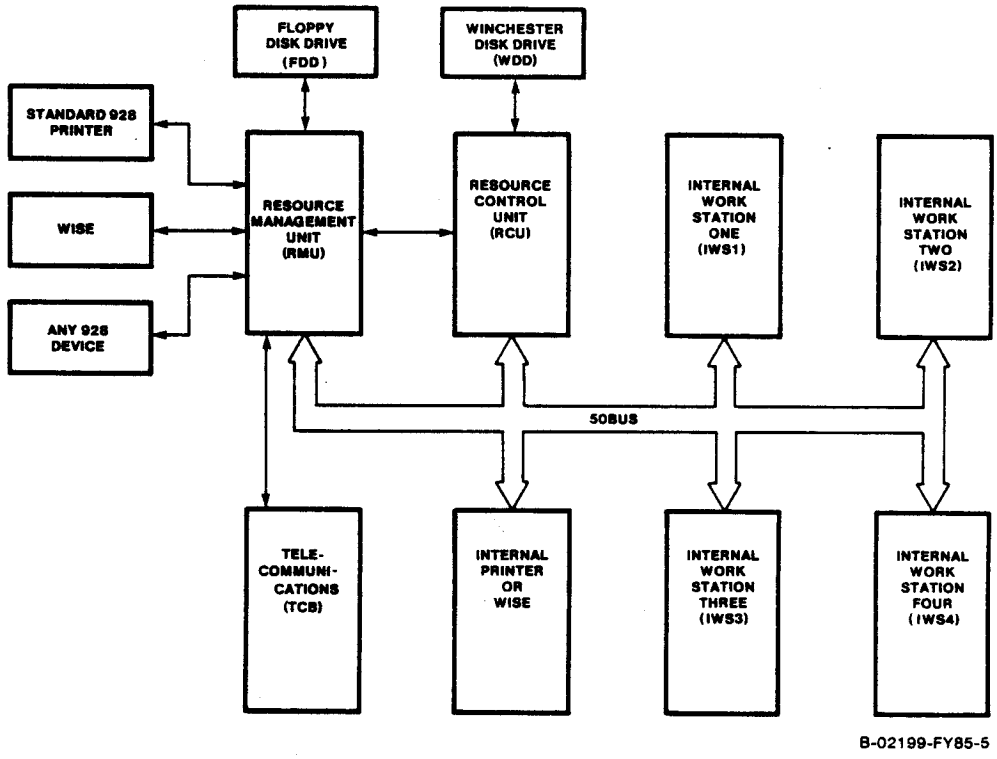


FIGURE 2.1-2
OIS 50 Block Diagram

Memory support for the OIS 40/50/60 is located on the Resource Management Unit (RMU) and is divided among RAM, PROM, and Memory Mapped Input/Output (MMI/O). Sixty-four kilobytes of RAM and 4k bytes of PROM are available for power-up diagnostics and Initial Program Load (IPL). Memory addresses from 1000-FF00 are used as random access memory, with the lower 4k bytes (0000-0FFF) overlayed by PROM. Memory addresses from FF00-FFFF are reserved for MMI/O.

The RMU board also contains serial transmit and receive logic for external Data Link ports 1-4. However, the 8X305 Microcontroller on the Resource Control Unit (RCU) board maintains control of these ports.

RMU-RCU Interaction

RMU-RCU communication involves shared memory, a Command Notification Bit (CNB), and the 8X305 Microcontroller interrupts that assert the Z80A. Two memory areas on the RCU board are shared between the Z80A and the 8X305: the 16-byte Parameter Register File (PRF) and the 12-byte Status Register File (SRF). Both the Z80A and the 8X305 can read from or write to the PRF; they cannot, however, access the PRF simultaneously. Only the Z80A can read the SRF, and only the 8X305 can write to it.

The RCU decodes RMU requests via the Parameter Register File. The Z80A microprocessor in the RMU loads the PRF with the command codes and data that the RCU needs to perform a specific operation. When the Z80A sets the Command Notification Bit, the 8X305 operates on the PRF as needed to complete the command. (Generally, the 8X305 moves the PRF data to its scratchpad RAM and then releases the PRF.) The PRF must be released quickly because the Z80A is suspended (ie, held in a bus request state) while the 8X305 uses the PRF.

PRF byte assignments depend upon the function requested (see Appendix G). Typically, the Z80A issues the FF20 (Command Request) byte and the FF22 (Specify Command) byte to the PRF. The RCU reads the bytes and defines the remaining bytes according to specific command requirements and then returns the FF21 (Command Acknowledge) byte to the PRF for the Z80A to read. To avoid invalid parameter errors, unused or undefined bytes should always be cleared to zero.

To perform a function that involves the RCU, the Z80A loads the command code and necessary data into the PRF. The Z80A then writes to address FF30 to issue the Command Notification Bit that initiates the command. Normally, the 8X305 is polling, waiting for the Command Notification Bit to be set. When the RMU issues a command, the 8X305 can perform one of two routines. If the command is an immediate command, the Z80A is awaiting command completion and the RCU must, therefore, execute the command immediately. If, however, the command is a non-immediate command, the RCU defers the command until it has completed any immediate operation in progress.

Upon receiving an immediate command, the RCU validates the command code, copies the PRF to its scratchpad RAM, completes the requested operation, and releases the RMU. Upon receipt of a non-immediate command, the RCU validates the command code, copies the PRF to its scratch RAM, sets RCU Busy status in the SRF, releases the RMU, completes the requested operation, and issues either an interrupt request or a Control Unit Busy (CUBUSY) signal to the RMU when the operation has been completed.