USER'S GUIDE
DIGITAL-TO-ANALOG CONVERTER MODULE

for use with

Varian 620 or V73 Series Computers

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1. INTRODUCTION

1.1 GENERAL

The Digital-to-Analog Converter (DAC) Module is a hardware option that interfaces Varian 620 and V73 series computers with external devices which require analog voltage as their inputs. DAC models are available to provide 10-bit, 12-bit, or 14-bit digital-to-analog resolution. A DAC module includes three functional features:

- One or two Digital-to-Analog (D/A) Converters, which convert digital data from the computer into equivalent analog voltage output signals.
- External Control (EXC) Interface Logic, which allows a computer program to control external devices via logic-signal output lines.
- Sense (SEN) Interface Logic, which allows a computer program to test the status of external devices by sampling logic levels present on Sense input lines.

The DAC's output capability may be expanded through the addition of Digital-to-Analog Converter Expansion (DACE) modules. Each DACE module provides two digital-to-analog converters. Up to three DACEs can be attached to each DAC. As many as eight DACs with 24 DACE modules can be attached to a single computer to provide the following I/O capability:

64 Analog Outputs	Each module (DAC and DACE) contains two digital-to-analog converters.
64 External Control Outputs	Each DAC contains eight External Control output lines.
64 Sense Inputs	Each DAC contains eight Sense input lines.

Simple installation procedures allow the DAC to be installed either at the factory or on-site at the user's facility. A comprehensive software test package is provided with the DAC for post-installation checkout of its operational status. In addition, the module is fully supported by standard Varian software and input/output options.

1.2 FUNCTIONAL DESCRIPTION

All elements needed to perform the module's three basic functions are packaged on a single plug-in printed circuit board. Figure 1-1 illustrates the functional elements included in a DAC module. A DACE contains only those elements shown in the shaded portion of Figure 1-1. Although the figure shows a DAC module which includes two digital-to-analog converters, some models of the DAC contain only one converter.

Device Address

The computer program must select a DAC by its device address before the module can perform any operation. There are eight device addresses (50_8 to 57_8) reserved for use by DACs. One DAC and three DACEs can be located at a device address; the DAC serves as the master module and contains the device address decode logic for the DACEs, which function as slaves to the DAC but provide the same basic conversion capability.

DAC Select

An individual D/A converter is selected by the computer program, using an Extended EXC (EXC2) instruction. There are eight DAC select lines at each device address; each line is enabled by the corresponding EXC2 instruction.

The master DAC module contains the DAC select logic for DACEs located at that device address. Once selected, a DAC remains selected until a different DAC at the same address is selected, until SYSTEM CLEAR occurs, or until power is interrupted.

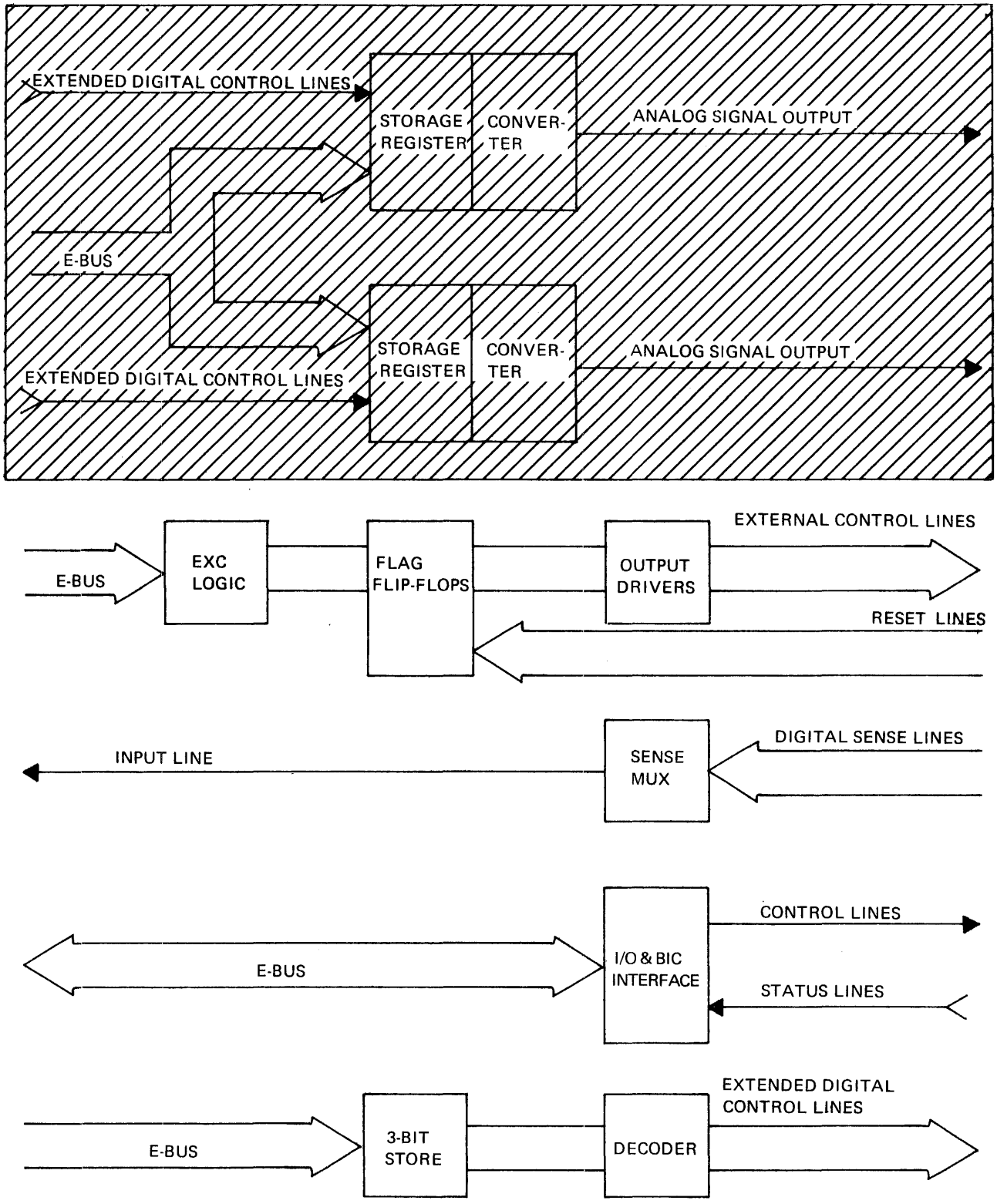


Figure 1-1. DAC Block Diagram

Buffer Enable Logic

The buffer enable logic is responsible for coordinating the transfer of data into the DAC buffer registers. If data transfer is under direct program control, the buffer enable logic exchanges data transfer control signals with the computer. When data transfer is under control of the Buffer Interlace Controller (BIC), special logic interfaces with the BIC.

Conversion

Digital data transmitted by the computer is gated into the addressed DAC's buffer register; the buffer data is immediately converted into a voltage signal by the D/A converter.

The converter output consists of a sequence of voltage levels which correspond to numbers transmitted by the computer. If the voltage changes are small enough, the converter output appears to the external device as an analog voltage curve rather than step value changes, as illustrated in Figure 1-2.

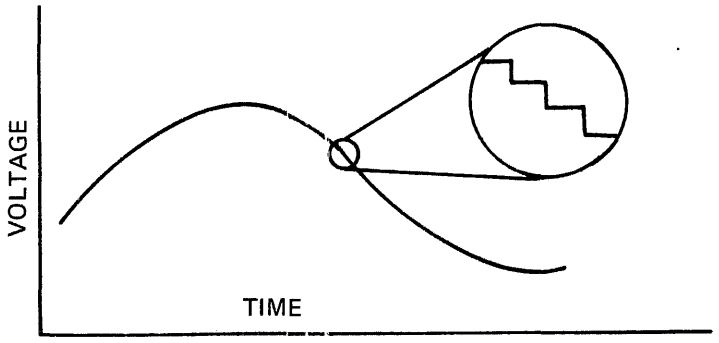


Figure 1-2. Analog Simulation by DAC Output

External Control (EXC) Interface

External Control Signals, which are generated by the computer to control operations in external devices, are distributed to the external devices via eight EXC output lines.

The DAC module's EXC interface logic selects one of the eight output lines according to the contents of the function code received from the computer. The master DAC contains all EXC interface logic for that device address.

Sense Interface

The DAC's Sense interface logic selects one of eight sense input lines according to the contents of the function code received from the computer. The logic level present on the selected line is gated to the computer. The master DAC contains all Sense interface logic for that device address.

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the DAC module and presents instructions for using the DAC software test package for module checkout. In addition, this section describes the usage of two special driver programs which are supplied with the DAC. More detailed programming information may be found in the 620 series or V73 system handbooks.

A program directs DAC operation in three ways:

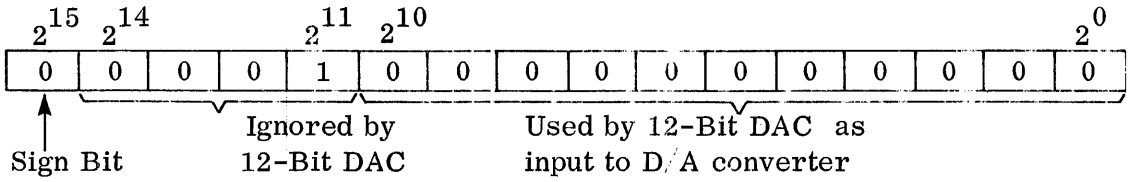
- Transfers data to the digital-to-analog converters.
- Distributes signals to External Control lines.
- Checks Sense input lines.

There are three basic factors to consider when writing a computer program to drive a DAC: data, timing, and hardware. Section 2.2 defines the restrictions placed on the numerical data which is generated by the computer program as input to the DAC. Section 2.3 discusses timing, which must be controlled by the program as it provides digital inputs for the DAC to generate real-time voltage output. Section 4 discusses the hardware capabilities of External Control and Sense lines, which should be evaluated by the programmer before setting up a permanent system.

2.2 INPUT DATA

The programmer may find it a useful precaution to check all DAC input data for numerical limits before it is transferred to the module. Table 2-1 provides the scale factor (F) which relates digital input (M) to the DAC with voltage output (V) from the DAC. M_+ to M_- are the maximum positive and negative numbers that will be converted properly.

If an attempt is made to convert numbers outside the range M_+ to M_- given in Table 2-1, the output voltage will be in error since the DAC assumes right-adjusted numbers with a high-order sign bit. For example, consider an attempt to convert +2048 to a voltage with a 12-bit DAC. In 2's complement binary +2048 is represented by:



Since a 12-bit DAC determines the output voltage magnitude from the 11 rightmost bits (2^0 to 2^{10}), 2048 would be read as 0.

Table 2-1. Numerical Properties of 10, 12, and 14 Bit DAC's

Number of DAC Bits	Scale Factor (F)	V_+ Volts	M_+ Decimal	M_+ Octal	V_- Volts	M_- Decimal	M_- Octal
10	1/512	9.980	511	777	-10.000	-512	177000
12	1/2048	9.995	2047	3777	-10.000	-2048	174000
14	1/8192	9.999	8191	17777	-10.000	-8192	160000

$V = FM$

Where
- V = Voltage Signal at DAC
- M = Digital Input to DAC
- F = Scale Factor
- V_+ = Maximum Positive Voltage
- V_- = Maximum Negative Voltage
- M_+ = Maximum Positive Digital Number
- M_- = Maximum Negative Digital Number

2.3 DATA TRANSFER UNDER PROGRAM CONTROL

The essential programming instructions for transferring data to a DAC are shown in Table 2-2. The instructions are given in the form of a block of code from a typical program.

An individual D/A converter is selected for a data transfer operation by means of an EXC2 instruction. For example, an instruction with the format EXC2 XYY selects converter number X at device address YY. Table 2-3 shows the converter number assignments for a device address. After a converter is selected, data is transferred to it by means of an OAR, OBR, or OME instruction.

Table 2-2. Instructions To Output Data Under Program Control

Program Step	Function
ONE LDA J	Load value of variable J into the computer A register. (LDB may be used instead of LDA.)
TWO EXC2 XYY	Select converter number X (0 to 7) at device address YY (50 to 57).
THRE OAR 0YY	Output data from A register to module at address YY (50 to 57). (OBR would be used if LDB had been used. OME could also be used to output data.)
(Time Delay Code)	(Timing data transfer to the DAC must allow for DAC settling time as discussed in Section 2.3.)
(Code To Generate Next Output Number)	
JMP ONE	

Table 2-3. D/A Converter Number Assignments

Module	D/A Converter Number
DAC (master)	0, 1
DACE (first slave)	2, 3
DACE (second slave)	4, 5
DACE (third slave)	6, 7

When an individual converter is selected at a particular device address, it remains selected until another EXC2 instruction selects a different converter at the same device address. For example, assume the following sequence of coding:

EXC2	053	Select First Converter on First Module at Device Address 53.
•		
•		
•		
EXC2	253	Select First Converter on Second Module at Device Address 53. This changes the selection specified by the previous EXC2 since both DACs are located at the same device address.
•		
•		
•		
EXC2	252	Select First Converter on Second Module at Device Address 52. This has no effect on the previous EXC2 instructions since the DACs are located at different device addresses.

Thus it is possible to select one D/A converter at each device address. The following example illustrates the selection and usage of converters at three different device addresses:

EXC2	050	Select First Converter on First Module at Device Address 50.
EXC2	351	Select Second Converter on Second Module at Device Address 51.
EXC2	453	Select First Converter on Third Module at Device Address 53.
LDA	V1	Load Variable V1 into Computer Register A.
LDB	V2	Load Variable V2 into Computer Register B.
OAR	050	Output V1 to selected DAC at Device Address 50.
OBR	051	Output V2 to selected DAC at Device Address 51.

```
        LDA     V3              Load Variable V3 into Computer Register A.

        OAR     053             Output Variable V3 to Selected DAC at Device
                                Address 53.
```

Timing is an essential part of programming data transfers to a DAC. There are two types of timing to be considered:

1. Settling-time delay, which is determined by the maximum rate at which a DAC can receive and accurately convert data, and
2. Real-time delay, which is a function of the required real-time DAC output voltage signal.

The maximum settling time for a DAC (when switching from minus full scale to plus full scale) is 20 microseconds.

Under program control, one data transfer is possible in every four cycles (for example, every 3.0 microseconds on the 620/f-100 computer). If the DAC is to provide an accurate analog representation of the digital data, settling-time delay should be provided so that the interval between successive data transmissions to the DAC is greater than 20 microseconds.

Some examples of steps to provide time delay include:

1. A number of NOP instructions for short delays.
2. An indexed loop for longer delays.
3. Use of a real time clock.
4. Use of an external clock and sense lines.

The following example illustrates the use of an indexed loop to provide a time delay:

```
        LDX     IND             Load Index Value into X Register.

ONE     DXR                     Decrement the Index.
```

```
JXZ     TWO     Jump Out to TWO when Index Equals Zero.
JMP     ONE     Jump Back to ONE.
```

Note that settling-time delay may not be the same as the real-time delay required to generate a real-time voltage signal. The following considerations affect real-time delay:

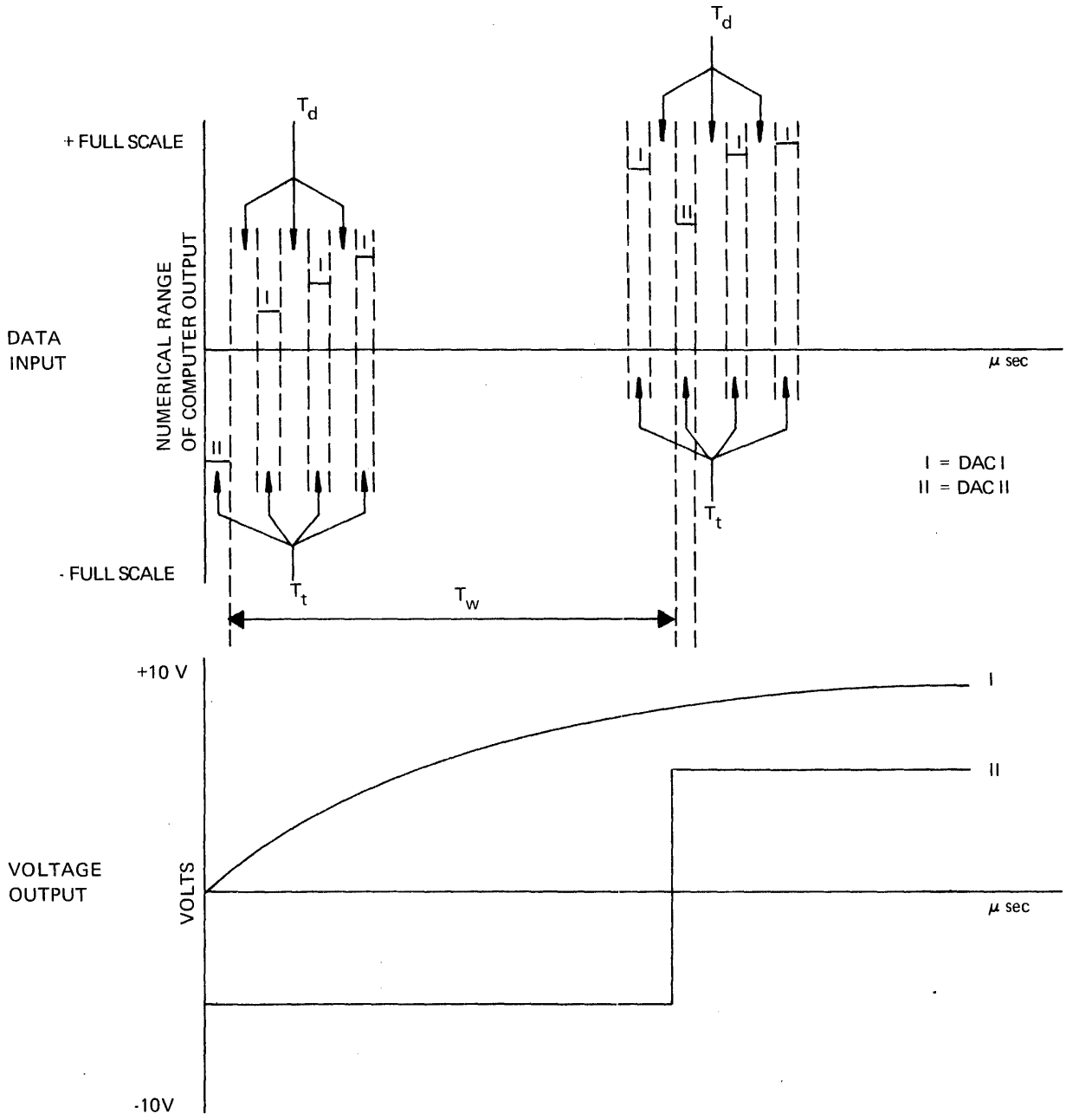
1. If data is being transferred to more than one DAC, then provision must be made for the time required to execute instructions that transfer data to other DAC's in the cycle.
2. Real-time delay should usually be greater than or equal to settling time delay.

Figure 2-1 illustrates settling-time delay and real-time delay for two voltage signals being generated simultaneously. Signal I is continuous, and requires the maximum data transmission rate; only settling-time separates these successive digital data inputs to DAC I. Signal II is a step function; it requires an initial signal at time zero and a reset signal after some real-time delay. The real-time delay in this example is computed using the cycle times of the program steps necessary for each data transfer. Lengthy real-time delays are more frequently controlled by an external clock, using a Sense line to initiate data transfers.

2.4 PROGRAMMING EXAMPLE

The following short program creates ramps via the A and B registers, and uses the X register to develop a time step during which the current contents of the A and B registers are output to two D/A converters.

```
ONE     LDBI    01777       Load A and B Registers.
        LDAI    0177000
```



T_t = TIME TO TRANSMIT ONE NUMBER TO DAC (μ sec.)
T_d = DESIRED MINIMUM DELAY BEFORE TRANSMITTING ANOTHER NUMBER TO THE SAME DAC.
T_w = DESIRED TIME DELAY BETWEEN TRANSMITTING TWO NUMBERS TO GENERATE SIGNAL (II).

Figure 2-1. Time Delays Required - 2 Voltage Signals/1 Program

```
TWO     EXC2    050     Load Contents of A Register into D/A
        OAR     050     Converters 0 and 1 Device
        EXC2    150     Address 50.
        OAR     050
        LDXI    0100    Inititalize X Register.
TRE     DXR             Decrement X Register.
        JXZ     GO      Branch Out if X Register is Zero.
        JMP     TRE     Return to X Register Decrement.
GO      IAR             Increment A Register.
        DBR             Decrement B Register.
        JBZ     ONE     Return to ONE If B Register
        JMP     TWO     is Zero; otherwise Return to TWO
```

2.5 DATA TRANSFER WITH BUFFER INTERLACE CONTROLLER

The Buffer Interlace Controller (BIC) is a hardware option which allows the user to transfer a block of data to or from a peripheral device using only one set of instructions. The user loads the first and last memory address location for a data block into special registers in the BIC; the BIC then transfers the specified data block to (or from) the peripheral device. Since data is transferred to a DAC, only this direction of data flow is considered in this section.

Once a program initiates the BIC data transfer, the BIC operates in parallel to the computer program, stealing cycles to read data from memory via direct memory access. The program can, therefore, proceed independently with other processing.

Typically, the program instructions for initializing a BIC are coded as a separate subroutine. The applications program then calls this subroutine when BIC usage is required. Table 2-4 illustrates the coding of a BIC initialization subroutine and demonstrates the usage of the subroutine within an applications program. This example assumes the BIC is assigned device address 20, 21 octal; the sequence of operations is as follows:

BIC Subroutine -

1. Sense that BIC is not busy, using a standard SEN 020 instruction. The BIC cannot be initialized while it is busy. If busy, loop until BIC completes its operation.

2. Initialize the BIC, using a standard EXC 021 instruction.

3. Store data block's initial and final addresses in the appropriate BIC address registers.

4. Enable the BIC for connection to device which will initiate the data transfer.

Applications Program -

1. Call BIC subroutine.

2. Check readiness of peripheral device that is to receive analog data from the DAC. Sense line M (0 to 7) at device address NN (50 to 57) is used to declare the device's status. Loop if device is busy.

3. Connect BIC to DAC, using an EXC instruction to initiate data transfer. An EXC 0YY instruction, where YY is the DAC device address, is used to output data. An EXC 1YY instruction is used to read gated input data.

4. The data block transfer will be complete when the BIC is, again, "not busy." The applications program may perform other processing and subsequently use SEN 020 and SEN 021 instructions to check for BIC-not-busy and BIC-abnormal-halt conditions.

Note that the BIC initial and final register addresses may be any pair of octal numbers in the range 20 through 27. Ordinarily, in systems employing more than one BIC, addresses 20 and 21 are assigned to the first BIC's registers; 22 and 23, 24 and 25, and 26 and 27 are assigned to the second, third, and fourth pairs of registers, respectively.

Table 2-4. Example of Instructions To Output Data Under BIC Control

Program Step			Function
BIC Subroutine -			
BICS	ENTR	0	
WAIT	SEN	020, GO	Go when BIC not busy.
	NOP		
	NOP		
	JMP	WAIT	
GO	EXC	021	Initialize BIC.
	OME	020, FIRST	Set start address of memory block.
	OME	021, LAST	Set end address of memory block.
	EXC	020	Enable BIC.
	RETU*	BICS	
Applications Program -			
	CALL	BICS	Set up BIC.
BUSY	NOP		
	NOP		
	SEN	MNN, BUSY	Loop if device busy.
	EXC	050	Connect BIC to DAC
	•		
	•		
	•		

2.6 EXTERNAL CONTROL

External Control signals may be generated by a computer program to provide a variety of logic controls for external devices.

The user has eight External Control lines available at each master DAC module. The instruction that causes an External Control Signal is:

EXC XYY

where X (0 to 7) defines one of eight External Control lines at DAC device address YY (50 to 57).

The signals are also made available to the backplane connectors so that they may be used to control certain portions of DAC logic when required by the use of an option such as the BIC. This use of External Control signals will depend on specific applications of the DAC module.

A program can set, but cannot reset, an External Control signal; reset is a function of external hardware. As determined by external interconnections, one External Control signal can reset another, other external electronic components can control reset, or the External Control signal can reset itself (pulse operation). Several methods for resetting External Control output signals are discussed in this section. These methods illustrate how the program can use the EXC command to trigger sequences of operations that have been predetermined by system hardware interconnection. The wiring configurations for these methods are illustrated in Figures 2-2 through 2-7. In all cases, some external wiring is required; the external modifications for each method are shown to the right of the vertical dashed line in each figure. Section 4.3 discusses the circuit logic for these reset types.

Command Sequence Reset

By connecting the EXC-N output of one latch to the REX-M of another latch, selecting the first will reset the second. This requires that the function codes in a series of EXC commands always follow the sequence prescribed by the latch interconnections. Figure 2-2 illustrates one configuration. In this example, the command sequence would progress from EXC-0 to EXC-7.

For example, in the following sequence of instructions used with this configuration, one External Control line resets one other line.

EXC	050	EXC 750 is automatically reset, EXC 050 is set.
EXC	150	EXC 150 is automatically reset, EXC 150 is set.
EXC	250	EXC 150 is automatically reset, EXC 250 is set.

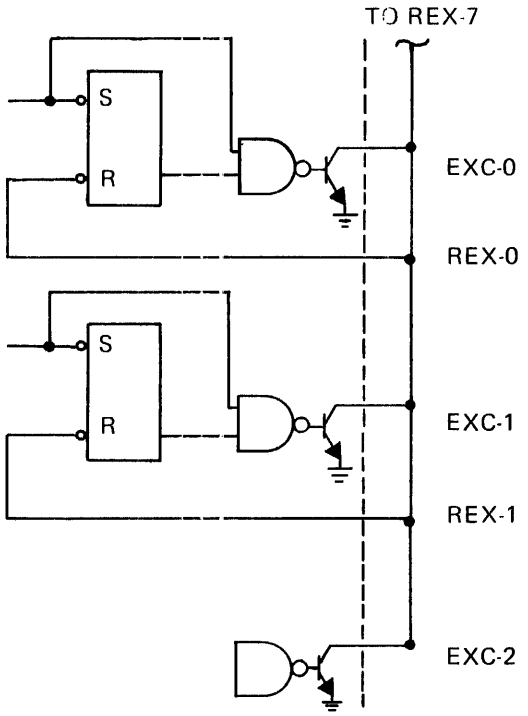


Figure 2-2. Command Sequence Reset Wiring

Special Assignment Reset

One latch can be assigned as the reset latch. An EXC command selecting that latch will then reset all other EXC latches. Figure 2-3 illustrates this configuration. The following sequence of program instructions used with this configuration functions as follows:

EXC	050	Set EXC 050.

EXC	150	Set EXC 150.
EXC	250	Set EXC 250.
EXC	750	EXC 050, EXC 150, and EXC 250 are automatically reset.

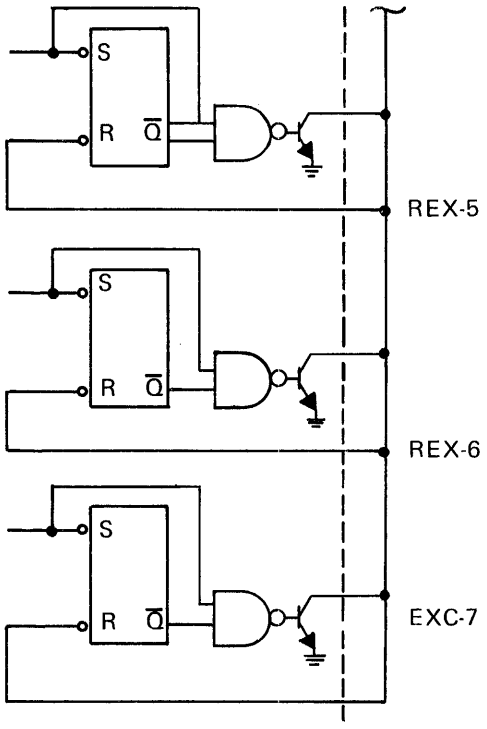


Figure 2-3. Special Assignment Reset Wiring

Fixed Delay Reset

An EXC latch can reset itself, following a suitable delay provided by an RC, transmission line, or other delay circuit. Figure 2-4 illustrates a typical latch circuit with an RC delay. An example of an instruction which can be used with such a configuration is as follows:

EXC	050	EXC is set for nn microseconds, then resets itself. (nn is determined by delay hardware added to the EXC output.)

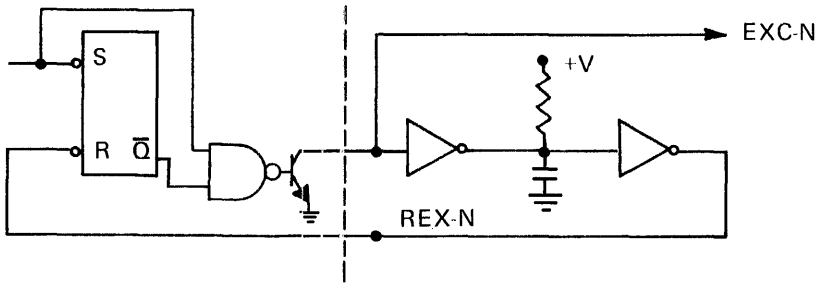


Figure 2-4. Fixed Delay Reset Wiring

Reset Returned By Receiving Device

The reset signal can be returned by the receiving device as shown in Figure 2-5. In this case, the pulse width is determined by the cable length. This insures that the pulse width is great enough for proper reception, regardless of cable capacitance.

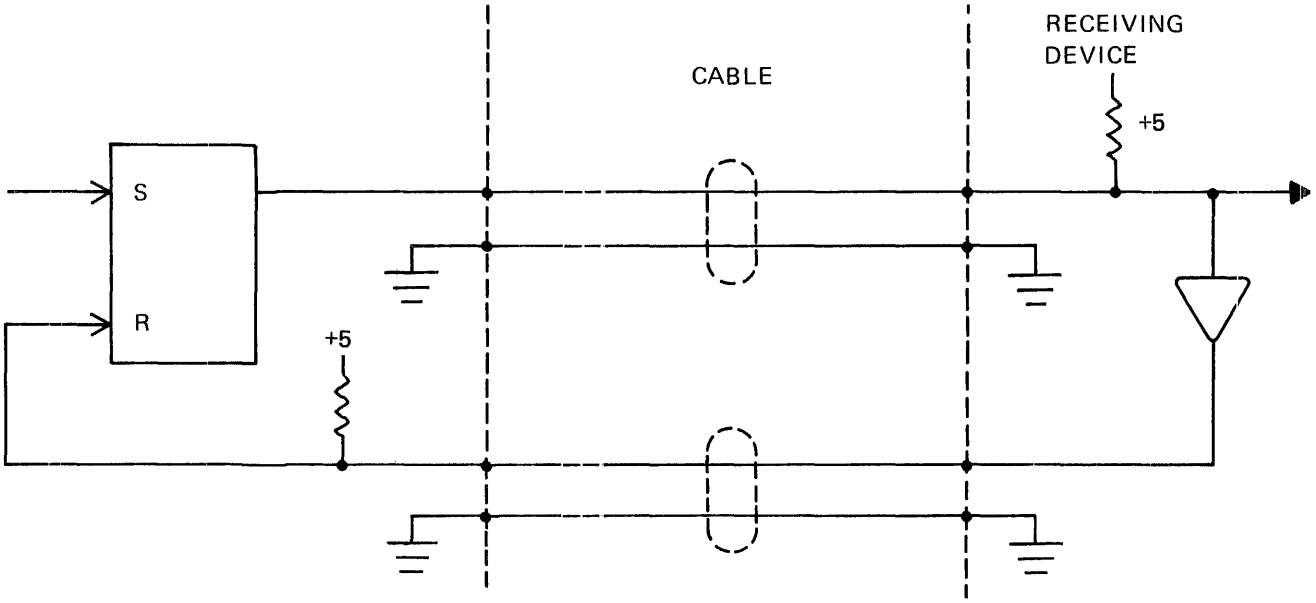


Figure 2-5. Reset Returned By Receiving Device

Automatic Reset

Connecting a REX-N output to ground will cause the EXC-N output to reset as soon as the EXC input to the latch goes false. In the 620/L-100 computer, this produces a 200 nanosecond pulse. (The pulse duration will differ slightly for other computers.) Figure 2-6 illustrates such a configuration. In this configuration, an EXC is set, and then reset after 200 nanoseconds. This is accomplished by making the EXC latch output follow the latch input, which is a 200 nanosecond pulse. Normally, the input pulse causes the EXC to be set "on", but the input pulse in no way influences resetting the EXC to "off".

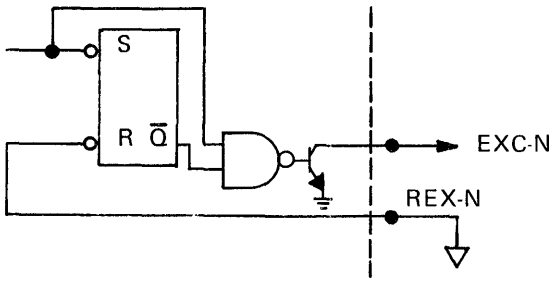


Figure 2-6. Automatic Reset Wiring

External Logic Reset

In this case, the flip-flop is set by the program and reset by the external device. This is especially useful in passing data or control commands; the program sets the EXC flag to indicate that data is ready, and the external device resets it to acknowledge that it has received the data or that it is ready to accept additional data. The EXC output is connected to a Sense input as well as to the external device, so the program can

determine that the acknowledgement has been received. (See Figure 2-7.) The same scheme can, of course, be used for receipt of data by the computer.

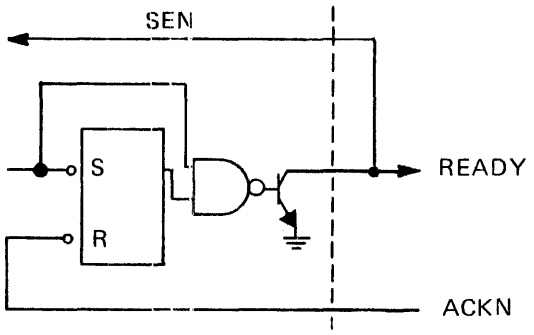


Figure 2-7. External Logic Reset Wiring

External Control Usage With BIC

Table 2-5 illustrates a program utilizing External Control Line 253 to connect the BIC to the DAC module located at device address 53. (Note that this would also require a jumper from EXC 253 to signal EPO-N, as discussed in Section 5.2). Statement FIVE connects the DAC at device address 53 to the BIC (assuming External Control line 2 at device address 53 has been connected to EPO-N of the BIC enable logic). Statement SIX resets EXC 253, then resets itself after a short delay. Figure 2-8 shows the logic that would be needed by the program in Table 2-5.

2.7 SENSE LINES

Sense lines allow the program to sense a signal from an external device, and branch depending on whether a Sense line is true or false.

There are eight external sense lines associated with each DAC device address. The command which selects a Sense line is:

SEN XYY

X (0 to 7) defines a specific line at device address YY (50 to 57).

Table 2-5 illustrates three uses of the SEN statement. Statement TWO inhibits data transfer via the BIC until Sense line 4 at device address 50 is sensed "false". The other two SEN statements are BIC system commands. (See 620 series or V73 system handbooks.)

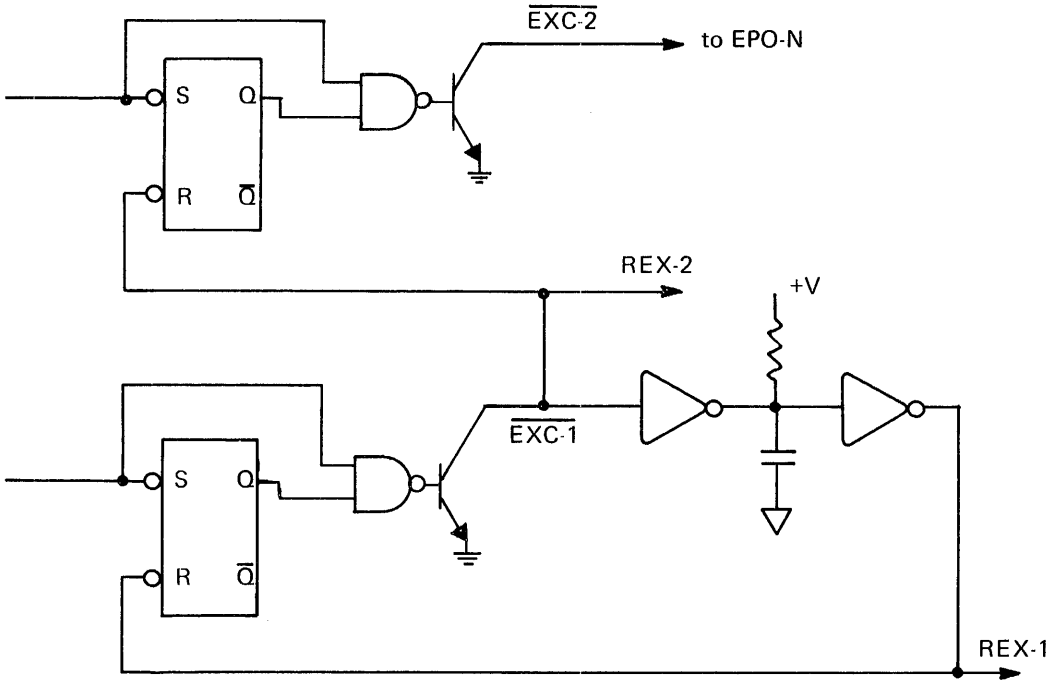


Figure 2-8. External Control To Connect and Disconnect BIC

Table 2-5. Use of External Sense Logic

Program Step			Function
WAIT	SEN	020, ONE	Sense BIC not busy.
	NOP		
	NOP		
	JMP	WAIT	
ONE	EXC	021	Initialize BIC.
	OAR	020	Output start address to BIC register.
	OBR	021	Output end address to BIC register.
	EXC	020	Enable BIC
NOP	NOP		
	NOP		
TWO	SEN	450, NOP	Start data transfer when Sense line 4 at device address 50 is "false". Branch back if "true."
FIVE	EXC	253	Connect BIC to DAC.
	SEN	021, TEN	Check for abnormal stop.
SIX	EXC	153	Reset EXC 253.

2.8 DAC SOFTWARE DRIVERS

Two driver programs are supplied to provide convenient access to digital-to-analog converters without detailed knowledge of hardware. These drivers may be used by themselves or embedded in an operating system.

The drivers and their functions are:

PDAC	Provides programmed data transfers.
DDAC	Provides direct memory transfers.

These drivers assume standard device address assignments (50_8 to 57_8) for the DAC modules. If other device addresses are used for DAC's, the drivers must be reassembled.

The drivers assume the following device address assignments for BICs:

Address (Octal)	Device
020 - 021	BIC, No. 1
022 - 023	BIC, No. 2
024 - 025	BIC, No. 3
026 - 027	BIC, No. 4

Programmed Data Transfer

The PDAC driver provides programmed data transfers to a selected DAC. A variable number of 16-bit words are transferred each time the driver is called. The time interval between data transfers is approximately 20 microseconds.

PDAC is called with the following assembly language sequence:

```
CALL PDAC, DACNR, NUM, SOURCE, EXIT
```

All entries in the calling sequence are either direct or indirect addresses which point to the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

DACNR - An integer value which specifies the D/A converter to which data is to be transferred. The range of DACNR must be between 1 and 64, inclusive; otherwise control passes to EXIT. The DACNR arguments correspond to the actual device address codes as follows:

DACNR	Device Address
1	050
2	150
3	250
•	•
•	•
•	•
9	051
•	•
•	•
•	•
64	757

NUM - An integer value which specifies the total number of 16-bit words to be transferred to the selected DAC.

SOURCE - The values in the SOURCE vector represent the data which is to be transferred to the selected DAC. Care should be taken to insure that integer data does not exceed the limits of the DAC size.

EXIT - The start address of the user's error routine. Control is transferred to EXIT when illegal input arguments are detected.

Programmed Data Transfer Example

The following example illustrates the use of PDAC. In this example, one word is transferred to DAC number 63 (device address 657 octal).

```
        CALL PDAC, = 63, = 1, WORD, ERROR
          •
          •
          •
ERROR   HLT         Error Exit
          •
          •
          •
WORD    DATA 10     Data Word to be Transferred
          •
          •
          •
```

Direct Memory Data Transfer

Two programs, DDAC and SDAC, are provided to utilize the BIC to transfer data directly from memory to a selected DAC without programmed intervention. DDAC and SDAC offer two advantages over PDAC:

- Data transfer rates are not limited by software overhead.
- The applications program is freed to work on other processes while the BIC supervises and controls the data transfer.

Unlike other peripherals, DACs do not have built-in logic to determine when the next data item should be transferred to them. Therefore, external hardware must be provided to indicate when data from memory is to be transferred to the DAC. This is accomplished by providing a Data Ready line at P1-73 on the computer backplane. The data transfer timing is completely under the control of this external control line.

In addition to this external signal, one of the eight EXC outputs on the master DAC module must be dedicated, and a jumper must be placed between P1-101 and P1-79. This provides a BIC connect function for the selected DAC. The DDAC driver uses the following EXC's for this function:

DACNR	EXC Used For BIC Connect
1-8	EXC 050
9-16	EXC 051
17-24	EXC 052
25-32	EXC 053
33-40	EXC 054
41-48	EXC 055
49-56	EXC 056
57-64	EXC 057

J1-9 also must be grounded so that the flip-flop associated with EXC 0XX is automatically reset.

Direct memory data transfer to a DAC is accomplished by a two-step process. First DDAC is called to initiate the transfer and return control immediately. Then, SDAC is called at the user's convenience to determine when the transfer is complete.

DDAC Driver

The DDAC driver is called with the following assembly language sequence:

CALL DDAC, BICNR, DACNR, NUM, SOURCE, EXIT

All entries in the calling sequence are either direct or indirect addresses of the arguments. Multiple levels of indirect address are permitted. The arguments are defined as follows:

BICNR - An integer value which specifies the BIC to be used for data transfer. The range of BICNR is from 1 to 4 corresponding to BIC device addresses $20\text{-}21_8$ through $26\text{-}27_8$. A value outside the legal range causes control to pass to EXIT.

DACNR - An integer value which specifies the individual D/A converter to be selected. The range of DACNR must be between 1 and 64 inclusive; otherwise control passes to EXIT. (See PDAC driver for a description of DACNR and actual device address relationship.)

NUM - An integer value which specifies the total number of 16-bit words to be transferred to the selected DAC.

SOURCE - The values in the SOURCE vector represent the data which is to be transferred to the selected DAC. Care should be taken to insure that integer data does not exceed the limits of the DAC size.

EXIT - The start address of the user's error routine. Control is transferred to EXIT when illegal input arguments are detected.

SDAC Routine

The SDAC routine checks the status of a previously-initiated direct memory data transfer. SDAC is called with the following assembly language sequence:

```
CALL SDAC, STATUS
```

The single entry in the calling sequence can be either a direct address or an indirect address which points to the actual argument. The argument is defined as follows:

STATUS - This argument receives a value of 0, 1 or 2 to indicate the status of the transfer operation:

Value	Meaning
0	Operation not complete
1	Operation complete; no errors
2	Operation aborted

Direct Memory Transfer Example

The following example illustrates the use of DDAC and SDAC. In this example, a sequence of numbers (0, 1, 2, . . . 100) is transferred to D/A converter number 10 (which is located at device address 0151). The transfer rate is determined by external hardware, and the transfer is performed by the BIC at device address 24_8 - 25_8. The program steps are as follows:

```
CALL DDAC,  = 3, = 10, = 101, RAMP, ERR
   •
   •
   •                    (Concurrent Processing)
```

```
WAIT    CALL SDAC, STATE        Check Status.
        LDA STATE               Test Status Word.
        JAZ WAIT                If Not Complete, Continue Wait.
        DAR                     If Complete, Check for Normal Completion.
        JAZ ...                 Normal Completion, Jump to Other Processing.
        JMP ERR                 Error.
ERR     HLT
RAMP    DATA 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10
        DATA 11, 12, 13, 14, 15, 16, 17, 18, 19, 20
           •
           •
           •
        DATA 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100
```

2.9 TEST PROGRAMS

A set of test programs is provided for DAC checkout. The set consists of three programs which may be selected through the Maintain II Test Executive. The programs, numbered 0 through 3, are as follows:

Test No.	Description
0	Returns control to the Test Executive Program.
1	Tests External Control and Sense lines.
2	Tests digital-to-analog converters.
3	Tests BIC interface.

These programs may be selected in any order and may be run as often as desired. This allows DACs with different device codes to be tested.

The minimum computer configuration on which the tests may be run is a 620 or V73 series computer with 4 K of memory, a teletype terminal, and a DAC card. In addition, a DAC test shoe (Part No. 03-950225) is required for running the tests.

Supervisor Program

A simple supervisor or test program selector is provided as part of the test package to allow the user to select individual tests and return control to the Test Executive

Program. The Test Executive Program is a standard Varian software option which must be loaded and run prior to the initiation of the DAC test package. Instructions for operating this program are given in the Test Program Manual (Publication No. 98A 9952-061). The DAC test package is loaded through the Test Executive.

When the Test Executive Program is running, the "L" command may be used to load the test package and transfer control to its supervisor. If the test package is already loaded, the "G500" command may be used to transfer control to the supervisor.

When the supervisor is activated, it responds by issuing a carriage return/line feed and by starting to print a series of prompting messages. The user must enter a valid response to each message as it is printed. An invalid response causes the message to be repeated. The first message is:

```
EXC, SENSE AND DAC TEST SUPERVISOR
ENTER DAC DEVICE ADDRESS?
```

The user must enter the DAC device address, which is an octal number between 050 and 057, followed by a period. The supervisor will then print:

```
ENTER BIC DEVICE ADDRESS?
```

The user must enter any of the following assigned octal numbers: 020, 022, 024, or 026 followed by a period.

The DAC and BIC device addresses entered at this time will be used throughout the three tests, where applicable. To change device address selections, the supervisor must be reactivated from the Test Executive Program or run from location 500. After the device addresses have been entered, the supervisor will print:

```
ENTER TEST NO. ?
```

The user should enter any number between 0 and 3 followed by a period. The supervisor will then transfer control to the selected test program, which will identify itself and perform its specified functions.

Test 1 should be used for each master DAC module to test the EXC and SENSE logic.

Test 2 should be used for each D/A converter in the system.

Test 3 should be used to check the BIC interface to the DAC's and should be exercised on each DAC that will be driven under BIC control.

Sense Switches

During all DAC tests, the sense switches may be used to control the mode of operation. The normal mode is followed when all switches are OFF; one or more switches may be set to control operation as follows:

SS1 — Sense switch 1 suppresses teletype printouts of test results and error messages. This function is useful to speed up the continuous execution of a test so that an oscilloscope may be used to monitor signals.

SS2 — Sense switch 2 causes a test to repeat indefinitely without user intervention.

SS3 — Sense switch 3 terminates execution of a test and returns control to the supervisor. If sense switch 3 is set when the supervisor requests a new test number, the following message will be printed:

RESET SENSE SWITCH 3

A new test may be selected after SS3 is reset.

Test 1 - External Control and Sense Test

This test uses a special test shoe which must be plugged into J1 and J2 of the DAC card. The test checks all EXC and Sense lines on a given device address. The test shoe is designed to connect each EXC output to a Sense input and to reset another EXC according to the following table.

EXC Output	Sense Line	EXC Reset
00XX	07XX	05XX
03XX	04XX	00XX
04XX	03XX	03XX
01XX	06XX	04XX
02XX	05XX	01XX
06XX	02XX	02XX
07XX	01XX	06XX
05XX	00XX	07XX

Therefore, at each step in the table only one of the Sense lines should be true at a time. All Sense lines are polled after each step and errors are reported if detected and if sense switch 1 is reset.

When the test program is activated, it will print:

EXTERNAL CONTROL AND SENSE TEST

If no errors occur during the execution of the test, the program returns control to the supervisor after printing the following message:

TEST PASSED

If errors occur during the test, one or more of the following messages will be printed:

EXC 00XX OR SEN 07XX ERROR
EXC 03XX OR SEN 04XX ERROR
EXC 04XX OR SEN 03XX ERROR

EXC 01XX OR SEN 06XX ERROR

EXC 02XX OR SEN 05XX ERROR

EXC 06XX OR SEN 02XX ERROR

EXC 07XX OR SEN 01XX ERROR

EXC 05XX OR SEN 00XX ERROR

If the first error occurs, the problem may be in the address decoder logic on the master DAC card.

Test 2 - DAC Test

Each DAC card has two digital-to-analog converters. For purposes of these tests the converters at a particular device are numbered as shown in Table 2-3.

The DAC test program provides for the checking of any of 64 DACs, one at a time. The test provides a full scale negative to full scale positive ramp in one count increments.

Ten, twelve, and fourteen-bit DAC's may be tested with this program. The following table shows the plus full scale and minus full scale values for each DAC size.

No. of Bits	+Full Scale	-Full Scale	Signal Rep Rate (Hz)
10	511	-512	139.3
12	2047	-2048	34.7
14	8191	-8192	8.7

When the program is activated, it will print:

DAC RAMP TEST

ENTER DAC NO. ?

The user must enter any number from 0 to 7 followed by a period. The test program then requests the DAC size:

ENTER NO. OF BITS?

The user must enter the appropriate DAC size, either 10, 12, or 14 followed by a period.

The ramp will be continuously generated until sense switch 3 is set. No errors are generated by the test program. An oscilloscope may be used to monitor the voltage and check that the DAC functions properly. The DAC outputs are on J2-1 for even numbered DACs and J2-43 for odd numbered DACs. All other terminals on the J2 connector are at analog ground.

Test 3 - BIC Interface Test

This test exercises the BIC interface by outputting data to the DAC under BIC control. A monotonically decreasing bipolar waveform consisting of eighteen data points is output to the DAC through the BIC. The waveform starts at full scale and decreases to zero.

EXC 0 on the DAC is used to connect the DAC controller to the BIC. To provide for this, P1-101 must be wired to P1-79.

The BIC transfers a word of data to the DAC controller whenever the DEVICE READY line (P1-73) goes low. To keep more than one word from being transferred, this signal may go low for only one machine cycle. EXC 5 is used to control this function in conjunction with EXC 0. EXC 5 (P1-87) is wired to DEVICE READY (P1-73). EXC 0 resets EXC 5 and causes the trap out. EXC 5 is given directly thereafter to inhibit further trap outs.

EXC 5 is used in this fashion for test purposes only and the jumper from P1-87 to P1-73 should be removed after the testing is completed.

When the test program is activated, it will print:

```
DAC - BIC TEST
ENTER DAC NO. ?
```

The user must enter the appropriate DAC number from 0 to 7 followed by a period. The test program then requests the DAC size:

ENTER NO. OF BITS

The user must enter the appropriate DAC size, either 10, 12, or 14 followed by a period.

The waveform will be continuously generated until sense switch 3 is set. No errors are generated by this program.

3. THEORY OF OPERATION

3.1 DATA CONVERSION NETWORK

The DAC output voltage is provided by an operational amplifier whose input is the sum of a set of scaled currents (see Figure 3-1).

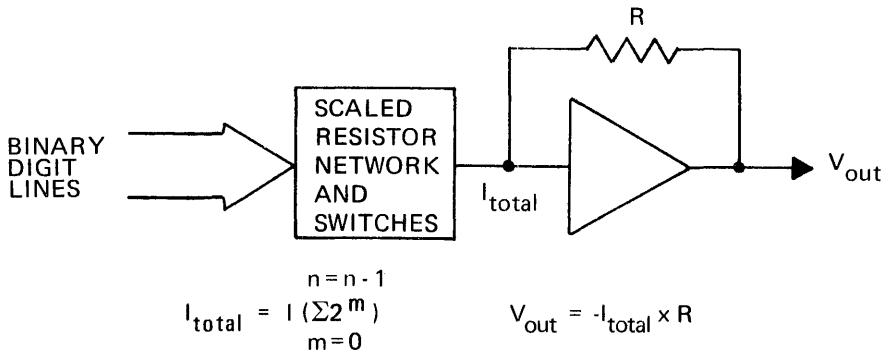


Figure 3-1. Basic DAC Simplified Diagram

The individual scaled currents are provided by current switches arranged in a ladder network.

Each switch is controlled by a different bit of the data word received from the computer. A relative-high output from the data buffer register in a bit position turns the corresponding switch on, adding its weighted current to the total current. A relative-low output turns the switch off so that it contributes no current to the sum.

3.2 DAC SWITCHES

Figure 3-2 represents a single DAC switch; the reference designators are arbitrary and do not apply to any actual assemblies. Refer to Appendix C for detailed schematics of the DAC switches.

When a data bit out of the buffer register is relative-high (approximately +4 Vdc), current steering diode CR1 is reverse biased. This directs current flowing through precision resistor R1 to the virtual ground summing junction. When a data bit out of the buffer register is a relative-low (approximately +0.5 Vdc), CR1 is forward biased and current from R1 flows through CR1 to the -15 Vdc sink; no current flows to the summing junction. The voltage levels present at the cathode of CR1 are approximately +1 Vdc when the data bit is high and approximately -1 Vdc when the data bit is low.

The value of precision resistor R1 determines the current through the switch and, consequently, the amount of current that switch adds to the summing junction. The precision resistor for each switch is scaled to provide an amount of current corresponding to the weighted value of the bit position controlling that switch.

CR2 and CR3 are matched diodes that, together, cancel the effect of temperature variations on the voltage drop across the switch.

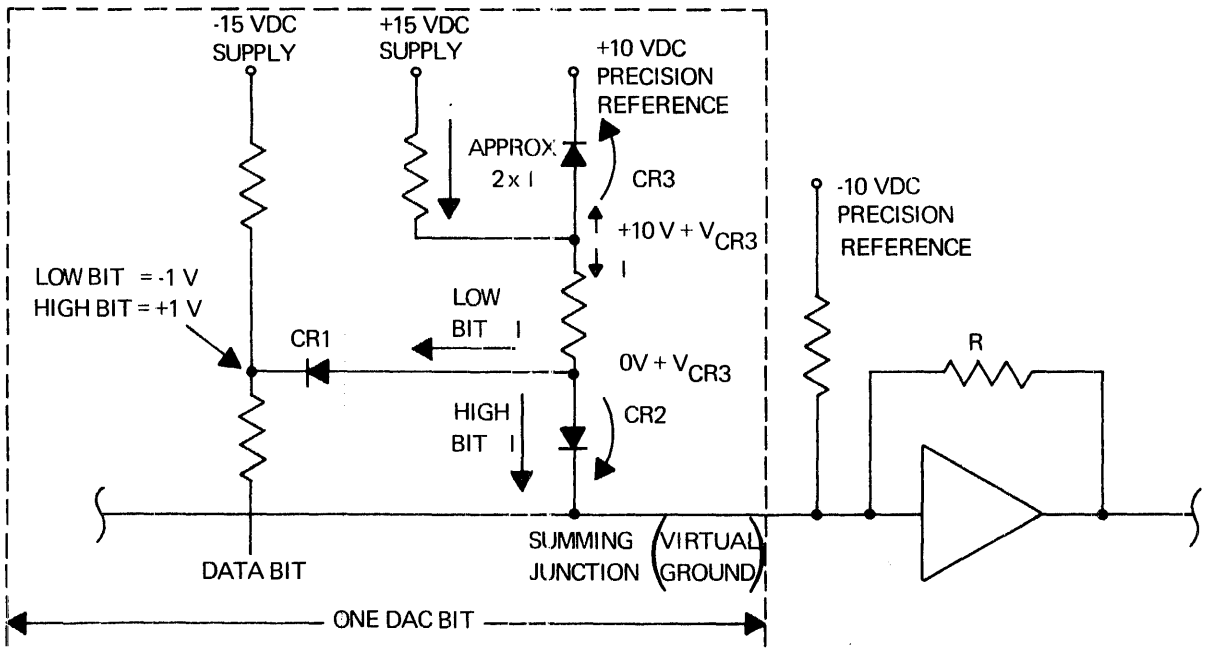


Figure 3-2. Current Steering Switch

3.3 SWITCH LADDER

A DAC may have any one of three resolutions: 10, 12, or 14 bits. The switch ladder schematic shown in Appendix C represents a DAC with 14-bit resolution. The current switches are arranged in a ladder network.

The amount of current added to the summing junction by a switch is directly proportional to the relative significance of the bit controlling that switch. The least significant bit controls the switch that supplies the least amount of current. The most significant data bit controls the second-most significant switch, with the sign bit controlling the most significant switch.

For DACs of 12- or 10-bit resolution, the two or four most significant switches are deleted. Since the sign bit must be preserved, a jumper connection at the buffer register input directs that bit to the most significant switch regardless of the DAC's resolution.

The three most significant switches on 14-bit DACs include calibration resistors. The values of these resistors are set during final assembly according to the results of a computer calibration program. Although field calibration is not normally required, these resistors may be adjusted to assure specified accuracy for these switches.

An attenuating resistor network, in series with the six least significant switches, allows the use of smaller values than would otherwise be required for these positions.

3.4 POWER SUPPLIES AND REFERENCE VOLTAGES

Two regulated power supplies, +15 Vdc and -15 Vdc, are provided by circuits located on a power supply module.

The +10 Vdc and -10 Vdc precision references are provided by voltage supplies contained on the DAC module. If two converters occupy the same module, they share the same reference voltages.

Output of the minus reference, as measured at its test point, is within the range +8.5 Vdc to +9.5 Vdc. This output is stable to within $\pm$0.1 mV. Coarse and fine adjustments set the amount of constant offset current provided to the summing junction from the minus reference. With all switches open, this offset current is provided entirely by the output amplifier feedback loop, and the amplifier output voltage is at + full scale.

Output of the plus reference source is +10 Vdc $\pm$0.1 mV. The feedback resistance of this circuit may be calibrated with both coarse and fine adjustment.

3.5 OUTPUT AMPLIFIER

The output amplifier converts the switch current sum to an inverted voltage output with a gain of one. Resistance values of the amplifier's feedback loop, the minus reference load and the sign bit switch are nominally equal.

When all current switches are open, output of the amplifier is plus full scale (approximately +10 Vdc) and full current flows from the amplifier output through the feedback loop to the minus reference. When all current switches are closed, amplifier output is at minus full scale (-10 Vdc) and full current flows from the summing junction through the feedback loop to the amplifier output. The crossover point (0 Vdc) is produced when the sign bit switch is open and all others are closed. All currents leaving the bit switches sum together and flow into the minus reference; no current flows through the output amplifier and feedback loop.

Tables 3-1 through 3-3 compare switch settings with the corresponding amplifier output voltage levels for various digital numbers received from the computer. Output voltage levels for other numerical values in the allowed range can be derived by application of one of the following equations:

14-bit DAC

$$V_{out} \approx N\ (1.2\ mV)$$

12-bit DAC

$$V_{out} \approx N\ (4.88\ mV)$$

10-bit DAC

$$V_{out} \approx N\ (19.52\ mV)$$

where N is the decimal value of the number received from the computer.

For example, the decimal number -5250 would result in a voltage output from a 14-bit DAC of:

$$V_{out} \approx -5250\ (1.2\ mV) \approx -7.3\ V$$

Table 3-1. 14-Bit DAC Output Scale

ANALOG VALUE				COMPUTER OUTPUT AND SWITCH SETTINGS													
				EB 15 SW	EB 12 SW	EB 11 SW	EB 10 SW	EB 09 SW	EB 08 SW	EB 07 SW	EB 06 SW	EB 05 SW	EB 04 SW	EB 03 SW	EB 02 SW	EB 01 SW	EB 00 SW
RANGE	DECIMAL	OCTAL	Vout	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+Full Scale-1	+8191	017777	+9.999	0	1	1	1	1	1	1	1	1	1	1	1	1	1
				0	0	0	0	0	0	0	0	0	0	0	0	0	0
+Half Scale	+4096	010000	+5.000	0	1	0	0	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	1	1	1	1	1	1	1
+1 LSB	+1	01	+0.0012	0	0	0	0	0	0	0	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1	1	1	1	1
- LSB	- 1	17777.7	-0.0012	1	1	1	1	1	1	1	1	1	1	1	1	1	1
				1	0	0	0	0	0	0	0	0	0	0	0	0	0
-Half Scale	-4096	170000	-5.000	1	1	0	0	0	0	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	1	1	1	1	1	1	1
-Full Scale+1	-8191	160001	-9.999	1	0	0	0	0	0	0	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	1	1	1	1	1	1	0
-Full Scale	-8192	160000	-10.000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE

The data contents of all the E bus lines are inverted once, except for the sign bit, which is inverted twice. This means a true level on an E bus data line (0 vdc) opens its switch, which tends to make the amplifier output more positive.

Table 3-2. 12-Bit DAC Output Scale

ANALOG VALUE				COMPUTER OUTPUT AND SWITCH SETTINGS											
				EB 15 SW 11	EB 10 SW 10	EB 09 SW 9	EB 08 SW 8	EB 07 SW 7	EB 06 SW 6	EB 05 SW 5	EB 04 SW 4	EB 03 SW 3	EB 02 SW 2	EB 01 SW 1	EB 00 SW 0
RANGE	DECIMAL	OCTAL	Vout												
+Full Scale -1	+2047	3777	+ 9.995	0	1	1	1	1	1	1	1	1	1	1	1
				0	0	0	0	0	0	0	0	0	0	0	0
-Half Scale	+1024	2000	+ 5.000	0	1	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1
+1 LSB	+ 1	1	+ 0.005	0	0	0	0	0	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1	1	1
-1 LSB	- 1	177777	- 0.005	1	1	1	1	1	1	1	1	1	1	1	1
				1	0	0	0	0	0	0	0	0	0	0	0
-Half Scale	-1024	176000	- 5.000	1	1	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1
+Full Scale +1	-2047	174001	- 9.995	1	0	0	0	0	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	1	1	1	1	0
-Full Scale	-2048	174000	-10.000	1	0	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1

Table 3-3. 10-Bit DAC Output Scale

ANALOG VALUE				COMPUTER OUTPUT AND SWITCH SETTINGS										
RANGE	DECIMAL	OCTAL	Vout	EB 12 SW 9	EB 08 SW 8	EB 07 SW 7	EB 06 SW 6	EB 05 SW 5	EB 04 SW 4	EB 03 SW 3	EB 02 SW 2	EB 01 SW 1	EB 00 SW 0
+Full Scale -1	+511	777	+ 9.980	0	1	1	1	1	1	1	1	1	1
				0	0	0	0	0	0	0	0	0	0
+Half Scale	+256	400	+ 5.000	0	1	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1
+1 LSB	+ 1	1	+ 0.020	0	0	0	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1
-1 LSB	- 1	177777	- 0.020	1	1	1	1	1	1	1	1	1	1
				1	0	0	0	0	0	0	0	0	0
-Half Scale	-256	177400	- 5.000	1	1	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1
-Full Scale +1	-511	177001	- 9.980	1	0	0	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	1	1	0
-Full Scale	-512	177000	-10.000	1	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1

4. I/O INTERFACE THEORY OF OPERATION

The DAC Modules coordinate three types of communication between the computer and peripheral device: digital-to-analog data out, External Control signals out, and Sense signals in. The DAC logic responsible for providing these three interfaces is discussed in this section.

All communication between the DAC and the computer is conducted on the computer I/O bus. In the following discussion, mnemonics used to identify E-bus signals include the suffix "I". Signals transferred between the DAC and the BIC are carried on the B-bus; mnemonics for these signals include the suffix "B". Refer to Varian 620 and V73 system handbooks and Buffer Interlace Controller Manual for details regarding communication conducted via the computer I/O bus.

The following discussions are keyed by letter designations to schematics and logic diagrams presented in Appendix C.

4.1 PROGRAM-CONTROLLED DATA TRANSFER

A data transfer operation, resulting in a digital-to-analog conversion, occurs in two stages. First, the individual DAC is selected; then a data word is sent to the DAC buffer register inputs and strobed into the selected register.

DAC Selection Stage

The selection stage begins when the computer enters the desired device address and function code on E bus lines EB00-I through EB05-I and EB06-I through EB08-I. An NAND gate on the addressed master DAC decodes the device address and generates a Device Select signal. This is combined with the control line pulse FRYX-I (Function Ready). The resulting signal Function Select combines with a true level on EB15-I to clock the contents of the function code into the EXC2 storage register.

The EXC2 Decode Logic selects one of eight output lines, EXC2-0 through EXC2-7, according to the contents of the function code. Each EXC2 line is connected via a wire wrap jumper in the backplane to the clock input gate of a different DAC buffer register. An active EXC2 line enables one of three inputs to the clock input gate in preparation for the data transfer stage of the operation.

Data Transfer Stage

The device address is again placed on the E bus. A true level on EB14-I identifies the operation as a data transfer out and, together with Function-Select, sets the data transfer out (DTOS) latch. Output of the DTOS latch enables the second input to the clock input gate.

After the control pulse FRYX-I goes false, the computer removes the device address from the E bus and places a data word on lines EB00-I through EB14-I, with a sign bit on EB15-I. This is followed by the control pulse DRYX-I. DRYX-I enables the clock input gate of the selected DAC buffer register, clocking the data into the register. DRYX-I also resets the DTOS latch.

After DRYX-I goes false, the only true input to the clock input gate of the register is provided by the selected EXC2 line. This input remains true until a different EXC2 line at that device address is selected. Until that time, subsequent data transfer operations for that device address will be routed to the same DAC, without requiring another EXC2 instruction.

4.2 BIC-CONTROLLER DATA TRANSFER

When a data transfer is under BIC control, a different set of DAC logic is involved.

DAC Selection Stage

The DAC selection stage is the same for a BIC-controlled data transfer as for a program-controlled data transfer; the data transfer stage, however, is not.

Data Transfer Stage

The DAC module is selected by a special signal, EPO-N, which is made available through custom hardwire connections. One method for providing this signal is to jumper an EXC output to the EPO-N pin (P1-79) and execute an EXC instruction selecting that line. All eight EXC signals are made available to the backplane by the DAC for this reason.

The EPO-N pulse is combined with the BIC-generated signal DCEX-B. Together they set the DAC's Connected latch. When the BIC receives the output of the Connected latch, CDCX-B, indicating that the DAC has been connected, it resets DCEX-B. The Connected latch remains set, however, until the end of the data transfer.

Output from the Connected latch is also returned to the BIC as TROX-B and TRQX-B. TROX-B identifies the direction of the data transfer (from the computer to the DAC) and TRQX-B is a request for data.

TRQX-B will be true while the Connected latch is set if the signal Device Ready is true. Device Ready is a pulse that indicates that the DAC has had sufficient time to convert the last data word or that the external device can accept a new voltage signal from the DAC.

Since Device Ready determines the rate at which data words are supplied to the DAC, the maximum frequency with which that signal occurs must be determined by the speed of the DAC or the external device. Settling times for DACs of different resolutions are given in the table of specifications. Device Ready may be provided in a number of ways, using external hardware. The choice of method will depend on the specific application. Suggested implementation is the application of the pulse output from the programmable timer contained on the ADC module or the use of a standard laboratory pulse generator.

With Device Ready true and Transfer Enable false (data word has not yet been placed on the E-bus), TRQX-B is true. When the BIC receives TRQX-B, it causes the computer

to place the data on the E-bus and responds to the DAC with TAKX-B. TAKX-B produces Transfer Enable, which resets TRQX-B and enables the second input to the clock input gate of the selected DAC. Transfer Enable is the BIC equivalent to DTOS.

After the computer places the data word on the E-bus, it generates DRYX-I. This control pulse enables the clock input gate of the DAC buffer register, clocking the data into the register. When Deivce Ready goes true again, TRQX-B will go true and another data word will be transferred. This sequence is repeated until the last word in the block has been transferred. At that time, DESX-B from the BIC resets the connected latch, disconnecting the DAC.

4.3 EXTERNAL CONTROL DECODE

Each master DAC module makes available eight EXC outputs. An output goes true (ground) when its flip-flop is set by the EXC decode logic. A function code, provided by the computer as a result of an EXC program instruction, specifies which EXC output flip-flop is set.

EXC output flip-flops are not reset by program instructions alone; they may be reset through a variety of hardware or hardware/software techniques. Some examples of methods for resetting EXC output flip-flops are discussed in Section 2.6.

The EXC output driver is capable of providing signals at levels up to +30 volts, with current sinking of up to 300 mA (see Appendix B).

4.4 SENSE DECODE

Every master DAC is capable of sampling, one at a time, up to eight Sense input lines and forwarding the logic level present on the selected line to the computer. A function code, provided by the computer as a result of a SEN program instruction, specifies which sense input is to be sampled.

Sense input signals are considered logically true when they are at 0 Vdc and logically false at +4 Vdc. When sampled, a logically true input will cause a jump condition in the program. The DAC provides a 5.6 K pullup resistor to +5 volts on each Sense input. It is, therefore, not necessary to drive the Sense inputs high. The Sense inputs are normally connected to external logic (0 to +5 volts) or switch closures to ground.

Note: Sensed signals should not be allowed to go negative with respect to DAC logic ground and should not be allowed to go more positive than the DAC +5 volts.

5. INSTALLATION

5.1 PREREQUISITES

Each DAC or DACE requires one card slot in either the mainframe or Memory Expansion/ Peripheral Controller frame. No special slots are reserved for use by DACs; their location in the frame is determined solely by considerations of convenience in backplane wiring.

An Analog Power Supply Module (Part No. 620-88) must be installed when using one or more DAC or DACE moudles. If a Power Supply Module has been previously installed and sufficient current is available to support the DAC modules, an additional power supply need not be installed.

5.2 INSTALLATION AND INTERCONNECTION

A DAC or DACE is installed vertically, with its component side to the installer's left in 620/i and 620/L computers, and horizontally in the 620/f computer. Figure 5-1 illustrates a typical installation.

CAUTION

Do not install DAC modules in slots that have been previously wired to provide power to other modules; if the intended slot is already wired, remove any connections to power before installing the DAC module to protect its components. Refer to Table 5-1 for proper power connection.

The card is installed with the double pin edge pointing toward the installer. Proper orientation of the module is important since the cards are not keyed.

Connection to the computer I/O-bus and the BIC option B-bus is provided through backplane wiring. All pin assignments for the I/O-bus and B-bus are listed in Appendix A.

For each DAC, connections to external instruments include one or two DAC outputs and may include up to eight External Control outputs and up to eight Sense inputs. Connections between DAC and DACE modules may also be required (for example, EXC2 and DAC Enable outputs from a master DAC to digital-to-analog converters located on slave DACEs). Pin assignments for these connections are also listed in Appendix A. Recommended connector types for J1 and J2 are identified in the summary of key specifications in Appendix B.

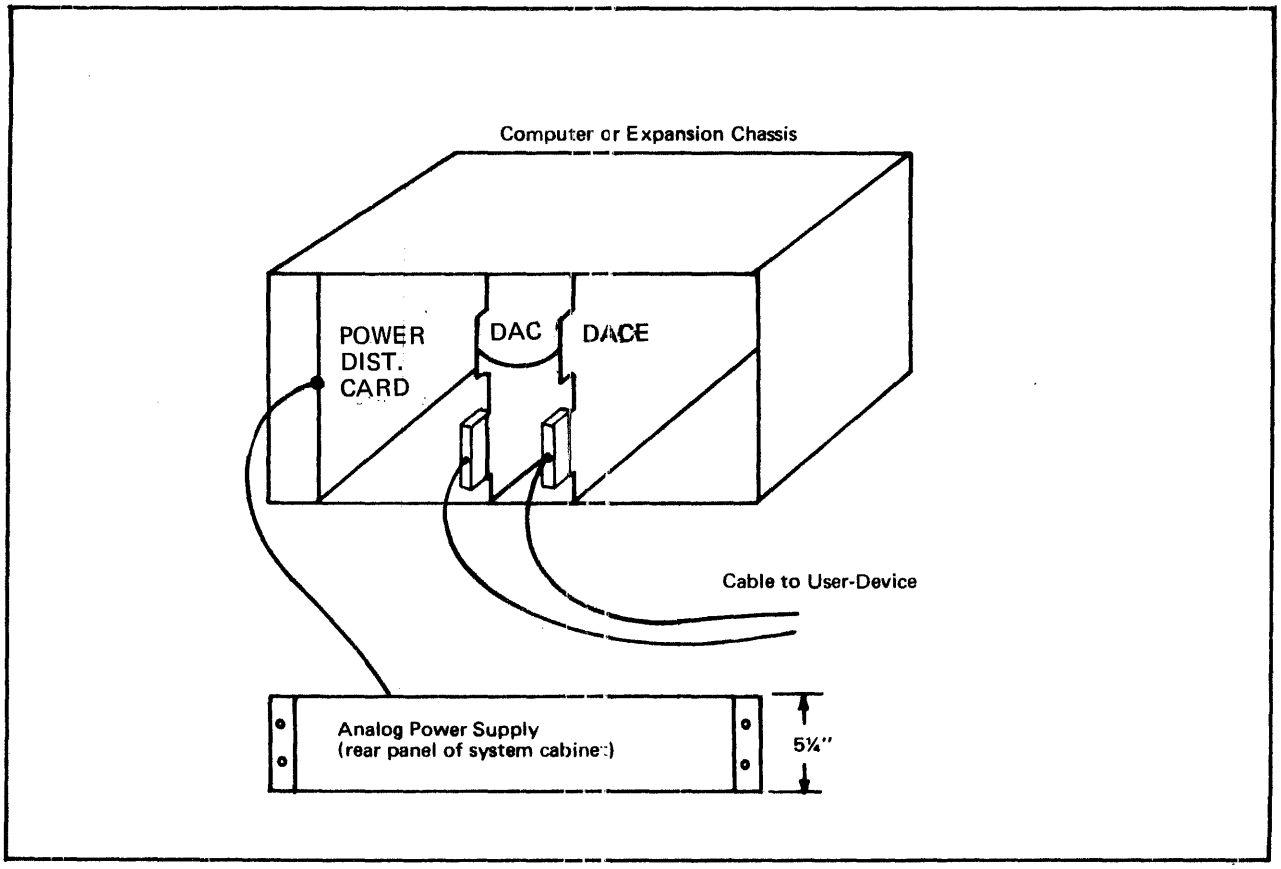


Figure 5-1. Typical Module Installation

Power Supply Wiring

Connections to the DAC must be made for three power supply voltages and senses, an analog ground, digital ground, and digital ground sense. Table 5-1 lists the pin assignments on the DAC wirewrap backplane for these connections. When the DAC is used with other modules (ADCMs, DACEs, MUXs, etc.), similar voltages should be tied together, and the voltage sense line should be brought from the mid-point of the voltage tie-line to a voltage sense line on the power supply wirewrap backplane.

The voltages and sense points for the power supply backplane are given in the Power Supply Manual (Publication No. 03-996-812).

Table 5-1. DAC Wirewrap Backplane Pin Connections for Power Supply

Power Supply Voltage	DAC Pins
Digital Ground	P1-1, 48, 100, 122
+5 Vdc	P1-118, 121
+15 Vdc	P1-111
-15 Vdc	P1-113
Analog Ground	P1-115

Device Address Wiring

Table 5-2 lists the jumper connections required to wire a device address for a master DAC. Note that P1-76 (Enable) is not normally used. It is available, however, and may be used as an additional addressing condition. For example, if multiple master DAC modules have the same device address, the Enable input can be used to permit only one module to respond to that address at a given time.

Table 5-2. Device Address Wiring

Address	Wirewrap Jumpers		
050	P1-72 to P1-71	P1-69 to P1-68	P1-66 to P1-65
051	P1-72 to P1-71	P1-69 to P1-68	P1-66 to P1-64
052	P1-72 to P1-71	P1-69 to P1-67	P1-66 to P1-65
053	P1-72 to P1-71	P1-69 to P1-67	P1-66 to P1-64
054	P1-72 to P1-70	P1-69 to P1-68	P1-66 to P1-65
055	P1-72 to P1-70	P1-69 to P1-68	P1-66 to P1-64
056	P1-72 to P1-70	P1-69 to P1-67	P1-66 to P1-65
057	P1-72 to P1-70	P1-69 to P1-67	P1-66 to P1-64

EXC2 Output Wiring (DAC Select)

Table 5-3 lists the jumper connections required to wire the eight EXC2 outputs to select individual converters on the DAC and DACEs.

Table 5-3. DAC Select Connections

EXC2 Output	Master (DAC 1) Pin		Pin		DAC Card
0	P1-110	to	P1-77	of	1
1	P1-112	to	P1-78	of	1
2	P1-114	to	P1-77	of	2
3	P1-103	to	P1-78	of	2
4	P1-104	to	P1-77	of	3
5	P1-105	to	P1-78	of	3
6	P1-106	to	P1-77	of	4
7	P1-107	to	P1-78	of	4

External Control Reset Wiring

Provision must be made for resetting External Control outputs. Basic information on techniques for resetting the outputs is presented in Section 2.6. One possible configuration is illustrated in Table 5-4; this configuration converts the eight EXC flags to four RS flip-flops with both set and reset driven by the program.

Table 5-4. External Control Reset Wiring

Signals	Master DAC	Master DAC
EXC1/REX0	J1-6	J1-5
EXC3/REX2	J1-12	J1-11
EXC5/REX4	J1-18	J1-17
EXC7/REX6	J1-24	J1-23

Device Ready and EPO-N Wiring

DACs used in conjunction with the BIC option require that two special signals be provided to the master DAC. One, called Device Ready, synchronizes data transfer with the DAC or external device operation; it is applied to P1-73 of the master DAC. The other, called EPO-N, selects the DAC for connection to the BIC; it is applied to P1-79 of the master DAC. If a BIC is not used P1-79 should be grounded. Further discussion of this wiring can be found in Section 4.2 of this manual.

5.3 INSTALLATION EXAMPLE

A typical single DAC module could be installed with the following wiring:

Device Address 050

P1-71 wired to P1-72
P1-68 wired to P1-69
P1-65 wired to P1-66

DAC Select Connections

P1-110 wired to P1-77
P1-112 wired to P1-78

BIC Control

P1-79 wired to P1-101
P1-73 wired to P1-87

Note: If a BIC is not used, P1-79 should be grounded.

Note that appropriate EXC Reset wiring would also be configured. See Sections 2.6 and 5.2 for further details. In addition, analog power supply wiring would be required, as described in Section 5.2.

APPENDIX A: DAC PIN ASSIGNMENTS

BACKPLANE WIRING

PIN NO.	NAME	FUNCTION
P1-1	Digital ground	
-2	EB00	One bit of Device Address or data word
-3	Digital ground	
-4	EB01	One bit of Device Address or data word
-5	Digital ground	
-6	EB02	One bit of Device Address or data word
-7	Digital ground	
-8	EB03	One bit of Device Address or data word
-9	Digital ground	
-10	EB04	One bit of Device Address or data word
-11	EB05	One bit of Device Address or data word
-12	EB06	One bit of EXC, EXC2 or SEN code or data word
-13	EB07	One bit of EXC, EXC2 or SEN code or data word
-14	EB08	One bit of EXC, EXC2 or SEN code or data word
-15	EB09	One bit of data word
-16	EB10	One bit of data word
-17	EB11	EXC tag line or one bit of data word
-18	EB12	Sense tag line or one bit of data word
-19	EB13	One bit of data word
-20	EB14	Data tag line or one bit of data word
-21	EB15	EXC2 tag line or one bit of data word
-22	Digital ground	
-23	Not used	
-24	Digital ground	
-25	Not used	
-26	Digital ground	
-27	FRYX	Device Address tag line
-28	Digital line	
-29	DRYX	Gates data into buffer register
-30	Digital ground	
-31	SERX	Sense input to computer
-32	Digital ground	
-33	Not used	

PIN NO.	NAME	FUNCTION
P1-34	Digital ground	
-35	Not used	
-36	Digital ground	
-37	Not Used	
-38	Digital ground	
-39	Not used	
-40	Digital ground	
-41	Not used	
-42	Not used	
-43	SYRT	Resets system logic
-44	IUAX	Interrupt acknowledge from computer
-45	Not used	
-46	Not used	
-47	Not used	
-48	Digital ground	
-49	TRQZ	Transfer Request from AOM to BIC
-50	TROX	Identifies direction of BIC-controlled data transfer
-51	Digital ground	
-52	Not used	
-53	Digital ground	
-54	CDCX	Notifies BIC that AOM is connected
-55	Digital ground	
-56	DCEX	Connect signal from BIC
-57	Digital ground	
-58	TAKX	Transfer Request acknowledge from BIC
-59	Digital ground	
-60	DESX	Disconnect from BIC
-61	Not used	
-62	Not used	
-63	Not used	
-64	EB00+	Jumper connection for wiring Device Address
-65	EB00-	Jumper connection for wiring Device Address
-66	EB0I	Jumper connection for wiring Device Address
-67	EB01+	Jumper connection for wiring Device Address
-68	EB01-	Jumper connection for wiring Device Address
-69	EBlI	Jumper connection for wiring Device Address

PIN NO.	NAME	FUNCTION
P1-70	EB02+	Jumper connection for wiring Device Address
-71	EB02-	Jumper connection for wiring Device Address
-72	EB2I	Jumper connection for wiring Device Address
-73	Device Ready	Externally supplied timing for BIC-connected operations
-74	Not used	
-75	Not used	
-76	Enable	Not used
-77	EXC2-N	Jumper connection for EXC2 signal assigned to DAC 1
-78	EXC2-M	Jumper connection for EXC2 signal assigned to DAC 2
-79	EPO-N	DAC Select signal for BIC-connected operations
-80	Not used	
-81	Not used	
-82	Not used	
-83	Not used	
-84	Not used	
-85	DTOS	Data transfer request to computer
-86	EXC7	Jumper connection for internal use of EXC7
-87	EXC5	Jumper connection for internal use of EXC5
-88	Not used	
-89	Not used	
-90	EXC6	Jumper connection for internal use of EXC6
-91	EXC2	Jumper connection for internal use of EXC2
-92	Not used	
-93	EXC3	Jumper connection for internal use of EXC3
-94	EXC4	Jumper connection for internal use of EXC4
-95	Not used	
-96	Not used	
-97	Not used	
-98	EXC1	Jumper connection for internal use of EXC1

PIN NO.	NAME	FUNCTION
P1-99	Not used	
-100	Digital ground	
-101	EXC0	Jumper connection for internal use of EXC0
-102	Enable	Jumper connection for Enable signal to slave DACs
-103	EXC2-3	Jumper connection for DAC Select line 3
-104	EXC2-4	Jumper connection for DAC Select line 4
-105	EXC2-5	Jumper connection for DAC Select line 5
-106	EXC2-6	Jumper connection for DAC Select line 6
-107	Not used	
-108	EXC2-7	Jumper connection for DAC Select line 7
-109	Not used	
-110	EXC2-0	Jumper connection for DAC Select line 0
-111		Jumper connection for +15 Vdc source
-112	EXC2-1	Jumper connection for DAC Select line 1
-113		Jumper connection for -15 Vdc source
-114	EXC2-2	Jumper connection for DAC Select line 2
-115		Jumper connection for -15 Vdc ground
-116	Not used	
-117	Not used	
-118	+5 Vdc	+5 Vdc
-119	Not used	
-120	Not used	
-121	+5 Vdc	+5 Vdc
-122	Digital ground	

TERMINAL EDGE CONNECTOR WIRING

PIN NO.	NAME	FUNCTION
J1-1	Not used	
-2		Jumper connection to +5 Vdc supply
-3	REX5	Jumper connection for EXC5 reset
-4	Not used	
-5	REX4	Jumper connection for EXC4 reset
-6	Not used	
-7	REX1	Jumper connection for EXC1 reset
-8	Not used	
-9	REX0	Jumper connection for EXC0 reset
-10	Not used	
-11	REX7	Jumper connection for EXC7 reset

PIN NO.	NAME	FUNCTION
J1-12	Not used	
-13	REX6	Jumper connection for EXC6 reset
-14	EXC-7	Output connection for EXC7
-15	REX2	Jumper connection for EXC2 reset
-16	EXC6	Output connection for EXC6
-17	REX3	Jumper connection for EXC3 reset
-18	EXC5	Output connection for EXC5
-19		Jumper connection for DAC1 buffer clock
-20	EXC4	Output connection for EXC4
-21		Jumper connection for DAC2 buffer clock
-22	EXC3	Output connection for EXC3
-23	Device Ready	Externally supplied timing for BIC-connected operations
-24	EXC2	Output connection for EXC2
-25	Not used	
-26	EXC1	Output connection for EXC1
-27	Not used	
-28	EXC0	Output connection for EXC0
-29	Sense 7	Input connection for Sense 7 line
-30		Jumper connection to digital ground
-31	Sense 6	Input connection for Sense 6 line
-32		Jumper connection to digital ground
-33	Sense 5	Input connection for Sense 5 line
-34		Jumper connection to digital ground
-35	Sense 4	Input connection for Sense 4 line
-36		Jumper connection to digital ground
-37	Sense 3	Input connection for Sense 3 line
-38		Jumper connection to digital ground
-39	Sense 2	Input connection for Sense 2 line
-40		Jumper connection to digital ground
-41	Sense 1	Input connection for Sense 1 line
-42		Jumper connection to digital ground
-43	Sense 0	Input connection for Sense 0 line
-44		Jumper connection to digital ground
J2-1		DAC1 analog output signal
-43		DAC2 analog output signal

APPENDIX B: SPECIFICATIONS

Accuracy

± 0.003% of 20 V full scale (14-bit option)

± 0.012% of 20 V full scale (12-bit option)

± 0.05% of 20 V full scale (10-bit option)

Temperature Coefficient

±0.1 LSB/°C (0 °C to 50 °C)

Warm Up Time

Essentially 0; however allow 15 minutes for best results.

Slew Rate

4 volts/microsecond

Settling Time

20 microseconds to stated accuracy

Adjustments

Full scale and zero (10-bit option)

Full scale, zero, and MSB (12-bit option)

Full scale, zero, and 3 MSB (14-bit option)

Output Voltage Range

± 10 V full scale

Output Current Range

10 ma

(40 ma option available)

Switching Transient

200 mV peak, maximum duration less than 5 microseconds.

Capacitive Load

200 pF at specified settling time.

Short Circuit Protection

DAC outputs may be shorted to ground indefinitely without damage.

Output Noise

Less than $\pm$ 1/2 LSB maximum due to activity on computer E-bus or other DACs.

Digital Control Outputs

Number: Eight.

Type: Open Collector Transistor. TI SN75451P Dual Peripheral Driver sinks current when true. Each output will sink 300 mA when and standoff +30 volts. Outputs are controlled by flip-flops which are set by computer instructions and are reset externally. (See manufacturer's specifications for further details.)

Digital Sense Inputs

Number: Eight

Type: TTL logic levels. Ground true, open circuit inputs are held to +5 volt supply through 5.6 K ohm resistors.

Power

+15 Vdc ±0.1%, 90 mA

-15 Vdc ±3%, 90 mA

+5 Vdc ±1%, 850 mA

Temperature Range

Specification: 0°C to 50°C

Operating: -10°C to 70°C

Storage: -55°C to 85°C

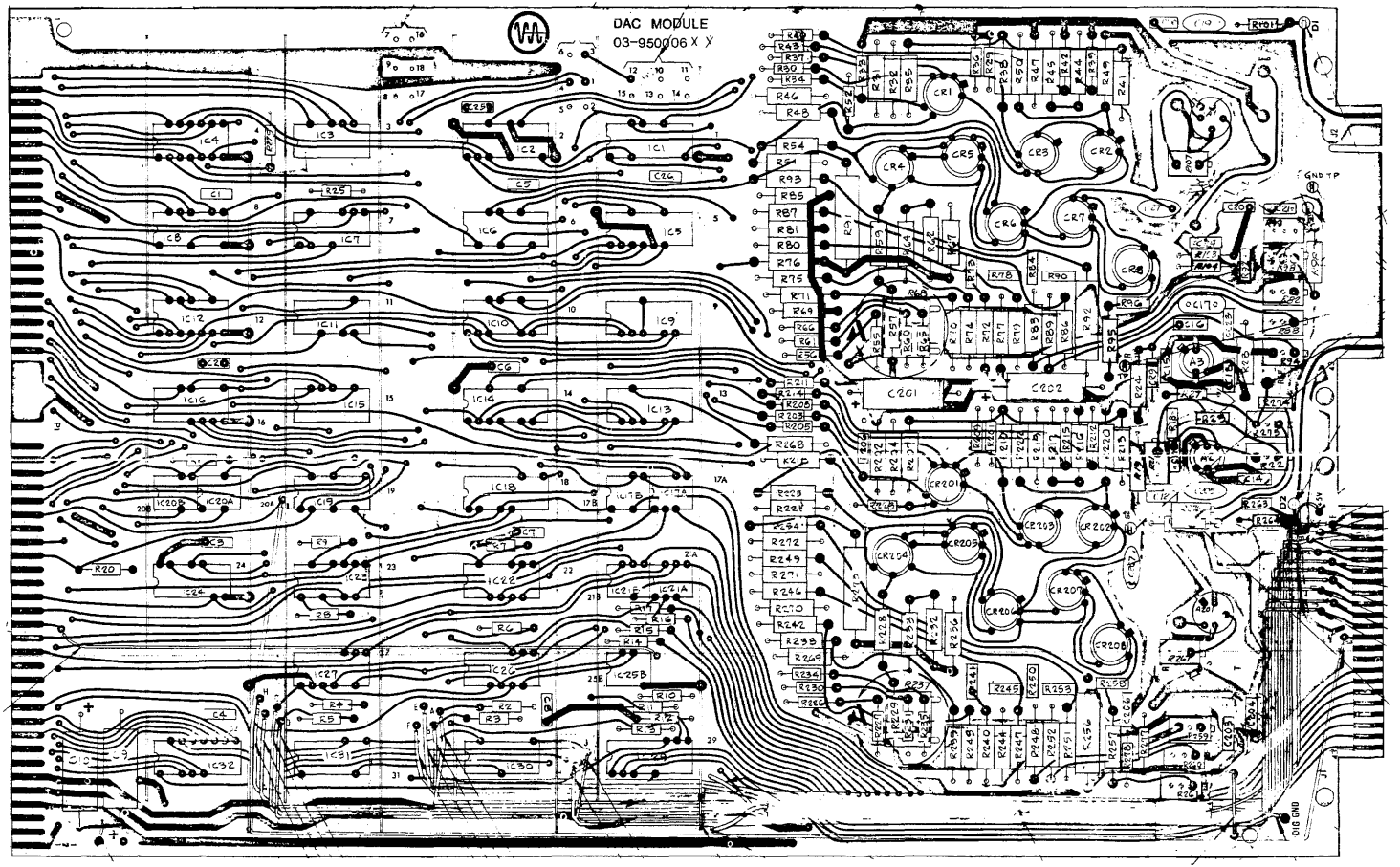
Physical Characteristics

Dimensions: One printed circuit board 7-3/4 x 12 x 1/2 inches.

Connectors: One 122-terminal card edge connector. Two 44-terminal card edge connectors.

APPENDIX C:
SCHEMATIC, ASSEMBLIES, AND PARTS LIST

DAC Module 03-950004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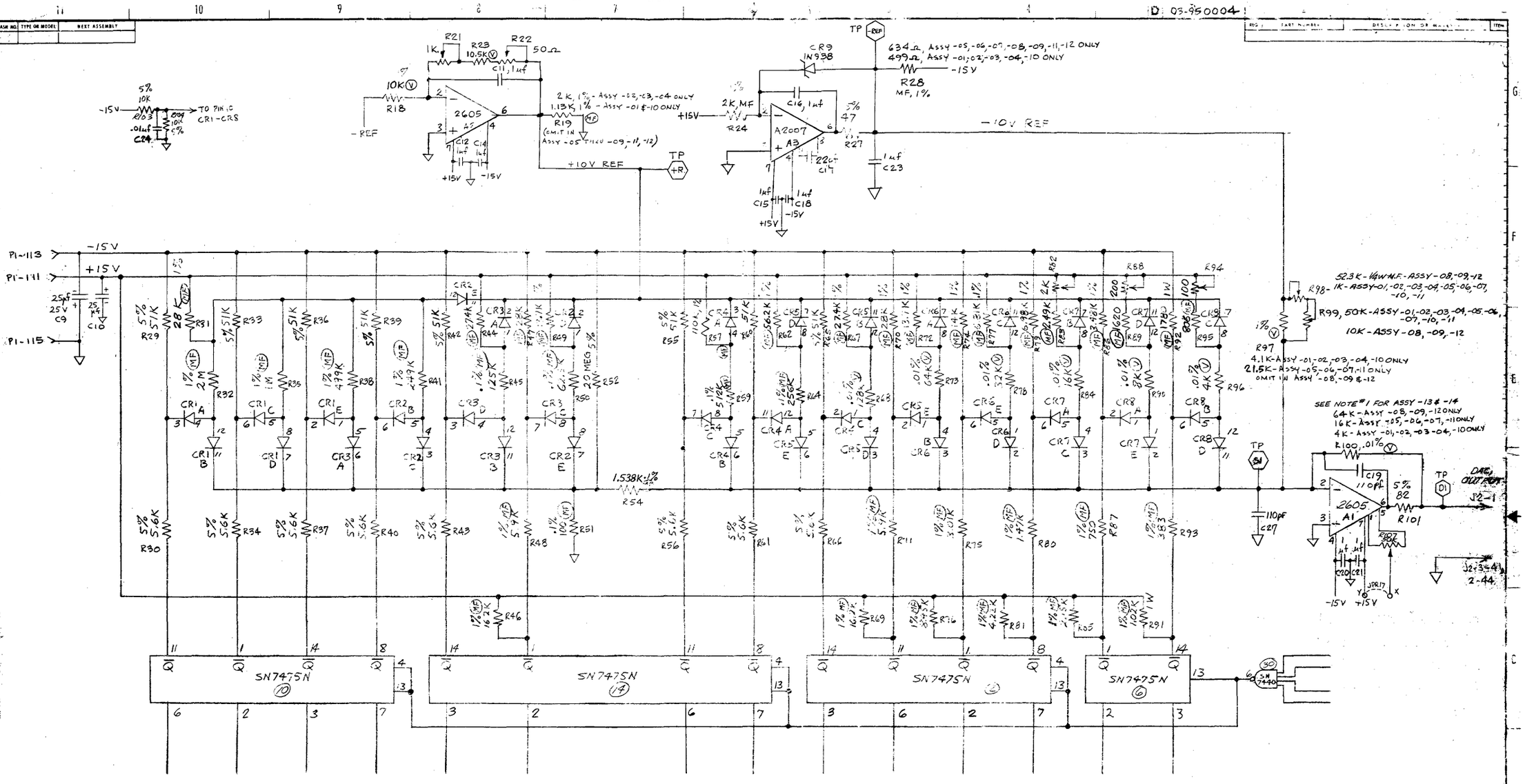
03-950006 X X
GND TP
DIG GND

D 03-950004



DO NOT SCALE DRAWING

1, A1 & A201 AMPLIFIER CIRCUITS FOR ASSY 03-950006-13 & -14
SEE SCHEMATIC DWG NO. 03-950724

NOTES:

DRAWN	DATE	APPROVED	DATE	CODE
CHECKED	DATE	APPROVED	DATE	CLASS
	12/15/70			A

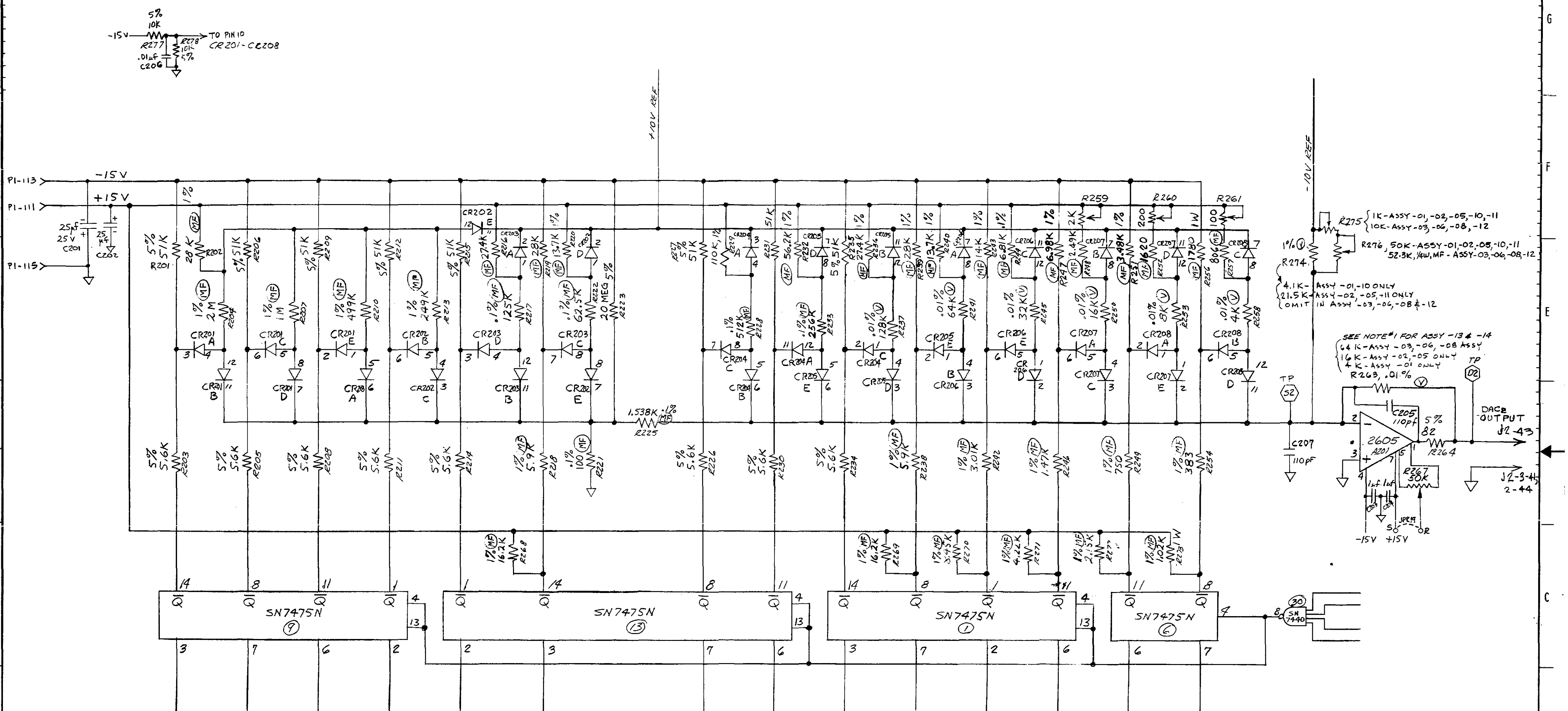
DAC 1

NOT OTHERWISE SPEC: FRAC ± | ANG ± | SCALE

FIN. √ DEC X ± | XX ± | XXX ±

DIVISION GDS | SIZE D | DRAWING NO. 03-950004 | REV R

SHT 1 OF 3



DO NOT SCALE DRAWING

SEE SHT 1 OF 3

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CHECKED Jim Day	DATE 12/15/70	APPROVED	DATE

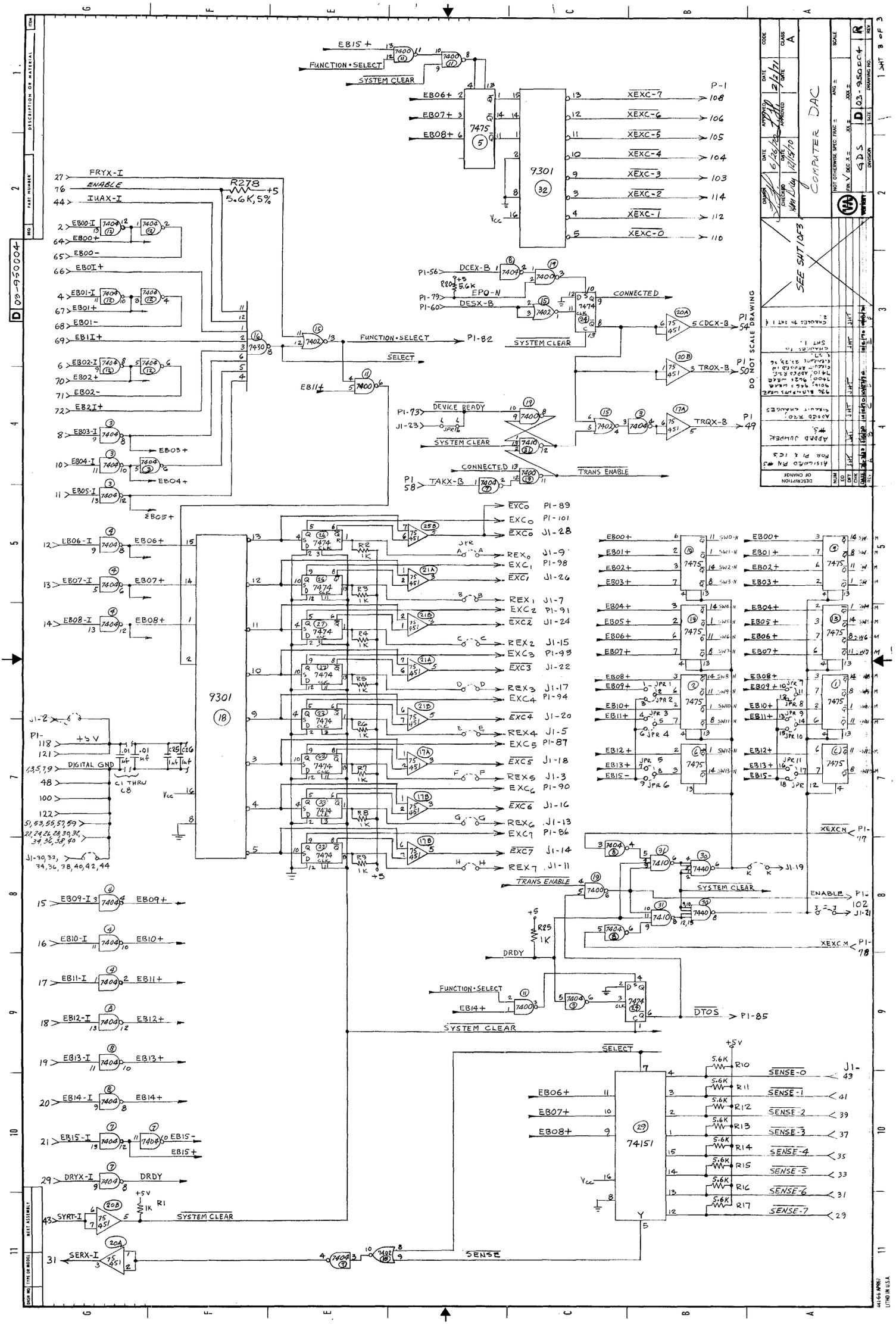
CLASS A

DAC 2

varian

GDS — D — 03-950004 — REV

SHT 2 of 3


COMPUTER DAC
SEE SHT 1 OF 3
DO NOT SCALE DRAWING
9301
74151
7475
7474
7430
7402
7400
7404
7410
7440
75451
FUNCTION • SELECT
SYSTEM CLEAR
ENABLE
SELECT
DRDY
TRANS ENABLE
DEVICE READY
CONNECTED
DTOS
SENSE
R278 5.6K,5%
XEXC-7
XEXC-6
XEXC-5
XEXC-4
XEXC-3
XEXC-2
XEXC-1
XEXC-0
CDCX-B
TROX-B
TRQX-B
TAKX-B
DCEX-B
EPO-N
DESX-B
SYRT-I
SERX-I
FRYX-I
IUAX-I
SENSE-0
SENSE-1
SENSE-2
SENSE-3
SENSE-4
SENSE-5
SENSE-6
SENSE-7

DAC MODULE ASSEMBLY, 03-950006

Schematic Reference	Description	Varian Part No.
IC1,2,5,6,9,10, 13,14	IC Element 7475N	62-600351
IC3,4,7,8,12	IC Element 7404N	62-600013
IC11,19	IC Element 7400	62-600355
IC15	IC Element 7402N	62-600356
IC16	IC Element 7430N	62-600359
IC17A,17N,20A, 21A,21B,25B	IC Element 75451P	62-600260
IC18,32	IC Element 9301	62-600400
IC22,23,24,26,27	IC Element 7474N	62-600365
IC29	IC Element 74151N	62-600270
IC 30	IC Element 7440N	62-600310
IC31	IC Element 7410	62-600357
A1,A201,A2	Amplifier, 2605	62-600203
CR1- ,CR201-208	Diode Array, CA 3039	62-600091
CR9	Diode IN 938	66-300938
R1-9,R25	Res, FXD Comp, 1K, 1/4W 5%	32-301410
R-10-17,20,30,34 37,40,43,56,61,66 279,203,205,208, 211,214,226,230, 234	Res, FXD Comp, 5.6K 1/4W, 5%	32-301456
R27	Res, FXD Comp, 47Ω ¼W 5%	32-301247
R29,33,36,39,42 55,60,65,201,206 209,212,215,227, 231,235	Res, FXD Comp, 51K ¼W 5%	32-301551
R52,R223	Res, FXD Comp, 1K, ¼W 5%	32-301820
R101,R264	Res, FXD Comp, 82Ω ¼W 5%	32-301282
R103,R104,277,278	Res, FXD Comp, 10K, ¼W, 5%	32-301510
R19	Res, MF, 1.13K, ¼W, 1%	31-224113
R19,24	Res, MF 1.13K, ¼W, 1%	31-224200
R28	Res, MF 499Ω, ¼W, 1%	31-223499

Schematic Reference	Description		Varian Part No.
R28	Res, MF	634Ω ¼W 1%	31-223634
R31,47,70	Res, MF	28K ¼W 1%	31-225280
R202,219,239	Res, MF	28K ¼W 1%	31-225280
R32	Res, MF	2M ¼W 1%	31-607200
R204	Res,MF	2M ¼W 1%	31-607200
R35	Res, MF	1M ¼W 1%	31-227100
R207	Res, MF	1M ¼W, 1%	31-227100
R38	Res, MF	499K, ¼W, 1%	31-226499
R210	Res, MF	499K, ¼W, 1%	31-226499
R41	Res, MF	249K, ¼W, L%	31-226249
R213	Res, MF	249K, ¼W, 1%	31-226249
R44	Res, MF	274K, ¼W, 1%	31-225274
R67,216,236	Res, MF	274K, ¼W, 1%	31-225274
R46,R69	Res, MF	16.2K, ¼W, 1%	31-225162
R268,269	Res, MF	16.2K, ¼W, 1%	31-225162
R48,R71	Res, MF	5.9K, ¼W, 1%	31-224590
R218,238	Res, MF	5.9K, ¼W, 1%	31-224590
R49,R72	Res, MF	13.7K, ¼W, 1%	31-225137
R220,240	Res, MF	13.7K, ¼W, 1%	31-225137
R57	Res, MF	110K, ¼W, 1%	31-226110
R229	Res, MF	110K, ¼W, 1%	31-226110
R62	Res, MF	56.2K, ¼W, 1%	31-225562
R232	Res, MF	56.2K, ¼W, 1%	31-225562
R74	Res, MF	14K, ¼W, 1%	31-225140
R243	Res, MF	14K, ¼W, 1%	31-225140
R75	Res, MF	3.01, ¼W, 1%	31-224301
R242	Res, MF	3.01, ¼W, 1%	31-224301
R76,R270	Res, MF	8.45, ¼W, 1%	31-224845
R79,R247	Res, MF	6.98K, ¼W, 1%	31-224698
R80,R246	Res, MF	1.47K, ¼W, 1%	31-224147
R81,R271	Res, MF	4.22K, ¼W, 1%	31-224422
R83,R248	Res, MF	2.49K, ¼W, 1%	31-224249
R85,R272	Res, MF, 2.15K, ¼W, 1%		31-224215

Schematic Reference	Description	Varian Part No.
R86, R251	Res, MF, 3.48, ¼W, 1%	31-224348
R87, R249	Res, MF, 750Ω, ¼W, 1%	31-223750
R89, R252	Res, MF, 1.62K, ¼W, 1%	31-224162
R93, R254	Res, MF, 383Ω, ¼W, 1%	31-223383
R95, R257	Res, MF, 806Ω, ¼W, 1%	31-223806
R276, R98	Res, MF, 52.3K, 1%, ¼W	31-225523
R18	Res, MF, 10K, 1%	31-239033
R23	Res, MF, 10.5K, 1%	31-239057
R68, R237	Res, MF, 128K, .01%	31-239114
R73, R100, R241, R263	Res, MF, 64K, .01%	31-239054
R78, R245	Res, MF, 32K, .01%	31-239053
R84, R100, R250 R263,	Res, MF, 16K, .01%	31-239052
R90. R253	Res, MF, 8K, .01%	31-239051
R96, 100, 258, 263	Res, MF, 4k, .01%	31-239050
R97, R274	Res, MF, 4.1K, 1%	31-239048
R97, R274	Res, MF, 21.5K, 1%	31-239060
R91, R273	Res, MF, 1.02K, 1W, 1%	31-464102
R92, R256	Res, MF, 1.78k, 1W, 1%	31-464178
R22	Res, VAR W.W., 50Ω	37-577308
R88, 260	Res, VAR W.W., 200Ω	37-577310
R82, R259	Res, VAR W.W., 2K	37-577312
R94, R261	Res, VAR W.W., 100Ω	37-577309
R98, R275, R21	Res, VAR W.W.., 1K	37-577311
R45, R217	Res, MF, 125K, ¼W, .01%	31-613328
R50, R222	Res, MF, 62.5K, ¼W, 01%	31-613341
R51, R221	Res, MF, 100Ω, ¼W, 01%	31-613308
R54, R225	Res, MF, 1.538K, ¼W, .01%	31-613338
R59, R228	Res, MF, 512K, ¼W, 01%	31-613339
R64, R233	Res, MF, 256K, ¼W, .01%	31-613340
R77, R244	Res, MF, 6.81K, ¼W, 0.1%	31-613342