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DWG NO

B. N. Posthill
 B. N. Posthill
 Vice President
 Engineering

D. E. Elder for L. E. T.
 L. E. Taylor
 Director
 Development

DR	J. De Muzio	10/30/70
CHK	<i>BTS</i>	12-15-70
DSGN	<i>Brickett</i>	11/9/70
ENGR	<i>W. Santoni</i>	11/13/70
APPD	<i>W. Santoni</i>	11/13/70
APPD	<i>J. Watson</i>	11/13/70



varian data machines / a varian subsidiary
 2722 michelson drive / irvine / california / 92664

TITLE

SOFTWARE PERFORMANCE SPECIFICATIONS
 620 PIM TEST PROGRAM

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SECTION 1: TEST PROGRAM OVERVIEW


1.1 INTRODUCTION

This document describes the priority interrupt module (PIM) test program. The PIM test allows the user to verify the correct operation of the PIM option. The test consists of four subtests. Each of the subtests executes a different sequence of PIM instructions and each of the subtests should be executed to perform the total test. The test will check the PIM option on any of the 620 series computers and is designed to run under the 620 Test Executive Program (See Software Product Specification number 89A0122).

The test is designed to check a single priority interrupt module at a time. The device address of the PIM and the origin of the memory interrupt addresses may be entered at run-time. (The memory interrupt address should lie between 0 and 0377.) After testing a module the test may be restarted and a new PIM device address and memory interrupt address entered. The interrupts may be set by using an interrupt simulator or by momentarily grounding the PIM interrupt lines (IL00-IL07). The descriptions of the individual subtests state when the interrupts should be set.

Subtest 1

The mask register is disabled, the PIM is enabled, and the test pauses to allow interrupts to be set. When the test is resumed, the program enters a five second idle loop and then prints the message 'NO INTERRUPTS' to indicate successful completion. Any message indicating interrupts occurred or failure of the 'NO INTERRUPTS' message to be typed, denotes an error. Interrupts may be set at any time during the interval from the request for interrupt message until the completion of the subtest.

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Subtest 2

The mask register is enabled for all interrupts, the line (interrupt) register is cleared, the PIM is enabled and the program requests the number of five second intervals to delay before completing the test. After this is entered, the program will type out the line number on which any interrupt occurs. If multiple interrupts are set, the line numbers should be typed in the proper priority order.

Subtest 3

The mask register is enabled for all interrupts, the PIM is disabled and the test pauses to allow interrupts to be set. When the test is resumed, the program enters a five second idle loop and then prints the message 'NO INTERRUPTS' to indicate successful completion. Any message indicating interrupts occurred, or failure of the 'NO INTERRUPTS' message to be typed, denotes an error. Interrupts may be set at any time during the interval from the request for interrupts message until the completion of the subtest.

Subtest 4

The mask register is enabled for all interrupts, the line (interrupt) register is cleared and the PIM is disabled, and the test pauses to allow interrupts to be set. When the test is resumed, the line (interrupt) register is cleared and the PIM enabled, and the program enters a five second idle loop and then prints the message 'NO INTERRUPTS' to indicate successful completion. Any messages indicating interrupts occurred, or the failure of the 'NO INTERRUPTS' message to be typed, denotes an error. Interrupts should only be set when the request for interrupts message is typed and before the test is resumed.



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Subtest 5*

The mask register is enabled for all interrupts, the line (interrupt) register is cleared, the PIM is enabled, the PIM Group disable is executed, and the test pauses to allow interrupts to be set. When the test is resumed, the program enters a five second idle loop and then prints the message 'NO INTERRUPTS' to indicate successful completion. Any message indicating interrupts occurred, or failure of the 'NO INTERRUPTS' message to be typed, denotes an error. Interrupts may be set at any time during the interval from the request for interrupts message until the completion of the subtest.

Subtest 6*

The mask register is enabled for all interrupts, the line (interrupt) register is cleared and the PIM is disabled, the PIM Group enable is executed, and the test pauses to allow interrupts to be set. When the test is resumed, the program enters a five second idle loop. After this is entered, the program will type out the line number on which any interrupt occurs. If multiple interrupts are set, the line numbers should be typed in the proper priority order.

*The group enable/disable is standard on Revision M, optional on prior revisions.



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1.2 HARDWARE SUMMARY

The minimum configuration of the PIM test is a 620 series computer with a minimum of 4K memory and one or more PIM modules.

The object program is normally supplied in the form of a punched paper tape to be loaded with the teletype reader or high speed paper tape reader. However, the object can be made available in object card or other formats.

The execution of the program is designed to take place with either a basic CPU only or a basic CPU and teletype. The selection is made by placing the program in the console mode or teletype mode.

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SECTION 2: EXTERNAL SPECIFICATION

2.1 GENERAL

The external specification provides all the operating procedures and information pertinent to user interface. The PIM test is normally loaded and executed via teletype keyboard commands from the user. The 620 Test Executive Program is the software interface for accomplishing these functions.

2.2 LOADING PROCEDURE

The 620 Test Executive (SPS number 89A0122) must be loaded before the Priority Interrupt Module Test Program will operate correctly. All of the teletype input/output subroutines are resident in the Test Executive and are called by the PIM test program.

2.2.1

Load the Test Executive, which includes the binary object tape loader, per the procedure outlined in the Test Executive external specifications (89A0122).

2.2.2

Press key L on the keyboard, followed by a period to command the Test Executive to load the tape. Refer to the Test Executive external specifications (89A0122) for details on loading test program.



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2.2.3

An alternate loading procedure can be used in the absence of a teletype. A direct CPU console interface with the Test Executive i.e. starts execution of the Test Executive at the loader module which loads the test program via the available object input device (card reader, mag tape, etc.).

2.3 OPERATING PROCEDURE

The execution of the test may be performed by the use of the teletype interface or by direct CPU console interface (in the absence of a teletype).

For systems that do not contain a teletype unit, test programs will be loaded via the available object input device (card reader, mag tape, etc.). In this mode of operation (console mode), any required run-time parameters will be inserted into the CPU register and error information or event reporting will be displayed thru program halts and CPU register contents.

The operator has the ability to return to the beginning of the test by toggling sense switch 3. The test program may also be manually restarted at location 0500.

2.3.1 TELETYPE MODE OF OPERATION

The PIM test starts out by identifying itself and requesting information about the teletype interrupts. If the system has no teletype interrupts or the interrupts are to be tested, respond with 0. Otherwise, respond with the PIM device address, the read ready interrupt trap, and the write ready interrupt trap, separated by commas and terminated with a period. The program then requests the device address of the PIM module to be tested. The user enters the device address followed by a period. The program then requests the origin of the 16-word block of trap locations associated with the PIM module to be tested. The user enters the address followed by a period. The program then requests the subtest to be run. The user enters the subtest number followed by a period. For subtests 1, 3, 4, 5, and 6 the program will request that interrupts are set. After the interrupts are set, the user presses the teletype space bar to resume execution of the program. For subtest 2 the program will request the number of 5 second intervals to delay before terminating the test. The user enters the number of intervals followed by a period. If 0 intervals are entered, the test will run indefinitely and must be terminated with sense switch 3. Termination of each subtest is indicated by the request for a new subtest number.



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The following example shows teletype input/output messages generated during the test and includes some pertinent comments. Those messages which are underscored are typed by the user.

In this example the interrupt simulator was used. The results are indicative of a correctly functioning PIM module.

THIS IS THE 620 TEST EXECUTIVE
MEMORY SIZE IS 8K

L.
PIM TEST
TTY INTERRUPTS? 0.
ENTER PIM DEVICE ADDRESS 41.

ENTER ORIGIN OF TRAP ADDRESSES 140.

ENTER SUBTEST NUMBER 1.
SET INTERRUPTS
NO INTERRUPTS

ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 1.
12345678

ENTER SUBTEST NUMBER 3.
SET INTERRUPTS
NO INTERRUPTS

ENTER SUBTEST NUMBER 4.
SET INTERRUPTS
NO INTERRUPTS

ENTER SUBTEST NUMBER
PIM TEST

ENTER PIM DEVICE ADDRESS 42.

ENTER ORIGIN OF TRAP ADDRESSES 160.



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The PIM test was loaded under control of the 620 Test Executive, identified itself and requested the PIM device address of the module to be tested.

The PIM device address and the origin of the 16-word block of trap addresses associated with the module to be tested was entered.

After the SET INTERRUPT message was typed, interrupts were raised on all the interrupt lines; then the teletype space bar was pressed to proceed with the test.

After the ENTER NUMBER OF 5 SECOND INTERVALS message was typed, interrupts were raised on all the interrupt lines; then the number of delay intervals was entered.

After the four tests had been executed, sense switch 3 was set to return control to the start of the program. At this point the device address and trap address of a new module to be tested can be entered. (When done testing a module or when testing is completed, always return to the start of the program via sense switch 3 so that certain locations in the trap area will be restored to their original contents.)

The 5 second interval pertains to the 620/i. The interval on the 620/F is approximately 2 seconds.

Sense Switch Option

<u>Switch</u>	<u>Set</u>	<u>Reset</u>
SS1	Suppress error printout	Print error message
SS2	Halt on error	Do not halt on error
SS3	Terminate test and return to beginning of PIM test	Continue test



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2.3.2 COMPUTER CONSOLE MODE OF OPERATION

If a teletype is not available or is inoperative, the PIM test may be executed by using the following procedure.

Load the program from the CPU console using the manual loading procedure outlined in the Test Executive external specification (89A0122).

In the console mode, when the program is loaded, or started at location 0500, it will halt with 01 in the instruction register and the A, B and X registers cleared. At this point set the A register (bits 0 through 5) = the PIM device address and the B register (bits 0 through 7) = the origin of the interrupt addresses.

Press the RUN(START) button.

The program will halt with 02 in the instruction register. Set the A register = the subtest number to be executed and, if subtest 2 is to be executed, set the B register = the number of delay intervals. (All ones indicate continuous running of test 2.)

Press the RUN (START) button.

The program will run thru the subtest, halting at times to display pertinent information (see section 2.4.2) and returning to the 02 halt to allow a new subtest to be selected. To test a new module, or when done testing, branch to PTER to restore certain trap locations. (The location of PTER may be obtained from the program listing.)

Sense Switch Option

<u>Switch</u>	<u>Set</u>	<u>Reset</u>
SS2	Halt on error	Do not halt on error
SS3	Terminate test and return to beginning of PIM test	Continue test



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2.4 MESSAGES AND PROGRAM HALTS

2.4.1 MESSAGES

The following messages are informative messages only and require no response on the part of the user.

PIM TEST

The PIM test identifies itself.

NO INTERRUPTS

If at the end of a subtest the interrupt flag is reset (indicating no interrupts were detected) this message is printed.

INVALID INTERRUPT

If an interrupt occurs which traps to a location outside the 16-word interrupt block associated with the module being tested, this message is printed. This message may be suppressed by sense switch 1.

XXX...X

In subtest 2 the line number associated with each interrupt is typed as it occurs.

The following messages require some response from the user.

ENTER PIM DEVICE ADDRESS

The PIM device address is entered, followed by a period (see section 2.3.1 for example).

ENTER ORIGIN OF TRAP ADDRESSES

The origin of the 16-word interrupt block associated with the module being tested is entered, followed by a period.

ENTER SUBTEST NUMBER

The number of the subtest to be executed is entered, followed by a period.

TTY INTERRUPTS

The PIM Device Address, the Read Ready Interrupt Trap, and the Write Ready Interrupt Trap, Separated by commas and terminated with a period, or 0.



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SET INTERRUPT

The user may set the interrupts and press the space bar on the teletype to continue execution of the program.

2.4.2 PROGRAM HALTS

There are several HALTS in the program and they are defined below. Unless stated otherwise, they pertain only to the console mode of operation.

<u>HALT</u>	<u>Meaning</u>
01	The PIM device address is entered in the A register and the origin of the interrupt addresses is entered in the B register.
02	The number of the subtest is entered in the A register and, if subtest 2 is to be executed, the number of delay intervals is entered in the B register.
03	The program halts to allow the user to set the interrupts.
04	This halt may occur in both console and teletype mode. It indicates an invalid interrupt occurred.
05	This halt occurs at the end of a subtest. If the A register is zero, no interrupts were detected during the subtest.
06	This halt occurs when an interrupt is detected at one of the specified trap locations. The A register displays the interrupt line number.



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SECTION 3: INTERNAL SPECIFICATION

3.1 INTRODUCTION

The Priority Interrupt Mode Test consists of four subtests, each of which tests a logical feature of the Priority Interrupt Module option. The test allows the PIM device address and associated block of interrupt locations to be selected at run-time so that a single version of the test will suffice for all PIM device address/interrupt location combinations.

The 620 Test Executive must be loaded before the Priority Interrupt Module Test can be run. The test makes use of Test Executive subroutines for teletype input/output, sense switch testing, etc. The PIM test program does not overlay any part of the Test Executive, however, the transfer vectors for the power fail routines are saved, and if the PIM test is properly terminated, restored.

3.1.1 Memory Map

<u>Location</u>	<u>Description</u>
0000 - 0377	Interrupt Locations
0400 - 0477	Test Executive Tables
0500 - 0501	Entry to PIM Test
0504 - 0517	Indirect Pointers Table
0520 - 0577	Literal Table
0600 - 2111	PIM Test
05100 - 07547	Test Executive Routines

3.2 INTERNAL DESCRIPTION

Subroutine names in parenthesis indicate the subroutine is part of the 620 Test Executive.



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Title: Priority Interrupt Module Test

Symbolic Name: PIMT

Purpose: To identify the test, acquire a PIM device address and interrupt trap address, select a subtest for execution, and terminate the subtest.

Description: The test identifies itself; then requests the PIM device address and the origin of the trap locations for the module to be tested. It adds the device address to the PIM I/O instructions and builds transfer vectors to the interrupt routines in the proper memory locations. It then requests the subtest to be executed. After the subtest is initiated, control is returned to PIMT for a delay interval. At its conclusion, the subtest is terminated, the 'NO INTERRUPTS' message is output if appropriate, and another request for a subtest is made. Toggling sense switch 3 will return control to the start of the program so that new device address and trap location information may be entered. The routine contain several halts for entering or displaying data in the console mode.

Entry Points: PIMT

Calling Sequence: PIMT may be entered thru the transfer vector at location 0500 and directly at location 0600. If the test is to be executed in console mode, the program will halt at PIMI to allow the PIM device address and trap locations to be selected.

Entrance Parameters: Not applicable

Exit Point: PIMT gives up control to each of the subtests; to PIAA if subtest 1 is selected, to PIBA if subtest 2 is selected, to PICA if subtest 3 is selected, and to PIDA if subtest 4 is selected. Each of the subtests return control to PIMT at PIAE for monitoring of subtest execution.

Exit Parameters: Not applicable

Tables or Files Modified or Read: Not applicable



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Tables or Files Created: Not applicable

Called By: Normally entered from 620 Test Executive

Called From: (OUTC), (OUTD), (INPG), (TDLY), (SSWT), PLOW, PMOD, POVL

Exception Conditions: If the interrupt flag remain reset at the completion of the subtest, the 'NO INTERRUPTS' message is typed.

Timing: Not applicable


Size: 172 words

Comments: PIMT contain several program halts for entering run-time parameter or for displaying information during execution if the test is run in the console mode. See section 2.4.2 for a description of program halts 01, 02, and 05.

Special Notation: Not applicable

Hardware Details: Not applicable

Flowcharts: See Section 3.2.1.

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Title: Subtest 1

Symbolic Name: PIAA

Purpose: To verify disabled mask register will inhibit interrupts on an enabled PIM.

Description: All lines in the mask register are disabled and the PIM is enabled. A request is made to the user to set the interrupts. When the user responds, control is returned to PIMT for the delay interval. No interrupts should occur.

Entry Points: PIAA

Calling Sequence: Receives control from PIMT

Entrance Parameters: Not applicable

Exit Point: PIAA exits to PIMT at symbolic PIAD after requesting that interrupts be set.

Exit Parameters: Not applicable

Tables or Files Modified or Read: Not applicable

Tables or Files Created: Not applicable

Called By: Entered from PIMT

Called From: PIO

Exception Conditions: Not applicable

Timing: Not applicable

Size: 7 words



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Comments: Not applicable
Special Notations: Not applicable
Hardware Details: Not applicable
Flowcharts: See section 3.2.1



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Title: Subtest 2

Symbolic Name: PIBA

Purpose: To verify the PIM can be enabled, and that interrupt traps occur at the correct location.

Description: The interrupt register is cleared, all lines in the mask register are enabled, and the PIM is disabled. The user is requested to enter the length of the delay interval and when the user responds, the PIM is enabled and control is returned to PIMT for the delay interval. [The user may raise interrupts during this interval. Their occurrence will be reported by interrupt level routines.]

Entry Points: PIBA

Calling Sequence: Receives control from PIMT.

Entrance Parameters: Not applicable

Exit Point: PIBA normally exits to PIMT at PIAD for execution of the subtest, however, if the test is aborted by the use of sense switch 3 in the INPG routine, control is returned to the top of PIMT.

Exit Parameters: Not applicable

Tables or Files Modified or Read: Not applicable

Tables or Files Created: Not applicable

Called By: Receives control from PIMT

Called From: (OUTD), (OUTC), (INPG)

Exception Conditions: Previously mention use of sense switch 3.

Timing: Not applicable



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Size: 30 words

Comments: If the test is run in the console mode, the routine will bypass the teletype routine and just execute the PIM instructions.

Special Notation: Not applicable

Hardware Details: The PIM instructions to enable the mask register, clear outstanding interrupts and enable the PIM are executed in this routine.

Flowcharts: See section 3.2.1



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Title: Subtest 3
Symbolic Name: PICA
Purpose: To verify the PIM can be disabled when the mask register is enabled.
Description: All lines in the mask register are enabled and the PIM is disabled. A request is made to the user to set the interrupts. When the user responds, control is returned to PIMT for the delay interval. No interrupts should occur.
Entry Points: PICA
Calling Sequence: Receives control from PIMT
Entrance Parameters: Not applicable
Exit Point: PICA exits to PIAC to request that interrupts be set.
Exit Parameters: Not applicable
Tables or Files Modified or Read: Not applicable
Tables or Files Created: Not applicable
Called By: Receives control from PIMT
Called From: Not applicable
Exception Conditions: Not applicable
Timing: Not applicable
Size: 5 words
Comments: Not applicable

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Title: Subtest 5

Symbolic Name: PIEA

Purpose: To verify the PIM can be disabled with the PIM Group Disable.

Description: All lines in the Nask Register are enabled, the Interrupt Register is cleared and the PIM enabled (Exc 03XX), and the 620-16 disabled (Exc 0444). A request is made to the user to set the interrupts when the user responds, control is returned to PIMT for decay interval. No interrupts should occur.

Entry Points: PIEA

Calling Sequence: Receives Control From PIMT



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Table or Files Modified or Read: None

Tables or Files Created: None

Called By: RIONE

Called From: PIMT

Exception Conditions: None

Timing: N/A

Size: Six Words

Comments: None

Special Notation: None

Hardware Details: The PIM must have the Group Enable/Disable

Flowcharts: See Section 3.2.1



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Title: Subtest 6

Symbolic Name: PILA

Purpose: To verify the PIM can be Enabled with the PIM Group Enable

Description: All lines in the Nask Register are Enabled, the Interrupt Register is cleared and the PIM Disabled (EXC 05XX) and the 620-16 Enabled (EXC 0244). A request is made to the user to set the Interrupts When the user responds, control is returned to PIMT for Decay Interval. Interrupts should occur.

Entry Points: PIFA

Calling Sequence: Receives Control From PIMT



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Table or Files Modified or Read: None

Tables or Files Created: None

Called By: None

Called From: PIMT

Exception Conditions: None

Timing: N/A

Size: 29 Words

Comments: None

Special Notation: None

Hardware Details: The PIM must have the Group Enable/Disable

Flowcharts: See Section 3.2.1



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Special Notation: Not applicable

Hardware Details: The PIM instruction to disable the PIM is given here.

Flowcharts: See section 3.2.1

Title: Subtest 4

Symbolic Name: PIDA

Purpose: To verify the clear interrupt register instruction clears outstanding interrupts.

Description: All lines in the mask register are enabled, and the interrupt register is cleared and the PIM disabled (EXC 05XX). A request is then made to the user to set the interrupts. When the user responds, an EXC 03XX is executed which clears the interrupt register (clearing outstanding interrupts) and enables the PIM. Control is returned to PIMT for the delay interval. No interrupts should occur.

Entry Points: PIDA


Calling Sequence: Receives control from PIMT

Entrance Parameters: Not applicable

Exit Point: PIDA returns control to PIMT at PIAD for the delay interval.

Exit Parameters: Not applicable

Tables or Files Modified or Read: Not applicable

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Tables or Files Created: Not applicable

Called By: Receives control from PIMT

Called From: PIO

Exception Conditions: Test can be terminated in PIO subroutine.

Timing: Not applicable

Size: 8 words

Comments: Not applicable

Special Notation: Not applicable

Hardware Details: The PIM instructions to enable the mask register, clear the interrupt register and enable the PIM module is given here.

Flowcharts: See section 3.2.1

Title: Interrupt routine

Symbolic Name: PIN(N)

Purpose: To report the occurrence of interrupts on one of the interrupt lines being tested.

Description: There are eight of these interrupt level routines, one for each interrupt line in the module being tested. Each routine saves the registers, types the interrupt line number, restores the registers, increments the interrupt flag, enables the PIM, and returns to the point of interrupt.



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Entry points: PIN(N) where N = 1,2,..8; one for each interrupt line in the module under test.

Calling sequence: Routine is entered, when a priority interrupt occurs on its associated line, via a jump and mark-instruction in its corresponding trap location.

Entrance Parameters: The A, B, and X register contents are saved upon entering routine.

Exit Point: The routine returns control to the interrupted routine via the P-register setting at time of interrupt.

Exit Parameters: The A, B and X contents are restored before exiting.

Table or Files Modified or Read: Not applicable

Table or Files Created: Not applicable

Called By: Not applicable

Called From: PSAV, PRES, TT20

Exception Conditions: Not applicable

Timing: Not applicable

Size: 96 words (12 words per interrupt line)

Comments: A table of transfer vectors to these interrupt routines are put in the proper trap locations at run-time by POVL.

Special Notation: Not applicable

Hardware Details: These routines re-enable the PIM after interrupt.

Flowcharts: See section 3.2.1



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Title: Save lower memory
Symbolic Name: PLOW
Purpose: To save the power fail/restart transfer vectors.
Description: The contents on locations 01, 041, and 043 are saved so that the interrupt area (0-0377) may be overlaid.
Entry Points: PLOW
Calling Sequence: CALL PLOW
RETURN
Entrance Parameters: Not applicable
Exit Point: Return is via the P-register contents saved at PLOW.
Exit Parameters: Not applicable
Tables or Files Modified or Read: Not applicable
Tables or File Created: Not applicable
Called By: PIMT
Called From: Not applicable
Exception Conditions: Not applicable
Timing: Not applicable
Size: 9 words
Comments: The transfer vectors saved are restored by terminating the test using sense switch 3 when a subtest number is requested.



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Special Notation: Not applicable

Hardware Details: Not applicable

Flowcharts: See section 3.2.1

Title: Overlay

Symbolic Name: POVL

Purpose: To overlay the interrupt area with transfer vectors.

Description: The interrupt area (000-0377) is filled with jump and mark instructions to a routine which reports spurious interrupts. A table of jump and mark instructions to the valid interrupt routines is then moved to the 16-word interrupt block associated with the module being tested.

Entry Points: POVL

Calling Sequence: CALL POVL
RETURN

Entrance Parameters: Not applicable

Exit Point: Return is via the P-register contents saved at POVL.

Exit Parameters: Not applicable

Tables or Files Modified or Read: The table of transfer vectors (PTAB) to the interrupt routines is move to the appropriate trap locations. PTAB is created at assembly time.



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Table or Files Created: Not applicable

Called By: PIMT

Called From: Not applicable

Exception Conditions: Not applicable

Timing: Not applicable

Size: 24 words

Comments: The origin of the trap locations for the module to be tested, obtained during the PIMT initialization dialogue, is saved in PADR.

Special Natation: Not applicable

Hardware Details: Not applicable

Flowcharts: See section 3.2.1

Title: Modify I/O

Symbolic Name: PMOD

Purpose: To add the current PIM device address to all PIM I/O instructions.

Description: The routine, using a table of pointers to PIM I/O instructions (PPOP), retrieves each instruction, modifies its device address field, and restores it.

Entry Points: PMOD



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Calling Sequence: CALL PMOD
 RETURN

Entrance Parameters: Not applicable

Exit Point: Return is via the P-register contents saved at PMOD

Exit Parameters: Not applicable

Tables or Files Modified or Read: The table of pointers to PIM I/O instructions (PPOP) is read by this routine. PPOP is created at assembly time.

Table or Files Created: Not applicable

Called By: PIMT

Called From: Not applicable

Exception Conditions: Not applicable

Timing: Not applicable


Size: 12 words

Comments: Not applicable

Special Notation: Not applicable

Hardware Details: Not applicable

Flowcharts: See Section 3.2.1

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Title: Print Line Number
Symbolic Name: TT20
Purpose: To print the line number of the current interrupt.
Description: The line number of the current interrupt is typed and the character count is incremented. When 70 characters have been typed, a carriage return and line feed is typed and the character count zeroed.
Entry Points: TT20
Calling Sequence: CALL TT20
RETURN
Entrance Parameters: The A register contains the line number, in ASCII, right-justified, on which the interrupt occurred.
Exit Point: Return is via the P-register contents saved at TT20.
Exit Parameters: Not applicable
Tables or Files Modified or Read: Not applicable
Tables or Files Created: Not applicable
Called by: PIN(N)
Called From: (OUTA), (OUTC)
Exception Conditions: Not applicable
Timing: Not applicable
Size: 23 words
Comments: If the program is running in console mode, the line number will be displayed in the A register at program halt 06. (See section 2.4.2)



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Special Notation: Not applicable
Hardware Details: Not applicable
Flowcharts: See Section 3.2.1

Title: Request Interrupts
Symbolic Name: PIO
Purpose: To notify the user that interrupts may now be set.
Description: The delay interval count is set to one and the message 'SET INTERRUPTS' is typed. When the user responds by hitting the teletype space bar (or any other character) the test continues.
Entry Points: PIO
Calling Sequence: CALL PIO
RETURN
Entrance Parameters: Not applicable
Exit Point: The normal return is via the P-register contents saved at PIO, however, the test may be terminated and control returned to the top of PIMT by toggling sense switch 3 at the request for input.



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Exit Parameters: Not applicable

Tables or Files Modified or Read: Not applicable

Tables or Files Created: Not applicable

Called by: PIAA, PIDA

Called From: (OUTC), (OUTD), (INDP)

Exception Conditions: Not applicable

Timing: Not applicable

Size: 20 words

Comments: If the program is running in the console mode, program halt 03 will allow the user to set interrupts.

Special Notation: Not applicable

Hardware Details: Not applicable

Flowcharts: See Section 3.2.1

Title: Spurious Interrupt

Symbolic Name: PINX



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Purpose: To report interrupts which occur in the interrupt area but outside of the current 16-word interrupt block being tested.

Description: The routine saves the registers, calls upon the test executive subroutine SSWT to output the message 'INVALID INTERRUPT' restores the registers, and returns to the point of interrupt.

Entry Points: PINX

Calling Sequence: The routine is entered when an interrupt occurs outside the 16-word interrupt block overlaid by POVL.

Entrance Parameters: The A, B and X register contents are saved upon entering this routine.

Exit Point: The routine returns control to the interrupted routine via the P-register setting at the time of interrupt.

Exit Parameters: The A, B, and X register contents are restored before exiting.

Tables or Files Modified or Read: Not applicable

Tables or Files Created: Not applicable

Called By: Not applicable

Called From: PSAV, PRES, (SSWT)

Exception Conditions: The test may be terminated by using sense switch 3 in SSWT.

Timing: Not applicable

Size: 15 words

Comments: Program halt 04 may be conditionally used by SSWT to halt on the error. (See section 2.4.2)



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Special Notation: Not applicable

Hardware Details: The routine re-enables the PIM after the interrupt.

Flowcharts: See Section 3.2.1

Title: Save registers

Symbolic Name: PSAV

Purpose: To save the contents of the operational registers.

Description: The routine, called at the interrupt level, saves the contents of the A, B and X registers.

Entry Points: PSAV

Calling Sequence: CALL PSAV
RETURN

Entrance Parameters: Not applicable

Exit Point: Return is via the P-register contents saved at PSAV.

Exit Parameters: Not applicable

Tables and Files Modified or Read: Not applicable

Tables or Files Created: Not applicable

Called By: PINX, PIN(N)



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Called From: Not applicable

Exception Conditions: Not applicable

Timing: Not applicable

Size: 6 words

Comments: Not applicable

Special Notation: Not applicable

Hardware Details: Not applicable

Flowcharts: See Section 3.2.1

Title: Restore Registers

Symbolic Name: PRES

Purpose: To restore the contents of the operational registers.

Description: The routine restores the contents of the A, B, and X registers saved by PSAV.

Entry Points: PRES

Calling Sequence: CALL PRES
RETURN



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Entrance Parameters: Not applicable

Exit Point: Return is via the P-register contents saved at PRES.

Exit Parameters: Not applicable

Tables and Files Modified or Read: Not applicable

Tables or Files Created: Not applicable

Called By: PINX, PIN(N)

Called From: Not applicable

Exception Conditions: Not applicable

Timing: Not applicable

Size: 6 words

Comments: Not applicable

Special Notation: Not applicable

Hardware Details: Not applicable

Flowcharts: Not applicable



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Flowchart Worksheet

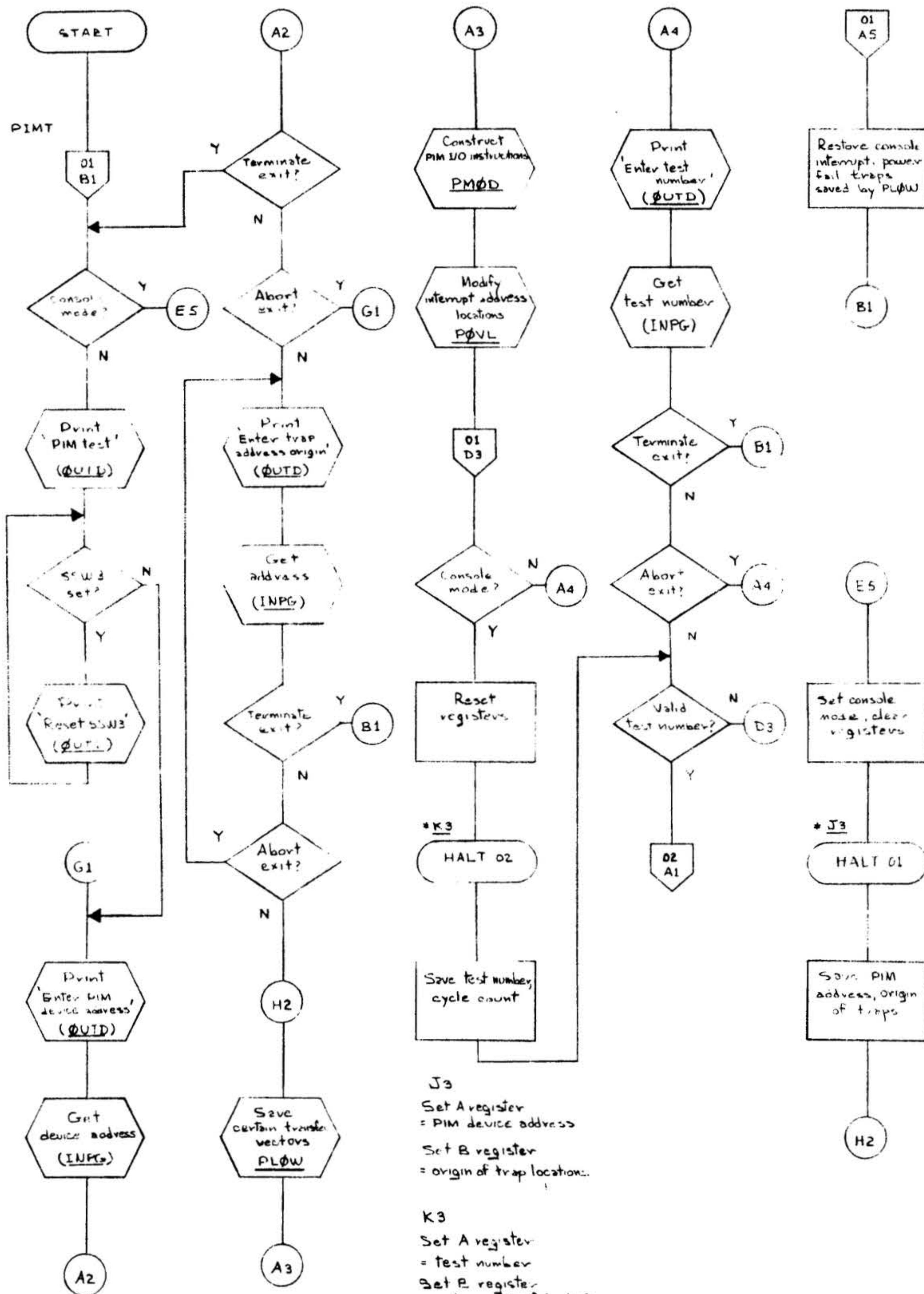
PROGRAMMER:	PROGRAM NO.:	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	
<p>3.2.1 FLOWCHARTS</p> <p>NOTE: SUBROUTINE NAMES IN PARENTHESES ARE LOCATED IN THE TEST EXECUTIVE.</p> <p>EACH CALL TO THE TEST EXECUTIVE SUBROUTINE SSWT HAS AN ACCOMPANYING NOTE DEFINING THE PARAMETER LIST FOLLOWING THE CALL. THE PARAMETER LIST CONSISTS OF A HALT OR OTHER INSTRUCTION TO BE EXECUTED BY SSWT, THE ORIGIN OF AN ERROR MESSAGE OR ERROR MESSAGE SUBROUTINE, A TERMINATE TRANSFER VECTOR, A LOOP TRANSFER VECTOR AND A CONTINUE TRANSFER VECTOR.</p>			
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↑ FOLD UNDER AT DOTTED LINE

↑ FOLD UNDER AT DOTTED LINE

Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME PRIORITY INTERRUPT TEST	



FOLD UNDER AT DOTTED LINE

FOLD UNDER AT DOTTED LINE

J3
Set A register = PIM device address
Set B register = origin of trap location.

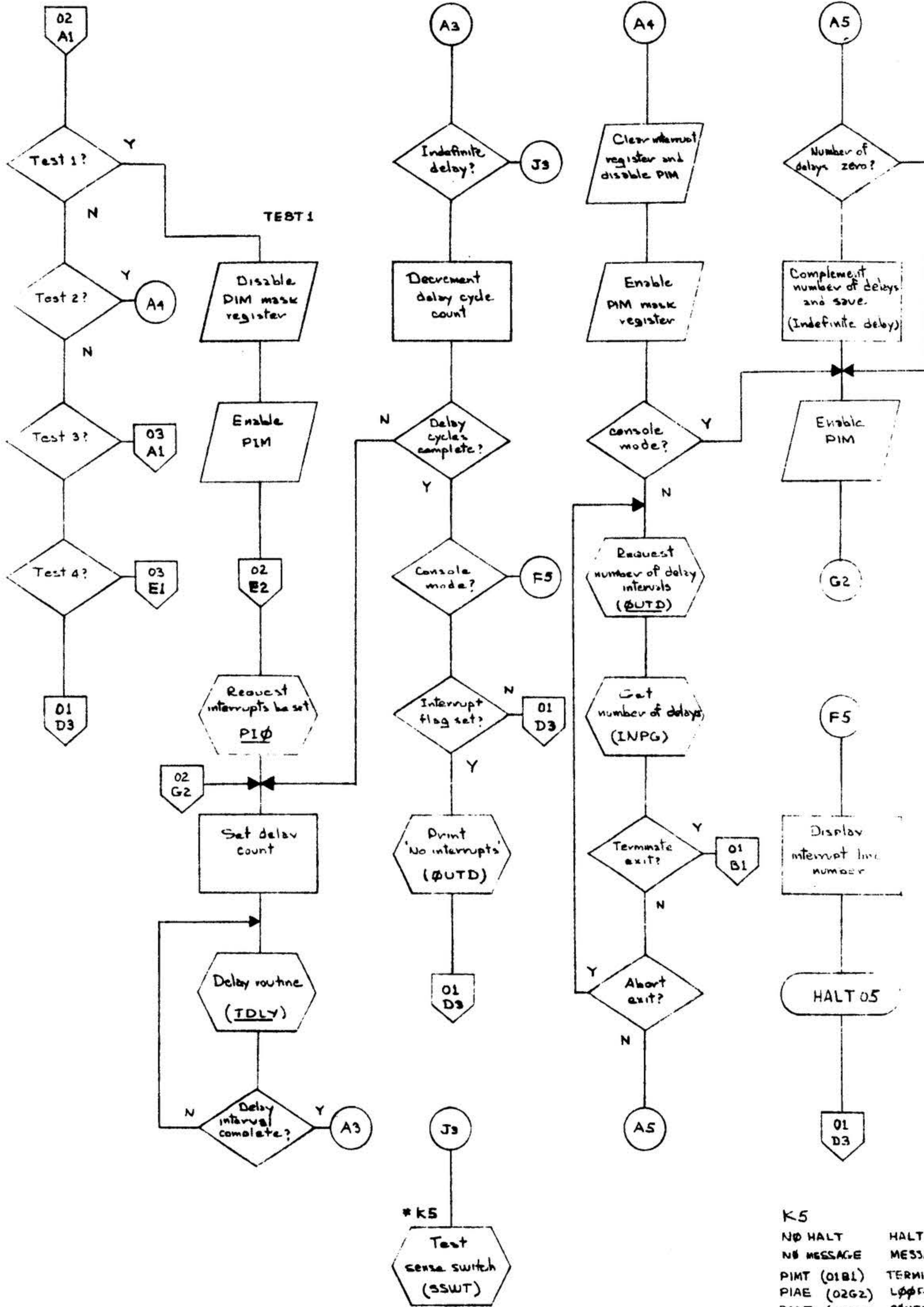
K3
Set A register = test number
Set B register = cycle count (if test 2)

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Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE
CHART I. D.	CHART NAME	PROGRAM NAME	

TEST 2



↑ FOLD UNDER AT DOTTED LINE

↑ FOLD UNDER AT DOTTED LINE

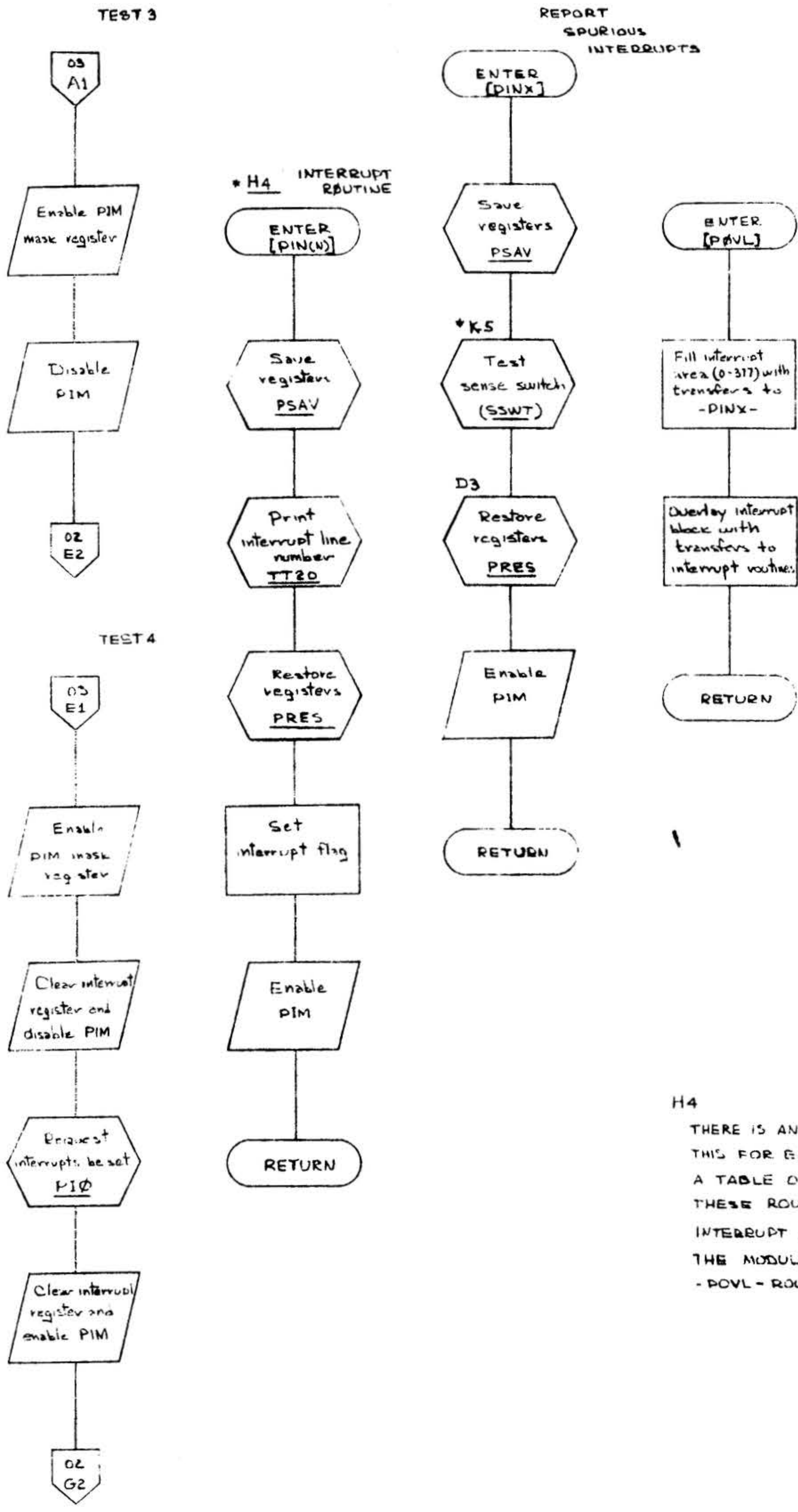
*K5
Test sense switch (SSWT)

K5
 NO HALT HALT
 NO MESSAGE MESSAGE
 PINT (01B1) TERMINATE
 PIAE (02G2) LOOP
 PIAE (02G2) CONTINUE

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Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	



↑ FOLD UNDER AT DOTTED LINE

↑ FOLD UNDER AT DOTTED LINE

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PIEA

ENABLE
MASK
REGISTER

CLEAR \square
ENABLE
PIM

GROUP
DISABLE

DZ
EZ

A2 - +
TEST 5

A3 - +



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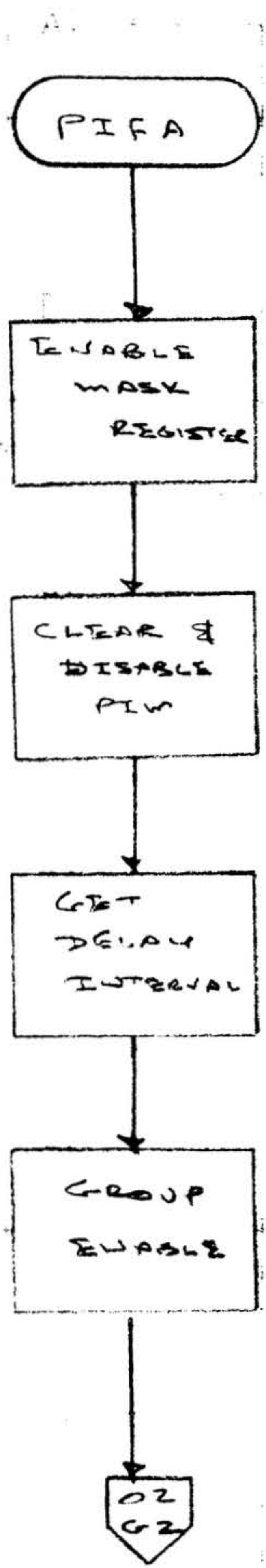
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A2 - + - -
TEST 6

A3 - + - -

B2 - + - -

B3 - + - -

C2 - + - -

C3 - + - -

D2 - + - -

D3 - + - -

E2 - + - -

E3 - + - -

F2 - + - -

F3 - + - -



CODE IDENT NO.
21101

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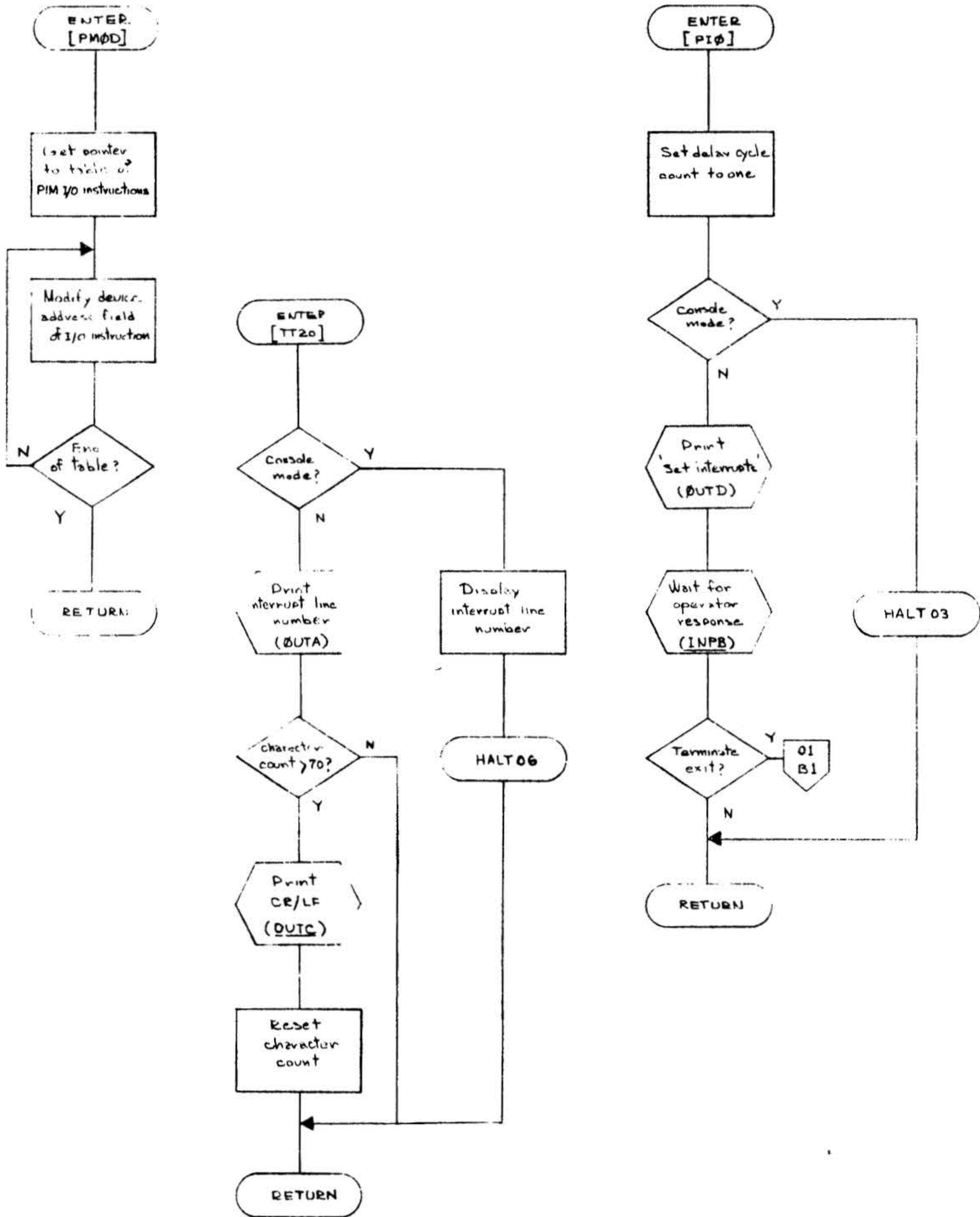
B

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Flowchart Worksheet

PROGRAMMER:	PROGRAM NO.:	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	



↑ FOLD UNDER AT DOTTED LINE

↑ FOLD UNDER AT DOTTED LINE

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SECTION 4: TEST SPECIFICATIONS

4.1 INTRODUCTION

The purpose of the test procedure is to demonstrate to the extent possible, that the program achieves its stated aims. This is done by making several passes thru the test, exercising its various features and inducing hardware and procedural errors which the program should detect. The result is the annotated printout which is included in this section. This printout should also provide additional insight into how to use the test and interpret its results. The test procedure will also define the hardware configuration used in testing.

4.2 TEST PROCEDURE

The following test was run on a 622/i with 4K of core, a model 33 ASR teletype, and one PIM module.

```
THIS IS THE 620 TEST EXECUTIVE
MEMORY SIZE IS 4K
```

```
G500.
```

```
PIM TEST
```

```
ENTER PIM DEVICE ADDRESS 40.
```

```
ENTER ORIGIN OF TRAP ADDRESSES 120.
```

```
ENTER SUBTEST NUMBER 1.
SET INTERRUPTS
NO INTERRUPTS
```

The PIM test was entered thru the 620 Test Executive. The PIM device address and the origin of trap location was entered and subtest 1 was run. After the 'SET INTERRUPTS' message was completed, the 'ALL' button on the interrupt simulator was pressed and the test was resumed by hitting the teletype spacebar. The program correctly reported that no interrupts occurred.



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ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 2.
12345678

ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 2.
123456786666666666666666666666

After the request for the number of delay intervals had completed, the 'ALL' button was pressed and the number of delays entered. When the test was resumed, the number of the lines on which interrupts occurred was printed. (Note the correct priority sequence). The test was run again using the same procedure but additional interrupts were raised on interrupt line 6 during the delay interval.

ENTER SUBTEST NUMBER 3.
SET INTERRUPTS
NO INTERRUPTS

ENTER SUBTEST NUMBER 4.
SET INTERRUPTS
NO INTERRUPTS

ENTER SUBTEST NUMBER
PIM TEST

toggling sense switch 3 returned us to the start of the program. (The trap locations for the console interrupt and power fail were restored by taking this exit.)

ENTER PIM DEVICE ADDRESS 40.
ENTER ORIGIN OF TRAP ADDRESSES 100.
ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 1.
INVALID INTERRUPT

An incorrect origin for the trap locations was specified and an interrupt raised on line 1. The occurrence of an interrupt outside of the 16-word block specified resulted in the invalid interrupt message.



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ENTER SUBTEST NUMBER
PIM TEST
RESET SENSE SWITCH 3
RESET SENSE SWITCH 3

ENTER PIM DEVICE ADDRESS 40.

ENTER ORIGIN OF TRAP ADDRESSES 120.

ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 2.
123412345678

ENTER SUBTEST NUMBER 4.
SET INTERRUPTS
12345678

Interrupts were raised during the delay interval in subtest 4. Since interrupts should not be raised in this subtest following the resumption of the program following the "SET INTERRUPTS" message, the interrupt printout occurred.



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