SPERRY UNIVAC

V70 Series
Writable Control Store II
Operation and Service

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SPERRY UNIVAC®

V70 SERIES
WRITABLE CONTROL STORE II
OPERATION AND SERVICE MANUAL

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SECTION 1
GENERAL DESCRIPTION

The SPERRY UNIVAC 70 Series Writable Control Store II Manual describes the high density writable control store II option (models 70-4003 and 70-4004) and its interface with a SPERRY UNIVAC 70 series computer.

The manual is divided into six sections:

- Features and specifications of the high density writable control store II, and related publications
- Installation and interconnection data
- Operation
- Theory of operation
- Maintenance
- Mnemonics list

Documents such as logic diagrams, schematics, and parts lists are supplied in a system documentation package. This documentation is assembled when the equipment is shipped, and reflects the configuration of a specific system.

The following list contains the part numbers of other manuals pertinent to the SPERRY UNIVAC 70 series computers (the x at the end of each document part number is the revision number and can be any digit 0 through 9).

Title	Manual Number
72 System Handbook	98 A 9906 20x
73 System Handbook	98 A 9906 01x
74 System Handbook	98 A 9906 21x
75 System Supplement	98 A 9906 22x
76 System Reference Manual	98 A 9906 23x
Processor Manual	98 A 9906 02x
8K Core Memory Manual	98 A 9906 03x
16K Core Memory Manual (1200 ns)	98 A 9906 24x
16K Core Memory Manual (990 ns)	98 A 9906 25x
8K Semiconductor Memory Manual	98 A 9906 04x
Option Board Manual	98 A 9906 05x
70 Series Power Supply Manual (Universal)	98 A 9906 06x
72 Power Supply Manual	98 A 9906 12x
72/76 Power Supply Manual	98 A 9906 13x

Title	Manual Number
Microprogramming Guide	98 A 9906 07x
Writable Control Store Manual	98 A 9906 08x
70 Series Cache Manual	98 A 9906 28x
Memory Map Manual	98 A 9906 10x
Megamap Manual	98 A 9906 27x
MAINTAIN III Manual	98 A 9952 07x
VORTEX Reference Manual	98 A 9952 10x
VORTEX II Reference Manual	98 A 9952 24x

The Writable Control Store II option (WCS II) extends the processor's read-only control store to permit addition of new instructions, development of microdiagnostics, and optimum tailoring of the computer system to its application. Unlike the read-only control store, which contains the 70 basic instruction set and cannot be altered, the WCS II can be loaded from the computer system's main memory under control of certain I/O instructions. The capability of altering the contents of the WCS gives the user complete access to the resources of the 70 series computer system.

Through processor interface circuits, the WCS II can disable the processor's internal read-only control store and assume control of processor operations. Microinstructions are written into and read out of the WCS II using I/O instructions.

Supporting software for the WCS II includes a utility loader, a machine micro simulator and a micro assembler. The WCS II can operate in a stand-alone environment or under control of the VORTEX operating system. A test program is provided in Maintain III to aid in maintaining the WCS II hardware.

An additional WCS II feature enables main memory in a 70 series system to be expanded to 65,536 words.

The WCS II is available in the following two configurations:

a. Model 70-4003 includes a 1024-word by 64-bit control store and a subroutine stack.

b. Model 70-4004 includes a 2048 word by 64-bit control store and a subroutine stack.

Specifications for the WCS II are listed in table 1-1.

Table 1-1. Writable Control Store II Specifications

Parameter	Specification
Cycle Time	190 nanoseconds.
Capacity	Up to three WCS IIs (4096 words maximum) for each computer system.
Selection	WCS II can be selected by a BCS macroinstruction or a processor page-branch microinstruction.
Control	WCS IIs are loaded and read under programmed I/O control. Loading can be performed in one WCS II while executing from another.
Dimensions	Contained on a 15.6 by 19 inch printed circuit board.
Installation	Plugs into a SPERRY UNIVAC 70 series mainframe chassis using one module slot.
Input Power	+5V dc, 16 amperes for model 70-4003 (1024 words), 22 amperes for model 70-4004 (2048 words).
Operational Environment	0 to 50 degrees C (32 to 122 degrees F) 0 to 90 percent relative humidity without condensation.

SECTION 2
INSTALLATION

This section contains installation instructions for the SPERRY UNIVAC 70 Series WCS II Module.

2.1 INSPECTION

The WCS II modules are packed using standard practices for the shipment of electronic parts. Every precaution is taken to ensure that each WCS II module arrives in good working order, ready for installation. However, it is recommended that upon unpacking, each module be inspected for in transit damage. Ascertain that all components, wires, cables, etc., are in good physical condition and all hardware is secure. In the case of damage, notify the transportation company and Sperry Univac immediately; save all packing materials. Check the modules removed from the shipping carton against the shipping list to verify quantity and serial numbers. Contact Sperry Univac immediately upon determining any discrepancies.

2.2 INSTALLATION

The WCS II module is depicted in figure 2-1. The module plugs into the SPERRY UNIVAC 70 series mainframe chassis; only one module slot is required. The WCS II module connectors interface to the system as follows:

P01	Main memory
J2	Processor
J3	Processor
J4	PMA
J5	I/O bus
J6	Option board, processor and DMA
J7	Power

J7 supplies power to the WCS II module. This power is usually provided by a WCS II power supply (p/n 01P1280-004); it may alternately be supplied by the SPERRY UNIVAC 70 main supply or a configuration specified by the user.

Figure 2-2 shows the WCS II module interconnections in a SPERRY UNIVAC 70 series CPU chassis. The chassis shown is fully-loaded and contains three WCS II boards. Pin assignments for the WCS II module connectors are listed in the logic diagrams.

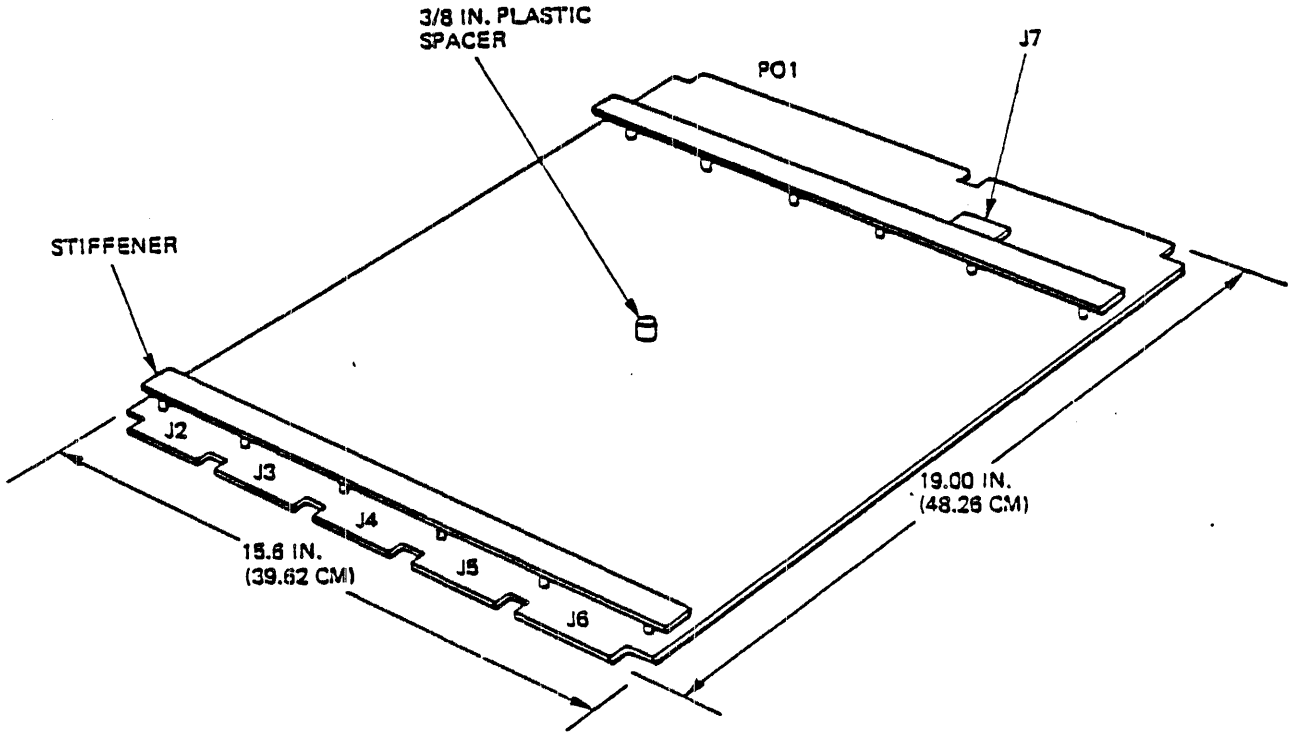


Figure 2-1. WCS Board

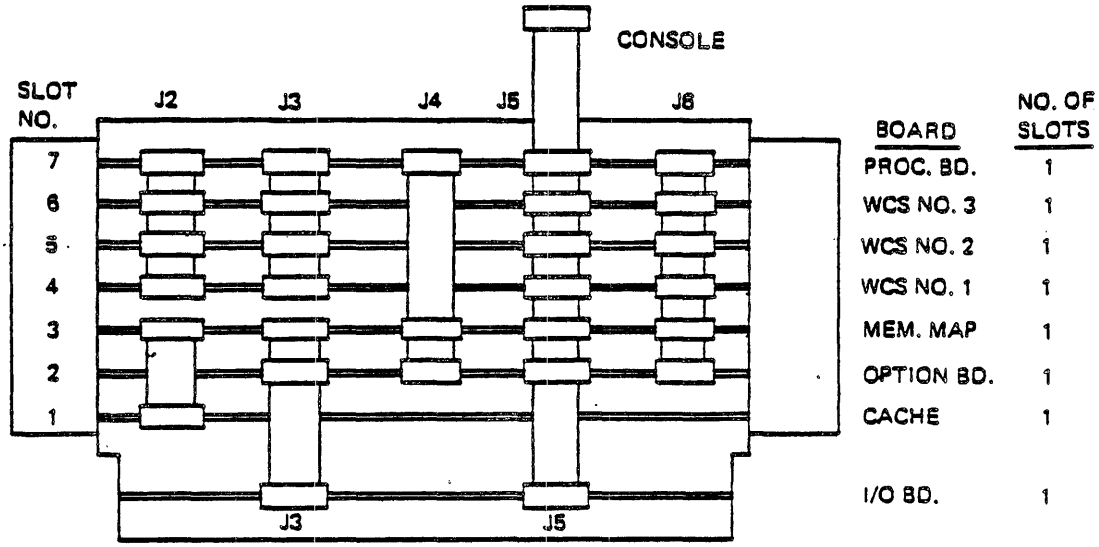


Figure 2-2. 70 Configuration with Three WCS II Boards

2.3 WIRING OF WCS II JUMPER TERMINALS

The connections to the jumper terminals on the WCS II module are factory wired. The connections are not normally changed unless the user is expanding the WCS II capability. The jumper terminal connections, on the WCS II module, are listed in the WCS II option drawing. The jumper terminal designations referred to, in the option drawing, appear on the WCS II module adjacent to the referenced terminal.

2.4 CONFIGURATION

Each WCS II module in the system must be configured as depicted in table 2-1. Table column headings are defined as follows:

Function	The name of the feature under consideration.
Logic Page	The page number of the WCS II logic drawing, 91C0570, where the feature is located.
Standard Configuration	The standard configuration assembled prior to discretionary configuration of the board.
Alternate Configuration or Remarks	The alternate method by which the feature may be configured. This configuration is specified by the Sperry Univac systems engineer. This column may contain a remark if not used for defining an alternate configuration.

2.4.1 Power Requirements

Power for the WCS II may be provided in one of three ways, as follows:

a. By a 115V ac (01P1280-004) or 230V ac (01P1280-005) power supply and cable (53D0872) for each WCS II module.

b. If sufficient excess logic power is available in the system, a second cable (53P0873) from a 73 power supply (01P1320) or a second cable (53P0808) from a 72/76 power supply (01P1896) may be used.

c. A specially designed power supply arrangement may be used as specified by the user and a Sperry Univac systems engineer.

Table 2-1. Configuration for WCS II System

Function	Logic Page	Standard Configuration	Alternate Configurations or Remarks
I/O device address selection	14.0	Device Address / Configuration Setting: 4 5 6 70-71: ON OFF OFF 72-73: OFF ON OFF 74-75: OFF OFF ON	All modules (pages are jumpered to same device address.
Page address selection	22.0	Connection / Page / Selected ST2E 1-2 etched: 1 Yes ST2E 4-5 etched: 2 Yes ST2E 7-8 etched: 3 Yes ST2E 10-11 etched: 4 Yes ST2E 9 no conn: 5 No ST2E 12 no conn: 6 No ST2E 6 no conn: 7 No ST2E 3 no conn: 8 No	To change page address selection: 1. Cut etch between wire wrap pins at location ST2E for only those pages to be deselected. 2. Add wire-wrap jumper at ST2E between wire wrap pin corresponding to page to be selected and any one of the pins freed-up by cutting etch in step 1 (i.e., pins 2, 5, 8 or 11). Up to four pages can be selected per WCS II board.
I/O module selection	27.0	Connection / I/O Module / Selected Y6E 2-3 etched: 1 Yes Y6E 4-5 etched: 2 Yes Y6E 6-7 etched: 3 Yes Y6E 8-9 etched: 4 Yes Y6E 10 no conn: 5 No Y6E 11 no conn: 6 No Y6E 12 no conn: 7 No Y6E 1 no conn: 8 No	To change I/O module selection: 1. Cut etch between wire wrap pins at location Y6E for only those I/O modules to be deselected. 2. Add wire-wrap jumper at Y6E between wire-wrap pin corresponding to I/O module to be selected and any one of the pins freed-up by cutting etch in step 1 (i.e., 3, 5, 7 or 9).

Table 2-1. Configuration for WCS II System (Continued)

Function	Logic Page	Standard Configuration	Alternate Configurations or Remarks
			Up to four I/O modules can be selected per WCS II board.
Fine clock output connection	20.0	A1E1-2	Jumper clip is only installed on module one (master clock module).
Page select signal to processor	21.0	AB1E1-2	Jumper clip is only installed on module one (master clock module).
Module one enable	14.0	Configuration Switch Setting: Switch one is OFF.	Switch one is only on module one. Set switch one off on second and subsequent modules.
Precharge	14.0	Configuration Switch Setting: Switch two is OFF. Precharges control lines CEAD0- through CEAD8-.	Only on module one. Set switch two OFF on second and subsequent modules.
BCS entry table	18.0	Entry Table Size / Jumper Clip E13E1-2 / E13E1-2 / E13E3-4: 32 words — No / No / No (std.); 64 words — Yes / No / No (opt.); 128 words — Yes / Yes / Yes (opt.); 256 words — Yes / Yes / Yes (opt.)	System definition defines size of jump table. All modules must be jumpered the same. BCS test prints errors for table size larger than enabled.
BCS not privileged instruction	21.0	X2E1-2	Leave jumper off on all modules except module one. Jumper off on all modules enables decode I/O signal to memory protect.

Table 2-1. Configuration for WCS II System (Continued)

Function	Logic Page	Standard Configuration	Alternate Configurations or Remarks
Memory port data address 15, memory lockout, and memory done selection (MYD00- through MYD15-, MYMA15+, MYAA15+, MYMB15+, MYAB15+, MIMY-, MIGP-, YDNMA, B+)	14.0	Configuration Switch (X12) Setting Port A: SWITCH SEVEN ON Port B: SWITCH SEVEN OFF	Select same port as processor in final system configuration.
Address 15 control	19.0	MYMA15+ — Port A — Sw. three ON (Map Present) / -- (Map Not Present) MYAA15+ — Port A — -- (Map Present) / Sw. three OFF (Map Not Present) MYMB15+ — Port B — Sw. three ON (Map Present) / -- (Map Not Present) MYAB15+ — Port B — -- (Map Present) / Sw. three OFF (Map Not Present)	
65K memory control	19.0	S13E1-2 etched. Enable 65K mode only when WCS II is selected.	Cut etch between S13E1-2. This allows 65K mode to always be enabled.
65K memory request	22.0	X1E2-3 etched. Allows 65K mode control from processor only.	Cut etch X1E2-3 and add jumper X1E1-2. Allows 65K mode control from PMA device during PMA memory request and from processor.
Memory hog Port A	19.0	A13E1-2 D13E1-2	
Port B		A13E2-3 D13E2-3	

2.4.2 WCS II Debug Configuration

The WCS II can be debugged using the WCS II Test Program (in Maintain III). The minimum configuration required to run this program is:

> 70 system containing a processor, option board (with TTY controller), 32K minimum memory, Teletype, and one or more WCS IIs.

2.4.3 WCS II with 73 Configuration

The following modification to the 73 processor board (44P0614) is required for installation of a WCS II:

> Remove the jumper from J1 to J2; connect J2 to J3. (This modification supplies the processor with the WCS II fine clock in place of the processor fine clock.)

The following modification to the WCS II board is required for installation in a 73 computer:

> Connect a jumper from A1E-1 to A1E-2.

2.4.4 65K Mode with PMA Configuration

When the WCS II is to be operated in the 65K mode of operation with a PMA, the WCS II must connect to the J4 cable to pick up the MAKO+ signal. This means that a ribbon cable connector (57A0272-003) must be added to the J4 cable (in the position corresponding to the WCS II slot assignment) for each WCS II in the system. When a floating point processor (FPP) is present, each WCS II must connect to the J4 cable on the option board side of the FPP.

2.4.5 WCS Mixed Configuration

The WCS I (model 70-4002) and WCS II (models 70-4003, 70-4004) can coexist in a system with up to a maximum of eight pages of writable control store (4096 words). In each configuration, the CPU ROM is designated as page zero and pages 1 through 8 are for use of the WCS I & II. However, page 8 of the WCS I & II cannot be returned through the subroutine stack.

2.4.6 Multiprocessor Configuration

The only restraint upon using a WCS II in a multiprocessor system is that the system configuration must ensure that independent memory acknowledgement signals on both ports do not simultaneously set memory lockout for the same memory module. This locks out both ports, making the memory module inaccessable.

To ensure this does not happen, a few basic rules should be followed; they are:

a. Do not enable a lockout condition on both ports. If an 8K core or 8K semiconductor memory module has a lockout condition on both ports simultaneously, it will serve neither port and the memory system will hang up. (If a 660 nanosecond semiconductor memory is used, the ports will be serviced on a priority basis and a system hang-up will not occur.)

b. Common memory between two processors which is to be accessed from either processor using lockout mode should be restricted to one non-interleaved module. Then, if both processors enable lockout during memory access to the common module at the same time, only the port that receives the memory access will activate lockout of the other port. (This does not apply to 660 nanosecond semiconductor memory.)

c. The processor memory access with lockout enabled should always be to the common module (does not apply to 660 nanosecond semiconductor memory), the common module being the only memory module in the system that has both hog lines connected. MHGY- is etch connected and MHMY- connection is jumper clip selectable (does not apply to 660 nanosecond semiconductor memory).

SECTION 3
OPERATION

The WCS II contains no operating controls or indicators other than the WCS II-active indicator (this is a LED that lights when the WCS II is selected). The following subsections describe various WCS II instructions. For further information on WCS II microprogramming, refer to the Microprogramming Guide, document number 98A9906-07x. In the microprogramming guide, all fields of the 64-bit micro words are designated with two letters making them consistent with the mnemonics used in the microprogramming assembler (MIDAS). This is done by adding the letter F to all one-letter designated fields except the A and B fields. The A and B fields are designated AA and BB, respectively.

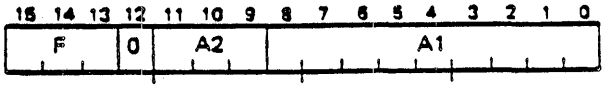
3.1 I/O INSTRUCTIONS

The I/O instructions used with the WCS II are listed in table 3-1. Two device addresses are used for each WCS system to differentiate data transfers from the other I/O instructions. Three pairs of device addresses are available to provide address flexibility. The device-address pairs are: 70 and 71, 72 and 73, 74 and 75. In the table, the last digit of the device addresses is represented with an X or Y (where X can equal 0, 2, or 4; and Y can equal 1, 3, or 5).

Following each I/O data-transfer instruction, the WCS II address register is incremented.

3.2 FORMAT FOR I/O OUTPUT-CONTROL TRANSFERS

The word format for an I/O output-control transfer instruction is:



The A1 field specifies the address in the WCS II address register, the A2 field specifies the WCS II module address, and the F field specifies the function.

Table 3-1. I/O Instructions

Mnemonics	Machine Code (Octal)	E-Bus Code (Octal)	Function
External Control			
EXC 07X*	10007X	00407X	This is the initializing instruction that resets the WCS II, deselects all WCS II control stores, and enables the clock from the WCS II board.
Program Sense			
SEN 07X*	10107X	01007X	This instruction senses if the WCS II is busy. A WCS II module is busy when one of its control stores is both I/O and process selected.
Output Control Transfer			
OAR 07X*	10317X	04007X	Transfers address and control functions from A register (OAR), B register (OBR), or main memory (OME), respectively, to WCS II.
OBR 07X*	10327X		
OME 07X*	10307X		
Output Data Transfer			
OAR 07Y**	10317Y	04007Y	Transfers data from A register (OAR), B register (OBR), or main memory (OME), respectively, to WCS II.
OBR 07Y**	10327Y		
OME 07Y**	10307Y		
Input Data Transfer			
INA 07Y	10217Y	02007Y	Transfers data from WCS II to A register.
INB 07Y	10227Y		Transfers data from WCS II to B register.
INAB 07Y	10237Y		Inclusively ORs data from the WCS II with the contents of the A and B registers and places the results in the A and B registers, respectively.

Table 3-1. I/O Instructions (Continued)

Mnemonics	Machine Code (Octal)	E-Bus Code (Octal)	Function
IME 07Y	10207Y		Transfers data from WCS II to main memory.
CIA 07Y	10257Y		Transfers data from WCS II to cleared A register.
CIB 07Y	10267Y		Transfers data from WCS II to cleared B register.
CIAB 07Y	10277Y		Clears the A and B registers and transfers data from the WCS II to the A and B registers.

* X equals 0, 2 or 4
** Y equals 1, 3 or 5 when X equals 0, 2 or 4 respectively.

Table 3-2. Function Definitions

Bits 15	14	13	Function
0	1	1	Selects the central control store in the module specified by the A2 field. The WCS II address register is loaded with bits from the A1 field.
1	0	0	Selects the current address for the central control store. Subsequent input data transfers cause the 12-bit WCS II address to be transferred to the processor.

All other bit configurations in the F field are not implemented.

The I/O output-control transfer instruction provides setup in-information for subsequent I/O data transfers (F field contains 011 or 100). The remaining bit configurations for the F field (bits 13, 14, 15) are not used.

The functions for bits 13 through 15 are shown in table 3-2.

3.3 BRANCH AND MEMORY-CONTROL MICROINSTRUCTIONS

The following subsections describe the various microinstructions used for page-branch and memory-control functions. When the page-branch microinstructions are used, the control store of the selected page is also selected. If the selected page does not contain a control store, the control buffer driver CBI(00 through 63) outputs are all high. Unless otherwise specified, the fields referred to are part of the 64-bit microword format.

3.3.1 Branch with Memory Control

This page-branch microinstruction implements a WCS II page-branch operation when the following field* conditions occur:

T contains 00
S contains 10
G contains x1xx

The selected WCS II module (or page) is specified by the 4-bit TS field and the word address is defined by the normal addressing mode (see section 4.9 of the processor manual, 98A9906-02x). The WCS II board contains the logic for buffering the TS, T, S, and G fields, and to implement the page-branch control.

3.3.2 Branch Without Memory Control

This page-branch microinstruction allows execution overlap of the last WCS II microinstruction with the decoding of the next processor microinstruction. This microinstruction is implemented when the following field conditions occur:

T contains 00
S contains 00
IM contains 0011

The microinstruction for branching without memory control is also useful as a general page branch when the G field contains x0xx. This enables the TS field to specify the target page without enabling interrupts.

* For field definitions, refer to the Microprogramming Guide.

3.3.3 Stack Operations

There are three page-branch microinstructions used with the subroutine stack: branch/push, branch/pop, and branch/delete. All three operations have the following field conditions:

S contains 00
T contains 00
IM contains 1101
LB contains 11

For the branch/push operation, bit one of the A field is one. For the branch/pop operation, bit two of the A field is one and bit zero of the B field is zero. For the branch/delete operation, bit two of the A field is one and bit zero of the B field is one.

The stack is a 16-level wraparound structure. Reset initializes the stack pointer to zero. Therefore, for a push operation, the stack will start at location one (the stack pointer is incremented before access). For a pop operation, the stack will start at location zero (the stack pointer is decremented after access).

3.3.4 64K Memory Addressing

This microinstruction sets or resets an enabling signal (65KMDE+) for bit 15 of the memory address bus. While operating from the read-only control store in the processor, address bit 15 is automatically disabled. Thus, it is possible to have WCS II microinstructions addressing 64K (65,536 words) without setting and resetting the bit 15 enabling signal as the microprogram jumps back and forth between WCS II and the read-only control store of the processor.

The enabling signal for address bit 15 is set when the following field conditions occur:

S contains 00
T contains 00
IM contains 1101
LB contains 11
M contains 1

The enabling signal for address bit 15 is reset when the following field conditions occur:

S contains 00
T contains 00
IM contains 1101
LB contains 11
C contains 1x

3.3.5 Memory Lockout (Hog Mode)

This microinstruction sets and resets the memory lockout control of the WCS II. Setting the memory lockout control (MHMY- or MHGY-) prevents the processor's main memory from being accessed by devices on the opposite port. Resetting it clears (or removes) the lockout control. This feature is useful in a multiprocessor system where one processor must exclusively update memory locations that are also accessible to other processors.

The memory lockout control is set when the following field conditions occur:

S contains 00
T contains 00
IM contains 1101
LB contains 11
C contains x1

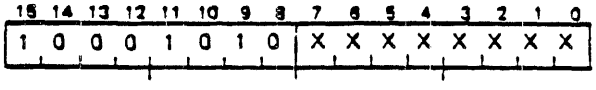
The memory lockout control is reset when the following field conditions occur:

S contains 00
T contains 00
IM contains 1101
LB contains 11
A contains xxx1

A system restraint when using the memory lockout feature is that a main memory module having a lockout control set on both ports will service neither port. Memory lockout is set when a memory acknowledgement (YDNMA- or YDNMB-) indicates the port is available. The system configuration must ensure that independent memory acknowledgement signals on both ports do not simultaneously set memory lockout for the same memory module.

3.4 BCS MACROINSTRUCTION (BRANCH TO CONTROL STORE)

The BCS macroinstruction selects the central control store (CCS) in the WCS II module one. The BCS word format is:



where bits 0 through 7 specify the address in the CCS of WCS II module one. A branch to any one of the first 32 words is standard, and the capability for branching to any one of the 256 words is made optional with jumper connections on the WCS II board of module one.

Decoding of the BCS macroinstruction is implemented on the WCS II board, and occurs during preliminary instruction decoding as defined by the processor. The following are important characteristics of the BCS operation.

a. The BCS macroinstruction is performed only if the processor's instruction decoder is currently selected. If it coexists with the WCS I, which has a decoder control store, then the BCS is simply part of a different instruction set definition.

b. The BCS macroinstruction can operate from the CCS of the processor or any active WCS II module.

c. The BCS macroinstruction is the only instruction that will micro page-branch from the processor's ROM (page zero) to WCS II control store (page one).

In order to execute the BCS macroinstruction from an unprotected location in main memory without causing a memory protection error, it is necessary to disable I/O control signal CIDIO+. CIDIO+ is disabled with a jumper connection on the WCS II board. By removing the jumper, the BCS is protected the same as an I/O instruction. For operation with the jumper removed, the WCS II microcoded entry points must be programmed to process an interrupt condition (OINT) caused by the memory protection request.

3.5 SUMMARY OF OPERATION

This section summarizes the differences in operation between the WCS I model 70-4002 and the WCS II models 70-4003 and 70-4004 described in this manual. Tables 3-3 and 3-4 are operations and function implementation summaries, respectively.

Both series of WCS modules use the same instruction word format for I/O output control transfers (OAR 07X, OBR 07X, OME 07X); the format is shown below:

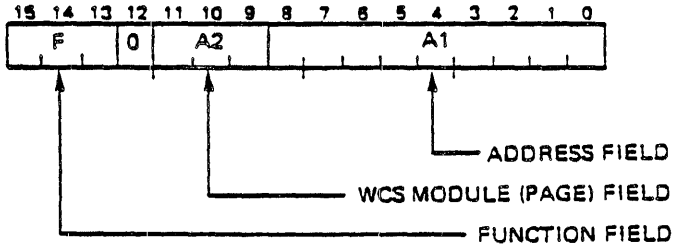


Table 3-3. Summary of Operation

WCS Operation Feature	WCS I (70-4002)	WCS II (70-4003, 70-4004)
Central control store size	256 or 512 words	1024 or 2048 words
I/O and decoder control store	Yes	No
Clock generator	Yes	Yes
Subroutine stack	16 level with overflow/ underflow detection	16 level wrap-around, no overflow/ underflow detection
Memory interface capability to configure port A and port B	Yes	Yes
BIC interface control	Yes	No
Micro-step function	Yes	No
I/O instructions:		
EXC 07X*	Yes	Yes
EXC 17X	Yes	No
EXC 27X	Yes	No
EXC 37X	Yes	No
EXC 47X	No	No
EXC 57X	No	No
EXC 67X	No	No
EXC 77X	Yes	No
SEN 07X	Yes	Yes
SEN 17X	Yes	No
SEN 27X	Yes	No
SEN 37X	Yes	No
OAR 07X	Yes	Yes
OBR 07X	Yes	Yes
OME 07X	Yes	Yes
OAR 07Y**	Yes	Yes
OBR 07Y	Yes	Yes
OME 07Y	Yes	Yes
INA 07Y	Yes	Yes
INB 07Y	Yes	Yes
INAB 07Y	Yes	Yes

* X equals 0, 2, or 4.
** Y equals 1, 3, or 5.

Table 3-3. Summary of Operation (Continued)

WCS Operation Feature	WCS I (70-4002)	WCS II (70-4003, 70-4004)
IME 07Y	Yes	Yes
CIA 07Y	Yes	Yes
CIB 07Y	Yes	Yes
CIAB 07Y	Yes	Yes
BCS macroinstruction - standard 32 entries, option 1 to 256 entries	Yes	Yes
Page branch microinstructions:		
Branch with memory control	Yes	Yes
Branch without memory control	Yes	Yes
Stack push	Yes	Yes
Stack pop	Yes	Yes
Stack pop/delete	Yes	Yes
64K memory addressing	Yes	Yes
Memory lockout	Yes	Yes

Table 3-4. Function Implementation Summary

[F] Implemented	WCS I	WCS II
000	Yes	No
001	Yes	No
010	No	No
011	Yes	Yes
100	Yes	Yes
101	Yes	No
110	Yes	No
111	Yes	No

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

The WCS II theory of operation section consists of an overall functional description followed by detailed circuit descriptions. Functional block diagrams accompany the text to aid the reader in understanding the circuit descriptions. For ease of reading, some mnemonics are written with the variables n and x in place of the actual numbers and letters. For example, memory data mnemonics MYDA00- through MYDA15- and MYDB00- through MYDB15- are written MYDxn-(00 through 15). Mnemonic definitions are provided in section 6.

4.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the WCS II is illustrated in figure 4-1. An instruction word MYDAn-(00 through 15) or MYDBn-(00 through 15) from the memory port A or B is decoded; the resulting signal is the 9-bit address CEADn(0 through 8) that is applied to the central control store (CCS).

With each processor clock pulse, a 64-bit microinstruction CBIn+(00 through 63) is read from the CCS to specify processor operations. A typical microinstruction may define several operations such as selecting the next control store address, specifying test conditions for micro branching, initiating a memory operation, and selecting an ALU function.

Addressing for the 64-bit microinstruction is provided by the 9-bit address word WSABn+(0 through 8) from either the processor or subroutine stack.

Data are written into the CCS in 16-bit words WSEBn+(00 through 15) from the I/O bus. A 64-bit word in the CCS consists of four words from the I/O bus. Addressing for these operations is provided by an address register WSARn+(0 through 8) which is loaded from the I/O bus.

The subroutine stack increases the WCS II storage efficiency by providing a call and return capability for microinstruction subroutines. Up to sixteen 12-bit addresses can be stored in the stack. The addresses consist of CCS data CBIn+(04 through 15). The addresses are returned to the CCS as WSSTn-(00 through 11).

4.3 BASIC WCS II CIRCUITS

The basic circuits of the WCS II are shown in the block diagram of figure 4-2. Page numbers of the WCS II logic diagrams are shown in parentheses for each circuit block. A description for each circuit of the basic WCS II is provided in the following subsections.

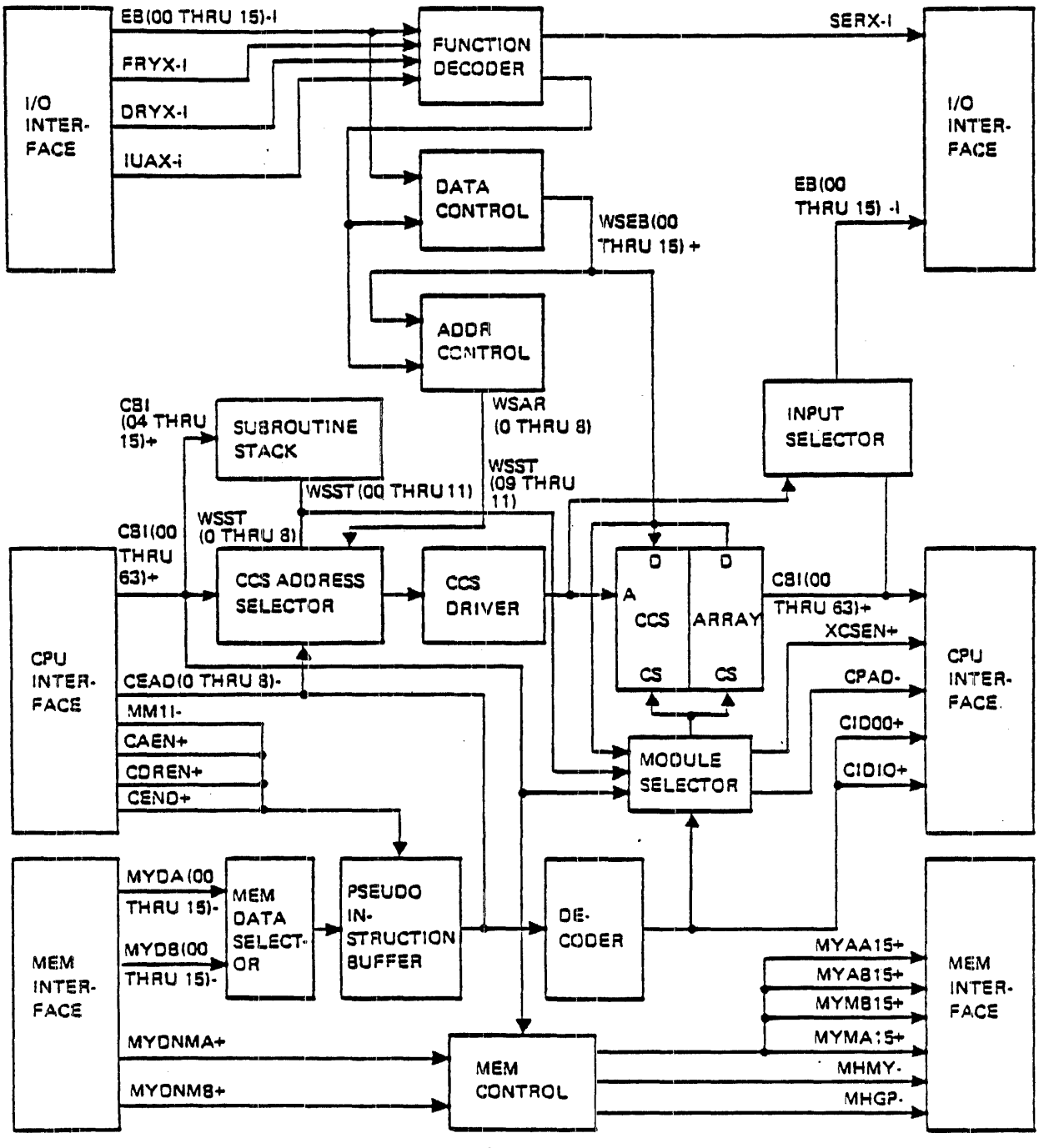


Figure 4-1. WCS II Functional Block Diagram

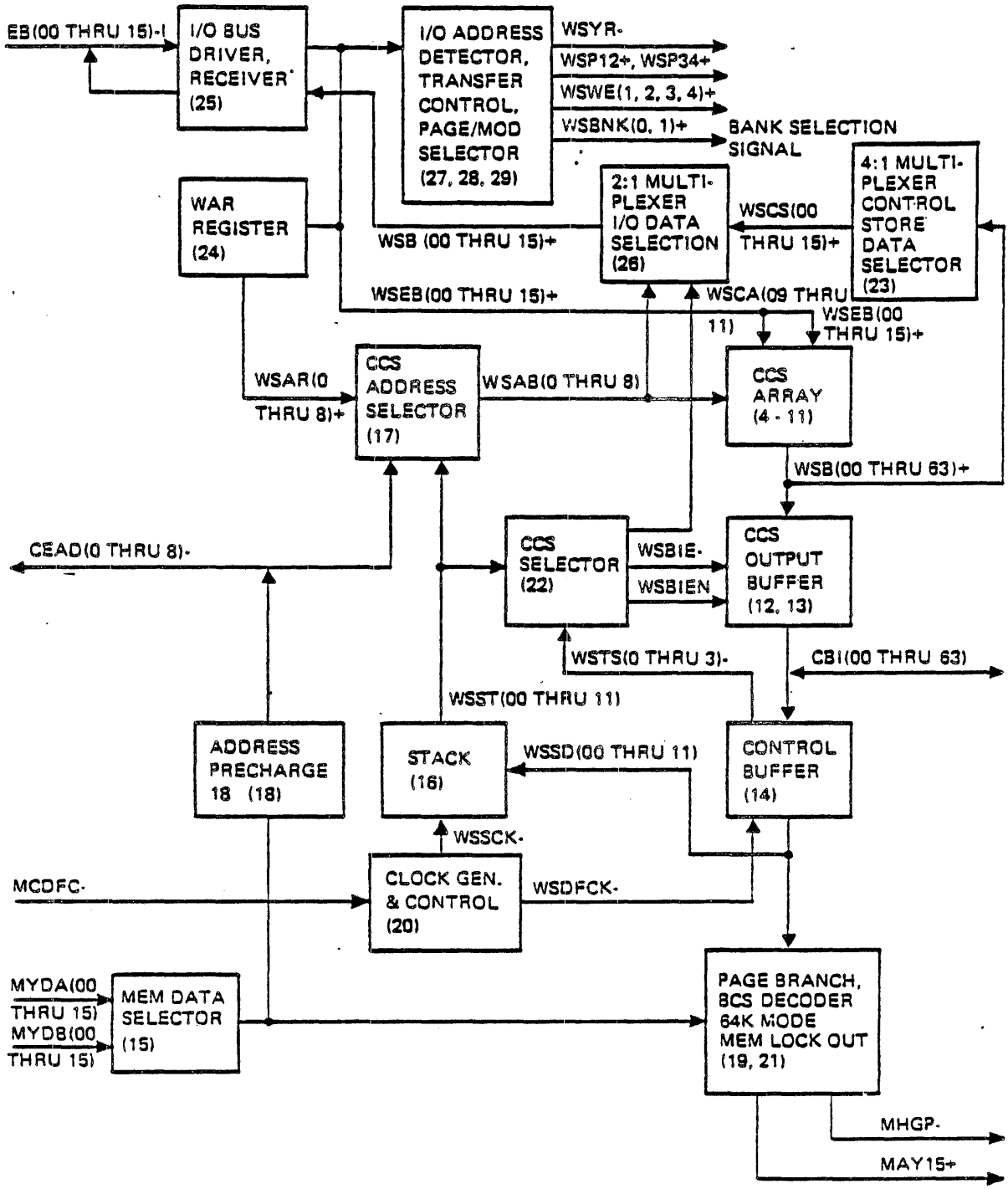


Figure 4-2. Block Diagram of WCS II Circuits

4.3.1 I/O Bus Drivers and Receivers

During an input-data transfer (WDT1+ high), the I/O bus drivers transfer data from the two-to-one data multiplexor onto the bi-directional I/O bus.

Data from the I/O bus are inverted by the I/O bus receivers and routed to the control store, and I/O address detection and control. Low power schottky receivers are used for light loading to the bus (360 microamp/input).

4.3.2 CCS Array

As shown in figure 4-3, the CCS array is divided into two banks. Each bank consists of 1024 words by 64 bits, each of which is further subdivided into four 16-bit word sections. The banks are selected by a high WSBNK0+ or WSBNK1+. A high WSWEn(1 through 4) is the strobe for writing 16-bit data words WSEBn+(00 through 15) from the I/O bus receivers into the addressed location of a selected sector.

4.3.3 CCS Address Selector

As shown in figure 4-4, the CCS arrays are addressed from three sources: the subroutine stack WSSTn-(0 through 8); the processor CEADn-(0 through 8); the I/O address register WSAR(0 through 8). These three address sources are selected through the multiplexor to produce the CCS address WSABn(0 through 8).

4.3.4 Page Selector

As shown in figure 4-5, the CCS arrays are segmented into four pages which are selected by the page and module registers. The page register outputs WSPS (A,B,C,D)- are decoded from the microinstruction page-branch or subroutine stack. The module register outputs WSMOD (A,B,C,D)- are decoded from the I/O control transfer.

The outputs of these registers generate the ninth address bit (either WSP12+ or WSP34+) and the bank select signal (either WSBNK0+ or WSBNK1+). The LED diode is lighted when the WCS II is either selected by the page or module registers.

4.3.5 CCS Drivers

The CCS drivers provide refreshing of address, write-enabling, and chip select signals to the whole arrays.

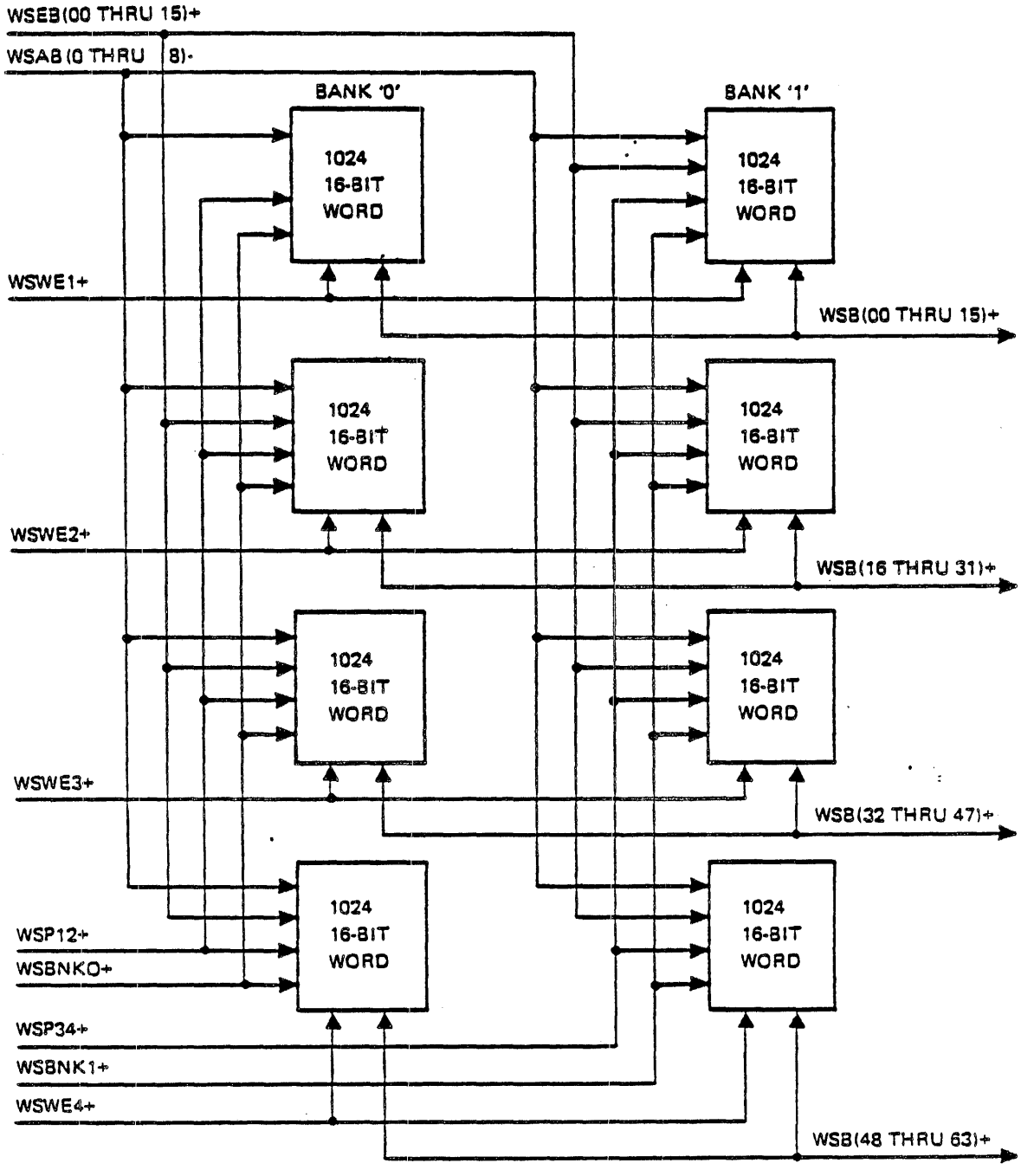


Figure 4-3. CCS Array Block Diagram

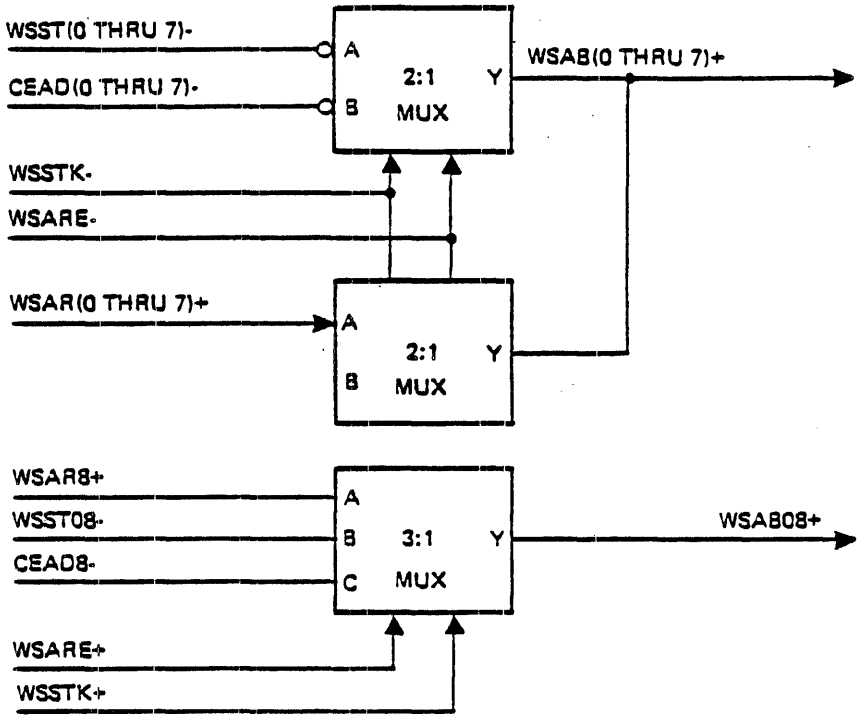


Figure 4-4. CCS Address Select

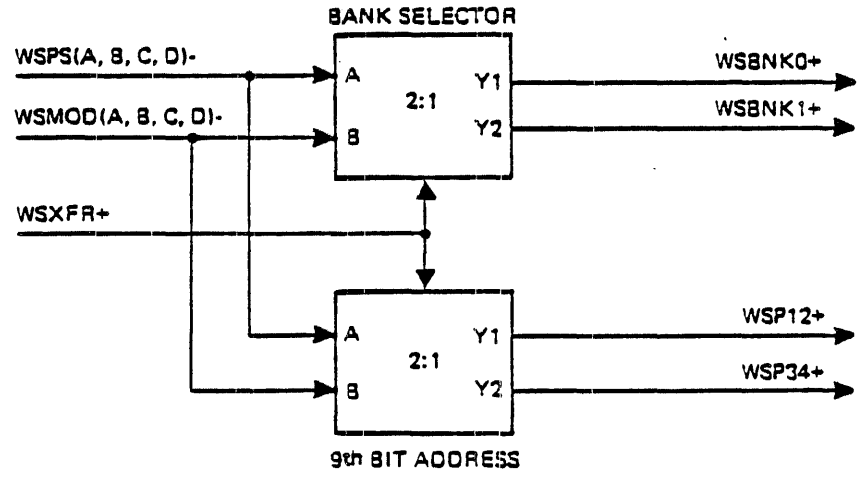


Figure 4-5. Page Selector

4.3.6 I/O Address Detector

This circuit detects the WCS II device address on the I/O bus. One of three address pairs is used for each WCS II module in a system. An address pair consists of an even and odd address designated 7X and 7Y, where Y equals 1, 3 or 5 and X equals 0, 2, or 4, respectively. Selection of an address pair is made by means of switches. When the function ready signal FRYX-1 goes low, WSFY7E+ and WSFY70+ are generated for the even and odd addresses, respectively. The I/O bus function bits EB0n-1(6, 7, 8) are also decoded to produce WSKFn-(0 through 7).

The WCS system reset (WSYR- low) can be generated by one of two sources:

a. An I/O instruction (WCS II initializing, WSEB11+ and WSFY7E+).

b. I/O bus system reset (SYRT-1).

4.3.7 Transfer Control

The transfer-control logic implements input and output transfers between the WCS II and processor. An input transfer (WSDTI+ high) uses the odd device address WSFY70+, and transfers WCS II data or CCS address to the processor.

There are two types of output transfers: output-control and output-data. The output-control transfer (WSKDF+ high) uses the even device address WSFY7E+ to initiate a WCS II function such as a branch to a CCS, or selection of a control store address. The output-data transfer (WSDTO+ high) uses the odd device address and causes data from the processor to be written into a control store that was selected by the previous output-control transfer.

4.3.8 Module Selector

The WCS II module that transfers data (odd device address) over the I/O bus is selected by the previous output-control transfer (even device address). The module selector decodes I/O bits WSEBn+(00 through 12) into page numbers. If conditions are met for setting the WSIOS+ flip-flop, the WCS II module is selected. Signal WSKD7E-, which clocks the WSIOS+ flip-flop, also clocks control store selection data WSKF (3,4) into the write enable circuits for future reference during transfers. The control store selection data is decoded from I/O data bits WSEBn+(13 through 15) into four functions WSKF (0, 1, 2, 3)-.

4.3.9 Four-to-One Data Multiplexor

The four-to-one data multiplexor shown in figure 4-6 selects 16-bit portions, called sector outputs, of the CCS data word as directed by the address counter outputs WSAS0- and WSAS1-. The CCS data word is divided into 16-bit portions to meet I/O bus transfer requirements. Table 4-1 shows the selection of input data according to states of the address counter.

4.3.10 Two-to-One Data Multiplexor

The two-to-one data multiplexor selects 16-bit data words for the I/O bus from either the four-to-one multiplexor or the option-input multiplexor. The selected data WSDn+(00 through 15) are applied to the I/O bus drivers.

4.3.11 Clock Generator

The clock generator supplies the clock used for the processor and the WCS II (the oscillator on the processor board is jumper clipped out of the processor timing circuit in systems containing a WCS II). Clock signal WSFKL+ is sent to the WCS; this is the inverted clock signal TCLKC- which is sent to the processor.

Table 4-1. Four-to-One Data Multiplexor (Input) and Write Strobe (Output)

Addr. Counter		Data Inputs	Write Strobe
WSAS1-	WSAS0-	Selected	Decoded
L	L	WSB (00 through 15)+	WSWE1+
L	H	WSB (16 through 31)+	WSWE2+
H	L	WSB (32 through 47)+	WSWE3+
H	H	WSB (48 through 63)+	WSWE4+

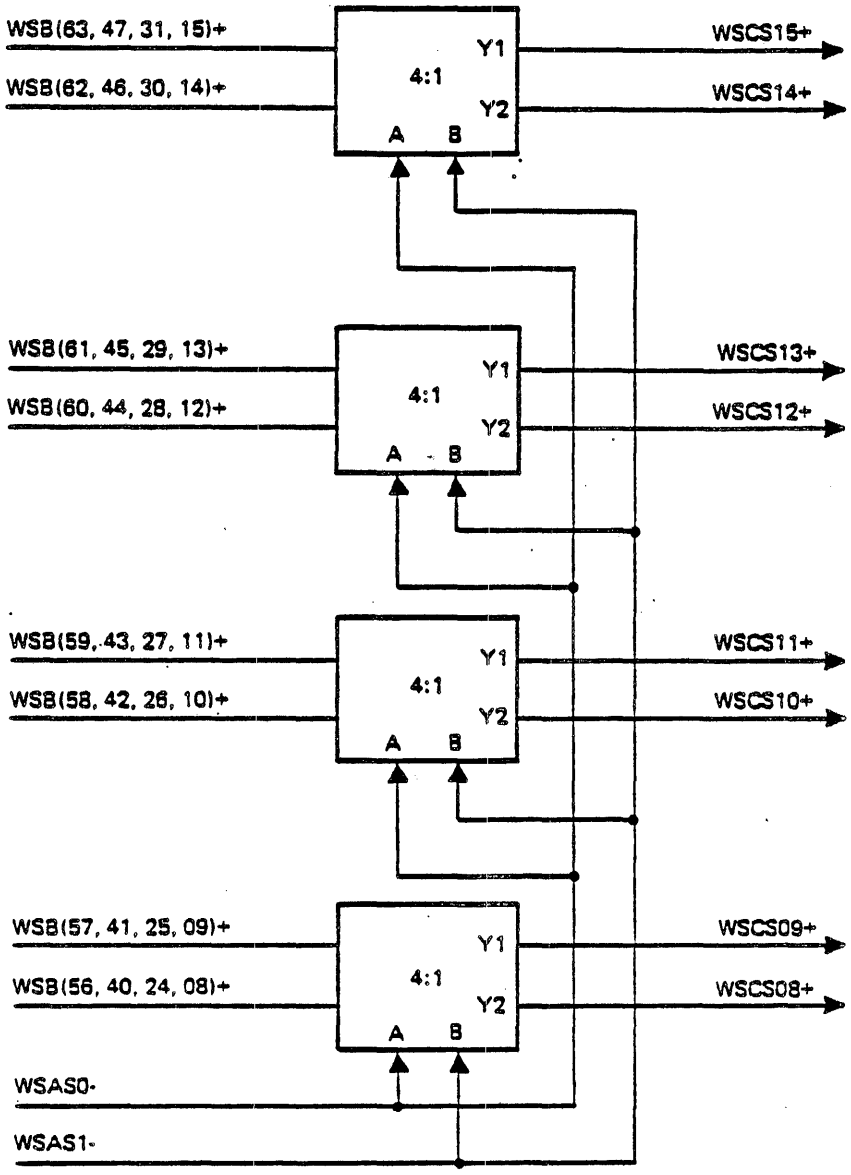


Figure 4-6. Four-to-One Data Multiplexor (Page 1 of 2)

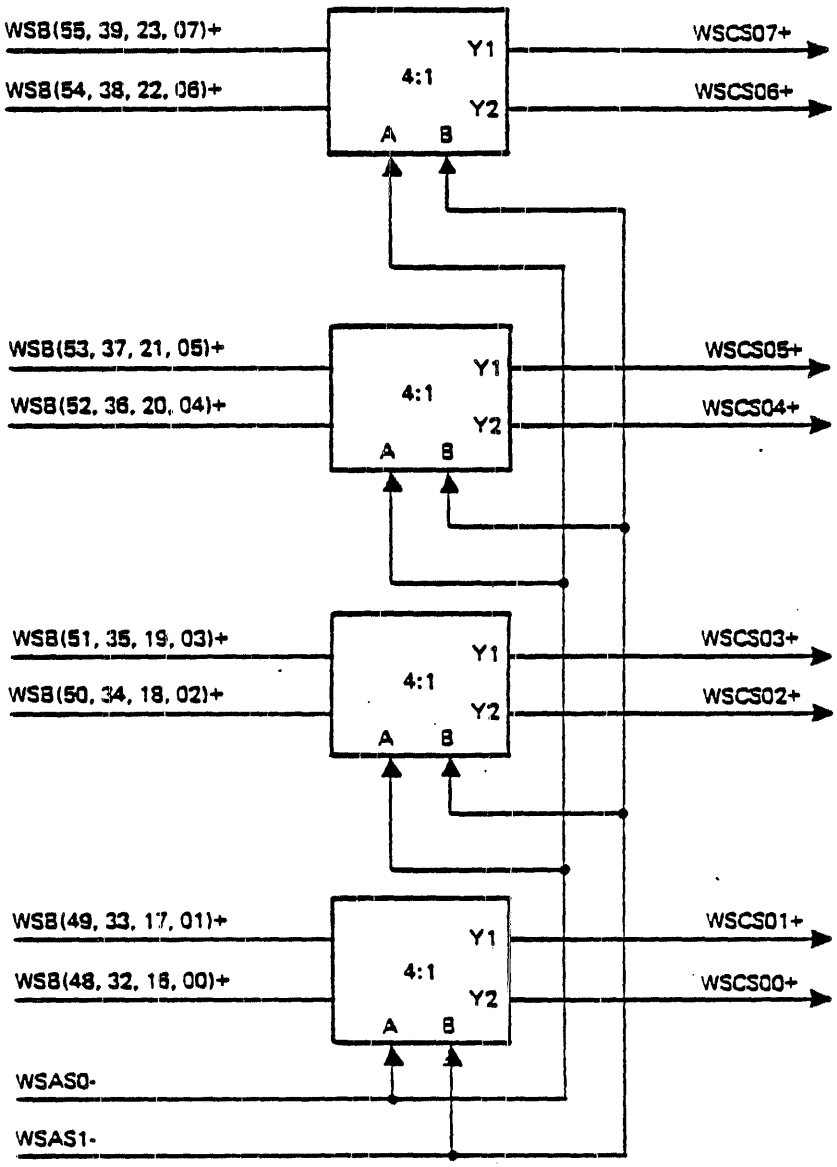


Figure 4-6. Four-to-One Data Multiplexor (Page 2 of 2)

When access is made from the WCS II, the clock is interrupted for one-half cycle to allow for the longer times that are required. This changes the microinstruction execution time of the processor from 165 nanoseconds to 190 nanoseconds. With signal WSHCK+ high, a low WSRAM- or WSCAENB+ causes an extended third phase of the processor cycle. With signal WSKL3+ high, a low WSPSEL- or WSIBS- causes an extended fourth phase of the processor cycle. The extended fourth phase allows execution of a page-jump or BCS instruction from the read-only control store in the processor.

4.3.12 Clock Control

The clock control circuit provides full and half-clock functions synchronized with the processor full-clock MCDFC-. The clock control circuit generates one sequence of clock functions for each processor full-clock received.

4.3.13 CCS Output Buffer

The CCS output buffer provides gate buffering for the CCS output data WSBn+(00 through 63). When buffer enabling signals WSBIEN- and WSBIE- are low, all 64 bits are transferred through the buffer. When the enabling signals are high, the tristate buffer output becomes a high impedance so that it can be controlled by the processor or another WCS II module. Buffer output bits CBIn+ (00 through 63) are routed to three locations: 64 bits go to the processor, bits 4 through 15 are looped back into the sub-routine stack, while other bits loop back to the WCS II control buffer.

4.3.14 Control Buffer

The control buffer duplicates portions of the control store buffer in the processor. On the trailing edge of every processor full clock (WSDFCK-), data from a CCS in the WCS system or from the processor control store are loaded into the control buffer. Output signals from the control buffer are used to process page-jump operations, special micro functions, and stack-return references.

4.3.15 Page-Branch Decoder

The page-branch decoder decodes the five types of microword page-branches as follows:

a. Branch with memory control (WSMBR- low) is decoded when: T field contains 00, S field contains binary 10, and WSGF2+ is high (bit 2 of G field is set).

b. Branch without memory control (WSMBR- low) is decoded when: T field contains 00, S field contains 00, and IM field contains 0011.

c. Branch/push (WSPSH- low) is decoded when: T field contains 00, S field contains 00, IM field contains 1101, and WA1+ is high (bit 1 of A field is set).

d. Branch/pop (WSPOP- low) is decoded when: T field contains 00, S field contains 00, IM field contains 1101, WSAF2+ is high (bit 2 of A field is set), and WSSD00+ is low (bit 0 of B field is set).

e. Branch/delete is decoded the same as branch/pop except WSSD00+ is high (bit 0 of B field is reset).

WSPSEL- goes low to indicate one of the above page-branching operations is being performed. A low CPAD- is sent to the processor, preventing the TS field from being an input to the next control-store address.

4.3.16 64K Mode Control

The 64K mode control circuit allows addressing of up to 64K of main memory by enabling memory address bit 15 (WS65K+) onto the memory address bus. Bit 15 is connected to the A or B memory port by the two switch configuration WSMA- and WSMAP-.

With WS65K+ (bit 15) connected:

a. When DMA or PMA request memory, memory address bit 15 is released to override the CPU 32K memory configuration.

b. When the etch 513E1-2 is removed, WRAM- is not applied. This allows 64K addressing from the processor control store or any WCS II module when the 65KMDE+ flip-flop (in the 64K-mode control circuit) is set.

c. With the jumper etch installed, WSRAM- is applied, causing 64K addressing from only WCS II when the WS65K+ flip-flop is set.

The WS65K+ flip-flop is set and reset as follows:

a. The flip-flop is set when: IM field contains 1101, S and T fields contain 00, and M field contains 1.

b. The flip-flop is reset when: IM field contains 1101, S and T fields contain 00, and WSCF1+ is high (bit 1 of C field is set).

4.3.17 Memory Lockout Control (Hog Mode)

The memory lockout control prevents the processor's main memory from being accessed on the opposite port by other devices. A lockout request (WSHOG+), generated in the memory lockout circuit, is set and reset as follows:

a. The lockout request is set (WSHOG+ high) when: S and T fields contain 00, IM field contains 1101, and WSCF0+ is high (bit 0 of C field is set).

b. The lockout request is reset (WSHOG+ low) when: S and T fields contain 00, IM field contains 1101, and WSAF0+ is high (bit 0 of A field is set).

When the lockout request is set, the next memory acknowledgement signal (YDNMA+ or YDNMB+) from memory port A or B sets a flip-flop causing the lockout signal WSMHG+ to go high. WSMHG+ is steered to the memory port by the processor. If the processor is connected to memory port B, WSMHG+ is steered to the priority-modifier line MHMY- which inhibits all memory accesses on port A. If the processor is connected to memory port A, WSMHG+ is steered to the priority-modifier line MHMY- which inhibits all memory accesses on port B.

When the lockout request is reset, the lockout function is immediately cleared (WSMHG+ low). The lockout function is also cleared with reset signal WSYR-.

4.4 SUBROUTINE STACK CIRCUITS

The stack uses the last-in-first-out concept, which means the last address added to the stack is the first address to be removed from it. Adding an address to the stack is referred to as a push operation; removing an address from the stack is referred to as a pop operation. A stack pointer is provided to keep track of the last stack location used (i.e., stack location that contains an address).

The stack is a 16-level wrap-around stack. Figure 4-7 shows the circuits of the subroutine stack in block diagram form. Page numbers of the WCS II logic diagrams are shown in parentheses for each circuit block.

The subroutine stack can accommodate up to 16 addresses of CCS microinstructions. The addresses consist of 12 bits from the CCS output buffer CBIn+(04 through 15). When read out of the stack, the address bits are designated WSSTn+(00 through 11). A description of each circuit of the subroutine stack is provided in the following subsections.

NOTE: Because there are only three bit fields (WSST 11, 10, 9) for page-branch, a return from stack to page eight will be vectored to page zero (CPU ROM). Therefore, page eight cannot be returned from stack/pop operations.

4.4.1 Stack Buffer

The stack buffer transfers data CBIn+(04 through 15) from the bus of the CCS output buffer to data inputs WSSDn-(00 through 11) of the stack array. Loading of the stack buffer occurs at the end of the cycle.

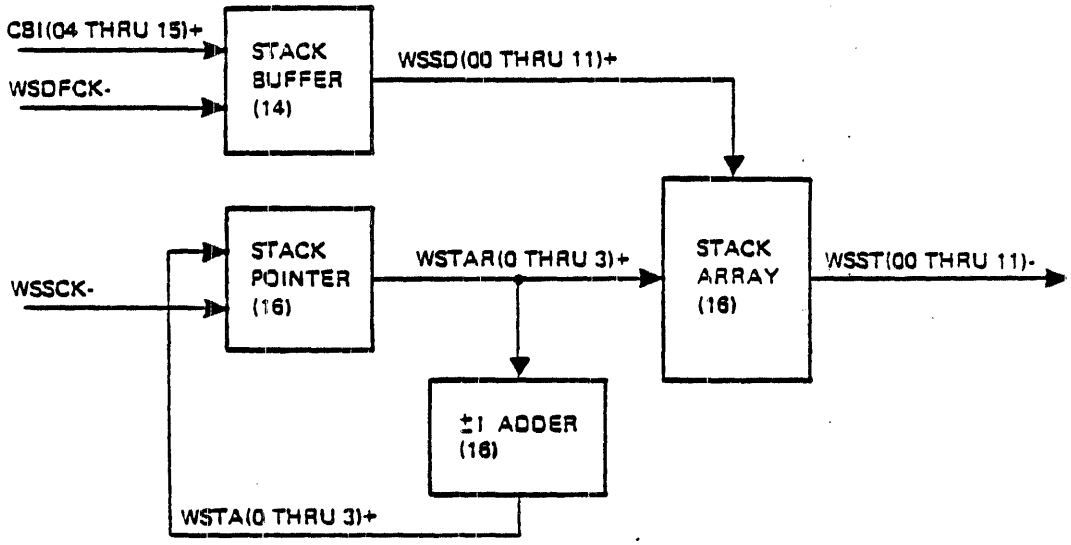


Figure 4-7. Subroutine Stack Block Diagram

4.4.2 Stack Array

The stack array contains sixteen 12-bit words (addresses). The words are addressed with the 4-bit code WSTARn+(0 through 3) from the stack pointer. When an address is applied along with a low (WSSDW-), input data WSSDN-(00 through 11) are loaded (push operation) into the addressed location. When an address is applied along with a high (WSSDW-), the addressed data WSSTn+ (00 through 11) are read (pop operation) from the array and sent to the CCS address selector.

4.4.3 Stack Pointer

The stack pointer consists of a 4-bit register and an adder. The reset signal, WSYR- initializes the stack pointer to location zero. A push operation causes the adder to be incremented by 1, while a pop operation causes the adder to be decremented by 1.

4.5 PSEUDO INSTRUCTION REGISTER

(Refer to WCS II logic points when reading this section.) The pseudo instruction register duplicates the function of the instruction buffer in the memory control section of the processor. Inputs to the register consist of memory data from either port A or B of the processor's main memory. Selection of port A or B data MYDAn-(00 through 15) or MYDBn-(00 through 15) is through the two-to-one multiplexor. A low loading signal MM11- from the memory control section of the processor enables the memory data to be clocked into the register on the positive-going transition of the memory acknowledgement signal YDNM-. The pseudo introduction register output data WSIBn-(00 through 15) are applied to the address decoding logic and decoder multiplexor. Bits zero through eight are applied to the decoder multiplexor to be transferred onto the CEADn-(0 through 8) bus during the operation of a BCS instruction. Bits eight through fifteen are decoded to detect a branching operation of an output-control transfer instruction.

4.6 WCS II TIMING DIAGRAMS

The following timing diagrams show the timing relationships between WCS II signals. The timing scale is not relevant to WCS II operations; however, the sequence of the signals is of the utmost importance.

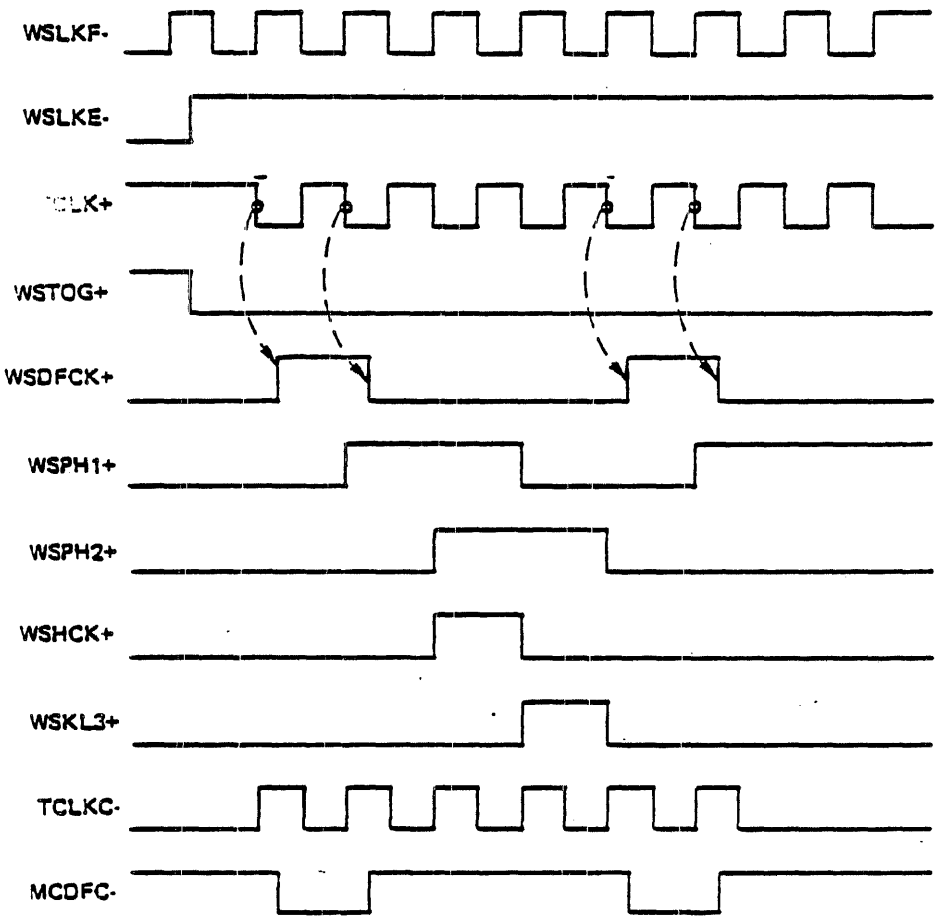


Figure 4-8. WCS II Clock Control (when WCS II is Not Selected)

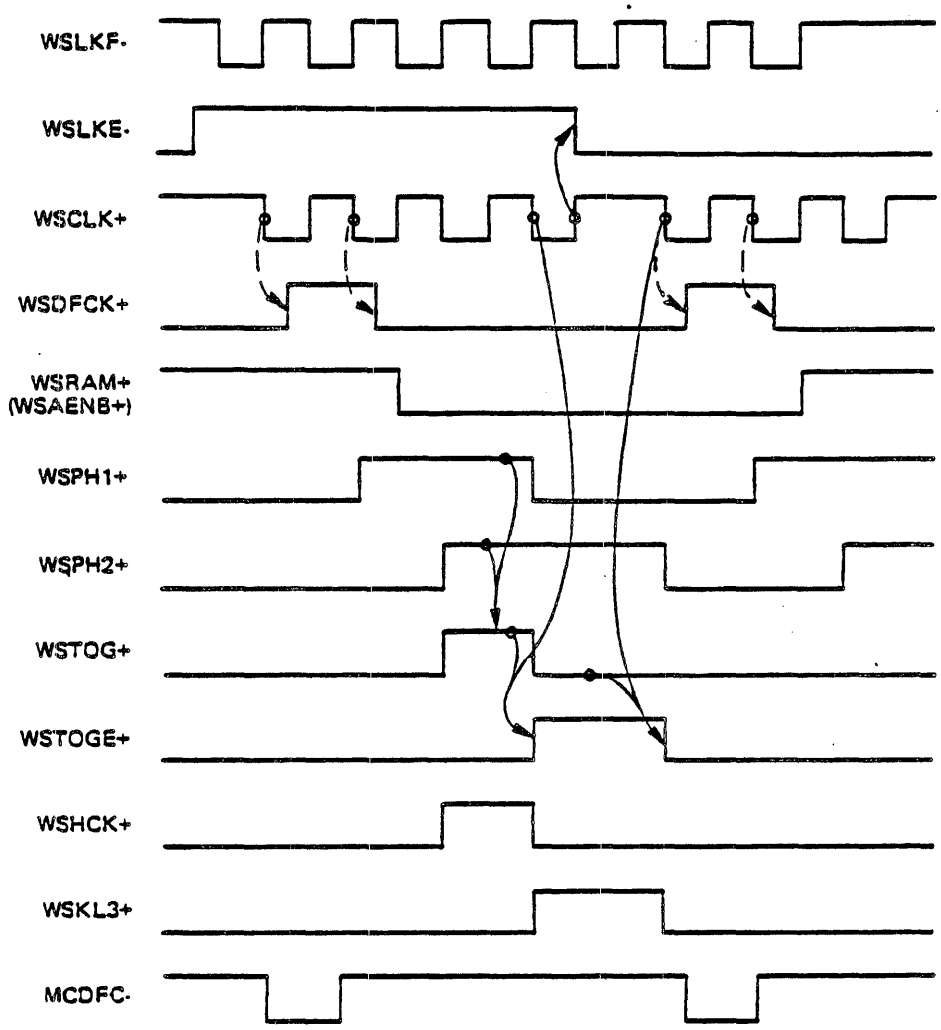


Figure 4-9. WCS II Clock Control (when WCS II is Selected via WSRAM+ or WSAENB+)

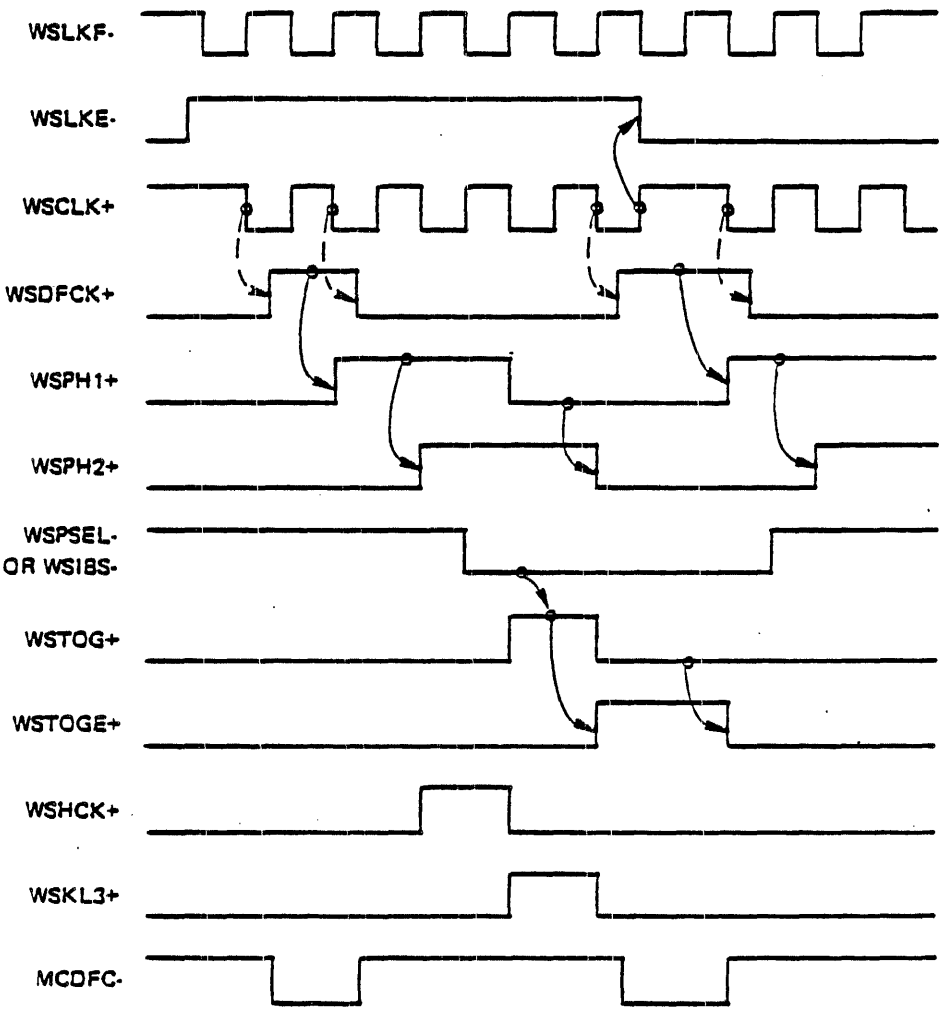


Figure 4-10. WCS II Clock Control (when WCS II is Selected via WSPSEL- or WSIBS-)

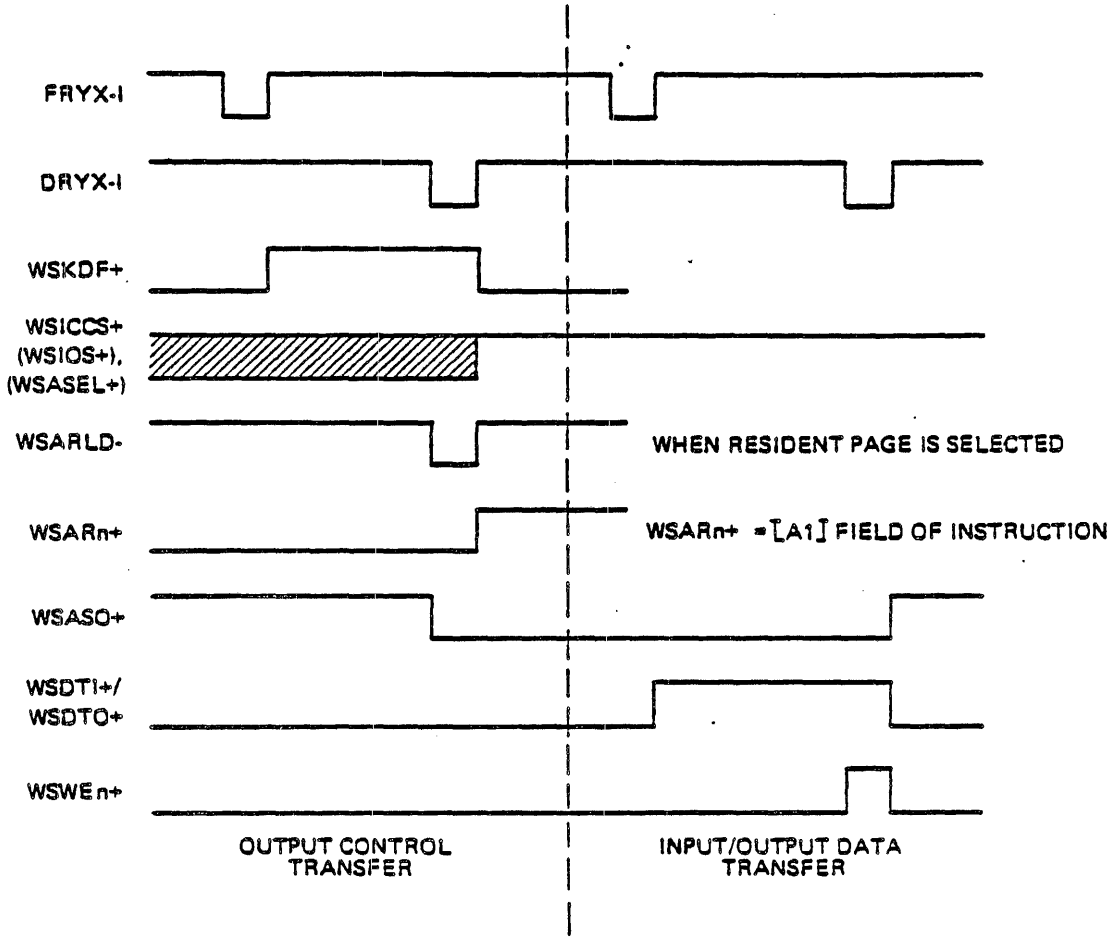


Figure 4-11. Programmed Input/Output Transfer to the Selected Control Store

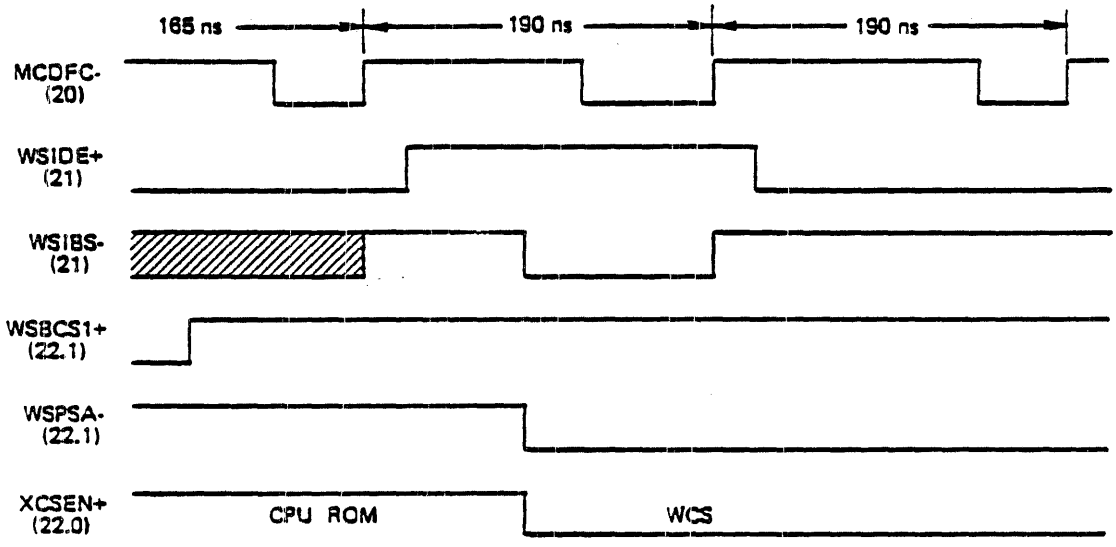


Figure 4-12. BCS Instruction

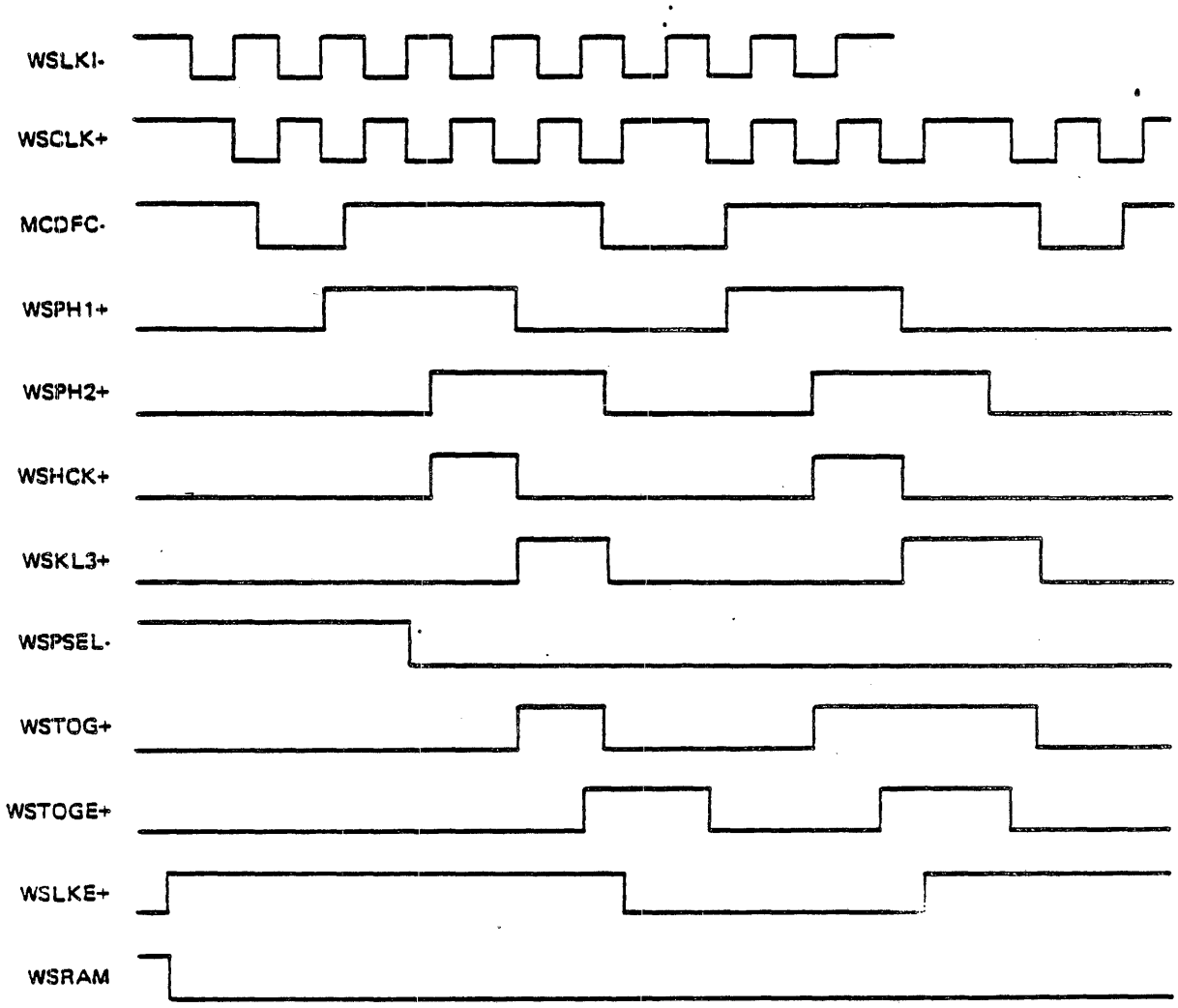


Figure 4-13. BCS Instruction/Page Branch from One WCS II to Another WCS II

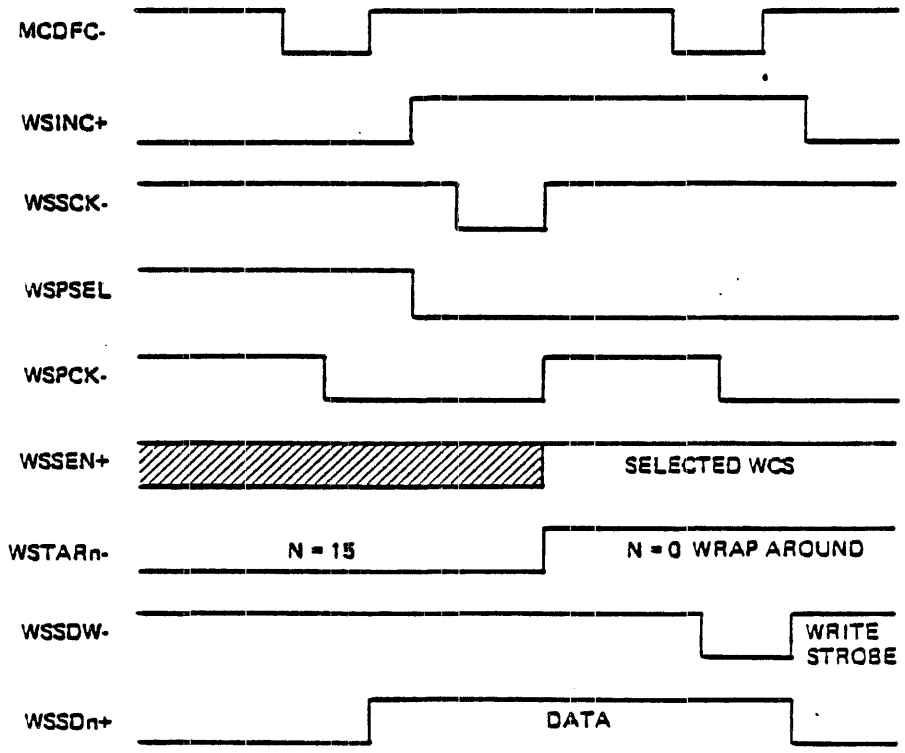


Figure 4-14. Branch/Push Microinstruction

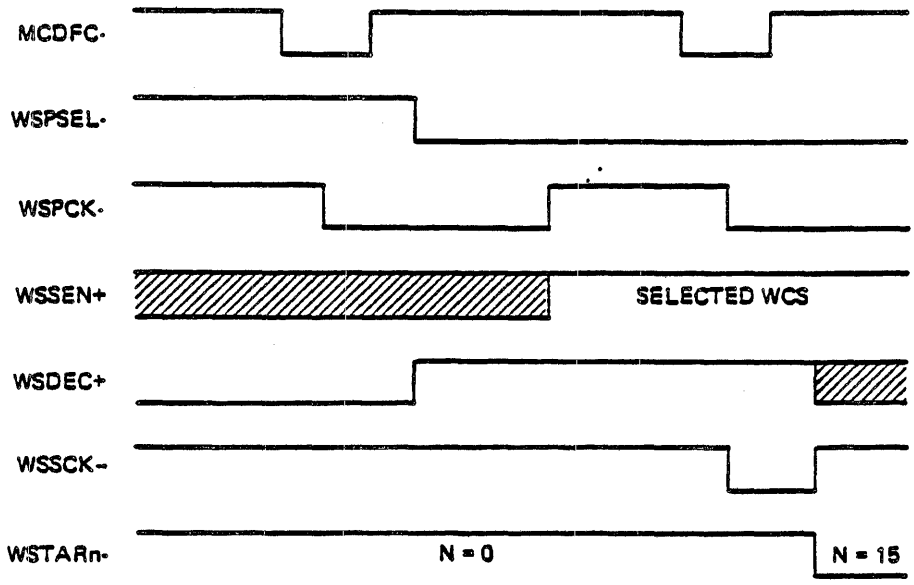


Figure 4-15. Branch/Pop Microinstruction

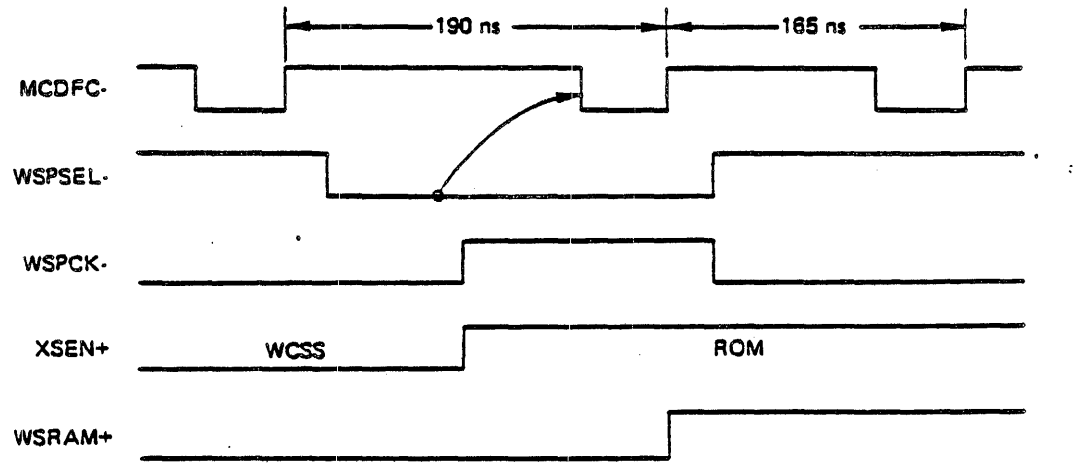


Figure 4-16. Page Branch from WCS II to Processor Instruction Decoder ROM

SECTION 5
MAINTENANCE

It is essential that maintenance personnel be familiar with the contents of this manual (especially section 4) before attempting WCS II troubleshooting. The SPERRY UNIVAC MAINTAIN III Test Program System (70/620 MAINTAIN III Manual 98A995207x) contains a WCS test program used to isolate a malfunction within the WCS II board. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following is a list of test equipment and tools recommended for WCS II maintenance:

1. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit or equivalent.

2. Multimeter, Triplett type 630 or equivalent.

3. Soldering iron, 15-watt pencil type.

5.2 CIRCUIT BOARD REPAIR

The WCS II board is a standard 2-layer PC board. The board is comprised of various IC (integrated circuit) chips which consist of: LSI memories, MSI multiplexors, SSI gates, decoders, registers, and flip-flops.

After it has been determined that circuit board repair is required, it is recommended that the nearest Sperry Univac customer service office be contacted to install a new circuit board in the system and return the faulty one to the factory for repairs. However, if the user decides to perform on-site repairs, extreme caution must be taken to avoid causing permanent damage to the circuit board. Approved repair procedures should be followed such as those described in document IPC-R-700A prepared by the Institute of Printed Circuits.

5.3 CIRCUIT COMPONENT IDENTIFICATION

The WCS II board utilizes the following methods for identifying component locations:

a. IC components are identified by location coordinates in the logic diagrams that appear inside the component's symbol. For example, a flip-flop designated C8 in the logic diagram is contained in the IC chip at location row C, column 8 on the board. (Coordinates are marked along the outer edges of the board.)

b. Discrete components are identified by location coordinates in the logic diagrams that appear near the component. These same reference designations appear on the circuit board adjacent to each component.

SECTION 6
MNEMONICS

This section contains an alphabetized list of WCS II signal mnemonics with their associated definitions. I/O bus signal mnemonics end with a -I; internal signals are prefixed by "WS".

Plus (+) or minus (-) signs are included at the end of each write control store mnemonic. The plus sign indicates the signal is at a high logic level (2.4V-5V) when its function is being performed. The minus sign indicates the signal is at a low logic level (0V-.5V) when its function is being performed. A signal that is a logical inversion of another uses the same mnemonic with an opposite sign; these signals are the complements of each other.

Mnemonic	Definition
CAEN+	When false (low), disables the instruction decoder in the processor
CBIn+	CCS output buffer bits 00 through 63
CEADn-	CCS address bits 00 through 8 from processor
CIDIO+	Signal BCS execution
CID00+	Signal BCS execution
CPAD-	Signal page-branch to processor
EBnn-I	I/O bus data bits 0 through 15
MM11+	Loading signal for pseudo instruction register
RCLKC-	Clock signal sent to processor
SERX-I	I/O bus sense line
SYRT-I	I/O system reset
WS65K+	Enable signal for the 64K mode control
WSAnn-	CCS address bits 0 through 9
WSABnn+	Address bits (0 through 8) input to CCS address buffer
WSAENB+	True if decoder ROM in processor is active
WSARn+	WCS II address register, bits 0 through 8
WSARE-	Selects WCS II address register

Mnemonic	Definition
WSARLD-	Loads WCS II address register
WSASn-	Sector counter bits 0, 1 selects CCS sector
WSASEL+	Stored CCS address selection
WSBCS1+	Enable BCS instruction strobe
WSBCSE+	Decoded BCS instruction signal
WSBIE-	Enables 56 most significant bits (08 through 63) of CCS output buffer
WSBIEN-	Enables 8 least significant bits (0 through 7) of CCS output buffer
WSBNK0+	Selects CCS lower 1K words
WSBNK1+	Selects CCS upper 1K words
WSBSY+	WCS II busy sense data
WSDEC+	Decoded stack-pop operation
WSDFCK	Processor full clock received
WSDT0+	Output data transfer strobe
WSDT1+	Enable data input to processor through I/O bus
WSEBnn+	Input data bits (00 through 15) to CCS
WSENA-	Enable CEADn- buffer
WSFY7E+	WCS II even address during FRYX-1 time
WSFY70+	WCS II odd address during FRYX-1 time
WSHCK+	Half-clock time synchronized with processor
WSIBnn-	Pseudo I-register bits (00 through 15)
WSIBS-	Decoded BCS instruction strobe
WSICCS+	Goes low to select CCS address; goes high to select CCS output
WSIDE+	Processor decoder timing
WSINC+	Decoded stack push operation
WSIOS+	Stores page selected for I/O

Mnemonic	Definition
WSKFn-	Output control transfer function (n=0,1,3,4)
WSKD7E-	I/O select clock
WSKL3+	Phase 3 of full clock cycle
WSMA-	Selects memory port A
WSMAP-	Enable map function
WSMCK+	Memory control clock for 64K or hog line
WSMHG+	Enable signal for memory hog mode control
WSMSEL+	WCS II module select over I/O
WSP12+	WCS II module page 1 and 2 most significant address bit
WSP34+	WCS II module page 3 and 4 most significant address bit
WSPCK+	Page-branch select clock
WSPH1-	First phase of WCS II microcycle clock
WSPH2-	Second phase of WCS II microcycle clock
WSPRE-	Selects precharge to CEADn-
WSPSEL-	Decoded page-branch microinstruction
WSSCK+	Stack pointer clock
WSSDnn+	Input data bits (00 through 15) to stack
WSSDW	Write strobe for stack
WSSEN+	WCS II control store is selected
WSSTnn-	Output data bits (00 through 15) from stack
WSSTK-	True, selects stack outputs (WSSTnn-); false, selects CEADn-, to address CCS
WSTARn-	Stack pointer register bits 0 through 4
WSWEn+	Write strobes (1 through 4) to CCS sectors
WSXFR+	Input or output data transfer through I/O instructions

Mnemonic	Definition
WSYR-	WCS II reset
XCSEN+	Goes low when WSSEN+ is high to disable control store in the processor