COFY No.

UNIVAC II

ANALYSIS OF INSTRUCTIONS

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UNIVAC II

ANALYSIS OF INSTRUCTIONS

VOLUME III

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1. GENERAL .

The "Analysis of Instructions" manual contains three sections relevant to the analysis and understanding of the routines performed by the computer. These sections include 1) a format which relates the discrete operations of each sequence by description, and with the corresponding control Function Table (FT) signal, in such a manner that the time of occurrence of each operation is clearly delineated; 2) a roster of the computer routines by code with the Function Table signals as they appear with regard to time of occurrence in the routine; and 3) a list of the Function Table signals with pertinent information concerning each signal.

The basic period in the performance of an instruction routine is the Program Counter (PC) step. Depending on the complexity of the routine, the number of PC steps varies: only one is required to conclude many instructions, while sixteen are required for the division, D, routine. Each PC step is comprised of two distinct cycles, the Time-out (TO) cycle and the Time-on cycle (exceptions to this occur in the division, multiplication, and shift routines). Timeout is always one minor cycle (91 pulse times) in duration. Time-on, however, exists for as long a period as is necessary to complete the operations required during a particular PC step. Time-out provides time for the FT signals to become fully alerted and to perform some operations that require no FT signals. Time-on determines the life of the FT signals and, therefore, is essentially the time in which the operations to be performed during a PC step are accomplished.

The Function Table signals provide most of the control necessary to accomplish the computer routines. Each FT signal provides a unique function, the proper combination of which enables the computer to execute the various instructions. There are 101 discrete FT signals. For purposes of identification these are numbered, the numbers ranging between 100 and 861. The appropriate FT

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signals are alerted by a signal generated from the proper combination of the instruction character code and the PC step during which the routine produced by the FT signal is to occur. A descriptive presentation of the FT signal decoding is made in Figure 1, page 91.

The PC steps and the FT signals provide the basis for the instruction analysis. Subroutines occurring in the proper sequence produce the routines specified by the instructions.

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- 2. GLOSSARY OF ABBREVIATIONS AND SYMBOLS.
 - AOC All Ones Checker
 - BC Binary Counter
 - BCI The binary counter which controls the order, right-hand or lefthand, of reference to a word in register I.
 - BCM The binary counter which controls the order, right-hand or lefthand, of reference to a word in main memory.
 - BCO The binary counter which controls the order, right-hand or lefthand, of reference to a word in register O.
 - BIR Backward Interlock Release signal
 - BP Backward Pick-up signal
 - CC The Control Counter
 - Comp Comparison
 - CR1 The 91 pulse register of the Control Register
 - CR2 The 42 pulse register of the Control Register
 - CT Conditional Transfer
 - CU The Cycling Unit
 - CY The Cycle Counter
 - EP Ending Pulse
 - FF Flip-flop
 - FIR Forward Interlock Release signal

FIR-BIR The Uniservo tape is in the First Block condition.

FT Function Table

- FTIC The Function Table Intermediate Checker
- FTOC The Function Table Output Checker
- HSB The High-Speed Bus
- IER The multipl<u>IER</u> signal
- IER-OR A signal used by both multiplication and division routines
- IO-INT Input-Output Interlock checker

- IOS Interrupted Operation Switch
- IRG Interlock Release Gate output
- IRP Interlock Release Pulse
- LE Leading Edge
- LM Left-hand section of the main memory
- LSB Least Significant Bit
- LSD Least Significant Digit
- M₁ The half-word magnetic switching core register of the rM Bit Plane Control
- M₂ The half-word magnetic-switching core register of the rI Bit Plane Control
- M₃ The half-word magnetic-switching core register of the rO Bit Plane Control
- M₄ The half-word magnetic-switching core register of the Output Distributor
- min Minuend
- MQC The Multiplier-Quotient Counter
- MQC-FT The output matrix of MQC
- MSD Most Significant Digit
- MTO Memory Time Out
- N₅ The seven-bit magnetic-switching core register of the Input Distributor
- nS Uniservo selector signal
- OE Odd-Even
- OEC Odd-Even Checker
- OR The divisOR signal
- PC The Program Counter
- PPI Pulses per inch
- PS Pulse Stretcher
- rA The one-word A register

rF	The one-word F register
rI	The 60-word I register
rL	The one-word L register
rM	The 2000 word main memory register
RM	The right-hand section of the main memory
r0	The 60-word 0 register
RP	The Read Pick-up signal
rW	The ten-word W register
rX	The one-word X register
rZ	The 60-word Z register
S/NS	Signal/No Signal
S1CP	The subtraction signal generated in CP (operate the complementer)
SIX	The subtraction signal generated in MQC (operate the complementer)
S2	Switch inputs to AA
SC	Supervisory Control
SCI-CR	Type into CR from SC
sub	Subtrahend
t	t pulses - any of the timing pulses in the 91 pulse cycle generated by CU
TE	Trailing Edge
то	Time-Out
TRI	Input section transfer pulses
TRO	Output section transfer pulses
TT	Test Terminal
TZ	Through-zero
WP	The Write Pick-up signal
Z	Decimal zero
()	The contents of
>	Transmit
m	A word in rM from which a specified field is selected
rx	Duplicated X register

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3. ANALYSIS OF INSTRUCTIONS.

This section provides a detailed analysis of the various computer instructions. The instructions are listed in the binary order of the character code which specifies the routine. This code occupies the first-character position of the six-character instruction word. Where the instruction routine is altered by a symbol in the second character position, the routine is again presented but with the modification that has been made. An "F" in the second instruction character "field selects" the operand as it is transferred from storage and an "H" returns the results of an operation to storage. For the input-output operation, the second instruction character addresses the Uniservo required by the instruction. Other instruction modifications are made by use of the second instruction character. These are described in the instructions concerned. The "m" section of the instruction word designates an address in storage.

The analysis of each instruction begins with a shorthand presentation of the routine to be accomplished by the instruction. Following this, and organized with regard to time of occurrence; i.e., by PC steps, is a description of the functions performed by the various FT signals that are alerted for the routine. In the column to the right of the page is the number of the FT signal described. Appropriate footnotes are supplied where clarification or qualification is necessary.

The CY outputs of β , β COMPUTE, γ , and δ and the RETAIN INSTRUCTION routine are not considered instructions, but they do control FT signals as part of the automatic internal programming of the computer. The routine accomplished during these cycles and the FT signals required to perform these routines are described on page 7.

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INSTRUCTION	DESCRIPTION	FT
Beta	$(CC) + 1 \rightarrow CC; LH (CR) \rightarrow SR Distributor$	
	Set up adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect CR1 to SR Distributor Line. Connect CC to adder min input, Cycling Unit	714 435 \ 204 _
	(000000 000001) to adder sub input. Clear CC and read the sum from the unbarred adder to CC. (Transfer to CC ends t12 of TO). Supply reset pulse to Overflow FF's	212 737
Beta Computer	(m)>CR	
	Operate rM address exceeded and preset checkers. Set BCM to RM Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M1 cores. Strobe, rM sense amplifiers. Develop Serialize Pulse. Connect HSB to CR, and clear CR. Set MTO. Supply EP. (rM address sets up at t7 of Beta TO, unless over- flow occurs, which delays Set-up until t35, thereby setting SR to Z ¹ s.)	860 827 429 428 820 821 824 201 4 825 206
Gamma	$RH(CR) \longrightarrow SR$ Distributor; Execute LH instruction.	
	Connect CR1 to CR2. (LH Instruction sets up at t7 of Gamma TO)	203 203K
Delta	$RH(CC) \longrightarrow SR$ Distributor; Execute RH Instruction.	
	Connect CC to SR via CR2#.	850
	#RH Instruction is set up at t7 of Delta TO.	203K
RETAIN INSTRUCTION	Repeat routine performed during a selected CY cycle. eta cycle: Inhibit FT 201, 204,212, 435	
	Alert FT 850 y cycle: Inhibit FT 203 Alert FT 204, 203K and specified in- struction FT signals	
	8 cycle: Inhibit FT 850 Alert FT 203, 203K and specified in- struction FT signals	

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INSTRUCTION	DESCRIPTION	FT
A O m 1.	<pre>(m) → rX; (rX) + (rA) → rA. Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M1 cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rX. Operate rX clear gate. Set MTO. Step PC, set TO.</pre>	860 827 429 428 820 821 824 126 120 825 214
то	Compare (rA) and (rX).	NONE
2.	Operate adder for eleven-place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. (Transfer to rA ends at t12 of TO) Supply EP.	160 435 125 109 206
	*If decimal carry occurs from eleventh digit position, set Overflow FF. If second instruction digit is a minus sign, overflow sets Stop FF.	

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INSTRUCTION	DESCRIPTION	FT
AFm	$(\underline{m}) \longrightarrow rX; (rX) + (rA) \longrightarrow rA$	
1.	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M1 Cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rX. Operate rX, clear gate. Operate extract circuit in rF.* Set MTO. Step PC, Set TO. *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	860 827 429 428 820 821 824 126 120 193 825 214
то	Compare (rA) and (rX).	NONE
2.	Operate adder for eleven-place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA (Transfer to rA ends at t12 of TO). Supply EP.	160 435 125 109 206
	*If decimal carry occurs from eleventh digit position, set Overflow FF.	

INSTRUCTION	DESCRIPTION	FT
AHm	$(m) \longrightarrow rX; (rA) + (rX) \longrightarrow rA; (rA) \longrightarrow m$	
1.	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M ₁ Cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rX. Operate rX clear gate. Set MTO. Step PC, set TO.	860 827 429 428 820 821 824 126 120 825 214
то	Compare (rA) and (rX).	NONE
2.	<pre>Operate adder for eleven-place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer to rA ends at t12 of TO.) Step PC, set TO. *If decimal carry occurs from 11th digit position, set Overflow FF. + FT206 is present, but its effect is suppressed by FT214.</pre>	160 435 125 109 214 206+
то З.	Operate rM address exceeded and preset checkers. Connect rA to HSB. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M1 Cores. Develop Staticize Pulse. Set MTO. Supply EP.	860 100 429 428 826 823 825 206

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INSTRUCTION	DESCRIPTION	FT
BOm	<pre>(m) → rA, rX. Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M1 Cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rA. Operate rA clear gate. Connect HSB to rX. Operate rX clear gate. Set MTO. Supply EP.</pre>	860 827 429 428 820 821 824 105 101 126 120 825 206
BFm	 (m) → rA, rX. Operate rM address exceeded and preset checkers. Preset BCM to RM. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M₁ Cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate Extract Circuit in rF.* Connect HSB to rA. Operate rA clear gate. Connect HSB to rX. Operate rX clear gate. Set MTO. Supply EP. *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is re-placed with a decimal zero. 	860 827 429 428 820 821 824 193 105 101 126 120 825 206

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INSTRUCTION	DESCRIPTION	FT
COm	<pre>(rA)→ m; Z→ rA Operate rM address exceeded and preset checkers. Connect rA to HSB. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M1 Cores. Develop Staticize Pulse. Operate rA clear gate. Connect CU (000000 000000) to rA. Set MTO. Supply EP.</pre>	860 100 429 428 826 823 101 108 825 206
DOm	(m) → rA; (rA) ÷ (rL) → rA rounded, rX unrounded	d 1
1.	Operate rM address exceeded and preset checker. Preset BCM to RM. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M ₁ Cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rA. Operate rA clear gate. Delete rX input to comparator, connect HSB.* Delete rA input to comparator, connect rL.* Preset BC-120 in MQC to non-complement position, thus alerting the non-complementing gates between MQC and MQC-FT. Clear MQC to decimal zero. Set MTO. Step PC, set TO. *Sign comparison is performed between (rA) and (rL).	860 827 429 428 820 821 824 105 101 152 151 138 825 214

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INSTRUCTION	DESCRIPTION	FT
D O m TO		
2. T0	Retain results of sign comparison in comparator. Operate rA clear gate. Operate rA left shift path (including sign).* Insert decimal zero in LSD position of rA. Set Repeat FF. Step PC, set TO. *Shifting (rA) left deletes sign digit.	159 101 103 171 226 214
3.	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replac- ing sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop FF's after each time on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input clearing rA and transferring sum from adder to rA. Gate non-complement output of BC-120 as S1X signa to operate the complementer in adder sub, thus (rL) are subtracted from (rA)	159 714 435 188 109
	(rL) are subtracted from (rA). Gate non-complement output of BC-120 to operate Improper Division Detector in MQC.* Step MQC at t2 following each subtraction until the Through- Zero signal is developed, at which time generate OR CYCLE.# If rA or rX comp error occurs, set TO at follow- ing t1.	145 246
	*If rL \geq rA, Improper Division occurs at t2 of the eleventh minor cycle of PC-3.	
	#The Through-Zero signal indicates that the sub- traction produced a negative remainder, since no decimal carry occurred from the twelfth-digit po- sition. At the beginning of the OR CYCLE, the MOC-FT will contain a digit equal to the number of sub- tractions performed minus the one which produced the Through-Zero signal.	

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INSTRUCTION DESCRIPTION FT Delete functions of FT109, except HSB to adder DOm IER-OR+1 sub input. Inhibit the transfer of (rL) to HSB. IER-OR+2 Delete functions of FT435. OR CYCLE IER-OR+3 Operate rA and rX clear gates. IER - OR - 2Operate rX left shift path. Transfer quotient digit from MQC-FT to LSD position of rX. Clear MQC to decimal zero. Step BC-120 to alert the complement gates connecting the MOC and MOC-FT. (MOC-FT now reads nines complement of MOC.) Step PC at end of OR-CYCLE. OR-1 Operate rA left shift path inserting a decimal zero in the LSD position OR-2Inhibit alerting signal to complementer and the stepping signal to the MQC. OR+1 NOTE: Those FT signals present on PC-3 are also present during the OR CYCLE, performing the same functions except as noted above. 4. 159 Retain results of sign comparison in comparator. Operate adder for twelve-place addition. 714 Operate adder OE and sum comparison checkers. 435 Connect rL to HSB. Transfer (rL) to HSB, replacing sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop FF's after each Time-on minor cycle if IOS is in "One Addition". 188 Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to 109 rA. Step MQC at t2 following each addition, until the Through-Zero signal is developed, at which 145 time, generate OR CYCLE.* If rA or rX comp error occurs, set TO at follow-246 ing tl. *The Through-Zero signal indicates that the addition produced a positive number, since a decimal carry occurred from the twelfth digit position. At the beginning of the OR CYCLE, the MQC will contain a digit equal to the number of additions performed, minus the one which produced the Through-Zero signal, and the MQC-FT will contain the nines complement of this digit.

INSTRUCTION	DESCRIPTION	FT
D O m 5 thru 13	All OR CYCLES are identical. All odd PC-Steps are identical to PC-3. All even PC-Steps are identic to PC-4. Initially the divisor, (rL), is subtrac from the shifted dividend, (rA), until the Throug Zero signal occurs, indicating that the remainder in rA is negative. During the OR CYCLE (rA) and (rX) are shifted lef one digit position, a decimal zero is inserted in the LSD position of rA and the quotient digit from the MQC-FT is inserted into the LSD position of r (rL) is then added to (rA) until the Through-Zero signal occurs, in this case indicating that (rA) is again positive; and an OR CYCLE occurs. (rL) is thus alternately subtracted and added to (rA) as the quotient is built up in rX. Followin each OR CYCLE, PC is advanced.	e al ted h- t to m X.
14	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checker. Connect rL to HSB; transfer (rL) to HSB, replac- ing sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop after each time on minor cycle; if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Step MQC at t2 following each addition, except when Through-Zero signal is developed at which time generate OR CYCLE. If rA, or rX comp occurs, set TO at following t1. Reset Repeat FF at end of OR CYCLE. Set TO at end of OR CYCLE.	159 714 435 188 109 145 246 228 244
OR CYCLE	Same as previous OR CYCLES, except that in addition: Reset Repeat FF. Set TO.	IER-OR-1 OR-1

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DESCRIPTION

INSTRUCTION	DESCRIPTION	FT
D O m TO		
15	 Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Operate rA clear gate.* Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Connect CU (round-off, 000000 000005) to adder min input. Step PC, set TO. *Operating rA's clear gate destroys the divide remainder and, consequently, nothing is read from rA to the adder min input. Thus the results of the addition are (rX) + (round-off)—>rA. 	159 714 435 101 125 109 111 214
TO		
16	Retain results of sign comparison in comparator. Operate rA clear gate. Operate right shift path of rA. Transfer sign from comparator to rA and rX. Operate rX clear gate. Operate right shift path of rX. Transfer sign from comparator to rA and rX, deleting the insertion of a decimal zero to rA. Supply EP.	159 101 106 120 123 161 206

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INSTRUCTION	DESCRIPTION	FT
DFm	(<u>m</u>)—>rA; (rA) : (rL)—>rA rounded, rX unrounde	d
1.	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M1 Cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rA. Operate rA clear gate. Operate Extract Circuit in rF.* Delete rA input to comparator, connect rL.# Delete rX input to comparator, connect HSB.# Preset BC-120 in MQC to non-complement position, thereby alerting the non-complement gates between MQC and MQC-FT. Clear MQC to decimal zero. Set MTO. Step PC, set TO. *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replace with a decimal zero. #Perform sign comparison between (rA) and (rL).	860 827 429 428 820 821 824 105 101 193 151 152 138 825 214
то		
2.	Retain results of sign comparison in comparator. Operate rA clear gate. Operate rA left shift path.* Insert decimal zero in LSD position of rA. Set Repeat FF. Step PC, set TO. *Shifting (rA) left deletes sign digit.	159 101 103 171 226 214

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INSTRUCTION	DESCRIPTION	FT
DFm		
TO		
3.	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replac- ing the sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop after each time on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Gate non-complement output of BC-120 as SIX signal to operate the Complementer on adder sub input, thus (rL) is subtracted from (rA). Gate non-complement output of BC-120 to operate the Improper Division Detector in MQC.* Step MQC t2 following each subtraction, until the Through- Zero signal is developed, at which time generate OR CYCLE.# If rA or rX comp error occurs, set TO at following tl. *If (rL) ≤ (rA), Improper Division occurs at t2 of the eleventh minor cycle of PC-3. #The Through-Zero signal indicates that the sub- traction produced a negative remainder, since no decimal carry occurred from the twelfth digit position. At the beginning of the OR CYCLE, the MQC-FT will contain a digit equal to the number of subtractions performed minus the one which produced the Through-Zero signal.	159 714 435 188 109 145 246
OR CYCLE	Delete Functions of FT109, except HSB to adder sub input. Inhibit the transfer of (rL) to HSB. Delete functions of FT435. Operate rA and rX clear gates. Operate rX left shift path. Transfer quotient digit from MQC-FT to LSD position of rX. Clear MQC to decimal zero. Step BC-120 to alert the complement gates connecting the MQC and MQC-FT. (MQC-FT now reads nines complement of MQC) Step PC at end of OR CYCLE. Operate rA left shift path, insert a decimal zero into the LSD position of (rA). Inhibit alerting signal to complementer and the stepping signal to the MQC. NOTE: Those FT signals present on PC-3 are also present during the OR CYCLE, performing the same functions except as noted above.	IER-OR+1 IER-OR+2 IER-OR+3 IER-OR-2 OR-1 OR-2 OR+1

INSTRUCTION	DESCRIPTION	FT
DFm		
4.	 Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replacing the sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop FF's after each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA, and transfer sum from adder to rA. Step MQC at t2 following each addition, until the Through-Zero signal is developed, at which time generate OR CYCLE.* If rA or rX comp error occurs, set TO at following tl. *The Through-Zero signal indicates that the addition produced a positive number, since a decimal carry occurred from the twelfth digit position. At the beginning of the OR CYCLE, the MQC will contain a digit equal to the number of additions performed, minus the one which produced the Through-Zero signal, and the MQC-FT will contain the nines complement of this digit. 	159 714 435 188 109 145 246
5-13	All OR CYCLES are identical. All odd PC-Steps are identical to PC-3. All even PC-Steps are identical to PC-4. Initially the divisor, (rL), is subtracted from the shifted dividend, (rA), until the Through-Zero signal occurs, indicating that the remainder in rA is negative. During the OR CYCLE, (rA) and (rX) are shifted one digit position left, a decimal zero is in- serted into the LSD position of rA and the quotient digit from the MQC-FT is inserted into the LSD position of rX. (rL) is then added to (rA) until the Through-Zero signal occurs, in this case indicating that (rA) is again positive, and an OR CYCLE occurs. (rL) is thus alter- nately subtracted and added to (rA) as the quotient is built up in rX. After each OR CYCLE, PC is stepped.	

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INSTRUCTION	DESCRIPTION	FT
DFm		
14.	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checker. Connect rL to HSB. Transfer (rL) to HSB, replac- ing the sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop FF's after each Time-on minor cycle if IOS is in	159 714 435
	"One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Step MQC at t2 following each addition, until the	188 109
	Through-Zero signal is developed, at which time generate OR CYCLE. If rA or rX comp error occurs, set TO at following	145
	Reset Repeat FF at end of OR CYCLE. Set TO at end of OR CYCLE.	228 224
OR CYCLE	Same as previous OR CYCLES, except that in addi- tion:	
	Reset Repeat FF. Set TO.	IER-OR-1 OR-1
то		
15.	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checker. Operate rA clear gate.* Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Connect CU roundoff, (OOOOOO OOOOO5) to adder min input. Step PC, set TO.	159 714 435 101 125 109 111 214
	*Operating rA's clear gate destroys the divide remainder and, consequently, nothing is read from rA to the adder min input. Thus the results of the addition are: $(rX) + (round-off) \rightarrow rA$.	

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INSTRUCTION	DESCRIPTION	FT
DFm		
то		L
16	Retain results of sign comparison in comparator. Operate rA clear gate. Operate right shift path of rA. Transfer sign from comparator to rA and rX. Operate rX clear gate. Operate right shift path of rX. Transfer sign from comparator to rA and rX, delet ing the insertion of a decimal zero to rA. Supply EP.	159 101 106 120 123
EOm	<pre>(rF) Odd digits extracts (m)→rA. Operate rM address exceeded and preset checker. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, Set M₁ Cores. Strobe rM sense amplifiers. Develop Serialize Pulse Connect HSB to rA. Operate rA clear gate. Operate extract circuit in rF.* Delete CU (000000 000000) input to extract cir- cuit and connect rA.* Set MTO. Supply EP. *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is deleted and the corresponding digit in rF is a trans- ferred to the HSB.</pre>	860 827 429 428 820 821 824 105 101 193 832 825 206

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INSTRUCTION	DESCRIPTION	FT
EFm	(rF) Even Digits Extracts (m)→rA; (<u>rA</u>)→m	
1.	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M ₁ cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rA. Operate rA clear gate. Operate extract circuit in rF.* Complement the operation of the extract circuit.* Delete CU (000000 000000) input to extract cir- cuit and connect rA. Set MTO. Step PC, set TO. *Transfer is controlled by (rF).If the LSB of the corresponding digit in rF is a binary one, the digit from rM is read onto the HSB. If the LSB is a binary zero, the digit from rM is deleted and the corresponding digit from rA is transferred to HSB. + FT206 is present, but its effect is suppressed by FT214.	860 827 429 428 820 821 824 105 101 193 831 832 825 214 206+
TO		0/0
2.	Operate rM address exceeded and preset checkers. Connect rA to HSB. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, Set M ₁ cores. Develop Staticize Pulse. Set MTO. Supply EP.	860 100 429 428 826 823 825 206
FOm	(m)→rF	
	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M_1 cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rF, and operate rF clear gate. Set MTO. Supply EP.	860 827 429 428 820 821 824 190 825 206

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DESCRIPTION

INSTRUCTION	DESCRIPTION	FT
GOm	$(rF) \rightarrow m$ Operate rM address exceeded and preset checkers. Connect rF to HSB. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M ₁ cores. Develop Staticize Pulse. Set MTO. Supply EP.	860 192 429 428 826 823 825 206
HOm	<pre>(rA)→m Operate rM address exceeded and preset checkers. Connect rA to HSB. Operate HSB-OEC. Operate HSB-AOC Set rM Read FF, set M₁ cores. Develop Staticize Pulse. Set MTO. Supply EP.</pre>	860 100 429 428 826 823 825 206
IOm	<pre>(rL)→m Operate rM address exceeded and preset checkers. Connect rL to HSB. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M₁cores. Develop Staticize Pulse. Set MTO. Supply EP.</pre>	860 187 429 428 826 823 825 206
J O m	<pre>(rX)→m Operate rM address exceeded and preset checkers. Connect rX to HSB. Operate HSB-OEC. Operate HSB-AOC. Set rM read FF, set M₁ cores. Develop Staticize Pulse. Set MTO. Supply EP.</pre>	860 125 429 428 826 823 825 206

INSTRUCTIONS	DESCRIPTION	FT
КО	$(rA) \longrightarrow rL; Z \longrightarrow rA.$	
	Connect rA to HSB.	100
	Operate rA clear Gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect HSB to rL, operating rL clear gate.	185
	Operate HSB-OEC.	429
	Supply FD	420
	Suppry Er.	200
LOm	(m)>rL, rX	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M ₁ cores	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	195
	Connect HSD to FL, operate FL clear gate.	105
	Connect HSB to rX input gate.	120
	Supply EP	206
	Set MTO.	825
LFm	(<u>m</u>)→rL, rX	
	Operate TM address eveneded and protect sheekers	860
	Set BCM to BM	827
	Operate HSB-OEC	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate extract circuit in rF.*	193
	Connect HSB to rL, operate rL clear gate.	185
	Operate rX clear gate.	120
	Connect HSB to rX.	126
	Succlus ED	020
	Supply Er.	200
	*Transfer is controlled by (rF). If the LSB of	
	the digit from rM is read onto the HSR If the	
	ISB is a binary one the digit from rM is re-	
	placed with a decimal zero.	
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DESCRIPTION

FT

INSTRUCTION	DESCRIPTION	FT
MOm	(m) \rightarrow rX; (rL) x (rX) \rightarrow rA (rounded) 11 MSD rX 11 LSD	
1	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M ₁ cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate rA clear gate. Connect CU (000000 000000) to rA. Connect rL to adder sub input. Transfer (rL) to adder, replacing sign digit with a decimal zero. Connect rA to adder min input, clear rA, and read sum from the adder to rA. (Transfer ends at t12 of TO.)* Operate adder OE and sum comparison checkers. Connect HSB to rX. Operate rX clear gate. Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC and MQC-FT. Set MTO. Step PC, set TO. *If decimal carry occurs from eleventh digit	860 827 429 428 820 821 824 101 108 110 113 435 126 120 139 825 214
	position, set Overflow flip-flop.	
ТО		
2	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL)	714 435
	to adder, replacing the sign digit with a decimal zero. Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at	110
	t12 of TO) Step PC, set TO.	113 214

INSTRUCTION	DESCRIPTION	FT
MOm		
то		
3	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with a decimal	714 435
	zero. Delete rA input to comparator and connect rL.* Connect rA to adder min input, clear rA, and	110 151
	read sum from adder to rA. (Transfer ends at t12 of TO.) Step PC, set TO.	113 214
	*rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	
ТО		
4.	Store results of sign comparison in comparator. Operate adder OE and sum comparison checkers. Operate HSB-OEC. Operate HSB-AOC. Connect rA to HSB Operate rA clear gate. Connect CU (000000 000000) to rA. Connect HSB to rF, operate rF clear gate. Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC and set the nines complement of the digit into the MQC. Connect rA to adder min input, clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Operate right shift path in rX Operate rX clear gate. Set Repeat flip-flop. Step PC,set TO.	159 435 429 428 100 101 108 190 112 113 123 120 226 214
	NOTE: At the completion of PC-4, rA contains the roundoff, rL contains the multiplicand, rF contains three times the multiplicand, rX contains the multiplier shifted one digit right, the MQC con- tains the nines complement of LSD shifted out of rX, and the comparator contains the sign of the product. The sign position of rX is vacant.	5

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DESCRIPTION

FT

INSTRUCTION	DESCRIPTION	FT
M O m TO		
	Store results of sign comparison in comparator. Operate adder for twelve-place addition.	159 714
5	Operate adder OE and sum comparison checkers. Connect rL and rF to the ≥ 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in One Addition. Connect HSB to adder sub input, rA to adder min input, clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is ≤ 3 , reset the ≥ 3 FF, which transfers (rL) to HSB, and supply one stepping pulse to MQC. If digit ≥ 3 , set the ≥ 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit $= 0$, set IER and IER-OR FF's at following t ₂ . If rA or rX comp error occurs, set TO at following t ₁ . NOTE: At the beginning of the operation, the MQC- FT will contain the LSD from rX. If the digit is ≥ 3 , three times the multiplicand (rF) is added to the partial product in rA, and the MQC is step- ped three times, thus reducing the digit in the MQC-FT by three. If the digit in the MQC-FT is < 3, the multiplicand (rL) is added to the par- tial product in rA and the MQC is stepped once, thus reducing the digit in the MQC-FT by one. Successive additions occur until the digit in the MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the orig- inal LSD of (rX).	435 188 109 147

INSTRUCTION

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DESCRIPTION

FT

MOm		
IER (PC-5)	Operate the right shift path of rA and insert a decimal zero into the sign position of (rA). Operate the right shift path of rX, transferring LSD of (rX) to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the comple- ment of the LSD from (rX) in the MQC. Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER-CYCLE. Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. Inhibit min input to the algebraic adder. (Delete the functions of FT109) Inhibit the adder OE and sum comparison checkers. (Delete the functions of FT435)	IER-6 IER-4 IER-0R-2 IER-3 IER-1 IER-0R+2 IER+1 IER-0R+1 IER-0R+3
6 through 13	Same as PC-5.	
14	Same as PC-5 except for one addition FT signal which is used to set TO at the end of the IER CYCLE.	244
ТО		
15	Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE.	
PC 15	Insert sign into sign position of (rA) and (rX).	161 & IER
164	Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. Reset Repeat FF. Supply EP.	-5 149 & IER-1 228 & IER-0R-1 215 & IER-2

INSTRUCTION	DESCRIPTION	FT
MFm	$(\underline{m}) \longrightarrow rX; (rL) \times (rX) \longrightarrow rA (rounded) 11 MSDrX 11 LSD$	
l	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M1 cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate rA clear gate. Operate extract circuit in rF.* Connect CU (000000 000000) to rA. Connect rL to adder sub input, transfer (rL) to adder, replacing sign digit with a decimal zero. Connect rA to adder Min input, clear rA, and read the sum from the adder to rA. (Transfer ends at t12) + Operate adder OE and sum comparison checkers. Connect HSB to rX. Operate rX clear gate. Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC to the MQC-FT. Set MTO. Step PC, set TO. *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero. +If decimal carry occurs from eleventh digit position, set Overflow flip-flop.	860 827 429 428 820 821 824 101 193 108 110 113 435 126 120 139 825 214
то		
2	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with a decimal zero. Connect rA to adder min input, clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Step PC set TO	714 435 110 113 214

INSTRUCTION

UNIVAC II

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FT

DESCRIPTION

r		
M E	Operate adder for twelve-place addition	714
M F M	Operate adder OF and sum comparison checkors	135
2	Connect rI to sub input of adder Transfer (rI)	100
ა	to adden replacing the sign digit with a	
	to adder, replacing the sign digit with a	110
	decimal zero.	110
	Delete rA input to comparator, connect rL.*	151
	Connect rA to adder min input, clear rA, and	
	read sum from adder to rA. (fransfer ends	
	at t12 of TO.)	113
	Step PC, set TO.	214
	*rX is connected to the comparator via a	
	direct path. A sign comparison is performed	
	between (rL) and (rX), and the sign of the	
	product is stored in the comparator.	
ТО	· · · · · · · · · · · · · · · · · · ·	
4	Store results of sign comparison in comparator.	159
	Operate adder OE and sum comparison checkers.	435
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect rA to HSB.	100
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect HSB to rF, operating rF Clear gate.	190
	Connect CU (050000 000000) to adder sub input.	
	Transfer the LSD of (rX) to the MOC, setting	
	the nines complement of the digit into the MOC.	112
	Connect rA to Min input. clear rA. and read	
	sum from adder to rA. (Transfer ends at t12	
	of TO.)	113
	Operate right shift path in rX.	123
	Operate rX clear gate.	120
	Set Repeat flip-flop.	226
	Step PC, set TO.	214
	NOTE: At the completion of $PC-4$ rA contains	
	the roundoff rI contains the multiplicand	
	The roundorr, it contains the multiplicand,	
	Tr contains the multiplican shifted are dist	
	ra contains the multiplier shifted one digit	l
	right, the myt contains the nines complement	[
	of LSD shifted out of rX, and the comparator	
	contains the sign of the product. The sign	
	position of rX is vacant.	
L		

INSTRUCTION	DESCRIPTION	FT
MFm		
ТО		
5	Store results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL and rF to the \geq 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and	159 714 435
	Stop FF's at end of each Time-on minor cycle if IOS is in"One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MOC-FT). If digit is < 3, reset the	188 109
	\geq 3 FF, which transfers (rL) to HSB, and supplies one stepping pulse to MQC. If digit is \geq 3, set the \geq 3 FF, which transfers (rF) to HSB, and supplies three stepping pulses to MQC. If digit is = 0, set IER and IER-OR FF's at following t2. If rA or rX comp error occurs, set TO at following t1.	147 246
	NOTE: At the beginning of the operation, the MQC- FT will contain the LSD from rX. If the digit is ≥ 3 , three times the multiplicand (rF) is added to the partial product in rA, and the MQC is steppe three times, thus reducing the digit in MQC-FT by three. If the digit in MQC-FT is < 3, the multi- plicand (rL) is added to the partial product in rA and MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in the MQC-FT is reduced to zero, at whic time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	d h
IER CYCLE	Operate the right shift path of ra and insert a decimal zero into the sign position of (rA). Operate the right shift path of rX transferring LSD of rX to the MOC distributor line.	IER-6 IER-4
	Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement	IER-OR-2
	of the LSD from (rX) in the MQC. Transfer LSD of (rA) to the MSD position of rX and	IER-3
	step PC at the end of the IER CYCLE.	IER-1
	for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the	IER-OR+2
	stepping of the MQC. Inhibit the min input of the algebraic adder. (Delete the functions of FT109) Inhibit the adder odd-even and the adder sum	IER+1 IER-OR+1
	comparison checkers. (Delete the functions of FT435)	TED ODLQ

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INSTRUCTION	DESCRIPTION	FT
MFm		
6 through 13	Same as PC-5.	
14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
то		
15	Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE.	
PC 15	Insert sign into sign position of (rA) and (rX).	161 Plus
IER CYCLE	Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC.	149 Plus
	Reset Repeat FF.	$\frac{12R-1}{228 \text{ Plus}}$
	Supply EP.	1ER-0R-1 215 Plus 1FR-2
NOm	$-(m) \longrightarrow rX; (rL) X (rX) \longrightarrow rA (rounded) 11 MSD's rX 11 LSD's$	104 2
1	<pre>Operate rM address exceeded and preset checkers. Set BCM to RM Operate HSB-OEC Operate HSB-AOC Set rM Read FF, set M1 cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate rA clear gate. Connect CU (000000 000000) to rA. Connect rL to adder sub input. Transfer (rL) to adder, replacing sign digit with a decimal zero Connect rA to adder min input. Clear rA and read the sum from the adder to rA. (Transfer ends at t12 of TO)* Operate adder OE and sum comparison checkers. Connect HSB to rX, via sign reversal gates.+ Operate rX clear gate. Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC to MQC-FT. Set MTO. Step PC, set TO. *If decimal carry occurs from eleventh digit position, set Overflow flip-flop. +The sign reversal gates complement the LSB and</pre>	860 827 429 428 820 821 824 101 108 110 113 435 153 120 139 825 214
	+The sign reversal gates complement the LSB and check pulse of the sign digit during transfer to p	x .

INSTRUCTION	DESCRIPTION	FT
N O m TO		
2	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer	714 435
	(rL) to adder, replacing sign digit with a decimal zero. Connect rA to adder min input. Clear rA, and read sum from adder to rA (Transfer	110
	ends at t12 of TO.) Step PC, set TO.	11 3 21 4
то		
3	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with a	714 435
	decimal zero. Delete rA input to comparator, connect rL.* Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at	110 151
	t12 of TO.) Step PC, set TO.	113 214
	*rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	

UNIVAC II

DESCRIPTION

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INSTRUCTION	DESCRIPTION	FT
NOm		
то		
4	 Store results of sign comparison in comparator. Operate adder OE and sum comparison checkers Operate HSB-AOC. Operate HSB-AOC. Connect rA to HSB. Operate rA clear gate. Connect CU (000000 000000) to rA. Connect HSB to rF, operate rF clear gate. Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC and set up the nines complement of the digit into the MQC Connect rA to min input of the adder. Clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Operate right shift path in rX. Operate rX clear gate. Set Repeat flip-flop. Step PC, set TO. NOTE: At the completion of PC-4, rA contains the roundoff. rL contains the multiplicand, rF contains three times the absolute value of the multiplicand, rX contains the multiplier shifted one digit right, the MQC contains the nines complement of LSD shifted out of rX, and the comparator contains the sign of the product. The sign position of rX is vacant. 	159 435 429 428 100 101 108 190 112 113 123 120 226 214
UNIVAC II

INSTRUCTION

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DESCRIPTION

0 m		
то		
5	Store results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers Connect rL and rF to the \geq 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset the \geq 3 FF, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is \geq 3, set the \geq 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit is = 0, set IER and IER-OR FF's at following t2. If rA or rX comp error occurs, set TO at following t1. NOTE: At the beginning of the operation, the MQC- FT will contain the LSD from rX. If the digit is \geq 3, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the digit in MQC-FT by three. If the digit in the MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Succes- sive additions occur until the digit in MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	159 714 435 188 109 147 246

35

INSTRUCTION

UNIVAC II

DESCRIPTION

NOm		
IER CYCLE (PC-5)	Operate the right shift path of rA and insert a decimal zero into the sign position of (rA). Operate the right shift path of rX, transferring LSD of rX to the MQC distributor line.	IER-6 IER-4
	Operate rA and rX clear gates.	IER-OR-2
	of the LSD from rX in the MQC.	IER-3
	Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. Inhibit the transfer of (rL) and the decimal	IER-1
	zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the step-	IER-OR+2
	ping of the MQC. Inhibit the min input to the algebraic adder. (Delete the functions of FT109)	IER + 1 IER-OR+1
	Inhibit the adder odd-even and the adder sum	
	FT435.)	IER-OR+3
6 through 13	Same as PC-5.	
14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
ТО		
15	Same as PC-5 except for four additional FT signal which are used during PC-15 IER CYCLE.	S
PC 15 IER CYCLE	Insert sign into sign position of (rA) and (rX).	161 plus JFR-5
	Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC.	149 plus
	Reset Repeat FF.	228 plus
	Supply EP.	1ER-OK+1 215-plus IER-2

UNIVAC II

INSTRUCTION

DESCRIPTION

NFm	$-(\underline{m}) \rightarrow rX;$ (rL) X (rX) \rightarrow rA (rounded) 11 MSD's rX 11 LSD's	
1	<pre>Operate rM address exceeded and preset checkers. Set BCM to RM Operate HSB-OEC Operate HSB-AOC Set rM Read FF, set M₁ cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate rA clear gate Connect CU (000000 000000) to rA. Connect rL to adder sub input, transfer (rL) to adder, replacing sign digit with a decimal zero. Connect rA to adder min input. Clear rA, and read the sum from the adder to rA. (Transfer ends at t12 of TO.)* Operate adder OE and sum comparison checkers Operate extract control circuit in rF.+ Connect HSB to rX, via sign reversal gates.# Operate rX clear gate. Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC to MQC-FT. Set MTO. Step PC, set TO. *If decimal carry occurs from eleventh digit position, set Overflow flip-flop. #The sign reversal gates complement the LSB and check pulse of the sign digit during transfer to rX. +Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero</pre>	860 827 429 428 820 821 824 101 108 110 113 435 193 153 120 139 825 214
L		

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INSTRUCTION

DESCRIPTION

NFm		
TO		
2	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder. replacing sign with a decimal	714 435
	zero. Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at	110
	tl2 of TO.) Step PC, set TO.	113 214
Т0		
3	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL)	714 435
	to adder, replacing the sign with a decimal zero. Delete rA input to comparator, connect rL.* Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at	110 151
	tl2 of TO.) Step PC, set TO.	113 214
	*rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	

INSTRUCTION

UNIVAC II

DESCRIPTION

T-		
NFm		
		L
10		
4	Store results of sign comparison in comparator.	159
_	Operate adder OE and sum comparison checkers.	435
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect rA to HSB.	100
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect HSB to rF, operate rF clear gate.	190
	Connect CU (050000 000000) to adder sub input.	
	Transfer the LSD of (rX) to the MQC, set up the	
	nines complement of the digit into the MQC.	112
	Connect rA to min input of the adder. Clear rA,	
	and read sum from adder to rA。 (Transfer ends	
	at tl2 of TO.)	113
	Operate right shift path in rX.	123
	Operate rX clear gate.	120
	Set Repeat flip-flop.	226
	Step PC, set TO.	214
	NOTE: At the completion of PC-4 rA contains	
	the roundoff, rL contains the multiplicand, rF	
	contains three times the absolute value of the	
	multiplicand, rX contains the multiplier shifted	
	one digit right, the MOC contains the nines complement	
	of ISD shifted out of rX. and the comparator contains	
	the sign of the product. The sign position of rX is	
	vacant.	
1 1		

INSTRUCTION

UNIVAC II

DESCRIPTION

NFm		
то		
5	Store results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL and rF to the \geq 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign digit with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and	159 714 435
	Stop FF's at end of each Time-on minor cycle if IOS, is in"One Addition".	188
	Connect HSB to adder sub input, rA to adder min	
	adder to rA. Sample (MQC-FT). If digit is < 3, reset \geq 3 FF, which transfers (rL) to HSB and supplies one step- ping pulse to MQC. If digit is \geq 3, set the \geq 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit is = 0, set IER	109
	and IER-OR FF's at following t2.	147
	If rA or rX comp error occurs, set TO at	0.4/
	NOTE: At the beginning of the operation, the MQC- FT will contain the LSD from rX. If the digit is ≥ 3 , three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the MQC-FT by three. If the digit in MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	240

INSTRUCTION

UNIVAC II

DESCRIPTION

Operate the right shift path of rA and insert a NFm decimal zero into the sign position. IER-6 IER CYCLE Operate the right shift path of rX transferring LSD of rX to the MQC distributor line. IER-4 (PC-5) Operate rA and rX clear gates. IER-OR-2 Clear MOC to binary zero and set up the complement of the LSD from (rX) in the MQC. IER-3 Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. IER-1 Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. IER-OR+2 Disconnect rF from the HSB and inhibit the stepping of the MOC. IER+1 Inhibit the min input to the algebraic adder. IER-OR+1 (Delete the functions of FT109) Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of (FT435.) IER-OR+3 6 Through Same as PC-5. 13 Same as PC-5 except for one additional FT signal 14 which is used to set TO at the end of the IER CYCLE. 244 TO Same as PC-5 except for four additional FT signals 15 which are used during PC-15 IER CYCLE. PC-15 IER CYCLE Insert sign into the sign position of rA and rX. 161 Plus IER-5 Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. 149 Plus IER-1 Reset Repeat FF. 228 Plus IER-OR-1 Supply EP. 215 Plus IER-2

UNIVAC II

INSTRUCTION

DESCRIPTION

POm	(m) \longrightarrow rX; (rL) X (rX) \longrightarrow rA = 11 MSD's, rX = 11 LSD's	
1	Operate rM Address exceeded and preset checkers. Set BCM to RM. Operate HSB-AOC. Operate HSB-OEC. Set rM Read FF, set M ₁ cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate rA clear gate. Connect CU (000000 000000) to rA. Connect rL to adder sub input, transfer (rL) to adder and replace sign digit of (rL) with a decimal zero. Connect rA to adder min input, Clear rA and read sum from adder to rA. (Transfer ends at t12 of TO.)* Operate adder OE and sum comparison checkers. Connect HSB to rX. Operate rX clear gate. Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC and MQC-FT. Set MTO. Step PC, set TO. *If decimal carry occurs from the eleventh digit position, set Overflow FF.	860 827 428 429 820 821 824 101 108 110 113 435 126 120 139 825 214
TO		
2	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder, transfer (rL) to adder, replacing the sign digit with a decimal	714 435
	zero. Connect rA to adder min input. Clear rA and	110
	Step PC, set TO.	214

INSTRUCTION

UNIVAC II

DESCRIPTION

F		
POm TO		
3	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder, transfer (rL)	714 435
	zero. Delete rA input to comparator and connect rL.*	110 151
	read sum from adder to rA. Step PC, set TO.	113 214
	*rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	
TO		
4	Store results of sign comparison in comparator. Operate HSB-OEC. Operate HSB-AOC. Connect rA to HSB. Operate rA clear gate. Connect CU (000000 000000) to rA. Connect HSB to rF and operate rF clear gate. Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC and set up the nines complement of the digit into the MQC. Operate right shift path in rX. Operate rX clear gate. Set Repeat FF. Step PC, set TO.	159 429 428 100 101 108 190 112 123 120 226 214
	NOTE: At the completion of PC-4, rA contains decimal zeros, rL contains the multiplicand, rF contains three times the multiplicand, and rX contains the multiplier shifted one digit right, the MQC contains the nines complement of the LSD shifted out of rX, and the comparator contains the sign of the product. The sign position of rX is vacant.	

ANALYSIS OF INSTRUCTIONS INSTRUCTION

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UNIVAC II

DESCRIPTION

	r	
°Om TO		
TO PC-5	Store result of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL and rF to the \geq 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset the \geq 3 FF, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is \geq 3, set the \geq 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit = 0, set IER and IER OR FF's at following t2. If rA or rX comp. error occurs, set to FF at fol-	159 714 435 188 109 147
	NOTE: At the beginning of the operation, the MQC-FT will contain the LSD from rX. If the digit is \geq 3, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the digit in the MQC-FT by three. If the digit in the MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in the MQC-FT by one. Successive additions occur until the digit in the MQC-FT is reduced to zero, at which time the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	246
IER PC-5	Operate the right shift path of rA and insert a decimal zero into the sign position. Operate the right shift path of rX, including the sign, transfer LSD of rX to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement of the LSD from rX in the MQC. Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the step- ping of the MQC. Inhibit the min input to the algebraic adder. (Delete the functions of FT109) Inhibit the adder odd-even and the adder sum com-	IER-6 IER-4 IER-0R-2 IER-3 IER-1 IER-0R+2 IER+1 IER-0R+1
	Inhibit the adder odd-even and the adder sum com- parison checkers. (Delete the functions of FT435.)	IER-(

UNIVAC II

INSTRUCTION

DESCRIPTION

FΓ

POm		
6 Through 13	Same as PC-5.	
PC-14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
IER	Insert sign into the sign position of (rA) and (rX). Inhibit the generation of a second IER CYCLE.	161 Plus IER-5
PC-15	in case a decimal zero is set up in the MQC.	149 Plus IER-1 228 Plug
	Supply EP.	IER-OR-1 215 Plus IER-2
P F m	$(\underline{m}) \longrightarrow rX; (rL) \chi (rX) \longrightarrow rA, 11 MSD's rX, 11 LSD's$	
1	Operate rM address exceeded and preset checkers.	860
	Set BUM to KM.	021
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M ₁ cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate rA clear gate.	· 101
	Connect CU (000000 000000) to rA. Connect rL to adder sub input. transfer (rL)	108
	to adder, replacing sign digit with a decimal zero. Connect rA to adder min input. Clear rA, and read	110
	the sum from the adder to rA. (fransfer ends at	110
	LIZ OI 10.)"	113
1	operate adder of and sum comparison checkers.	430
	Operate extract control circuit in rf.+	193
	Lonnect Hob to rA.	120
	Operate rX clear gate. Preset BC-120 to the complement state, thereby	120
	alerting the complement gates connecting the myc	120
	LO LAE MUU-FI.	137
	Set MIU.	025
	Step PC, set TO.	214
	*If decimal carry occurs from eleventh digit position, set Overflow flip-flop.	
	+Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is re- placed with a decimal zero.	

UNIVAČ II

STRUCTION	DESCRIPTION	FT
		73.6
PFm	Operate adder for twelve-place addition.	/14
TO	Compart ri to sub input of odder Transfer	400
10	(rl) to adder replacing sign digit with a	
2	decimal zero.	110
-	Connect rA to adder min input. Clear rA, and	
	read sum from adder to rA. (Transfer ends at	
	t12 of TO.)	113
	Step PC, set TO.	214
то		
3	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Connect rL to sub input of adder. Transfer	
	(rL) to adder, replacing the sign digit with	
	a decimal zero.	
	Delete rA input to comparator and connect rL."	151
	read sum from adder to rA (Transfer ands at	
	tl2 of TO)	113
	Step PC, set TO.	214
	*rX is connected to the comparator via a direct	
	path. A sign comparison is performed between (rL)	
	and (rX), and the sign of the product is stored	
	in the comparator.	
то		
4	Store results of sign comparison in computer.	159
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect rA to HSB.	100
	Operate rA clear gate.	
	Connect CU (UUUUUU UUUUUU) to FA.	100
	Connect CI (050000 000000) to adder sub input	170
	Transfer the $(SD of (rX))$ to the MOC and set up the	
5	nines complement of the digit into the MOC.	112
	Operate right shift path in rX.	123
	Operate rX clear gate.	120
	Set Repeat flip-flop.	226
	Step PC, set TO.	214
	NOTE: At the completion of PC-4, rA contains deci-	
	mal zeros, rL contains the multiplicand, rF contains	
	three times the multiplicand, rX contains the multi-	
	piler sniited one digit right, the MQC contains the	
	nines complement of the Lop Shilled Out of rA, the Comparator contains the sign of the product and the	
	comparator contarno the sign of the product, and the	

UNIVAC II

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INSTRUCTION	DESCRIPTION	FT
P F m TO 5	Store results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL and rF to the ≥ 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset ≥ 3 FF, which transfers (rL) to HSB and supplies one step- ping pulse to MQC. If digit is ≥ 3 , set the ≥ 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit is = 0, set IER and IER-OR FF at following t2. If rA or rX comp error occurs, set TO FF at following t1. NOTE: At the beginning of the operation, the MQC- FT will contain the LSD from rX. If the digit is ≥ 3 , three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the MQC-FT by three. If the digit in MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	159 714 435 188 109 147 246
P F m IER CYCLE (PC-5)	Operate the right shift path of rA, inserting a decimal zero into the sign position. Operate the right shift path of rX, transferring LSD of rX to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the comple- ment of the LSD from (rX) in the MQC. Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. Inhibit the transfer of (rL), and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. Inhibit the min input to the algebraic adder. (Delete the functions of FT10%) Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435.)	IER-6 IER-4 IER-0R-2 IER-3 IER-1 IER-0R+2 IER+1 IER-0R+1 IER-0R+1

INSTRUCTION

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UNIVAC II

DESCRIPTION

PFM		
6 through 13	Same as PC-5.	
14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
то		
15	Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE.	
PC-15	Insert sign in sign position of (rA), (rX).	161 Plus JER 5
IER CYCLE	Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. Reset Repeat FF. Supply EP.	149 Plus IER-1 228 Plus IER-OR-1 215 Plus IER 2
Qnm	If (rA) = (rL), Transfer control>m.	
1	Operate HSB-OEC. Operate HSB-AOC. Connect rL to HSB. Eanble comparator to perform equality comparison.* Delete rX input to comparator and connect HSB. If 2nd Instruction Digit "n" equals Conditional Transfer Breakpoint Selector setting, pass tl to set Stop FF. Step PC, set TO.	429 428 187 156 152 236 214
	<pre>*If (rA) = (rL), the Conditional Transfer FF is set at t5 of PC-2 TO.</pre>	
ТО		
2	Retain results of comparison in comparator. Operate HSB-OEC. Operate HSB-AOC. Connect CR and CU (000000 00) to HSB.* If Conditional Transfer FF is set, connect HSB to CC and operate CC clear gate. Supply EP.	159 429 428 200 209 206
	*The four LSD's of (CR) are merged with eight decimal zeros from CU to make the complete word which is transferred to the HSB.	

ANALYSIS OF	UNIVAC II	
INSTRUCTIO	DESCRIPTION	FT
ROm	(000000 U0(CC))→ m	
	Operate rM address exceeded and preset checkers. Operate HSB-OEC. Operate HSB-AOC. Connect CC and CU (000000 U0) to HSB.* Set rM Read FF, set M ₁ cores. Develop Staticize Pulse. Set MTO. Supply EP.	860 429 428 245 826 823 825 206
	*The four LSD's of (CC) are merged with (000000 UO) from the CU to make the complete word which is transferred to the HSB.	
SOm	$-(m) \longrightarrow rX; (rX) + (rA) \longrightarrow rA$	
1	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M ₁ cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rX via sign reversal gates.* Operate rX clear gate. Set MTO. Step PC, set TO. *The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX.	860 827 429 428 820 821 824 153 120 825 214
то	Compare (rA) and (rX).	None
2	Operate adder for eleven place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Supply EP.	160 435 125 109
	<pre>#If decimal carry occurs from eleventh digit position, set Overflow FF. If Second Instruction Digit is a minus sign, overflow sets Stop FF.</pre>	

INSTRUCTION

UNIVAC II

DESCRIPTION

SFm	$-(\underline{m}) \longrightarrow rX; (rX) + (rA) \longrightarrow rA.$	
1	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M ₁ cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rX via sign reversal gates.+ Operate rX clear gate. Operate extract circuit in rF.* Set MTO. Step PC, set TO.	860 827 429 428 820 821 824 153 120 193 825 214
	 *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero. +The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX. 	
то	Compare (rA) and (rX).	None
2	Operate adder for eleven place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. Connect HSB to adder sub input and rA to adder . min input. Clear rA and transfer sum from adder to rA	160 435 125
	Supply EP.	206
	*If decimal carry occurs from eleventh digit position, set Overflow FF.	

ANALYSIS OF INSTRUCTIONS INSTRUCTION

UNIVAC II

DESCRIPTION

SHm	$-(m) \longrightarrow rX; (rX) + (rA) \longrightarrow rA \longrightarrow m$	
1	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC.	860 827 429 428
	Set rM Read FF, set M _l cores. Strobe rM sense amplifiers	820 821
	Develop Serial Pulse.	824
	Connect HSB to rX via sign reversal gates.* Operate rX clear gate.	153 120
	Set MTO.	825
	Step PC, set TO.	214
	*The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX.	
то	Compare (rA) and (rX).	None
SHm		
2	Operate adder for eleven place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from	160 435 125
	adder to rA. Step PC, set TO.	214
	*If decimal carry occurs from eleventh digit position, set Overflow FF. +FT206 is present, but its effect is suppressed by	206+
	FT214.	ļ
I S H m		
3	Operate rM address exceeded and preset checkers. Connect rA to HSB. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M_1 cores. Develop Staticize Pulse. Set MTO. Supply EP.	860 100 429 428 826 823 825 206

INSTRUCTION

UNIVAC II

DESCRIPTION

T n m 1	<pre>If (rA) > (rL), Transfer control to m. Operate HSB-OEC. Operate HSB-AOC. Connect rL to HSB. Set up comparator to perform algebraic comparison.* Delete rX input to comparator and connect HSB. If 2nd Instruction Digit "n" equals Conditional Transfer Breakpoint Selector setting, pass tl to set Stop FF. Step PC, set TO. *If (rA) > (rL), the Conditional Transfer FF is set at t5 of PC-2 TO.</pre>	429 428 187 172 152 236 214
		ļ
TO		
Tnm		1
2	Retain results of comparison in comparator. Operate HSB-OEC. Operate HSB-AOC. Connect CR and CU (000000 00) to HSB.* If Conditional Transfer FF is set, connect HSB to CC and operate CC clear gate. Supply EP.	159 429 428 200 209 206
	*The four LSD's of (CR) are merged with eight decimal zeros from CU to make the complete word which is transferred to the HSB.	
UOm	Transfer control to m Operate HSB-OEC. Operate HSB-AOC. Connect CR and CU (000000 00) to HSB. Connect HSB to CC, operating CC clear gate. Supply EP.	429 428 200 208 206

UNIVAC II

INSTRUCTION

DESCRIPTION

FT

Vnm	(m) $(m+1)$ $(m+n-1)$ rW	
4 11 III		
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AUC.	428
	Preset r7W units counter to alevans complement	820
	of the 2nd Instruction Digit When the r7W	
	units counter reads zero, gate a t59 to set	
	MTO.*+#	817
	Read and restore rZW simultaneously with the	
	reading and restoring of rM. When MTO is set,	
	supply EP.	818
	Develop Serialize Dulas	821
	Step rM counters and r7W units counter once each	824
	minor cycle until rZW units counter reads zero	833
	Supply EP.	206
	*If 2nd Instruction Digit is a zero and if com-	
	patibility switch on SC is set to Univac II,	
	treat instruction as a Skip.	
	LTf Compatibility quitable and to Take T	
	the rZW units counter is unconditionally act to	
	nine.	
	#The "Tens" 7 or W line is always up except during	
	the Y or Z instructions.	

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INSTRUCTION

UNIVAC II

DESCRIPTION

 \mathbf{FT}

······		· · · · · · · · · · · · · · · · · · ·
Wnm	$(rW) \longrightarrow m, m + 1 \dots m + n - 1$	
	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M1 cores. Preset rZW units counter to elevens complement	860 827 429 428 820
	of the 2nd Instruction Digit. When the rZW units counter reads zero, gate a t59 to set MTO.*+# Read and restore rZW simultaneously with the reading and restoring of rM. When MTO is set	817
	supply EP. Strobe rZW sense amplifiers. Develop Serialize Pulse. Step rM counters and rZW units counter once each	818 819 824
	<pre>minor cycle until rZW units counter reads zero. Supply EP. *If 2nd Instruction Digit is a zero and if Com- patibility switch on SC is set to Univac II, treat instruction as a Skip. +If Compatibility switch is set to Univac I the rZW units counter is unconditionally set to nine. #The "Tens" 7 or W line is always up except during the Y or Z instructions.</pre>	833 206
XOm	$(rA) + (rX) \longrightarrow rA$	
TO	Compare (rA) and (rX).	None
	Operate adder for eleven place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from	160 435 125
	adder to rA. Supply EP.	109 206
	"II decimal carry occurs from eleventh digit position, set Overflow FF. If second instruction digit is a minus sign, overflow sets Stop FF.	

UNIVAC II

INSTRUCTION

DESCRIPTION

Ynm	(m), (m+1) (m+10n - 1) $\rightarrow rZ$	
	Operate rM address exceeded and preset checkers.	860
	Operate HSB-OFC	429
	Operate HSB-AOC	428
	Set rM Read FF, set M ₁ cores.	820
	Preset rZW tens counter to elevens complement	
	of the 2nd Instruction Digit. Preset rZW units	
	counter to one.	
	when the rZW tens and units counters read zero, $\pi + 50$ to not WTO $\pi + 50$	014
	Read and restore r7W simultaneously with the	010
	reading and restoring of rM. When MTO is set.	
	supply EP.	818
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Step rM counters and rZW units counter once	
	each minor cycle. When the rZW units counter	000
	passes trhough zero it steps the rZW tens counter.	833
	Supply Mr. *If 2nd Instruction Digit is a 7 8 9 or 0 and	200
	if Compatibility switch on SC is set to Univer II	
	treat instruction as a Skip.	
	+If Compatibility switch is set to Univac I.	
	the rZW tens counter is preset to zero.	
Znm	$(rZ) \longrightarrow m, m+1 \dots m+10n-1$	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M1 cores.	820
	of the 2nd Instruction Digit Preset r7W units	
1	counter to one	
•	When the rZW tens and units counters read zero.	
	gate a t59 to set MTO. *+	816
	Read and restore rZW simultaneously with the	
	reading and restoring of rM. When MTO is set,	
	supply EP.	818
	Strobe rZW sense amplifiers.	819
	Step rM counters and r7W units counter once each	824
	minor cycle. When the rZW units counter passes	•
	through zero it steps the rZW tens counter.	833
	Supply EP.	206
	if Compatibility switch on SC is set to Univer IT	
	treat instruction as a Skin	
	+If Compatibility switch is set to Univac I the	
1		
	rZW tens counter is preset to zero.	

INSTRUCTION

UNIVAC II

DESCRIPTION

.n m	Shift rA right, with sign, n places	
A 11	Preset rZW units counter to the elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO. Operate rA clear gate. Operate right shift path of rA and insert a decimal zero into the sign position.* Step rZW and rM counters once each minor cycle until rZW units counter reads zero. Step PC once per minor cycle. + When MTO is set, supply EP at following tl. *rA shifts one digit right during each minor cycle of Timé-on.	817 101 106 833 213 818
	+If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting the FT Inter- mediate Checker FF, and TO.	
-n m	Shift rA right, without sign, n places	
A11	 Preset rZW units counter to the elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO. Operate rA clear gate, except for sign position. Operate right shift path of rA and insert a decimal zero into the (MSD) position.* Step rZW and rM counters once each minor cycle until rZW units counter reads zero. Step PC once each minor cycle. + When MTO is set, supply EP and set TO at following tl. *rA shifts one digit right during each minor cycle of Time-on. +If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting the FT Intermediate Checker FF and TO. 	817 170 107 833 213 818

UNIVAC II

INSTRUCTION

~

DESCRIPTION

 \mathbf{FT}

;n m	Shift rA left, with sign, n places	
A 11	Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO. Operate rA clear gate. Operate left shift path of rA. * Insert decimal zero into LSD position of (rA). Step rZW and rM counters once each minor cycle until rZW units counter reads zero. Step PC once each minor cycle. + When MTO is set, supply EP and set TO at following t1.	817 101 103 171 833 213 818
	<pre>*rA shifts one digit left during each minor cycle of Time-on.</pre>	
	+If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting FT Intermediate Checker FF and TO.	
Onm	Shift rA left, without sign, n places	
A11	Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO. Operate rA clear gate, except for sign position. Operate left shift path of rA. * Insert decimal zero into LSD position of (rA). Step rZW and rM counters once each minor cycle until rZW units counter reads zero. Step PC once each minor cycle. + When MTO is set, supply EP at following t1.	817 170 104 171 833 213 818
	<pre>*rA shifts one digit left during each minor cycle of Time-on.</pre>	
	+If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting FT Intermediate Checker FF and TO.	

INSTRUCTION

UNIVAC II

DESCRIPTION

00m	Skip instruction (Supply Ending Pulse and proceed to next instruction) Supply EP.	206
Om	Stop computation if Breakpoint switch on SC is depressed Set Stop FF if Breakpoint switch is depressed. Supply EP.	217 206
90 m	Stop computation Set Stop FF. Supply EP.	218 206
1 n m	60 words from tape to rI, forward	
1	Gate nS (Servo Selector) signal from second Instruction Digit to determine if Uniservo desired will pass interlock. Gate, FIR, BIR or FIR-BIR to determine if	629
	computer will pass interlock to start read operation. ≠ + If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following tl	606
	generate IRP. * Gate IRP as Sequence I Preset.	No ne 621
	 + Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. 	
	 * IRP is used to: 1. Step PC. 2. Set TO. 3. Supply set pulse to Direction Memory. 4. Set Reversal Memory if BIR was returned from Uniservo. 5. Reset Interlock Release FF. 6. Supply Sequence I Preset. 	
	✓ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	

INSTRUCTION	DESCRIPTION	FT
lnm	Gate nS signal to Uniservo (n) to alert Read and Forward thyratrons.	629
ТО	Gate RP and FP signals to fire Read and Forward thyratrons in Uniservo (n). Gate RP to set	
2	Read Interlock. Gate LE of FT604 to ending pulse delay.	604
	If Direction Memory agrees with first instruction digit, supply Read Tape Preset and gate an EP to	
	control circuits. Gate EP to set Read Forward and Start Read FF's	609
	after appropriate delay. *	614
	* Length of time before Read Forward FF is set is determined by condition of Reversal Memory. Length of time before Read Control FF is set is determined by condition of Reversal Memory and First Block Memory.	

UNIVAC II

INSTRUCTION

DESCRIPTION

2 n m	60 words from tape to rI, backward	
1	Gate nS (Servo Selector) signal from Second In- struction Digit to determine if Uniservo desired will pass interlock. Gate FIR, BIR or FIR-BIR to determine if com- puter will pass interlock to start read oper- ation. $+ \neq$ If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following tl gate a pulse to generate IRP. * Gate IRP as Sequence I Preset.	629 606 None 621
	 + Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. 	
	 * IRP is used to: 1. Step PC. 2. Set TO. 3. Supply reset pulse to Direction Memory. 4. Set Reversal Memory if FIR was returned from Uniservo. 5. Reset Interlock Release FF. 6. Supply Sequence I Preset. 	
	✓ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	
то		

AN TN	ALYSIS OF	UNIVAC II	
TI	INSTRUCTION	DESCRIPTION	FT
	2 n m 2	Gate nS signal to Uniservo (n) to alert Read and Backward thyratrons. Gate RP and BP signals to fire Read and Backward thyratrons in Uniservo (n). + Gate RP to set	629
		pulse delay. If Direction Memory agrees with First Instruc- tion Digit, supply Read Tape Preset and gate an	604
		EP to control circuits. Gate EP to set Read Backward and Start Read FF's after appropriate delay. *	609 61 4
;		* Length of time before Read Backward FF is set is determined by condition of Reversal Memory. Length of time before Read Control FF is set is determined by condition of Reversal Memory and First Block Memory.	
	3 n m	$(rI) \longrightarrow m$ THRU m+59; 60 words $\longrightarrow rI$, forward	
	1	Operate rM address exceeded & preset checkers. Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo de-	860
		sired will pass interlock. Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read	629
		operation. $+ \neq$ If FIR, BIR or FIR-BIR pass interlock test set Interlock Release FF. At following tl gener-	606
		ate IRP. * Gate IRP as Sequence I Preset.	None 621
		 + Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. IO-INT FF is reset. 4. First Block Memory is reset. 5. No rewind has been initiated within 3 ms. 	
		 * IRP is used to Step PC. Set TO. Supply set pulse to Direction Memory. 4. Set Reversal Memory if BIR was returned from Uniservo. 5. Reset Interlock Release FF. 6. Supply Sequence I Preset. 	
		≠ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	

INSTRUCTION

UNIVAC II

DESCRIPTION

		1
3 n m		
то		
2	Set rM Read FF. Set BCM to RM. Inhibit set of M1 cores, strobe rI sense amplifiers, transfer $M_2 \longrightarrow M_1$ and $M_2 \longrightarrow rI$.	820 827
	fer until "59" signal occurs, at which time set MTO, step PC, and set TO. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Step rM and rZW address counters. Gate nS signal to Uniservo (n) to alert Read and Forward thyratrons. Gate RP and FP signals to fire Read and For- ward thyratrons in Uniservo (n).	641 824 429 428 833 629
	Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay.	604
то		+
3	If Direction Memory agrees with First In- struction Digit, supply Read Tape Preset and gate an EP to control circuits. Gate EP to set Read Forward and Start Read FF's after appropriate delay. *	609 614
	Length of time before Read Forward FF is set is determined by condition of Reversal Memory. Length of time before Read Control FF is set is determined by condition of Reversal Memory and First Block Memory.	

ANALYSIS OF INSTRUCTIONS	UNIVAC II	
INSTRUCTION	DESCRIPTION	FT
4 n m	(rI)→m THRU m+59; 60 words→rI, backward	
1	Operate address exceeded & preset checkers. Gate nS (Servo Selector) signal from Second	860
	sired will pass interlock. Gate FIR, BIR or FIR-BIR to determine if com-	621
	ation. + If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF At following th	606
	generate IRP. * Gate IRP as Sequence I Preset.	None 629
	 + Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. 	
	 * IRP is used to: 1. Step PC. 2. Set TO. 3. Supply reset pulse to Direction Memory. 4. Set Reversal Memory if FIR was returned from Uniservo. 5. Reset Interlock Release FF. 6. Supply Sequence I Preset. 	
	✓ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	
то		
4 n m 2	Set rM Read FF. Set BCM to RM. Inhibit set of M_1 cores, strobe rI sense amplfiers, transfer $M_2 \longrightarrow M_1$ and $M_2 \longrightarrow rI$.	820 827
	Step rI address counters for each word trans- ferred until "59" signal occurs at which time set MTO, step PC, and set TO. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Step rM and rZW address counters. Gate nS signal to Uniservo (n). Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay.	641 824 429 428 833 629 604

INSTRUCTIONS	UNIVAC II	
INSTRUCTION	DESCRIPTION	FT
4 n m 3	If Direction Memory agrees with First Instruction Digit, supply Read Tape Preset and gate an EP to control circuits. Gate EP to set Read Backward and Start Read FF's after appropriate delay. * * Length of time before Read Backward FF is set is determined by conditions of Reversal Memory and First Block Memory.	609 61 4
5 n m	(m THRU m+59)> tape, 215 pulses per inch. 108 pulses per inch if (n) Tape Density button is depressed.	
1	Operate rM address exceeded & preset checkers. Gate nS (Servo Selector) signal from Second	860
	pass interlock. Gate FIR, BIR or FIR-BIR to determine if com-	629
	puter will pass interlock to start write operation. $+ \neq \%$ If FIR, BIR or FIR-BIR passes interlock test,	606
	set Interlock Release FF. At the following tl generate IRP. * Gate IRP to generate Sequence "O" Preset.	No ne 669
	 + Computer will pass interlock if: Write Interlock is reset. Reversal Memory is reset. First Block Memory is reset. IO-INT FF is reset. No rewind has been initiated within 3 ms. Supervisory Control Interlock FF is reset. # If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.) % Gated F and W signal from the First Instruction Digit samples ring switch on Uniservo (n). If tape on Uniservo (n) is ringed, inhibit return of FIR, BIR or FIR-BIR. IRP is used to: Set Reversal Memory if BIR was returned from Uniservo. Reset Interlock Release FF. 	

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UNIVAC II

INSTRUCTION	DESCRIPTION	FT
5 n m	Sequence rM for RH timing	820
	Strobe rM sense amplifiers.	821
то	Transfer $M_1 \longrightarrow M_3$.	829
10	1100000000000000000000000000000000000	
2	Step r0 address counters for each word trans-	
L	ferred until "59" signal occurs at which time	
	set MTO step PC and set TO	681
	Step rM r7W address counters	833
	Develon Serialize Pulse	824
	Operate HSB-OFC	429
	Operate HSB-AOC	128
	Cate nS signal to Uniservo (n) and alert Write	-12-0
	and Forward thurstrons	629
	Cate WD and FD signals to fire Write and For-	027
	word thurstrong in Unicorus (n) Cote MD sig-	
	nol to got Write Interlock Cate IF of FT604	
	to ording pulse delay +	604
	to ending puise delay. +	004
	+ If nS signal agrees with Tape Density Selec- tor switch, gate WP to pick up Tape Density relay for 108 PPI.	
то		
2	Supply Write Tang Preset and gate on FP to	
5	control circuits	609
	Cate FD to set Write Forward and Start Write	007
	FE's ofter oppropriate delay *	615
	rr s alter appropriate deray.	015
	* length of time before Write Forward FF is	
	set is determined by condition of Reversal	
	Memory	
	Length of time before Write Control FF is set	
	is determined by condition of Reversel Memory	
	and First Black Memory	
	and its block memory.) I
1	1	1

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INSTRUCTION	DESCRIPTION	FT
6 n m	Rewind Uniservo (n)	
1	Gate nS (Servo Selector) signal from Second In- struction Digit to determine if Uniservo desired will pass interlock. Gate FIR, BIR or FIR-BIR to determine if com- puter will pass interlock to start rewind operation. $+ \neq$ If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following tl generate IRP. * Inhibit step PC, supply EP if Uniservo is re- wound.	629 606 None 608
	 + Computer will pass interlock if: 1. Write Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. 6. Supervisory Control Interlock FF is reset. 	
	 ★ IRP is used to: Step PC. Set TO. Set Reversal Memory if FIR was returned from Uniservo. 4. Reset Interlock Release FF. ✓ If FIR-BIR is returned from Uniservo, set First Block Memory and inhibit IRP. 	
то		
2	Gate nS signal to alert Rewind and Backward thyratrons in Uniservo (n). Generate BP signal and supply pulse to initi- ate Rewind Start circuits, supply FD ofter	629
	Rewind Control FF is set.	619

INSTRUCTION	DESCRIPTION	FT
7 n m	(m THRU m+59) -> tape; 54 pulses per inch	
1	Operate rM address exceeded & preset checkers. Gate nS (Servo Selector) signal from Second	860
	Instruction Digit to determine if Uniservo de- sired will pass interlock. Gate FIR, BIR or FIR-BIR to determine if com-	629
	puter will pass interlock to start write oper- ation. $+ \neq \%$ If FIR, BIR or FIR-BIR passes interlock test,	606
	set Interlock Release FF. At the following tl generate IRP. * Gate IRP to generate Sequence "O" preset.	No ne 669
	 + Computer will pass interlock if: Write Interlock is reset. Reversal Memory is reset. First Block Memory is reset. IO-INT FF is reset. No rewind has been initiated within 3 ms. Supervisory Control Interlock FF is reset. * IRP is used to: Set Reversal Memory if BIR was returned from Uniservo. Reset Interlock Release FF. Supply Sequence "O" Preset. # If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.) % Gated F and W signal from the First Instruction Digit samples ring switch on Uniservo (n). If tape on Uniservo (n) is ringed, inhibit return of FIR, BIR or FIR-BIR. 	
то		

INSTRUCTION	DESCRIPTION	FT
7 n m 2	Set rM Read FF, set M ₁ cores. Strobe rM sense amplifiers. Transfer M ₁ \rightarrow M ₃ . Step rM, rZW address counters. Transfer M ₃ \rightarrow rO. Step rO address counters for each word transferred until "59" signal occurs at which time set MTO, step PC, and set TO. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-OEC. Operate HSB-AOC. Set 54 pulses per inch thyratron to write at 54 PPI. Gate nS signal to Uniservo (n) to alert Write and Forward thyratrons. Gate WP and FP signals to fire Write and Forward thyratrons in Uniservo (n). Gate WP signal to set Write Interlock. Gate LE of FT604 to ending pulse delay.	820 821 829 833 681 824 429 428 None 629 604
TO		
3	Gate an EP to control circuits. Gate an EP to set Write Forward and Start Write FF's after appropriate delay.	609 615
	• · · · · · · · · · · · · · · · · · · ·	

UNIVAC II

INSTRUCTION	DESCRIPTION	FT
8 n m	Rewind Uniservo (n) with interlock	
1	 Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo de- sired will pass interlock. Gate FIR, BIR or FIR-BIR to determine if com- puter will pass interlock to start rewind operation. + ≠ If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF (IRG), and at following tl generate IRP. Gate IRG to pick Interlock relay in Uniservo (n). Inhibit step PC, supply EP if Uniservo is rewound. + Computer will pass interlock if: Write Interlock is reset. Reversal Memory is reset. First Block Memory is reset. No rewind has been initiated within 3 ms. Supervisory Control Interlock FF is reset. ≠ If FIR-BIR is returned from Uniservo, set First Block Memory and inhibit IRP. NOTE: Uniservo will assume First Block condition if both Forward and Backward thyratrons are extinguished in the Uniservo. 	629 606 None 607 608
ТО		
8 n m 2	Gate nS signal to alert Rewind and Backward thyratrons in Uniservo (n). Generate BP signal and supply pulse to initiate rewind start cir- cuits.	629
	Supply EP after Rewind With Interlock relay is picked up and Rewind Control FF is set.	607

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UNIVAC II

 \mathbf{FT}

INSTRUCTION	DESCRIPTION	FT
10 m	Supervisory keyboard —> rM	
1	Operate rM address exceeded & preset checkers. Generate signal to pass Supervisory Control interlock provided that no Read, Supervisory	860
	Control Type-out, or Supervisory Control Type-In is in progress. Set Supervisory Control Input FF. Set Interlock Release FF provided that Reversal Memory, and First Block Memory is reset, and no	616
	rewind has been initiated within 3 ms. Gate following tl as IRP. * Gate IRP as Sequence I Preset.	No ne 621
	 * IRP is used to: 1. Step PC. 2. Set TO. 3. Reset Interlock Release FF. 4. Set Supervisory Control Input FF. 5. Supply Sequence I Preset. 	
то		
2	The Sequence I Preset clears and presets the input counters. The K signals (result of setting Supervisory Control Input FF) control the Input Distributor Control circuits to facilitate a Supervisory Control input. Type in 6 digits, digit by digit, checking each digit for any odd-even error, and step TRI counters after each key is depressed. Transfer each digit from the N5 cores to M2. After the 6th digit is typed, transfer M2 \longrightarrow M1 and type in 6 more digits to M2. After the 12th digit is typed, set Stop FF and depress Word Release which will step PC and set TO.	No FT
то		
3	Set rM Read FF. Transfer $M_2 \rightarrow M_1$, inhibit set of M_1 cores. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Set MTO. Supply EP.	820 645 824 429 428 825 206

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NALYSIS OF	UNIVAC II	
INSTRUCTION	DESCRIPTION	FT
30 m	(rI)→m thru m+59	
1	Operate rM address exceeded & preset checkers.	860
	struction digit.	629
	ter will pass interlock, to start transfer	(0)
	operation. + If "O Select" passes interlock test, set Inter-	606
	lock Release FF. At following tl gate a pulse to generate IRP. *	
	Gate IRP as Sequence I Preset.	621
	 + Computer will pass interlock if: l. Read Interlock is reset. 	
	 Reversal Memory is reset. IO-INT FF is reset. 	
	 First Block Memory is reset. No rewind has been initiated within 3 ms. 	
	* IRP is used to:	
	2. Set TO.	
	 Supply set pulse to Direction Memory. Reset Interlock Release FF. 	
	5. Supply Sequence I Preset.	· · · · · · · · · · · · · · · · · · ·
T0		
2	Set rM Read FF Set BCM to RM.	820 827
	Strobe rI sense amplifiers transferring	
	counters for each word transferred until	
	MTO, step PC, and set TO.	64 1
	Develop Serialize Pulse Operate HSB-OEC.	824 429
	Operate HSB-AOC.	428
	Step rM and rZW address counters.	833 629*
	Gate LE of FT604 to ending pulse delay.	604
	* FT629 is brought up for a 30 instruction, but is not used because no Uniservo is	
	operated.	
ТО		
3	If Direction Memory agrees with instruction Gate EP to control circuits.	609
	* FT614 is brought up for a 30 instruction, but is not used because no Uniservo is operated.	61 4 *

UNIVAC II

INSTRUCTION

DESCRIPTION

FT

40 m	(rI)→m thru m+59	
1	Operate rM address exceeded & preset checkers.	860
	tion Digit.	629
	Gate "O Select" signal to determine if computer will pass interlock to start transfer operation. + If "O Select" passes interlock test, set Inter- lock Release FF. At following tl gate a pulse to generate TPP. *	606
	Gate IRP as Sequence I Preset.	62 1
	 + Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. IO-INT FF is reset. 4. First Block Memory is reset. 5. No rewind has been initiated within 3 ms. 	
	* IRP is used to:	
	2. Set TO.	
	 3. Supply reset pulse to Direction Memory. 4. Reset Interlock Release FF. 5. Supply Sequence I Preset. 	
то		
2	Set rM read FF, set M_1 cores. Set BCM to RM. Inhibit set of M1 cores, strobe rI sense amplifiers transferring $M_2 \rightarrow M_1$ and $M_2 \rightarrow$ rI. Step rI address counters for each	820 827
	word transferred until "59" signal occurs at which time set MTO, step PC, and set TO.	641
	Develop Serialize Pulse. Operate HSB-OEC.	824 429
	Operate HSB-AOC.	428
	Gate RP to set Read Interlock. Gate LE of	833
	FT604 to ending pulse delay. * FT629 is brought up for a 40 instruction	604 629 *
	but is not used because moUniservo is operated.	02 /
то		
3	If Direction Memory agrees with first instruction, gate an EP to control circuits.	609 614*
	* FT614 is brought up for a 40 instruction, but is not used because no Uniservo is operated.	

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INSTRUCTION	DESCRIPTION	FT
50	(Register determined by SC output button) > SC printer	
1	Operate rM address exceeded & preset checkers. Generate signal to pass Write Interlock at Write Interlock gate provided the Supervisory Control	860
	Interlock FF and Write Interlock FF are reset. Set Interlock Release FF provided the First Block Memory, Reversal Memory, IO-INT are reset and no rewind has been initiated within 3	606
	ms.	None
	Gate output of Interlock Release FF with a tl to generate IRP. * Gate IRP to generate Sequence O Preset. Gate IRP to set Supervisory Control Output FF, set Write Interlock.	None 669 617 629+
	 * IRP is used to: Step PC. Set TO. Reset Interlock Release FF. Set Supervisory Control Output FF. Supply Sequence O Preset. + FT629 is picked up for a 50 instruction, but is used only in the FTOC. 	

ANALYSIS OF INSTRUCTIONS INSTRUCTION

UNIVAC II

DESCRIPTION

50		
то		
2	The Sequence O Preset clears and presets the out- put counters. The T signals (result of setting the Supervisory Control Output FF) control the Output Distributor control circuits to facilitate a Supervisory Control output. Set rZW Read FF. Set rM Read FF, set M ₁ cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Set MTO. Step PC, set TO. Above steps are for readout of rM. With FT 620, 621, and 624 deleted, and FT 623, 826, 861 and the read out FT of a particular register inserted, a register type out is accomplished. The sequence for type out from a register is: Set rZW Read and Write FF's Transfer (rA) — HSB. Operate HSB-OCC. Operate HSB-AOC. Develop Staticize Pulse Set MTO. Step PC, set TO. Set rZW Read FF, set M ₁ cores. Inhibit set of rM Read/Write FF. + Up only if rA Output Selector button is depressed. Other FT signals are: 1. rF 192 2. rL 187 3. rA 100 4. rX 125 5. CC 210 6. CR 248 • The EP gated by FT818 in the Control Circuits is suppressed by FT214.	818 820 821 824 429 428 825 214 818* 100+ 429 428 823 825 214 826 861
ТО		

FT

ANALYSIS OF INSTRUCTIONS	UNIVAC 11	
INSTRUCTION	DESCRIPTION	FT
50 3	Operate HSB-OEC. Operate HSB-AOC. Set rZW Read/Write FF's. Strobe rZW sense amplifiers. Set rZW Read FF, set M_1 cores. Develop Serialize Pulse. Set MTO. Transfer $M_1 \longrightarrow M_3$. Inhibit set of rM Write FF. Transfer $M_3 \longrightarrow M_4$. Step PC, set TO.	429 428 818 819 820 824 825 829 861 685 214
ТО		
4	Supply EP.	206
50 Breakpoint	<pre>(Register determined by SC output button) → SC printer Stop computer if Type Out Breakpoint switch on SC is operated. Operate rM address exceeded & preset checkers. Generate signal to pass write interlock at Write Interlock gate provided that Supervisory Control Interlock FF and Write Interlock FF is reset. Set Interlock Release FF provided that, First Block Memory, Reversal Memory, IO-INT are reset, and no rewind has been initiated within 3 ms. Gate output of Interlock Release FF with a t1 to generate IRP. * Gate IRP to generate Sequence 0 Preset. Gate IRP to set Supervisory Control Output FF, set Write Interlock. Set Stop FF if Output Breakpoint switch is thrown. * IRP is used to: 1. Step PC 2. Set TO 3. Reset Interlock Release FF 4. Set Supervisory Control Output FF 5. Supply Sequence 0 Preset + FT 629 is picked up for a 50 instruction, but is used only in the FTOC.</pre>	860 606 None 669 617 218 629+

UNIVAC II

INSTRUCTION

DESCRIPTION

TO 50 Breakpoint		
50 Breakpoint 2	The Sequence O Preset clears and present the out- put counters. The T signals (result of setting the Supervisory Control Output FF) control the Output Distributor control circuits to facilitate a Super- visory Control output. Set rZW Read FF. Set rM Read FF, set M1 Cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Set MTO. Step PC, set TO.	818 820 821 824 429 428 825 214
	Above steps are for read out of rM. With FT 820, 821, and 824 deleted and FT 823, 826, 861, and the read out FT of a particular register inserted, a register type out is accomplished. The sequence for read out from a register is:	
	Transfer (rA)→ HSB. Operate HSB-OEC. Operate HSB-AOC. Develop Staticize Pulse. Set MTO. Step PC, set TO. Set rZW Read FF. Inhibit set of rM Read/Write FF's. Set rZW Read FF. + Up only if rA Output Selector button is de- pressed. Other FT signals are:	100+ 429 428 823 825 214 826 861 818*
	 rF 192 rL 187 rA 100 rX 125 CC 210 CR 248 *The EP gated by FT818 in the control circuits is suppressed by FT214. 	
то		

FT

INSTRUCTION

UNIVAC II

DESCRIPTION

50 Breakpoint		
	Operate HSB-OEC.	429
3	Operate HSB-AOC.	428
	Set rZW Read/Write FF's.	818
	Strobe rZW sense amplifiers.	819
	Set rZW Read FF, Set M ₁ Cores.	820
	Develop Serialize Pulse.	824
	Set MIU.	820
	Iransier $M_1 \rightarrow M_3$.	861
	Transfer $M_{-} \rightarrow M_{-}$	685
	Step PC, set TO.	214
то		<u></u>
10		
4	Supply EP.	206
50 Skip	(Register determined by SC output button)	
	Skin the type out if Skin Type Out switch on SC	
	is operated.	
	Supply EP (if switch is operated)	206
Empty	rM successive words \rightarrow SC printer	
Linpey		
1	Operate rM address exceeded & preset checkers.	860
	Insert decimal zeros onto HSB.	401
	Operate HSB-OEC.	429
	Operate HSB-AUC.	428
	Operate HSB>CR gate, operate CR clear gate.	201
	White Interlock gate provided the Supervisory	
	Control Interlock FE and Write Interlock are	
	reset	606
	Set Interlock Release FF provided the First	000
	Block Memory, Reversal Memory, IO-INT are reset	
	and no rewind has been initiated within 3 ms.	None
	Gate output of Interlock Release FF with a tl	
	to generate IRP.	None
	Gate IRP to generate Sequence O Preset.	669
	Gate IRP to set Supervisory Control Output FF,	
	to Write Interlock.	617
	* TRP is used to:	629+
	1. Step PC.	
	2. Set TO.	1
	3. Reset Interlock Release FF.	
	4. Set Supervisory Control Output FF.	
	5. Supply Sequence O Preset.	
	157(20 is nicked up for an EMPTY instruction	
	hut is used only in FTOC.	
L TU		

 \mathbf{FT}

INSTRUCTION	DESCRIPTION	FT
2	The Sequence O Preset clears and presets the output counters. The T signals (result of setting the Supervisory Control Output FF) con- trol the Output Distributor control circuits to facilitate a Supervisory Control output.	
	Set rM Read FF, Set M ₁ cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Set MTO. Step PC, set TO.	820 821 824 429 428 825 214
ТО		
Empty 3	Operate HSB-OEC. Operate HSB-AOC. Set rZW Read/Write FF's. Set rM Read FF, Set M_1 Cores. Strobe rZW sense amplifiers Develop Serialize Pulse. Set MTO. Transfer $M_1 \longrightarrow M_3$. Inhibit set of rM Read/Write FF's. Read M3, transfer $M_3 \longrightarrow M_4$. Step PC, set TO.	429 428 818 820 819 824 825 829 861 685 214
Empty TO		
4	Transfer CC —> min input adder, (000000 000001) sub input adder. Transfer sum from unbarred adder to CC after clearing CC. Operate adder for 12-place addition. Operate adder OE and sum comparison checkers. Supply reset pulse to Overflow FF. Transfer (CR)—> SR distributor line without delay. Supply EP.	212 714 435 737 204 206
	Note: EMPTY instruction is started by depressing the Empty switch on SC. It is executed in Beta time with the typed information being read from rM location, designated by SR - the current CC reading. After the EP, two skip instructions will be executed because of the decimal zeros read into CR during PG-1, thus permitting (CC) to set up into SR with mext memory to be emptied.	

INSTRUCTION	DESCRIPTION	FT
Fill	SC keyboard —> rM, successive words	
1	Operate rM address exceeded & preset checkers. Insert decimal zeros onto HSB. Operate HSB-OEC. Operate HSB-AOC. Operate HSB -> CR gate, Operate CR clear gate Generate signal to pass Supervisory Control Interlock, provided that no read, Supervisory Control type-out, or Supervisory Control type-in is in progress. Set Interlock Release FF, provided that Reversal Memory and First Block Memory are reset, and no rewind has been initiated within 3 ms. Gate following t1 as IRP. * Gate IRP as Sequence I Preset. * IRP is used to: 1. Step PC. 2. Set TO. 3. Reset Interlock Release FF. 4. Set Supervisory Control Input FF. 5. Supply Sequence I Preset.	860 401 429 428 201 616 None 621
Fill TO		
2	The Sequence I Preset clears and presets the input counters. The K signals (result of set- ting Supervisory Control Input FF) control the Input Distributor control circuits to facili- tate a Supervisory Control input. Type in 6 digits, digit by digit, check each digit for an odd-even error, and step TRI counters after each key is depressed. Transfer each digit from the N ₅ cores to M ₂ . After the 6th digit is typed, transfer M ₂ \longrightarrow M ₁ and type in 6 more digits to M ₂ . After the 12th digit is typed, set Stop FF and depress Word Release which will step PC and set TO.	NO FT
то		

INSTR	UCTION	DESCRIPTION	FT
3		<pre>Set rM Read FF, set M₁ Cores. Read M₂. Transfer M₂→M₁. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Transfer CC→ min input adder, (000000 000001) to sub input adder. Transfer sum from unbarred adder to CC after clearing CC. Operate adder for 12-place addition. Operate adder OE and sum comparison checkers. Supply reset pulse to Overflow FF. Transfer (CR)→ SR Distributor Line without delay. Set MTO. Supply EP.</pre> Note: FILL instruction is started by moving the CR Interlock/Fill Mem switch on Supervis- ory Control to the Fill Mem position. It is executed in Beta time with the typed information going to the memory location designated by the SR, which contains the current CC reading. After the EP two skip instructions will be executed because of the decimal zeros read into CR during PC-1, thus permitting (CC) to set up in SR the next memory address to be filled.	820 645 824 429 428 212 714 435 737 204 825 206
Cl	ear CC	CU (000000 000000) → CC Connect CU (000000 000000) to HSB. Operate HSB-OEC. Operate HSB-AOC. Connect HSB to CC, clear CC. Supply EP. Note: By depressing the clear C switch on Supervisory Control, CY is automatically jammed to Beta, and the addition of one to (CC) is inhibited.	401 429 428 208 206

INSTRUCTION	DESCRIPTION	FT
SCI-CR	One word S C keyboard—>CR	
1	Generate signal to pass Supervisory Control interlock provided that no read, Supervisory Control type-out, or Supervisory Control type- in is in progress. Set Interlock Release FF provided that Re- versal Memory, First Block Memory, and Rewind Frequency control is reset. Gate tl after setting Interlock Release FF as IRP. * Gate IRP as Sequence I Preset. Gate IRP to set Supervisory Control FF. Supply reset pulse to Overflow FF.	616 None 621 616 737
	 * IRP is used to: 1. Step PC. 2. Set TO. 3. Reset Interlock Release FF. 4. Set Supervisory Control FF. 5. Supply Sequence I Preset. 	
то		
2	The Sequence I Preset clears and presets the input counters. The K signals (result of setting Supervisory Control Input FF) control the Input Distributor control circuits to fac- ilitate a Supervisory Control input. Type in 6 digits, digit by digit, check each digit for an odd-even error, and step TRI counters after each key is depressed. Transfer each digit from the N ₅ cores to M ₂ . After the 6th digit is typed, transfer M ₂ \longrightarrow M ₁ and type in 6 more digits to M ₂ . After the 12th digit is typed, set Stop FF, depress Word Release which will step PC and set TO.	No FT
то		
3	Inhibit set of rM Read/Write FF's. Enable set of rZW Read FF. Develop Serialize Pulse. Set rZW Read FF, set M_1 Cores Read M_2 , transfer $M_2 \longrightarrow M_1$. Set MTO. Operate HSB-OEC Operate HSB-AOC Step PC, set TO, and inhibit EP supplied by FT818.	861 818 824 820 645 825 429 428 214

INSTRUCTION	DESCRIPTION	FT
SCI-CR 4	Preset BCM to RM. Inhibit rM Read/Write FF. Enable set of rZW Read/Write FF's. Set rZW Read FF. Strobe rZW sense amplifiers. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Connect HSB to CR, clear CR. Read LH(CR) ~> SR. Set MTO. Supply EP NOTE: CR TYPE IN switch will jam CY to Beta, and set up SR for SCI-CR.	827 861 818 820 819 824 429 428 201 204 825 206
Memory Clear	Connect CU (000000 000000) to HSB. Operate HSB-OEC. Operate HSB-AOC. Develop Staticize Pulse. Set rM Read FF, set M ₁ Cores. Operate rM address exceeded and preset checkers. Set MTO.	401 429 428 823 826 860 825

4. CONDENSED INSTRUCTION REFERENCE.

This section is similar to Section 3 in that it lists the instructions, in order and by PC steps. However, it lists the FT signals associated with each PC step by number only, and not with description. This offers a rapid reviewal of FT signals present during maintenance routines.

ANALYSIS OF		UNIVAC II	
Instruction	Program Counter <u>Step</u>	FT Signals Notes	<u>i</u>
Α	1	120, 126, 214, 429, 820, 821 In all cases 824, 825, 827, 428, 860 step not show an F order is	a PC m for
	2	109, 125, 160, 206, 435 same as that without "F".	step
AF	1	120, 126, 193, 214, 429, 820 821, 824, 825, 827, 428, 860	
AH	1	Same as A PC 1	
	2	Same as A PC 2, inhibit 206, pick up 214	
	3	Same as H	
B		101, 105, 120, 126, 206, 429, 820, 821, 824, 825, 827, 428, 860	
BF		101, 105, 120, 126, 193, 206, 429, 820, 821, 824, 825, 827, 428, 860	
C		100, 206, 429, 823, 825, 826, 860, 428, 101, 108	
D	1	101, 105, 138, 151, 152, 214, 429, 820, 821, 824, 825, 827, 860, 428	
	2	101, 103, 159, 171, 214, 226	
D	3-14	109, 145, 159, 188, 246, 435, 714	
	14	228, 244	
	15	101, 109, 111, 125, 159, 214 435, 714	
	16	101, 106, 120, 123, 159, 161, 206	
DF	1	101, 105, 138, 151, 152, 193 214, 429, 820, 821, 824, 825 827, 428, 860	
E		193, 206, 429, 820, 821, 824, 825, 827, 832, 428, 860, 101, 105	_

ANALYSIS OF	F NS.	UNIVAC II
EF	1	193, 214, 429, 820, 821, 824, 101 825, 827, 831, 832, 860, 428, 105
	2	100, 206, 429, 823, 825, 826 860, 428
F		190, 206, 429, 820, 821, 824 825, 827, 860, 428
G		192, 206, 429, 823, 825, 826 860, 428
H		100, 206, 429, 823, 825, 826, 860, 428
I		187, 206, 429, 823, 825, 826, 860, 428
J		125, 206, 429, 823, 825, 826, 860, 428
К		100, 101, 108, 185, 206, 429, 428
L		120, 126, 185, 206, 429, 820, 821, 824, 825, 827, 860, 428
LF		120, 126, 185, 193, 206, 429, 820, 821, 824, 825, 827, 428, 860
MP	1	101, 108, 110, 113, 120, 126, 139, 214, 429, 435, 820, 821, 824, 825, 827, 860, 428
MNP	2	110, 113, 214, 435, 714
MNP	3	110, 113, 151, 214, 435, 714
MN	4	100, 101, 108, 112, 113, 120, 123, 159, 190, 214, 226, 435, 428, 429
NMP	5-15	109, 147, 159, 188, 246, 435, 714
MNP	14	244
MNP	15	149, 161, 215, 228

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MF-PF	1	101, 108, 110, 113, 120, 126, 139, 193, 214, 429, 435, 820, 821, 824, 825, 827, 860, 428
*N	1	101, 108, 110, 113, 120, 139 *(N, NFP and PF 153, 214, 429, 435, 820, 821, have P C steps 824, 825, 827, 860, 428 and same FT signals
*Nf	1	101, 108, 110, 113, 120, 139, 153, 193, 214, 429, 435, 820, 821, 824, 825, 827, 860, 428
* P	4	100, 101, 108, 112, 120, 123, **If 2nd Inst. digit 159, 190, 214, 226, 429, 428 is zero treat Instruction as Instruction as
Q	1	152, 156, 187, 214, 236, 429, 428 skip if compati- bility switch is set to Univer II
	2	159, 200, 206, 209, 429, 428
R		206, 245, 429, 823, 825, 826 860, 428
S	1	120, 153, 214, 429, 820, 821, 824, 825, 827, 860, 428
	2	109, 125, 160, 206, 435
SF	1	120, 153, 193, 214, 429, 820, 821, 824, 825, 827, 860, 428
SH	1	Same as S PC 1
	2	109, 125, 160, 214, 435
	3	100, 206, 429, 823, 825, 826, 860, 428
Т	1	152, 172, 187, 214, 2 3 6, 429, 428
	2	159, 200, 206, 209, 429, 428
U		200, 206, 208, 429, 428
V		429, 817, 818, 820, 821, 824, 827, 833, 860, 428, 206**

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INSTRUCTIONS	1	UNIVAC II
W		429, 817, 818, 819, 820, 824, 827, 833, 860, 428, 206**
x		109, 125, 160, 206, 400, 435
Y		429, 816, 818, 820, 821, 824, 827, 833, 860, 428, 206* *If 2nd Inst. digit
Z		428, 429, 816, 818, 819, 820 824, 827, 833, 860, 206* Is a 7, 8, 9 or 0 and if compatibility switch is set to
on all		101, 106, 213, 817, 818, 833 struction as skip.
-n all		107, 170, 213, 817, 818, 833 ** If 2nd Inst. digit
;n all		101, 103, 171, 213, 817, 818, 833 IOI, 103, 171, 213, 817, 818, IS zero and com- patibility switch is set to Univac
0 n all		104, 170, 171, 213, 817, 818, tion as a Skip. 833.
00		206
.0		206, 217
90		206, 218
ln	1	606, 621, 629
	2	609, 604, 614, 629
2n	1	606, 621, 629
	2	609, 604, 614, 629
3n	1	606, 621, 629, 860,
	2	429, 604, 629, 641, 820, 824, 827, 833, 428
	3	609, 614
4n	1	606, 621, 629, 860,
	2	429, 604, 629, 641, 820, 824, 827, 833, 428
	3	609, 614
5n	1	606, 629, 669, 860

5n	2	429, 604, 629, 681, 820, 821, 824, 829, 833, 428
	3	609, 615
6n	1	606, 608, 629
	2	619, 629
7n	1	606, 629, 669, 860
	2	429, 604, 629, 681, 820, 821, 824, 829, 8 33 , 428
	3	609, 615
8n	1	606, 607, 608, 629
	2	607, 619, 629
10m	1	616, 621, 860
	2	
	3	206, 428, 429, 645, 820, 824, 825
10, CR	1	616, 621, 737,
	2	
	3	645, 818, 820, 825, 861, 214, 428, 429, 824
	4	201, 203, 428, 429, 818, 819, 820, 824, 825, 827, 861, 206
30		Same as 3n except O Selector signal prevents tape operation.
40		Same as 4n except O Selector signal prevents tape operation.
50	1	606, 617, 669, 629*, 860 *Note 629 is
	2	214, 429, 685, 825, 818, 428 used only in
		M 820, 821, 824
		A 100, 823, 826, 861
		X 125, 823, 826, 861

ANALYSIS OF INSTRUCTIONS			UNIVAC II
50	2	L	187, 823, 826, 861
		F	192, 823, 826, 861
		сс	210, 823, 826, 861
		CR	248, 823, 826, 861
	3		214, 428, 429, 685, 818, 819, 820, 824, 825, 861, 829
	4		206
50 Breakpo	int		
	1		218, 606, 617, 669, 629, 860
	2		Same as 50 PC-2
	3		Same as 50 PC-3
	4		Same as 50 PC-4
50 Skip	1		206
*Fill	1		201, 401, 428, 429, 616, 621, *Beta cycle is allowed to excite on PC4 of Fill or
	2 3		PC3 of Empty.(F.T. 204, 212, 435, 714, 206 429 645 820 824 825 737 are up during
 ≉⊊mnt v			$\frac{200, 427, 043, 020, 024, 025}{201}$ Beta) $\frac{100}{201}$
Empoy	-		860, 428
	2		214, 429, 820, 821, 824, 825, 428, 818
	3		214, 428, 429, 685, 818, 819, 820, 824, 825, 829, 861
	4		206
Clear CC			206, 208, 401, 428, 429
β Compute			201, 206, 429, 820, 821, 824, 825, 827, 860, 428
BETA			204, 212, 435, 714, 737
GAMMA			203, 203K
DELTA			850, 203K
Memory Cle	ar		401, 429, 823, 826, 860, 428, 825 89

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5. DESCRIPTION OF FUNCTION TABLE SIGNALS.

The Function Table signals described on the following pages generate the minor sequences which complete the instruction routines. The FT signals are initiated by either the decoding of a programmed instruction or by some element of the automatic interval programming of the computer. Figure 1 presents, logically, the signals which control the alerting of the FT signals.

The FT signals are listed in the numerical order of their assigned numbers. Duplicated signals are indicated with the barred notation, e.g., 100 and $\overline{100}$. In the instances where an FT signal originates from several drivers, symbols are used following the FT signal number to differentiate between the various outputs to facilitate identification in the outlying circuits, e.g. FT160A, FT160B, FT160C, etc. Most FT signals are negative-going, those that are not usually carry a plus sign following the FT number; e.g. FT645+.

Pertinent information concerning the FT signals is presented in the columns following the FT number. Column 1 locates the chassis in which the FT signal is generated and gives the output terminal on which the FT signal appears. Column 2 lists the test terminal, for maintenance purposes, on which the full signal appears. Column 3 names the vacuum tube on the chassis from which the FT signal appears. Column 4 lists the signal-no signal condition of the FT signal; i.e., the voltage levels that appear on the corresponding test terminal of the FT. Column 5 provides a logical description of the function performed by each FT signal.

<u>CL C</u> MEM. CL EMPTYI, FILLI (<u>ª</u>) £ COMPOSITE HI D3-14 MNP4 Å PR Q2, T2 209 PR (²³) g 50 (3) MNP5-15 <u>DI6</u> MEM. CL 50 (A) 2 (<u>8</u>) 10 CR (3) MNP4 MNP4 50 (C) 2 210 ์ซิ Я 50 (X) 2 R F С 125 PR В A2, S2, X OF AA TL D15 D2 읬 [92] 50 (2) EMPTY2 ß Į 212 50 (F) 2 к QI RETAIN INST AI ;n FIELD SE С В 'n (126 R હિ 0R U MPI D15 $\binom{42}{8}$ (<u>a</u>) <u>AI</u> ٠n DI 9 213 R K <u>On</u> B 20 DI 유 (I3) (BEI) DI6 DI Q2, T2 <u>– n</u> E 50(3) EMPTY MNP4 B COMPUTE. MNPI F DI5 A MNPI (³ 8 MNP4 RETAIN INST. G COMPOSITE H QI EMPTY I TI I (45) D3-14 20 10 (CR) 4 ļð MNP2 ;n MNP3 (ā) Я Я <u>D2</u> MNPI D2 <u>8</u> 2|4 MNP5-1 (I4) Ŗ 203 9 RETAIN INST 50 (2) MNP4 SI 10 (CR) 3 (P P On <u>vw</u> EFAH2.SH2 RETAIN INST MNP15 (4 9 YZ MNPI <u>3-4n2</u> DI **4**29 **B** (×23 DI (ē <u>5-7n2</u> AI Di E δ ۳ð ନ୍ନ (15) MNP3 10 (M) 3.FILL SI γ RETAIN INST 10(CR)4 MNP 15 215 B COMPUTE D £ ٢ TI R 52 DI6 CL C EMPTY I, FILL I (20 4 QI .0 217 Q2, T2 RETAIN INST. Q, Ν PR 5 βx OF AA UNIVAC I 90 <u>S1</u> С 218 1A OR 50 BKPT IO(CR) 4 MNPI 0R (\bar{a}) R β Q 56 βı MNP4 <u>D2</u> 226 Ŗ RETAIN INST. MNP4 50(4),EMPTY4 MNP5-15 MNP5-15 Е MNPL MNPI D15 <u>D3-14</u> R 228 <u>DI6</u> (ē) 12 <u>D 15</u> <u>D14</u> <u>D3-14</u> D15 С MNP5-15 <u>D2</u> A2, S2, X (5) R MNP4 <u>D3-14</u> ΤI 435 ន្ត 236 00 19 A2.52.) Q Q2,T2 MNPI ٥, (ē) MNP2 <u>D 16</u> MNP2 PR 90 MNP3 <u>D14</u> MNP3 윘 244 50 SKIP A2.52.X . MN4 MNP14 F VWYZ DI5 Ξ I-2n2 D16 245 R A2,52,X R (<u>ē</u>) 604 MNP15 <u>3-4n2</u> 鴙 SPARE MNP4 112 5-7n 2 (²0 6 Q2. T2 MNP5-15 = 0246 R R 28 U 5 <u>5-7ni</u> D3-14 MNPI On к 50 (I) EMPTY D15 6 D2 (<u></u>] MNP2 <u>6-8ni</u> Ŗ 248 50 (CR) 2 В $\overline{\Xi}$ 3-4ni R MNP3 in G 1-2n1 <u>On</u> <u>MN4</u> COMPOSITE H (eq <u>8n</u> (<u>7</u> F ΤI MNPL B COMPUTE 60 10 (M) 3 <u>6-8n</u> (R) AI ĥ α С R 85 В 1-2n2 MNP4 CL C (609) <u>3-4n3</u> ≯♀ ≯ 208 <u>50 (L)</u> DIG U 5-7n3 I **7**87 QI ΤI

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Figure 1. Logical Diagram, Function Table Signals

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Figure 1. Logical Diagram, Function Table Signals (cont'd.)

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Function Table	<u>Chassis</u>	TT	<u>Tube</u>	<u>s/ns</u>	Definition
×100	B5T28	A2	V1	60/90	Connect rA to HSB.
100	B5T29	A4	V2	60/90	
- 101	B3T65	C2	V5	60/90	Operate rA clear gate.
101	B3T33	C1	V4	60/90	
103	B10T54	A12	V1	60/90	Operate left shift path of rA (including
/103	B10T29	A13	V 2	60/90	519n).**
√10 4	B10T85	G6	V13	60/90	Operate left shift path of rA
<u>√104</u>	B10T87	G7	V14	60/90	(excluding sign).
^J 105	B3T43	E4	V 8	60/90	Connect HSB to rA.
105	B3T38	C7	V7	60/90	
106A	B12T56	A4	V 2	60/90	Operate right shift path of rA.
-106A	B12T54	A2	V1	60/90	
́106В	B12T62	A7	V4	60/90	Insert decimal zero into sign
106B	B12T60	A6	V3	60/90	position in FA.
i 106C	B12T39	C4	V6	60/90	Transfer sign from comparator to
- 106C	B12T35	C3	V 5	60/90	rA and rX.
-107	B10 T46	Gl	V11	60/90	Operate right shift path of rA, and insert a decimal zero into the
107	B10T81	G3	V12	60/90	
∽108	C1V66	C6	V6	60/90	Connect CU (000000 000000) to rA.
-108	C1V33	C3	V 5	60/90	
- 109A	C4V6 0	A6	V3	60/90	Connect HSB to adder sub input.
• 109A	C4V62	Cl	V4	60/90	

** rA shifts one digit left for each minor cycle of Time-On.

* rA shifts one digit right for each minor cycle of Time-On.

Function Table	Chassis	TT	Tube	S/NS	Definition
-109D	C4V66	C4	V5	60/90	Connect rA to adder min input. Clear
v109D	C4V68	C6	V6	60/90	rA and transfer sum from adder to rA.
0 110	€3856- C.3 <i>V5</i> G	A2	V1	60/90	Connect rL to adder sub input. Transfer (rL) to adder, replacing
v <u>110</u>	C3V29	A4	V2	60/90	sign digit with a decimal zero.
111	B5T85	G5	V13	60/90	Connect CU (round-off 000000 000005)
×111	B5T87	G7	V14	60/90	to adder min input.
-112A	B11 T7 0	C7	V7	60/90	Connect CU (050000 000000) to the
₹12A	B11 T7 3	E3	V8	60/90	
√112B	B11T75	E6	V 9	60/90	Clear MQC to binary zero and set up
✓ 112B	B11 T77	E8	V10	60/90	
-⁄ 112C	B11T81	G2	V11	60/90	Transfer the LSD of (rX) to MQC.
✓ 112C	B11T83	G4	V12	60/90	·
·113	B3T87	G7	V14	60/90	Connect rA to adder min input. Clear rA and read sum from adder to rA (transfer ends at t12 to TO).
/ 113	B3T83	G6	V13	60/90	
·120	B3T31	A7	V3	60/90	Operate rX clear gate.
~120	B3T58	A6	V 2	60/90	
Z 12 3	C1V62	A8	V4	60/90	Operate right shift path in rX.
~ <u>123</u>	C1V31	A7	V3	60/90	
~ 125	B5T67	C6	V 6	60/90	Connect rX to HSB.
125	B5T72	C8	V7	60/90	
- 126	C1V73	E3	V 8	60/90	Connect HSB to rX.
126	C1V70	C6	V7	60/90	
~138A	B8T60	A7	V3	60/90	Clear MQC to decimal zero.
138A	B8T64	A8	V4	60/90	

Function <u>Table</u>	<u>Chassis</u>	TT	<u>Tube</u>	<u>s/ns</u>	Definition
√138 В	B8T66	C3	V 5	60790	Preset BC-120 in MQC to the non- complement state thereby alerting the non-complementing gates between
√138B	B8T68	C6	V 6	60/90	MQC and MQC-FT.
√13 9	B8T71	E2	V7	60/90	Preset BC-120 to the complement state, thereby alerting the complement gates
139	B8T73	E3	V 8	60/90	connecting the muc and muc-ri.
✓145A	C 5V62	C1	V4	60/90	Gate non-complement output of BC-120 to operate Improper Division Detector
√145A	C5V60	A6	V3	60/90	111 mgc.**
√145B	C5V68	C6	V6	60/90	Enable non-complement output of
_145B	C5V66	C3	V 5	60/90	BC-120 to develop SIX signal.
, 145C	C5V73	E3	v 8	60/90	Step MQC at t2 following each sub- traction until the Through-Zero
-145C	C5B71	E2	V7	60/90	OR CYCLE.
<u>л</u> ́147а	B6T83	G3	V12	60/90	Sample (MQC-FT). If digit is < 3, re- set the \geq 3FF, this transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is \geq 3, set the \geq 3FF, this transfers (rF) to HSB and supplies three stepping pulses to MQC
147A	B6T87	G <u>7</u>	V14	60/90	MQC.
√147B	B6T81	G 2	V11	60/90	If digit in MQC-FT=0, set IER and
√ <u>147</u> B	B6T85	G6	V13	60/90	lek-OK FF's at following t2.
×149	B12T73	E3	V 8	60/90	Inhibit generating a second IER CYCLE in the case that a decimal zero is set up in the MOC.
L-149	B12T71	C7	V7	60/90	up an one moo.
1−151 C	C3V60 1 C3B60	A6	V3	60/90	Disconnect rA input to comparator and
v151C	C3V33	AB	V4	60/90	connect rL. •

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If $rL \leq rA$, Improper Divison occurs at t2 of the eleventh minor cycle of PC-3.

* Sign comparison is performed on (rA) and (rL).

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ANALYSIS OF INSTRUCTIONS

Function Table	<u>Chassis</u>	<u>TT</u>	<u>Tube</u>	<u>s/ns</u>	Definition
~152A	C3V68	C 5	V6	60/90	Disconnect rX input to comparator and
	C3V66	C3	V 5	60/90	connect HSB.*
~152B~	C3V42	E3	V8	60/90	Connect HSB to comparator.
-152B - C	C3V39	C 8	V7	60/90	
-153A	B8T75	E6	V9	60/90	Connect HSB to rX via sign reversal
- 153A	B8T44	E7	V10	60/90	gates.#
√153B	B8T81	G2		60/90	Operate sign reversal gates in rX.
153B	B8T48	G4	V12	60/90	
156A	C3V87		V14	60/90	Set up comparator to perform
156A	C3V85		V13	60/90	equality comparison, ##
> 156B	C3V48		V12	60/90	
156B	C3V79		V11	60/90	
- 156C	C3V77	E7	V10	60/90	
- 156C	C3V75	E5	V 9	60/90	
- 159	B6T46	E5	<u>v9</u>	60/90	Retain results of comparison in
. 159	B6T48	E6	V10	60/90	comparator.

* Sign comparison is performed on (rA) and (rL).

The sign reversal gates complement the LSB and Check Pulse of the sign digit during transfer to rX.

If rA = rL develop CT signal.

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ANALYSIS OF INSTRUCTIONS

Function Table	<u>Chassis</u>	<u> 11</u>	<u>Tube</u>	<u>s/ns</u>	Definition
~160A	C4V7 0	C7	V7	60/90	Operate adder for eleven-place
- 160A	C4V71	E3	٧ð	60/90	
ι 160B	C4V75	E5	V 9	60/90	
✓ <u>160B</u>	C4V77	E8	V10	60/90	
. 160C	C4V79	G2	V11	60/90	
✓ 160C	C4V81	G3	V 12	60/90	
√160D	C4V85	G6	V13	60/90	
v 160D	C4V87	G7	V14	60/90	· · · · · · · · · · · · · · · · · · ·
√161A	B12T44	E8	V 10	60/90	Transfer sign from comparator to rA
<u></u>	B12T75	E5	<u>v9</u>	60/90	and rx.
6 /1 61+	B12T81	G3	V12,10	090/60	Inhibit the insertion of a decimal
161+	B12T79	G2	V11, 9	90/60	zero into ra.
.′170	B10 T7 5	E5	V 9	60/90	Operate rA clear gate, except for
J ₁₇₀	B10T77	E7	V 10	60/90	sign position.
J ₁₇₁	B10 T6 0	A17	V3	60/90	Insert decimal zero in LSD position
√ <u>171</u>	B10T62	C11	V4	60/90	01 FA.
~ 172A	B9T31	A6	V3	60/90	Set up comparator to perform
~ 172A	B9T29	A5	V 2	60/90	argebraic comparison.*
√ 172B	B9T66 .	C3	V 5	60/90	
√172B	B9T64	C1	V4	60/90	

** If decimal carry occurs from eleventh digit position, set Overflow FF. If Second Instruction Digit is a minus sign, overflow sets Stop FF.

* If rA > rL, develop CT signal.

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Function				- 4	
<u>Table</u>	<u>Chassis</u>	TT	<u>Tube</u>	<u>S/NS</u>	Definition
-185A	C1V77	E5	V 9	60/90	Connect HSB to rL. Operate rL clear gate.
~185A	C1V83	G3	V12	60/90	
√18 7	B9T75	E5 _.	V 9	60/90	Connect rL to HSB.
-187	B9T40	E3	V 8	60/90	
√ 188 A	C5V77	E7	V 10	60/90	With<3 signal. Transfer (rL) to HSB
/188A	C5V75	E5	V 9	60/90	
, 188B	C5V83	G4	V 12	60/90	Replace sign digit with a decimal zero. Set TO and STOP FF's after each Time-on minor cycle if IOS is in "One Addition"
√ <u>188B</u>	C5V81	Gl	V 11	60/90	In One Addition .
√188C	C5V87	G7	V14	60/90	With ≥ 3 signal. Connect rF to HSB. Step PC upon completion of each
 ✓ 188C 	C5V85	G6	V13	60/90	IER-OR CICLE.
/190	B3T7 8	E2	V 9	60/90	Connect HSB to rF, and operate rF
v 190	B3T 50	E7	V 10	60/90	clear gale.
v192	B5T41	E2	V 8	60/90	Connect rF to HSB.
192	B5T74	E5	V 9	60/90	
-193	B3T29	(A3)/44	V1	60/90	Operate extract circuit in rF.*
- 193	B3T28	E5C5	V 6	60/90	
-200	B11 T 66	C3	V 5	60/90	Connect CR and CU (000000 00) to HSB.**
-200	B11T68	C6	V 6	60/90	

Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.

** The four LSD's of (CR) are merged with eight decimal zeros from CU to make a complete word which is transferred to HSB.

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Table	<u>Chassis</u>	TT	Tube	<u>S/NS</u>	Definition
-201	B2T26	A2	V1	60/90	Operate HSB CR gate, operate CR clear gate.
~203	C2V46	G1	V11	60/90	Connect CR1 to CR2. (LH Instruc- tion sets up at t7 of Gamma TO)
203K	C2V28	A3	V1	60/90	To FTOC.
204	C2V83	G4	V12	60/90	Connect CR1 to SR Distributor Lin
- 206	B2T64	C1	V4	60/90	Supply EP.
-206	B2T65	C2	V 5	60/90	
-208A	C1V53	G7	V14	60/90	Connect HSB to CC.
208B	C1V51	G 5	V13	60/90	Operate CC clear gate.
/209A	B11 T8 5	G6	V13	60/90	If Conditional Transfer FF is set connect HSB to CC.
209B	B11T87	G8	V14	60/90	If CT FF is set, operate CC clear gate.
210	C2V44	E8	V10	60/90	Connect CC to HSB.
210	C2V75	E5	V 9	60/90	
212A	C2V62	A8	V4	60/90	Connect CC to adder min input.
/212A	C2V60	A5	V3	60/90	
212B	C2V71	E3	V8	60/90	Clear CC.
~212C	C2V70	C7	V7	60/90	Transfer sum from unbarred adder to CC.
212D	C2V37	C5	V6	60/90	Connect CU (000000 000001) to
212D	C2V66	C3	V 5	60/90	adder sub input.
-213CK	B8T87	G17	V14,13	-20/+5	Operate shift selector checker.
/213	B10 T7 0	C7	V7	60/90	Step PC once each minor cycle.*
213	B10T73	E3	V8	60/90	

* If PC is advanced in excess of thirteen, an Overshift signal is developed which stops machine operation by setting FT Intermediate Checker FF and TO.

Function Table	<u>Chassis</u>	<u>TT</u>	<u>Tube</u>	<u>s/ns</u>	Definition
214	B2T51	G4	V12	60 <u>/</u> 90	Step PC, set TO.
V 214	B2T52	G5	V13	60/90	
✓215	B7T68	C6	V7	60/90	Supply EP.
$\sqrt{215}$	B7T37	C5	V6	60/90	
4217	B7T87	G7	V14	60/90	Set Stop FF if Comma Breakpoint
$\sqrt{217}$	B7T85	G6	V13	60/90	switch is depressed.
. 218	BATT BAT 79	Gl	V11	60/90	Set Stop FF.
v <u>218</u>	B9T44	E 7	V10	60/90	
-226	B10T64	C3	V5	60/90	Set Repeat FF.
226	B10T37	<u>(</u> 5)	V6	60/90	
V228	B12T87	G7	V14	60/90	Reset Repeat FF at end of IER OR
$\sqrt{228}$	B12T85	G6	V13	60/90	
236	B9T85	G5	V13	60/90	Set Stop FF with CT Selector. Switch signals during Q or T
~ 236	B9T48	G3	V12	60/90	instructions.
/244	B7T48	G3	V12	60/90	Set TO at end of IER OR CYCLE.
√ <u>244</u>	B7T79	Gl	V11	60/90	
\245	B5T77	EIGE7	V10	60/90	Transfer 4 LSD's of (CC) and
√245	B5T79	G11)G1	V11	60/90	OUCOU DU TROM CU CO HSB.
~ 246	C4V56	A2	V1	60/90	If rA or rX comp error occurs, set
246	C4V58	A4	V2	60/90	10 at following tl.
- 248	B7T66	C3	V5	60/90	Connect CR to HSB.
248	B7T62	A8	V4	60/90	
~ 401	B2T49	E8	V 10	60/90	Connect CU (000000 000000) to HSB.
~ 401	B2T50	G2	V11	60/90	

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Function Table	<u>Chassis</u>	TT	Tube	<u>s/ns</u>	Definition
. ⁄428	B11 T58	A1	V 1	60/90	Operate HSB-AOC.
428	B11 T57	A3	V2	60/90	
i ⁄429	B11 T62	A7	V3	60/90	Operate HSB-OEC.
429	B11 T64	C1	V4	60/90	
435A	B3T48	G4	V12	60/90	Operate adder OE and sum comparison
^J 435B	B3T46	G 2	V11	60/90	checkers.
-604A	B4T42	E4	V 9	60/90	Gate LE of FT604 to ending pulse
.∕604B	B4T54	A1	V 1	60/90	delay.
×606	B4T31	A6	V3	60/90	Gate "O Select" signal to determine if computer will pass interlock to start transfer operation.*
607	B4T50	· G6	V13	60/90	Gate IRG to pick Interlock relay in Uniservo (n).
~608	B4T64	C1	V4	60/90	Inhibit step PC, supply EP if Uniservo is rewound.
/ 609	B4T79	G1	V11	60/90	If Direction Memory agrees with instruction, gate EP to control circuits.
609G	B4T46	Notabe	test Pa	int -	To FTIC.
/614	B4T77	E 7	V10	60/90	Gate EP to set Read Forward and Start Read FF's after appropriate delay.
615	B4T48	G4	V12	60/90	Gate EP to set Write Forward and Start Write FF's after appropriate delay.**

* Computer will pass interlock if: 1. Read Interlock is reset.

2. Reversal Memory is reset.

3. IO INT-FF is reset.

First Block Memory is reset.
 No rewind has been initiated within 3 ms.

** Length of time before Write Forward FF is set is determined by condition of Reversal Memory.

V 681+

681

B4V79

B4V38

G11

E18

V12,9 +5/-20

V11# -20/+5

12,9

Function Table Chassis TT Tube <u>S/NS</u> Definition /616 E2 B4T73 **V8** 60/90 Generate signal to pass Supervisory Control interlock provided that no read, Supervisory Control type-out, or Supervisory Control type-in is in progress. 617 V2 60/90 B4T28 A4 Gate IRP to set Supervisory Control Output FF, set Write Interlock. (V16) 60/90 **v619** B4T53 G7 Generate BP signal and supply pulse to initiate Rewind Start circuits. $\sqrt{14}$ 621 B4T66 **C**5 V6 +5/-20Gate IRP as Sequence I Preset. 629G B4T38 C14 ٧5 30/90 Generate nS (servo select) signal from Second Instruction digit. V4 | +5/-20L641+ B5V62 A18 Inhibit set of M₁ cores, strobe rI sense amplifiers, and transfer $M_2 \longrightarrow M_1$ and $M_2 \longrightarrow rI$. Step rI address counters once for each word transferred until "59" signal occurs, at which time set MTO, step PC. and set TO. -641+ V8 5 +5/-20 E12 B5V71 V641 B5V31 A16 V3,4,1 -20/+5 Permits the rI Preset error to be recognized during PC-2 only in the 3n or 4n instruction. **~**645+ B5V44 E16 V109 +5/-20 Operate Input Distributor for typein. 669 3 +5/-20 B7T58 A13 V2 Gate IRP to generate Sequence 0 Preset. 681+ +5/-20B4V41 E12 V8, S Transfer $M_3 \rightarrow r0$. Step r0 address counters once for each word transferred until "59" signal occurs at

UNIVAC II

which time set MTO, step PC, and

Permits the rO No Address error to

be recognized during PC-2 only of

the 5n or 7n instruction.

set TO.

Function Table

B5V81

685+

<u>Chassis</u> TT <u>Tube</u> S/NS Definition V12/1 +5/-20 Read M_3 , transfer $M_3 \longrightarrow M_4$, type out digit on SC printer. G12

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~714A	B6T60	C1 _	V4	60/90	Operate adder for 12-place addition.
√714A	B6T31	A6	V3	60/90	
⁄714В	B6T35	C6	V6	6 0/90	
7 14B	B6T33	C4	V5 .	60/90	
1714C	B6T77	E3	V8	60/90	
714C	B6T44	E2	V7	60/90	
^ 737	C2V87	G8	V14	60/90	Enables a tl pulse to reset the
-737	C2V85	G6	V13	60/ 90	overriow rrip-rrop.
816+	B7V30	A15	V3/1	+5/-20	When the rZW tens and units counters
£ 816+	B7V67	C15	V6, 4/	+5/-20	Tead 2010, gate a to/ to set mio. "
<i>L</i> 817+	B7V46	G12	V11,9	+5/-20	Preset rZW units counter to the
817-	B7U50	G17	V13,14,1	2+5/-20	struction Digit. When counter reads
V817+	B7V52	G18	V14,12,	+5/-20	zero, gale 139 to set mio.
818+	B6V62	A17	V4,3	+5/-20	Enable the set of the rZW Read FF. When MTO is set, supply EP at
L 818+	B6V64	C12	٧5, ٤	+5/-20	Torrowing Ci.
<u>~819+</u>	B3V76	E3	V9,8	+5/-20	Strobe rZW sense amplifiers.
⊷″820 +	B2V27	A12	VIZ	+5/-20	Enable set of rM, rZW Read/Write FF's, set M _l cores.
√821 +	B2V37	C15	کر۷6	+5/-20	Generate Strobe rM signal.
√ 823+	B3V55	C17	v2, 1	+5/-20	Develop Staticize Pulse, Read M ₁
√823	B3V83	G16	V14	60/90	cores, m1 ro, m1 to staticizer.

* If 2nd Instruction Digit is a 7, 8, 9, or 0, treat instruction as a Skip if Compatibility switch is set to Univac II.

If Compatibility switch is set to Univac I, the rZW tens counter is preset to zero.

Function Table	<u>Chassis</u>	TT	Tube	S/NS	Definition
≁ 824B	B2V31	A 7 (A16)	<u>v4</u> V3	+5/-20	Develop Serialize Pulse, Read M_1 Cores, $M_1 \longrightarrow PS$, $M_1 \longrightarrow Serializer$.
-⁄824A	B2V79	E1656	V11	60/90	Operate rM→ HSB "extract"
824A	B2V51	G8	V14	60/90	circuits.
- 825-	B4V55	A11	V1, 2	-25/gnd	Set MTO. X
825-	B4V59	C11	V4, 3	-25/gnd	×
,#826+	B3V37	C15	V7, 6	+5/-20	Set rM and rZW Read/Write FF's, Set M _l cores.
827+	B2V74	E18	V10,9	+5/-20	Set BCM to RM.
/ 827+	B2V69	C18	V7,8	+5/-20	
L 829+	B2V81	(G2G12	V12,1	3+5/ - 20	Transfer M₁→M₃.
~ 83 1	B9T54	Al	V1	60/90	Complement the operation of the
✓ 831	B9T87	G7	V14	60/90	"extract" circuit.*
y 832	B9T37	C6	V6	60/90	Disconnect CU (000000 000000) input
× 832	B9T70	C7	V7	60/90	to "extract" circuit, connect rA.
v 833+	B6V79	Gl	V11/2	+5/-20	Step rM counters and rZW units counter once each minor cycle until
↓ 833+	B6V86	G7	V14/3	+5/-20	rZW units counter reads zero.
- 850	C1V47	Gl	V11	60/90	Connect CC to SR via CR2.#
- 860+	B7V71	E12	V8, 7	+5/-20	Operate rM address exceeded and
~~860	B7V26	E11	V7	+30/+90	preset checkers.
v 861A	B7T47	AH	V10 / /	-20/+5	Inhibit rM line drivers.
√ 861A	B7T41	É12	v8,	-20/+5	
√ 861 B	B7T72	A //. E14	V9.VI	+ 30/ +90	
Dummay 1	B8V26	A2) G12	¥ r VIZ	60/90	Enforce order of "eveness" in FTOC.

UNIVAC II

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RH Instruction set up at t7 of Delta TO.