ANALYSIS OF INSTRUCTIONS

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UNIVAC II

## ANALYSIS OF INSTRUCTIONS

VOLUME III

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## 1. GENERAL .

The "Analysis of Instructions" manual contains three sections relevant to the analysis and understanding of the routines performed by the computer. These sections include l) a format which relates the discrete operations of each sequence by description, and with the corresponding control Function Table (FT) signal, in such a manner that the time of occurrence of each operation is clearly delineated; 2) a roster of the computer routines by code with the Function Table signals as they appear with regard to time of occurrence in the routine; and 3) a list of the Function Table signals with pertinent information concerning each signal.

The basic period in the performance of an instruction routine is the Program Counter (PC) step. Depending on the complexity of the routine, the number of PC steps varies: only one is required to conclude many instructions, while sixteen are required for the division, D, routine. Each PC step is comprised of two distinct cycles, the Time-out (T0) cycle and the Time-on cycle (exceptions to this occur in the division, multiplication, and shift routines). Timeout is always one minor cycle (91 pulse times) in duration. Time-on, however, exists for as long a period as is necessary to complete the operations required during a particular PC step. Time-out provides time for the FT signals to become fully alerted and to perform some operations that require no FT signals. Time-on determines the life of the FT signals and, therefore, is essentially the time in which the operations to be performed during a PC step are accomplished.

The Function Table signals provide most of the control necessary to accomplish the computer routines. Each FT signal provides a unique function, the proper combination of which enables the computer to execute the various instructions. There are 101 discrete FT signals. For purposes of identification these are numbered, the numbers ranging between 100 and 861 . The appropriate $F T$

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signals are alerted by a signal generated from the proper combination of the instruction character code and the PC step during which the routine produced by the FT signal is to occur. A descriptive presentation of the FT signal decoding is made in Figure l, page 91.

The PC steps and the FT signals provide the basis for the instruction analysis. Subroutines occurring in the proper sequence produce the routines specified by the instructions.
2. GLOSSARY OF ABBREVIATIONS AND SYMBOLS.

AOC All Ones Checker
BC Binary Counter
BCI The binary counter which controls the order, right-hand or lefthand, of reference to a word in register I.

BCM The binary counter which controls the order, right-hand or lefthand, of reference to a word in main memory.

BCO The binary counter which controls the order, right-hand or lefthand, of reference to a word in register 0 .

Backward Interlock Release signal
BP Backward Pick-up signal
CC The Control Counter
Comp Comparison
CRI The 91 pulse register of the Control Register
CR2 The 42 pulse register of the Control Register
CT Conditional Transfer
CU The Cycling Unit
CY The Cycle Counter
EP Ending Pulse
FF Flip-flop
FIR Forward Interlock Release signal
FIR-BIR The Uniservo tape is in the First Block condition.
FT Function Table
FTIC The Function Table Intermediate Checker
FTOC The Function Table Output Checker
HSB The High-Speed Bus
IER The multiplIER signal
IER-OR A signal used by both multiplication and division routines
IO-INT Input-Output Interlock checker

IOS Interrupted Operation Switch
IRG Interlock Release Gate output
IRP Interlock Release Pulse
LE Leading Edge
LM Left-hand section of the main memory
LSB Least Significant Bit
LSD Least Significant Digit
$M_{1} \quad$ The half-word magnetic switching core register of the rMBit Plane Control

The half-word magnetic-switching core register of the rI Bit Plane Control

The half-word magnetic-switching core register of the r0 Bit Plane Control

The half-word magnetic-switching core register of the Output Distributor
min Minuend
MQC
MQC-FT The output matrix of MQC
MSD Most Significant Digit
MTO Memory Time Out
$N_{5} \quad$ The seven-bit magnetic-switching core register of the Input Distributor

Uniservo selector signal
Odd-Even
OEC Odd-Even Checker
OR The divisOR signal
PC The Program Counter
PPI Pulses per inch
PS Pulse Stretcher
rA
The one-word A register

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$: L$
rM

RM
ro
RP
rW
rX
rZ
S/NS
S1CP
SIX
S2

SC
SCI-CR
sub
t

TE
T0 Time-0ut
TRI Input section transfer pulses
TRO Output section transfer pulses
TT
TZ
WP
Z Decimal zero
( ) The contents of
Transmit
A word in rM from which a specified field is selected

Duplicated X register

## 3. ANALYSIS OF INSTRUCTIONS.

This section provides a detailed analysis of the various computer instructions. The instructions are listed in the binary order of the character code which specifies the routine. This code occupies the first-character position of the six-character instruction word. Where the instruction routine is altered by a symbol in the second character position, the routine is again presented but with the modification that has been made. An "F" in the second instruction character "field selects" the operand as it is transferred from storage and an " H " returns the results of an operation to storage. For the input-output operation, the second instruction character addresses the Uniservo required by the instruction. Other instruction modifications are made by use of the second instruction character. These are described in the instructions concerned. The " $m$ " section of the instruction word designates an address in storage.

The analysis of each instruction begins with a shorthand presentation of the routine to be accomplished by the instruction. Following this, and organized with regard to time of occurrence; i.e., by PC steps, is a description of the functions performed by the various FT signals that are alerted for the routine. In the column to the right of the page is the number of the FT signal described. Appropriate footnotes are supplied where clarification or qualification is necessary.

The CY outputs of $\beta, \beta$ COMPUTE, $\gamma$, and $\delta$ and the RETAIN INSTRUCTION routine are not considered instructions, but they do control FT signals as part of the automatic internal programming of the computer. The routine accomplished during these cycles and the FT signals required to perform these routines are described on page 7.

| Beta | (CC) $+1 \longrightarrow$ CC; $\mathrm{LH}(\mathrm{CR}) \longrightarrow$ SR Distributor <br> Set up adder for twelve-piace addition. Operate adder OE and sum comparison checkers. Connect CRI to SR Distributor Line. Connect CC to adder min input. Cycling Unit ( 000000000001 ) to adder sub input. Clear CC and read the sum from the unbarred adder to CC. (Transfer to CC ends $t 12$ of TO). <br> Supply reset pulse to Overflow FF's | 714 <br> 435 \} <br> $204+$ <br> 212 <br> 737 |
| :---: | :---: | :---: |
| Beta Computer | $(\mathrm{m}) \longrightarrow \mathrm{CR}$ <br> Operate rM address exceeded and preset checkers. <br> Set BCM to RM <br> Operate HSB - OEC. <br> Operate HSB - AOC. <br> Set rM Read FF, set Ml cores. <br> Strobe, rM sense amplifiers. <br> Develop Serialize Pulse. <br> Connect HSB to CR, and clear CR. <br> Set MTO. <br> Supply EP. <br> ( rM address sets up at $\mathrm{t7}$ of Beta TO, unless overflow occurs, which delays Set-up until t35, thereby setting SR to $Z^{\prime}$ s.) | 860 <br> 827 <br> 429 <br> 428 <br> 820 <br> 821 <br> 824 <br> $201+$ <br> 825 <br> 206 |
| Gamma | $\mathrm{RH}(\mathrm{CR}) \longrightarrow$ SR Distributor; Execute LH instruction. <br> Connect CR1 to CR2. <br> (LH Instruction sets up at t 7 of Gamma T0) | $\begin{aligned} & 203 \\ & 203 \mathrm{~K} \end{aligned}$ |
| Delta | $\mathrm{RH}(\mathrm{CC}) \longrightarrow$ SR Distributor; Execute RH Instruction. Connect CC to SR via CR2\#. <br> \#RH Instruction is set up at t 7 of Delta TO. | $850$ $203 \mathrm{~K}$ |
| RETAIN <br> INSTRUCTION | ```Repeat routine performed during a selected CY cycle. \beta cycle: Inhibit FT 201, 204,212, 435 Alert FT }85 cycle: Inhibit FT 203 Alert FT 204, 203K and specified in- struction FT signals \delta cycle: Inhibit FT }85 Alert FT 203, 203K and specified in- struction FT signals``` |  |

FT


\begin{tabular}{|c|c|c|}
\hline A F m

1. \& | $(\mathrm{m}) \longrightarrow \mathrm{rX}$; $(\mathrm{rX})+(r A) \longrightarrow r A$ |
| :--- |
| Operate rM address exceeded and preset checkers. Set BCM to RM. |
| 0 perate HSB - OEC. |
| operate HSB - AOC. |
| Set rM Read FF, set M1 Cores. |
| Strobe rM sense amplifiers. |
| Develop Serialize Pulse. |
| Connect HSB to rX. |
| Operate rX, clear gate. |
| Operate extract circuit in rF.* |
| Set MTO. |
| Step PC, Set T0. |
| *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from $r M$ is replaced with a decimal zero. | \& \[

$$
\begin{aligned}
& 860 \\
& 827 \\
& 429 \\
& 428 \\
& 820 \\
& 821 \\
& 824 \\
& 126 \\
& 120 \\
& 193 \\
& 825 \\
& 214
\end{aligned}
$$
\] <br>

\hline T0 \& Compare ( rA ) and ( rX ). \& NONE <br>

\hline 2. \& | Operate adder for eleven-place addition.* Operate adder $O E$ and sum comparison checkers. Connect rX to HSB. |
| :--- |
| Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA (Transfer to rA ends at tl2 of TO). Supply EP. |
| *If decimal carry occurs from eleventh digit position, set Overflow FF。 | \& \[

$$
\begin{aligned}
& 160 \\
& 435 \\
& 125 \\
& \\
& 109 \\
& 206
\end{aligned}
$$
\] <br>

\hline
\end{tabular}

FT

| A H m 1. | ```(m) }->\textrm{rX;}(\textrm{rA})+(rX)->rA; (rÅ)-> Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB - OEC. Operate HSB - AOC. Set rM Read FF, set M1 Cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Connect HSB to rX. Operate rX clear gate. Set MTO. Step PC, set TO.``` | 860 827 429 428 820 821 824 126 120 825 214 |
| :---: | :---: | :---: |
| T0 | Compare (rA) and ( XX ) . | NONE |
| 2 。 | Operate adder for eleven-place addition.* <br> Operate adder 0 E and sum comparison checkers. <br> Connect rX to HSB. <br> Connect HSB to adder sub input, rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer to rA ends at tl2 of T0.) Step PC, set TO. <br> *If decimal carry occurs from llth digit position, set Overfiow FF. <br> + FT206 is present, but its effect is suppressed by FT214. | $\begin{aligned} & 160 \\ & 435 \\ & 125 \\ & \\ & 109 \\ & 214 \\ & 206+ \end{aligned}$ |
| $\begin{gathered} \mathrm{TO} \\ 3 . \end{gathered}$ | Operate rM address exceeded and preset checkers. <br> Connect rA to HSB. <br> Operate HSB - OEC. <br> Operate HSB - AOC. <br> Set rM Read FF, set M1 Cores. <br> Develop Staticize Pulse. <br> Set MTO. <br> Supply EP. | $\begin{aligned} & 860 \\ & 100 \\ & 429 \\ & 428 \\ & 826 \\ & 823 \\ & 825 \\ & 206 \end{aligned}$ |

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INSTRUCTIONS

| B 0 m | $(\mathrm{m}) \longrightarrow \mathrm{rA}, \mathrm{rX}$. <br> Operate rM address exceeded and preset checkers. <br> Set BCM to RM. <br> Operate HSB - OEC. <br> operate HSB - AOC. <br> Set rM Read FF, set M1 Cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Connect HSB to rA. <br> Operate rA clear gate. <br> Connect HSB to rX. <br> Operate rX clear gate. <br> Set MTO. <br> Supply EP. | 860 827 429 428 820 821 824 105 101 126 120 825 206 |
| :---: | :---: | :---: |
| B F m | $(\underline{m}) \rightarrow r A_{i} r X$. <br> Operate rM address exceeded and preset checkers. <br> Preset BCM to RM. <br> Operate HSB - OEC. <br> Operate HSB - AOC. <br> Set rM Read FF, set $M_{1}$ Cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Operate Extract Circuit in rF.* <br> Connect HSB to rA. <br> Operate ra clear gate. <br> Connect HSB to rX. <br> Operate rX clear gate. <br> Set MTO. <br> Supply EP. <br> *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero. the digit from $r M$ is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero. | 860 827 429 428 820 821 824 193 105 101 126 120 825 206 |


| C 0 m | $(\mathrm{rA}) \longrightarrow \mathrm{m} ; \mathrm{Z} \longrightarrow \mathrm{rA}$ <br> Operate rM address exceeded and preset checkers. <br> Connect rA to HSB. <br> Operate HSB - OEC. <br> Operate HSB - AOC. <br> Set rM Read $\mathrm{FF}_{\mathrm{q}}$ set $\mathrm{M}_{1}$ Cores. <br> Develop Staticize Pulse。 <br> Operate ra clear gate. <br> Connect CU (000000 000000) to rA. <br> Set MTO. <br> Supply EP. | $\begin{aligned} & 860 \\ & 100 \\ & 429 \\ & 428 \\ & 826 \\ & 823 \\ & 101 \\ & 108 \\ & 825 \\ & 206 \end{aligned}$ |
| :---: | :---: | :---: |
| $\begin{aligned} & \text { D } 0 \mathrm{~m} \\ & 1 . \end{aligned}$ | $(\mathrm{m}) \rightarrow \mathrm{rA} ;(\mathrm{rA}) \div(r \mathrm{~L}) \longrightarrow r A$ rounded, $r X$ unrounded <br> Operate rM address exceeded and preset checker. <br> Preset BCM to RM. <br> Operate HSB - OEC. <br> Operate HSB - AOC. <br> Set rM Read FF, set $M_{1}$ Cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Connect HSB to rA. <br> Operate rA clear gate. <br> Delete rX input to comparator, connect HSB.* <br> Delete rA input to comparator, connect rL.* <br> Preset $\mathrm{BC}-120$ in MQC to non-complement position, <br> thus alerting the non-complementing gates between <br> MQC and MQC-FT. Clear MQC to decimal zero. <br> Set MTO. <br> Step PC , set TO . <br> *Sign comparison is performed between (rA) and (rL). | 860 827 429 428 820 821 824 105 101 152 151 138 825 214 |


| $\begin{gathered} \text { D } 0 \mathrm{~m} \\ \mathrm{~T} 0 \end{gathered}$$2 .$ |  |  |
| :---: | :---: | :---: |
|  |  |  |
|  | Retain results of sign comparison in comparator. Operate rA clear gate. <br> Operate rA left shift path (including sign).* <br> Insert decimal zero in LSD position of rA. <br> Set Repeat FF. <br> Step PC, set TO. <br> *Shifting (rA) left deletes sign digit. | $\begin{aligned} & 159 \\ & 101 \\ & 103 \\ & 171 \\ & 226 \\ & 214 \end{aligned}$ |
| T0 |  |  |
| 3. | Retain results of sign comparison in comparator. Operate adder for twelve-place addition. <br> Operate adder OE and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replacing sign digit with a decimal zero. Step PC upon completion of 0R CYCLE. Set T0 and Stop FF's after each time on minor cycle if IOS is in "One Addition". <br> Connect HSB to adder sub input, rA to adder min input clearing rA and transferring sum from adder to rA. <br> Gate non-complement output of $\mathrm{BC}-120$ as SIX signa to operate the complementer in adder sub, thus (rL) are subtracted from (rA). <br> Gate non-complement output of $\mathrm{BC}-120$ to operate Improper Division Detector in MQC.* Step MQC at t2 following each subtraction until the ThroughZero signal is developed, at which time generate OR CYCLE. $\#$ <br> If rA or rX comp error occurs, set $T 0$ at following $t 1$. <br> *If rL $\geq r A$, Improper Division occurs at $t 2$ of the eleventh minor cycle of PC-3. <br> \#The Through-Zero signal indicates that the subtraction produced a negative remainder, since no decimal carry occurred from the twelfth-digit position. At the beginning of the OR CYCLE, the MQC-FT will contain a digit equal to the number of subtractions performed minus the one which produced the Through-Zero signal. | 159 <br> 714 <br> 435 <br> 188 <br> 109 <br> 145 <br> 246 |


| $\text { D } 0 \mathrm{~m}$ <br> OR CYCLE | Delete functions of FTIO9, except HSB to adder sub input. <br> Inhibit the transfer of (rL) to HSB. <br> Delete functions of FT435. <br> Operate rA and rX clear gates. <br> Operate rX left shift path. Transfer quotient digit from MQC-FT to LSD position of rX. Clear $M Q C$ to decimal zero. Step $B C-120$ to alert the complement gates connecting the MQC and MQC-FT. (MQC-FT now reads nines complement of MQC.) Step PC at end of OR-CYCLE. <br> Operate rA left shift path inserting a decimal zero in the LSD position <br> Inhibit alerting signal to complementer and the stepping signal to the MQC. <br> NOTE: Those FT signals present on PC-3 are also present during the OR CYCLE, performing the same functions except as noted above. | $\begin{aligned} & \text { IER-OR }+1 \\ & \text { IER }=0 \mathrm{R}+2 \\ & \\ & \text { IER }-0 \mathrm{R}+3 \\ & \text { IER }-0 \mathrm{R}-2 \end{aligned}$ <br> 0R-1 <br> OR-2 <br> OR+1 |
| :---: | :---: | :---: |
| 4. | Retain results of sign comparison in comparator. Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replacing sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop $\mathrm{FF}^{\text {'s }}$ after each Time-on minor cycle if IOS is in "One Addition". <br> Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. <br> Step MQC at t2 following each addition, until the Through-Zero signal is developed, at which time, generate OR CYCLE.* <br> If rA or rX comp error occurs, set TO at following $t$. <br> *The Through-Zero signal indicates that the addition produced a positive number, since a decimal carry occurred from the twelfth digit position. At the beginning of the OR CYCLE, the MQC will contain a digit equal to the number of additions performed, minus the one which produced the Through-Zero signal, and the MQC-FT will contain the nines complement of this digit. | 159 <br> 714 <br> 435 <br> 188 <br> 109 <br> 145 <br> 246 |

ANALYSIS OF INSTRUCTIONS


| $\begin{aligned} & \text { D } 0 \mathrm{~m} \\ & \mathrm{TO} \\ & 15 \end{aligned}$ | Retain results of sign comparison in comparator. Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers. <br> Operate rA clear gate.* <br> Connect rX to HSB. <br> Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. <br> Connect CU (round-off, 000000000005 ) to adder min input. <br> Step PC, set TO. <br> *Operating rA's clear gate destroys the divide remainder and, consequently, nothing is read from rA to the adder min input. Thus the results of the addition are $(r X)+($ round $-0 f f) \longrightarrow r A$. | $\begin{aligned} & 159 \\ & 714 \\ & 435 \\ & 101 \\ & 125 \\ & \\ & 109 \\ & 111 \\ & 214 \end{aligned}$ |
| :---: | :---: | :---: |
| T0 |  |  |
| 16 | Retain results of sign comparison in comparator. <br> Operate rA clear gate. <br> Operate right shift path of rA. Transfer sign from comparator to rA and rX. <br> Operate rX clear gate. <br> Operate right shift path of rX. <br> Transfer sign from comparator to $r A$ and $r X_{8}$ deleting the insertion of a decimal zero to rA. Supply EP。 | $\begin{aligned} & 159 \\ & 101 \\ & \\ & 106 \\ & 120 \\ & 123 \\ & \\ & 161 \\ & 206 \end{aligned}$ |



ANALYSIS OF INSTRUCTIONS

| D F m |  |  |
| :---: | :---: | :---: |
| T0 |  |  |
| 3. | Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder $O E$ and sum comparison checkers. Connect rL to HSB . Transfer (rL) to HSB , replacing the sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop after each time on minor cycle if IOS is in "One Addition"。 <br> Connect HSB to adder sub inputs $r A$ to adder min input. Clear rA and transfer sum from adder to rA. <br> Gate non-complement output of $\mathrm{BC}-120$ as SIX signal to operate the Complementer on adder sub input, thus (rL) is subtracted from (rA). Gate non-complement output of $\mathrm{BC}-120$ to operate the Improper Division Detector in MQC.* Step MQC t2 following each subtraction, until the ThroughZero signal is developed, at which time generate OR CYCLE.\# <br> If rA or rX comp error occurs $\mathrm{s}_{8}$ set TO at following tl. <br> ${ }^{*}$ If $(r L) \leq(r A)$, Improper Division occurs at $t 2$ of the eleventh minor cycle of $\mathrm{PC}-3$. <br> \#The Through-Zero signal indicates that the subtraction produced a negative remainder, since no decimal carry occurred from the twelfth digit position. At the beginning of the OR CYCLE $s$ the MQC-FT will contain a digit equal to the number of subtractions performed minus the one which produced the Through-Zero signal. |  |
| OR CYCLE | Delete Functions of FT109, except HSB to adder sub input. <br> Inhibit the transfer of (rL) to HSB. <br> Delete functions of FT435. <br> Operate rA and rX clear gates. <br> Operate rX left shift path. Transfer quotient digit from MQC-FT to LSD position of rX. Clear $M Q C$ to decimal zero. Step $B C-120$ to alert the complement gates connecting the MQC and MQC-FT. (MQC-FT now reads nines complement of MQC) Step PC at end of OR CYCLE. <br> Operate rA left shift path, insert a decimal zero into the LSD position of (rA). <br> Inhibit alerting signal to complementer and the stepping signal to the MQC. <br> NOTE: Those FT signals present on PC-3 are also present during the OR CYCLE performing the same functions except as noted above. | $\begin{aligned} & \text { IER }-0 R+1 \\ & \text { IER }-0 R+2 \\ & \text { IER }-0 R+3 \\ & \text { IER }-0 R-2 \\ & \\ & 0 R-1 \\ & 0 R-2 \\ & \text { OR+1 } \end{aligned}$ |


| D F m | Retain results of sign comparison in comparator. Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers. Connect rL to IISB. Transfer (rL) to HSB replacing the sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop <br> FF's after each Time-on minor cycle if $10 S$ is in "One Addition". <br> Connect HSB to adder sub input, rA to adder min input. Clear rAs and transfer sum from adder to rA. <br> Step MQC at t 2 following each addition, until the Through-Zero signal is developed, at which time generate OR CYCLE.* <br> If rA or rX comp error occurs, set $T 0$ at following ti. <br> *The Through-Zero signal indicates that $t$ he addition produced a positive number since a decimal carry occurred from the twe fth digit position. At the beginning of the OR CYCLEs the WQC wili contain a digit equal to the number of additions performed, minus the one which produced the Through-Zero signal, and the MQC-FT will contain the nines complement of this digit. | 159 <br> 714 <br> 435 <br> 188 <br> 109 <br> 145 <br> 246 |
| :---: | :---: | :---: |
| 5-13 | All OR CYCLES are identical. All odd PC-Steps are identical to PC-3. All even PC-Steps are identical to PC-4. Initially the divisor, (rL), is subtracted from the shifted dividend, ( $\mathrm{r} A$ ), until the Through-Zero signal occurs, indicating that the remainder in rA is negative. During the OR CYCLE, ( rA ) and ( rX ) are shifted one digit position left, a decimal zero is inserted into the LSD position of rA and the quotient digit from the MQC-FT is inserted into the LSD position of $r X$. ( rL ) is then added to (rA) until the Through-Zero signal occurs, in this case indicating that (rA) is again positives and an OR CYCLE occurs. (rL) is thus alternately subtracted and added to (rA) as the quotient is built up in rX. After each OR CYCLE PC is stepped. |  |


| $\begin{array}{r} \text { D F m } \\ 14 . \end{array}$ | Retain results of sign comparison in comparator． Operate adder for twelve－place addition． <br> Operate adder OE and sum comparison checker． <br> Connect rL to HSB．Transfer（rL）to HSB，replac－ ing the sign digit with a decimal zero．Step PC upon completion of OR CYCLE．Set TO and Stop <br> FF＇s after each Time－on minor cycle if IOS is in ＂One Addition＂。 <br> Connect HSB to adder sub input，rA to adder min input．Clear rA and transfer sum from adder to rA． <br> Step MQC at t 2 following each addition，until the Through－Zero signal is developed，at which time generate OR CYCLE． <br> If rA or rX comp error occurs；set TO at following t1。 <br> Reset Repeat FF at end of OR CYCLE． <br> Set TO at end of OR CYCLE | 159 <br> 714 <br> 435 <br> 188 <br> 109 <br> 145 <br> 246 <br> 228 <br> 244 |
| :---: | :---: | :---: |
| OR CYCLE | Same as previous OR CYCLES，except that in addi－ tion： <br> Reset Repeat FF． <br> Set T0． | $\begin{aligned} & \text { IER-OR-1 } \\ & \text { OR-1 } \end{aligned}$ |
| T0 |  |  |
| 15. | Retain results of sign comparison in comparator． Operate adder for twelve－place addition． <br> Operate adder 0 E and sum comparison checker． <br> Operate rA clear gate。＊ <br> Connect rX to HSB． <br> Connect HSB to adder sub input，rA to adder min input．Clear rA and transfer sum from adder to rA． Connect CU roundoff，（ 000000 000005）to adder min input． <br> Step PC，set TO． <br> ＊Operating rA＇s clear gate destroys the divide remainder and，consequently，nothing is read from rA to the adder min input．Thus the results of the addition are：（rX）+ （round－off）$\longrightarrow \mathrm{rA}$ 。 | $\begin{aligned} & 159 \\ & 714 \\ & 435 \\ & 101 \\ & 125 \\ & \\ & 109 \\ & \\ & 111 \\ & 214 \end{aligned}$ |


| D F m |  |  |
| :---: | :---: | :---: |
| T0 |  |  |
| 16 | Retain results of sign comparison in comparator. Operate rA clear gate. <br> Operate right shift path of rA. Transfer sign from comparator to rA and rX. <br> Operate rX clear gate. <br> Operate right shift path of rX. <br> Transfer sign from comparator to rA and rX , delet ing the insertion of a decimal zero to rA. Supply EP. | 159 <br> 101 <br> 106 <br> 120 <br> 123 <br> 161 |
| E 0 m | (rF) Odd digits extracts (m) $\rightarrow$ rA. <br> Operate rM address exceeded and preset checker. <br> Set BCM to RM. <br> Operate HSB-0EC. <br> Operate HSB-AOC. <br> Set rM Read FF, Set M1 Cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse <br> Connect HSB to rA. <br> Operate rA clear gate. <br> Operate extract circuit in rF.* <br> Delete CU ( 000000000000 ) input to extract circuit and connect rA.* <br> Set MTO. <br> Supply EP. <br> *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero. the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from $r \mathrm{M}$ is deleted and the corresponding digit from rA is transferred to the HSB. | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & 821 \\ & 824 \\ & 105 \\ & 101 \\ & 193 \\ & 832 \\ & 825 \\ & 206 \end{aligned}$ |

ANALYSIS OF
INSTRUCTIONS

INSTRUCTION

| E F m | (rF) Even Digits Extracts ( m ) $\rightarrow \mathrm{rA}$; ( rA ) $\rightarrow \mathrm{m}$ <br> Operate rM address exceeded and preset checkers. Set BCM to RM. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF, set $M_{1}$ cores. <br> Strobe rin sense amplifiers. <br> Develop Serialize Pulse. <br> Connect HSB to rA. <br> Operate ra clear gate. <br> Operate extract circuit in rF.* <br> Complement the operation of the extract circuit." <br> Delete CU ( 000000 000000) input to extract circuit and connect rA. <br> Set MTO. <br> Step PC, set TO. <br> *Transfer is controlled by (rF).If the LSB of the corresponding digit in rF is a binary one, the digit from rM is read onto the HSB. If the LSB is a binary zero, the digit from rM is deleted and the corresponding digit from $\overline{\mathrm{r}} \hat{\mathrm{A}}$ is transîerred to HSB . + FP206 is present, but its effect is suppressed by FT214. | 860 827 429 428 820 821 824 105 101 193 831 832 825 214 $206+$ |
| :---: | :---: | :---: |
| $\begin{array}{r} \text { T0 } \\ 2 . \end{array}$ | Operate rM address exceeded and preset checkers. <br> Connect rA to HSB. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF, Set $M_{1}$ cores. <br> Develop Staticize Pulse. <br> Set MTO. <br> Supply EP. | $\begin{aligned} & 860 \\ & 100 \\ & 429 \\ & 428 \\ & 826 \\ & 823 \\ & 825 \\ & 206 \end{aligned}$ |
| F 0 m | $(\mathrm{m}) \rightarrow \mathrm{rF}$ <br> Operate rM address exceeded and preset checkers. <br> Set $B C M$ to RM. <br> Operate HSB-0EC. <br> Operate HSB-AOC. <br> Set rM Read FF, set $M_{1}$ cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Connect HSB to rF , and operate rF clear gate. <br> Set MTO. <br> Supply EP。 | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & 821 \\ & 824 \\ & 190 \\ & 825 \\ & 206 \end{aligned}$ |


| G 0 m | $(\mathrm{rF}) \rightarrow \mathrm{m}$ <br> Operate rM address exceeded and preset checkers. <br> Connect rF to HSB. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF, set $M_{1}$ cores. <br> Develop Staticize Pulse. <br> Set MTO. <br> Supply EP. | $\begin{aligned} & 860 \\ & 192 \\ & 429 \\ & 428 \\ & 826 \\ & 823 \\ & 825 \\ & 206 \end{aligned}$ |
| :---: | :---: | :---: |
| H 0 m | ```(rA)}->\textrm{m Operate rM address exceeded and preset checkers. Connect rÂ to HiSB. Operate HSB-OEC. Operate HSB-AOC Set rM Read FF, set M cores. Develop Staticize Pulse. Set MTO. Supply EP.``` | $\begin{aligned} & 860 \\ & 100 \\ & 429 \\ & 428 \\ & 826 \\ & 823 \\ & 825 \\ & 206 \end{aligned}$ |
| I 0 m | ```(rL)}->\textrm{m Operate rM address exceeded and preset checkers. Connect rL to HSB. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M1cores. Develop Staticize Pulse. Set MTO. Supply EP.``` | $\begin{aligned} & 860 \\ & 187 \\ & 429 \\ & 428 \\ & 826 \\ & 823 \\ & 825 \\ & 206 \end{aligned}$ |
| J 0 m | ```(rX)}->\textrm{m Operate rM address exceeded and preset checkers. Connect rX to HSB. Operate HSB-OEC. Operate HSB-AOC. Set rM read FF, set M1 cores. Develop Staticize Pulse. Set MTO. Supply EP.``` | $\begin{aligned} & 860 \\ & 125 \\ & 429 \\ & 428 \\ & 826 \\ & 823 \\ & 825 \\ & 206 \end{aligned}$ |

ANALYSIS OF INSTRUCTIONS

| K 0 | ```(rA)}->rL; Z T rA. Connect rA to HSB. Operate rA clear Gate. Connect CU (000000 000000) to rA. Connect HSB to rL, operating rL clear gate. Operate HSB-0EC. Operate HSB-AOC. Supply EP.``` | $\begin{aligned} & 100 \\ & 101 \\ & 108 \\ & 185 \\ & 429 \\ & 428 \\ & 206 \end{aligned}$ |
| :---: | :---: | :---: |
| L 0 m | ```\[ (m) \longrightarrow r L, r X \] \\ Operate rM address exceeded and preset checkers. \\ Set BCM to RM. \\ Operate HSB-OEC. \\ Operate HSB-AOC. \\ Set rM iead FF , set \(\mathrm{M}_{1}\) cores \\ Strobe rM sense amplifiers. \\ Develop Serialize Pulse. \\ Connect HSB to rL, operate rL clear gate. \\ Operate rX clear gate. \\ Connect HSB to IX input gate. \\ Supply EP. \\ Set MTO.``` | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & 821 \\ & 824 \\ & 185 \\ & 120 \\ & 126 \\ & 206 \\ & 825 \end{aligned}$ |
| L F m | $(\mathrm{m}) \longrightarrow \mathrm{rL}, \mathrm{rX}$ <br> Operate rM address exceeded and preset checkers. <br> Set BCM to RM. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF, set M1 Cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Operate extract circuit in rF.* <br> Connect HSB to rL, operate rL clear gate. <br> Operate rX clear gate. <br> Connect HSB to rX. <br> Set MTO. <br> Supply EP. <br> *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from $r M$ is replaced with a decimal zero. | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & 821 \\ & 824 \\ & 193 \\ & 185 \\ & 120 \\ & 126 \\ & 825 \\ & 206 \end{aligned}$ |

ANALYSIS OF
UNIVAC II

\begin{tabular}{|c|c|c|}
\hline \multirow[t]{2}{*}{M 0 m} \& \[
(\mathrm{m}) \rightarrow \mathrm{rX} ; \quad(\mathrm{rL}) \quad \mathrm{x} \quad(\mathrm{rX}) \longrightarrow \underset{\mathrm{rX}}{\mathrm{rA}} \quad \text { (rounded) } \begin{array}{ll}
11 \& \mathrm{MSD} \\
\text { ll } \& \mathrm{LSD}
\end{array}
\] \& \\
\hline \& \begin{tabular}{l}
Operate rM address exceeded and preset checkers. \\
Set BCM to RM. \\
Operate HSB-OEC. \\
Operate HSB-AOC. \\
Set rM Read Fr, set M1 cores. \\
Strobe rM sense amplifiers. \\
Develop Serialize Pulse. \\
Operate rA clear gate. \\
Connect CU ( 000000000000 ) to rA. \\
Connect rL to adder sub input. Transfer (rL) \\
to adder, replacing sign digit with a decimal zero \\
Connect rA to adder min input, clear rA, and read \\
sum from the adder to rA. (Transfer ends at tl2 of TO.)* \\
Operate adder OE and sum comparison checkers. \\
Connect HSB to rX. \\
Operate rX clear gate. \\
Preset \(\mathrm{BC}-120\) to the complement state, thereby alerting the complement gates connecting the MQC and MOC-FT. \\
Set MTO. \\
Step PC, set TO. \\
*If decimal carry occurs from eleventh digit position, set Overflow flip-flop.
\end{tabular} \& \begin{tabular}{l}
860 827 429 428 820 821 824 101 108 \\
110 \\
113 \\
435 \\
126 \\
120 \\
139 \\
825 \\
214
\end{tabular} \\
\hline \multirow[t]{2}{*}{T0

2} \& \& <br>

\hline \& | Operate adder for twelve-place addition. |
| :--- |
| Operate adder OE and sum comparison checkers. |
| Co nnect rL to sub input of adder. Transfer (rL) |
| to adder, replacing the sign digit with a decimal zero. |
| Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at tl2 of T0) |
| Step PC, set TO. | \& | 714 435 |
| :--- |
| 110 |
| 113 |
| 214 | <br>

\hline
\end{tabular}

\begin{tabular}{|c|c|c|}
\hline \[
\begin{array}{r}
\text { M } 0 \mathrm{~m} \\
\mathrm{~T} 0 \\
\\
3
\end{array}
\] \& \begin{tabular}{l}
Operate adder for twelve-place addition. Operate adder \(0 E\) and sum comparison checkers. Connect rL to sub input of adder. Transfer ( \(r \mathrm{~L}\) ) to adder, replacing the sign digit with a decimal zero. \\
Delete rA input to comparator and connect rL.* Connect rA to adder min input, clear rA, and read sum from adder to rA. (Transfer ends at t12 of T0.) \\
Step PC, set TO. \\
*rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and ( rX ), and the sign of the product is stored in the comparator.
\end{tabular} \& \[
\begin{aligned}
\& 714 \\
\& 435 \\
\& \\
\& 110 \\
\& 151 \\
\& \\
\& 113 \\
\& 214
\end{aligned}
\] \\
\hline \multirow[t]{2}{*}{\[
\begin{array}{r}
\mathrm{T0} \\
4 .
\end{array}
\]} \& \& \\
\hline \& \begin{tabular}{l}
Store results of sign comparison in comparator. Operate adder \(O E\) and sum comparison checkers. Operate HSB-OEC. \\
Operate HSB-AOC. \\
Connect rA to HSB \\
Operate rA clear gate. \\
Connect CU ( 000000 000000) to rA. \\
Connect HSB to rF, operate rF clear gate. \\
Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC and set the nines complement of the digit into the MOC. Connect rA to adder min input, clear rA, and read sum from adder to rA. (Transfer ends at tI2 of T0.) \\
Operate right shift path in rX \\
Operate rX clear gate. \\
Set Repeat flip-flop. \\
Step PC,set TO. \\
NOTE: At the completion of PC-4, rA contains the roundoff, rL contains the multiplicand, rF contains three times the multiplicand, rX contains the multiplier shifted one digit right, the MQC contains the nines complement of LSD shifted out of rX , and the comparator contains the sign of the product. The sign position of rX is vacant.
\end{tabular} \& 159
435
429
428
100
101
108
190

112

113
123
120
226
214 <br>
\hline
\end{tabular}

| M 0 m T0 |  |  |
| :---: | :---: | :---: |
| 5 | Store results of sign comparison in comparator. Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers. Connect rL and rF to the $\geq 3 \mathrm{FF}$ control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in One Addition. <br> Connect HSB to adder sub input, rA to adder min input, clear rA and transfer the sum from the adder to rA. <br> Sample (MOC-FT). If digit is < 3, reset the $\geq 3$ FF , which transfers ( rL ) to HSB, and supply one stepping pulse to MQC. If digit is $\geq 3$, set the $\geq 3$ FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit $=0$, set $I E R$ and IER-OR FF's at following $t_{2}$ 。 <br> If rA or rX comp error occurs, set TO at following $\mathrm{t}_{1}$. <br> NOTE: At the beginning of the operation, the MQCFT will contain the LSD from rX. If the digit is $\geq 3$, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the digit in the $M Q C-F T$ by three. If the digit in the MQC-FT is $<3$, the multiplicand ( rL ) is added to the partial product in rA and the MQC is stepped once. thus reducing the digit in the MQC-FT by one. <br> Successive additions occur until the digit in the MQC-FT is reducen to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain ( $r$ L) times the original LSD of (rX). | 159 <br> 714 <br> 435 <br> 188 <br> 109 <br> 147 |

ANALYSIS OF INSTRUCTIONS




M F m

T0
5
Store results of sign comparison in comparator.
Operate adder for twelve-place addition.
Operate adder $O E$ and sum comparison checkers.
Connect rL and rF to the $\geq 3 \mathrm{FF}$ control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in"One Addition".
Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA.
Sample (MQC-FT). If digit is $<3$, reset the $\geq 3 \mathrm{FF}$, which transfers (rL) to HSB, and supplies one stepping pulse to MQC. If digit is $\geq 3$, set the $\geq 3 \mathrm{FF}$, which transfers ( rF ) to HSB, and supplies three stepping pulses to MQC. If digit is $=0$, set IER and IER-OR FF's at following t2. If rA or rX comp error occurs, set $T 0$ at following tl.

NOTE: At the beginning of the operation, the MQCFT will contain the LSD from rX. If the digit is $\geq 3$, three times the multiplicand (rF) is added to the partial product in rA , and the MQC is stepped three times, thus reducing the digit in MQC-FT by three. If the digit in $M Q C-F T$ is $<3$, the multiplicand (rL) is added to the partial product in rA and MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in the MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).

IER CYCLE
Operate the right shift path of ra and insert a decimal zero into the sign position of (rA). Operate the right shift path of rX transferring LSD of $r X$ to the $M Q C$ distributor line. Operate rA and rX clear gates.
Clear MCC to binary zero and set up the complement of the LSD from ( $r X$ ) in the MOC.
Transfer LSD of (rA) to the MSD position of rX and step PC at the end of the IER CYCLE.
Inhibit the transfer of ( $r \mathrm{~L}$ ) and the decimal zero for the sign position of (rL) to the HSB.
Disconnect $r F$ from the HSB and inhibit the stepping of the MQC.
Inhibit the min input of the algebraic adder.
(Delete the functions of FT109)
Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435 )

IER-6
IER-4
IER-OR-2
IER-3
IER-1
IER-OR+2
IER +1
IER-OR+1

M F m
6
through
13

T0
15

PC 15
IER CYCLE

N 0 m
1

Same as PC-5.
Same as PC-5. .

| $\begin{gathered} \mathrm{N} 0 \mathrm{~m} \\ \mathrm{TO} \end{gathered}$ |  |  |
| :---: | :---: | :---: |
| 2 | Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing sign digit with a decimal zero. <br> Connect ra to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at t 12 of TO.) Step PC, set TO. | 714 <br> 435 <br> 110 <br> 113 <br> 214 |
| T0 |  |  |
| 3 | Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers. <br> Connect rL to sub input of adder. Transfer (rL) <br> to adder, replacing the sign digit with a decimal zero. <br> Delete rA input to comparator, connect rL.* <br> Connect râ to adder min input. Clear rÂ, and read sum from adder to rA. (Transfer ends at t12 of TO.) <br> Step PC, set TO. <br> *rX is connected to the comparator via a direct path. A sign comparison is performed between ( rL ) and ( rX ), and the sign of the product is stored in the comparator. | 714 <br> 435 <br> 110 <br> 151 <br> 113 <br> 214 |

DESCRIPTION

\begin{tabular}{|c|c|c|}
\hline \multirow[t]{2}{*}{\[
\begin{gathered}
\mathrm{N} 0 \mathrm{~m} \\
\mathrm{TO}
\end{gathered}
\]} \& \& \\
\hline \& \& \\
\hline 4 \& \begin{tabular}{l}
Store results of sign comparison in comparator. \\
Operate adder \(O E\) and sum comparison checkers \\
Operate HSB-OEC. \\
Operate \(\operatorname{HSB}-A O C\). \\
Connect rA to HSB. \\
Operate rA clear gate. \\
Connect CU ( 000000000000 ) to rA. \\
Connect HSB to rF, operate rF clear gate. \\
Connect CU ( 050000000000 ) to adder sub input. \\
Transfer the LSD of (rX) to the MQC and set up the nines complement of the digit into the MOC Connect rA to min input of the adder. Clear rA, and read sum from adder to rA. (Transfer ends at \(t 12\) of TO.) \\
Operate right shift path in rX. \\
Operate rX clear gate. \\
Set Repeat flip-flop. \\
Step PC, set TO. \\
NOTE: At the completion of \(\mathrm{PC}-4\), rA contains the roundoff. rL contains the multiplicand, rF contains three times the absolute value of the multiplicand, \(r X\) contains the multiplier shifted one digit right, the MQC contains the nines complement of LSD shifted out of \(r X\), and the comparator contains the sign of the product. The sign position of \(r X\) is vacant.
\end{tabular} \& 159
435
429
428
100
101
108
190

112

113
123
120
226
214 <br>
\hline
\end{tabular}

| N 0 m T0 |  |  |
| :---: | :---: | :---: |
| 5 | Store results of sign comparison in comparator. <br> Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers <br> Connect rL and rF to the $\geq 3 \mathrm{FF}$ control circuits. <br> Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". <br> Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. <br> Sample (MQC-FT). If digit is $<3$, reset the $\geq 3$ FF, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is $\geq 3$, set the $\geq 3 \mathrm{FF}$, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit is $=0$, set IER and IER-OR FF's at following t2. <br> If if or ix comp errón occurs, set to at following tl. <br> NOTE: At the beginning of the operation, the MQCFT will contain the LSD from $r X$. If the digit is $\geq 3$, three times the multiplicand ( $r F$ ) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the digit in $M Q C-F T$ by three. If the digit in the MOC-FT is $<3$, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX). | 159 <br> 714 <br> 435 <br> 188 <br> 109 <br> 147 <br> 246 |

## INSTRUCTION

DESCRIPTION
FT

| N 0 m <br> IER CYCLE <br> (PC-5) | Operate the right shifit path of râ and insert a decimal zero into the sign position of (rA). <br> Operate the right shift path of rX, transferring LSD of $r X$ to the MQC distributor line. <br> Operate rA and rX clear gates. <br> Clear MCC to binary zero and set up the complemen of the LSD from $r X$ in the MQC. <br> Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. <br> Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. <br> Inhibit the min input to the algebraic adder. (Delete the functions of FT109) <br> Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435.) | IER-6 <br> IER-4 <br> IER-OR-2 <br> IER-3 <br> IER-1 <br> IER-OR +2 <br> IER +1 <br> IER-OR+1 <br> IER-OR+3 |
| :---: | :---: | :---: |
| $\begin{gathered} 6 \\ \text { through } \\ 13 \\ 14 \end{gathered}$ | Same as PC=5. |  |
|  | Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE. | 244 |
| T0 |  |  |
| 15 | Same as PC-5 except for four additional FT signal which are used during PC-15 IER CYCLE. |  |
| PC 15 <br> IER CYCLE | Insert sign into sign position of (rA) and (rX). <br> Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. <br> Reset Repeat FF. <br> Supply EP. | 161 plus IER-5 <br> 149 plus <br> IER-1 <br> 228 plus <br> IER-0R-1 <br> 215-plus <br> IER-2 |

\begin{tabular}{|c|c|c|}
\hline N F m \& \begin{tabular}{l}
Operate rM address exceeded and preset checkers. Set BCM to RM \\
Operate HSB-OEC \\
Operate HSB-AOC \\
Set rM Read FF, set \(\mathrm{M}_{1}\) cores. \\
Strobe rM sense amplifiers. \\
Develop Serialize Pulse. \\
Operate rA clear gate \\
Connect CU (000000 000000) to rA. \\
Connect rL to adder sub input, transfer (rL) to adder, replacing sign digit with a decimal zero. Connect rA to adder min input. Clear rA, and read the sum from the adder to rA. (Transfer ends at tl2 of TO.)* \\
Operate adder OE and sum comparison checkers Operate extract control circuit in rF。+ Connect HSB to rX, via sign reversal gates.\# Operate rX clear gate. \\
Preset \(\mathrm{BC}-120\) to the complement state, thereby alerting the complement gates connecting the MQC to MQC-FT. \\
Set MTO. \\
Step PC, set TO. \\
*If decimal carry occurs from eleventh digit position, set Overflow flip-flop. \\
\#The sign reversal gates complement the LSB and check pulse of the sign digit during transfer to rX. \\
+Transfer is controlled by (rF). If the LSB of the corresponding digit in \(r F\) is a binary zero, the digit from \(r M\) is read onto the HSB. If the LSB is a binary one, the digit from \(r M\) is replaced with a decimal zero.
\end{tabular} \& 860
827
429
428
820
821
824
101
108

110

113
435
193
153
120

139
825
214 <br>
\hline
\end{tabular}

\begin{tabular}{|c|c|c|}
\hline \multicolumn{3}{|l|}{N F m} \\
\hline \multicolumn{3}{|l|}{T0} \\
\hline 2 \& \begin{tabular}{l}
Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing sign with a decimal zero. \\
Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at tl2 of TO.) \\
Step PC, set TO.
\end{tabular} \& \begin{tabular}{l}
714 \\
435 \\
110 \\
113 \\
214
\end{tabular} \\
\hline \multicolumn{3}{|l|}{T0} \\
\hline 3 \& \begin{tabular}{l}
Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign with a decimal zero. Delete rA input to comparator, connect rL.* Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at tl2 of TO.) \\
Step PC, set TO. \\
*rX is connected to the comparator via a direct path. A sign comparison is performed between ( rL ) and ( rX ), and the sign of the product is stored in the comparator.
\end{tabular} \& 714
435

110
151

113
214 <br>
\hline
\end{tabular}

| NFm |  |  |
| :---: | :---: | :---: |
| T0 |  |  |
|  | Store results of sign comparison in comparator. | 159 |
|  | Operate adder OE and sum comparison checkers. | 435 |
|  | Operate HSB-OEC. | 429 |
|  | Operate HSB-AOC. | 428 |
|  | Connect ra to HSB. | 100 |
|  | Operate rA clear gate. | 101 |
|  | Connect CU (000000 000000) to rA. | 108 |
|  | Connect HSB to rF, operate rF clear gate. Connect CU (050000 000000) to adder sub input. | 190 |
|  | Connect CU (050000 000000) to adder sub input. Transfer the LSD of ( rX ) to the MQC, set up the |  |
|  | nines complement of the digit into the MQC. Connect rA to min input of the adder. Clear rA, and read sum from adder to rA. (Transfer ends | 112 113 |
|  | at $t 12$ of TO.) | 113 |
|  | Operate right shift path in rX. | 123 |
|  | Operate rX clear gate. | 120 |
|  | Set Repeat flip-flop. | 226 |
|  | Step PC, set TO. | 214 |
|  | NOTE: At the completion of PC-4, rA contains the roundoff, rL contains the multiplicand, rF contains three times the absolute value of the multiplicand, rX contains the multiplier shifted one digit right, the MQC contains the nines complement of LSD shifted out of $r X$, and the comparator contains the sign of the product. The sign position of rX is vacant. |  |


| $\begin{array}{r} \mathrm{NFm} \\ \mathrm{TO} \end{array}$ |  |  |
| :---: | :---: | :---: |
| 5 | Store results of sign comparison in comparator. Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers. <br> Connect rL and rF to the $\geq 3 \mathrm{FF}$ control circuits. Transfer of (rL) to the HSB and replace the sign digit with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS, is in"One Addition". <br> Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. <br> Sample (MQC-FT). If digit is $<3$, reset $\geq 3 \mathrm{FF}$, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is $\geq 3$, set the $\geq 3$ FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit is $=0$, set IER and IER-OR FF's at following t2. <br> If rA or rX comp error occurs, set TO at following tl. <br> NOTE: At the beginning of the operation, the MQCFT will contain the LSD from $r X$. If the digit is $\geq 3$, three times the multiplicand ( rF ) is added to the partial product in $r A$, and the $M O C$ is stepped three times, thus reducing the MQC-FT by three. If the digit in MOC-FT is $<3$, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX). | 159 714 435 <br> 188 <br> 109 <br> 147 <br> 246 |



| P 0 m | $\begin{aligned} (\mathrm{m}) \rightarrow \mathrm{rX} ;(\mathrm{rL}) X(\mathrm{rX}) \rightarrow \mathrm{rA} & =11 \mathrm{MSD} \cdot \mathrm{~s}, \\ \mathrm{rX} & =11 \mathrm{LSD}, \end{aligned}$ <br> Operate rM Address exceeded and preset checkers. <br> Set BCM to RM. <br> Operate HSB-AOC. <br> Operate HSB-OEC. <br> Set rM Read FF, set $M_{1}$ cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Operate rA clear gate. <br> Connect CU ( 000000 000000) to rA. <br> Connect rL to adder sub input, transfer <br> ( $r \mathrm{~L}$ ) to adder and replace sign digit of ( rL ) <br> with a decimal zero. <br> Connect rA to adder min input, Clear rA and read sum from adder to rA. (Transfer ends at $t 12$ of TO.)* <br> Operate adder $O E$ and sum comparison checkers. <br> Connect HSB to rX. <br> Operate rX ciear gate. <br> Preset $\mathrm{BC}-120$ to the complement state, thereby alerting the complement gates connecting the $M Q C$ and $M Q C-F T$. <br> Set MTO. <br> Step PC, set TO. <br> *If decimal carry occurs from the eleventh digit position, set Overflow FF. |  |
| :---: | :---: | :---: |
| $\begin{array}{r} \text { T0 } \\ 2 \end{array}$ |  |  |
|  | Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers. <br> Connect rL to sub input of adder, transfer (rL) <br> to adder, replacing the sign digit with a decimal zero. <br> Connect rA to adder min input. Clear rA and read sum from adder to rA. <br> Step PC, set TO. | 714 <br> 435 <br> 110 <br> 113 <br> 214 |


| $\begin{array}{r} \text { PO m } \\ \text { T0 } \end{array}$ |  |  |
| :---: | :---: | :---: |
|  | Operate adder for twelve-place addition. Operate adder 0 E and sum comparison checkers. Connect rL to sub input of adder, transfer (rL) to adder, replacing the sign digit with a decimal zero. <br> Delete rA input to comparator and connect rL.* Connect rA to adder min input. Clear rA and read sum from adder to ra. <br> Step PC, set TO. <br> *rX is connected to the comparator via a direct path. A sign comparison is performed between ( rL ) and ( rX ), and the sign of the product is stored in the comparator. | $\begin{aligned} & 714 \\ & 435 \\ & \\ & 110 \\ & 151 \\ & 113 \\ & 214 \end{aligned}$ |
| T0 |  |  |
| 4 | Store results of sign comparison in comparator. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Connect rA to HSB. <br> Operate rA clear gate. <br> Connect CU (000000 000000) to rA. <br> Connect HSB to rF and operate rF clear gate. <br> Connect CU ( 050000 000000) to adder sub input. <br> Transfer the LSD of (rX) to the MQC and set up the nines complement of the digit into the MQC. <br> Operate right shift path in rX. <br> Operate rX clear gate. <br> Set Repeat FF. <br> Step PC, set TO. <br> NOTE: At the completion of PC-4, rA contains decimal zeros, rL contains the multiplicand, rF contains three times the multiplicand, and rX contains the multiplier shifted one digit right, the MQC contains the nines complement of the LSD shifted out of $r X$, and the comparator contains the sign of the product. The sign position of rX is vacant. | $\begin{aligned} & 159 \\ & 429 \\ & 428 \\ & 100 \\ & 101 \\ & 108 \\ & 190 \\ & \\ & 112 \\ & 123 \\ & 120 \\ & 226 \\ & 214 \end{aligned}$ |


| $\begin{gathered} \text { P } 0 \mathrm{~m} \\ \text { TO } \\ \text { PC-5 } \end{gathered}$ |  |  |
| :---: | :---: | :---: |
|  | Store result of sign comparison in comparatór. Operate adder for twelve-place addition. <br> Operate adder $O E$ and sum comparison checkers. <br> Connect ri and rF to the $\geq 3$ FF control circuits. <br> Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". <br> Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. <br> Sample (MQC-FT). If digit is < 3, reset the $\geq 3 \mathrm{FF}$, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is $\geq 3$, set the $\geq 3 \mathrm{FF}$, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit $=0$, set IER and IER OR FF's at following t2. <br> If rA or rX comp. error occurs, set to FF at following tl. <br> NOTE: At the beginning of the operation, the $M O C-F T$ will contain the LSD from $r X$. If the digit is $\geq 3$, three times the multiplicand ( rF ) is added to the partial product in rA, and the MOC is stepped three times, thus reducing the digit in the MOC-FT by three. If the digit in the MQC-FT is $<3$, the multiplicand (rL) is added to the partial product in rA and the MOC is stepped once, thus reducing the digit in the MOC-FT by one. Successive additions occur until the digit in the $M Q C-F T$ is reduced to zero, at which time the IER CYCLE, rA will contain (rL) times the original LSD of (rX). | 159 <br> 714 <br> 435 <br> 188 <br> 109 <br> 147 <br> 246 |
| $\begin{aligned} & \text { IER } \\ & \text { PC-5 } \end{aligned}$ | Operate the right shift path of ra and insert a decimal zero into the sign position. <br> Operate the right shift path of rX, including the sign, transfer LSD of rX to the MQC distributor line. Operate rA and rX clear gates. <br> Clear MQC to binary zero and set up the complement of the LSD from $r X$ in the $M Q C$. <br> Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. <br> Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. <br> Disconnect rF from the HSB and inhibit the stepping of the MQC. <br> Inhibit the min input to the algebraic adder. <br> (Delete the functions of FT109) <br> Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435.) | $\begin{aligned} & \text { IER-6 } \\ & \text { IER-4 } \\ & \text { IER-0R-2 } \\ & \text { IER-3 } \\ & \text { IER-1 } \\ & \text { IER-0R+2 } \\ & \text { IER+1 } \\ & \text { IER-OR+1 } \\ & \text { IER-OR+3 } \end{aligned}$ |


| P 0 m <br> 6 <br> Through | Same as PC-5. |  |
| :---: | :---: | :---: |
| PC-14 | Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE. | 244 |
| IER PC-15 | Insert sign into the sign position of (rA) and ( $r X$ ). Inhibit the generation of a second IER CYCLE. in case a decimal zero is set up in the MQC. <br> Reset Repeat FF. <br> Supply EP. | 161 Plus IER-5 <br> 149 Plus <br> IER-1 <br> 228 Plus <br> IER-OR-1 <br> 215 Plus <br> IER-2 |
| P F m | $\begin{aligned} &(\underline{m}) \longrightarrow r X ;(r L) X(r X) \longrightarrow r A, \quad 11 M S D^{i} s \\ & r X, \text { 11 } L S D^{i} s \end{aligned}$ |  |
| 1 | Operate rM address exceeded and preset checkers. | 860 |
|  | Set BCM to RM. | 827 |
|  | Operate HSB-0EC. | 429 |
|  | Operate HSB-AOC. | 428 |
|  | Set rM Read FF, set M cores. | 820 |
|  | Strobe rM sense amplifiers. | 821 |
|  | Develop Serialize Pulse. | 824 |
|  | Operate ra clear gate. | 101 |
|  | Connect CU ( 000000000000 ) to rA. <br> Connect rL to adder sub input, transfer (rL) | 108 |
|  | to adder, replacing sign digit with a decimal zero. Connect rA to adder min input. Clear rA, and read the sum from the adder to rA. (Transfer ends at | 110 113 |
|  | $t 12$ of TO.)** <br> Operate adder OE and sum comparison checkers. | $\begin{aligned} & 113 \\ & 435 \end{aligned}$ |
|  | Operate extract control circuit in rF.+ | 193 |
|  | Connect HSB to rX. | 126 |
|  | Operate rX clear gate. <br> Preset $\mathrm{BC}-120$ to the complement state, thereby alerting the complement gates connecting the MQC to the MOC-FT. | 120 139 |
|  | Set MTO. | 825 |
|  | Step PC, set TO. | 214 |
|  | *If decimal carry occurs from eleventh digit position, set Overflow flip-flop. |  |
|  | + Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero. |  |

FT


\begin{tabular}{|c|c|c|}
\hline \& \& <br>
\hline P F m
T0

5 \& | Store results of sign comparison in comparator. |
| :--- |
| Operate adder for twelve-place addition. |
| Operate adder OE and sum comparison checkers. |
| Connect rL and rF to the $\geq 3 \mathrm{FF}$ control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. |
| Step PC at end of each IER CYCLE. Set TO and stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". |
| Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to ra. |
| Sample (MุC-FT). If digit is < 3, reset $\geq 3 \mathrm{FF}$, which transfers (rL) to HSB and supplies one stepping pulse to $M Q C$. If digit is $\geq 3$, set the $\geq 3 \mathrm{FF}$, which transfers (rF) to HSB and supplies three stepping pulses to MOC. If digit is $=0$, set IER and IER-OR FF at following t2. |
| If rA or rX comp error occurs, set TO FF at following tl. |
| NOTE: At the beginning of the operation, the MQCFT will contain the LSD from rX. If the digit is $\geq 3$, three times the multiplicand ( rF ) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the MQC-FT by three. If the digit in MQC-FT is < 3, the multiplicand ( rL ) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in MOC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of ( rX ). | \& 159

714
435

188

109

147
246 <br>

\hline | P F m |
| :--- |
| IER CYCLE |
| (PC-5) | \& | Operate the right shift path of rA, inserting a decimal zero into the sign position. Operate the right shift path of $r X$, transferring LSD of $r X$ to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement of the LSD from ( rX ) in the MOC. |
| :--- |
| Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. |
| Inhibit the transfer of (rL), and the decimal zero for the sign position of (rL) to the HSB. |
| Disconnect rF from the HSB and inhibit the stepping of the MOC. |
| Inhibit the min input to the algebraic adder. (Delete the functions of FT109.) |
| Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435.) | \& | IER-6 |
| :--- |
| IER-4 |
| IER-OR-2 |
| IER-3 |
| IER-1 |
| IER-OR+2 |
| IER +1 |
| IER-OR +1 $\text { IER-OR }+3$ | <br>

\hline
\end{tabular}

| $\begin{gathered} \text { P F M } \\ 6 \\ \text { through } \\ 13 \end{gathered}$ | Same as PC-5. |  |
| :---: | :---: | :---: |
| 14 <br> T0 <br> 15 | Same as PC-5 except for one additional FT signal which is used to set $T 0$ at the end of the IER CYCLE. | 244 |
|  |  |  |
|  | Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE. |  |
| PC-15 <br> IER CYCLE | Insert sign in sign position of (rA), (rX). <br> Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. <br> Reset Repeat FF。 <br> Supply EP. | 161 Plus IER 5 <br> 149 Plus IER-1 228 Plus IER-OR-1 215 Plus IER 2 |
| Q n m | If $(r A)=(r L)$, Transfer control $\longrightarrow m$. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Connect rL to HSB. <br> Eanble comparator to perform equality comparison.* <br> Delete rX input to comparator and connect HSB. <br> If 2nd Instruction Digit " $n$ " equals Conditional <br> Transfer Breakpoint Selector setting, pass tl to <br> set Stop FF. <br> Step PC, set TO. <br> *If (rA) $=$ (rL), the Conditional Transfer FF is set at t 5 of $\mathrm{PC}-2 \mathrm{TO}$. | 429 <br> 428 <br> 187 <br> 156 <br> 152 <br> 236 <br> 214 |
| T0 2 | Retain results of comparison in comparator. Operate HSB-OEC. <br> Operate HSB-AOC. <br> Connect CR and CU (000000 00) to HSB.* If Conditional Transfer FF is set, connect HSB to CC and operate CC clear gate. Supply EP. <br> *The four LSD's of (CR) are merged with eight decimal zeros from CU to make the complete word which is transferred to the HSB. | $\begin{aligned} & 159 \\ & 429 \\ & 428 \\ & 200 \\ & 209 \\ & 206 \end{aligned}$ |

\begin{tabular}{|c|c|c|}
\hline \[
\text { R } 0 \mathrm{~m}
\] \& \begin{tabular}{l}
\[
\text { (000000 UO (CC) } \quad) \longrightarrow m
\] \\
Operate rM address exceeded and preset checkers. \\
Operate HSB-OEC. \\
Operate HSB-AOC. \\
Connect CC and CU (000000 UO) to HSB.* \\
Set rM Read FF , set \(\mathrm{M}_{1}\) cores. \\
Develop Staticize Pulse. \\
Set MTO. \\
Supply EP. \\
*The four LSD's of (CC) are merged with ( 000000 UO ) from the CU to make the complete word which is transferred to the HSB.
\end{tabular} \& \[
\begin{aligned}
\& 860 \\
\& 429 \\
\& 428 \\
\& 245 \\
\& 826 \\
\& 823 \\
\& 825 \\
\& 206
\end{aligned}
\] \\
\hline S 0 m

1 \& | $-(m) \longrightarrow r X ; \quad(r X)+(r A) \longrightarrow r A$ |
| :--- |
| Operate rM address exceeded and preset checkers. |
| Set BCM to RM. |
| Operate HSB-OEC. |
| Operate HSB-AOC. |
| Set rM Read FF, set $M_{1}$ cores. |
| Strobe rM sense amplifiers. |
| Develop Serialize Pulse. |
| Connect HSB to rX via sign reversal gates.* |
| Operate rX clear gate. |
| Set MTO. |
| Step PC, set TO. |
| *The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX. | \& 860

827
429
428
820
821
824
153
120
825
214 <br>
\hline т0 \& Compare ( IA ) and ( rX ). \& None <br>

\hline 2 \& | Operate adder for eleven place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. |
| :--- |
| Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. |
| Supply EP. |
| *If decimal carry occurs from eleventh digit position, set Overflow FF. If Second Instruction Digit is a minus sign, overflow sets Stop FF. | \& \[

$$
\begin{aligned}
& 160 \\
& 435 \\
& 125 \\
& \\
& 109
\end{aligned}
$$
\] <br>

\hline
\end{tabular}

| S F m | $-(\underline{m}) \rightarrow r X ;(r X)+(r A) \rightarrow r A .$ <br> Operate rM address exceeded and preset checkers. <br> Set BCM to RM. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF, set M1 cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Connect HSB to rX via sign reversal gates.+ <br> Operate rX clear gate. <br> Operate extract circuit in rF.* <br> Set MTO. <br> Step PC, set TO. <br> *Transfer is controlled by (rF). If the LSB of the corresponding digit in $r F$ is a binary zero, the digit from $r M$ is read onto the HSB. If the LSB is a binary one, the digit from $r M$ is replaced with a decimal zero. <br> +The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX. | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & 821 \\ & 824 \\ & 153 \\ & 120 \\ & 193 \\ & 825 \\ & 214 \end{aligned}$ |
| :---: | :---: | :---: |
| T0 | Compare (rA) and (rX). | None |
| 2 | Operate adder for eleven place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. <br> Connect HSB to adder sub input and rA to adder min input. Clear rA and transfer sūn from adder to rA. <br> Supply EP. <br> *If decimal carry occurs from eleventh digit position, set Overflow FF. | $\begin{aligned} & 160 \\ & 435 \\ & 125 \\ & \\ & 109 \\ & 206 \end{aligned}$ |

ANALYSIS OF INSTRUCTIONS
INSTRUCTION

| SHm | $-(m) \longrightarrow r X ; \quad(r X)+(r A) \longrightarrow r A \longrightarrow \dot{m}$ <br> Operate rM address exceeded and preset checkers. <br> Set BCM to RM. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF, set $M_{1}$ cores. <br> Strobe rM sense amplifiers. <br> Develop Serial Pulse. <br> Connect HSB to rX via sign reversal gates.* <br> Operate rX clear gate. <br> Set MTO. <br> Step PC, set TO. <br> *The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX. | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & 821 \\ & 824 \\ & 153 \\ & 120 \\ & 825 \\ & 214 \end{aligned}$ |
| :---: | :---: | :---: |
| T0 | Compare (rA) and (rX). | None |
| $2$ | Operate adder for eleven place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. <br> Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. <br> Step PC, set TO. <br> *If decimal carry occurs from eleventh digit position, set Overflow FF. <br> + FT206 is present, but its effect is suppressed by FT214. | $\begin{aligned} & 160 \\ & 435 \\ & 125 \\ & \\ & 109 \\ & 214 \\ & 206+ \end{aligned}$ |
| 3 | Operate rM address exceeded and preset checkers. <br> Connect rA to HSB. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF, set $M_{1}$ cores. <br> Develop Staticize Pulse. <br> Set ITTO. <br> Supply EP. | $\begin{aligned} & 860 \\ & 100 \\ & 429 \\ & 428 \\ & 826 \\ & 823 \\ & 825 \\ & 206 \end{aligned}$ |

ANALYSIS OF INSTRUCTIONS


| V nm | $(\mathrm{m}),(\mathrm{m}+1) \cdot . \cdot(\mathrm{m}+\mathrm{n}-1) \longrightarrow \mathrm{r} W$ <br> Operate rM address exceeded and preset checkers. Set BCM to RM. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF , set $\mathrm{M}_{1}$ cores. <br> Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When the rZW units counter reads zero, gate a t59 to set MT0.*+\# <br> Read and restore rZW simultaneously with the reading and restoring of rM. When MTO is set, supply EP. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Step rM counters and rZW units counter once each minor cycle until rZW units counter reads zero. Supply EP. <br> *If 2nd Instruction Digit is a zero and if compatibility switch on SC is set to Univac II, treat instruction as a Skip. <br> +If Compatibility switch is set to Univac I, the rZW units counter is unconditionally set to nine. <br> \#The "Tens" 7 or $W$ line is always up except during the $Y$ or $Z$ instructions. | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & \\ & 817 \\ & \\ & \\ & 818 \\ & 821 \\ & 824 \\ & 833 \\ & 206 \end{aligned}$ |
| :---: | :---: | :---: |


| W n m | $(r W) \longrightarrow m, m+1 \ldots \ldots m+n-1$ <br> Operate rM address exceeded and preset checkers. Set BCM to RM. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF, set $M 1$ cores. <br> Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When the rZW units counter reads zero, gate a t59 to set MTO.*+\# Read and restore rZW simultaneously with the reading and restoring of rM . When MTO is set, supply EP. <br> Strobe rZW sense amplifiers. <br> Develop Serialize Pulse. <br> Step rM counters and rZW units counter once each minor cycle until rZW units counter reads zero. Supply EP. <br> *If 2nd Instruction Digit is a zero and if Compatibility switch on SC is set to Univac II, treat instruction as a Skip. <br> +If Compatibility switch is set to Univac I the rZW units counter is unconditionally set to nine. <br> "The "Tens" 7 or $W$ line is always up except during the $Y$ or $Z$ instructions. | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & \\ & 817 \\ & \\ & 818 \\ & 819 \\ & 824 \\ & \\ & 833 \\ & 206 \end{aligned}$ |
| :---: | :---: | :---: |
| X 0 m | $(r A)+(r X) \longrightarrow r A$ |  |
| T0 | Compare (rA) and (rX). | None |
|  | Operate adder for eleven place addition.* <br> Operate adder OE and sum comparison checkers. <br> Connect rX to HSB. <br> Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. <br> Supply EP. <br> *If decimal carry occurs from eleventh digit position, set Overflow FF. If second instruction digit is a minus sign, overflow sets Stop FF. | $\begin{aligned} & 160 \\ & 435 \\ & 125 \\ & \\ & 109 \\ & 206 \end{aligned}$ |

$$
x_{0}
$$

| Y n m | $(m),(m+1) \ldots \ldots . .(m+10 n-1) \longrightarrow r Z$ <br> Operate rM address exceeded and preset checkers. <br> Set BCM to KM . <br> Operate HSB-OEC. <br> Operate HSB-AOC <br> Set rM Read FF, set $M_{1}$ cores. <br> Preset rZW tens counter to elevens complement of the 2nd Instruction Digit. Preset rZW units counter to one. <br> When the rZW tens and units counters read zero, gate a 559 to set MTO. *+ <br> Read and restore rZW simultaneously with the reading and restoring of rM . When MTO is set, supply EP. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Step rM counters and rZX units counter once each minor cycle. When the rZW units counter passes trhough zero it steps the rZW tens counter. Supply EP. <br> *If 2nd Instruction Digit is a 7, 8, 9, or 0, and if Compatibility switch on SC is set to Univac II, treat instruction as a Skip. <br> +If Compatibility switch is set to Univac I, the rZW tens counter is preset to zero. | 860 827 429 <br> 428 <br> 820 <br> 816 <br> 818 <br> 821 <br> 824 <br> 833 <br> 206 |
| :---: | :---: | :---: |
| 2 n m | $(r Z) \rightarrow m, m+1 \ldots \ldots \ldots \ldots m^{m+10 n-1}$ <br> Operate rM address exceeded and preset checkers. <br> Set BCM to RM. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rM Read FF , set $\mathrm{M}_{1}$ cores. <br> Preset rZW tens counter to elevens complement of the 2nd Instruction Digit. Preset rZW units counter to one. <br> When the rZW tens and units counters read zero, gate a 559 to set MTO. *+ <br> Read and restore rZW simultaneously with the reading and restoring of rM . When MTO is set, supply EP. <br> Strobe rZW sense amplifiers. <br> Develop Serialize Pulse. <br> Step rM counters and rZW units counter once each minor cycle. When the rZW units counter passes through zero it steps the rZW tens counter. <br> Supply EP. <br> *If 2nd Instruction Digit is a 7, 8. 9, or 0, and if Compatibility switch on SC is set to Univac II, treat instruction as a Skip. <br> +If Compatibility switch is set to Univac $I$, the rZW tens counter is preset to zero. | $\begin{aligned} & 860 \\ & 827 \\ & 429 \\ & 428 \\ & 820 \\ & \\ & \\ & 816 \\ & \\ & 818 \\ & 819 \\ & 824 \\ & \\ & 833 \\ & 206 \end{aligned}$ |


| . n m <br> Aill | Shift ra right, with sign, n places |  |
| :---: | :---: | :---: |
|  | Preset rZ̄W units counter to the elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO. <br> Operate rA clear gate. <br> Operate right shift path of rA and insert a decimal zero into the sign position.* <br> Step rZW and rM counters once each minor cycle until rZW units counter reads zero. <br> Step PC once per minor cycle. + When MTO is set, supply EP at following tl. <br> *rA shifts one digit right during each minor cycle of Time-on. <br> +If PC is adyanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting the FT Intermediate Checker FF, and TO. | $\begin{gathered} 817 \\ 101 \\ 106 \\ \\ 833 \\ 213 \\ 818 \end{gathered}$ |
| -n m <br> All | Shift rA right, without sign, n places |  |
|  | Preset rZW units counter to the elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO. <br> Operate rA clear gate, except for sign position. Operate right shift path of rA and insert a decimal zero into the (MSD) position.* Step $r Z W$ and $r M$ counters once each minor cycle until rZW units counter reads zero. Step PC once each minor cycle. + When MTO is set, supply EP and set TO at following tl. <br> *ra shifts one digit right during each minor cycle of Time-on. <br> +If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting the FT Intermediate Checker FF and T0. | $\begin{aligned} & 817 \\ & 170 \\ & 107 \\ & 833 \\ & 213 \\ & \\ & 818 \end{aligned}$ |


| $\begin{gathered} ; \mathrm{n} \mathrm{~m} \\ \text { All } \end{gathered}$ | Shift rA left, with sign, n places |  |
| :---: | :---: | :---: |
|  | Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When counter reads zero, gate $t 59$ to set MTO. Operate rA clear gate. Operate left shift path of rà. * Insert decimal zero into LSD position of (rA). Step rZW and rM counters once each minor cycle until rZW units counter reads zero. Step PC once each minor cycle. + When MTO is set, supply EP and set TO at following tl. <br> *rA shifts one digit left during each minor cycle of Time-on. <br> +If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting FT Intermediate Checker FF and TO. | $\begin{aligned} & 817 \\ & 101 \\ & 103 \\ & 171 \\ & 833 \\ & 213 \\ & 818 \end{aligned}$ |
| 0 n m All | Shift rA left, without sign, n places |  |
|  | Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When counter reads zero, gate $t 59$ to set MTO. <br> Operate rA clear gate, except for sign position. Operate left shift path of rA. * <br> Insert decimal zero into LSD position of (rA). Step rZW and rM counters once each minor cycle until rZW units counter reads zero. <br> Step PC once each minor cycle. + When MTO is set, supply EP at following $t 1$. <br> *rA shifts one digit left during each minor cycle of Time-on. <br> +If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting FT Intermediate Checker FF and TO. | $\begin{aligned} & 817 \\ & 170 \\ & 104 \\ & 171 \\ & 833 \\ & 213 \\ & 818 \end{aligned}$ |


| 00 m | Skip instruction (Supply Ending Pulse and proceed to next iñstruction) Supply EP. | 206 |
| :---: | :---: | :---: |
| 0 m | Stop computation if Breakpoint switch on SC is depressed <br> Set Stop FF if Breakpoint switch is depressed. Supply EP. | $\begin{aligned} & 217 \\ & 206 \end{aligned}$ |
| 90 m | Stop computation Set Stop FF. Supply EP. | $\begin{aligned} & 218 \\ & 206 \end{aligned}$ |
| $1 \mathrm{~nm}$ | 60 words from tape to rI, forward <br> Gate nS (Servo Selector) signal from second Instruction Digit to determine if Uniservo desired will pass interlock. <br> Gate, FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read operation. $\neq+$ <br> If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following tl generate IRP.* <br> Gate IRP as Sequence I Preset. <br> + Computer will pass interlock if: <br> 1. Read Interlock is reset. <br> 2. Reversal Memory is reset. <br> 3. First Block Memory is reset. <br> 4. IO-INT FF is reset. <br> 5. No rewind has been initiated within 3 ms . <br> * IRP is used to: <br> 1. Step PC. <br> 2. Set TO. <br> 3. Supply set pulse to Direction Memory. <br> 4. Set Reversal Memory if BIR was returned from Uniservo. <br> 5. Reset Interlock Release FF. <br> 6. Supply Sequence I Preset. <br> $\neq$ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.) | 629 <br> 606 <br> None <br> 621 |


| $\begin{gathered} 1 \overline{\mathrm{n}} \overline{\mathrm{~m}} \\ \mathrm{TO} \\ 2 \end{gathered}$ |  |  |
| :---: | :---: | :---: |
|  | Gate nS signal to üniservo ( $n$ ) to alert Read and Forward thyratrons. <br> Gate RP and FP signals to fire Read and Forward thyratrons in Uniservo ( $n$ ). Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay. <br> If Direction Memory agrees with first instruction digit, supply Read Tape Preset and gate an EP to control circuits. <br> Gate EP to set Read Forward and Start Read FF's after appropriate delay. <br> * Length of time before Read Forward FF is set is determined by condition of Reversal Memory. Length of time before Read Control FF is set is determined by condition of Reversal Memory and First Block Memory. | $\begin{aligned} & 629 \\ & 604 \\ & 609 \\ & 614 \end{aligned}$ |


| $2 \mathrm{~nm}$ $1$ | 60 mords from tape to ri, backward <br> Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo desired will pass interlock. <br> Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read operation. $+\neq$ <br> If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following tl gate a pulse to generate IRP. Gate IRP as Sequence I Preset. <br> + Computer will pass interlock if: <br> 1. Read Interlock is reset. <br> 2. Reversal Memory is reset. <br> 3. First Block Memory is reset. <br> 4. IO-INT FF is reset. <br> 5. No rewind has been initiated within 3 ms. <br> * IRP is used to: <br> 1. Step PC. <br> 2. Set T0. <br> 3. Supply reset pulse to Direction Memory. <br> 4. Set Reversal Memory if FIR was returned from Uniservo. <br> 5. Reset Interlock Release FF. <br> 6. Supply Sequence I Preset. <br> $\neq$ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.) | 629 <br> 606 <br> None <br> 621 |
| :---: | :---: | :---: |
| T0 |  |  |


| $\begin{aligned} & 2 \mathrm{~nm} \\ & 2 \end{aligned}$ | Gate nS signal to Uniservo (n) to alert Read and Backward thyratrons. <br> Gate RP and BP signals to fire Read and Backward thyratrons in Uniservo ( n ). + Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay. <br> If Direction Memory agrees with First Instruction Digit, supply Read Tape Preset and gate an EP to control circuits. <br> Gate EP to set Read Backward and Start Read FF's after appropriate delay.* <br> * Length of time before Read Backward FF is set is determined by condition of Reversal Memory. Length of time before Read Control FF is set is determined by condition of Reversal Memory and First Block Memory. | $\begin{aligned} & 629 \\ & \\ & 604 \\ & 609 \\ & 614 \end{aligned}$ |
| :---: | :---: | :---: |
| $3 \mathrm{~nm}$ <br> 1 | (rI) $\longrightarrow \mathrm{m}$ THRU $\mathrm{m}+59$; 60 words $\longrightarrow \mathrm{rI}$, forward <br> Operate rM address exceeded $\mathcal{E}$ preset checkers. Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo desired will pass interlock. <br> Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read operation. $+\neq$ <br> If FIR, BIR or FIR-BIR pass interlock test set Interlock Release FF. At following tl generate IRP. <br> Gate IRP as Sequence I Preset. <br> + Computer will pass interlock if: <br> 1. Read Interlock is reset. <br> 2. Reversal Memory is reset. <br> 3. $\mathrm{IO}-\mathrm{INT} \mathrm{FF}$ is reset. <br> 4. First Block Memory is reset. <br> 5. No rewind has been initiated within 3 ms . <br> * IRP is used to <br> 1. Step PC. <br> 2. Set TO. <br> 3. Supply set pulse to Direction Memory. <br> 4. Set Reversal Memory if BIR was returned from Uniservo. <br> 5. Reset Interlock Release FF. <br> 6. Supply Sequence I Preset. <br> $\neq$ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. <br> (If First Block Memory is set, Reversal Memory will also be set.) | 860 <br> 629 <br> 606 <br> None <br> 621 |



| $4 \mathrm{n} \text { m }$ <br> 1 | $(\mathrm{rI}) \longrightarrow \mathrm{m}$ THRU $\mathrm{m}+59$; 60 words $\longrightarrow \mathrm{rI}$, backward <br> Operate address exceeded $\mathcal{E}$ preset checkers. Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Üniservo desired will pass interlock. <br> Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read operation. $+\neq$ <br> If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following tl generate IRP. <br> Gate IRP as Sequence I Preset. <br> + Computer will pass interlock if: <br> 1. Read Interlock is reset. <br> 2. Reversal Memory is reset. <br> 3. First Block Memory is reset. <br> 4. IO-INT FF is reset. <br> 5. No rewind has been initiated within 3 ms . <br> * IRP is used to: <br> 1. Step PC. <br> 2. Set TO. <br> 3. Supply reset pulse to Direction Memory. <br> 4. Set Reversal Memory if FIR was returned from Uniservo. <br> 5. Reset Interlock Release FF. <br> 6. Supply Sequence I Preset. <br> $\neq$ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.) | $\begin{aligned} & 860 \\ & 621 \\ & 606 \\ & \\ & \text { None } \\ & 629 \end{aligned}$ |
| :---: | :---: | :---: |
| T0 |  |  |
| $\begin{aligned} & 4 \mathrm{~nm} \\ & 2 \end{aligned}$ | Set rM Read FF. <br> Set BCM to RM. <br> Inhibit set of $M_{1}$ cores, strobe rI sense <br> amplfiers, transfer $M_{2} \rightarrow M_{1}$ and $M_{2} \rightarrow r i$. <br> Step rI address counters for each word trans- <br> ferred until "59" signal occurs at which time <br> set MTO, step PC, and set TO. <br> Develop Serialize Pulse. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Step rM and rZW address counters. <br> Gate $n S$ signal to Uniservo ( $n$ ). <br> Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay. | 820 <br> 827 <br> 641 <br> 824 <br> 429 <br> 428 <br> 833 <br> 629 <br> 604 |



| InSTRUCTION | DESCRIPTION | FT |
| :---: | :---: | :---: |
| $\begin{aligned} & 5 \mathrm{~nm} \\ & \mathrm{~T} 0 \\ & 2 \end{aligned}$ | Sequence rM for RH timing. <br> Strobe rM sense amplifiers. <br> Transfer $\mathrm{Ml}_{1} \longrightarrow \mathrm{M}_{3}$ 。 <br> Transfer $\mathrm{M}_{3} \longrightarrow$ r0. <br> Step ro address counters for each word transferred until " 59 " signal occurs, at which time set MTO, step PC, and set TO. <br> Step rM, rZW address counters. <br> Develop Serialize Pulse <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Gate nS signal to Uniservo (n) and alert Write and Forward thyratrons. <br> Gate WP and FP signals to fire Write and Forward thyratrons in Uniservo ( $n$ ). Gate WP signal to set Write Interlock. Gate LE of FT604 to ending pulse delay. + <br> + If nS signal agrees with Tape Density Selector switch, gate WP to pick up Tape Density relay for 108 PPI. | $\begin{aligned} & \hline 820 \\ & 821 \\ & 829 \\ & \\ & 681 \\ & 833 \\ & 824 \\ & 429 \\ & 428 \\ & 629 \\ & \\ & 604 \end{aligned}$ |
| T0 |  |  |
| 3 | Supply Write Tape Preset and gate an EP to control circuits. <br> Gate EP to set Write Forward and Start Write FF's after appropriate delay.* <br> * Length of time before Write Forward FF is set is determined by condition of Reversal Memory. <br> Length of time before Write Control FF is set is determined by condition of Reversal Memory and First Block Memory. | $\begin{aligned} & 609 \\ & 615 \end{aligned}$ |




| INSTRUCTION | DESCRIPTION | FT |
| :---: | :---: | :---: |
|  | Set riin kead FF, set iin cores. <br> Strobe rM sense amplifiers. <br> Transfer $\mathrm{M}_{1} \rightarrow \mathrm{M}_{3}$. <br> Step $\mathrm{rM}, \mathrm{rZW}$ address counters. <br> Transfer $H_{3} \rightarrow$ ro. Step r0 <br> address counters for each word transferred <br> until "59" signal occurs at which time set <br> MTO, step PC, and set TO. <br> Develop Serialize Pulse. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set 54 pulses per inch thyratron to write at 54 PPI. <br> Gate nS signal to Uniservo (n) to alert Write and Forward thyratrons. <br> Gate WP and FP signals to fire Write and Forward thyratrons in Uniservo ( $n$ ). Gate WP signal to set Write Interlock. Gate LE of FT604 to ending pulse delay. | 820 <br> 821 <br> 829 <br> 833 <br> 681 <br> 824 <br> 429 <br> 428 <br> None <br> 629 <br> 604 |
| $\begin{aligned} & \text { T0 } \\ & 3 \end{aligned}$ |  |  |
|  | Gate an EP to control circuits. <br> Gate an EP to set Write Forward and Start Write FF's after appropriate delay. | $\begin{aligned} & 609 \\ & 615 \end{aligned}$ |



| 10 m 1 | Supervisory keyboard $\longrightarrow \mathrm{rM}$ <br> Operate rin address exceeded $\mathcal{E}$ preset checkers. Generate signal to pass Supervisory Control interlock provided that no Read, Supervisory Control Typerout, or Supervisory Control Type-in is in progress. Set Supervisory Control Input FF. Set Interlock Release FF provided that Reversal Memory, and First Block Memory is reset, and no rewind has been initiated within 3 ms . Gate following tl as IRP. <br> Gate IRP as Sequence I Preset. <br> * IRP is used to: <br> 1. Step PC. <br> 2. Set TO. <br> 3. Reset Interlock Release FF. <br> 4. Set Supervisory Control Input FF. <br> 5. Supply Sequence I Preset. | $\begin{aligned} & 860 \\ & 616 \\ & \\ & \text { None } \\ & 621 \end{aligned}$ |
| :---: | :---: | :---: |
| T0 |  |  |
| 2 | The Sequence I Preset clears and presets the input counters. The $K$ signals (result of setting Supervisory Control Input FF) control the Input Distributor Control circuits to facilitate a Supervisory Control input. Type in 6 digits, digit by digit, checking each digit for any odd-even error, and step TRI counters after each key is depressed. Transfer each digit from the $\mathrm{N}_{5}$ cores to $\mathrm{M}_{2}$. After the 6th digit is typed, transfer $M_{2} \rightarrow M_{1}$ and type in 6 more digits to $M_{2}$. After the 12 th digit is typed, set Stop FF and depress Word Release which will step PC and set $T O$. | No FT |
| T0 |  |  |
| 3 | Set rM Read FF. <br> Transfer $\mathbb{W} 2 \rightarrow M_{1}$, inhibit set of $M_{1}$ cores. <br> Develop Serialize Pulse. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set MTO. <br> Supply EP. | $\begin{aligned} & 820 \\ & 645 \\ & 824 \\ & 429 \\ & 428 \\ & 825 \\ & 206 \end{aligned}$ |





| $\begin{aligned} & 50 \\ & \text { T0 } \\ & 2 \end{aligned}$ |  |  |
| :---: | :---: | :---: |
|  | The Sequence 0 preset clears and presets the out－ put counters．The T signals（result of setting the Supervisory Control Output FF）control the Output Distributor control circuits to facilitate a Supervisory Control output． <br> Set rZW Read FF。 <br> Set rM Read FF，set $M_{1}$ cores． <br> Strobe rM sense amplifiers． <br> Develop Serialize Pulse。 <br> Operate HSB－OEC． <br> Operate HSB－AOC． <br> Set MTO． <br> Step PC，set TO． <br> Above steps are for readout of rM ．With FT 820，821，and 824 deleted，and FT 823，826， 861 and the read out FT of a particular register inserted，a register type out is accomplished．The sequence for type out from a register is： <br> Set rZW Read and Write FF＇s <br> Transfer（ rA ）$\longrightarrow$ HSB． <br> Operate HSB－OEC． <br> Operate HSB－AOC． <br> Develop Staticize Pulse <br> Set MTO． <br> Step PC，set TO． <br> Set rZW Read FF，set $M_{1}$ cores． <br> Inhibit set of rM Read／Write FF。 <br> + Up only if rA Output Selector button is depressed． <br> Other FT signals are： <br> 1． rF 192 <br> 2．rL 187 <br> 3． rA 100 <br> 4．rX 125 <br> 5．CC 210 <br> 6．CR 248 <br> ＊The EP gated by FT818 in the Control Circuits is suppressed by FT214． | 818 <br> 820 <br> 821 <br> 824 <br> 429 <br> 428 <br> 825 <br> 214 <br> 818＊ <br> 100＋ <br> 429 <br> 428 <br> 823 <br> 825 <br> 214 <br> 826 <br> 861 |
| T0 |  |  |


| $50$ <br> 3 | Operate HSB－OEC． <br> Operate HSB－AOC． <br> Set rZV Read／Write $\mathrm{FF}^{\text {＇s }} \mathrm{s}$ 。 <br> Strobe rZW sense amplifiers． <br> Set rZW Read FF，set $M_{l}$ cores． <br> Develop Serialize Pulse。 <br> Set MTO． <br> Transfer $\mathrm{M}_{1} \rightarrow \mathrm{M}_{3}$ ． <br> Inhibit set of $r M$ Write $F F$ ． <br> Transfer $\mathrm{M}_{3} \longrightarrow \mathrm{M}_{4}$ 。 <br> Step PC，set T0． | 429 <br> 428 <br> 818 <br> 819 <br> 820 <br> 824 <br> 825 <br> 829 <br> 861 <br> 685 <br> 214 |
| :---: | :---: | :---: |
| T0 |  |  |
| 4 | Supply EP． | 206 |
| 50 Breakpoint | （Register determined by $S C$ output button） <br> $\rightarrow$ SC printer <br> Stop computer if Type Out Breakpoint switch on SC is operated． <br> Operate rM address exceeded $\mathcal{E}$ preset checkers． Generate signal to pass write interlock at Write Interlock gate provided that Supervisory Control Interlock FF and Write Interlock FF is reset． Set Interlock Release FF provided that，First Block Memory，Reversal Memory，IO－INT are reset， and no rewind has been initiated within 3 ms ． Gate output of Interlock Release FF with a tl to generate IRP．＊ <br> Gate IRP to generate Sequence 0 Preset． <br> Gate IRP to set Supervisory Control Output FF， set Write Interlock． <br> Set Stop FF if Output Breakpoint switch is thrown． <br> ＊IRP is used to： <br> 1．Step PC <br> 2．Set TO <br> 3．Reset Interlock Release FF <br> 4．Set Supervisory Control Output FF <br> 5．Supply Sequence O Preset <br> + FT 629 is picked up for a 50 instruction，but is used only in the FTOC． | $\begin{aligned} & 860 \\ & 606 \\ & \\ & \text { None } \\ & \text { None } \\ & 669 \\ & \\ & 617 \\ & 218 \\ & 629+ \end{aligned}$ |


| $\begin{aligned} & \text { T0 } \\ & 50 \text { Breakpoint } \\ & 2 \end{aligned}$ |  |  |
| :---: | :---: | :---: |
|  | The Sequence 0 Preset clears and present the ouit put counters. The $T$ signals (result of setting the Supervisory Control Output FF) control the Output Distributor control circuits to facilitate a Supervisory Control output. <br> Set rZW Read FF. <br> Set rM Read FF, set Ml Cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set MTO. <br> Step PC, set TO. <br> Above steps are for read out of rM . With FT 820, 821, and 824 deleted and FT 823, 826. 861, and the read out FT of a particular register inserted, a register type out is accomplished. The sequence for read out from a register is: <br> Transfer ( rA ) $\longrightarrow$ HSB. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Develop Staticize Pulse. <br> Set MTO. <br> Step PC, set T0. <br> Set rZW Read FF. <br> Inhibit set of rM Read/Write FF's. <br> Set rZW Read FF. <br> + Up only if rA Output Selector button is depressed. <br> 0ther FT signals are: <br> 1. rF 192 <br> 2. rL 187 <br> 3. rA 100 <br> 4. rX 125 <br> 5. CC 210 <br> 6. CR 248 <br> *The EP gated by FT818 in the control circuits is suppressed by FT214. | 818 <br> 820 <br> 821 <br> 824 <br> 429 <br> 428 <br> 825 <br> 214 <br> $100+$ <br> 429 <br> 428 <br> 823 <br> 825 <br> 214 <br> 826 <br> 861 <br> 818 |
| T0 |  |  |


| 50 Breakpoint 3 | Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rZW Read/Write $\mathrm{FF}^{\prime}$ s. <br> Strobe rZW sense amplifiers. <br> Set rZW Read FF, Set $\mathrm{M}_{1}$ Cores. <br> Develop Serialize Pulse. <br> Set MTO. <br> Transfer $M_{1} \rightarrow M_{3}$. <br> Inhibit rM Write FF. <br> $\underset{\text { Transfer }}{ } \mathrm{M}_{3} \rightarrow \mathrm{M}_{4}$. <br> Step PC, set T0. | $\begin{aligned} & 429 \\ & 428 \\ & 818 \\ & 819 \\ & 820 \\ & 824 \\ & 825 \\ & 829 \\ & 861 \\ & 685 \\ & 214 \\ & \hline \end{aligned}$ |
| :---: | :---: | :---: |
| T0 |  |  |
| 4 | Supply EP. | 206 |
| 50 Skip | (Register determined by SC output button) <br> $\longrightarrow$ Printer. <br> Skip the type out if Skip Type Out switch on SC is operated. <br> Supply EP (if switch is operated) | 206 |
| Empty <br> 1 | $r M$, successive words $\longrightarrow$ SC printer <br> Operate rM address exceeded $\mathcal{E}$ preset checkers. Insert decimal zeros onto HSB. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Operate HSB $\longrightarrow C R$ gate, operate CR clear gate. Generate a signal to pass write interlock at Write Interlock gate provided the Supervisory Control Interlock FF and Write Interlock are reset. <br> Set Interlock Release FF provided the First Block Memory, Reversal Memory, IO-INT are reset and no rewind has been initiated within 3 ms . Gate output of Interlock Release FF with a tl to generate IRP. <br> Gate IRP to generate Sequence 0 freset. <br> Gate IRP to set Supervisory Control Output FF, to Write Interlock. <br> * IRP is used to: <br> 1. Step PC. <br> 2. Set TO. <br> 3. Reset Interlock Release FF. <br> 4. Set Supervisory Control Output FF. <br> 5. Supply Sequence 0 Preset. <br> +FT629 is picked up for an EMPTY instruction, but is used only in FTOC. | $\begin{aligned} & 860 \\ & 401 \\ & 429 \\ & 428 \\ & 201 \\ & \\ & 606 \\ & \\ & \text { None } \\ & \\ & \text { None } \\ & 669 \\ & \\ & 617 \\ & 629+ \end{aligned}$ |
| T0 |  |  |


| 2 | The Sequence 0 Preset clears and presets the output counters. The T signals (result of setting the Supervisory Control Output FF) control the Output Distributor control circuits to facilitate a Supervisory Control output. <br> Set rM Read FF , Set $\mathrm{M}_{1}$ cores. <br> Strobe rM sense amplifiers. <br> Develop Serialize Pulse. <br> Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set MTO. <br> Step PC, set T0. | $\begin{aligned} & 820 \\ & 821 \\ & 824 \\ & 429 \\ & 428 \\ & 825 \\ & 214 \end{aligned}$ |
| :---: | :---: | :---: |
| T0 |  |  |
| $\begin{aligned} & \text { Empty } \\ & 3 \end{aligned}$ | Operate HSB-OEC. <br> Operate HSB-AOC. <br> Set rZW Read/Write FF's. <br> Set rM Read FF, Set $M_{1}$ Cores. <br> Strobe rZW sense amplifiers <br> Develop Serialize Pulse. <br> Set MT0. <br> Transfer $\mathrm{M}_{1} \longrightarrow \mathrm{M}_{3}$. <br> Inhibit set of rM Read/Write FF's. <br> Read M3, transfer $\mathrm{M}_{3} \longrightarrow \mathrm{M}_{4}$. <br> Step PC, set TO. | 429 <br> 428 <br> 820 <br> 819 <br> 824 <br> 825 <br> 829 <br> 861 <br> 685 <br> 214 |
| $\begin{aligned} & \text { Empty } \\ & \text { T0 } \end{aligned}$ |  |  |
| 4 | Transfer $\mathrm{CC} \longrightarrow$ min input adder, ( 000000000001 ) sub input adder. Transfer sum from unbarred adder to CC after clearing CC. <br> operate adder for 12-place addition. <br> Operate adder OE and sum comparison checkers. <br> Supply reset pulse to Overflow FF. <br> Transfer $(C R) \rightarrow$ SR distributor line without delay. Supply EP. <br> Note: EMPTY instruction is started by depressing the Empty switch on SC. It is executed in Beta time with the typed information being read from $r M$ location, designated by SR the current CC reading. After the EP, two skip instructions will be executed because of the decimal zeros read into $C R$ during PG1, thus permitting (CC) to set up into SR with next memory to be emptied. | $\begin{aligned} & 212 \\ & 714 \\ & 435 \\ & 737 \\ & 204 \\ & 206 \end{aligned}$ |



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| 3 | Set rM Read FF , set $\mathrm{M}_{1}$ Cores. <br> Read $\mathrm{M}_{2}$. Transfer $\mathrm{M}_{2} \rightarrow \mathrm{M}_{1}$. <br> Develop Serialize Pulse. <br> Operate HSB-OEC. <br> 0perate HSB-AOC. <br> Transfer CC $\longrightarrow$ min input adder, (000000 000001) to sub input adder. Transfer sum from unbarred adder to CC after clearing CC. <br> Operate adder for 12-place addition. <br> Operate adder OE and sum comparison checkers. <br> Supply reset pulse to Overflow FF. <br> Transfer (CR) $\longrightarrow$ SR Distributor Line without delay. <br> Set MTO. <br> Supply EP. <br> Note: FILL instruction is started by moving the CR Interlock/Fill Mem switch on Supervisory Control to the Fill Mem position. It is executed in Beta time with the typed information going to the memory location designated by the SR, which contains the current CC reading. After the EP two skip instructions will be executed because of the decimal zeros read into CR during PC-1, thus permitting (CC) to set up in SR the next memory address to be filled. | $\begin{aligned} & 820 \\ & 645 \\ & 844 \\ & 429 \\ & 428 \\ & \\ & 212 \\ & 714 \\ & 435 \\ & 737 \\ & \\ & 204 \\ & 825 \\ & 206 \end{aligned}$ |
| :---: | :---: | :---: |
| Clear CC | CU ( 000000000000$) \longrightarrow \mathrm{CC}$ <br> Connect CU ( 000000000000 ) to HSB. <br> Operate HSB-OEC. <br> 0 perate HSB-AOC. <br> Connect HSB to CC, clear CC. <br> Supply EP. <br> Note: By depressing the clear $C$ switch on Supervisory Control, CY is automatically jammed to Beta, and the addition of one to (CC) is inhibited. | $\begin{aligned} & 401 \\ & 429 \\ & 428 \\ & 208 \\ & 206 \end{aligned}$ |


| $\begin{aligned} & \text { SCI-CR } \\ & 1 \end{aligned}$ | One word S C keyboard $\longrightarrow \mathrm{CR}$ <br> Generate signal to pass Supervisory Control interlock provided that no read, Supervisory Control type-out, or Supervisory Control typein is in progress. <br> Set Interlock Release FF provided that Reversal Memory, First Block Memory, and Rewind Frequency control is reset. Gate tlafter setting Interlock Release FF as IRP. <br> Gate IRP as Sequence I Preset. <br> Gate IRP to set Supervisory Control FF. <br> Supply reset pulse to Overflow FF. <br> * IRP is used to: <br> 1. Step PC. <br> 2. Set T0. <br> 3. Reset Interlock Release FF. <br> 4. Set Supervisory Control FF. <br> 5. Supply Sequence I Preset. | 616 <br> None <br> 621 <br> 616 <br> 737 |
| :---: | :---: | :---: |
| T0 |  |  |
| 2 | The Sequence I preset clears and presets the input counters. The $K$ signals (result of setting Supervisory Control Input FF) control the Input Distributor control circuits to facilitate a Supervisory Control input. <br> Type in 6 digits, digit by digit, check each digit for an odd-even error, and step TRI counters after each key is depressed. Transfer each digit from the $\mathrm{N}_{5}$ cores to $\mathrm{M}_{2}$. After the 6 th digit is typed, transfer $M_{2} \rightarrow M_{1}$ and type in 6 more digits to $M_{2}$. After the 12 th digit is typed, set Stop FF, depress Word Release which will step PC and set TO. | No FT |
| T0 |  |  |
| 3 | Inhibit set of rM Read/Write FF's. <br> Enable set of rZW Read FF. <br> Develop Serialize Pulse. <br> Set rZW Read FF, set $M_{1}$ Cores <br> Read $M_{2}$, transfer $M_{2} \rightarrow M_{1}$. <br> Set MTO. <br> Operate $\operatorname{HSB}-0 E C$ <br> Operate HSB-AOC <br> Step PC, set TO, and inhibit EP supplied by FT818. | 861 <br> 818 <br> 824 <br> 820 <br> 645 <br> 825 <br> 428 <br> 214 |


| INSTRUCTION | DESCRIPTION | FT |
| :---: | :---: | :---: |
| $\begin{aligned} & \text { SCI-CR } \\ & 4 \end{aligned}$ | Preset BCM to RM. <br> Inhibit rM Read/Write FF. <br> Enable set of rZW Read/Write FF's. <br> Set rZW Read FF. <br> Strobe rZW sense amplifiers. <br> Develop Serialize Pulse. <br> Operate HSB-OEC. <br> operate HSB-AOC. <br> Connect HSB to CR, clear CR. <br> Read $\mathrm{LH}(\mathrm{CR}) \longrightarrow$ SR. <br> Set MTO. <br> Supply EP <br> NOTE: CR TYPE IN switch will jam CY to Beta, and set up SR for SCI-CR. | $\begin{aligned} & 827 \\ & 861 \\ & 818 \\ & 820 \\ & 819 \\ & 824 \\ & 429 \\ & 428 \\ & 201 \\ & 204 \\ & 825 \\ & 206 \end{aligned}$ |
| Memory <br> Clear | Connect CU ( 000000000000 ) to HSB. <br> Operate HSB-0EC. <br> 0 perate HSB-AOC. <br> Develop Staticize Pulse. <br> Set rM Read FF, set $M_{1}$ Cores. <br> 0perate rM address exceeded and preset checkers. <br> Set MTO. | 401 429 428 823 826 860 825 |

4. CONDENSED INSTROCTION REFERENCE.

This section is similar to Section 3 in that it lists the instructions, in order and by PC steps. However, it lists the FT signals associated with each PC step by number only, and not with description. This offers a rapid reviewal of FT signals present during maintenance routines.

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| EF | 2 | $\begin{aligned} & 193,214,429,820,821,824,101 \\ & 825,827,831,832,860,428,105 \\ & 100,206,429,823,825,826 \\ & 860,428 \end{aligned}$ |
| :---: | :---: | :---: |
| F |  | $\begin{aligned} & 190,206,429,820,821,824 \\ & 825,827,860,428 \end{aligned}$ |
| G |  | $\begin{aligned} & 192,206,429,823,825,826 \\ & 860,428 \end{aligned}$ |
| H |  | $\begin{aligned} & 100,206,429,823,825,826, \\ & 860,428 \end{aligned}$ |
| I |  | $\begin{aligned} & 187,206,429,823,825,826, \\ & 860,428 \end{aligned}$ |
| J |  | $\begin{aligned} & 125,206 ; 429,823,825,826, \\ & 860,428 \end{aligned}$ |
| K |  | $\begin{aligned} & 100,101,108,185,206, \\ & 429,428 \end{aligned}$ |
| L |  | $\begin{array}{llll} 120, & 126,185, & 206, & 429, \\ 821, & 824, & 825, & 827, \\ 860, & 428 \end{array}$ |
| LF |  | $\begin{aligned} & 120,126,185,193,206,429, \\ & 820,821,824,825,827,428,860 \end{aligned}$ |
| MP | 1 | $\begin{aligned} & 101,108,110,113,120,126, \\ & 139,214,429,435,820, \\ & 824,825,827,860, \\ & 428 \end{aligned}$ |
| MNP | 2 | 110, 113, 214, 435, 714 |
| MNP | 3 | 110, 113, 151, 214, 435, 714 |
| MN | 4 | $\begin{array}{llll} 100, & 101, & 108, & 112, \\ 123, & 159, & 190, & 1214, \\ 435, & 428, & 429 \end{array}$ |
| NMP | 5-15 | $\begin{aligned} & 109,147,159,188,246, \\ & 435,714 \end{aligned}$ |
| MNP | 14 | 244 |
| MNP | 15 | 149, 161, 215, 228 |


| MF-PF | 1 | $\begin{array}{llllll} 101, & 108, & 110, & 113, & 120, & 126, \\ 139, & 193, & 214, & 429, & 435, & 820, \\ 821, & 824, & 825, & 827, & 860, & 428 \end{array}$ |  |
| :---: | :---: | :---: | :---: |
| *N | 1 | 101, 108, 110, 113, 120, 139 <br> 153, 214, 429, 435, 820, 821, <br> 824, 825, 827, 860, 428  | * ( $\mathrm{N}, \mathrm{NFP}$ and PF have P C steps and same FT signals |
| *Nf | 1 | $\begin{array}{llllll} 101, & 108, & 110, & 113, & 120, & 139, \\ 153, & 193, & 214, & 429, & 435, & 820, \\ 821, & 824, & 825, & 827, & 860, & 428 \end{array}$ | cept as noted) |
| *P | 4 | $\begin{aligned} & 100,101,108,112,120,123, \\ & 159,190,214,226,429,428 \end{aligned}$ | **If 2nd Inst. digit is zero treat |
| Q | 2 | $\begin{aligned} & 152,156,187,214,236,429 \\ & 428 \\ & 159,200,206,209,429,428 \end{aligned}$ | skip if compatibility switch is set to Univac II. |
| R |  | $\begin{aligned} & 206,245,429,823,825,826 \\ & 860,428 \end{aligned}$ |  |
| S | 2 | $\begin{aligned} & 120,153,214,429,820,821, \\ & 824,825,827,860,428 \\ & 109,125,160,206,435 \end{aligned}$ |  |
| SF | 1 | $\begin{aligned} & 120,153,193,214,429,820 \\ & 821,824,825,827,860,428 \end{aligned}$ |  |
| SH | 1 2 3 | $\begin{aligned} & \text { Same as S PC l } \\ & 109,125,160,214,435 \\ & 100,206,429,823,825,826 \\ & 860,428 \end{aligned}$ |  |
| T | 2 | $\begin{aligned} & 152,172,187,214,236,429, \\ & 428 \\ & 159,200,206,209,429,428 \end{aligned}$ |  |
| U |  | 200, 206, 208, 429, 428 |  |
| $\checkmark$ |  | $\begin{aligned} & 429,817,818,820,821,824 \text {, } \\ & 827,833,860,428,206 * * \end{aligned}$ |  |

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| W | $\begin{aligned} & 429,817,818,819,820,824 ; \\ & 827,833,860,428,206 \text {; } \end{aligned}$ |
| :---: | :---: |
| X | 109, 125, 160, 206, 400, 435 |
| Y | $\begin{aligned} & 429,816,818,820,821,824, \\ & 827,833,860,428,206^{*} \end{aligned}$ |
| Z | 428, 429, 816, 818, 819, 820 $824,827,833,860,206$ |
| on all | 101, 106, 213, 817, 818, 833 |
| -n all | 107, 170, 213, 817, 818, 833 |
| ; n all | $\begin{aligned} & 101,103,171,213,817,818 \\ & 833 \end{aligned}$ |
| 0 n all | $\begin{aligned} & \text { 104, } 170,171,213,817,818 \text {, } \\ & \text { 833. } \end{aligned}$ |


| 00 |  | 206 |
| :---: | :---: | :---: |
| . 0 |  | 206, 217 |
| 90 |  | 206, 218 |
| ln | 1 2 | $\begin{aligned} & 606,621,629 \\ & 609,604,614,629 \end{aligned}$ |
| 2 n | 1 2 | $\begin{aligned} & 606,621,629 \\ & 609,604,614,629 \end{aligned}$ |
| 3 n | 1 2 3 | $\begin{aligned} & 606,621,629,860, \\ & 429,604,629,641,820,824, \\ & 827,833,428 \\ & 609,614 \end{aligned}$ |
| 4 n | 1 2 3 | $\begin{aligned} & 606,621,629,860 \\ & 429,604,629,641,820,824 \\ & 827,833,428 \\ & 609,614 \end{aligned}$ |
| $5 n$ | 1 | 606, 629, 669, 860 |

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| 5n | $2$ <br> 3 | $\begin{aligned} & 429,604,629,681,820,821, \\ & 824,829,833,428 \\ & 609,615 \end{aligned}$ |
| :---: | :---: | :---: |
| 6n | $\begin{aligned} & 1 \\ & 2 \end{aligned}$ | $\begin{aligned} & 606,608,629 \\ & 619,629 \end{aligned}$ |
| 7n | 1 <br> 2 <br> 3 | $\begin{aligned} & 606,629,669,860 \\ & 429,604,629,681,820,821, \\ & 824,829,833,428 \\ & 609,615 \end{aligned}$ |
| 8 n | $1$ $2$ | $\begin{aligned} & 606,607,608,629 \\ & 607,619,629 \end{aligned}$ |
| 10 m | 1 <br> 2 <br> 3 | $616,621,860$ $206,428,429,645,820,824,825$ |
| 10, CR | 1 <br> 2 <br> 3 <br> 4 | $\begin{aligned} & \text { 616, 621, 737, } \\ & 645,818,820,825,861,214,428,429,824 \\ & 201,203,428,429,818,819, \\ & 820,824,825,827,861,206 \end{aligned}$ |
| 30 |  | Same as 3 n except 0 Selector signal prevents tape operation. |
| 40 |  | Same as 4 n except 0 Selector signal prevents tape operation. |
| 50 | $1$ $2$ | $606,617,669,629 *, 860$ *Note 629 is <br> picked up but <br> used only in  <br> $214,429,685,825,818,428$ FTOC.  <br> M $820,821,824$  <br> A $100,823,826,861$  <br> X $125,823,826,861$  |

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5. DESCRIPTION OF FUNCTION TABLE SIGNALS.

The Function Table signals described on the following pages generate the minor sequences which compiete the instruction routines. The FT signals are initiated by either the decoding of a programed instruction or by some element of the automatic interval programing of the computer. Figure 1 presents, logically, the signals which control the alerting of the FT signals.

The FT signals are listed in the numerical order of their assigned numbers. Duplicated signals are indicated with the barred notation, e.g., 100 and $\overline{100}$. In the instances where an FT signal originates from several drivers, symbols are used following the FT signal number to differentiate between the various outputs to facilitate identification in the outlying circuits, e.g. FTl60A, FTl60B, FTl60C, etc. Most FT signals are negative-going, those that are not usually carry a plus sign following the FT number; e.g. FT645+.

Pertinent information concerning the FT signals is presented in the columns following the FT number. Column l locates the chassis in which the FT signal is generated and gives the output terminal on which the FT signal appears. Column 2 lists the test terminal, for maintenance purposes, on which the full signal appears. Column 3 names the vacuum tube on the chassis from which the FT signal appears. Column 4 lists the signal-no signal condition of the FT signal; i.e., the voltage levels that appear on the corresponding test terminal of the FT. Column 5 provides a logical description of the function performed by each FT signal.

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Figure 1. Logical Diagram, Function Table Signals


Figure 1. Logical Diagram, Function Table Signals (cont'd.)

| Function <br> Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\checkmark 100$ | B5T28 | A2 | V1 | 60/90 | Connect rA to HSB. |
| $\bigcirc$ | B5T29 | A4 | V2 | 60/90 |  |
| $\cdot 101$ | B3T65 | C2 | v5 | 60/90 | Operate rA clear gate. |
| . 101 | B3T33 | Cl | V4 | 60/90 |  |
| 1103 | B10T54 | Al2 | V1 | 60/90 | Operate left shift path of ra (including sign).** |
| $\overline{103}$ | B10T29 | Al3 | V2 | 60/90 |  |
| $\checkmark 104$ | B10T85 | G6 | V13 | 60/90 | Operate left shift path of rA (excluding sign). |
| $\overline{104}$ | B10T87 | G7 | V14 | 60/90 |  |
| ${ }^{\prime} 105$ | B3T43 | E4 | V8 | 60/90 | Connect HSB to rA. |
| $\overline{105}$ | B3T38 | C7 | v7 | 60/90 |  |
| 106 A | Bl2T56 | A4 | V2 | 60/90 | Operate right shift path of rA. |
| $\overline{106 A}$ | B12T54 | A2 | V1 | 60/90 |  |
| 才06B | Bl2T62 | A7 | V4 | 60/90 | Insert decimal zero into sign position in rA. |
| $\overline{106 B}$ | B12T60 | A6 | V3 | 60/90 |  |
| i106C | Bl2T39 | C4 | V6 | 60/90 | Transfer sign from comparator to rA and rX. |
| $-\overline{106 C}$ | B12T35 | C3 | V5 | 60/90 |  |
| $\checkmark 107$ | B10T46 | G1 | V11 | 60/90 | Operate right shift path of $r A_{8}$ and insert a decimal zero into the MSD position.* |
| 107 | B10T81 | G3 | V12 | 60/90 |  |
| $\checkmark 108$ | ClV66 | C6 | V6 | 60/90 | Connect CU (000000 000000) to rA. |
| $\overline{108}$ | Clv33 | C3 | V5 | 60/90 |  |
| $\therefore 109 \mathrm{~A}$ | C4V60 | A6 | V3 | 60/90 | Connect HSB to adder sub input. |
| - $\overline{109 \mathrm{~A}}$ | C4V62 | Cl | V4 | 60/90 |  |

\$\# rA shifts one digit left for each minor cycle of Time-On.

* rA shifts one digit right for each minor cycle of Time-On.

| $\begin{aligned} & \text { Function } \\ & \text { Table } \\ & \hline \end{aligned}$ | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -109D | C4V66 | C4 | V5 | 60/90 | Connect ra to adder min input. Clear rA and transfer sum from adder to ra. |
| $\checkmark 109 \mathrm{D}$ | C4V68 | C6 | V6 | 60/90 |  |
| - 110 | $\begin{aligned} & \text { C3B56 } \\ & \text { C3v5 } 6 \end{aligned}$ | A2 | V1 | 60/90 | Connect rL to adder sub input. Transfer (rL) to adder, replacing sign digit with a decimal zero. |
| $\overline{110}$ | C3V29 | A4 | V2 | 60/90 |  |
| V11 | B5T85 | G5 | V13 | 60/90 | Connect CU (round-off 000000000005 ) to adder min input. |
| $\frac{1}{\sqrt{111}}$ | B5T87 | G7 | V14 | 60/90 |  |
| $\checkmark 112 \mathrm{~A}$ | Bl1770 | C7 | v7 | 60/90 | Connect CU (050000 000000) to the adder sub input. |
| $\overline{\text { İ12A }}$ | B11773 | E3 | v8 | 60/90 |  |
| 112 B | B11T75 | E6 | v9 | 60/90 | Clear MQC to binary zero and set up nines complement of digit in $M Q C$. |
| $\overline{112 \mathrm{~B}}$ | BllT77 | E8 | V10 | 60/90 |  |
| - i12C | Biitil | G2 | Vii | 60/90 | Transfer the LSD of (rX) to MoC. |
| - $\overline{112 \mathrm{C}}$ | B11T83 | G4 | V12 | 60/90 |  |
| $\bigcirc 113$ | В3T87 | G7 | V14 | 60/90 | Connect râ to adder min input. Clear rA and read sum from adder to ra (transfer ends at tl2 to TO). |
| $/ \overline{113}$ | B3T83 | G6 | V13 | 60/90 |  |
| $\checkmark 120$ | B3T31 | A7 | V3 | 60/90 | Operate rX clear gate. |
| $\checkmark \overline{120}$ | B3T58 | A6 | V2 | 60/90 |  |
| 123 | Clv62 | A8 | V4 | 60/90 | Operate right shift path in rX. |
| $\checkmark \overline{123}$ | Clv31 | A7 | V3 | 60/90 |  |
| -125 | B5T67 | C6 | V6 | 60/90 | Connect rX to HSB. |
| $\overline{125}$ | B5T72 | C8 | V7 | 60/90 |  |
| - 126 | Clv73 | E3 | v8 | 60/90 | Connect HSB to rX. |
| $\overline{126}$ | C1V70 | C6 | V7 | 60/90 |  |
| $\checkmark 138 \mathrm{~A}$ | B8T60 | A7 | v3 | 60/90 | Clear MQC to decimal zero. |
| $\cdots$ | B8T64 | A8 | V4 | 60/90 |  |

## Function

| Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\checkmark 138 \mathrm{~B}$ | B8T66 | C3 | v5 | 60\%90 | Preset $\mathrm{BC}-120$ in MQC to the noncomplement state thereby alerting the non-complementing gates between MQC and MOC-FT. |
| $\sqrt{138 \mathrm{~B}}$ | B8T68 | C6 | V6 | 60/90 |  |
| -139 | B8T71 | E2 | v7 | 60/90 | Preset BC - 120 to the complement state, thereby alerting the complement gates connecting the MOC and MOC-FT. |
| $\sqrt{139}$ | B8T73 | E3 | v8 | 60/90 |  |
| 145A | C5V62 | Cl | V4 | 60/90 | Gate non-complement output of BC-120 to operate Improper Division Detector in MOC. $\#$ |



| $\sqrt{145 B}$ | C5V66 | C3 | V5 | 60/90 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 145C | C5V73 | E3 | v8 | 60/90 | Step MQC at t 2 following each subtraction until the Through-Zero signal is developed, then produce the |
| $\sqrt{145 \mathrm{C}}$ | C5B71 | E2 | v7 | 60/90 | OR CYCLE. |
| V147A | B6T83 | G3 | V12 | 60/90 | Sample (MOC-FT). If digit is < 3, |

                                    set the \(\geq 3 F F\), this transfers (rL)
                                    to HSB and supplies one stepping pulse
                                    to \(M Q C\). If digit is \(\geq 3\), set the
                                    \(\geq 3 F F\), this transfers (rF) to HSB
                                    and supplies three stepping pulses to MQC.
    | $\sqrt{147 \mathrm{~A}}$ | B6T87 | G7 | V14 | 60/90 | MQC. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\lambda_{147 B}$ | B6T81 | G2 | V11 | 60/90 | If digit in MOC-FT $=0$, set IER and IER-OR FF's at following t2. |
|  |  |  |  |  |  |
| $\sqrt{147 B}$ | B6'95 | G6 | V13 | 60/90 |  |
| $\checkmark 149$ | B12T73 | E3 | v8 | 60/90 | Inhibit generating a second IER CYCLE in the case that a decimal zero is set up in the MQC. |
|  |  |  |  |  |  |
| $\overline{149}$ | B12T71 | C7 | v7 | 60/90 |  |
| 1-151C | $\begin{aligned} & c 3 v 60 \\ & 69 B 6 \theta \end{aligned}$ | A6 | V3 | 60/90 | Disconnect rA input to comparator and connect rL.* |
| $1 \overline{151}$ c | C3V33 | A8 | V4 | 60/90 |  |

\# If rLS $r A$, Improper Divison occurs at t2 of the eleventh minor cycle
of PC-3.

* Sign comparison is performed on (rA) and (rL).

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| Function <br> Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 152A | C3v68 | C5 | V6 | 60/90 | Disconnect $r X$ input to comparator and connect HSB.* |
| - $\overline{52 \mathrm{~A}}$ | C3V66 | C3 | v5 | 60/90 |  |
| -152B ${ }^{-1}$ | C3V42 | E3 | v8 | 60/90 | Connect HSB to comparator. |
| $\overline{152 B}^{\text {- }}$ | C3V39 | C8 | V7 | 60/90 |  |
| 亿153A | B8T75 | E6 | V9 | 60/90 | Connect HSB to rX via sign reversal gates. |
| - $\overline{153 A}$ | B8T44 | E7 | V10 | 60/90 |  |
| $\checkmark 153 \mathrm{~B}$ | B8T81 | G2 | V11 | 60/90 | Operate sign reversal gates in rX. |
| $\overline{153 \mathrm{~B}}$ | B8T48 | G4 | V12 | 60/90 |  |
| $-156 \mathrm{~A}$ | C3V87 | -- | V14 | 60/90 | Set up comparator to perform equality comparison.\#\# |
| $\overline{156 A}$ | C3V85 | -- | V13 | 60/90 |  |
| - 156 B | C3V48 | -- | V12 | 60/90 |  |
| $\overline{156 B}$ | C3V79 | -- | V11 | 60/90 |  |
| -156C | C3V77 | E7 | V10 | 60/90 |  |
| - 156 C | C3V75 | E5 | v9 | 60/90 |  |
| -159 | B6T46 | E5 | v9 | 60/90 | Retain results of comparison in comparator. |
| . $\overline{159}$ | B6T48 | E6 | V10 | 60/90 |  |

* Sign comparison is performed on (rA) and (rL).
\# The sign reversal gates complement the LSB and Check Pulse of the sign digit during transfer to rX.
\#\# If rA $=$ rL develop CT signal.

| Function <br> Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -160A | C4V70 | C7 | V7 | 60/90 | Operate adder for eleven-place addition. |
| 160A | C4V71 | E3 | v8 | 60/90 |  |
| , 160B | C4V75 | E5 | V9 | 60/90 |  |
| $\sqrt{1608}$ | C4V77 | E8 | V10 | 60/90 |  |
| - 160C | C4V79 | G2 | V11 | 60/90 |  |
| $\checkmark \overline{160 C}$ | C4V81 | G3 | V12 | 60/90 |  |
| 160D | C4v85 | G6 | V13 | 60/90 |  |
| $1 \overline{1600}$ | C4V87 | G7 | V14 | 60/90 |  |
| $\checkmark 161 \mathrm{~A}$ | B12T44 | E8 | V10 | 60/90 | Transfer sign from comparator to rA and rX . |
| $\sqrt{161 A}$ | B12T75 | E5 | V9 | 60/90 |  |
| $1261+$ | B12T81 | G3 | $\mathrm{V} 12,1090 / 60$ |  | Inhibit the insertion of a decimal zero into rA. |
| $\sqrt{161+}$ | B12T79 | G2 | V11, ${ }^{\circ}$ | 90/60 |  |
|  | B10T75 | E5 | V9 |  | Operate rA clear gate, except for sign position. |
| $\sqrt{170}$ | B10T77 | E7 | V10 | 60/90 |  |
| ${ }^{\prime} 171$ | B10T60 | A17 | v3 | 60/90 | Insert decimal zero in LSD position of $r$. |
| $\sqrt{171}$ | B10T62 | Cll | V4 | 60/90 |  |
| $-172 \mathrm{~A}$ | B9731 | A6 | v3 | 60/90 | Set up comparator to perform algebraic comparison. |
| $-\overline{172 A}$ | B9729 | A5 | V2 | 60/90 |  |
| - 172B | B9T66 | C3 | V5 | 60/90 |  |
| $\sqrt{172 \mathrm{~B}}$ | B9T64 | Cl | V4 | 60/90 |  |

** If decimal carry occurs from eleventh digit position, set Overflow FF. If Second Instruction Digit is a minus sign, overflow sets Stop FF.

* If $r A>r L_{\text {, }}$ develop CT signal.

| Function <br> Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -185A | ClV77 | E5 | V9 | 60/90 | Connect HSB to rL. Operate rL clear gate. |
| $\overline{185 A}$ | Clv83 | G3 | V12 | 60/90 |  |
| -187 | B9T75 | E5 | V9 | 60/90 | Connect rL to HSB. |
| $\overline{187}$ | B9T40 | E3 | v8 | 60/90 |  |
| $\checkmark 188 \mathrm{~A}$ | C5V77 | E7 | V10 | 60/90 | With<3 signal. Transfer (rL) to HSB. |
| $\sqrt{188 \mathrm{~A}}$ | C5V75 | E5 | V9 | 60/90 |  |
| ,188B | C5V83 | G4 | V12 | 60/90 | Replace sign digit with a decimal zero. Set T0 and STOP FF's after each Time-on minor cycle if IOS is in "One Addition". |
| $\sqrt{188 \mathrm{~B}}$ | C5V81 | G1 | V11 | 60/90 |  |
| $\checkmark 188 \mathrm{C}$ | C5v87 | G7 | V14 | 60/90 | With $\geq 3$ signal. Connect rF to HSB. Step PC upon completion of each IER-OR CYCLE. |
| $\overline{188 \mathrm{C}}$ | C5v85 | G6 | V13 | 60/90 |  |
| /190 | B3T78 | E2 | V9 | 60/90 | Connect HSB to rF , and operate rF clear gate. |
| $\checkmark \overline{190}$ | B3T50 | E7 | V10 | 60/90 |  |
| $\checkmark 192$ | B5T41 | E2 | V8 | 60/90 | Connect rF to HSB. |
| $\overline{192}$ | B5T74 | E5 | V9 | 60/90 |  |
| 493 | B3T29 | (A3) 44 | V1 | 60/90 | Operate extract circuit in rF.* |
| $\overline{193}$ | B3T28 | (E5) ${ }^{5}$ | V6 | 60/90 |  |
| -200 | Bl1T66 | C3 | V5 | 60/90 | Connect CR and $\mathrm{CU}(000000$ 00) to HSB. ${ }^{* *}$ |
| $\sqrt{200}$ | B11T68 | C6 | v6 | 60/90 |  |

* Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from $r M$ is replaced with a decimal zero.
** The four LSD's of (CR) are merged with eight decimal zeros from CU to make a complete word which is transferred to HSB.

ANALYSIS OF
INSTRUCTIONS

| Function <br> Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -201 | B2T26 | A2 | V1 | 60/90 | Operate HSB CR gate, operate CR clear gate. |
| $\checkmark 203$ | C2V46 | G1 | V11 | 60/90 | Connect CR1 to CR2. (LH Instruction sets up at t 7 of Gamma T0) |
| 203K | C2V28 | A3 | $\mathrm{V1}$ | 60/90 | To FTOC. |
| 204 | C2V83 | G4 | V12 | 60/90 | Connect CR1 to SR Distributor Line. |
| -206 | B2T64 | C1 | V4 | 60/90 | Supply EP. |
| $\sqrt{206}$ | B2T65 | C2 | v5 | 60/90 |  |
| -208A | C1V53 | G7 | V14 | 60/90 | Connect HSB to CC. |
| - 208B | C1V51 | G5 | V13 | 60/90 | Operate CC clear gate. |
| , 209A | B11T85 | G6 | V13 | 60/90 | If Conditional Transfer FF is set, connect HSB to CC. $\qquad$ $\qquad$ |
| , 209B | B11T87 | G8 | V14 | 60/90 | If CT FF is set, operate CC clear gate. |


| 210 | C2V44 | E8 | V10 | 60/90 | Connect CC to HSB. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -210 | C2V75 | E5 | v9 | 60/90 |  |
| - 212A | C2V62 | A8 | V4 | 60/90 | Connect CC to adder min input. |
| $\sqrt{212 \mathrm{~A}}$ | C2V60 | A5 | v3 | 60/90 |  |
| 212B | C2V71 | E3 | v8 | 60/90 | Clear CC. |
| . 212C | C2V70 | C7 | v7 | 60/90 | Transfer sum from unbarred adder to CC. $\qquad$ $\qquad$ $\qquad$ $\qquad$ |
| $\times 212 \mathrm{D}$ | C2v37 | C5 | V6 | 60/90 | Connect CU (000000 000001) to adder sub input. |
| $\overline{2120}$ | C2V66 | C3 | V5 | 60/90 |  |
| - 213 CK | B8T87 | G17 | V14, ${ }^{1}$ | -20/+5 | Operate shift selector checker. |
| '213 | B10T70 | C7 | V7 | 60/90 | Step PC once each minor cycle.* |
| $\longdiv { 2 1 3 }$ | B10T73 | E3 | v8 | 60/90 |  |

* If PC is advanced in excess of thirteen, an Overshift signal is developed which stops machine operation by setting FT Intermediate Checker FF and TO.

ANALYSIS OF INSTRUCTIONS

UNIVAC II

| Function <br> Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 214 | B2T51 | G4 | V12 | 60/90 | Step PC, set TO. |
| $\overline{214}$ | B2T52 | G5 | V13 | 60/90 |  |
| $\checkmark 215$ | B7T68 | C6 | V7 | 60/90 | Supply EP. |
| $\sqrt{215}$ | B7T37 | C5 | V6 | 60/90 |  |
| W217 | B7T87 | G7 | V14 | $60 / 90$ | Set Stop FF if Comma Breakpoint switch is depressed. |
| $\sqrt{217}$ | B7T85 | G6 | V13 | 60/90 |  |
| - 218 | $19$ | Gl | V11 | 60/90 | Set Stop FF. |
| - $\overline{218}$ | B9T44 | E7 | V10 | 60/90 |  |
| -226 | B10T64 | C3 | v5 | 60/90 | Set Repeat FF. |
| $\overline{226}$ | B10T37 | $\begin{aligned} & C 5 \\ & E 5 \end{aligned}$ | V6 | 60/90 |  |
| $\sqrt{228}$ | B12T87 | G7 | V14 | 60/90 | Reset Repeat FF at end of IER OR CYCLE. |
| $\sqrt{228}$ | B12T85 | G6 | V13 | 60/90 |  |
| -236 | B9785 | G5 | V13 | 60/90 | Set Stop FF with CT Selector. Switch signals during $Q$ or $T$ instructions. |
| -236 | B9T48 | G3 | V12 | 60/90 |  |
| $/ 244$ | B7T48 | G3 | V12 | 60/90 | Set T0 at end of IER OR CYCLE. |
| $\sqrt{244}$ | B7T79 | G1 | V11 | 60/90 |  |
| 1245 | B5T77 | (E16) 1 | V10 | 60/90 | Transfer 4 LSD's of (CC) and |
| $\sqrt{245}$ | B5T79 | G1IG1 | V11 | 60/90 | O00000 00 from CU to HSB. |
| - 246 | C4V56 | A2 | V1 | 60/90 | If rA or rX comp error occurs, set TO at following tl. |
| $\overline{246}$ | C4V58 | A4 | V2 | 60/90 |  |
| - 248 | B7T66 | C3 | V5 | 60/90 | Connect CR to HSB. |
| - $\overline{248}$ | B7T62 | A8 | V4 | 60/90 |  |
| $\checkmark 401$ | B2T49 | E8 | V10 | 60/90 | Connect CU (000000 000000) to HSB. |
| - $\overline{401}$ | B2T50 | G2 | V11 | 60/90 |  |

ANALYSIS OF
INSTRUCTIONS

UNIVAC II

Function

| Table | Chassis | TI | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| , 428 | Bl1T58 | Al | V1 | 60/90 | Operate HSB-AOC. |
| $\overline{428}$ | B11T57 | A3 | V2 | 60/90 |  |
| $\checkmark 429$ | B11T62 | A7 | V3 | 60/90 | Operate HSB-OEC. |
| $\sqrt{429}$ | Bl1T64 | Cl | V4 | 60/90 |  |
| $\sqrt{435 A}$ | B3T48 | G4 | V12 | 60/90 | Operate adder 0 E and sum comparison checkers. |
| -435B | B3T46 | G2 | V11 | 60/90 |  |
| 604A | B4T42 | E4 | V9 | 60/90 | Gate LE of FT604 to ending pulse delay. |
| $\sqrt{604 B}$ | B4T54 | Al | V1 | 60/90 |  |
| $\checkmark 606$ | B4T31 | A6 | V3 | 60/90 | Gate "O Select" signal to determine if computer will pass interlock to start transfer operation.* |


| 607 | B4T50 | G6 | V13 | 60/90 | Gate IRG to pick Interlock relay in Uniservo ( n ). |
| :---: | :---: | :---: | :---: | :---: | :---: |
| .608 | B4T64 | Cl | V4 | 60/90 | Inhibit step PC, supply EP if Uniservo is rewound. |
| $\checkmark 609$ | B4T79 | Gl | V11 | 60/90 | If Direction Memory agrees with instruction, gate EP to control circuits. |
| 609G | B4T46 | Notub | 51 | $n \tau$ | To FTIC. |
| $\sqrt{614}$ | B4T77 | E7 | V10 | 60/90 | Gate EP to set Read Forward and Start Read FF ${ }^{\text {s }}$ s after appropriate delay. |
| /615 | B4T48 | G4 | V12 | 60/90 | Gate EP to set Write Forward and Start Write $\mathrm{FF}^{\mathrm{P}}$ s after appropriate delay. |

产 Computer will pass interlock if: l. Read Interlock is reset.
2. Reversal Memory is reset.
3. IO INT-FF is reset.
4. First Block Memory is reset.
5. No rewind has been initiated within 3 ms .
\%* Length of time before Write Forward FF is set is determined by condition of Reversal Memory.

## Function

Table
$\sqrt{616}$
Chassis TT

| Tube | S/NS |
| :--- | :--- |
| V8 | $60 / 90$ |

## Definition

Generate signal to pass Supervisory Control interlock provided that no read, Supervisory Control type-out, or Supervisory Control type-in is in progress.

| $\sqrt{617}$ | B4T28 | A4 | V2 | 60/90 | Gate IRP to set Supervisory Control Output FF, set Write Interlock. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\checkmark 619$ | B4T53 | G7 | $\frac{\sqrt{V 16}}{\sqrt{2}, 4}$ | 60/90 | Generate BP signal and supply pulse to initiate Rewind Start circuits. |
| $\sqrt{621}$ | B4T66 | C5 | V6 | +5/-20 | Gate IRP as Sequence I Preset. |
| . 629 G | B4T38 | Cl4 | V5 | 30/90 | Generate nS (servo select) signal from Second Instruction digit. |
| L641+ | B5V62 | A18 | $\text { V4, } 1$ | +5/-20 | Inhibit set of $M_{1}$ cores, strobe rI sense amplifiers, and transfer $\mathrm{M}_{2} \rightarrow \mathrm{M}_{1}$ and $\mathrm{M}_{2} \rightarrow \mathrm{rI}$. Step rI address counters once for each word transferred until " 59 " signal occurs, at which time set MTO, step PC , and set TO . |


| 641+ | B5V71 | E12 | v8, $5+5 /-20$ |
| :---: | :---: | :---: | :---: |
| $\checkmark 641$ | B5V31 | A16 | V3, $4,1-20 /+5$ |

Permits the rI Preset error to be recognized during $\mathrm{PC}-2$ only in the $3 n$ or $4 n$ instruction.

| /645+ | B5V44 | E16 | V10, $9+5 /-20$ | Operate Input Distributor for typein. |
| :---: | :---: | :---: | :---: | :---: |
| $-669$ | B7T58 | Al3 | v2, $3+5 /-20$ | Gate IRP to generate Sequence 0 Preset. |
| , 681+ | B4V41 | E12 | v8, ${ }^{\text {S }}+5 /-20$ | Transfer M3 $\longrightarrow$ r0. Step r0 address counters once for each word transferred until "59" signal occurs at which time set MTO, step PC, and set T0. |
| $\overline{681+}$ | B4V79 | G11 | V12,9 +5/-20 |  |
| $\sqrt{681}$ | B4V38 | E18 | $\begin{aligned} & \text { V11-20/+5 } \\ & 12,9 \end{aligned}$ | Permits the ro No Address error to be recognized during PC-2 only of the $5 n$ or $7 n$ instruction. |


| Function <br> Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $685+$ | B5V81 | G12 | V12, ${ }^{\prime}$ | +5/-20 | Read $M_{3}$, transfer $M_{3} \longrightarrow M_{4}$, type out digit on SC printer. |
| $\checkmark 714 \mathrm{~A}$ | B6T60 | Cl | V4 | 60/90 | Operate adder for $12-$ place addition. |
| $\overline{714 \mathrm{~A}}$ | B6T31 | A6 | v3 | 60/90 |  |
| $\sim 144 \mathrm{~B}$ | B6T35 | C6 | V6 | 60/90 |  |
| $\longdiv { 7 1 4 \mathrm { B } }$ | B6T33 | C4 | V5 | 60/90 |  |
| $\checkmark 714 \mathrm{C}$ | B6T77 | E3 | v8 | 60/90 |  |
| $\overline{714 \mathrm{C}}$ | B6T44 | E2 | V7 | 60/90 |  |
| $\stackrel{737}{ }$ | C2v87 | G8 | V14 | 60/90 | Enables a tl pulse to reset the Overflow flip-flop. |
| $\checkmark \overline{737}$ | C2V85 | G6 | V13 | 60/90 |  |
| -816+ | B7V30 | Al5 | v3, 1 | +5/-20 | When the rZW tens and units counters read zero, gate a t59 to set MTO.*\# |
| $\sqrt{816 t}$ | BTV67 | C15. | v6, 4 | $\div 5 /-20$ |  |
| L817+ | B7V46 | G12 | V11,9 | +5/-20 | Preset rZW units counter to the elevens complement of the 2nd Instruction Digit. when counter reads zero, gate t59 to set MTO. |
|  | B7U5O | G17 | V13, 14,12 | +5/-20 |  |
| $\sqrt{817+}$ | B7V52 | G18 | V14,12, | +5/-20 |  |
| -818+ | B6V62 | Al7 | V4, 3 | +5/-20 | Whable the set of the rZMAR Read FF. following tl. |
| -818+ | B6V64 | C12 | V5, 6 | +5/-20 |  |
| $-819+$ | B3V76 | E3 | v9, 8 | +5/-20 | Strobe rZW sense amplifiers. |
| - $820+$ | B2V27 | A12 | V1, 2 | +5/-20 | Enable set of rM, rZW Read/Write FF's, set $M_{1}$ cores. |
| $\checkmark$ 821+ | B2V37 | C15 | v6, 5 | +5/-20 | Generate Strobe rM signal. |
| -823+ | B3V55 | C17 | v2, 1 | +5/-20 | Develop Staticize Pulse, Read $M_{1}$ cores, $M_{1} \longrightarrow P S, M_{1}$ to staticizer. |
| $\checkmark 823$ | B3V83 | G16 | V14 | 60/90 |  |

* If 2nd Instruction Digit is a 7, 8, 9, or 0, treat instruction as a Skip if Compatibility switch is set to Univac II.
\# If Compatibility switch is set to Univac I, the rZW tens counter is preset to zero.

| Function Table | Chassis | TT | Tube | S/NS | Definition |
| :---: | :---: | :---: | :---: | :---: | :---: |
| /824B | B2V31 | ${ }^{4}{ }^{4} 7$ | (v3) | $+5 /-20$ | Develop Serialize Pulse, Read $M_{1}$ <br> Cores, $M_{1} \longrightarrow P S, M_{I} \longrightarrow$ Serializer. |
| 824A | B2V79 | E16\% 6 | V11 | 60/90 | 0perate $\mathrm{rM} \longrightarrow$ HSB "extract" circuits. |
| $\overline{824 A}$ | B2V51 | G8 | V14 | 60/90 |  |
| . 825- | B4V55 | All | V1, ${ }^{2}$ | -25/gnd | Set MTO. $\times$ |
| . $\overline{825}$ | B4V59 | Cll | V4, ${ }^{3}$ | $-25 / \mathrm{gnd}$ | $X$ |
| /826+ | B3V37 | C15 | V7, 6 | $+5 /-20$ | Set $\mathbf{r M}$ and rZW Read/Write $\mathrm{FF}^{\text { }} \mathrm{s}$, Set $M_{1}$ cores. |
| - 827+ | B2V74 | E18 | V10,9 | $+5 /-20$ | Set BCM to RM. |
| $\overline{827}$ | B2V69 | C18 | VT, X | $+5 /-20$ |  |
| L. $829+$ | B2V81 | G2G12 | V12, 1 | -5/-20 | Transfer $\mathrm{M}_{1} \rightarrow \mathrm{M}_{3}$. |
| -831 | B9T54 | Al | V1 | 60/90 | Complement the operation of the "extract" circuit.* |
| - $\overline{831}$ | B9T87 | G7 | V14 | 60/90 |  |
| $832$ | B9T37 | C6 | V6 | $60 / 90$ | Disconnect CU (000000 000000) input to "extract" circuit, connect rA. |
| $\checkmark \overline{832}$ | B9T70 | C7 | V7 | 60/90 |  |
| $\longdiv { 8 3 3 + }$ | B6V79 | Gl | $\mathrm{V} 11 / 2$ | $+5 /-20$ | Step rM counters and rZW units counter once each minor cycle until rZW units counter reads zero. |
| $\checkmark \overline{833+}$ | B6V86 | G7 | V14,/3 | $+5 /-20$ |  |
| - 850 | ClV47 | G1 | V11 | 60/90 | Connect CC to SR via CR2.\# |
| C860+ | B7V71 | E12 |  | $+5 /-20$ | Operate rin address exceeded and preset checkers. |
| $\downarrow^{\prime 860}$ | B7V26 | Ell | V7 | +30/+90 |  |
| $\checkmark 861 \mathrm{~A}$ | B7T47 | $\mathrm{Al}_{\mathrm{E}} \mathrm{t}$ | V10, 1 | -20/+5 | Inhibit rM line drivers. |
| $\checkmark \overline{861 A}$ | B7T41 | E12 | $\text { v8, } 1$ | $-20 /+5$ |  |
| $\checkmark 861 \mathrm{~B}$ | B7T72 | $\begin{array}{r} \text { A } \\ \times \text { E14 } \end{array}$ | V9 V': | +30/+90 |  |
| Dumay 1 | B8V26 | (A2) <br> G/2 | サ $112$ | 60/90 | Enforce order of "eveness" in FTOC. |

\# RH Instruction set up at t7 of Delta T0.

