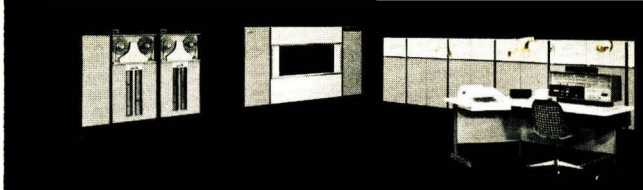
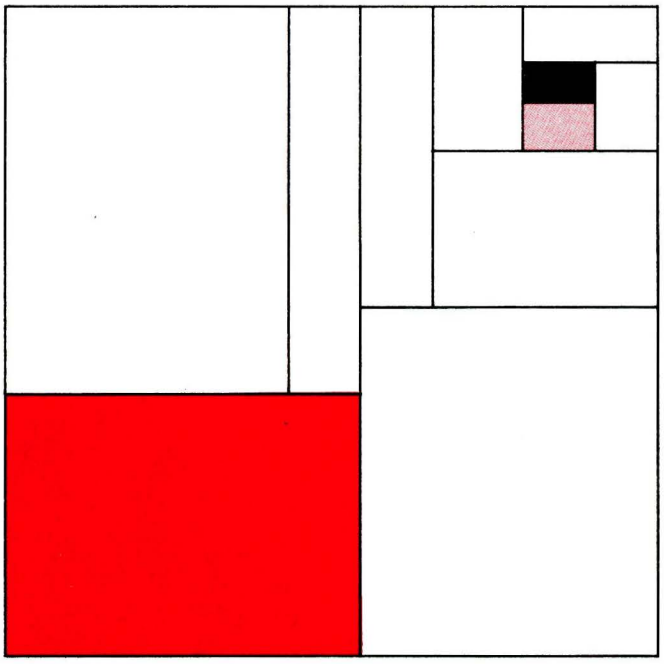


UNIVAC®
1050 SYSTEMS

TECHNICAL ABSTRACT



UNIVAC 1050

SYSTEMS

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Technical Information Abstract

UNIVAC 1050

C Card Systems

T Tape Systems

M Mass Storage Systems

R Real Time Systems

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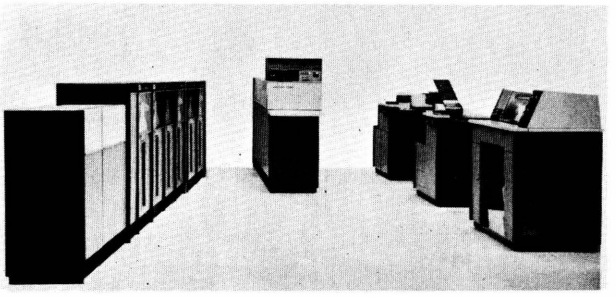
UNIVAC 1050–C



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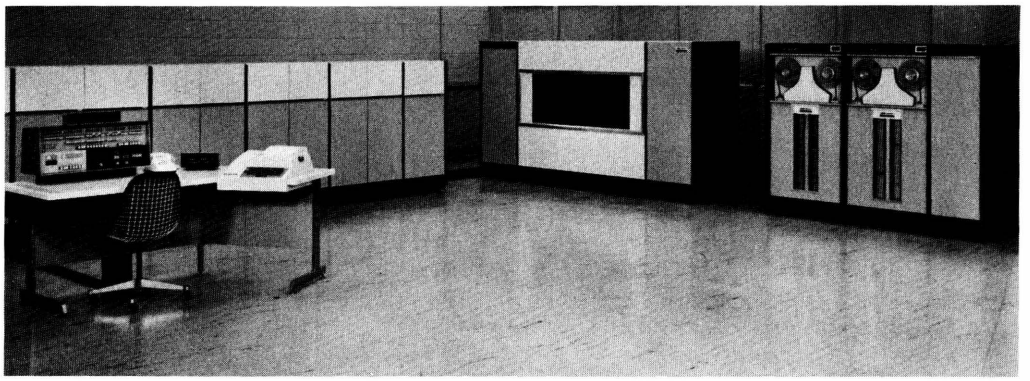

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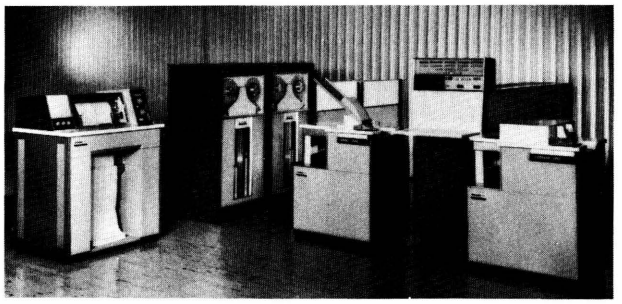
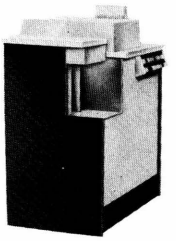
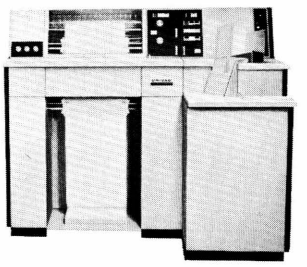
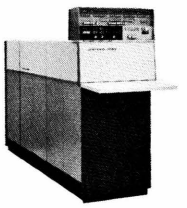


UNIVAC 1050–S







UNIVAC 1050–4

UNIVAC 1050 SYSTEMS

UNIVAC 1050 SYSTEMS

Technical Information Abstract

FOREWORD:

This manual presents a summary description of all UNIVAC 1050 Systems. The description of the hardware configurations available, software provided by system, and the hardware and software timing factors effecting through put and timing of UNIVAC 1050 Systems will enable the reader to evaluate the potential of the UNIVAC 1050 System which meets his exact requirements. This manual is intended for persons who already have a basic understanding of electronic data processing. The equipment specifications described herein may be subjected to revisions so that the latest technological improvments may be incorporated in UNIVAC 1050 Systems.

Table of Contents

UNIVAC 1050 SYSTEMS

Introduction

UNIVAC 1050 Systems - User oriented growth potential

UNIVAC 1050 Systems offer each user planned growth from a small powerful card oriented data processing system to a complete, high speed sophisticated mass storage, magnetic tape or real time oriented system. Each of these systems is program compatible to assure the user maximum protection of programming investment. The UNIVAC 1050 family of systems gives the user the ability to match the data processing system with his individual needs. The ability to adjust peripheral power, memory capacity, and processor speed gives the user a catalog of abilities to meet both the current as well as future data processing requirements.

UNIVAC 1050 Systems - Central Processors

The key to the modularity of UNIVAC 1050 Systems is in the flexible design philosophy built into the UNIVAC 1050 Central Processor. Two processing units are offered - Model III with 4.5 microsecond cycle time per character and Model IV with 2.0 μ sec. for two characters. Up to eight input/output channels on each of these Central Processors handle a variety of input/output peripheral units. Each channel generates an interrupt to the Central Processor to indicate when Central Processor action is required; this provides the user with minimum peripheral lock out time and maximum through put capabilities. The Central Processor also provides buffering of data from all channels, providing maximum channel overlap. The selection of the proper processor unit to satisfy the application requirement provides the user with the minimum cost for the maximum capability.

UNIVAC 1050 Systems - Peripheral Components

A variety of peripheral capabilities are offered with the UNIVAC 1050 Systems; from a 400 CPM reader to a 133 KC transfer rate magnetic tape or 185 KC transfer rate mass storage unit. This wide range of peripheral capability enables the user to select the peripherals needed for his job

without the requirement of tailoring the application to the computing system. The following table summarizes the peripheral modularity offered by UNIVAC 1050 Systems.

UNIVAC 1050 SYSTEMS – PERIPHERAL MODULARITY

CARD READING	400 CPM*	600 CPM	800/900 CPM**
CARD PUNCHING	200 CPM*	200 CPM	300 CPM
PRINTING	400 LPM*	600/750 LPM	700/922 LPM
MAGNETIC TAPE UNITS - Transfer Rates Characters/Second			
Uniservo VI C	8,500	23,700	34,100
Uniservo IV C	22,500	62,500	90,000
Uniservo III A	100,000	133,000	
FASTRAND MASS STORAGE Capacity - 66,000,000 Characters, Average Access to any character 92 Milliseconds, Transfer Rate 185,000 characters/second.			
Punched Paper Tape - Read 400/1,000 characters/second; Punch 110 characters/second.			
Communications Equipment - A variety of devices employing both telegraphic and voice grade transmission capabilities.			
*These speeds are attained through use of the UNIVAC 1004 Card Processor on line to the UNIVAC 1050 Central Processor. **Speed varies depending upon number of columns read. 900 CPM attained reading 72 columns of information.			

The Catalog of UNIVAC 1050 Systems

To enable the user to more easily select the exact system to meet his requirement, the UNIVAC 1050 Systems have been catalogued as follows:

UNIVAC 1050C Series - Card Systems
UNIVAC 1050T Series - Tape Systems
UNIVAC 1050M Series - Mass Storage Systems
UNIVAC 1050R Series - Real Time Systems
UNIVAC 1050S Series - Satellite Systems
UNIVAC 1050-4 Series - 1004 Expansion Systems

A brief description of each of these systems follows:

UNIVAC 1050C Series

This series of card oriented computing systems is designed to close the gap between input data and final reports for the punched card user. The C series features a variety of different card and printer peripherals to enable the user to select the exact system for the data processing requirement.

Configurations

Card reading - 600 or 800/900 CPM
Card punching - 200 or 300 CPM
Line printing - 600/750 LPM
700/922 LPM
Central Processor - Model III
4K to 32K, 4.5 μ sec per character.
Model IV
8K to 65K, 2.0 μ sec per two characters.

UNIVAC 1050T Series

This series of tape oriented computing systems is designed to enable punched card, competitive computer, or existing UNIVAC 1050C users to take advantage of the file passing, sorting, and collating abilities of magnetic tape. All existing UNIVAC 1050C programs will operate on a UNIVAC 1050T System.

Configurations

Card reading — same as
Card punching — UNIVAC
Line printing — 1050C
Central Processor — series

Magnetic Tape:
UNIVAC compatible
100-133 KC transfer rate
Compatible mode
8.5-90 KC transfer rate

UNIVAC 1050M Series

This series of mass memory oriented computing systems is designed to enable punched card, competitive computer, or existing UNIVAC 1050 C or T users to take advantage of rapid access to millions of characters of information. All existing UNIVAC 1050C or T programs will operate on a UNIVAC 1050M System.

Configurations

Card reading — same as
Card punching — UNIVAC 1050C
Line printing — UNIVAC 1050T
Central Processor — series
Magnetic tape
Mass memory - 185 KC transfer rate
Capacities - 66 to 528 million characters in 66 million increments
Access time - 92 milliseconds average

UNIVAC 1050R Series

This series of communication oriented systems is designed to enable UNIVAC 1050C, T, or M users to take advantage of decentralized control of remote facilities through a communications network. All existing UNIVAC 1050C, T, or M programs will operate on a UNIVAC 1050R System.

Configurations

Card reading — same as
Card punching — UNIVAC 1050C
Line printing — UNIVAC 1050T
Central Processor — UNIVAC 1050M
Magnetic tape — series
Mass memory
Communication Subsystem - 4, 8, 16, or 32 communications line terminals.

Communications Line Terminals

- Low Speed - Up to 300 BPS (50L, 51L, 80L, 81L)
- Medium Speed - 300 to 1600 BPS (80M, 81M)
- High Speed - 1600 to 4800 BPS (80H, 81H)

UNIVAC 1050S Series

This series of satellite systems is designed to assist large scale computer users in performing the utility operations of card to tape, tape to punch, tape to print, etc. This frees the larger systems time and memory for the important main computer application runs.

Configurations

Card reading — same as
Card punching — UNIVAC 1050C
Line printing — series
Central Processor

Magnetic tape 1 or 2 tapes
UNIVAC compatible - 100, 133 KC
Compatible mode - 8.5 to 90 KC

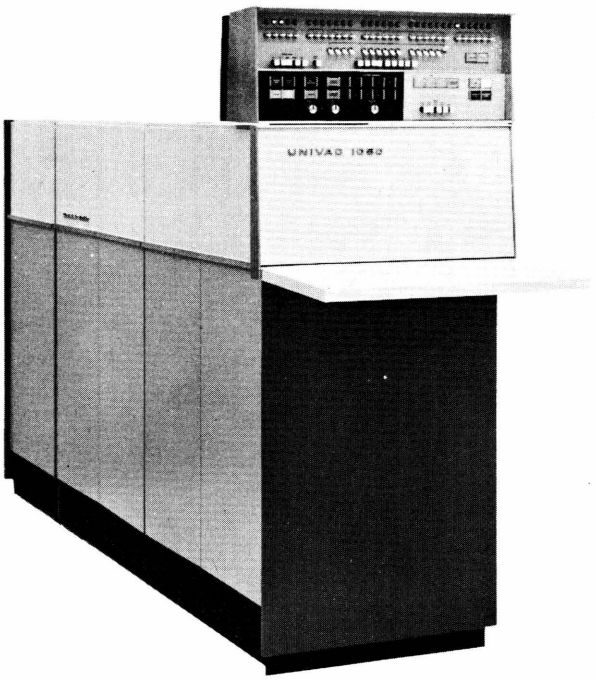
UNIVAC 1050-4 Series

This series of systems is designed to enable existing 1004 users to expand their data processing abilities with a minimum of effort. All existing UNIVAC 1004 programs will operate as initially programmed; only the new data processing requirements need be programmed. This series provides an easy transition from external to internally programmed systems.

Configurations

Central Processor - Model III or Model IV
1004 - adaptor
UNIVAC 1004
(May also include the following)
Card reading
Card punching — same as
Line printing — UNIVAC 1050
Magnetic tape — C, T, M, R
Mass storage
Communications

The Central Processor



CENTRAL PROCESSOR

OPTIONAL CONTROL CONSOLE

The heart of the Univac 1050 System is the Central Processor. The Central Processor contains the Control, Arithmetic, Storage, Indexing and other processing components which operate under program direction to perform the input-output, logical and arithmetic functions of the System.

MODEL III PROCESSOR

The Model III Processor available with UNIVAC 1050 Systems has a basic memory of 4096 seven bit characters of core storage; with a cycle time of 4.5 microseconds per character. Up to eight modules, 4096 characters per module, may be incorporated in a Model III Processor to provide a total storage capacity of 32,768 characters.

MODEL IV PROCESSOR

The Model IV Processor available with UNIVAC 1050 Systems has a basic memory of 8192 seven bit characters of core storage with a cycle time of 2.0 microseconds per two characters. Up to eight modules, 8192 characters per module, may be incorporated in a Model IV Processor to provide a total storage capacity of 65,536 characters. Programs written to utilize the abilities of the Model III Processor are upwards compatible with the Model IV.

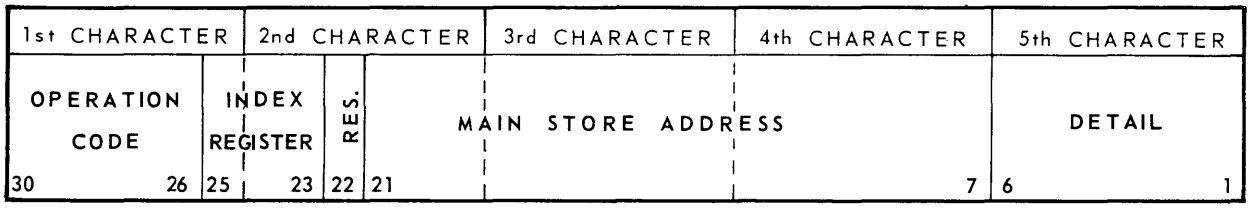
REPRESENTATION OF DATA

Data may be represented within the Univac 1050 System as either six-bit alphanumeric characters or as pure binary numbers. Special arithmetic instructions and data manipulation instructions are provided to deal with both binary and binary coded decimal representations.

The length of a particular data field is defined by the instructions that manipulate the data. In most instructions, a character count is provided to define the length of the data field.

INSTRUCTION FORMAT

Each instruction occupies five character positions. Instructions are always represented internally in binary form. The General Instruction format is shown below:



The first five bits of the instruction (30 through 26) define the operation code. The operation code specifies the function the Central Processor is to execute. The operation code is modified by the detail character (bits 6 through 1) which either defines the length of the data field involved, or expands upon the function to be performed. Bits 25 through 23 define the index register to be used with this instruction. The memory address of the operand involved in the instructions is designated by the address contained in bits 22 through 7. This is the general format of the instructions in the Univac 1050 System. Certain instructions such as input and output

CARD CODES		BINARY CODE (Machine Collating Sequence)	HIGH-SPEED PRINTER CHARACTER		OCTAL	NUMBER
80 COLUMN	90 COLUMN		STANDARD	OPTIONAL		
NO PUNCH	NO PUNCH	000000	Space (Non-Printing)		00	0
11-5-8	1-3-5-7	000001	]		01	1
11	0-3-5-7	000010	– (minus or hyphen)		02	2
0	0	000011	0		03	3
1	1	000100	1		04	4
2	1-9	000101	2		05	5
3	3	000110	3		06	6
4	3-9	000111	4		07	7
5	5	001000	5		10	8
6	5-9	001001	6		11	9
7	7	001010	7		12	10
8	7-9	001011	8		13	11
9	9	001100	9		14	12
0-6-8	0-1-3-7-9	001101	\		15	13
11-6-8	1-3-5-7-9	001110	;		16	14
12-5-8	0-5-7-9	001111	[		17	15
12	0-1-3-5-7	010000	+	&	20	16
5-8	1-3-7-9	010001	: (colon)		21	17
12-3-8	1-3-5-9	010010	. (period)		22	18
12-0	0-1-3	010011	?		23	19
12-1	1-5-9	010100	A		24	20
12-2	1-5	010101	B		25	21
12-3	0-7	010110	C		26	22
12-4	0-3-5	010111	D		27	23
12-5	0-3	011000	E		30	24
12-6	1-7-9	011001	F		31	25
12-7	5-7	011010	G		32	26
12-8	3-7	011011	H		33	27
12-9	3-5	011100	I		34	28
3-8	0-1-5-7	011101	=	#	35	29
12-6-8	0-1-5-9	011110	<		36	30
12-7-8	0-1-3-5-7-9	011111	#		37	31
7-8	0-1-5-7-9	100000	@	' (apostrophe)	40	32
11-4-8	0-1	100001	*		41	33
11-3-8	0-1-3-5-9	100010	$		42	34
11-0	0-3-7-9	100011	!		43	35
11-1	1-3-5	100100	J		44	36
11-2	3-5-9	100101	K		45	37
11-3	0-9	100110	L		46	38
11-4	0-5	100111	M		47	39
11-5	0-5-9	101000	N		50	40
11-6	1-3	101001	O		51	41
11-7	1-3-7	101010	P		52	42
11-8	3-5-7	101011	Q		53	43
11-9	1-7	101100	R		54	44
0-5-8	0-1-9	101101	%	(	55	45
4-8	0-1-3-7	101110	' (apostrophe)	@	56	46
11-7-8	0-1-7	101111	△		57	47
0-2-8	0-1-7-9	110000	≠		60	48
0-4-8	0-1-5	110001	(	%	61	49
0-3-8	0-3-5-9	110010	, (comma)		62	50
2-8	1-5-7-9	110011	&	+	63	51
0-1	3-5-7-9	110100	/		64	52
0-2	1-5-7	110101	S		65	53
0-3	3-7-9	110110	T		66	54
0-4	0-5-7	110111	U		67	55
0-5	0-3-9	111000	V		70	56
0-6	0-3-7	111001	W		71	57
0-7	0-7-9	111010	X		72	58
0-8	1-3-9	111011	Y		73	59
0-9	5-7-9	111100	Z		74	60
12-4-8	0-1-3-9	111101	)	¤	75	61
6-8	0-3-5-7-9	111110	>		76	62
0-7-8	0-1-3-5	111111	¤	)	77	63

***NOTE:** Only the characters that differ from the standard are listed for the optional print drum.

UNIVAC 1050 System Character Set

control utilize the instruction word in a slightly different manner. This will be explained in more detail in another section of this manual. Bit 22 is utilized for addressing in the Model IV Processor and must not be otherwise used for the Model III Processor if upwards compatibility is desired.

TETRADS

The first 256 character positions of the Univac 1050 Memory are subdivided in 4 character fields which are called Tetrads. The Tetrads are special purpose fields which are addressable by Tetrad number as well as being character addressable. Tetrads are used as arithmetic registers, index registers, and control information for input-output operations and special functions such as Block Transfer and Translate.

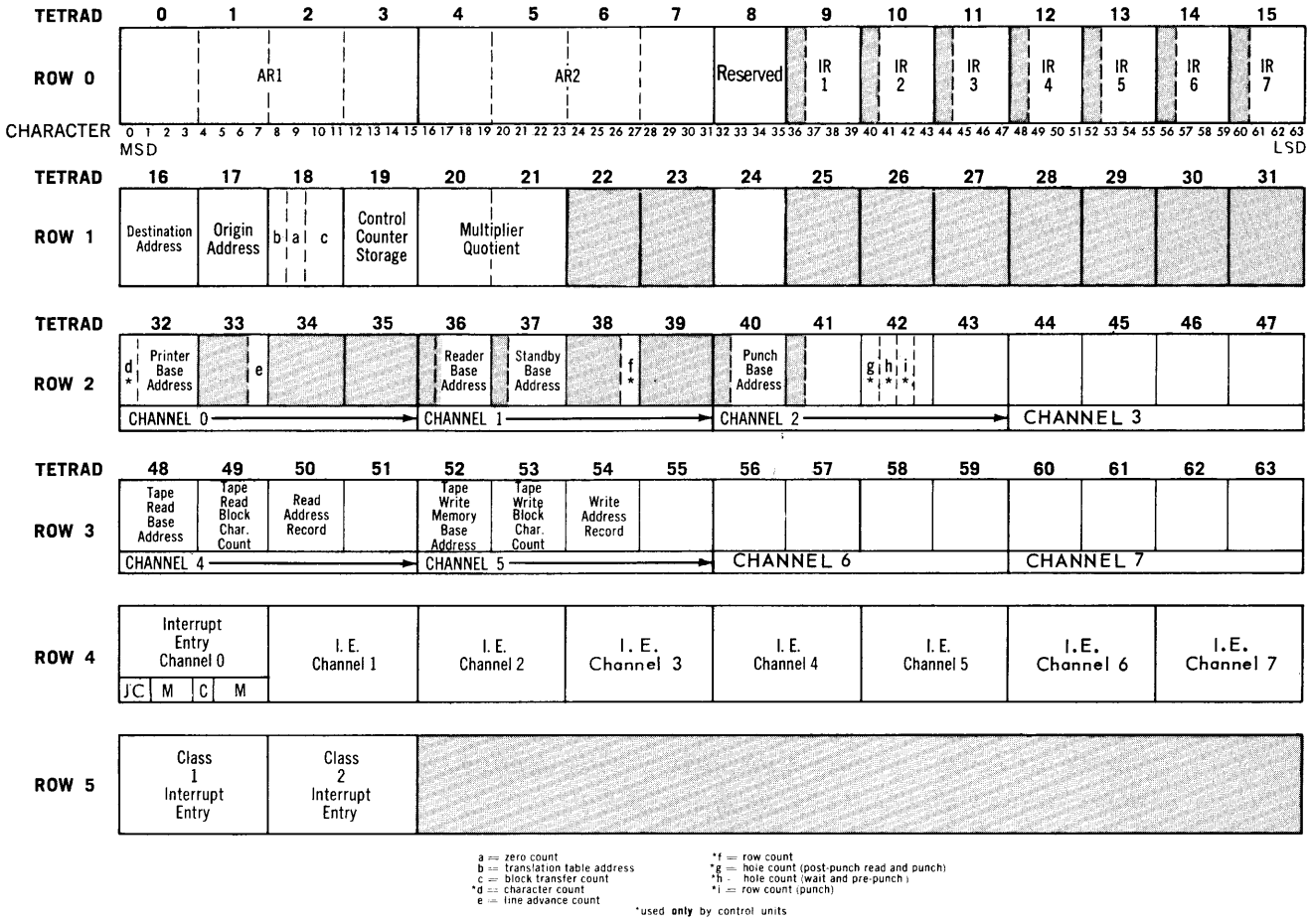
ARITHMETIC REGISTERS

Two 16-character arithmetic registers are provided to reduce the necessity of storing intermediate results. These registers are the first eight (0-7) Tetrads. They may be addressed by character (00-31) or by Tetrads (0-7). Through the use of assembly language they are referenced as AR1 or AR2. Tetrads 0, 1, 2, 3 (locations 0 through 15) form arithmetic register 1 (AR1) and Tetrads 4, 5, 6, 7 (locations 16 - 31) form arithmetic register 2 (AR2). The most significant character of each AR is its low order position.

INDEX REGISTERS

Seven index registers are provided in the Univac 1050 System. Tetrads 9, 10, 11, 12, 13, 14 and 15 contain the index registers. When utilized as index registers, only those bits which pertain to memory address are involved and the preceding bits are ignored. The index registers are character addressable, Tetrad addressable, and through the PAL assembly system addressable as index registers 1 through 7. A designation of zero in the index portion of an instruction indicates that index modification is not required.

An example of the memory layout showing the arithmetic registers, index registers, interrupt entries and Tetrads is pictured on the following chart.



Some special features include the following instructions:

JL - Jump Loop - This instruction will branch from 1 to 62 times depending on a counter which is part of this instruction. When the counter is automatically decremented to 1, control will pass to the next instruction following the JL instruction.

JR - Jump Return - This instruction provides the programmer with the facility to break program sequence and execute a subroutine, returning program control to the instruction immediately following the JR instruction.

TTI, TTR, TFI, TFR - Transfer Block - This group of instructions will transfer consecutive characters from one memory location to another depending on the contents of Tetrads 16 and 18, or Tetrads 17 and 18. The number of characters transferred can vary from 1 to 1024.

ZS - Zero Suppress - These instructions will replace blanks, zeros,
ZS* and commas with blanks or asterisks until a character which is
ZS$ neither a blank, a zero nor a comma is encountered. A dollar sign can also be inserted in the last position replaced.

Example:

Before Command 0, 347.12

After Command

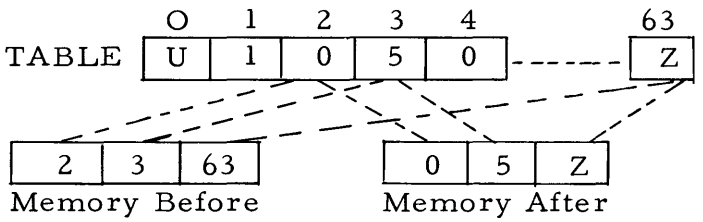
ZS	⟶	347.12
ZS*	⟶	**347.12
ZS$	⟶	$347.12

ED - Edit - This instruction will edit a field in AR1 depending on the mask in AR2. It has the power to interpret the sign of a field and also insert characters in a field.

Example:
MASK - AR2 - $@, @@@. @@
FIELD - AR1 - 421734
AFTER COMMAND - $4, 217. 34

TR - Translate - This instruction replaces characters in a field with characters in a table based on the binary value of the characters in the field being replaced.

Example:



OCTAL OP CODE	MNEMONIC	DESCRIPTION
00	–	(Unassigned)
02	–	"
04	–	"
06	–	"
10	JR	Jump Return
12	TR	TRanslate
14	LC	Logical Comparison
16	BCn	Bit Circulate
16	BSn	Binary Shift
20	FT	Fix Tetrad
22	ZS*	Zero Suppress with asterisk fill
22	ZS$	Zero Suppress with floating dollar sign
22	ZS	Zero Suppress with no floating dollar sign
24	TFI	Transfer From memory, Increment destination address
24	TFR	Transfer From memory, Reset destination address
24	TTI	Transfer To Memory, Increment origin address
24	TTR	Transfer To memory, Reset origin address
26	PD	PaD blanks
26	PD0	PaD decimal zeros
26	CDa	Compare Decimal
30	JC	Jump Conditionally
30	JE	Jump if Equal
30	JG	Jump if Greater
30	JS	Jump if Smaller
30	JU	Jump if Unequal
32	JL	Jump Loop
34	CC	Compare Character
36	–	(Unassigned)
40	XF	eXternal Function
42	ST	Store Tetrad
44	SC	Store Character
46	BT	Bring to Tetrad
50	DV	DiVide
50	MPC	MultiPly Cumulative
50	MPN	MultiPly Noncumulative
52	ED	EDit
52	SAa	Store Arithmetic register
52	SAR	Store both Arithmetic Registers
54	LP	Logical Product
56	BAa	Bring Alphanumeric
56	BDa	Bring Decimal
60	AC	Add Character
62	AMa	Add to Memory
62	SMa	Subtract from Memory
64	LS	Logical Sum
66	ADa	Add Decimal
66	SDa	Subtract Decimal
70	CBa	Compare Binary
72	ABa	Add Binary
72	SBa	Subtract Binary
74	CT	Compare Tetrad
76	AT	Add to Tetrad

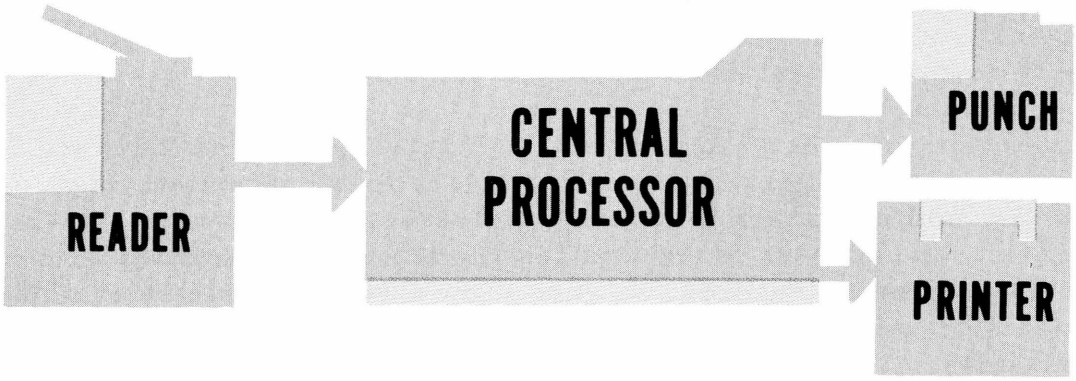
MNEMONIC OPERATIONS ORDERED BY OPERATION CODE.

MNEMONIC INSTRUCTION	OCTAL OP CODE	DESCRIPTION
ABa	72	Add Binary
AC	60	Add Character
ADa	66	Add Decimal
AMa	62	Add to Memory
AT	76	Add to Tetrad
BAa	56	Bring Alphanumeric
BCn	16	Bit Circulate
BDa	56	Bring Decimal
BSn	16	Binary Shift
BT	46	Bring to Tetrad
CBa	70	Compare Binary
CC	34	Compare Character
CDa	26	Compare Decimal
CT	74	Compare Tetrad
DV	50	DiVide
ED	52	EDit
FT	20	Fix Tetrad
JC	30	Jump Conditionally
JE	30	Jump if Equal
JG	30	Jump if Greater
JL	32	Jump Loop
JR	10	Jump Return
JS	30	Jump if Smaller
JU	30	Jump if Unequal
LC	14	Logical Comparison
LP	54	Logical Product
LS	64	Logical Sum
MPC	50	MultiPly Cumulative
MPN	50	MultiPly Noncumulative
PD	26	PaD blanks
PD0	26	PaD decimal zeros
SAa	52	Store Arithmetic register
SAR	52	Store both Arithmetic Registers
SBa	72	Subtract Binary
SC	44	Store Character
SDa	66	Subtract Decimal
SMa	62	Subtract from Memory
ST	42	Store Tetrad
TFI	24	Transfer From memory, Increment destination address
TFR	24	Transfer From memory, Reset destination address
TR	12	TRanslate
TTI	24	Transfer To memory, Increment origin address
TTR	24	Transfer To memory, Reset origin address
ZS*	22	Zero Suppress with asterisk fill
ZS$	22	Zero Suppress with floating dollar sign
ZS	22	Zero Suppress with no floating dollar sign
XF	40	eXternal Function

MNEMONIC OPERATIONS ORDERED ALPHABETICALLY.

Input-Output Control

The Univac 1050 System is equipped with bi-directional Input-Output channels which direct the flow of data between the Central Processor and the peripheral subsystems. The basic Univac 1050 III System is provided with three channels; an additional five channels are available at the customer's option.



Associated with each of the Input-Output channels is a fixed storage area consisting of 16 characters (four consecutive Tetrads). Information placed in this area controls the operation of the peripheral device and its data transfer; data transfers can be to any location in the computer memory. These Control Tetrads contain information such as the base address where data is to be taken from or placed, the number of lines to be skipped prior to printing, the number of characters to be written or read from tape, etc. In some instances they are used to record the present status of a control unit's sequence of operation, i.e., what row is being punched, what the hole count is, etc. The precise content of any channel Control Tetrad is a function of the subsystem associated with the channel and the operation being performed.

AUTOMATIC PROGRAM INTERRUPT

Automatic program interrupt is a feature incorporated into the control circuitry of the Univac 1050 System which enables the System to operate at optimum overall efficiency. The automatic program interrupt feature permits the efficient utilization of all Input-Output devices operating under control of the Central Processor.

Basically, automatic program interrupt consists in the generation of a signal to the Central Processor upon the recognition of a condition which requires immediate attention from the program. These interrupt signals are assigned a priority within a hierarchy of interrupts in order to facilitate their processing.

Associated with automatic program interrupt is interrupt inhibit, which prevents the acceptance of an interrupt signal when it is generated. However, the interrupt signal is stored in an indicator so that it will not be forgotten.

Interrupt results from one of two general classes of occurrences: first, an error, fault or emergency condition occurring either in the Central Processor or in an Input-Output device; and second, successful completion of an Input-Output function, or, in some cases, when an Input-Output device is ready to accept an Input-Output command.

Upon the occurrence of an interrupt, and if interrupt has not been inhibited, control is transferred to one of ten fixed store locations which must contain the starting address of a routine which processes the interrupt. At the time of interrupt, the address of the next instruction to be performed in the interrupted program is recorded as part of the interrupt table entry. Storage locations 256 through 335 are the fixed locations associated with the interrupt circuitry. These eighty locations are divided into ten groups of eight consecutive characters each, which are known as interrupt entries. These interrupt entries are assigned as follows:

ADDRESS	CHANNEL
256-263	Channel 0
264-271	Channel 1
272-279	Channel 2
280-287	Channel 3
288-295	Channel 4
296-303	Channel 5
304-311	Channel 6
312-319	Channel 7
320-327	Class I
328-335	Class II

The Class I Interrupt reflects conditions of a memory parity error which might be caused by referencing memory modules not contained in the Processor.

The Class II Interrupt is utilized to indicate operator request and arithmatic overflow. The utilization of interrupt entry for these conditions allows a subroutine to analyze and correct the problem, and permits continuation of the program if desired. The Input-Output interrupts are designated as Class III Interrupts and they are assigned a lower priority than the other classes.

The eight character interrupt entry register will contain the address of the subroutine that is to handle interrupts on this channel or of this class. This, in conjunction with the address stored at the time of interrupt, provides the control necessary to process the interrupt and return to the interrupted program.

The Interrupt Entry Register has the format:

JC	K_1	K_2	K_3	I	M_1	M_2	M_3

The Interrupt Entry Register performs two basic functions. First, it contains in positions M_1, M_2, and M_3 the location of the first instruction of the proper interrupt routine; that is, the one associated with that particular channel entry point. The positions K_1, K_2, and K_3 contain the location of the next step to be performed when returning to the main program; that is, the contents of the control counter at the time of interruption.

In addition, characters 1 through 5 normally constitute the Jump Test which releases the interrupt for the priority class associated with its channel Interrupt Entry Register. The index register bits in character one will be set to binary zero.

Regardless of the class of interrupt, the following sequence of actions is executed whenever an interrupt request is accepted:

1. Except for Class I Interrupt the instruction in progress at the time of Automatic Interrupt is completed.

2. The next instruction's address in the program being interrupted is stored in the Interrupt Entry Register associated with the channel which initiated the interrupt request. It is stored in positions, K_1, K_2, and K_3 as shown in the diagram above.

3. The Processor enters the interrupt routine by transferring an address from the appropriate Interrupt Entry Register to the control counter. Moreover, a signal is generated which prevents the Processor from accepting additional interrupt requests from channels of the same or lower classes. While steps 2 and 3 are in progress, the Processor will not recognize subsequent interrupt requests of any kind. At the completion of step 3, interrupts of higher classes are accepted.

Programs that use the PAL Assembler library of Input-Output routines and that operate under the control of the Coordinator routine supplied by UNIVAC are relieved of the burden of controlling and coordinating interrupts. A comprehensive set of interrupt coding is provided in these routines. Input-Output requests are initiated by the External Function Instruction. The format of the External Function Instruction differs from that of other UNIVAC 1050 instructions.

The machine format of the External Function Instruction is:

OP CODE	CHANNEL	UNIT	FUNCTION	DETAIL/INDICATORS

The operation code of an External Function Instruction is always 40. The channel designates one of the eight Input-Output channels. The unit is zero where only one unit is assigned to the channel, and for multi-unit subsystems such as magnetic tape it specifies the particular unit involved. The function portion of the instruction defines the operation to be performed by the peripheral unit. The detail/indicators field is utilized in <u>two</u> ways. First, as detail it expands upon the stated function to define such matters as whether the card image should be translated or untranslated, whether to print a full line or half line, the density of writing tapes, and in what direction tape read orders should be executed. Secondly, in the test and reset indicators function these bits designate the indicators. Each subsystem has a set of indicators which indicate if any off-normal or error condition exists. These indicators are checked after each interrupt to determine if this is a successful completion of a previous I/O request or a fault condition interrupt.

INPUT-OUTPUT CONTROL - SUMMARY

Two sets of memory locations are assigned for use with each Input-Output channel.

1. Four groups of four characters each (Tetrads) are assigned for each I/O channel. These contain memory base addresses, block character counts, and other details pertaining to an I/O function.

2. Eight character positions (Interrupt entries) are assigned to each I/O channel to work with the automatic I/O interrupt feature. These positions contain the information necessary to transfer to a routine to service an interrupting I/O device and to return control to the interrupted program.

Input-Output control in the UNIVAC 1050 System will involve the following functions:

1. Placing a memory base address into a Tetrad which provides a specific I/O control unit with the initial memory position to which or from which data transfers will take place.

2. Placing into other Tetrads any detail information (character counts, sector counts, etc.) necessary to perform a given I/O instruction.

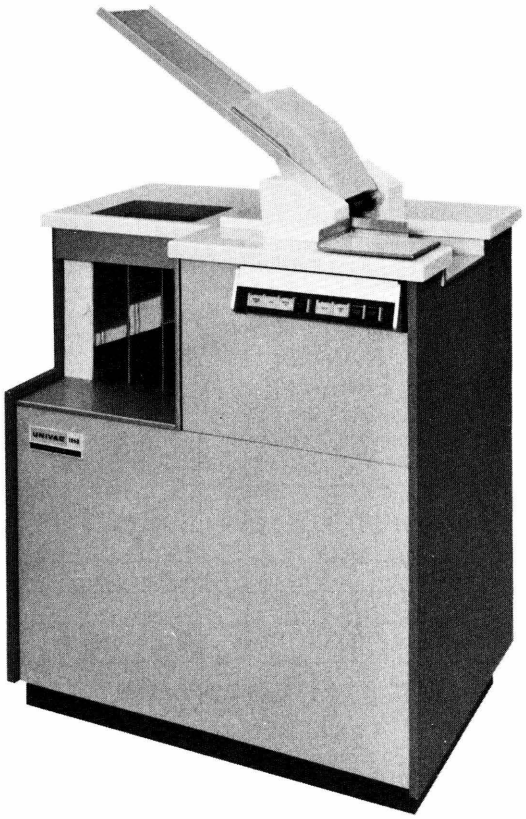
3. Issuing an I/O instruction which specifies the channel to be used, the particular I/O unit involved (if more than one is in the system), and the function or operation required.

4. Testing the Input-Output indicators to determine if the operation was completed successfully.

This logic and its associated interrupt control is all provided by the Input-Output library routines and macros that are available with the PAL Assembly System. Where advantage can be gained, these Input-Output subroutines provide reserve storage areas so that card reading, punching, and printing may proceed at maximum rate even though the processing time for any individual record may be subject to extensive variations.

UNIVAC 1050 PERIPHERAL SUBSYSTEMS

THE UNIVAC 1050 CARD READERS



Two card readers are available with the UNIVAC 1050 System. They are a 600 card/minute reader and a 800/900 card/minute reader. These readers are available for either 80 or 90 column punched cards. Both readers have the same basic features and they both have the same programming interface. The 800/900 card per minute reader will attain the 900 cards per minute speed while reading 72 columns of information. The issue of read commands and control of the card reader will normally be accomplished with the card reader subroutine supplied as part of the UNIVAC 1050 Software.

Features:

1. 2,500 card input hopper
2. 2,500 card output stacker
3. 100 card reject stacker
4. Photodiode Sensing
5. Automatic sensing check prior to each card read
6. Binary image reading
7. Automatic translation (80 column only)
8. Optional stub card feed
9. Clutched Reader (Read rate does not drop off at a fixed ratio but will be at the demand frequency of the program up to rated speed).

Timing Factors:

	900* Card/Min.		600 Card/Min.	
	Model III Processor	Model IV Processor	Model III Processor	Model IV Processor
Card Cycle (M.S.)	66	66	100	100
Memory Interlock I/O (M.S.)	6.0	.16	6.0	.16
Software Execution (M.S.)	2.0	.52	2.0	.52
Time Available to Process (M.S.)	58.0	65.32	92.0	99.32
No. of Avg. Inst/Card	580	2,512	920	3,820

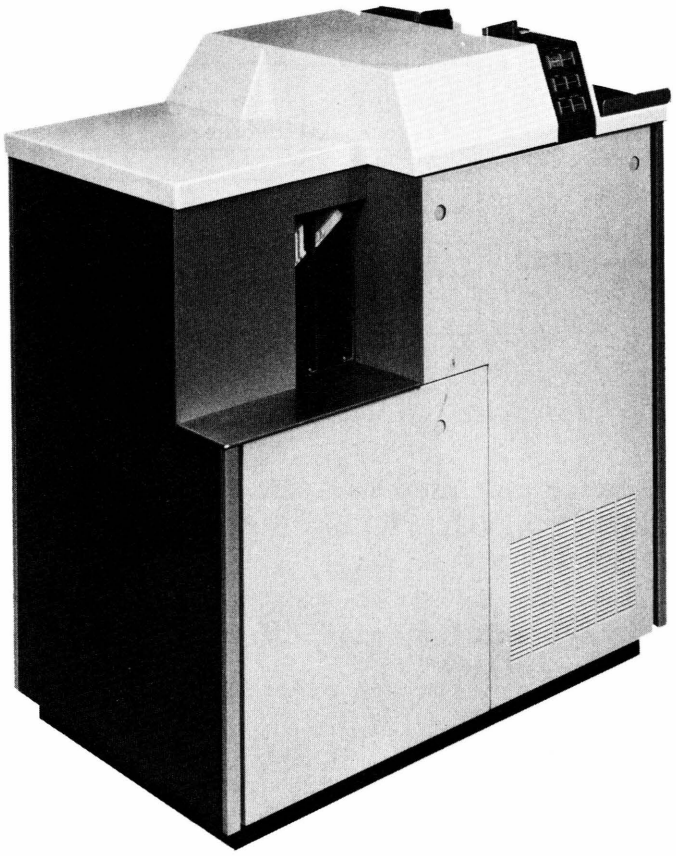
*Based on reading 900 CPM @ 72 columns per card.

Simultaneity:

1. The card reader may run with all peripherals except UNISERVO IIIA, UNISERVO IVC, VIC, and FASTRAND when using the Model III Processor.

2. The card reader may run with all peripherals when using the Model IV Processor.

THE UNIVAC 1050 CARD PUNCH



The two card punch units for the UNIVAC 1050 System operate at 200 cards per minute and 300 cards per minute respectively. Under the control of the programs in the Central Processor cards may be selectively punched or cards may be advanced without punching. Either an 80 or 90 column punch unit may be specified. Both the 300 card/minute and 200 card/minute card punch units have the same features and program interface. A punch subroutine is supplied as part of the PAL assembly library, and program control of the card punch unit is usually exercised through the subroutine.

Features:

1. A 1,000 card input hopper
2. Two output stackers, each with an 850 card capacity
3. Binary image punching
4. Automatic translation (80 column only)
5. Post punch check-read station utilizing positive hole count check.

Timing Factors:

	300 Card/Min.		200 Card/Min.	
	Model III Processor	Model IV Processor	Model III Processor	Model IV Processor
Card Cycle (M.S.)	200	200	300	300
Memory Interlock I/O (M.S.)	5.1	.16	5.1	.16
Software Execution (M.S.)	2.0	.52	2.0	.52
Time Available to Process (M.S.)	192.9	199.32	292.9	299.32
No. of Avg. Inst/Card	1,929	7,666	2,929	11,512

Simultaneity:

1. The card punch unit may run with all peripherals except UNISERVO IIIA, UNISERVO IVC, VIC and FASTRAND when using the Model III Processor.

2. The card punch unit may run with all peripherals when using the Model IV Processor.

THE UNIVAC 1050 PRINTER

The UNIVAC 1050 System may be equipped with a 600/750 line per minute printer or for larger print volumes a 700/922 line per minute printer. The range of printer speeds for each printer is determined by the characters that are printed in a line. Full rated speeds, 750 or 922 lines per minute, are attained while printing alphabetic and numeric characters. Extended use of special symbols can cause print speeds to slow down towards the lower rates. An optional buffer is provided for the printers. This buffer increases the amount of each print cycle that is available for processing. A subroutine to handle the printer is provided as part of the PAL Assembly library. The buffer is required with the 700/922 line per minute printer and whenever the 800/900 reader is used. It is also required on all other than Card Systems and on all Processor IV Systems.

Features:

1. 128 print positions per line
2. Vertical lines per inch, either 6 or 8 at option of operator
3. Horizontal spacing - 10 characters per inch
4. Half line printing - 64 characters. Reduces ribbon wear and I/O memory interlock
5. 63 printable characters - A-Z, 0-9, and 27 special symbols
6. Continuous paper feed rate - 20 inches/second
7. Paper stock - 4 to 22 inches in width, up to card stock thickness.
8. Copies - an original and at least five carbons can be obtained with 10 to 12# paper.

Timing Factors:

	600/750 LPM		700/922 LPM	
	Model III Processor	Model IV Processor	Model III Processor	Model IV Processor
Print Cycle* (M.S.)	80	80	65	65
Memory Interlock I/O** (M.S.)	.6	.26	.6	.26
Software Execution (M.S.)	2.0	.52	2.0	.52
Time Available to Processor (M.S.)	77.4	79.22	62.4	64.22
No of Avg. Inst/Line	774	3,047	624	2,469

* Includes printing and spacing one line.
** With optional print buffer

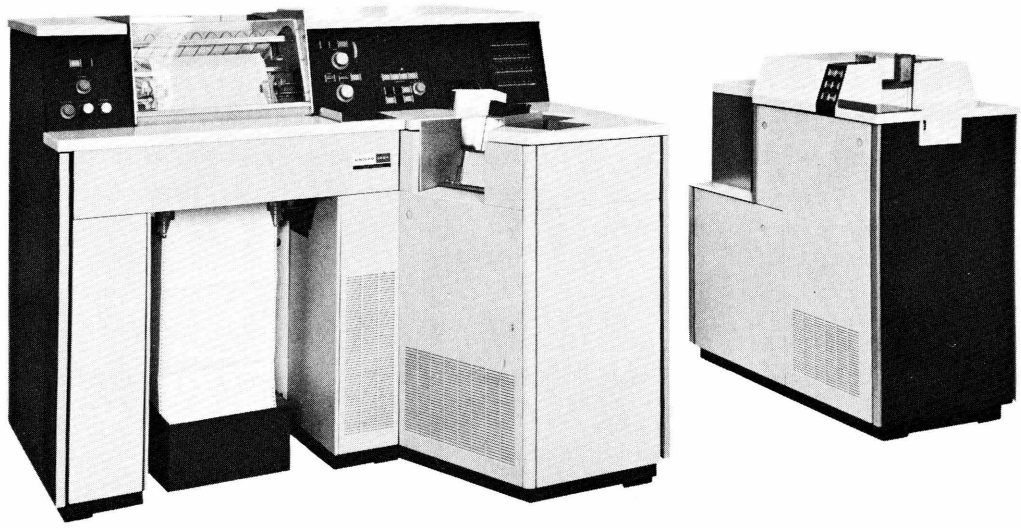
Without optional print buffer, the memory interlock I/O becomes

26.8 milliseconds for the Model III Processor

Simultaneity:

1. The buffered printer may run with all peripherals.
2. The unbuffered printer may run with the card reader, card punch and punched paper tape subsystem.

THE UNIVAC 1004 SUBSYSTEM



The UNIVAC 1004 Card Processor may serve as on line peripheral device for the UNIVAC 1050 System. This provides the user with a unique combination of data processing power. The UNIVAC 1004 subsystem may be utilized as an off line free standing card processor or as an on line card reader, card punch and printer.

Features:

1. Read cards at 400 to 615 cards/minute
2. Print 400 to 600 lines/minute
3. Punch cards at 200 cards/minute
4. Print line provides 132 character positions per line
5. Powerful plugboard instruction and 961 positions of core memory permit the UNIVAC 1004 subsystem to perform data validation, basic control computations, and data editing for the UNIVAC 1050.

Timing Factors:

The UNIVAC 1004 can deliver card images, and accept printer images and punch images as directed by the UNIVAC 1050 System. Its operation is fully buffered by its self-contained 961 positions of core memory. The operation of UNIVAC 1004 as a card reader, card punch and printer are considered in the following tables.

	Card Reader		Line Printer	
	400 cards/min		400 lines/min	
	Model III Processor	Model IV Processor	Model III Processor	Model IV Processor
Card or Printer cycle time (M.S.)	150	150	150	150
Memory interlock (M.S.)	.4	.16	.6	.26
Software execution (M. S.)	3.0	.78	3.0	.78
Time available to process (M. S.)	146.6	149.06	146.4	148.96
No. of avg. inst./card on line	1,466	5,733	1,464	5,729

	Card Punch	
	200 card/min	
Card cycle time	300	300
Memory interlock	.4	.16
Software execution	3.0	.78
Time available to process	296.6	299.06
No. of avg. inst/card	2,966	11,502

Simultaneity:

The UNIVAC 1004 Subsystem may run with all peripheral subsystems on the UNIVAC 1050 system with either the Model III or Model IV Processor.

THE UNIVAC 1050 TAPE SYSTEM

The UNIVAC 1050 System may be equipped with one of three tape subsystems. The UNISERVO IIIA tape subsystem provides high packing density and high transfer rates. The UNISERVO IVC tape subsystem is compatible with IBM tape systems and provides the user with a medium range of packing density and transfer speeds. The UNISERVO VIC is also IBM compatible. This tape subsystem provides a range of packing densities with a moderate transfer rate and at a much lower cost to the user.

The characteristics associated with each tape unit are displayed in the following table.

CHARACTERISTICS	UNISERVO IIIA	UNISERVO IVC	UNISERVO VIC
Data Transmission Rates	133,000 ch/sec 100,000 ch/sec	90,000 ch/sec 62,500 ch/sec 22,500 ch/sec	34,100 ch/sec 23,700 ch/sec 8,500 ch/sec
Tape Speed	100 in/sec	112.5 in/sec	42.7 in/sec
Space Between Blocks	0.75 inch	0.75 inch	0.75 inch
Operations:			
Read Forward	yes	yes	yes
Read Backward	yes	no	no
Write Forward	yes	yes	yes
Rewind Speed/Reel	125 seconds per 3500' reel	87 seconds per 2400' reel	180 seconds per 2400' reel
Overlap of Operation	R/C - W/C	R/C - W/C	R/W/C
Checking	read after write	read after write	read after write
Stop/Start time (milliseconds)			
Same Servo	13.2	14.2	24.0
Different Servos	7.8	10.2	24.0
Servo Units per Synchronizer	6	6	16
Tape Dimensions width	.5 inch	.5 inch	.5 inch
thickness	.001 inch	.0015 inch	.0015 inch
Reel Sizes	3,500 ft	2,400 ft.	2,400 ft
	1,800 ft		
	600 ft		
Reel change time (seconds)	30	30	30

UNISERVO IIIA

Timing Factors:

The timing factors for UNIVAC tape systems must be based upon the number of characters (N) contained in a block or record. The following formulas may be used to compute processing overlap by block.

Formulas:

A. Reading or writing involving continuous reference to the same servo unit.

Physical block time (M. S.) for 133 KC Density = 13. 2 + . 0075 N
Physical block time (M. S.) for 100 KC Density = 13. 2 + . 010 N

B. Reading or writing involving references to different servo units.

Physical block time (M. S.) for 133 KC Density = 7. 8 + . 0075 N
Physical block time (M. S.) for 100 KC Density = 7. 8 + . 010 N

C. Memory Interlock

Memory Interlock time (M. S.) - Model III Processor = . 0045 N
Memory Interlock time (M. S.) - Model IV Processor = . 002 N

N = No. of Characters/Block

Example

Assume 1200 character blocks being read and written from two different servo units.

For a single block (Read or Write) the following table shows processing overlap.

Read or Write a block	133,000 ch/sec		100,000 ch/sec	
	Model III	Model IV	Model III	Model IV
Physical block time (M.S.)	16.8	16.8	19.8	19.8
Memory interlock I/O (M.S.)	5.4	2.4	5.4	2.4
Software execution (M.S.)	7.5	1.9	7.5	1.9
Time available to process (M.S.)	3.9	12.5	6.9	15.5
No. of avg. inst./block	39	480	69	596

For the combined operation of reading a block and writing a block all factors double.

Read and Write a block	133,000 ch/sec		100,000 ch/sec	
	Model III	Model IV	Model III	Model IV
Combined physical block time (M.S.)	33.6	33.6	39.6	39.6
Combined memory interlock I/O (M.S.)	10.8	4.8	10.8	4.8
Combined software execution (M.S.)	15.0	3.8	15.0	3.8
Total process time (M.S.) available/block in and out	7.8	25.0	13.8	31.0
Total no. of avg. inst./thruput block	78	961	138	1192

Simultaneity:

1. The UNISERVO IIIA tape unit may run with the UNIVAC 1004, the punched paper tape systems and the buffered printer system when using the Model III Processor.

2. The UNISERVO IIIA tape unit may run with all peripherals except FASTRAND, UNISERVO IVC or other UNISERVO IIIA's when using the Model IV Processor.

UNISERVO IVC

Timing Factors:

The timing factors for UNIVAC IVC tape systems must be dependent upon the number of characters (N) contained in a block or record. The following may be used to compute processing overlap by block.

Formulas:

A. Reading or writing involving continuous reference to the same servo unit

X. Physical block time (M. S.) for 22.5 KC density = 14.2 + .045 N
Physical block time (M. S.) for 62.5 KC density = 14.2 + .016 N

B. Reading or writing involving different servo units

Physical block time (M. S.) for 22.5 KC density = 10.2 + .045 N
Physical block time (M. S.) for 62.5 KC density = 10.2 + .016 N

C. Memory Interlock

Memory Interlock time (M. S.) - Model III Processor = .0045 N
Memory Interlock time (M. S.) - Model IV Processor = .002 N

N = No. of characters/block

Example:

Assume 1200-character block being read and written from two different servo units.

For a single block (Read or Write) the following table shows process overlap.

Read or write a block	62,500 ch/sec		22,500 ch/sec	
	Model III	Model IV	Model III	Model IV
Physical block time (M.S.)	29.4	29.4	64.2	64.2
Memory interlock I/O (M.S.)	5.4	2.4	5.4	2.4
Software execution (M.S.)	7.5	1.9	7.5	1.9
Time available to process (M.S.)	16.5	25.1	51.3	59.9
No. of avg. inst./block	165	965	513	2304

For the combined operation of reading a block and writing it, all factors double.

Read and write a block	62,500 ch/sec		22,500 ch/sec	
	Model III	Model IV	Model III	Model IV
Combined physical block time (M.S.)	58.8	58.8	128.4	128.4
Combined memory interlock I/O (M.S.)	10.8	4.8	10.8	4.8
Combined software execution (M.S.)	15.0	3.8	15.0	3.8
Total process time (M.S.) available/block in and out	33.0	50.2	102.6	119.8
Total no. of avg. inst./throughput block	330	1,930	1,026	4,607

Simultaneity:

1. The UNISERVO IVC tape unit may run with the UNIVAC 1004, the punched paper tape systems, the communications subsystem and the buffered printer when using the Model III Processor.

2. The UNISERVO IVC tape unit may run with all peripheral subsystems except FASTRAND, UNISERVO IIIA and other UNISERVO IIIC's when using the Model IV Processor.

UNISERVO VIC

Timing Factors:

The timing factors for the UNIVAC VIC tape system must be based upon the number of characters (N) contained in a block or record. The following formulas may be used to compute processing overlap by block.

Formulas:

A. Reading or writing involving continuous reference to the same servo unit.

1. Physical block passing time (M. S.) for 34. 1 KC density = 24. 0 + . 029 N
2. Physical block passing time (M. S.) for 23. 7 KC density = 24. 0 + . 042 N
3. Physical block passing time (M. S.) for 8. 5 KC density = 24. 0 + . 117 N

B. Memory Interlock - I/O

1. Memory interlock time (M. S.) - Model III Processor = . 0045 N
2. Memory interlock time (M. S.) - Model IV Processor = . 002 N

N = No. of character/block

Example:

Assume a 1, 200 character block being read and written from two different servo units.

For a single block (Read or Write) the following table shows processor overlap.

Read or write a block	34,100 ch/sec		23,700 ch/ sec		8,500 ch/ sec	
	Model III	Model IV	Model III	Model IV	Model III	Model IV
Physical block passing time (M.S.)	58.8	58.8	74.4	74.4	164.4	164.4
Memory interlock I/O (M.S.)	5. 4	2. 4	5. 4	2. 4	5. 4	2. 4
Software execution (M.S.)	7. 5	1. 9	7. 5	1. 9	7. 5	1. 9
Time available to process block (M.S.)	45.9	54.5	61.5	70.1	151.5	160.1
Total no. of avg. inst./block	459	2,096	615	2,696	1,515	6,157

For the combined operation of reading a block and writing a block, the block passing time would be the same as shown above because of the Read/Write/Compute capabilities of the UNISERVO VIC. However, the memory interlock and the software execution time would double because there are Central Processor functions which must be executed for both read and write. The processor overlap of a combined read and write operation is shown in the following table.

Read and write a block	34,100 ch/sec		23,700 ch/sec		8,500 ch/sec	
	Model III	Model IV	Model III	Model IV	Model III	Model IV
Physical block time (read & write) (M.S.)	58.8	58.8	74.4	74.4	164.4	164.4
Memory interlock (read & write) (M.S.)	10.8	4.8	10.8	4.8	10.8	4.8
Software execution (read & write) (M.S.)	15.0	3.8	15.0	3.8	15.0	3.8
Time available to process (M.S.)	33.0	50.2	48.6	65.8	138.6	155.8
No. of avg. inst./throughput block	330	1,930	486	2,530	1,386	5,992

Simultaneity:

1. The UNISERVO VIC tape unit may run with the UNIVAC 1004, the communications subsystem and other UNISERVO VIC tape units when using the Model III Processor.

2. The UNISERVO VIC tape unit may run with all peripheral subsystems when using the Model IV Processor.

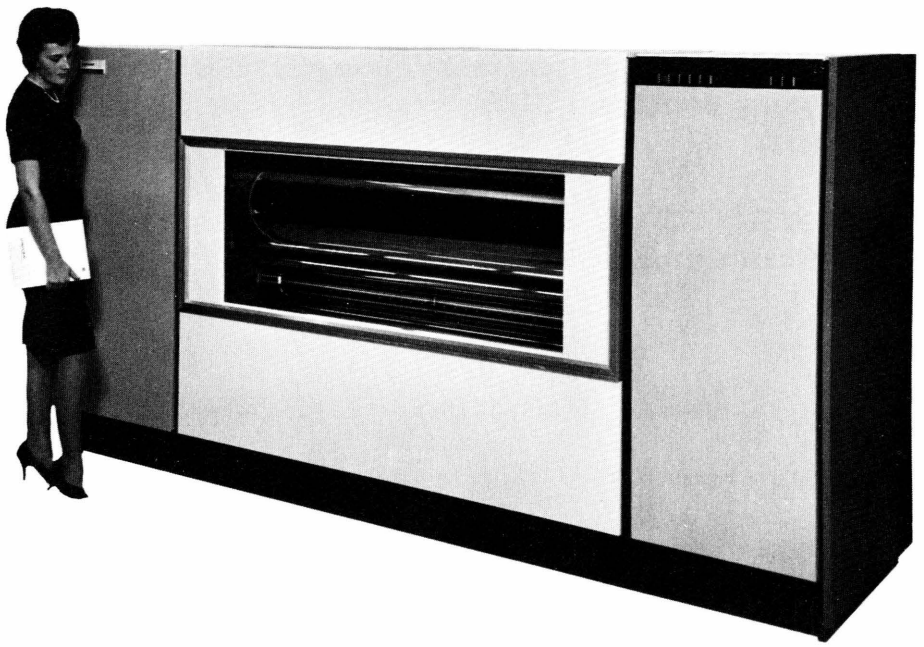
UNIVAC 1050 SYSTEMS – TAPE CAPACITY

Tape storage requirement:

The following table shows the number of records that may be written on a single reel of tape for various size records for the UNISERVO IIIA, UNISERVO IVC and UNISERVO VIC.

Record Size Characters	133 KC Recording 3500' Reel UNISERVO IIIA		62.5 KC Recording 2400' Reel UNISERVO IVC		35.7 KC Recording 2400' Reel UNISERVO VIC	
	No. of Records Thous.	No. of Char. Millions	No. of Records Thous.	No. of Char. Millions	No. of Records Thous.	No. of Char. Millions
80	51.8	4.14	32.3	2.58	33.8	2.71
200	46.6	9.33	25.9	5.18	28.8	5.76
400	40.0	16.00	19.5	7.83	23.0	9.21
600	35.0	21.00	15.7	9.44	19.2	11.52
800	31.1	24.88	13.1	10.52	16.4	13.16
1,000	28.0	28.00	11.2	11.29	14.4	14.40
1,200	25.4	30.54	9.8	11.87	12.8	15.36
1,400	23.3	32.66	8.8	12.32	11.5	16.12
1,600	21.5	34.46	7.9	12.68	10.4	16.75
1,800	20.0	36.00	7.2	12.98	9.6	17.28
2,000	18.6	37.33	6.6	13.24	8.8	17.72

THE UNIVAC 1050 FASTRAND Mass Storage Unit



The UNIVAC 1050 FASTRAND unit provides the user with 66 million characters of random access storage. Data is written or read from the FASTRAND unit in sectors that contain 168 characters. Several sectors can be written or read with one access. Sixty four read/write heads are attached to a common positioning mechanism. Each read/write head accesses any one of 96 tracks. Sixty four sectors are recorded around a single track. Therefore, one positioning of the read/write heads provides access to 64x64 or 4096 sectors. The addressing is sequential, making it possible to unload the FASTRAND unit with only 96 head positionings. A comprehensive system of parity and phase shift checking along with automatic address verifications assures the accuracy of the FASTRAND unit. Up to eight FASTRAND units may be attached to a single UNIVAC 1050 channel to provide a capacity of over 528 million characters.

Features:

1. Single unit capacity of 66, 050, 288 six-bit plus parity characters.
2. Average access time per sector 92 milliseconds
3. Data transfer rate (instantaneous/sector) 185, 000 char/second
4. Data transfer rate - Multiple sectors 153, 846 char/second
5. Variable key searching - 8, 16, or 32 character key (search for either 'equality' or 'equal to or greater than')
6. Head position time maximum (96 tracks) 86 milliseconds
7. Head position time minimum (1 track) 30 milliseconds
8. Rotational access time (full revolution) 70 milliseconds
9. Average rotational access (1/2 revolution) 35 milliseconds
10. Up to 8 units per UNIVAC 1050 channel to provide capacity of 528, 402, 304 characters.

Timing Factors

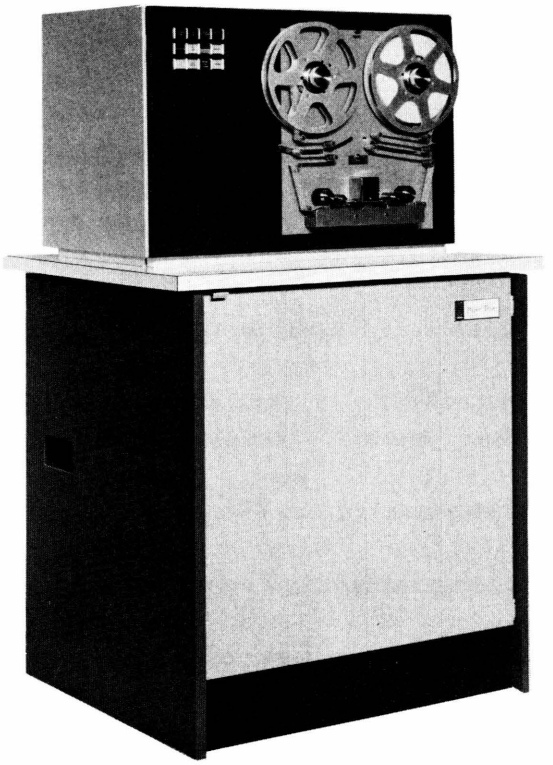
	Model III Processor	Model IV Processor
Average time to access and read or write a sector (M. S.)	93	93
I/O memory interlock (M.S.)	.9	.5
Software execution	2.5	.6
Available to processor (M. S.)	89.6	91.9
No. of avg. inst/access & read	896	3, 534

Simultaneity:

1. The FASTRAND unit may run with communications, punched paper tape, and the UNIVAC 1004 on line when using the Model III Processor.

2. The FASTRAND unit may run with all peripheral subsystems except the UNISERVO IIIA and UNISERVO IVC when using the Model IV Processor.

The UNIVAC 1050 Punched Paper Tape Subsystem



The UNIVAC 1050 System may utilize a punched paper tape subsystem. 5, 6, 7 and 8 level punched chad tape can be read and punched.

Features:

1. 1000 characters or 400 characters/second read speed

2. 110 characters/second punching speed

3. 5, 6, 7, 8 level punching

4. Chad tape 11/16, 7/8 or 1 inch in width

5. Start/Stop test equivalent to one word

6. Strip reading

7. Spool reading optional

Timing Factor:

The time required to complete a punched paper tape I/O function will be determined by the number of characters per block (N).

Block time at 1,000 characters/sec	= 1 X N
Block time at 400 " "	= 2.5 X N
Block time at 110 " "	= 9.1 X N
Memory Interlock time (M. S.) - Model III Processor	= .0045 N
Memory Interlock time (M. S.) - Model IV Processor	= .002 N

Timing table for 100 character block

	Read: 1000 char/sec		Read: 400 char/sec	
	Model III	Model IV	Model III	Model IV
Block read time M.S.	100	100	250	250
Memory interlock I/O M.S.	.45	.2	.45	.2
Software execution M.S.	2.0	.52	2.0	.52
Time available to process M.S.	97	99	247	249
No. of avg. instructions/block	970	3,807	2,470	9,576

UNIVAC 1050
STANDARD COMMUNICATION SUBSYSTEM

The UNIVAC Standard Communication Subsystem for the 1050 consists of three principal elements: Communication Line Terminals (CLTs), which establish direct connection with the communication facilities; Communication Multiplexers, which permit the simultaneous operation of up to 64

CLTs; and Communication Adapters, which control and synchronize all data transfers between the CLTs and the main frame of the 1050.

Communication Line Terminals (CLTs)

There are three basic kinds of input and output CLTs: low speed (up to 300 bits per second); medium speed (up to 1600 bits per second); and high speed (2000 to 4800 bits per second). Each is easily adjusted to the speed and other characteristics of the communications line with which it is to operate. These CLTs are used when data is transmitted to or from the UNIVAC 1050.

In addition to these CLTs, the Standard Communication Subsystem also provides a special output CLT which is not used for data transmission, the CLT-Dialing. This CLT is used to permit the Central Processor automatically to establish connections with remote points via the common carrier's switching network. Since the CLT-Dialing does not transmit data, it is always used in conjunction with an output CLT, an input CLT or, for two way communications, both.

Each CLT requires one position, either input or output, of the Communication Multiplexer.

a. Interface Modules

Modules are provided to interface CLTs with currently available modems in addition to telegraph facilities for which no modem is necessary. Where required, interface modules conform to EIA specifications. The modular concept of the Standard Communication Subsystem permits the addition of new interface modules as new offerings are made available by the common carriers. Jacks are provided on each telegraph interface module which permit a teletypewriter to monitor all data passing through the interface.

b. Clocks

All CLTs require a timing source to establish the proper sequencing of data bits or characters as they are transferred to and from the communication facilities. Medium speed parallel input CLTs, dialing CLTs, and high speed synchronous input and output CLTs use the modem or

dialing unit to which they are connected as their timing source, while all other CLTs use electronic clocks which are components of the Standard Communication Subsystem as their timing source.

Each asynchronous input CLT has its own clock; however, all asynchronous or parallel output CLTs which operate at the same speed share a common clock. Up to six output clocks are provided with the Subsystem.

c. Registers

Communication facilities usually operate in a bit serial, character serial mode in contrast to UNIVAC 1050 systems which handle data characters in a bit parallel, character serial mode. One of the principal functions of serial CLTs is to provide compatibility by performing a serial to parallel conversion for each input data character, or a parallel to serial conversion for each output data character. To accomplish this function, input CLTs are equipped with an assembly register in which each serial character, as it is received, (5, 6, 7 or 8 bits per character, depending on the code structure) is assembled into a complete parallel data character. Output CLTs are similarly equipped with a disassembly register.

When low speed CLTs are used, data must be transferred between the CLT and the Central Processor in the time interval between the arrival of the last data bit of one character and the start bit of the next character. Medium and high speed CLTs, however, contain a single character buffer or queuing register which permits a time interval corresponding to the length of a complete data character between data transfers.

INPUT COMMUNICATION LINE TERMINALS (CLT's)

	LOW SPEED		MEDIUM SPEED		HIGH SPEED
NAME	CLT51L	CLT81L	CLT81M	CLT81P	CLT81H
CODE	5 LEVEL	6,7, or 8 LEVEL	5,6,7, or 8 LEVEL	8 LEVEL	5,6,7, or 8 LEVEL
MODE	ASYNCHRONOUS	ASYNCHRONOUS	ASYNCHRONOUS	TIMING SIGNAL	SYNCHRONOUS
	BIT SERIAL	BIT SERIAL	BIT SERIAL	BIT PARALLEL	BIT SERIAL
SPEED	UP TO 300 bps	UP TO 300 bps	UP TO 1600 bps	UP TO 75 cps	2000-4800 bps

OUTPUT COMMUNICATION LINE TERMINALS (CLT's)

	LOW SPEED		MEDIUM SPEED		HIGH SPEED	DIALING
NAME	CLT50L	CLT80L	CLT80M	CLT80P	CLT80H	CLT DIALING
CODE	5 LEVEL	6,7, or 8 LEVEL	5,6,7, or 8 LEVEL	8 LEVEL	5,6,7, or 8 LEVEL	4 LEVEL
MODE	ASYNCHRONOUS	ASYNCHRONOUS	ASYNCHRONOUS	TIMING SIGNAL	SYNCHRONOUS	TIMING SIGNAL
	BIT SERIAL	BIT SERIAL	BIT SERIAL	BIT PARALLEL	BIT SERIAL	BIT PARALLEL
SPEED	UP TO 300 bps	UP TO 300 bps	UP TO 1600 bps	UP TO 75 cps	2000-4800 bps	VARIABLE

COMMUNICATION MULTIPLEXER

NAME	FUNCTION
C/M-4	Connects 2 input and 2 output CLT's to General Purpose Channel
C/M-8	Connects 4 input and 4 output CLT's to General Purpose Channel
C/M-16	Connects 8 input and 8 output CLT's to General Purpose Channel
C/M-32	Connects 16 input and 16 output CLT's to General Purpose Channel

Types of Communication Service Provided:

PRIVATE LINE TELETYPEWRITER PRIVATE LINE TELEPHONE

DIRECT DISTANCE DIALING (DDD) WIDE AREA TELEPHONE SERVICE (WATS)

TELETYPEWRITER EXCHANGE SERVICE (TWX)

Summary of Peripheral Simultaneity:

All peripheral operations provide a large amount of overlap between the reading or writing of the record and internal processing. In addition most peripheral devices provide for simultaneous operation with other peripheral devices. The following table shows the peripheral simultaneity.

Simultaneity of Operation for the UNIVAC 1050 System Utilizing the Model III Processor

	Card Reader	Card Punch	U 1004	Printer	FASTRAND	UNISERVO IIIA	UNISERVO IVC	UNISERVO VIC	Communications	Paper Tape	Computation	
Card Reader		x	x	x					x	x	x	
Card Punch	x		x	x					x	x	x	
U 1004	x	x		x	x	x	x	x	x	x	x	
Printer	x	x	x	x	x	x	x	x	x	x	x	
FASTRAND			x	x					x	x	x	
UNISERVO IIIA			x	x					x	x	x	
UNISERVO IVC			x	x					x	x	x	
UNISERVO VIC			x	x				x	x	x	x	
Communications	x	x	x	x	x	x	x	x	x	x	x	
Paper Tape	x	x	x	x	x	x	x	x	x		x	
Computation	x	x	x	x	x	x	x	x	x	x		

Simultaneity of Operation for the UNIVAC 1050 System Utilizing the Model IV Processor

	Card Reader	Card Punch	U 1004	Printer	FASTRAND	UNISERVO IIIA	UNISERVO IVC	UNISERVO VIC	Communications	Paper Tape	Computation	
Card Reader		x	x	x	x	x	x	x	x	x	x	
Card Punch	x		x	x	x	x	x	x	x	x	x	
U 1004	x	x		x	x	x	x	x	x	x	x	
Printer	x	x	x	x	x	x	x	x	x	x	x	
FASTRAND	x	x	x	x				x	x	x	x	
UNISERVO IIIA	x	x	x	x				x	x	x	x	
UNISERVO IVC	x	x	x	x				x	x	x	x	
UNISERVO VIC	x	x	x	x	x	x	x	x	x	x	x	
Communications	x	x	x	x	x	x	x	x	x	x	x	
Paper Tape	x	x	x	x	x	x	x	x	x		x	
Computation	x	x	x	x	x	x	x	x	x	x		

Concurrent Programs

The Coordinator (the UNIVAC 1050 executive system) provides for the concurrent operation of two separate programs within the UNIVAC 1050 Central Processor. The necessary linkage to the Coordinator is accomplished through the use of the Input/Output macros that are part of the PAL assembly system. The extremely high throughput capabilities of the Central Processor and the specially designed hardware functions included in the UNIVAC 1050 allow for concurrent processing of two programs. Thus, when one program is not using the full capability of the processor, processing of the second program occurs. Peripheral operations, such as card-to-tape, tape-to-print, etc. are logical choices for concurrent processing.

The following example illustrates the power of concurrent peripheral processing:

Sequential Operations		UNIVAC 1050 Concurrent Operations	
Operations	Time	Concurrent	Time
25,000 card-to-tape	38 minutes		
25,000 lines tape-to-print	28 minutes		
TOTAL	66 minutes	40 minutes	Total

This time saving of 40% can often be effected in day-to-day computer operations, minimizing scheduling problems and increasing the total work handled. No special programming knowledge or techniques must be used.

Software

Introduction

The software for the UNIVAC 1050 Systems has been designed to meet the exact requirements for each type of system; from the simple but powerful transition software required in the basic card and 1004 expansion series to the sophisticated software provided with the mass storage, tape, and real time series. All of the software has proven to be very easy to understand while providing powerful abilities to the user.

PAL Card Assembler

The Pal Card Assembler is an easy to learn and easy to use system. It contains a small set of assembler directives and data forms which are flexible and powerful.

The input of the PAL Card Assembler is a program punched on 80 or 90 column cards. The output of the PAL Card Assembler is an object program on 80 or 90 column cards with a printed side by side listing of the source and object coding.

A list of the PAL Card Assembler directives follows:

Directive		Use
BEGIN	-	Start of program
AREA	-	Definition of areas
-	-	Definition of fields within areas
EQU	-	Equality statements
ORIG	-	Program address adjustments
END	-	End of program
± (n)*	-	Data generation, constants

*(n) is the number of characters of data generation

The PAL Card Assembler is upward compatible with the PAL Tape Assembler.

Card Input-Output Specializer

The Card I/O Specializer produces a source deck of the reader, punch and/or printer control routines as specified by a call directive. The specialized output of this routine will be included with a programmer's source program before using the PAL Card Assembler. Using the Card I/O Specializer is the technique for generating the Input-Output routines for a 1050 card system.

The communication with these routines is identical to that of the PAL Tape Assembler generated routines described later in this manual.

PAL Tape Assembler

The PAL Tape Assembler is an extension of the PAL Card Assembly system. It maintains the simplicity of the Card Assembly system; however, it has the ability to handle the generation of powerful macros from a source program or a library.

The PAL Tape Assembler consists of a standard library of Input-Output routines, utility routines and diagnostic routines. The user also has the ability to add routines to this library. The PAL Tape Assembler employs the most up-to-date techniques in assembler design and power.

The Input of the Tape Assembler is a program punched on 80 or 90 column cards or on magnetic tape. The Output of the Assembler is an object program on 80 or 90 column cards or written on magnetic tape. A printed side by side listing of the source and object coding is also provided.

The PAL Tape Assembler Directives are the same as the PAL Card Assembler with the following additions:

Directive		Use
PROC	-	definition of a macro
NAME	-	alternate name of macro
DO	-	conditional or unconditional generation of coding
FORM	-	definition of the format in which data will be generated.

Coordinator

The Coordinator is a small but powerful executive routine for the UNIVAC 1050 system which controls the priority of operation of the on line peripherals. The Coordinator has the ability to run one program by itself or two programs concurrently; these programs may be independently written and can run individually, or together, or with other programs in a concurrent mode.

The Coordinator varies in size and ability according to the user's needs. Through the use of parameter cards, a Coordinator is generated by the PAL Assembler to control a variety of the following devices:

a) Reader, printer, and punch
b) UIIIA, IVC, and VIC tapes
c) FASTRAND mass storage units
d) Communications Subsystem
e) UNIVAC 1004 on line
f) Paper tape reader and punch
g) Single program operation or concurrent operations

The Coordinator also processes Class I and Class II interrupts, allocates memory, loads programs and releases memory when a program is completed.

Input/Output Routines

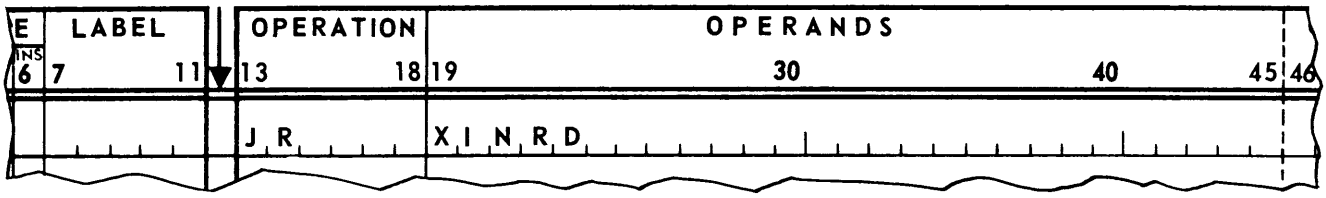
The peripheral units of the UNIVAC 1050 are controlled by input/output subroutines which may be called into a program during assembly using the PAL tape assembler or produced by the Card I/O Specializer for use with the PAL Card Assembler. These Input/Output Routines are designed to control the particular I/O units at their maximum rated speeds. All interrupt processing and the communication with the Coordinator are handled by these routines to simplify the control of the peripheral units by the programmer.

Card Reader Routine

This routine controls the operation of the card readers when reading in the translated or untranslated mode. The index register specified in the CALL directive is used to address the current card image area.

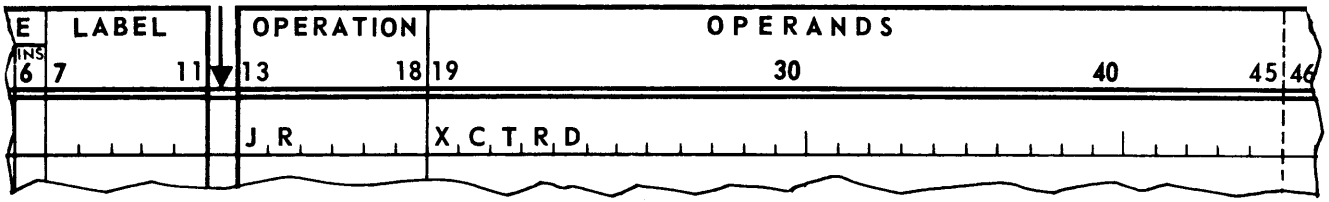
Initialization must be accessed before any read images are requested. The address of the first image is not supplied at this time.

Example of coding to initialize reader:



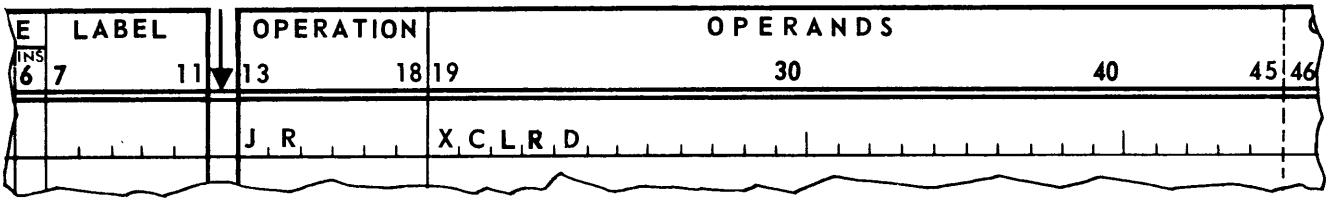
Execute is entered when the Worker Program wants a card image. The relative starting address of the currently available card image will be supplied to the Worker Program in the index register specified in the CALL directive. When this section is accessed, the routine assumes that the Worker Program no longer needs the previously supplied card image.

Example of coding to get card image:



At the conclusion of a run, the Worker Program must enter the closing section of the routine to feed a standard number of blank cards through the reader.

Example of coding to close reader:



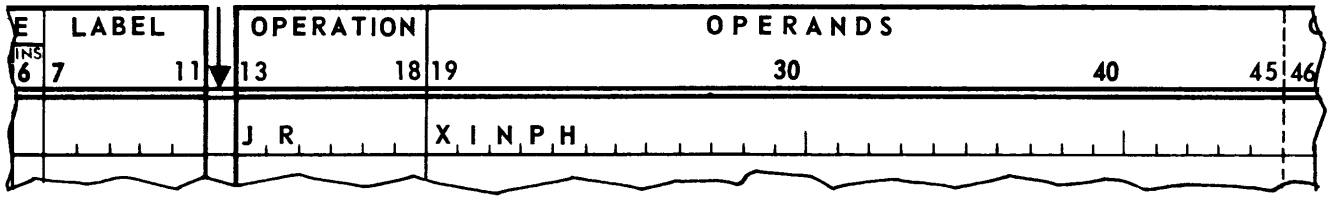
Card Punch Routine

This routine controls the operation of the punch when punching in the translated or untranslated mode. The index register specified will give the Worker Program the relative address of the current punch area.

Initialization must be referenced before any attempt to produce card

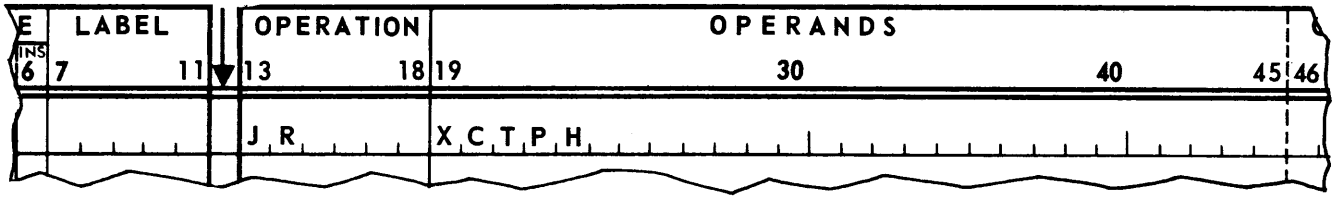
output. This section will clear the punch areas to blanks and provide the relative address of the punch area to the Worker Program.

Example of coding to initialize punch:



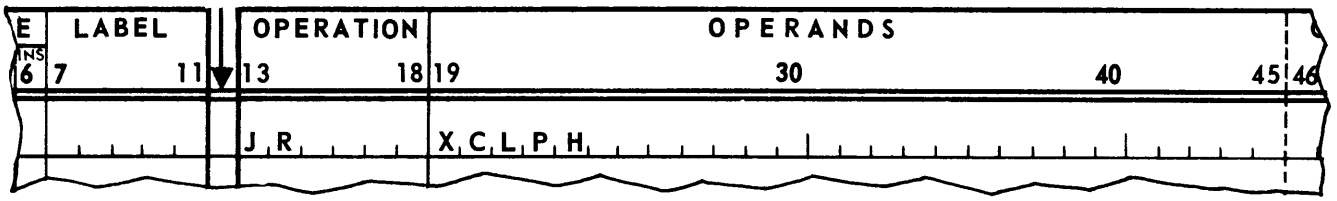
When a punch area is filled with data and is ready to be released for output, the Worker Program references the Execute section.

Example of coding to Punch Card:



At the conclusion of a run, the Worker Program must enter the closing section of the routine. This section will punch all remaining images provided and clear the punch unit of data cards.

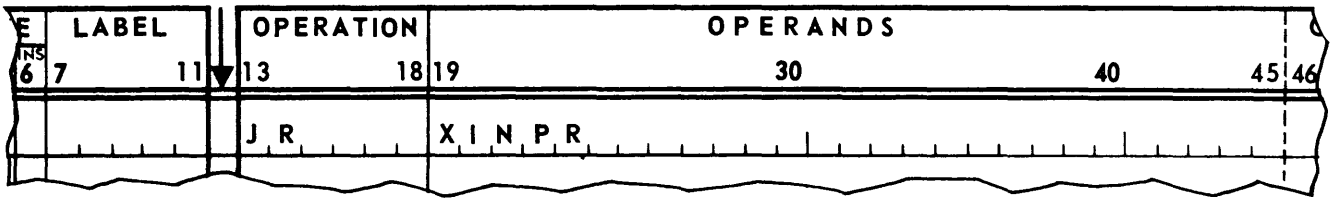
Example of coding to close punch:



Printer Routine

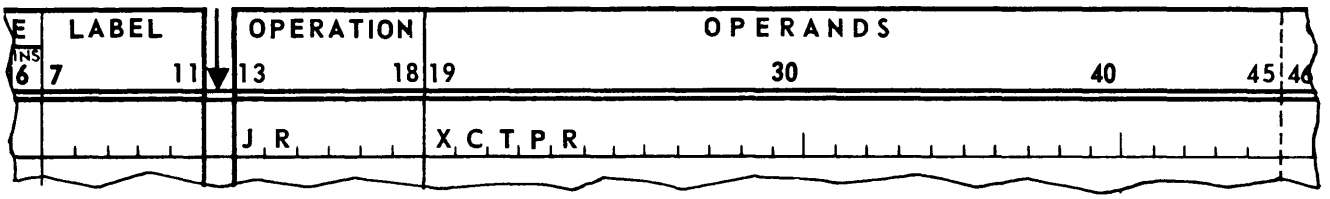
This routine controls the operation of the High Speed Printer. The index register specified is used to tell the Worker Program the relative address of the current print area. Initialization must be referenced before any attempt to produce printed output. This section clears the print areas to blanks and provides the Worker Program with the relative address of the first print area.

Example of coding to initialize printer:



The Execute section is entered when the Worker Program has filled a print area and is ready to release this area for printing.

Example of coding to print line:



Tape Handling Procedure

The handling of tape files is accomplished through the use of Input-Output macros. Basically there are 4 Input-Output macros:

1. OPEN

   Before using an input or output file, the file must be initialized through the use of this macro-instruction. OPEN causes the reading and checking or writing of the appropriate label blocks. The description of the files is included with the CALL for these tape routines.

2. GET

   The next input record to be processed is obtained through the use of this macro-instruction. This macro will result in the automatic reading of another block of records when necessary.

3. PUT

   The next output record to be written is delivered to the output file by the use of the macro. If more than one record is to be included in each output block, they are collected in an output area until enough records have been accumulated to make an output block, and then written on tape.

4. CLOSE

At the completion of a run involving tape output, the CLOSE macro-instruction must be executed. This instruction causes any partial blocks to be written, a sentinel block to be written, and the tape to be rewound if specified.

Macros controlling the 1004 on-line are similar to the control routine for the Reader, Printer and Punch units.

Macro instructions are also provided for FASTRAND and the paper tape read and punch systems.

An interface between the Coordinator and the Worker Program is provided for the Communications System. Because of the wide range of the types of remote devices available, the different methods of operation, and the different conventions employed within each installation, the communication control routine has been built to enable each user to satisfy his requirements with maximum flexibility. A priority control is also established between the Coordinator and the real time program to make for efficient real time processing.

SORT

The UNIVAC 1050 SORT uses the forward read poly-phase method, an extremely rapid and efficient method of tape sorting.

The user has the ability to generate a sort for a specific need by the use of parameter cards as input to the PAL Tape Assembler.

All sorts have a first pass section and a last pass section. The first pass section delivers items, one at a time, to the tournament of the dispersion routine. The final phase of the collation pass delivers sequenced items, one at a time, to the last pass section of the sort. Using this technique, the user can establish the peripheral units for the sort, as well as vary the first and last pass processing to suit his requirements.

The sort is designed to use a minimum of 8K of memory and 3 tape units. The item size for the sort may vary from 1 to 1024 characters. The volume of data can be up to a single reel of tape. The number of keys that the sort can handle varies from 1 to 10 with the length of the keys varying from 1 to 16 characters in length. Output from the sort can be in ascending or descending order.

The table below shows some estimated sort times with the following configuration:

a) U IIIA tapes
b) 16K memory Model III Processor
c) 80 character records
d) 10 character key

SERVOS	3	4	6
ITEMS			
10,000	9 min	7 min	7 min
20,000	18 min	15 min	14 min
50,000	49 min	38 min	36 min

Program load time of 1 minute is included.

For more detailed sort information, reference the UNIVAC 1050 System Sort Timing Procedure bulletin.

REGENT — UNIVAC 1050 REPORT GENERATOR

REGENT for the UNIVAC 1050 is designed to reduce the time and effort to prepare printed reports. The user describes the format of the files and the processing involved on the standard PAL coding form. The input file, summary item output file and detail lines of printing are each described in the same fashion by supplying to the generator the name of the field, the length of the field and the position of the field. Non-detail, headers, and constant lines of printing are described by supplying the generator position, spacing, and constant information.

Processing information is supplied to the generator in the form of statements which describe the processing desired. The acceptable types of statements are classed as follows:

Arithmetic Operations
Data Movement and Editing
Control
Input-Output

A list of the powerful REGENT verbs and directives is as follows:

ADD	LEV n	STOP
SUBTRACT	IFDEC	READ
MULTIPLY	IFALP	PUNCH
DIVIDE	IFCHR	PRINT
ROLL	IFDIG	BEGIN
RESET	IFZON	USE
ROUND	IFNEG	PAGE
SHIFT	XCUTE	CLOS
MOVE	ALTER	END
CLEAR	GOTO	

The processing information and the file description are then fed to REGENT, which produces an efficient ready to run object program. In addition, a listing of source input and coding generated by REGENT can also be obtained.

The generator also allows for the inclusion of specialized use code sections where they are required.

MARION - Source and Object Code Library Maintenance Routine

MARION is an integrated set of service routines providing the functions necessary to create and maintain card and tape libraries of source and object coding. It also may be used to maintain individual programs.

MARION has the ability to add runs, delete runs, replace runs, print runs, punch runs or alter runs of a library.

The PAL Tape Assembler is in MARION format and is maintained by MARION, which makes it possible for the user to add his own macro routines to the PAL Tape Assembler library.

MARION is controlled by parameter cards which are written in the PAL Assembler input format.

SOFTWARE CONFIGURATION CHART

UNIVAC 1050 SYSTEMS—SOFTWARE CONFIGURATOR

	ITEM	UNIVAC 1050-C					UNIVAC 1050-T						UNIVAC 1050-M[2] ALL OF C & T SOFTWARE PLUS	UNIVAC 1050-R[2] ALL OF C, T, M SOFTWARE PLUS	UNIVAC 1050-S							UNIVAC 1050-4	
	UNIVAC 1050 PROCESSOR	4K[3]	4K[3]	8K	8K	8K	8K	8K	8K	8K	8K	16K	12K REQUIRED	12K REQUIRED	8K	8K	8K	8K	8K	8K	8K	4K[3]	8K
EQUIPMENT	600 OR 800/900 CPM READER	1	1	1	1	1	1	1	1	1	1	1	REQUIRED	REQUIRED	1	1	1	1	1	1	1		1
	200 OR 300 CPM PUNCH	1	1	1	1	1	1	1	1	0	1	1			0	1	0	1	0	1	1		1
	600/750 OR 700/922 LPM PRINTER	1	1	1	1	1	1	1	1	1	1	1	REQUIRED	REQUIRED	1	1	1	1	2	2	1		1
	PRINT BUFFER (NOTE 4)		1		1	1	1	1	1	1	1	1	REQUIRED	REQUIRED	1	1	1	1	2	2	1		1
	PAPER TAPE READ/PUNCH UNIT					1					1										1		1
	1004 ON LINE																					1	1
	TAPE UNITS						1	2	3+	3+	3+	4+			1	1	2	2	2	2	2		3+
	MASS MEMORY												1 TO 8										
	COMMUNICATIONS													REQUIRED									
	SOFTWARE PROVIDED																						
ASSEMBLERS	PAL JR*	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓				✓		✓		✓	✓		✓
	PAL CARD*			✓	✓	✓	✓	✓	✓		✓	✓				✓		✓		✓	✓		✓
	PAL TAPE							✓	✓	✓	✓	✓						✓		✓	✓		✓
	PAL DRUM												✓										
	PAL 1004*																					✓	✓
	PATCH ASSEMBLER			✓	✓	✓	✓	✓	✓		✓	✓				✓		✓		✓	✓		✓
CONTROL ROUTINES	READER	✓	✓	✓*	✓*	✓*	✓	✓**	✓**	✓**	✓**	✓**				✓		✓**		✓**	✓**		✓**
	PUNCH	✓	✓	✓*	✓*	✓*	✓	✓**	✓**		✓**	✓**				✓		✓**		✓**	✓**		✓**
	PRINTER	✓	✓	✓*	✓*	✓*	✓	✓**	✓**	✓**	✓**	✓**				✓		✓**		✓**	✓**		✓**
	PAPER TAPE					✓					✓**										✓**		✓**
	1004 PERIPHERALS																					✓	✓**
	MAGNETIC TAPE FILES							✓**	✓**	✓**	✓**	✓**						✓**		✓**	✓**		✓**
	DRUM—MASS MEMORY												✓										
	MEMORY DUMP	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
OPERATING SYSTEM	COORDINATOR						✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓		✓
	LOADER	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
	TAPE CONTROL						✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓		✓
	DRUM CONTROL												✓										
	COMMUNICATIONS CONTROL													✓									
	LIBRARIAN							✓	✓	✓	✓	✓					✓	✓	✓		✓		✓
REPORT GENERATORS	REGENT—CARD			✓	✓	✓	✓	✓	✓		✓	✓				✓		✓		✓	✓		✓
	REGENT—TAPE							✓	✓	✓	✓	✓						✓		✓	✓		✓
	REGENT—DRUM												✓										
SORTS	DRUM—SORT												✓										
	TAPE—SORT								✓	✓[1]	✓	✓											✓
	TAPE—MERGE								✓	✓	✓	✓											✓
SATELLITE UTILITIES	CARD → TAPE														✓	✓	✓	✓	✓	✓	✓		
	TAPE → CARD															✓		✓		✓	✓		
	TAPE → PRINT														✓	✓	✓	✓	✓	✓	✓		
COMPILERS	COBOL											✓											
	FORTRAN											✓											

*SPECIALIZER I/O CONTROL **OFF LIBRARY TAPE [1]4—6 TAPES REQUIRED [2]DEPENDING ON CONFIGURATION OF C, T OR M SYSTEMS [3]8K REQUIRED WITH MODEL IV

[4]OPTIONAL FOR 600/750 LMP PRINTER ONLY WITH 600 CPM READER ON 1050-C SYSTEMS

USING THE UNIVAC 1050 SYSTEMS - SOFTWARE CONFIGURATOR

The Configurator shows the complete range of software to be operational for UNIVAC 1050 Systems. It also shows how systems may be built up so far as hardware is concerned. Reference to these notes and the Configurator should answer the questions which might occur.

These ground rules apply to all Univac 1050 Systems:

1. 80 and 90 column card peripherals are not to be mixed on one system.

2. Minimum memory sizes as specified in the Configurator must be used. The Model III Processor is basically 4K, with 4K modules. The Model IV Processor is basically 8K, with 8K modules.

3. Sufficient I/O channels must be provided to match the hardware configuration.

   Card reader, printer, punch, FASTRAND, paper tape unit, and the Standard Communications Subsystem each take one channel. Each magnetic tape subsystem takes two channels.

4. Any configuration that does not meet these rules requires home office approval and may require an RPQ.

5. The Power B unit is required whenever there are two or more subsystems included beyond the C-Series.

C-SERIES

1. All require reader, punch and printers.

2. The print buffer is required whenever the 700/922 LPM printer and/or the 800/900 CPM reader is specified, and on all T, M, R, and S Series Systems.

T-SERIES

1. Only one type of tape subsystem is allowable per system; i.e. Uniservo IIIA, or Uniservo IVC, or Uniservo VIC.

2. The Uniservo VIC subsystem requires a minimum of two servos.

M-SERIES

1. Minimum memory with the M-Series is 12K with Processor III and 16K with Processor IV.

R-SERIES

1. A console typewriter must be provided as the first position on the SCS. Minimum memory per the M-Series.

S-SERIES

1. This series may have a Uniservo IIIA subsystem and a Uniservo IVC or Uniservo VIC subsystem, but a minimum of two uniservos must be provided on either subsystem. All such systems are irregular and require home office approval.

1004 Expansion System

1. Note that 8K minimum is required when other than the 1004 is used as a peripheral.

Summary

UNIVAC 1050 Systems - Summary

This manual has presented a review of UNIVAC 1050 Systems, including hardware, software and timing information. The following is a summary of the information presented.

UNIVAC 1050 Systems - Hardware

The design philosophy of the Central Processor, available with all UNIVAC 1050 Systems, enables the user to select from a wide range of data processing capabilities to solve the specific data processing requirement. The interrupt network and buffering overlap provided by the Central Processor gives each UNIVAC 1050 user maximum throughput capabilities for the system selected.

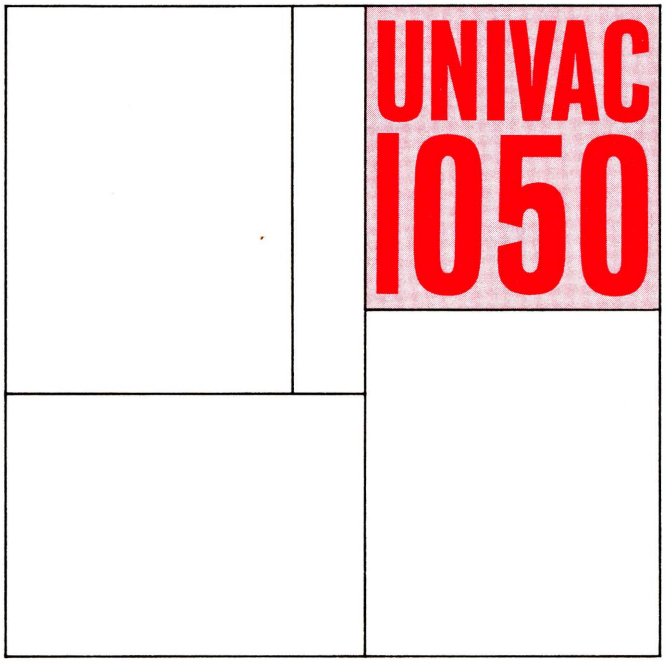
UNIVAC 1050 Systems - Software

The design philosophy of the software provided with UNIVAC 1050 Systems gives each UNIVAC 1050 System user software which is a balance between ease of learning and effectiveness of performance. A full range of assemblers, compilers, utility routines, report generators and satellite software is available with UNIVAC 1050 Systems.

UNIVAC 1050 Systems - Timing

The ability to select a Central Processor and related or matched Input-Output speeds provides the user with the maximum data throughput for the application requirement. Maximum performance from each peripheral device is possible because of the channel, interrupt, and buffering philosophy of the UNIVAC 1050 Central Processor.

UNIVAC 1050 SYSTEMS ARE A "CATALOG OF COMPUTING POWER" FROM WHICH THE USER CAN SELECT THE EXACT DATA PROCESSING SYSTEM FOR THE APPLICATION OR SYSTEM NEED.



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