OPR EXECUTIVE ROUTINE FASTRAND HANDLER SUPPLEMENT

1.0 CONTENTS

2.0 THE EXECUTIVE FASTRAND HANDLER

FASTRAND file control routines will be available at a future date. The following is a description for those users who wish to write their own routine.

2.1 ASSEMBLY

Parameter 6 (see Executive Routine - OPR, UP 3940.14) enables the user to assemble an Executive Routine that contains the FASTRAND Handler. If p_6 is F, the modification will be included and will function according to the following description.

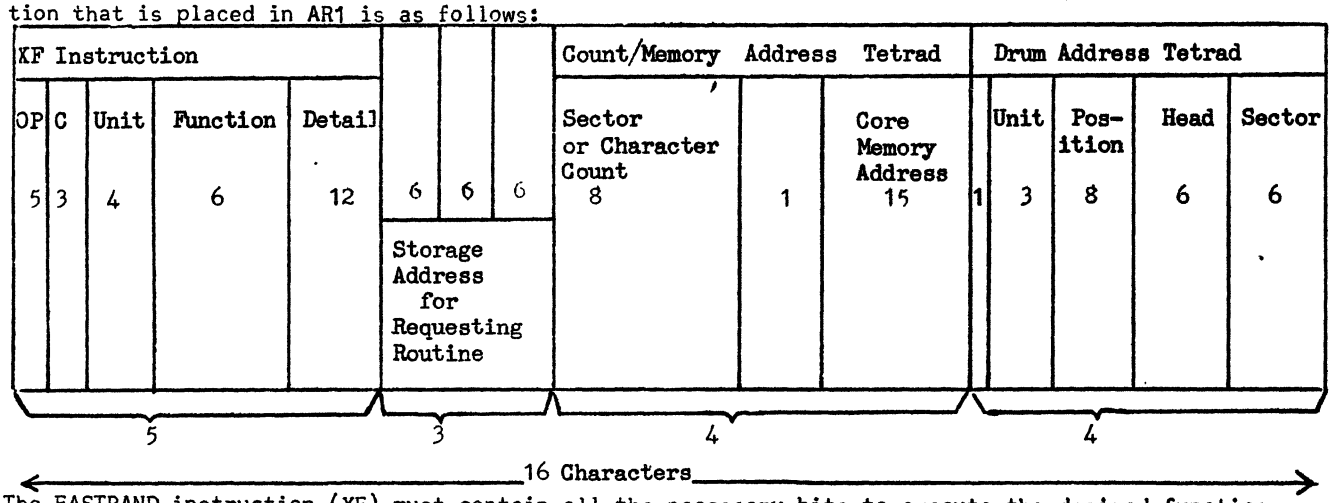
2.2 INITIALIZATION

Before using the FASTRAND Handler to issue any orders, the following lines must be executed:

LABEL	OPERATION	OPERANDS
	FT	1,7
	JR	0666

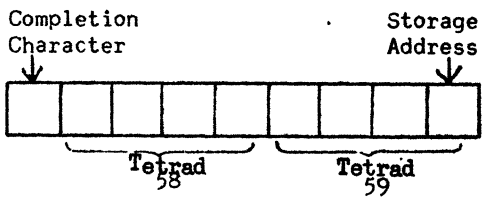
2.3 ISSUING THE ORDER

When the user wishes to issue a FASTRAND order, he must execute a JR 0750 with the FASTRAND order and associated parameters already placed in AR1. The format of the 16 character packet of information that is placed in AR1 is as follows:



The FASTRAND instruction (XF) must contain all the necessary bits to execute the desired function. The field marked Count/Memory Address Tetrad will be transferred to Tetrad 56. The field marked Drum Address Tetrad will be transferred to Tetrad 57.

The address that must appear as the "storage address" must be the right-hand address of a 9 character control field in the users program. The handler will store pertinent information, concerning the status of the order, into that field. The character at storage address minus eight (known as the completion status character) should be preset to binary 0. At the completion of the order the handler will move Tetrads 58 and 59 to the storage address as indicated.



As long as the completion character remains at 0, the user knows his order has not been finished, and must give up control to OPR (see Section 3.0).

The possible values of this character are

0 in process
1 successful completion
2 error - see below
3 unsuccessful search
4 error - see below

2.4 ERROR CONDITION INTERRUPTS

In some cases, when programmed recovery of an error condition is impossible, the computer will be brought to a display stop (JC...48). The 16 bits of the display have the following format:

Bit Positions					
16	15-13	12	11	10-7	6-1
1	Channel 110	0	0	Unit	Error Code

The following action is taken for each specific error condition:

2.4.1 Record Memory Error

The order causing the error will be reissued. Before reissuing the order, the bit designating head bar positioning will be inserted into the XF order. The order will be reissued 2 times with the head bar positioning bit. If the order is still unsuccessful after the 2nd issue, a two will be inserted into the completion character. The order will be peeled off the list of XF instructions. Tetrads 58 and 59 are stored in the storage address for the requesting routine and control is returned to the requesting routine.

Modular FASTRAND utilizes a different drum addressing scheme. This makes possible the occurrence of a condition where a Record Memory Error indication being received is in fact the equivalent of a Head Count Overflow in FASTRAND I or II.

Should this occur, a position bit will be inserted and the order reissued two times. It will not be successfully completed and the using program will be informed of a Record Memory Error. A Head Count Overflow indication is also possible on Modular FASTRAND. Further program action upon the above occurrence remains the using program's responsibility.

2.4.2 Drum Longitudinal Parity Error

The order will be reissued 2 times. If the order is still unsuccessful after the 2nd issue, a two will be inserted into the completion character. The order will be peeled off the list of XF instructions. Tetrads 58 and 59 are stored in the storage address for the requesting routine, and control is returned to the requesting routine.

2.4.3 First Phase Shift Error

Same as above

2.4.4 Second Phase Shift Error

Same as above

2.4.5 Missing Sector Error

Same as above if

1. the order was not a search; or
2. if it was a search and the return memory address was equal to the initial memory address; or

3. if it was a search and the return memory address was $\geq$ to the initial memory address +64.

If none of the above conditions existed and it was a search, it was an unsuccessful search. In this case a three will be inserted into the completion character. Tetrads 58 and 59 are stored in the storage address for the requesting routine.

2.4.6 Memory (Core) Parity Error

A display stop with an error code of 55 will occur. If the operator depresses the PROGRAM START button, control will be passed to a path that will temporarily bypass the worker program with an error.

2.4.7 Non-Ready

A display stop with an error code of 77 will occur. If the operator depresses the PROGRAM START button, the worker program will be bypassed with an error.

2.4.8 Memory Overload Anticipated or Busy

The instruction will be reissued and control will be returned to the interrupted program.

2.4.9 Head Count Overflow

The order will be peeled off the list of XF orders. A 4 will be inserted into the completion character. Tetrads 58 and 59 will be inserted into the storage address for the requesting routine, and control is returned to the requesting routine.

2.4.10 Locked Out Write

Some FASTRAND Systems will be delivered with the ability to have portions of the drum locked out (inhibit write). If a write is attempted in this area, an error indication will be given. A display stop with an error code of 33 will occur. If the operator depresses the PROGRAM START button, the worker program will be bypassed with an error.

The hardware indication of this occurrence is a Record Memory Error set in conjunction with Head Count Overflow.

3.0 SAMPLE CODING

An example of the necessary instructions to issue an order and to test for completion follows. Assume the following lines appear in the users constant area and will be used to specify the order:

LABEL	OP	OPERANDS	
	XF	05,0,0,6	FASTRAND order, position read
	+3	COMPL	Completion storage address
	+4	INSEC+00200000	Input area and sector count
FROR	+4	0	Starting drum address
	+8	0	
COMPL	+1	0	9 character control field

The coding to issue the order and test for completion follows:

	PD	COMPL-8,1	Completion status character
	BA1	FROR,16	Bring order to AR1
	JR	0750	Execute FASTRAND issue
TEST	JC	$+5,26	Inhibit Interrupt
	CC	COMPL-8,0	
	JS	DONE	Test for completion
	LS	0526,04	Set 4 bit channel status list
	JR	0724	Go to OPR
	J	TEST	Go to test completion
DONE	J	$+5,27	Allow interrupt
	CC	COMPL-8,01	Successful test
	JU	ERROR	Error routine
	J	MAIN	