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CIRCUIT DESIGN FOR THE NEW ILLINOIS COMPUTER

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1. GENERAL DESIGN PHILOSOPHY

1.1 Introduction

The aim of all computer designers is to produce a machine which is simultaneously:

1. Fast,
2. Reliable,
3. Simple,
4. Easy to maintain,
5. Satisfies certain boundary conditions of an a priori nature.

It is, practically speaking, very difficult to ascertain which direction to take in investigating circuits, since all the factors in the list above are strongly interdependent and since each item, taken separately, has several connotations. For example "fast" is only a useful feature if the speed is not bought by a lack of reliability and "simple", all by itself, can either mean simplicity of layout or also low cost: there may be a contradiction between the latter two.

In order to simplify the problem of designing circuits for a new machine, it is mandatory to make a certain number of a priori decisions about their nature. First of all the past experience of the design group usually dictates a certain approach. This is what is meant by item 5 in the list above. In the case of the new Illinois computer this means that the circuits must be:

1. Capable of asynchronous operation, more specifically they must be direct coupled and use 2 level dc-representation.
2. Make use of a given type of hardware, i.e. Western Electric GF-45011 transistors and Transitron S577G diodes.
3. Use emitter-follower-diode logic with non-saturating (bumped) switching amplifiers only when voltage-level restoration becomes necessary.

4. Use whenever possible constant current supplies in both emitters and collectors.

All these points will be discussed in separate sections later on.

It should also be mentioned that there is a strong interaction between the overall layout of the machine and the circuitry best suited to implement it. If, for instance, separate carry storage and a base 4 system are used, fast multiplication dictates the use of a special "integrated design" for the adder stages instead of the use of an assembly of standard basic circuits. Indeed the choice of what are called basic circuits is highly dependent on a rather detailed knowledge of the logical design of the fast parts of the machine (AU, etc.) and reciprocally the logical design can only be efficient if the designer interacts continuously with the circuit engineer. It is this close relationship between logical design and circuit design which makes it useless to list "logical design" in the boundary conditions mentioned above. As will be noted later on, the set of basic circuits is rather extensive in order to obtain the flexibility required in a fast machine; this does not mean that no standardizing effort has been made. Indeed (except for some very special applications) all basic circuits have standardized inputs and outputs and can be used in very big "erector set" assemblies.

A final remark may not be out of place. Hardware specifications (e.g. transistor α's, base-emitter reverse ratings, power ratings, resistor tolerances, power supply tolerances, etc.) have been assumed fixed in our discussion. This is obviously an idealization. Especially in the case of the new Illinois computer circuits there was a considerable effort made by certain firms to produce hardware meeting the Laboratory's specifications and conversely circuit design could be readjusted and improved several times as parameters of diodes and transistors became better. The question of when to freeze the design is, of course, quite difficult to decide. In general the answer is: when (maintaining good standards of reliability) a certain average speed of operation of the circuits has been attained, this average speed being that required in order to meet the multiplication and addition speed specifications desired.

1.2 Specific Design Aims

Speedwise the project calls for a multiplication time t_m of less than 4 μs. Using a base 4 system with separate carry storage and multiplier recoding, it can be shown that for n bits and two adders

$$t_m = n[\frac{t_s}{2} + \frac{t_a}{3}] + t_{ass} .$$

Neglecting the addition time t_a before the shift time t_s and also the carry assimilation time t_{ass}, we have

$$t_s = \frac{2t_m}{n} .$$

For $t_m = 2$ μs, $n = 52$ we obtain $t_s \cong 80$ mμs. Since

$$t_s = t_d + 2t_r + t_{ff} + t_c$$

where

t_d = driver delay time

t_r = driver rise or fall time

t_{ff} = flipflop setting time

t_c = control time

and since (see Sections 2.5 and 3.4) one has approximately

$$t_d = \tau , \; t_r = \tau , \; t_{ff} = 2\tau , \; t_c = \tau ,$$

where τ is the rise-time of the circuits,

$$t_s = 6\tau$$

meaning that τ must be somewhat less that 15 mμs. This, then fixes the class of transistors and diodes to be used as well as many questions of mechanical layout.

As regards reliability, predictions about a new type of semiconductor device are rather uncertain. The overall aim was to design a machine not only one hundred times faster than ILLIAC but also one hundred times more reliable per operation: the average time between breakdowns would then be the same. Since the new Illinois computer has 15,000 transistors as compared to 5,000 (double-) triodes in ILLIAC (with its drum), the average lifetime per unit (transistor or double-triode) must be three times higher in the new Illinois computer. With

preventive maintenance ILLIAC gives 10,000 hours/unit, the new Illinois computer must therefore have 30,000 hours/unit. Whether and how this goal can be attained will be discussed in Section 3.1.

Simplicity is harder yet to discuss in terms of specific requirements. It was definitely not planned to make the new Illinois computer particularly cheap; it was rather thought that simplicity would be interpreted as meaning a certain elegance and efficiency of both the overall layout and the individual circuits, the limitation being solely that of remaining "reasonable" costwise. Since reliability decreases with the number N of transistors used for a particular subunit, an operation which necessitates $\Theta(N)$ of faultless time in reality demands

$$\Theta'(N) = \Theta(N)\left[1 + \frac{NL}{T}\right]$$

where

T = average lifetime of transistors

L = time to correct a breakdown (supposed $\sim$ independent of N) .

Usually the cost C of the subunit is proportionate to N

$$C = \lambda N$$

where λ is the cost per active unit ($\neq$ from the cost of this unit). Assuming that the replacement cost is also λ the cost γ per operation actually performed becomes

$$\gamma = \frac{\lambda N \Theta(N)}{T}\left(1 + \frac{NL}{T}\right)$$

and the goal should be to minimize γ.

The ease of maintenance (once circuits of a given reliability have been designed) is a function of:

1. The facilities for marginal checking.
2. The ease of fault location.
3. The ease of replacement of a faulty unit.

In the new Illinois computer it is contemplated to split up the (highly iterative) arithmetic unit into plugable units of about 200 transistors each. Such a unit is large enough to virtually eliminate the problems caused by plug-capacitances since it can be chosen to contain circuits which have to be elec-

trically close together. On the other hand it is small enough to allow the use of individual marginal checking for fault location and can be replaced as a whole.

It should be noted that the maintenance philosophy in the control section is different. Here we do not have a highly iterative structure and the successful replacement of a part cannot be ascertained without using the computer (control) as a test bed. The use of plug-in units is therefore not mandatory. In order to simplify fault location special pains are taken to make this part "speed independent", i.e. truly asynchronous (see Section 1.3).

Since the discussion of point 5 in the preceding section will have to be more detailed, separate sections will be devoted to each a priori boundary condition.

1.3 Synchronism, Asynchronism and Speed Independence

Computer circuits are classified according to the type of control-sequencing used.

In a synchronous machine the elementary operations (shifting, adding, etc.) occur at fixed time intervals, the moment of occurrence being controlled by a central clock.

All that is really specified by "asynchronism" is the absence of this central clock. Operations may then be timed by delay elements (for instance in the form of a "model" of the circuits to be controlled), i.e. really local clocks which can be stopped and started: a timing device for operation 1 gives an "end-signal" which starts the timing device for operation 2, this timing device gives an end signal in turn, etc. Of course, checking devices may be incorporated which hold up the transmission of end signals if the operation has not been satisfactorily performed.

A type of asynchronous operation in which the delay elements are the actual information circuits themselves is called "speed independence": in this type of circuitry information can only flow when all previous elements in the chain producing the operation have reacted to it. This system has the great advantage of being self-checking because in case of failure it stops after the last correct operation: this is useful in control design. The design of the

actual circuits used in speed independence differs little from that for any asynchronous system — it is the mode of interconnection which determines the existence or non-existence of speed independence. In some cases the design procedures can be simplified by using special logical elements and so-called "last moving points" (see Section 4.1). It should, incidentally, be pointed out that speed independence by no means precludes paralleling of operations.

The absence of a clock or delay elements in speed independence has to be paid for in terms of complexity. For the new Illinois computer it is therefore proposed to make the control only speed independent, while the arithmetic unit will be asynchronous in the sense discussed above, i.e. its action times will be imitated by models inside the control. These models must be chosen in such a fashion that the 3 mμs/meter signal delays in going from control to the parts of the arithmetic unit are included.

1.4 Two-Level Dc-Representation

Once asynchronism is desired, it becomes quite involved to use ac coupling (and the then rather natural representation of signals by the absence or presence of a pulse at given times).

The Digital Computer Laboratory has followed the Institute for Advanced Study by working with dc-coupled circuits because asynchronous operation more or less dictates their use and because it is believed that circuits of this type have inherent advantages as regards reliability and serviceability: a given combination of dc-inputs to a logical element always corresponds to a predetermined combination of dc-outputs. These circuits may possibly require more engineering effort and more hardware, but the relative increase seems negligible.

Dc-coupling does not necessarily imply the use of a two-level dc-representation, but this representation seems to be the natural complement of dc-coupling. In this representation the binary states 0 and 1 correspond to predetermined voltage or current levels, or to be more precise, to voltage or current bands: in magnetic recording this would be called a "non-return-to-zero" system.

The often alleged superiority in speed of the two-level dc-representation, based on the fact that only <u>one</u> change (or its absence) transmits information instead of an up and down sequence, is based on an erroneous assumption: that of

comparable rise-times. In reality the duty cycle of an active element in a pulse representation cannot exceed 50%, the maximum power it can switch is therefore twice as big, giving twice the amount of current and half the rise-times. Speedwise, therefore, the pulse and dc systems are equivalent.

1.5 Transistors Vs. Tubes

Although the choice of transistors and diodes in preference to vacuum tubes is so generally accepted that no discussion seems to be needed, a few remarks about the logical reasons for this choice may not seem out of place.

The first consideration is the switching sensitivity of a transistor ($\sim$ .5v) compared to that of a tube (grid-base $\sim$ 5v). All signal swings can therefore be scaled down in the ratio 10:1. Since currents are of the same order of magnitude in both transistors and tubes ($\sim$ 10 ma) the times involved in charging and discharging (equivalent) capacitances are scaled down by 10. Furthermore the powers involved are also scaled down by 10. This does not imply by any means that fast transistor circuits should use low-powered transistors: for a given saturation margin δ (see Section 2.3) maximum currents i are proportional to the maximum power P and for a given circuit capacitance C the time t to change from state 0 to state 1 different by ΔV is

$$t = \frac{\delta C \Delta V}{P} .$$

Of course the actual transit time in the active element is also important. In the case of a transistor which is not in saturation the transit time is approximately the reciprocal of the 3 db-down-α-cutoff frequency. In a tube it is the transit time of electrons from grid to plate. For modern designs both these quantities are of the order of 2 μs. No decision can be made on this basis.

The elimination of saturation, which is mandatory for high-speed operation, requires the addition of some circuitry for bumping purposes. Furthermore, the input currents into a transistor which is "on" (emitter current divided by $(1-\alpha)$) are rather large for currently available α's and an emitter follower is necessary after practically every dc-stepdown network. This, together with bumping diodes to restandardize signals, makes for a somewhat great-

er complexity of the (non-saturating) transistor logical elements as compared to those using tubes.

The packing density of transistor circuits is perhaps somewhat higher than that of tube circuits, but it should be pointed out that the great temperature sensitivity of semiconductors imposes severe conditions on the power dissipated per unit volume. On the average it seems that lead lengths are not much shorter than in a miniaturized tube layout.

When discussing the influence of noise, it must be realized that the impedance level of transistor circuits is 10% of that of tube circuits: capacitive coupling is less important while inductive coupling becomes increasingly important. It seems, however, acceptable to assume that the capacitive interaction is still the major source of noise besides the direct interaction noise due to common power supplies; thermal and shot noise can be neglected in both tube and transistor switching circuits (see Section 3.5). The ratio noise power/switched power seems to be almost identical for both designs, since the decrease of voltage swings decreases the interaction noise by the same factor and the decreased impedance appears both in the numerator and the denominator.

The actual design parameters of the transistor (Western Electric GF-45011) and diodes (Transitron S577G) will be discussed in Section 7.1.

1.6 Emitter-Follower-Diode Logic with Non-Saturating Switching Amplifiers

It will be established later on that the operation time (see Section 2.5) of an emitter follower is less than 20% of that of the fastest voltage amplifier. Since a chain of diode logical elements attenuates both voltage and current swings, it is necessary to insert both current and voltage amplifiers.

The main idea in emitter-follower-diode logic is to precede each and every diode logic stage (i.e. AND diode combination or OR diode combination) by a current amplifier in the form of an emitter follower. The problem of current attenuation is then eliminated and it becomes even possible to guarantee at each output a minimum fan-out (FO = 3 after ANDs and ORs in the new Illinois computer). The addition of this input emitter follower, as was indicated above, costs very little in time. The problem of output voltages drifting outside their allowed bands is, however, in no way alleviated by this expedient — but it is not made worse either.

The remaining problem is then to restandardize voltages after a given number of cascaded emitter-follower diode stages. How many can be cascaded depends on:

1) The guaranteed minimum output swing of the last voltage amplifier.

2) The possible maximum required input swing of the next voltage amplifier.

3) The possible drift (positive or negative) in voltage between the input and the output of ANDs and ORs.

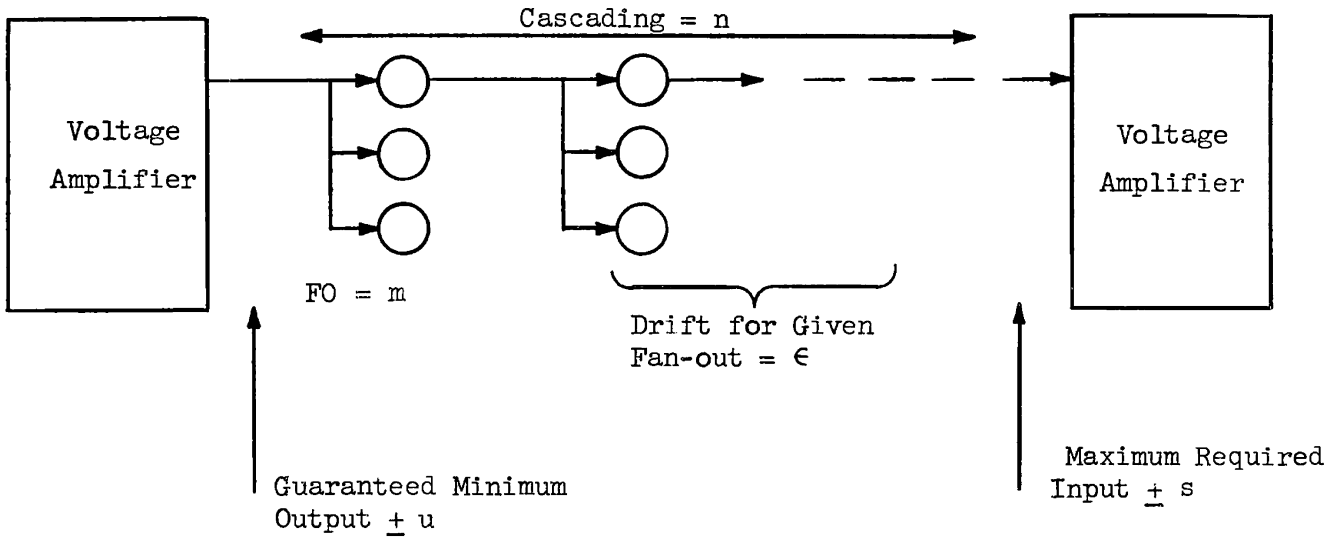


Figure 1
Fan-out and Cascading of Logical Elements

The guaranteed minimum output swing is indirectly determined by the hardware tolerances and the emitter-base reverse rating of transistors (see Section 2.2). The latter specifies the largest voltage U one can apply in the reverse direction to an emitter-base junction. Supposing that swings are symmetric (this gives the maximum amount of drift leeway when the end of a chain

of ANDs and ORs drives a switching amplifier) , this fixes the allowed maximum output swing $\pm$ U of the voltage amplifier. Using resistors, transistors and power supplies of given drift characteristics, $\pm$ U fixes the guaranteed minimum swing $\pm$ u. In the new Illinois computer, U = 3.2v, u = 2.5v.

In order to reduce the possible maximum required input swing $\pm$ s of a voltage amplifier, the design uses a switching stage. As will be shown in Section 2.4 such an input never requires more than s = .6v even under dynamic conditions.

Finally the absolute value of the drift across an AND or OR $-\epsilon-$ is a well known function of the FO,m, of each AND or OR, i.e. $\epsilon = \epsilon(m)$. For m = 3 the new Illinois computer circuits give $\epsilon < .3v$. It is then evident that the maximum cascading factor n_{max} is determined by

$$u - n_{max}\,\epsilon \geq s \quad .$$

In the new Illinois computer design this gives $n_{max} = 6$.

Since a voltage amplifier gives approximately 15 mμs operation time and an emitter-follower AND or OR approximately 3 mμs, the average time for 7 stages of logic with level restoration is (6 x 3 mμs + 1 x 15 mμs)/7 = 4.5 mμs. It should be noted that in case a NOT function is needed in the logic, it becomes necessary to go over to 2-wire logic in which each AND-OR combination has the dual combination in the second lead. The NOT operation then simply corresponds to crossing the two signal wires. In some fast parts of the new Illinois computer use is made of this possibility.

1.7 Constant Current Emitters and Collectors

One of the important characteristics of a voltage amplifier stage is its logical gain (LG) defined by: (see Figure 2)

$$LG = -\frac{\Delta j}{\Delta i} \quad .$$

This gain is always less than one because of the dc-stepdown between collector P and output Q.

Since $\Delta k + \Delta j + \Delta i = \Delta e$ in Figure 2, we have

$$LG = -\frac{\Delta j}{\Delta i} = 1 - \frac{\Delta e - \Delta k}{i_0}$$

The LG must be maximized with:

1. A given saturation margin δ at P (i.e. collector-base voltages must be $\geq \delta$).
2. A given minimum swing $\pm$ s at Q.

It can be shown that to a good approximation this leads to:

$$LG = \frac{V-s}{V-s-\delta} \quad .$$

Once more the choice of a big V becomes mandatory.

As regards the emitter-return voltage, it can easily be seen that it, too, must be big enough to make (E^*, R_{E^*}) behave like a current source. In this case all capacitances attached to the emitter can be charged or discharged with a constant current (chosen to be the maximum current $i_0 = P/\delta$ where P is the dissipation rating of the transistor's collector!). This is, of course, faster than any other system (see Section 2.5). In practice it is easiest to make $E^* = E$.

One of the non-negligible advantages of constant current emitters, collectors and dc-stepdown returns is the fact that the load variation on the busses supplying these points is greatly reduced. This, in turn, reduces interaction between neighboring circuits, a feature which is important in view of what was said about noise in Section 1.5.

2. HARDWARE PARAMETERS AND CIRCUIT PERFORMANCE

2.1 Intrinsic Time Constants

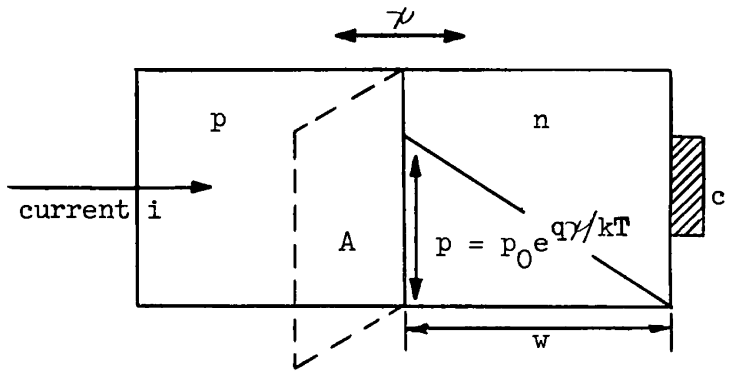


Figure 3
Planar Diode Junction
(forward bias)

Consider a planar pn diode junction with a potential jump $\mathcal{V}$ across it such that current flows in the forward direction. It is well known that the density of minority carriers in the n type base has the property that:

1. $p = p_0 e^{q\mathcal{V}/kT}$ at the junction.
2. $p = 0$ at the "ohmic contact" C.

(q = charge of an electron, t = absolute temperature, k = Boltzmann's constant). Assuming a linear decrease of p between junction and contact (this can be shown to be a good approximation) the charge Q of minority carriers in the base accumulated during the forward conduction is:

$$Q = \frac{1}{2} Awp = \frac{Awp_0}{2} \quad e^{q\mathcal{V}/kT}$$

where A is the junction area and w the base width.

On the other hand it is well known that

$$i = i_s \left(e^{q\mathcal{V}/kT} - 1\right) ,$$

where i_s is the (reverse) saturation current of the junction. This current i_s

is usually $\ll$ i during forward conduction and we can write $e^{q\psi/kT} \sim \frac{i}{i_s}$. Therefore

$$Q = \frac{Awp_0\, i}{2i_s} \quad .$$

Calling $Awp_0/2i_s$ the "intrinsic time constant" τ_D of the diode, we have

$$Q = \tau_D\, i \quad .$$

It is not too hard to measure τ_D by observing the reverse recovery curve of a diode: for a given forward current the i reverse vs. t curve for a

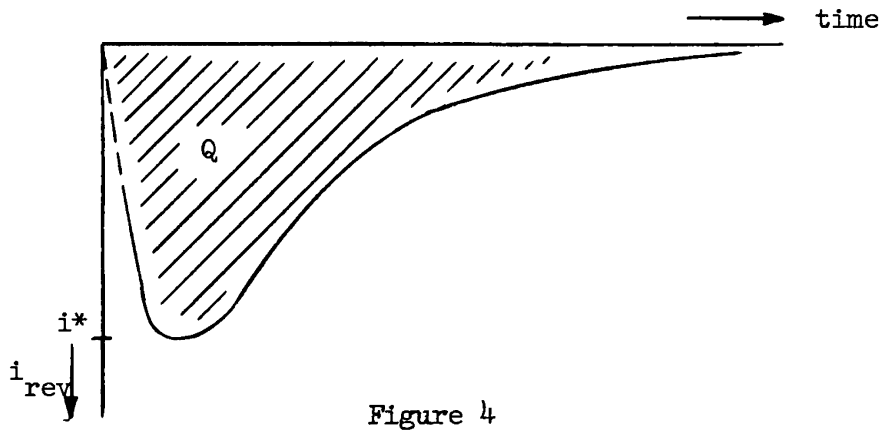


Figure 4

Reverse Recovery Curve of a Diode

given load R and reverse bias B is observed (i* in Figure 4 $\sim$ B/R, the initial downswing is due to the scope amplifier!); Q is the area under this curve. Experiment shows that the Q/i forward ratio is fairly constant, making τ_D a useful parameter.

It is evident that a transistor behaves like a diode as regards its emitter-base junction during forward conduction. It is then possible to define a τ_T for the transistor base charge.

When a diode or the emitter-base junction in a transistor is reverse biassed, equilibrium, i.e. "non-conduction" of the junction only occurs after the charge τ_D i forward or τ_T i_e has been taken from the base. Knowing the current available to eliminate the base charge, it becomes possible to calculate the "unhook times" of the devices.

2.2 Diode Parameters

Diodes are specified by the following parameters:

1. Their dissipation.
2. Their reverse rating (at a specified current).
3. Their intrinsic time constant (or their reverse recovery curve).
4. Their forward drop vs. i curve or more precisely the spread curves (see Section 3.2) for a given confidence level and age.

Usually the dissipation rating (at the maximum temperature) is not a limiting factor since $\tau_D\ i_{forw.}$ limits currents to a smaller value than $v_{forw.}\ i_{forw.}$. Generally i_{forw} is limited by the circuit to much lower values than those permitted dissipationwise.

The reverse rating (which decreases with temperature and has therefore to be measured at the highest temperature) is measured arbitrarily at a given current $i^*_{rev.}$ (100 μa for example). In reality this critical current

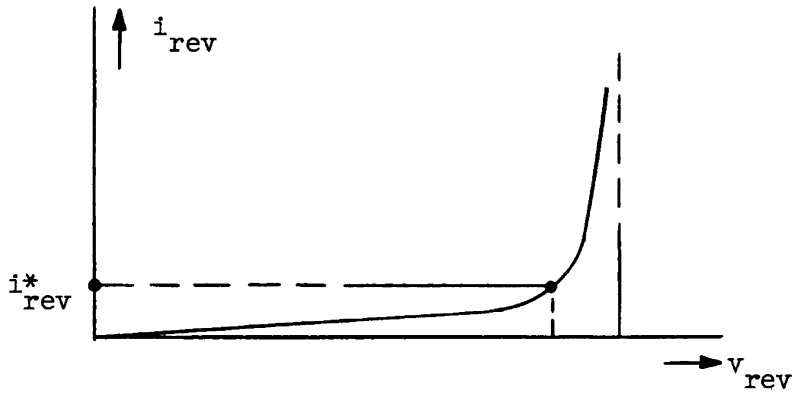


Figure 5
Reverse Behavior of a Diode

is a function of the diode, being chosen "below the knee" of the breakdown curve. Since this breakdown is preponderantly controlled by surface phenomena, it is very sensitive to aging, indeed so much so that it is often the critical parameter which determines the useful life of a transistor (see Section 3.1).

The intrinsic time constant and the way of obtaining its value has been discussed in the last section. It should only be added that in practice it is quite difficult to find diodes which have simultaneously a low forward drop and a low τ_D (eg. < 10 mμs).

The question of spread curves and their significance will be discussed in more detail in Section 3.2. The important thing to note is that it is impossible to trace these curves for a 100% confidence level; in other words, after some aging there are always a few units which are outside of any preset band. It should also be remarked that spread curves must be drawn to include temperature, humidity and, of course, aging effects.

2.3 Transistor Parameters

Besides diode parameters, collector parameters must be used to specify a transistor. The whole unit is therefore characterized by:

1. Its dissipation ($\sim$ collector dissipation).
2. The emitter-base reverse rating (at a given current this is the critical parameter in the new Illinois computer).
3. The emitter-base diode intrinsic time constant τ_T.
4. The emitter-base forward drop spread curve.
5. The base-collector reverse rating (at a given current).
6. The base spreading resistance r_b'.
7. The alpha cutoff frequency $f_{\alpha c}$.
8. The range of alpha (dc value).
9. The collector depletion capacitance plus header capacitance C_c (for average collector voltage).
10. The saturation margin δ (for a given collector current).
11. The collector dissipation P (for a given temperature).
12. The "thyristor breakdown voltage" (for a given load).

Item 5 is similar in nature to item 2. For both it should be remarked that some specification is necessary regarding the potential of the unused electrode. Generally two methods are adopted: either the unused electrode floats or it is connected to the base. Practically there seems to be only an insignificant difference.

It will be shown that the base spreading resistance r_b' must have a certain minimum value to guarantee the stability of emitter followers. On the other hand it adds to the emitter-base diode drop a term $r_b' (1 - \alpha) i_e$ and should therefore not be made too great either. A close relationship between the physical mechanisms responsible for the emitter-base reverse rating and r_b' leads to a simultaneous increase in both parameters.

The specification of the alpha cutoff frequency is only useful in so far as the reciprocal of the 3dG down-alpha cutoff frequency gives the carrier transit time in the base: this is an important parameter in switching. It turns out that for the new Illinois computer circuitry speeds are essentially circuit limited and that $f_{\alpha c}$ plays a relatively minor role.

The range of dc-alpha, and in particular the lowest value encountered under aging and drift conditions is primordial for the circuit designer since it fixes the input current range when emitter currents are known (the new Illinois computer system uses constant current sources!). It is customary to assume that the dc-alpha never exceeds 1.

The total collector to ground capacitance (depletion layer plus header) is a function of collector voltage: the depletion layer capacitance follows a $v_{cb}^{-1/2}$ or $v_{cb}^{-1/3}$ law, depending on the abruptness of the junction. To simplify matters it is accepted to measure C_c in the middle of the usual collector swing range.

The saturation margin δ (which depends on the collector current) can be defined in an approximate way by the fact that for $|v_{cb}| < \delta$ dc-alpha decreases violently for the assumed current. Since a collector near saturation acts approximately like an ohmic resistance, it is often useful to define a saturation resistance: this resistance, multiplied by the collector current, gives δ.

The allowed collector dissipation P (which is highly temperature dependent) determines the allowed maximum current i_{max} via $P = \delta(i_{max})\, i_{max}$ for non-saturating circuits. As was mentioned before (see Section 1.5) high power means high speed, because circuit speeds are proportional to i_{max}.

The thyristor breakdown voltage is defined under slightly simplified assumptions for the v_{cb} vs. i_c curve (as a function of i_b): in practice, once thyristor behavior occurs (i.e. once collector multiplication sets in and gives ac-alpha > 1) the negative resistance part of $v_{cb}(i_c)$ is nearly independent of i_b and $i_b = 0$ (floating base) can be taken as representative of the phenomenon. As shown in Figure 6, the value of this breakdown voltage is load dependent, since it is found by intersecting the tangent load line to the $i_b = 0$ $v_{cb}(i_c)$ curve with the v_{cb}-axis. It should be noted that usual thyrister breakdown voltages are only $\sim$ 50% of the collector reverse voltage rating.

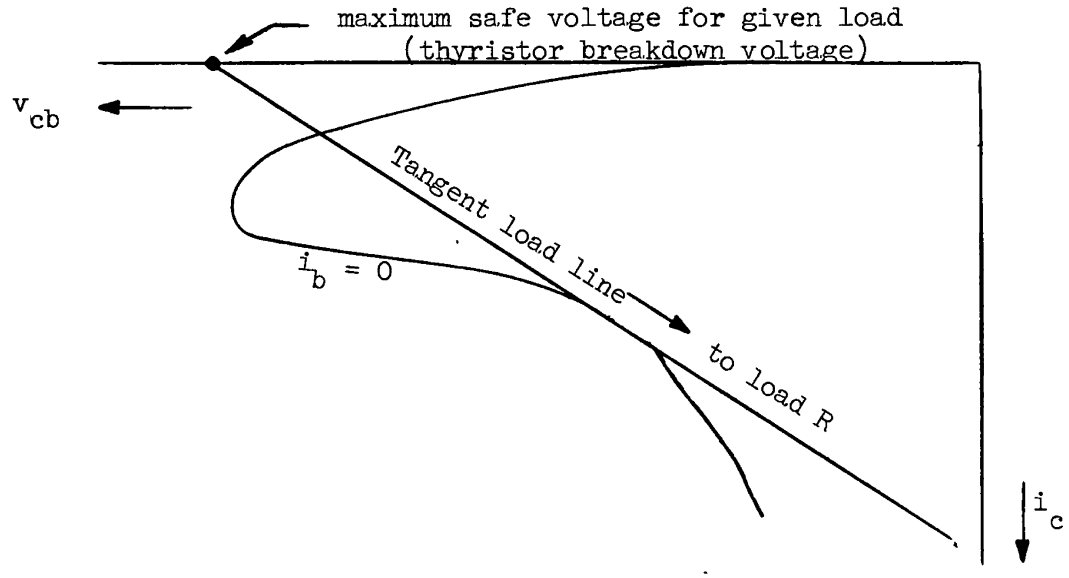


Figure 6
Thyristor Curve of Transistor

2.4 Sensitivity of Switching Amplifiers

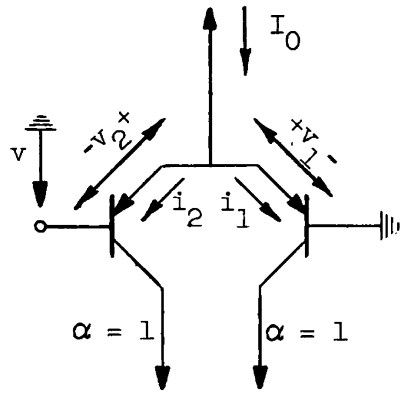


Figure 7
Idealized Switching Amplifier

Figure 7 shows an idealized switching amplifier in which it is assumed that the dc-alphas are equal to unity. I_1 and I_2 being the (reverse) saturation currents of the emitter-base diodes, we then have:

$$i_1 = I_1 \left(e^{\frac{qv_1}{kT}} - 1 \right)$$

$$i_2 = I_2 \left(e^{\frac{qv_2}{kT}} - 1 \right)$$

$$v = v_1 - v_2$$

$$I_0 = i_1 + i_2 \ .$$

It is trivial to show that this implies

$$i_2 = I_2 \left[\frac{I_0 + I_1 + I_2}{I_2 + I_1 e^{\frac{qv}{kT}}} - 1\right]$$

and therefore the $i_2(v)$ characteristic is directly known. In case $I_1 = I_2$, one can easily see that $i_1 = i_2 = I_0/2$ for $v = 0$ and that for $v = \pm .1v$ ratios of $\frac{i_1}{i_2}$ of .05 and .95 can be expected (see Figure 8). Statically, therefore,

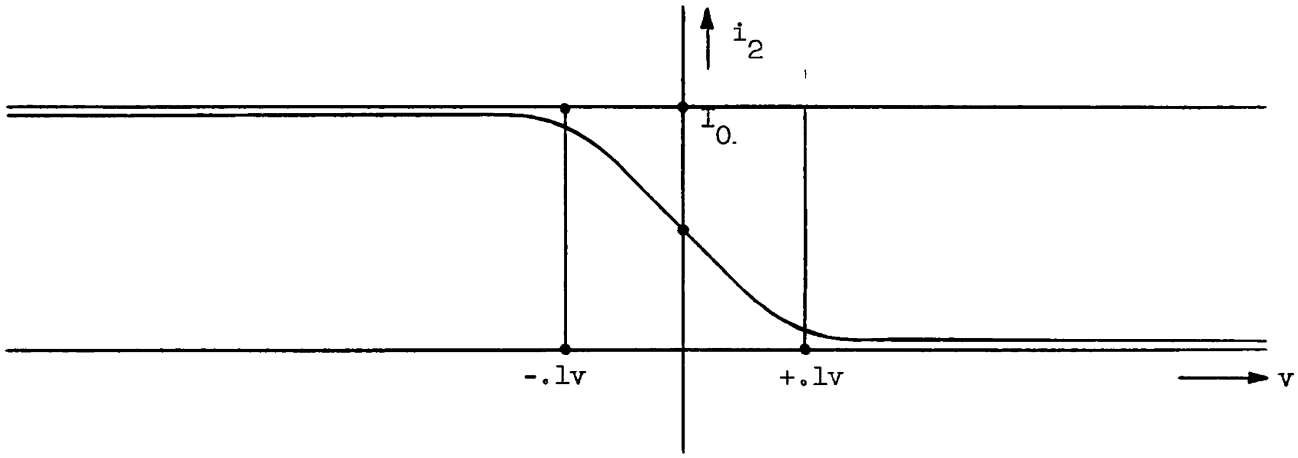


Figure 8

Switching Characteristic for a Switching Amplifier with Identical Transistors

practically the whole current is switched in the interval − .1v to + .1v: this gives the switching amplifier its great sensitivity. Since non-identical transistors as well as ionization phenomena under transient conditions can change the picture, an additional $\pm$ .5v is required under worst conditions, making the maximum required input to such a stage $\pm$ .6v.

It should be noted that the latter phenomena can most easily be discussed by using a graphical analysis according to Figure 9. Here the diode curves are drawn in opposite directions (currentwise) starting from two origins 0_1 and 0_2 which are separated by the amount of the constant current I_0. Going from a 5% on to a 95% on state then requires a switching voltage v' + v".

Finally it should be remarked that the analysis is unchanged if the transistor having a grounded base is replaced by a diode.

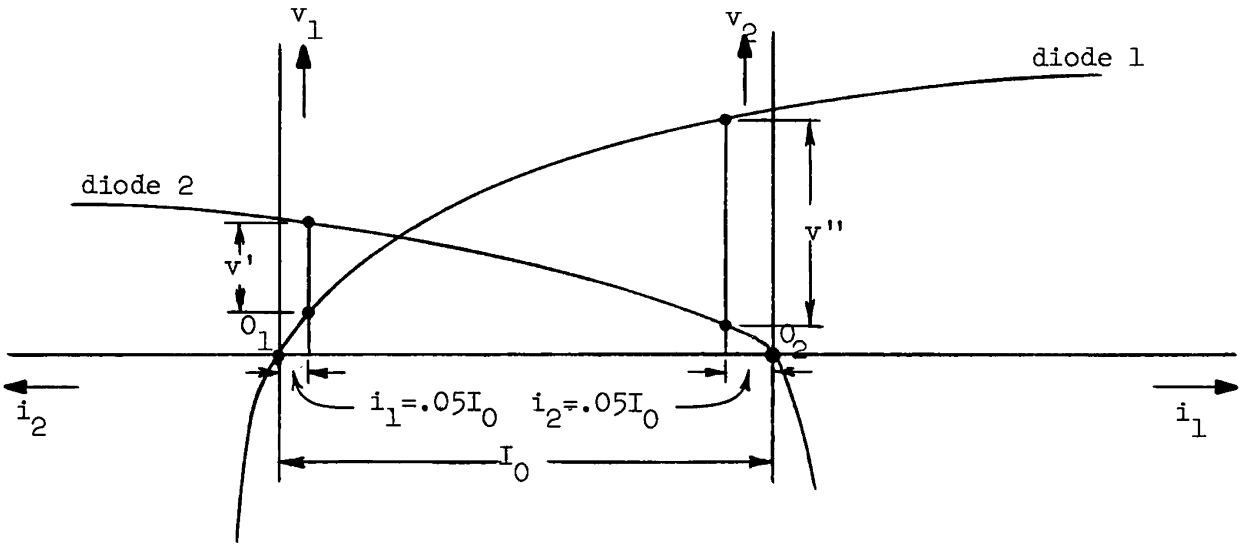


Figure 9

Graphical Analysis of Switching (Difference) Amplifier

2.5 Speed of Voltage and Current Amplifiers

The usual approach of setting $i_c = \alpha\, i_c$, assuming α of the form

$$\alpha = \frac{\alpha_0 \cosh p}{\cosh\left[p\sqrt{1+s}\right]} \qquad (s = \omega t)$$

and finding i_c in response to a step function $i_c = 1/s$ by Laplace transforms is practically not very useful, since it is only valid for "small pulses" superimposed on big dc-values.

A "large-signal" switching theory is always based on equivalent circuits for the transistor. In the discussion below this equivalent circuit is simplified to its utmost by the use of a linear addition principle and intrinsic time constants.

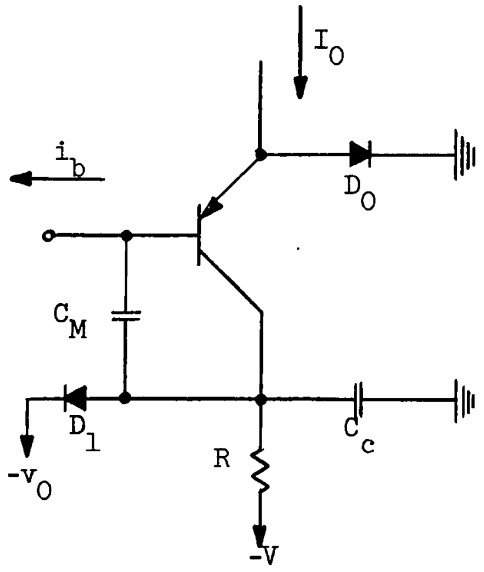


Figure 10

A Switching Amplifier with an Emitter Switching Diode D_0 and a Collector Bumping Diode D_1.

The operation of switching from ON to OFF or vice-versa is decomposed into several elementary steps of calculable duration in the table below. Base delays are assumed to be $1/f_{\alpha c}$, diode charge or discharge times of the form

$$\frac{\tau \text{ X forward current}}{\text{charge or discharge current}} .$$

Note that we can make some approximations by realizing that the base currents ("overcurrents") i_b available (above and beyond the dc-value $I_0/1-\alpha$) are rather small compared to I_0 and that it is legitimate to neglect the charge/discharge times of D_0 with respect to those of the base-emitter diode charged by i_b. Similarly it seems allowed to neglect the "charge time" for the bump D_1 while the discharge or "unhook time" can be quite big since the current in R can be small during the negative swing of the collector. Very exact analysis shows, however, that these "secondary effects" can be observed (see Section 3.6).

Another remark is relative to the Miller capacitance C_M between collector and base: it increases the input capacitance by C_M x (voltage gain − 1). Practically the base diffusion capacitance is so big that C_M can be neglected. The input delay is then solely caused by the diffusion charge $\tau_T I_0$ in its base, i.e. characterized by the intrinsic time constant τ_T of the emitter-base diode.

The table below gives the "elementary times" for ON-OFF and OFF-ON transitions. Analysis shows that:

1) Many terms are augmented for non-switching voltage amplifiers. By comparing their sum for current designs of voltage amplifiers meeting given tolerance conditions, it can be seen that the switching amplifier type comes out ahead.

2) All terms are zero for emitter-followers leaving only the capacitive loading on the emitter as time-determining factor.

Table of Elementary Switching Times

	Part of Transition	Time	Expression for Time	
			OFF ⟶ ON	ON ⟶ OFF
1.	Reach switching point	τ_{discr}	depends on time to reach 0 for the output of last stage.	
2.	Charge/discharge base-emitter diode	τ_{diff}	$\frac{\tau_T I_0}{i_b}$	$\frac{\tau_T I_0}{-i_b}$
3.	Base delay	τ_{base}	$\frac{1}{f_{\alpha c}}$	$\frac{1}{f_{\alpha c}}$
4.	Charge/discharge bumping diode	τ_{bump}	0	$\frac{\tau_D[I_0 - \frac{V-v_0}{R}]}{\frac{V-v_0}{R}}$
5.	1/2 Collector rise/fall	τ_{coll}	$\frac{1}{2}\frac{C_c(V-v_0)}{I_0}$	$\frac{1}{2} RC_c$

Several comments should be made. First of all the time to reach the switching point may be assumed to be the "1/2 Collector rise or fall time" of

the preceding stage. The reason for taking only 1/2 of these times is simply that this is sufficient to allow the output (under non-drift conditions) to switch the next stage.

$\tau_{sw} = \tau_{discr.} + \tau_{diff.} + \tau_{base} + \tau_{bump} + \tau_{coll.}$ is therefore a good estimate of the "delay per stage" or "operation time" (see Section 3.4). Another comment is that if the constant current emitter were replaced by a variable source (resistor to ground, for example), the $1/2\ \frac{C_c(V-v_0)}{I_0}$ would be replaced by $1/2\ \frac{C_c(V-v_0)}{I_{0\ av.}}$, where of course $I_{0\ av.} < I_0$: such an arrangement must be slower.

The order of magnitude of all the elementary times quoted is from 2 - 3 mμs in the new Illinois computer circuits. This gives rise to the 10 - 15 mμs operation times mentioned in Section 1.2. Substitution of the circuit values (see Section 6) and the hardware parameters (see Section 5) shows easily that the above expressions are indeed in the range 2 - 3 mμs.

In the case of an emitter-follower it can be seen that to a good approximation

$$\tau_{EF} = \frac{\text{output swing X } C_E}{I_0} \qquad (C_E = \text{emitter-ground capacitance})$$

giving values of the order of 2 - 3 mμs. This, then, justifies the use of "emitter-follower-diode logic with as few switching amplifiers as possible", discussed in Section 1.6.

2.6 Emitter-Follower Oscillations

Negative resistances can be created statically by amplification phenomena and dynamically by "out-of-phase responses" due to carrier storage in devices. In particular the carriers stored in the base of a diode or a transistor can give rise to "diode-amplifier" effects. In the case of an emitter-follower this implies that at certain frequencies its input impedance Z_{IN} can have a negative real component sufficient to throw circuits connected to the input into violent oscillations. A detailed analysis shows that the real part $R\ Z_{IN}$ is approximately of the form

$$R\ Z_{IN} = r_b' + r_e - \frac{1}{\omega_c C_E}$$

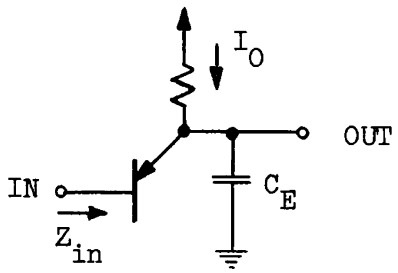


Figure 11
Emitter-Follower

where r_b' and r_e are the base spread resistance (see Section 2.3) and the equivalent small signal emitter resistance respectively, while $\omega_c = 2\pi f_{\alpha c}$. If we assume that $C_E \geq 3$ μμF (which is always obtainable by wiring) and knowing that $r_e > 0$ and $f_{\alpha c} < 500$ mc, we obtain

$$R\, Z_{IN} = (r_b' - 100)\,\Omega .$$

For this reason stable behavior of emitter-followers demands a lower bound on the specification of r_b' equal to 100 Ω for the new Illinois computer circuitry (see Section 7.1).

2.7 Hysterisis and Loop Gain in Flipflops

It can be shown in the most general case that a flipflop exhibits hysterisis and that the magnitude of this hysterisis is related to the closed loop gain of the flipflop.

Figure 12 shows a general amplifier of gain A having as input some quantity x_1 and delivering as output some quantity x_2. x_1 is composed of two quantities x_0, the input from the external world and x_3, a fraction β of the output quantity x_2.

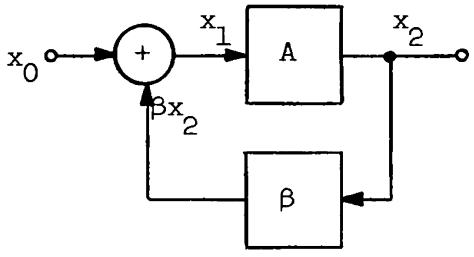


Figure 12
Feedback Amplifier

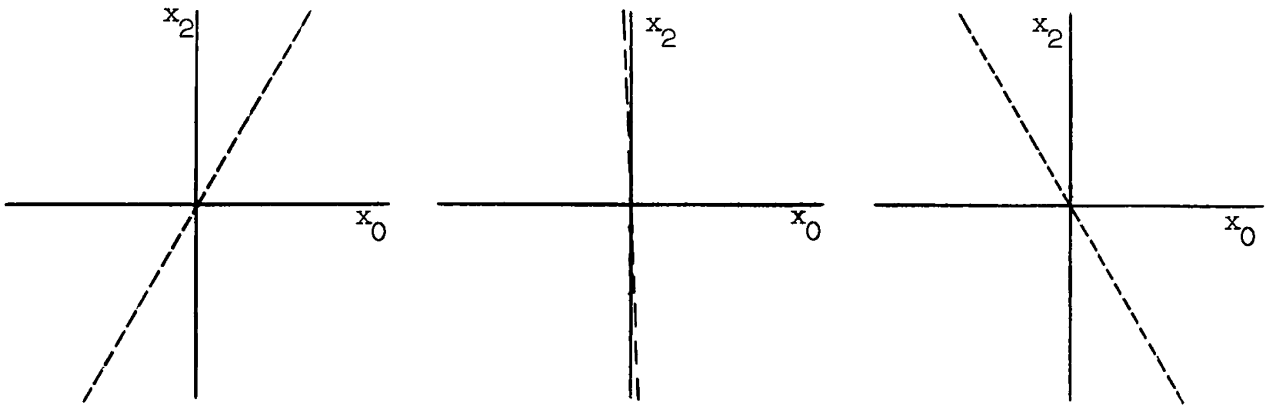
Evidently

$$x_2 = (x_0 + \beta x_2)\, A$$

or

$$\frac{x_2}{x_0} = A^* = \frac{A}{1 - \beta A}$$

where A^* is the overall gain between x_0 and x_2 terminals. The characteristic x_2 vs. x_0 is plotted in figure 13 for the three cases, $\beta A < 1$, $\beta A = 1$ and $\beta A > 1$.



Case 1 Case 2 Case 3

Figure 13

Transfer Characteristics of Feedback Amplifiers

Now βA is called the loop gain Γ : Γ is the gain when the amplifier-feedback loop is cut and the injected and resultant variations in x are compared. It is evident that $\Gamma < 1$ gives a situation where the output follows the input and that $\Gamma > 1$ gives one in which the output "resists" disturbance, i.e. the output opposes the input. $\Gamma = 1$ represents the crossover point between these two modes.

Assume now that some nonlinearity prevents the output x_2 from exceeding the limits $\bar{x}_2$ and $\underline{x}_2$,

$$\text{i.e. } \underline{x}_2 \leq x_2 \leq \bar{x}_2 \ .$$

The plots of figure 13 now become as shown in figure 14. In each case the gain A^* is given by the slope of the characteristic between the $\underline{x}_2$ and $\bar{x}_2$

limits. For zero input ($x_0 = 0$) there is evidently only one operating point (1) in case 1 but three operating points (1), (2) and (3) in case 3. It may be shown that of these points (1) and (3) represent points of stable equilibrium while (2) represents a point of unstable equilibrium. Hence case (3)

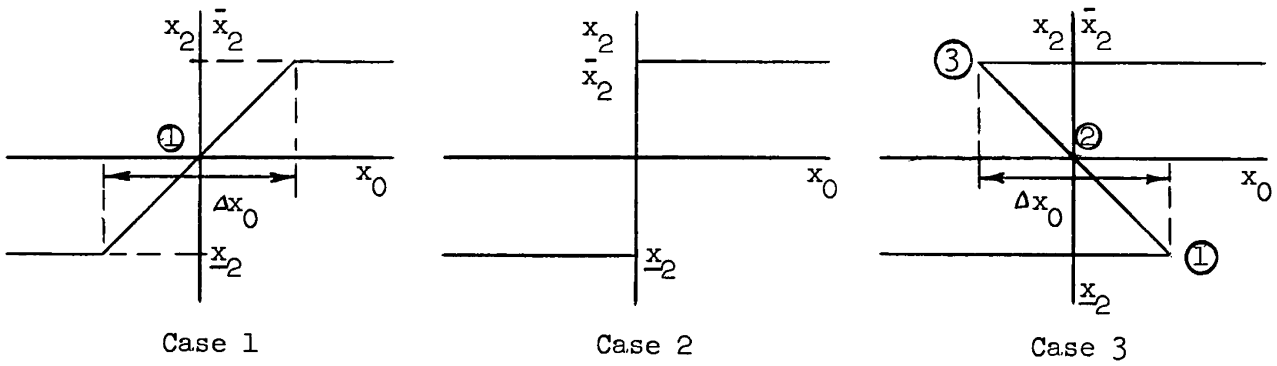


Figure 14

A Bumped Feedback Amplifier

represents a bistable circuit (flipflop) and we may define the hysterisis width as Δx_0, the distance between the intersections of a line of slope A* with the lines $\underline{x}_2$ and $\bar{x}_2$ projected onto the x_0 axis.

Then
$$\Delta x_0 = -\frac{\bar{x}_2 - \underline{x}_2}{A^*}$$
$$= \frac{\bar{x}_2 - \underline{x}_2}{A}\ (\Gamma - 1),$$

i.e. $\Delta x_0 = 0$ if $\Gamma = 1$ (as shown in case 2) and $\Delta x_0 < 0$ if $\Gamma < 1$ (case 1).

2.8 Simplified Model of a Flipflop

We may obtain approximate values for Γ and Δx_0 for the simplified flipflop circuit of figure 15. Here a constant current I_0 is fed into a difference amplifier T_1T_2, the collector of the grounded base transistor feeding back into the input via a zero attenuation network obtained by forcing a current i_0 into the feedback resistor R. The input current i to the base of T_1

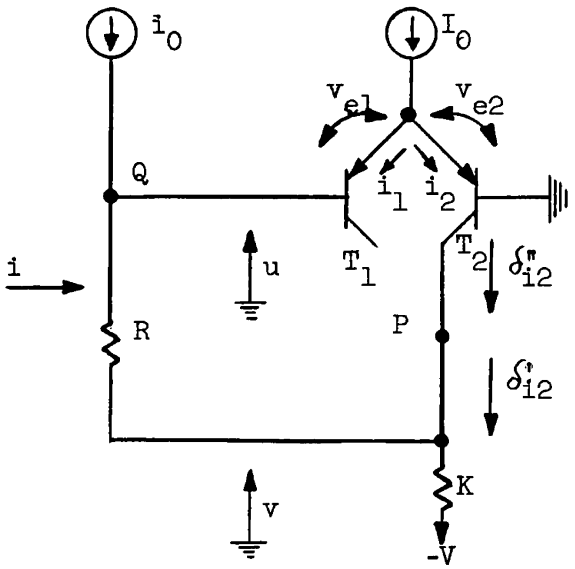


Figure 15

Model of an Asymmetric Flipflop

corresponds to the quantity x_0 in figure 12, while the output current i_2 corresponds to x_2 (note that in this simplified model none of i_2 is tapped off to drive a load). The open loop gain A is the current gain between terminals Q and P with the circuit broken at P. The feedback β is effected by the resistor R returned to the point W, increments in the current i and the current through R adding on the node Q to form the total input to the transistor corresponding to $x_1 = x_0 + \beta x_2$ in figure 15. Assume that $\alpha = 1$ for both transistors and that the emitter current i of a transistor is given by $i = I(e^{\frac{qv_e}{kt}} - 1)$. Then

$$i_1 = I_1 \left[e^{qv_{e1}/kt} - 1 \right]$$

$$i_2 = I_2 \left[e^{qv_{e2}/kt} - 1 \right]$$

$$\therefore \frac{kT}{q} \log_e \frac{(i_2 + I_2)I_1}{(i_1 + I_1)I_2} = (v_{e2} - v_{e1}) \quad .$$

If the loop is broken at point P and for an injected $\delta i_2'$ we get a return increment $\delta i_2''$, the loop gain Γ is given by

$$\Gamma = \frac{\delta i_2''}{\delta i_2'} \quad .$$

Put $i_1 = i_2 = \frac{I_0}{2}$ and $I_1 = I_2 = I$; this means that T_1 and T_2 are identical in characteristic. Then

$$k\,\delta i_2' = \frac{kT}{q} \log_e \frac{\left(\frac{I_0}{2} + I + \delta i_2''\right)}{\left(\frac{I_0}{2} + I - \delta i_2''\right)}$$

$$= \frac{kT}{q} \log_e \frac{1 + \frac{\delta i_2''}{\frac{I_0}{2} + I}}{1 - \frac{\delta i_2''}{\frac{I_0}{2} + I}}$$

which may be expanded to read

$$k\,\delta i_2' \simeq \frac{kT}{q} \cdot 2 \frac{\delta i_2''}{I + \frac{I_0}{2}}$$

neglecting higher order terms,

$$\text{i.e.} \quad \Gamma = \frac{\delta i_2''}{\delta i_2'} = \frac{q}{kT} \cdot \frac{k\,(I_0 + 2I)}{4}$$

or, since $I << I_0$,

$$\boxed{\Gamma \simeq \frac{q}{kT} \cdot \frac{k\,I_0}{4} \cdot}$$

Similarly it can be proved that the gain between points Q and P is

$$A \simeq \frac{q}{kT} \cdot \frac{(R + K)\,I_0}{4} \cdot$$

The output current bounds are $0 \leq i_2 \leq I_0$ and hence from the formula

$$\Delta x_0 = \frac{\bar{x}_2 - x_2}{A} (\Gamma - 1)$$

we get:

$$\boxed{\Delta i = \frac{4}{\lambda (R + K)} - \frac{K\,I_0}{R + K} \quad \text{where } \lambda = \frac{q}{kT} \cdot}$$

For typical values take R = 1k, say K = 2k, I_0 = 10 ma and λ = 40.

$$\Delta i \simeq \frac{4}{40 \times 3 \times 10^3} - \frac{20}{3} \simeq -7 \text{ ma.}$$

This, although only an approximation for the vastly simplified model of figure 15 agrees well with the observed value of some 5 ma for the asymmetric flipflop.

Remark: It is possible to obtain a value for Δi by a slightly cruder method: assuming that the circuit regenerates only at the critical position $i_1 = i_2 = \frac{I_0}{2}$ and that this corresponds to u = 0, then: case 1, T_1 ON to OFF

$$i_{0\to1} = \frac{V}{K + R} - i_0 \text{ by inspection}$$

case 2, T_1 OFF to ON

$$i_{1\to0} = \frac{V - K(I_0 + i_0) - Ri_0}{K + R}$$

$$\therefore \Delta i = i_{0\to1} - i_{1\to0} = \frac{K I_0}{K + R} \quad .$$

This differs by only about 1% from the value previously obtained, for the given values for R, K, etc.

2.9 Gain-Bandwidth Product of the Model Flipflop

For the same model as in the previous section (i.e. figure 15) we may find approximations to the operating time τ and hence a figure of merit, in terms of the gain bandwidth product $\frac{\Gamma}{\tau}$ for the flipflop. To do this we shall assume that point Q (in figure 15) carries a capacitor C_R and point P carries a capacitor C_K, the resulting circuit being redrawn in figure 16. A simple analysis yields for the input currents causing the 0→1 and 1→0 transitions respectively (see last section)

$$i_{0\to1} = \frac{V}{K + R} - i_0$$

$$i_{1\to0} = \frac{V - K(i_0 + I_0) - Ri_0}{K + R} \quad .$$

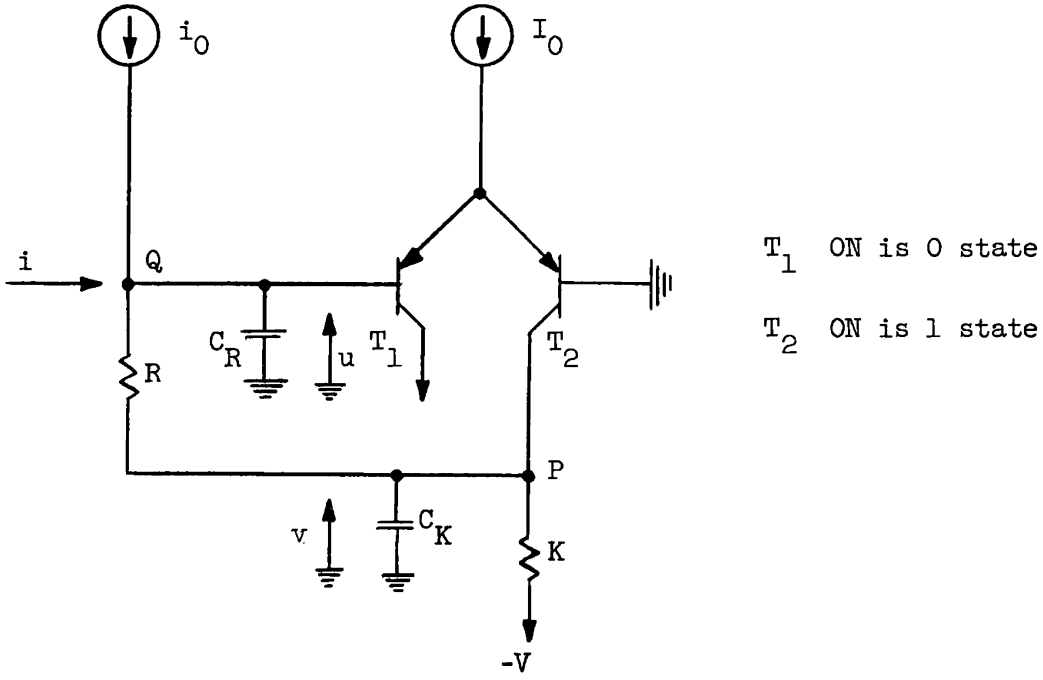


Figure 16

Assumed Capacitances in Time Model of Flipflop

It can also be easily seen that for the 0 and the 1 state respectively

$$u_0 = -V + (K + R)\, i_0$$

$$u_1 = -V + (K + R)\, i_0 + K\, I_0$$

$$v_0 = -V + K i_0$$

$$v_1 = V + K(i_0 + I_0) \,.$$

For a 0→1 transition,

$\tau_{0\to 1}$ = time to move input point Q to regenerating region + time for collector P to close loop + time for Q to settle at its new value.

$$= \frac{C_R\,[V - (R + K) i_0]}{\frac{V}{K + R} - i_0} + C_K K + \frac{RC_R\,[-V + K(i_0 + I_0) + R i_0]}{K I_0} \,.$$

Similarly

$$\tau_{1\to 0} = \frac{C_R\,[-V + (K+R)i_0 + KI_0]}{\dfrac{-V + K(I_0 + i_0) + Ri_0}{K+R}} + C_K K + \frac{RC_R\,[-(R+K)i_0 + V]}{KI_0}$$

$$\tau = \tau_{0\to 1} + \tau_{1\to 0} = 2C_K K + C_R R + 2C_R(K+R)$$

$$= C_R\,[2K + 3R] + C_K\,[2K] \quad .$$

Now

$$\Gamma = \frac{q}{kT} \cdot \frac{KI_0}{4} = \frac{q}{kT} \cdot \left[\frac{\tau - 3RC_R}{2(C_K+C_R)}\right] \cdot \frac{I_0}{4} \quad .$$

Now if $3RC_R << \tau$ (a somewhat crude assumption) we have

$$\text{gain x bandwidth} = \frac{\Gamma}{\tau} = \frac{\lambda I_0}{8(C_R + C_K)} \quad \text{where } \lambda = \frac{q}{kT} \, .$$

For $\lambda = 40$, $I_0 = 10$ ma, $C_R + C_K = 10$ $\mu\mu$F this gives

$$\frac{\Gamma}{\tau} = \frac{40 \times 0.01}{8 \times 10^{-11}}$$

$$= 5 \times 10^9 \text{ sec}^{-1}$$

which is not unreasonable. In practice, of course, there are several additional factors to take into account; e.g. minority carrier transit time through the base region, charge and discharge time of bumping diodes and emitter-base diodes, attenuation due to imperfect current sources for i_0 and I_0, etc.

3. RELIABILITY AND TOLERANCE CONSIDERATIONS

3.1 Aging of a Single Parameter

Consider a parameter, say A_ν, among the parameters defining the operations of a semiconductor device. If the specifications for this device limit the initial range of A_ν to $(\underline{A}_\nu, \bar{A}_\nu)$, it is usual for the manufacturer to select in the batch of devices produced in one run all those satisfying $\underline{A}_\nu \leq A_\nu \leq \bar{A}_\nu$ (and, usually, simultaneous similar conditions on other parameters). This selection mechanism gives rise to an initial distribution curve of nearly rectangular shape. Let $\delta(A_\nu, t)$ be the distribution at time t, defined by the property that for a large number - N - of devices the number dN of devices with the parameter between A_ν and $A_\nu + dA_\nu$ is given by

$$dN = N\delta(A_\nu, t)dA_\nu \quad .$$

Then we have in case of a rectangular distribution

$$\delta(A_\nu, 0) = \begin{cases} \dfrac{1}{\bar{A}_\nu - \underline{A}_\nu} & \text{for } \underline{A}_\nu \leq A_\nu \leq \bar{A}_\nu \\ 0 & \text{otherwise} \end{cases}$$

and obviously

$$\int_{\underline{A}_\nu}^{\bar{A}_\nu} \delta(A_\nu, 0)dA_\nu = 1 \quad .$$

As the device ages, the distribution will deviate more and more from the rectangular shape, tending often towards a Gaussian distribution, defined by

$$\delta(A_\nu, t) = \delta_0 \; e^{-\left(\frac{\bar{A}_\nu + \underline{A}_\nu}{2} - A_\nu\right)^2 / a(t)}$$

where a(t) is some function of time. The fraction of useful devices with $\underline{A}_\nu \leq A_\nu \leq \bar{A}_\nu$ will be called $p(\underline{A}_\nu, \bar{A}_\nu, t)$: This is clearly the probability of being able to use the device at time t. We have

$$p(\underline{A}_\nu, \bar{A}_\nu, t) = \int_{\underline{A}_\nu}^{\bar{A}_\nu} \delta(A_\nu, t)dA_\nu$$

$$1 = \int_{-\infty}^{+\infty} \delta(A_\nu, t)dA_\nu \quad .$$

Figure 17 shows the evolution of $\delta(A_\nu, t)$ graphically.

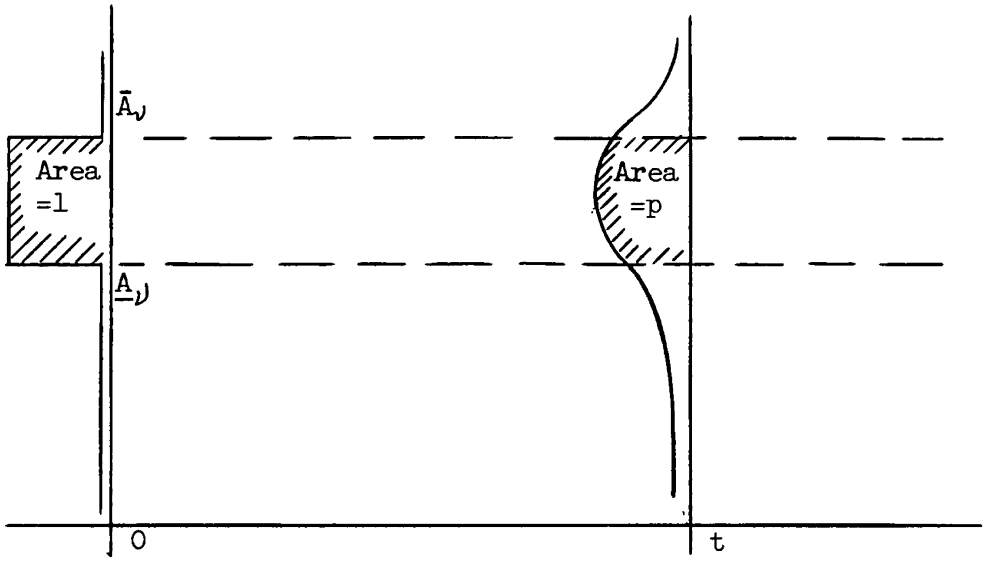


Figure 17
Evolution of a Parameter Distribution with Time

It can be seen without difficulty that it is possible to define an average lifetime T_ν for this device and this parameter A_ν by taking the average of the times at which the devices of a large sample (N units) drift out of range. T_ν has the property that it can be calculated once $\delta(A_\nu, t)$ is known:

$$T_\nu = \int_0^\infty p(\underline{A}_\nu, \bar{A}_\nu, t)dt$$

$$= \int_0^\infty \int_{\underline{A}_\nu}^{\bar{A}_\nu} \delta(A_\nu, t)dA_\nu dt \quad .$$

Suppose now that $T_\varnothing \ll$ all other T_ν's; $A_\varnothing$ is then called the life-determining parameter. (In case of the new Illinois computer this life determining parameter is the emitter-base reverse rating.)

3.2 Confidence Levels. Spread Curves.

Assuming that there is a life-determining parameter $A_\varnothing$, the question comes up: What are the reasonable limits for another A_ν during the $T_\varnothing$ hours that the device works on the average? Evidently A_ν has again a distribution $\delta(A_\nu, t)$

and it is not at all excluded that δ has "tails" (corresponding to non-zero values) for very large values of A_ν. This, then, means that if it is desired to talk about reasonable limits $\underline{A}_\nu$, $\bar{A}_\nu$ for the first $T_{@}$ hours, it is necessary to know

1) at what time $0 \leq t \leq T_{@}$ the tails are worst,
2) what percentage of the units has to be within the bounds ("confidence level")?

Usually $\delta(A_\nu, T_{@})$ is the "worst" distribution. Supposing this to be so and fixing a confidence level λ ($\lambda = 98\%$ for example), $\underline{A}_\nu$ and $\bar{A}_\nu$ can now be defined by

$$\int_{-\infty}^{\underline{A}_\nu} \delta(A_\nu, T_{@})\, dA_\nu = \frac{1 - \lambda}{2}$$

$$\int_{\bar{A}_\nu}^{+\infty} \delta(A_\nu, T_{@})\, dA_\nu = \frac{1 - \lambda}{2}$$

Remark: Often $\bar{A}_\nu$, $\underline{A}_\nu$ vary little with λ around a value λ^* which defines a "knee" in the distribution. Then λ^* is a good value for the confidence level.

If, now, A_ν is a function of an independent variable x, the reasoning above can be carried through and quantities $\bar{A}_\nu(x)$, $\underline{A}_\nu(x)$ can be defined for the first $T_{@}$ hours. These quantities plotted as a function of x result in the so-called spread curves. An example of such curves (see Figure 18) is the diode forward drop as a function of current. It must be realized that the very existence of such spread curves is only possible if 1) the parameter represented is not the life-determining one and 2) a given confidence level has been defined.

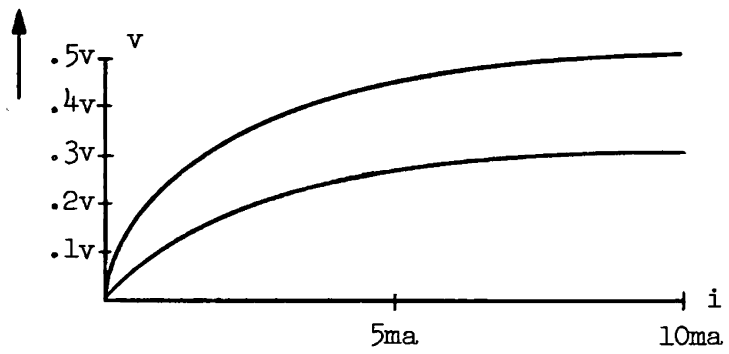


Figure 18

Example of a Spread Curve for a Diode Forward Drop

3.3 Tolerances. Critical Levels. Discrimination Levels.

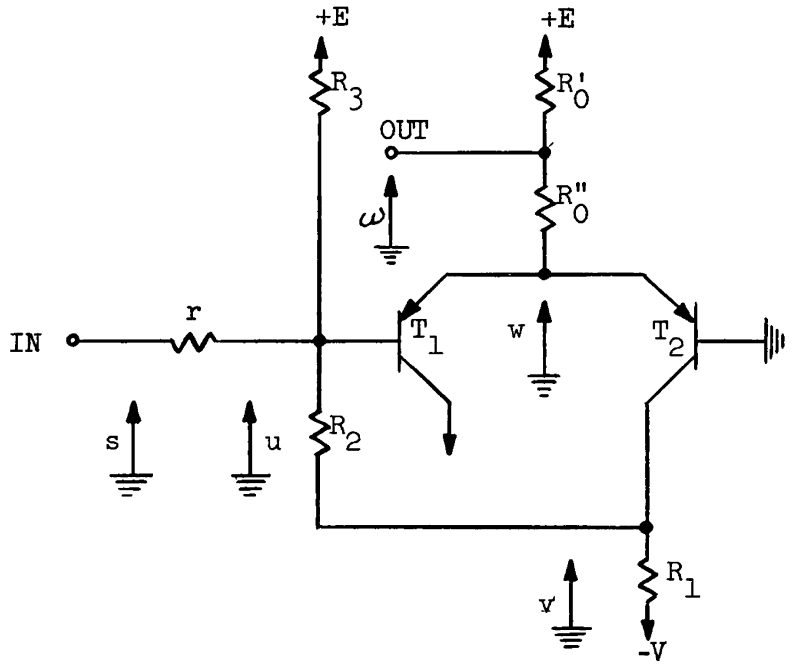


Figure 19

Asymmetric Flipflop used in Simplified Tolerance Analysis

Figure 19 shows an asymmetric flipflop circuit not unlike the one used in Section 2.8. Here, however, the constant currents into the emitters and the feedback network have been replaced by $\frac{E}{R'_0+R''_0}$ and $\frac{E}{R_3}$ respectively. An input resistor r has been provided in order to be able to control the input by voltages rather than by currents; r may be thought of as representing the output impedance of the previous stage. The output is taken from a tap on the emitter resistor (which is supposed to be of low impedance compared to the load). The operation will again be discussed for the case where both transistors have $\alpha = 1$, but here the additional simplifying hypothesis will be introduced that there is no voltage drop between emitter and base when a transistor conducts.

By definition the flipflop is in the 0 state when T_1 conducts and in the 1 state when T_2 conducts. It is quite straightforward to determine the voltages s, u, v, w and ω at the five "cardinal points", i.e. base of T_1,(IN), collector of T_2, emitters and OUT:

$$
\begin{aligned}
u_0 &= E\left(\frac{R_1 + R_2}{\Sigma}\right) - V\left(\frac{R_3}{\Sigma}\right) \\
v_0 &= E\left(\frac{R_1}{\Sigma}\right) - V\left(\frac{R_2 + R_3}{\Sigma}\right) \\
w_0 &= E\left(\frac{R_1 + R_2}{\Sigma}\right) - V\left(\frac{R_3}{\Sigma}\right) \\
\omega_0 &= E\left(1 - \frac{\nu R_1}{\Sigma}\right) - V\left(\frac{\nu R_3}{\Sigma}\right)
\end{aligned}
\qquad \text{For the 0 state}
$$

$$
\begin{aligned}
u_1 &= E\left(\frac{\Sigma + (\mu - 1)R_3}{\Sigma}\right) - V\left(\frac{R_3}{\Sigma}\right) \\
v_1 &= E\left(\frac{\mu(R_2 + R_3) + R_1}{\Sigma}\right) - V\left(\frac{R_2 + R_3}{\Sigma}\right) \\
w_1 &= 0 \\
\omega_1 &= E(1 - \nu)
\end{aligned}
\qquad \text{For the 1 state}
$$

where $\nu = \dfrac{R_0'}{R_0' + R_0''}$, $\mu = \dfrac{R_1}{R_0}$, $\Sigma = R_1 + R_2 + R_3$.

Consider the output voltage ω in the 1 state: ω_1 can take any value between two limits due to the fact that the power supplies and resistors vary--both from one unit to the next and in time: As explained in the last section, all hardware parameters have certain tolerances. If R is the "design center value" of a resistor with a fractional variation x, in extreme cases

$$
\begin{aligned}
\bar{R} &= R(1 + x) \\
\underline{R} &= R(1 - x) \quad .
\end{aligned}
$$

Here

$$\bar{\omega}_1 = \bar{E}\,\frac{\bar{R}_0''}{\underline{R}_1'}$$

$$\underline{\omega}_1 = \underline{E}\,\frac{\underline{R}_0''}{\bar{R}_1'}$$

Similarly it can be seen that if we suppose $V \gg E$ (and since $\frac{\bar{R}_0'}{\bar{R}_0' + \underline{R}_0''} > \frac{\underline{R}_0'}{\underline{R}_0' + \underline{R}_0''}$, $\frac{\bar{R}_3}{\bar{R}_3 + \underline{R}_1 + \underline{R}_2} > \frac{\underline{R}_3}{\underline{R}_3 + \underline{R}_1 + \underline{R}_2}$)

$$\bar{\omega}_0 = -\bar{V}\,\frac{\bar{R}_0'\bar{R}_3}{(\bar{R}_0' + \underline{R}_0'')(\underline{R}_1 + \underline{R}_2 + \bar{R}_3)}$$

$$\underline{\omega}_0 = -\underline{V}\,\frac{\underline{R}_0'\underline{R}_3}{(\underline{R}_0' + \bar{R}_0'')(\bar{R}_1 + \bar{R}_2 + \underline{R}_3)} \quad .$$

The output is therefore defined by a band $(\underline{\omega}_0, \bar{\omega}_0)$ defining a 0 output and a second (distinct) band $(\underline{\omega}_1, \bar{\omega}_1)$ defining a 1 output.

Suppose now that the flipflop is to be set to a new state by applying an input signal s through a resistance r to the base of T_1. If the circuit is in the 0 state, it will be necessary to apply a signal $s_{0\to1}$ which is sufficient to cut T_1 off: If the circuit has sufficient loop gain (see Section 2.8), the flipflop will then proceed on its own toward the new state. $s_{0\to1}$ is determined by the condition that in a circuit with T_1 on and T_2 off, u is brought up to ground potential. Similarly the signal $s_{1\to0}$ required to set the flipflop to 0 is determined by the condition that in a circuit with T_1 off and T_2 on, u is brought down to ground potential. This gives:

$$s_{0\to1} = -E\left(\frac{r}{R_3}\right) + V\left(\frac{r}{R_1 + R_2}\right)$$

$$s_{1\to0} = -E\left(\frac{r(R_1 + R_2 + \mu R_3)}{R_3(R_1 + R_2)}\right) + V\left(\frac{r}{R_1 + R_2}\right) \quad .$$

Visibly $s_{0\to1} \neq s_{1\to0}$ as long as $r \neq 0$: This again corresponds to the well-known hysteresis of the flipflop. Since tolerances are not zero, there are bands $(\underline{s}_{0\to1}, \bar{s}_{0\to1})$ and $(\underline{s}_{1\to0}, \bar{s}_{1\to0})$ in which the input signals necessary to trigger the flipflop must lie. Since $s_{0\to1} > s_{1\to0}$ under practical conditions, it will be sufficient to assure that $s > \bar{s}_{0\to1}$ to trigger the 1 state and $s < \underline{s}_{1\to0}$ to trigger the 0 state.

To summarize: in order to assure triggering in a chain of flipflops, the output ω of each one must swing under the worst conditions sufficiently far to trigger the next stage. This corresponds to the following inequalities:

$$\underline{\omega}_1 \geq \bar{s}_{0\to1} = c_1 \quad \text{(say)}$$

$$\bar{\omega}_0 \leq \underline{s}_{1\to0} = c_0 \quad \text{(say)} \quad .$$

c_1 and c_0 are called the upper and lower critical level respectively. Triggering is produced by overswinging these critical levels.

By reasoning in a similar fashion, discrimination levels d_1 and d_0 could be determined such that a signal in the band (d_0, d_1) cannot possibly trigger any flipflop of the given set: The existence of this "non-trigger band" (even if it is extremely narrow) is essential if infinitely slow signals are not to cause any confusion (push-pull gating!).

Figure 20 shows the general disposition of the input and output bands of flipflops which are to be connected together.

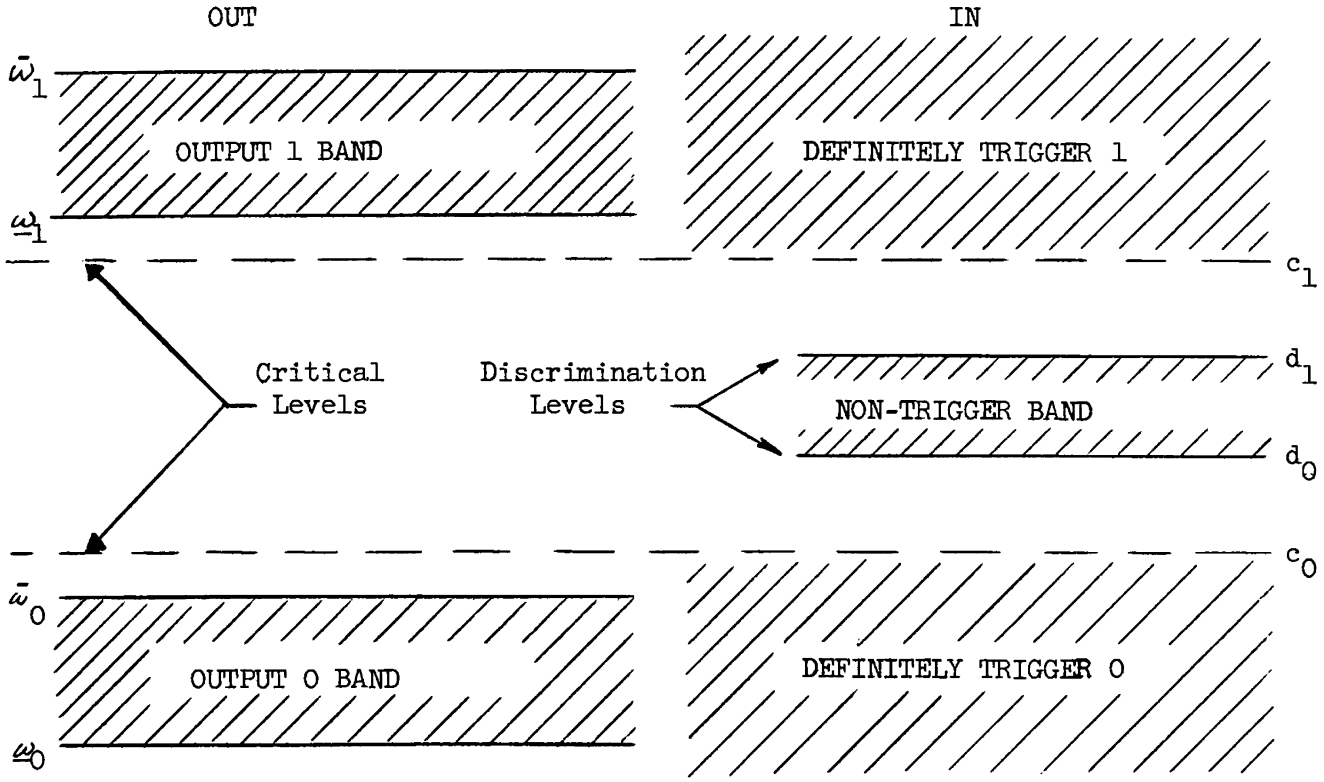


Figure 20

Bands for a "Well Disposed" Flipflop

3.4 Times and Time Tolerances

In Section 2.9 it was shown that for a flipflop model sightly simpler than that of the last section a reasonable estimate of the sum of the transition times $\tau_{0\to1} + \tau_{1\to0}$ with the calculated triggering currents $i_{0\to1}$ and $i_{1\to0}$ is

$$\tau = \tau_{0\to1} + \tau_{1\to0} = C_R(3R + 2K) + C_K(2K)$$

$$\sim 2K(C_R + C_K) \quad .$$

It stands to reason that the actually observed times will therefore lie between

$$\bar{\tau} = 2\bar{K}(\bar{C}_R + \bar{C}_K)$$

and

$$\underline{\tau} = 2\underline{K}(\underline{C}_R + \underline{C}_K) \quad .$$

It is very important to note that under degenerate conditions these times can tend towards $+\infty$. Suppose for instance that the swing in the circuit preceding the flipflop is just sufficient to furnish the required dc values of $i_{0\to1}$ or $i_{1\to0}$: Then the base of T_1 will never reach the point where regeneration sets in due to lack of charging currents for stray capacitances (C_R!) and the flip-flop will be "infinitely slow". Of course the satisfactory design of all circuits by the methods to be discussed in Sections 6.1 ff, excludes such degenerate cases. It is not excluded, however, that marginal time conditions can arise within the circuit itself under simultaneous worst drift conditions. Since no complete study has been made, it is assumed in the new Illinois computer that as long as only one resistor drifts the maximum amount (all others remaining nominal) the worst transistor gives not more than 50% increase in the characteristic times. Experiments seem to bear out this assumption fairly well.

Several characteristic times can be defined for a given circuit. In particular the following definitions are applied for the new Illinois computer:

Operation Time τ_{op}: This is defined as the average delay time of a circuit (restoring or non-restoring) i.e. the time between the moment the input signal crosses zero and the moment when the output signal crosses zero.

It should be remarked that it is essential to use the word "average": Under drift conditions the time defined could be negative, but its average value must be positive. An important property is that the operation time of a chain of elements is the sum of their individual operation times. It turns out that the operation time measured on restoring circuits is about 10 mμs for a circuit with one collector delay between IN and OUT, 20 mμs for two collector delays, etc. For a non-restoring circuit, operation times of less than 2 mμs are measured per emitter-follower-diode stage. In view of the 50% safety margin, the following rule has been established:

RULE:

1. For each collector in the signal path count 15 mμs operation time.
2. For each emitter in the signal path count 3 mμs operation time.

Rise Time τ_{rise}: This is the usual 10% to 90% rise (or fall) time observed at the output. It is only defined for restoring circuits.

Note that the latter proviso is necessary since it is nearly impossible to define such a quantity for an emitter follower: Such a circuit can rise and fall nearly arbitrarily fast (due to the big base-emitter diffusion capacitance), but needs a recovery period after each variation to regain its dc equilibrium. In the new Illinois computer this recovery time is much smaller than any rise or fall times of the restoring circuit used to drive the emitter follower and can be neglected. It should also be mentioned that restoring circuits have such recovery times, but again they are very small compared to operation times or rise times. To be more precise the following definition can be useful:

Recovery Time τ_{rec}: This is the time needed for the circuit to reach its dc-equilibrium (within a given percentage) after a fast transient.

Moving Time τ_{mv}: This is the time from the moment the input signal has gone through 10% of its variation to the moment the output signal has gone through 90% of its variation.

It is obvious that

$$\tau_{mv} = \tau_{op} + \tau_{rise}$$

and it is also clear that the quantities $\tau_{0\to1}$ and $\tau_{1\to0}$ discussed above are actually moving times.

One of the interesting properties of the new Illinois computer restoring circuits is that operation times and rise-times are nearly identical. Using the rule established in this section the estimate used in Section 1.2 results without difficulty.

A final remark concerning the measurement of operation times may not be out of place. If care is exercised to allow each circuit to work under full amplitude and an oscillating feedback chain of n_1 elements with τ_{op1} and n_2 elements with τ_{op2} is formed (there must be a phase inversion and one at least of the elements must be restoring, i.e. furnish voltage amplification), the period T of this oscillation is given by

$$2(n_1 \tau_{op1} + n_2 \tau_{op2}) = T \quad .$$

3.5 Noise

The possible sources of noise in a computer circuit are of two kinds:

1. "Physical sources" comprising
   a) "Thermal noise" ("white noise"), due to random charge motion in resistances,
   b) "Shot noise", due to fluctuation of emission in junctions,
   c) "Semiconductor noise" (1/f noise) due to surface leakage on the semiconductor.
2. "Circuit sources" comprising
   a) "Ohmic interaction noise", due to common impedances (surge impedance of power busses)
   b) "Capacitive interaction noise", due to capacitive coupling
   c) "Inductive interaction noise", due to inductive coupling.

By examining the theoretical basis of each one of them and comparing the new computer circuits to general cases, it becomes possible to eliminate all but two of these sources. Take, for example, the thermal noise at the input to a switching amplifier; the mean square amplitude is given by

$$e_T^2 = 4kTR\Delta f$$

(k = Boltzmann's constant, T = temperature, R = output resistance of last stage, Δf = bandwidth). For typical new computer circuitry R = 1000Ω, f = 10^8 cycles and $e_T \sim 26$ μv rms. Even when amplified 200 times by the switching amplifier only a total of 6 mv rms is obtained: e_T can be neglected.

The formula for white noise in a junction is

$$e_s^2 = 2qI^*r^2\Delta f$$

where $I^* = I + 2I_0$ (I = current, I_0 = saturation current)

$$r = \frac{kT}{q} \cdot \frac{1}{I + I_0}$$ = differential diode resistance.

For usual values of I, I_0 and $\Delta f = 10^8$ cycles voltages of the order of 1 μv are obtained.

The semiconductor noise is often 20 db or more above the termal level and could under some circumstances become observable at the collector. Since collectors are bumped (as well as all emitter-follower outputs), it is not to be feared that such noise could be presented to an amplifying stage. Its value can be approximately calculated from

$$e_{sc}^2 = \frac{K}{R^2} \cdot \frac{V^2 r \Delta f}{f} \qquad \left(K = \frac{\text{constant}}{\text{volume}}\right)$$

where R = surface leakage resistance
V = voltage across junction
r = differential resistance of junction.

The ohmic interaction noise is perhaps the most serious in semiconductor circuits. Suppose that a bank of 50 flipflops with a collector current varying between 0 and 20 ma is connected to a bus and changes state. Then a surge impedance of even 1Ω would give a 1v variation at the collectors and this may be more than the stability of circuits allows. In the new Illinois computer the coupling through common impedances has been minimized by using "constant current" emitters, voltage dividers and collectors (see Section 1.7): Only a 20-30% load variation is expected on busses under transient conditions. Furthermore RC filters with a time constant (1 μs) which is long compared to rise and fall times have been connected between the busses and the resistors furnishing the source or sink action. Interaction at the input to the actual circuits is then reduced to less than 10% of the value calculated above.

Another problem (and a more severe one) arises in busses supplying the low voltage bumps (+2.2v, -3.1v). Current requirements are somewhat lower, but to compensate extreme care has to be exerted to guarantee less than .1v variation at the input to the bumping diodes. This problem defied practical solutions until it was realized that the only economic solution was to create the bumping voltages on the spot by the use of stabistors (fed through resistors from +25v and -50v respectively). Their inherently high junction capacitance effectively provides a very useful filtering action and no difficulty with either long term drift nor spikes during transients has been encountered.

The capacitive interaction is the only remaining source of worry, since very little inductive coupling occurs in a 3-dimensional layout of circuits such as that proposed for the new Illinois computer. Here little quantitative information is available. All that can be said is that for the critical points (e.g. the base of a switching input transistor) even a 10 μμf stray capacitance between a collector swinging through 10v and this point cannot transmit enough energy to turn the transistor on when it is off or vice-versa.

3.6 Transients due to Enhancement Currents

Consider the switching circuit in Figure 21 which is similar to Figure 10 in Section 2.5. Instead of discussing the theoretical aspects of the transition of

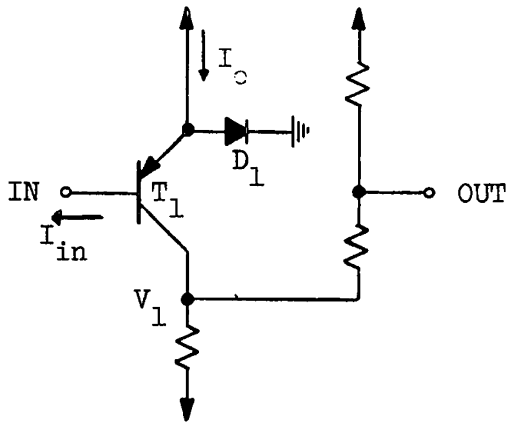


Figure 21
Switching Stage

such a circuit from one state to another, some of the (experimental) finer points must now be treated. In particular the influence of so-called "enhancement currents" in the switching diodes will be considered. This "enhancement current" is simply due to the fact that the diode (as explained in Section 2.5) is a reservoir of charges after having conducted in the forward direction. As a consequence D_1 is actually a short circuit to ground when T_1 first starts conducting and can therefore push into the emitter currents of considerable magnitude ($>I_0$). As a result, both the input current and the collector voltage

will exhibit peak excursions different from those expected in the simpler theories. Figure 22 shows a sketch of the input and collector waveforms as they are actually observed. The figure has been corrected to account for phenomena caused by the scope input circuits.

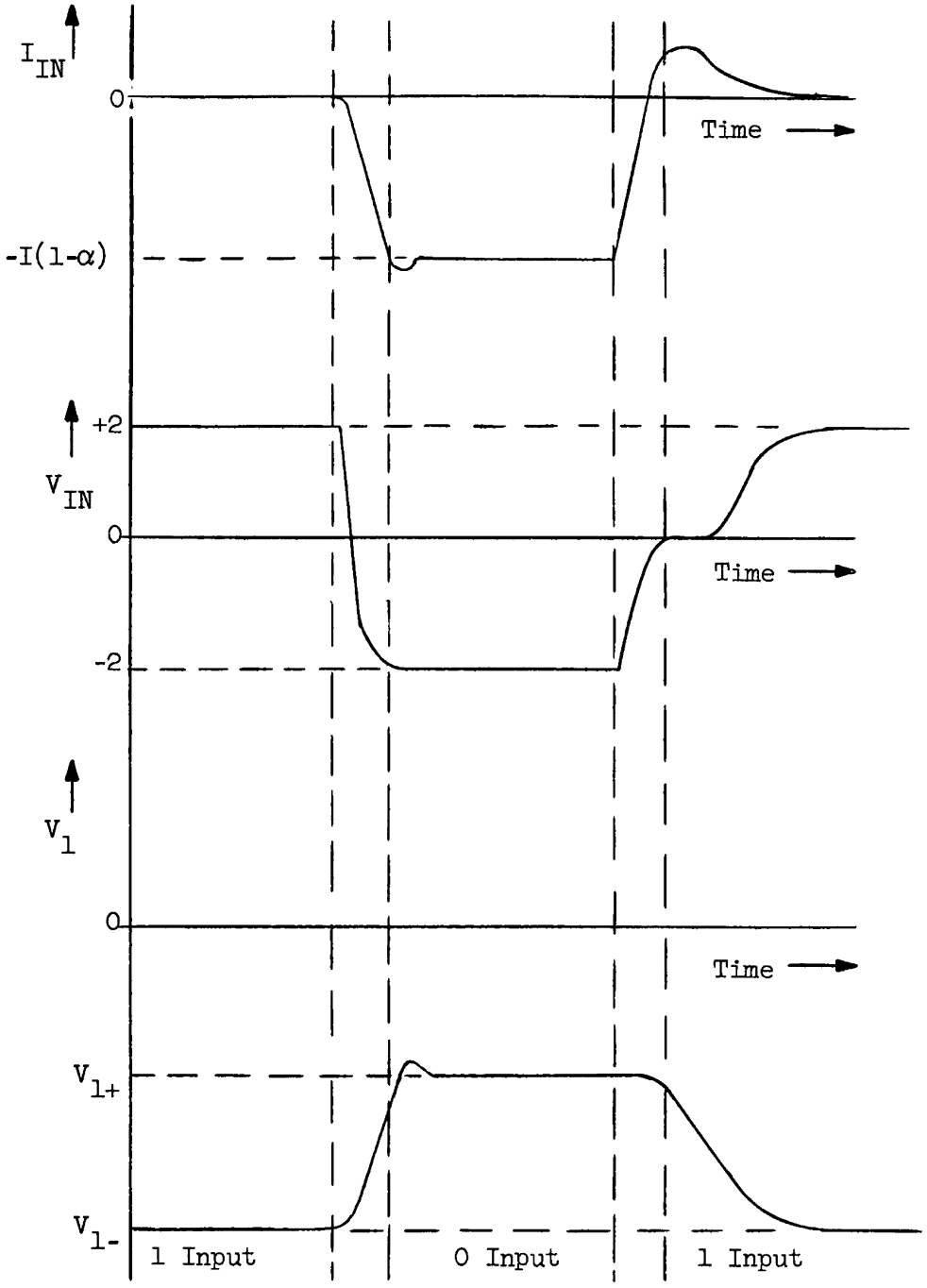
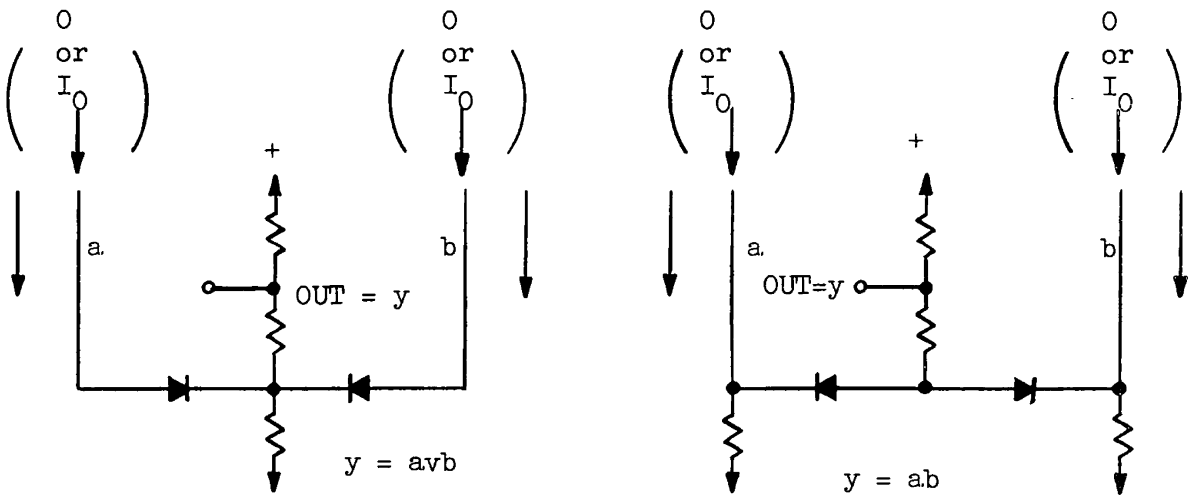


Figure 22

Waveforms in a Typical Switching Stage

Great care must be taken when collector logic is used (e.g. in the EXCLUSIVE OR, see Section 5.2.5) to make sure that enhancement currents do not produce output spikes giving rise to "false" transient signals. An example will show the problem: Compare Layout I and Layout II in Figure 23 corresponding to a "collector OR" and a "collector AND", the collectors being those of a switching input stage as discussed above. Suppose that a and b are normally in phase opposition ($a = x$, $b = \bar{x}$) and that Layout I is used to detect that they are not "ON" simultaneously be examining the output voltage at y and making sure that it does not exceed a certain value. The circuit will probably give false indications during a transition of x from $0 \rightarrow 1$ or from $1 \rightarrow 0$ since the sum of the collector currents may exceed $2I_0$ due to the enhancement current.



Layout I Layout II

Figure 23

Two Layouts for Collector Logic

Layout II makes sure of the exclusiveness of the signals by ascertaining that y is only dragged down by one collector at a time. Visibly an enhancement current could only cut off the second diode and no damage would be done.

4. SPECIFIC CIRCUIT TRICKS

4.1 Last Moving Points

In Section 1.3 it was stated that a desirable circuit property, in certain cases, is the existence of an output terminal which is the last moving point in the circuit. In practice this can be approximated in a number of ways and this section will be devoted to a description of the underlying principles.

Consider, for example, the circuit of Figure 23. Evidently the output terminal here is anything but a last moving point (it is in fact a first moving point!), i.e., an input signal produces an immediate output, even if T_1 is dead. The use of a double divider (Figure 24)--see the discussion in Section 5.3--helps somewhat in this respect since the amplifying transistor T_1 has to react before an output change occurs. However, unless the output branch of the divider attenuates more than the inside branch, the occurrence of an output change does not indicate that the regenerative loop is closed (this assumes threshold detection and equal time delays in the two branches).

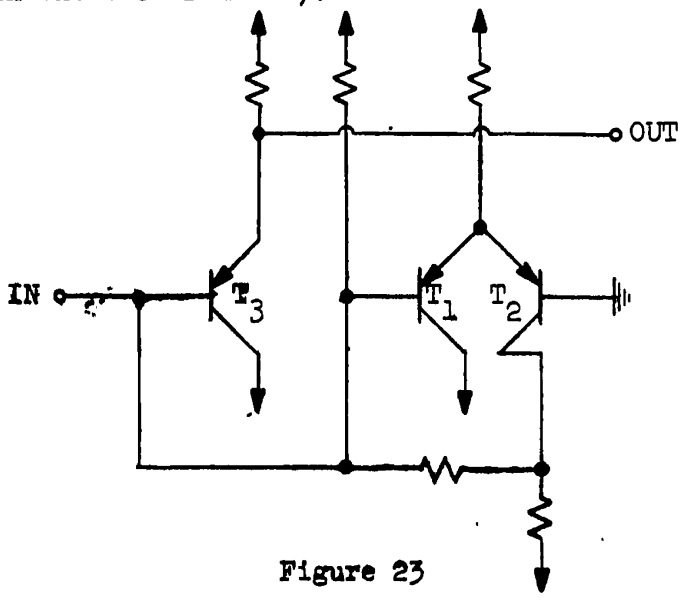


Figure 23
Single Divider Asymmetric Flipflop

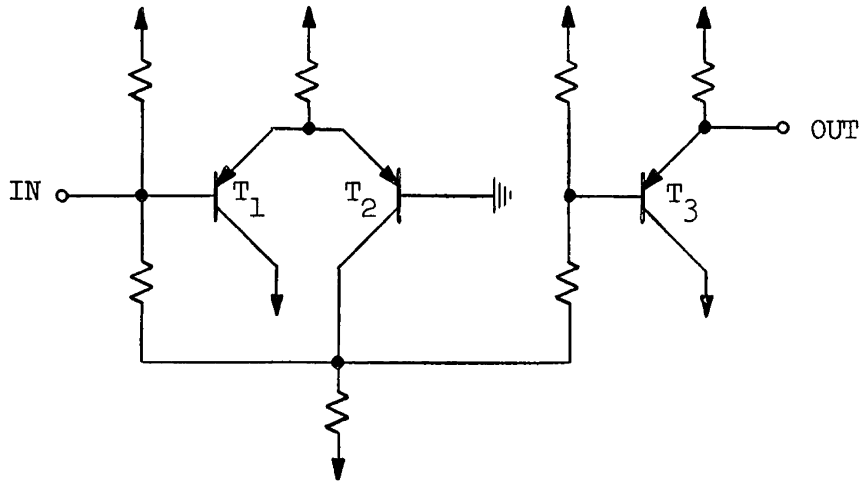


Figure 24

Double Divider Asymmetric Flipflop

Now a better indication can be obtained by adding circuitry to detect when the feedback loop is closed, this circuitry itself providing the output signal. The basic idea is shown in Figure 25.

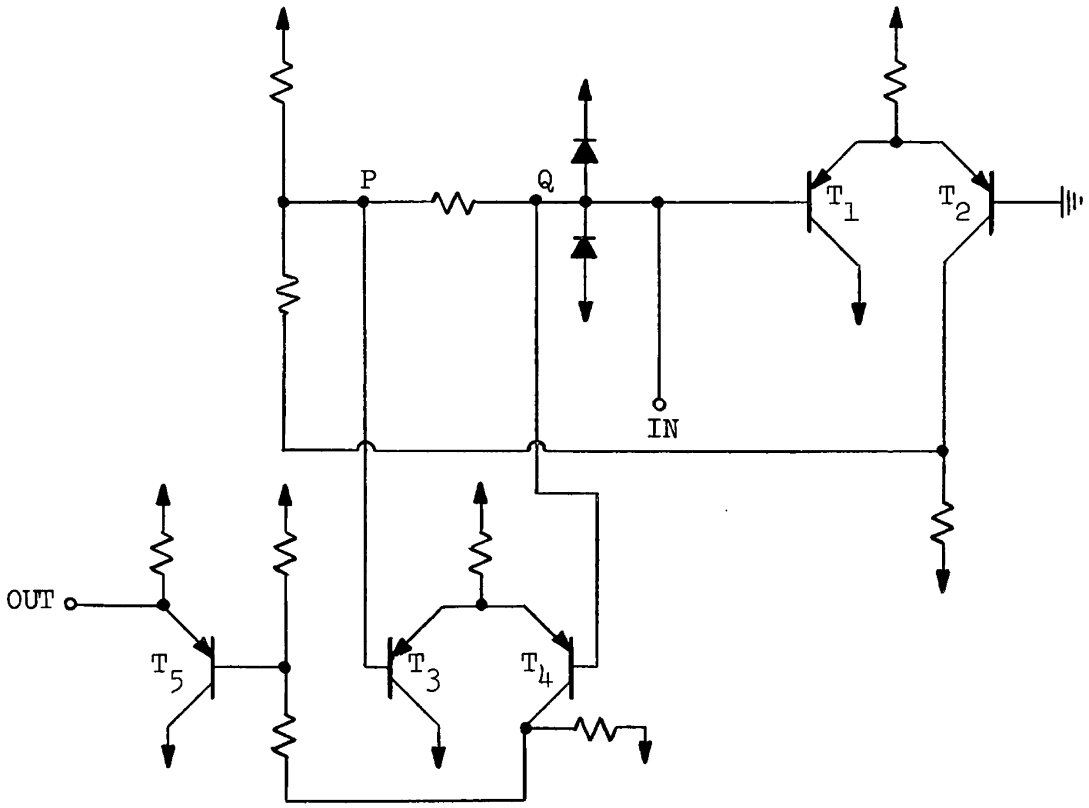


Figure 25

True Last Moving Point Flipflop

The difference amplifier T_3 T_4 yields an output of similar sign to the input only after the feedback loop is closed, as an analysis of the transitions of the circuit shows easily. Note that it is essential for point P to overswing the (bumped) point Q and that an input signal different from that held in the circuit will only increase the voltage fed to the difference amplifier as long as the flipflop has not "flipped." The output is in this sense a truly last moving point.

4.2 DC Compensation

When carrying a forward current of a few milliamps (or more) diodes and transistor emitter junctions exhibit a voltage drop of about 0.5v. Signals which pass through emitter followers and diodes are, therefore, subjected to a dc level shift of about 0.5v. In the new computer circuits it is usual to compensate for this effect approximately by using additional diodes back to back with the logic (or E.F.) diodes and carrying a current of similar magnitude. As an example consider the AND circuit of Section 5.1.2 which is reproduced below in outline. Here D_3 and D_4 are used for dc compensation and it is evident that their drop

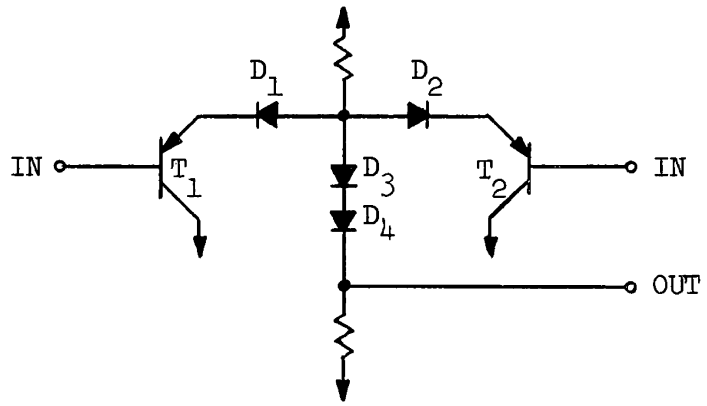


Figure 26

DC Compensation in an AND Circuit

can be adjusted to be approximately that of the logic diode (D_1 or D_2) plus the emitter (of T_1 or T_2), so that the "spread" or maximum overall

dc level shift is nearly equalized in the two directions for a given average loading on OUT.

4.3 Breaking into Feedback Loops

The realization of a flipflop integral with its gate is a problem of considerable interest. It is conventional to regard a flipflop as a 2-state regenerative amplifier which is set or reset by forcing it into one or the other of its stable states. A gate of some sort is usually required to enable the connection or disconnection of the flipflop from its information source.

Imagine now that the regenerative loop of a flipflop is broken at some appropriate point (see Figure 27). The flipflop will either take on some intermediate state or, more likely, move on to some definite one of its terminal states. For example, breaking the loop of the circuit in Figure 27 at point P will result in the state T_1 OFF, T_2 ON. The desired

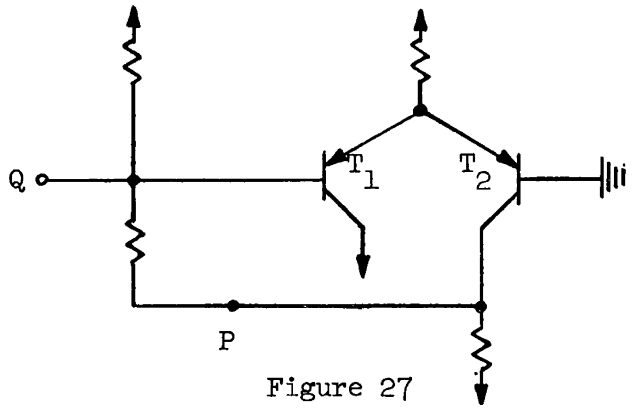


Figure 27

Breaking the Feedback Loop of an Asymmetric Flipflop

signal could now be impressed on the point Q and, after a suitable delay, the points P could be rejoined to "trap" the state impressed in the flip-flop. It is the function of the gate to open and close the points P and Q. In effect the feedback signal is replaced with the input signal for the gate time. A circuit using this principle is the F-element which is discussed in Section 5.3.2. As will be described there the opening and closing of the feedback path is accomplished by reverse or forward

biasing diodes in the feedback loop of what is essentially an asymmetrical flipflop. The obvious advantages of the integrated flipflop-gate complex is that both the gating and the information signal can be injected into (very sensitive) switching amplifiers, i.e. the signal at the input to such a design can be more degenerated than in the "separate gate" design.

4.4 Push-Pull Gating

An asynchronous shifting register usually contains two registers (call them A and B for illustration). Information is shifted by shuttling back and forth between A and B with a stagger on one (or both) of the paths, as shown in Figure 28. The B driver is normally energized only after the A driver is de-energized

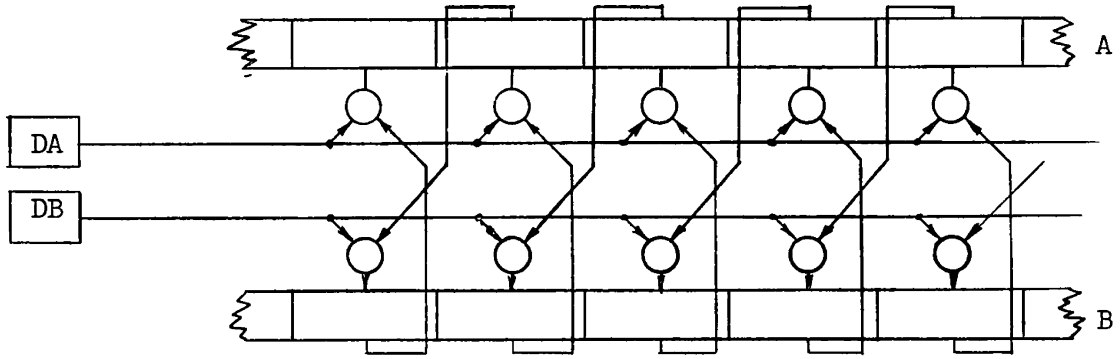


Figure 28

Shifting Register

and vice versa. Timing waveforms are shown in Figure 29 for a single up-down shift. Now the delay between energizing the A and B drivers can be reduced by operating the drivers with push-pull signals so that the rise of one driver coincides with the fall of the other. To avoid possible dangerous overlap due to unequal time delays in the two drivers, the push pull signal is created symmetrically in a single driver. Section 5.9.9 describes this push-pull driver.

Another interesting possibility is to use for the A-rank and the B-rank flipflops such that those in A gate in on 1 and those in B on 0. A single wire swinging up and down can then transmit the "shuttling signals." It can easily be seen that F-elements can easily be modified to gate in on "0". Such a system could be called a "one wire push-pull system."

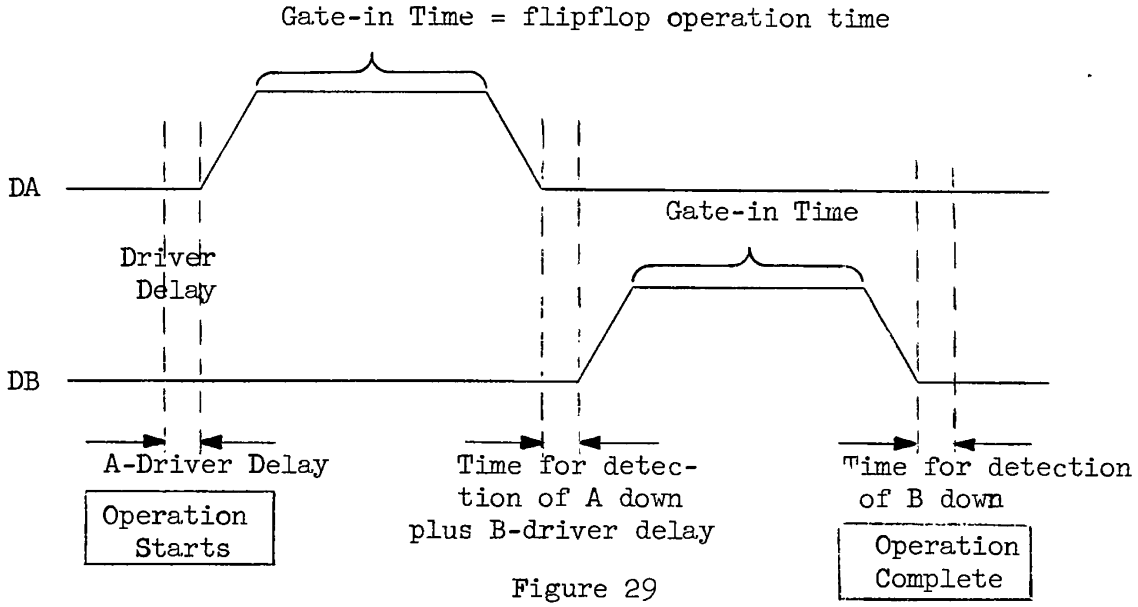


Figure 29

Delays in a 2-Driver System

4.5 Flow Gating

This is a somewhat unusual principle and will be described in fairly complete detail.

Consider a Schmitt trigger circuit using a single-supply voltage only. The input and output of such a circuit (which can be in either one of its states) can then exist at voltage levels which depend linearly on the supply voltage. In order to gate from one such circuit to another, a simple diode connection is used and the average potential of the two circuit is made different in such a way that information flows through the diodes. It turns out that the clearing, which has to precede the setting, can be accomplished automatically in the process of changing the average potential. Since information is gated by making it flow down a potential gradient (created by a gate signal which controls the supply voltage), the system is called "flow-gating". Figure 30 gives the circuit diagram of the device.

The theory is as follows. For a fixed -E, T_0 acts like a grounded-base amplifier (base return voltage = $-ER_5 / (R_4 + R_5)$ if $\alpha = 1$) and T_1 acts like an emitter follower. Note that OUT is in phase with the base of T_0 which is used as a triggering point. It is seen, therefore, that T_0

and T_1 together act like a Schmitt trigger. The base of T_1 is tied to a bias $-u_0$ through a diode and the circuit values are chosen in such a way that OUT is above $-u_0$ in the 1 state and below in the 0 state. (Note that the left-hand diode does not conduct as long as the supply voltage is -E.)

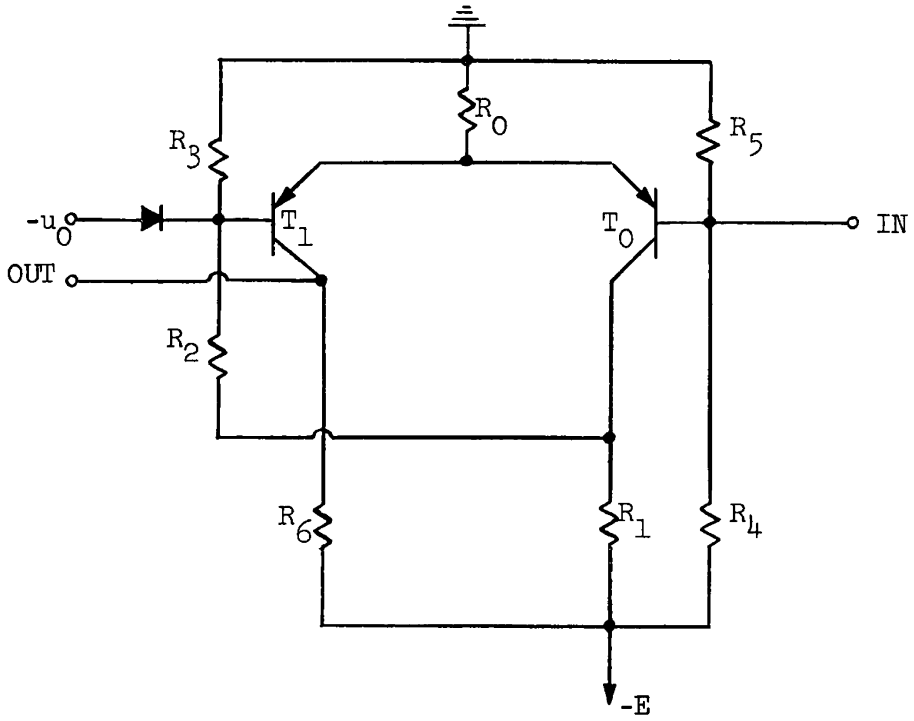


Figure 30

Layout of a Flow-Gating Flipflop

Suppose now that we connect several flipflops of the kind just described in a linear chain (see Figure 31), using diodes with their cathodes tied to IN. As long as the three supply voltages $-E_1$, $-E_2$ and $-E_3$ are equal to their normal value -E, the output is so much more negative (both in the 0 state and in the 1 state) that all diodes are cut off, allowing each flipflop to retain its state uninfluenced by neighboring units.

Now lower the supply of FF_2 from -E to -E'. This is certainly not going to influence FF_1 to the left since the connecting diode is cut off by an even greater margin than before. IN_2, however, will become more and more negative in this process and the moment will come (this depends on the judicious choice of -E') when its average value (determined by

-E', R_4 and R_5) is equal to $-u_0$, the bias applied to the opposite base through a diode. As mentioned before, circuit values are chosen such that OUT is above $-u_0$ in the 1 state, and below in the 0 state for a supply voltage -E. This means that if OUT_3 indicates a 1, T_0 is switched off, while if it indicates a 0, the bias diode switches T_1 off (i.e., T_0 on). Once this operation is accomplished, the supply voltage is brought back to its normal value, -E. One can easily verify that during this transition, the state impressed at -E' is conserved and thus "trapped" when all supply voltages are equal again.

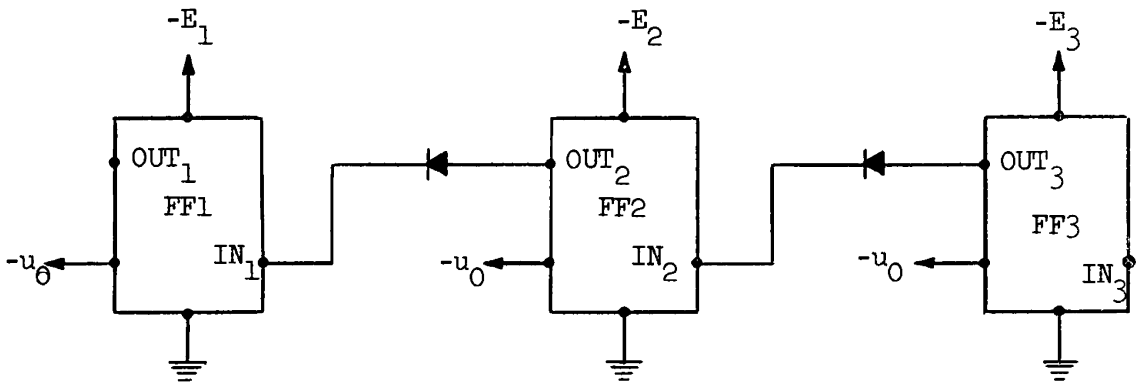


Figure 31

Gating with a Flow-Gating Flipflop

It turns out that the collector supply of T_1 need not be tied to -E. This not only diminishes the current requirements for gating by a considerable factor, but also allows us to control the gating out of a flipflop without modifying the supply voltage of the flipflop to be gated into. It can also be shown that by introducing a bumping diode into the collector of T_1, we can have a constant output from a flipflop (whether it is in the 0 or the 1 state) independently of whether it is being gated into or whether it is in its normal supply-voltage range.

A flow gating memory is contemplated for the provision of fast storage of some 16 words. It is expected that about 150 mμs access time will be attained.

4.6. Local Creation of Bumping Voltages (See Section 3.5)

A serious problem in large scale circuit engineering is concerned with the noise coupling between sensitive nodes in different circuits. Reference to any drawing for the new computer restoring circuits will confirm that the +2.2v and -3.1v bumping supply voltages serve to connect together such sensitive nodes and the figure below illustrates how serious this coupling could become.

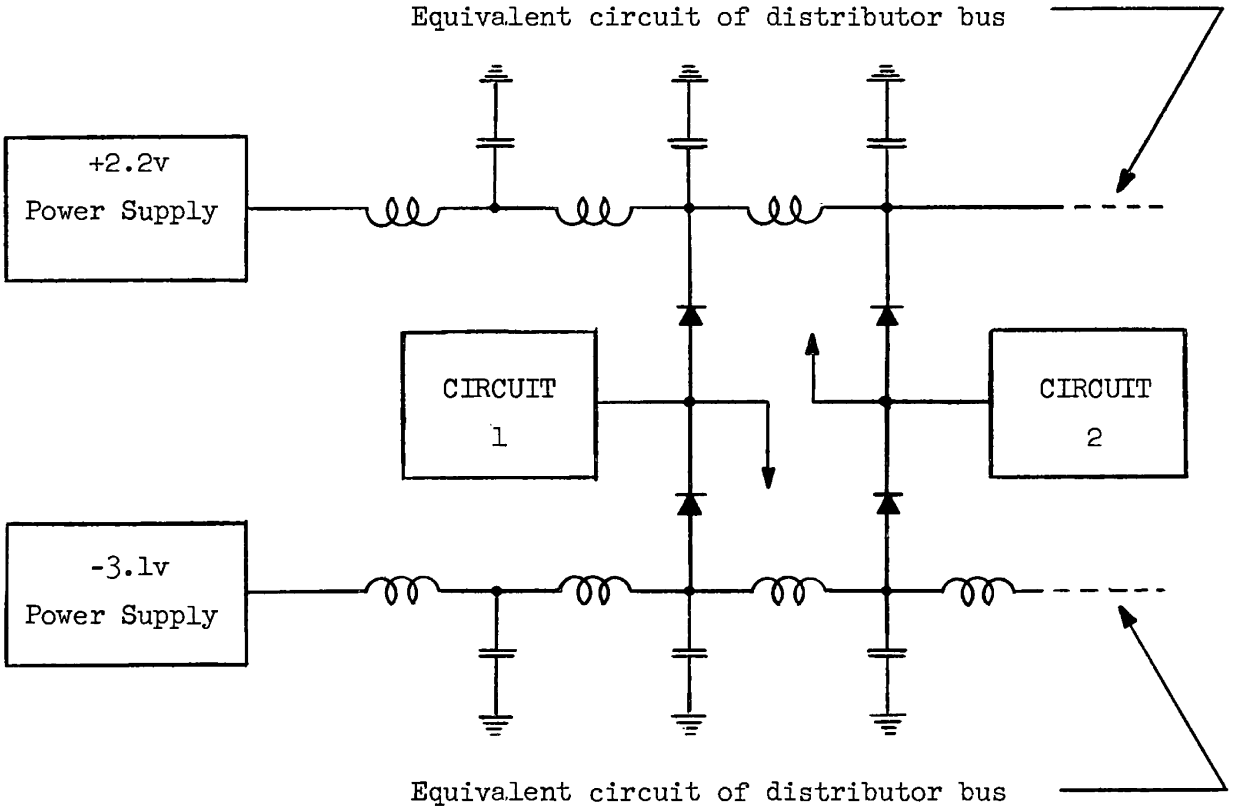


Figure 32

Interaction Noise on Low Voltage Busses

The distributed inductance of the distribution bus effectively isolates the power supply from transient disturbances produced by, say circuit 1, but may not isolate (because of its proximity) circuit 2 from the same disturbance. This problem has been solved for the new computer by providing local circuits to generate the

bumping voltages for each and every circuit. The simple circuits used are shown in Figure 33.

Figure 33
Creation of Bumping Voltages by Stabistors

5. DESCRIPTION OF THE NEW COMPUTER CIRCUITS

5.1 Non-Restoring Circuits

Non-restoring circuits have a gain less than unity and a certain dc drift between the input and output terminals. Statements regarding these two properties are collected into the hybrid statement, "maximum dc level shift" which is quoted for the two cases, output positive ("1") and output negative ("0"). The dc input current varies between 0 and -1.2 ma, depending on the transistor alphas.

5.1.1 OR Circuit

The OR circuit, see Figure 34, is the simplest of all basic circuits in the set and will be described first. It consists of a pair of emitter followers feeding a diode OR circuit. By the proper choice of R_2, the level shift in each emitter follower is compensated, approximately, by the drop in the corresponding OR diode.

Fan-out	Max dc $\pm$	Level $\mp$ Shift
1	0.135v	0.130v
2	0.135v	0.160v
3	0.135v	0.193v

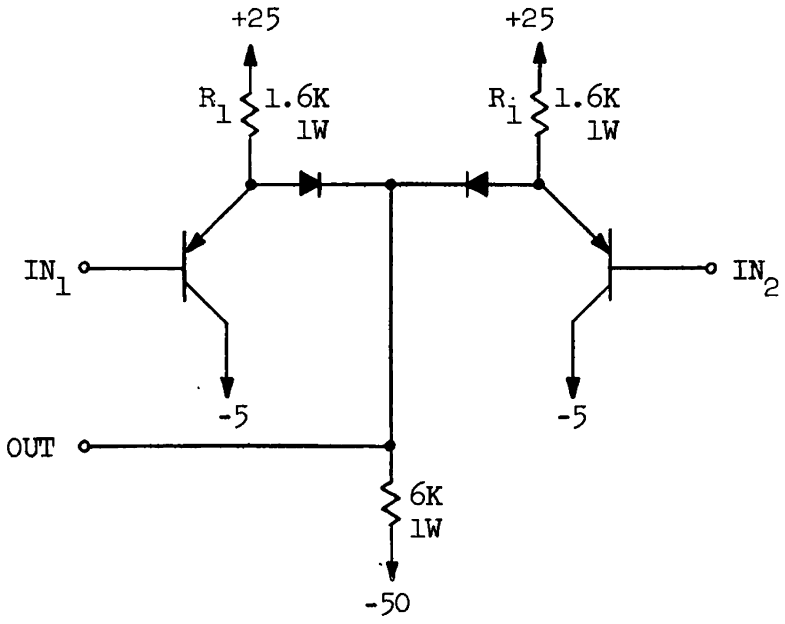


Figure 34

OR Circuit (This Is #S-855)

5.1.2. AND Circuit

Although, in principle, the AND function may be formed very simply using the emitter base junctions as the AND diodes (as shown in Figure 35), this method could not be used because of the low (4.5v) V_{EB} reverse rating

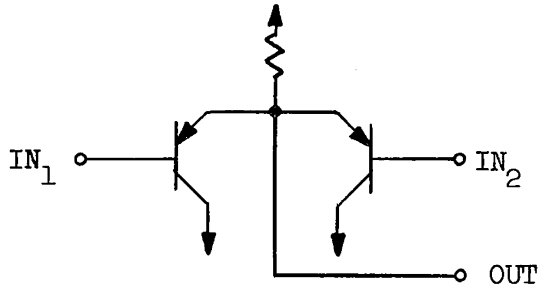


Figure 35
Simple AND Circuit

of the transistors used. Diodes in series with each emitter were provided for this reason, and after addition of the level shifting diodes D_3, D_4, and resistor R_2, the circuit became as shown in Figure 36.

Fan-out	Max dc +	Level Shift -
1	0.250v	0.160v
2	0.250v	0.220v
3	0.250v	0.290v

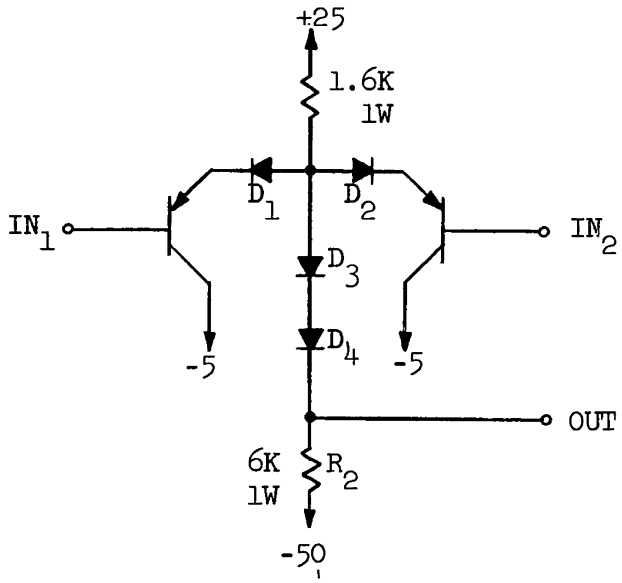


Figure 36
AND Circuit (This Is #S-856)

5.1.3 AND-OR Sequence

Sequences of AND-OR, which occur frequently in logical circuits, may be obtained for no additional expense by using the level shifting diodes of the AND circuits (D_3, D_4) as the OR diodes. A simple AND-OR sequence is shown in Figure 37.

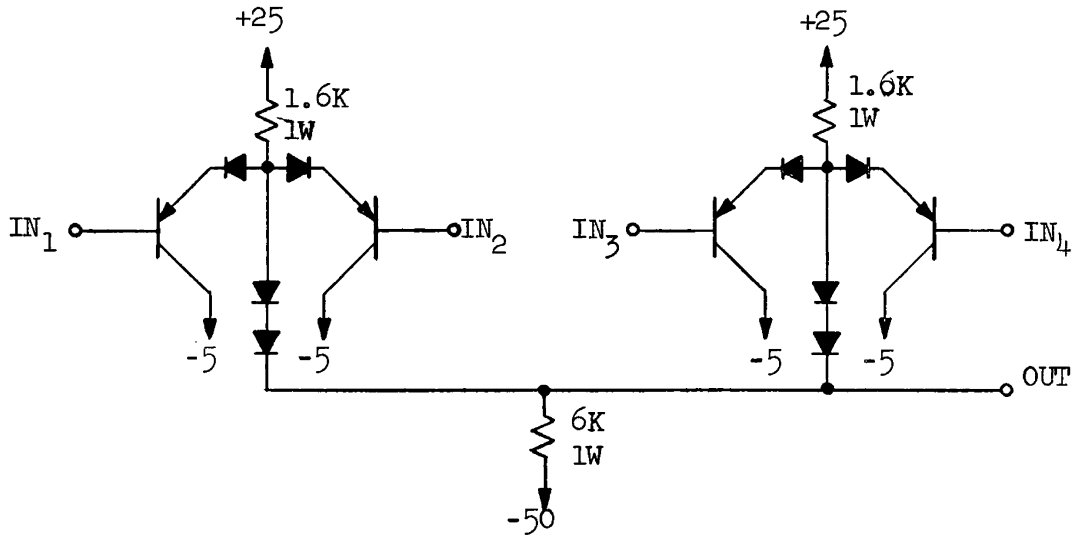


Figure 37
AND-OR Complex (This is S-861)

5.1.4 More Complex Circuits

With suitable precautions regarding transistor dissipation and input loading, it is possible to drive more than one diode circuit (AND or OR) with each emitter follower. Simple rules have been formulated to enable the assembly of large diode-transistor matrices (e.g., the half-adder shown in Figure 38, which uses push-pull signals).

5.2. Restoring Circuits

Restoring circuits have almost complete isolation between input and output terminals and input and output conditions and therefore quoted

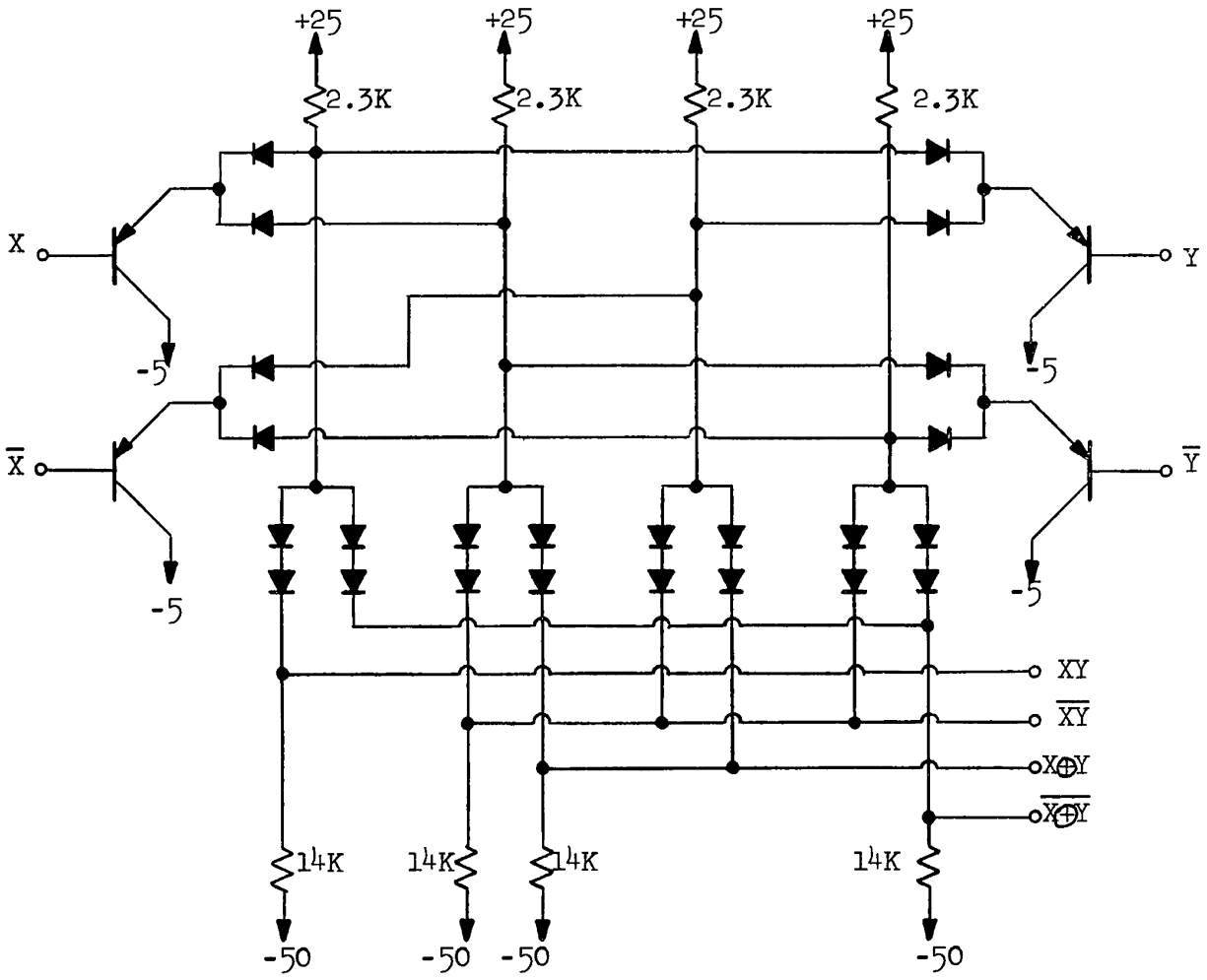


Figure 38

Half-Adder (This is M-857)

separately. ± 0.6 volts input to any switching circuit is sufficient to fully energize the circuit. The maximum dc input current is -1.2 ma (transistor on) or 0 (transistor off), but a substantial overcurrent is normally allowed to charge the Miller and base-diffusion capacitances during transitions [typically -1.5 ma (ON) and +1.5 ma (OFF)]. Output levels range between +2.5 and +3.2 volts for a "1" and between -2.5 and -3.2 volts for a "0", and any single output can feed up to 5 standard inputs.

5.2.1. NOT Circuit

The NOT circuit illustrates many of the special features of the new computer restoring circuits and is the simplest kind of restoring circuit used. Transistor T_1 has a "long-tailed" (i.e., constant current) emitter supply to furnish a current I, which is substantially independent of transistor and input source variations and may be considered very nearly constant. This current I is routed through the diode D_1 or the transistor T_1 according to the input polarity; an input of +0.6 volts ensures that all the current passes through the diode, and an input of -0.6 volts ensures that it all passes through the transistor. The collector of T_1 therefore delivers an "all or nothing" current, namely αI or 0, into the divider formed by R_1, R_2, R_3, which in turn feeds the output emitter follower T_2. The diode D_2 prevents T_1 from entering the saturation region and diodes D_3, D_4 establish the restored output levels. The emitter follower climb up in T_2 is responsible for the use of non-symmetrical bumping voltages for D_3, D_4. The design problem consisted essentially of

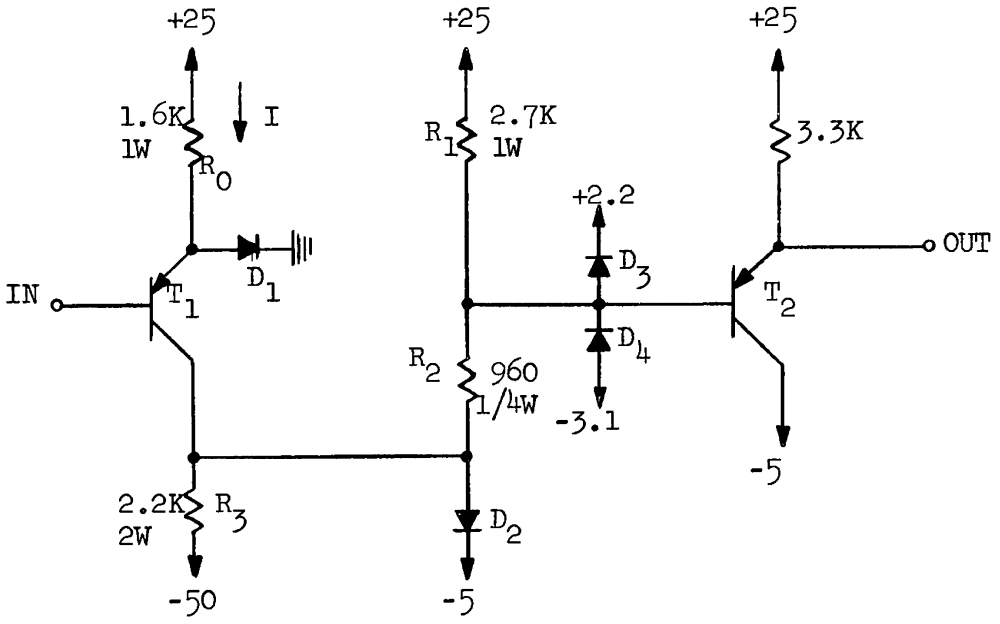


Figure 39
NOT Circuit (This Is # S-852)

choosing a divider design that provided the required output swing and load current. I was established from the minimum allowable resistor R_0, this being set by the maximum dc input current of -1.2mA. SINDY was used to obtain a suitable divider and 1206 was used to verify the circuit as a whole under all tolerance conditions.

Operation times of about 12mμs have been observed for the NOT circuit and it has become the yardstick by which most restoring circuits are evaluated. Many features of the NOT circuit are common to all types of restoring circuits; e.g., all switching input transistors have a long-tailed emitter supply to establish a constant current source, all outputs are taken from emitter followers and the bumped output levels are established on the base of each such emitter follower, all collectors carrying signals are bumped to prevent saturation.

5.2.2 LEVEL RESTORER

By substituting a difference amplifier (or "long-tailed pair") for the transistor-diode combination as the input stage, both phases of the input signal can be obtained. Figure 40 shows an arrangement which provides an output signal in-phase with the input. This is called a LEVEL RESTORER because it accepts a degenerated input signal (± 0.6v is sufficient) and delivers a restandardized output of the same sign. Operationally it is similar to the NOT circuit, and the same component values are used throughout.

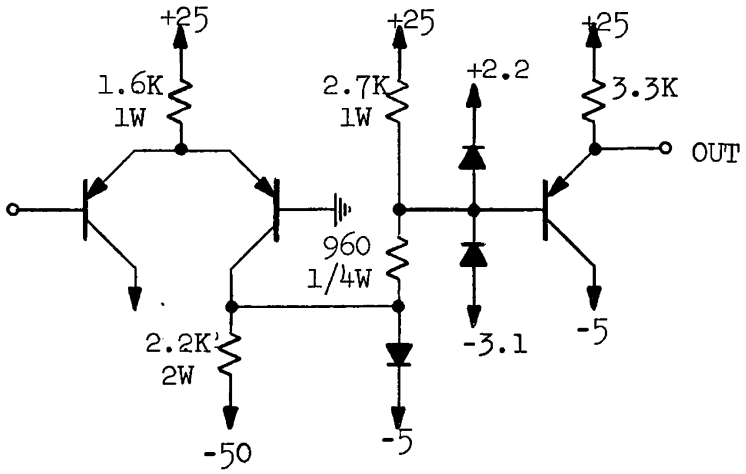


Figure 40
Level Restorer (This is #S-877)

5.2.3 Restoring AND

By paralleling input transistors as shown in Figure 41, the LEVEL RESTORER of Figure 40 becomes a restoring AND circuit, with no other circuit changes being required. That this is the case is easily seen by writing down the input conditions which cause T_3 to conduct or not conduct:

V_{IN1}	V_{IN2}	T_3
-	-	OFF
-	+	OFF
+	-	OFF
+	+	ON

Several input transistors may be paralleled, to form a multi-input AND, the total number of inputs being limited only by the transistor reverse characteristics and capacitive loading. This total is estimated to be 5.

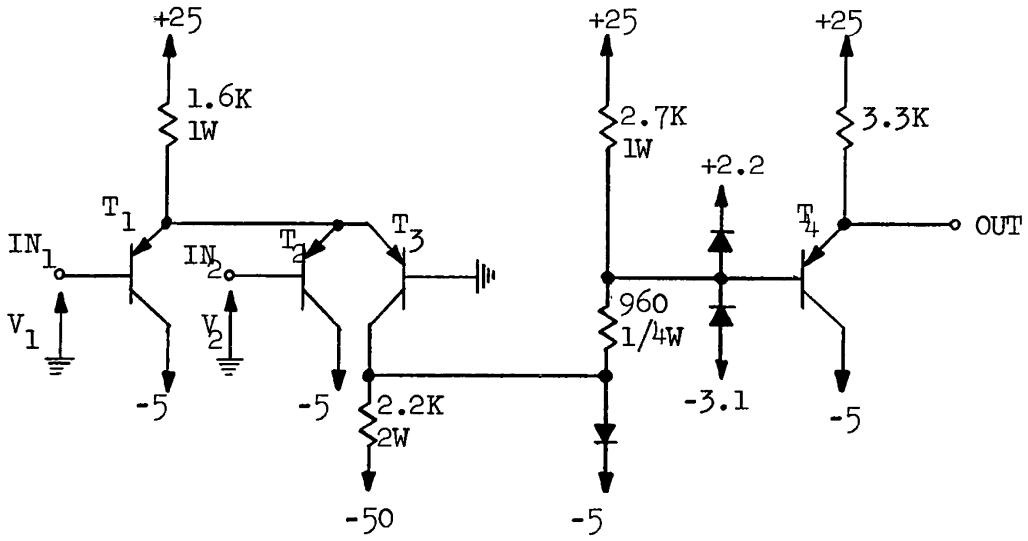


Figure 41

Restoring AND (This Is S-860)

Similarly, paralleling input transistors to the NOT circuit of Figure 39, leads to the

5.2.4 Restoring AND-NOT Circuit

This circuit is shown in Figure 42.

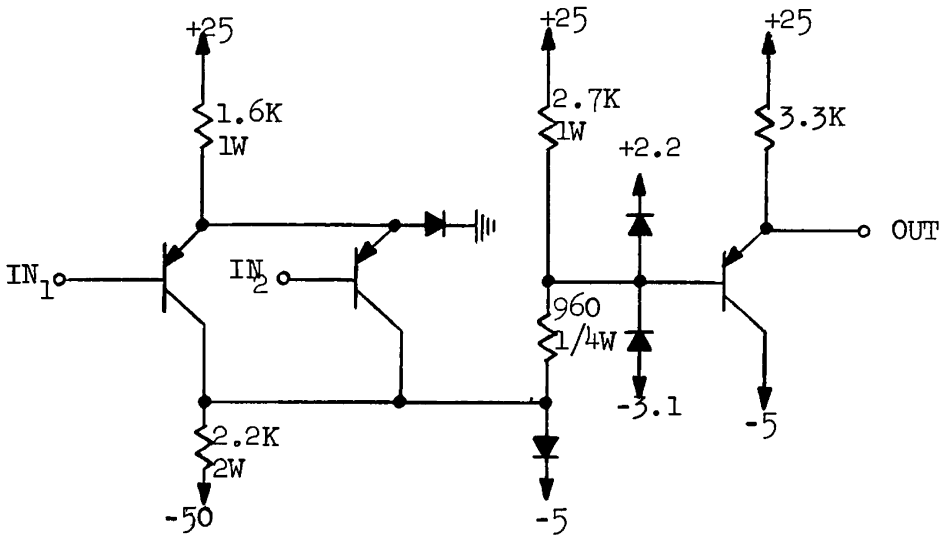


Figure 42
Restoring AND-NOT (This Is S-859)

5.2.5. Restoring EXCLUSIVE-OR:

This is a slightly more complex circuit and the general techniques adopted will be explained first. Consider firstly two switching transistors whose collectors feed a common load (Figure 43). If each transistor delivers a current αI or 0 (transistor ON or OFF), then suitable choices for R can be made to yield a voltage on the common node corresponding to either the sum (OR) or product (AND) of the currents I_1, I_2. Such a technique is known as analogue addition. Conversion of the analogue voltage to a digital signal requires the establishment of a threshold external to the system, such that voltages above the threshold are interpreted as "1" and voltages below are interpreted as "0". Now this threshold is a somewhat narrow and badly defined band for the AND since it is a critical function of I, which is subject to large tolerance variations. On the other hand, the corresponding threshold for the OR formation is a broad, well-defined band almost independent of fluctuations in I, since the output is either at $V(I_1 = I_2 = 0)$ or bumped at V_1 $(I_1 \vee I_2 \neq 0)$.

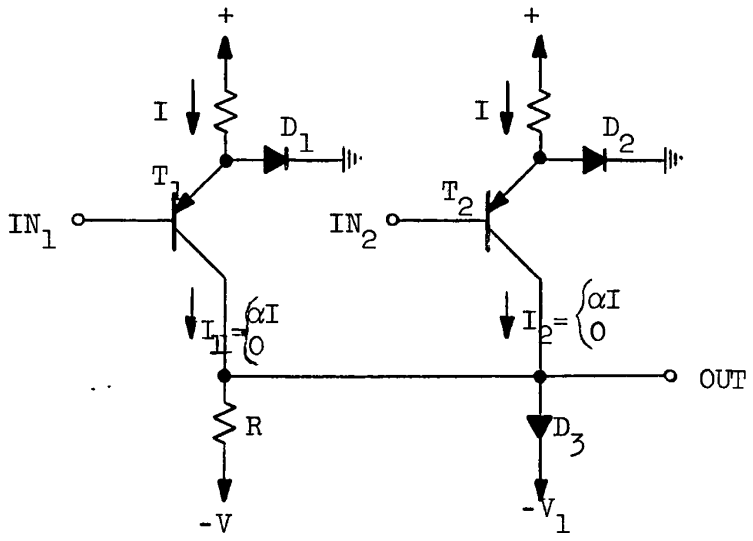


Figure 43

Analogue Addition Illustration

Consider now the exclusive-or function and its two equivalent canonical expressions:

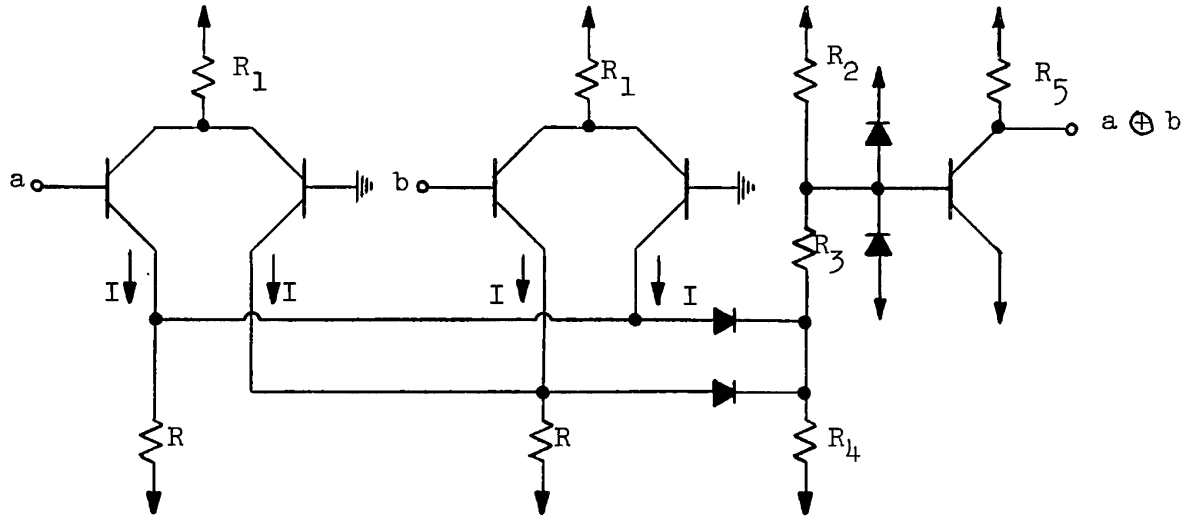
I. $a \oplus b = a\bar{b} \vee \bar{a}\bar{b} = x \vee y$ say

II. $a \oplus b = (a \vee b)(\bar{a} \vee \bar{b}) = x' y'$ say

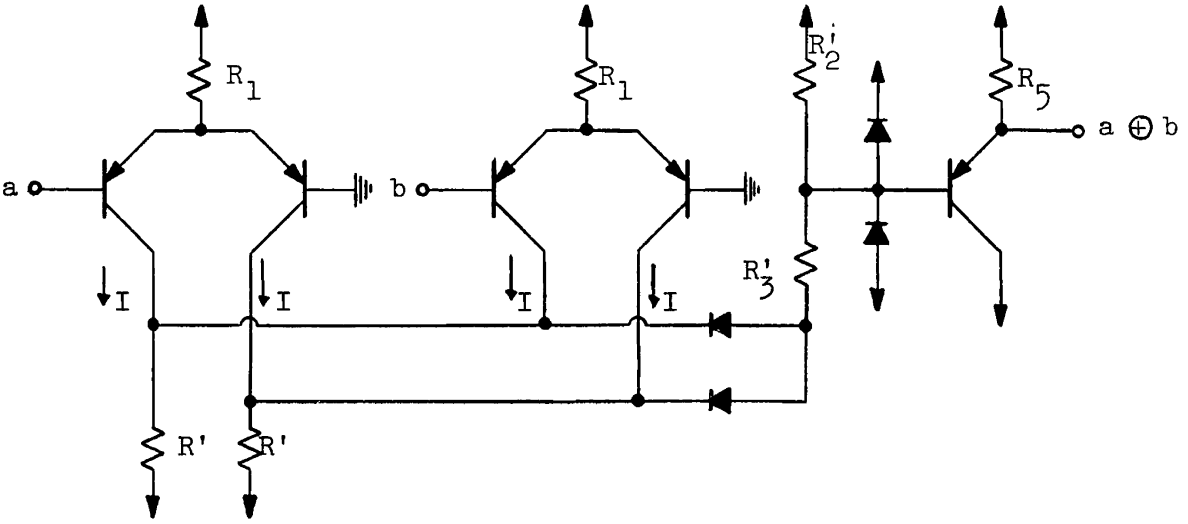
These expressions suggest directly the formation of x, y (or x', y') by analogue addition, both phases of the inputs a, b being formed with difference amplifiers. Realizations of the EXCLUSIVE-OR circuit by both methods I and II are shown in Figure 44. The second of these was chosen for a number of reasons:

1. The transistor dissipations are lower for the second than for the first since a conducting transistor has always only a small voltage (about 7 volts) between its base and collector;
2. The output divider can be used "free of charge" to pull up the AND circuit, whereas an additional resistor, R_4, is needed to pull down the OR circuit of the first arrangement;.

3. Any transient in I due, say, to enhancement current in the emitter-base diodes, cannot be propagated to the output terminals.



Method I



Method II

Figure 44

Two Possible Topologies for the F-Element

Design of the final EXCLUSIVE-OR (Figure 45) was undertaken with the use of SINDY, 1206 and a small amount of hand calculation. The small resistors, r (20Ω) in the collectors of the difference amplifiers are to ensure a good division of current into the bumping diodes.

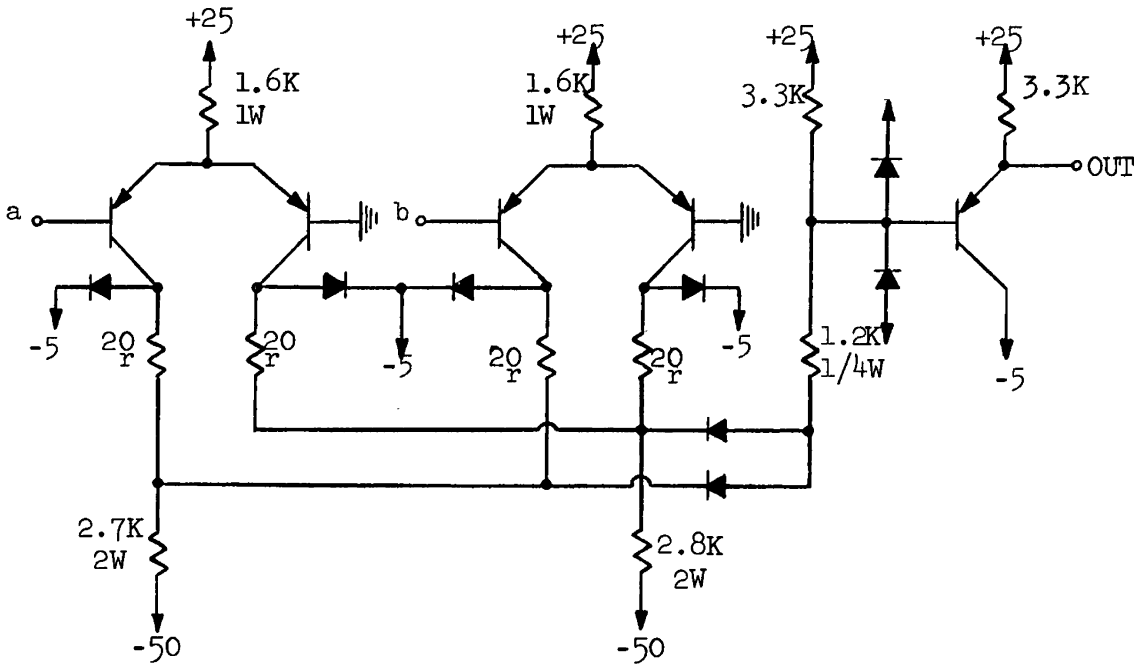


Figure 45
Restoring EXCLUSIVE-OR (This Is S-853)

In experiments this circuit has shown operation times, as expected, of around 15 mμs, and a pair of such circuits, connected to race, as shown in Figure 46, indicated a threshold time of less than 10 mμs [threshold times are those which lapse between the crossing of the input threshold (0.6v) and the crossing of the same threshold at the output point].

5.2.6 Restoring EQUIVALENCE Circuit

By inverting one of the inputs, the EXCLUSIVE-OR becomes an EQUIVALENCE circuit. This is evident from the definition of the equivalence expression:

$$AEB = AB \vee \bar{A}\bar{B}$$

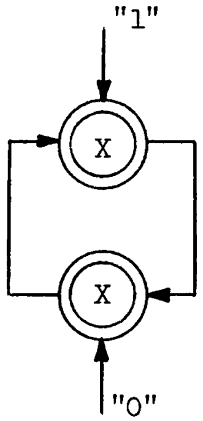


Figure 46

Racing EXCLUSIVE-OR Circuits

The circuit is shown in Figure 47.

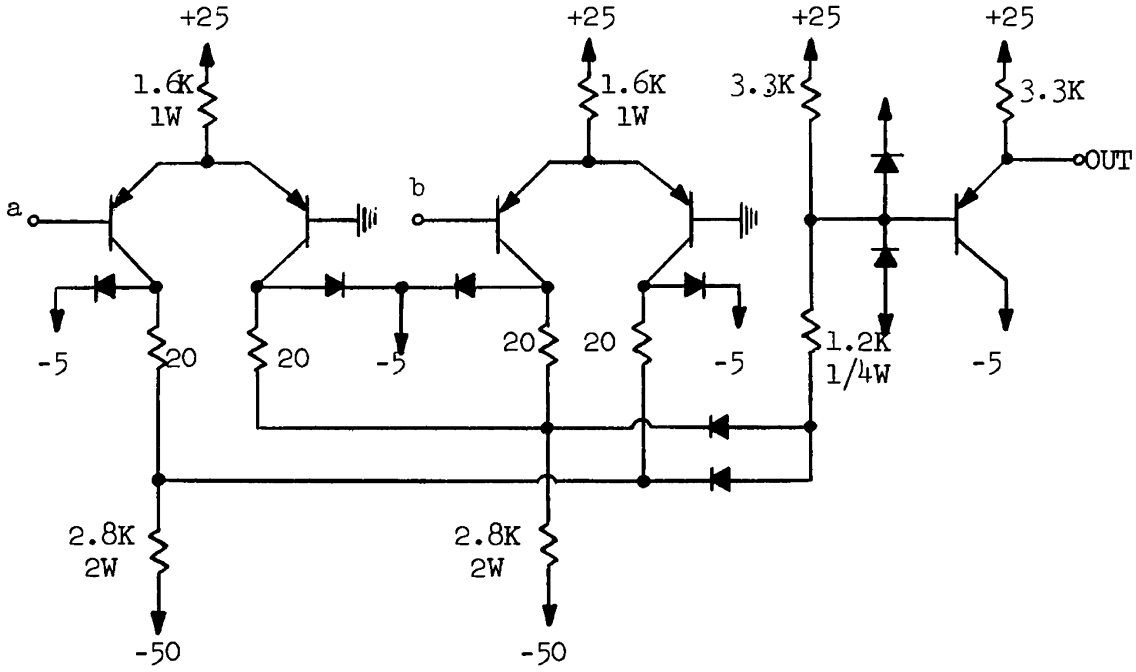


Figure 47

Restoring EQUIVALENCE Circuit (This Is S-862)

Another circuit, namely the F-Element, is also derived from the EXCLUSIVE-OR design, but since this circuit exhibits memory, it is well to consider firstly the simplest such circuit.

5.3 Memory Circuits

Various topological arrangements may be made to be bistable and there generally exists a justification for the choice of any given method. For instance an Eccles Jordan flipflop has two input terminals which accept similar type signals; it is symmetrical and provides symmetrical outputs.

On the other hand, an asymmetrical flipflop (similar to a Schmidt trigger) is faster because it has only one collector delay (an Eccles Jordan has 2), the transition states are easier to analyze and its single input terminal makes it suitable for pulse shaping. A latch-type circuit is also fast, has a one-wire input and is easily cleared to a standard state. Gating into these devices is in each case somewhat unsatisfactory and the F-Element described later is used almost exclusively. Where speed is at a premium, however, and the absence of a gate no great disadvantage, an asymmetrical flipflop has been designed, and it will be described first.

5.3.1. Asymmmetrical Flipflop

The asymmetrical flipflop in its simplest form is shown in Figure 48. The circuit values have been taken directly from the NOT circuit, and it is easily verified that the circuit is bistable. However, for two reasons,

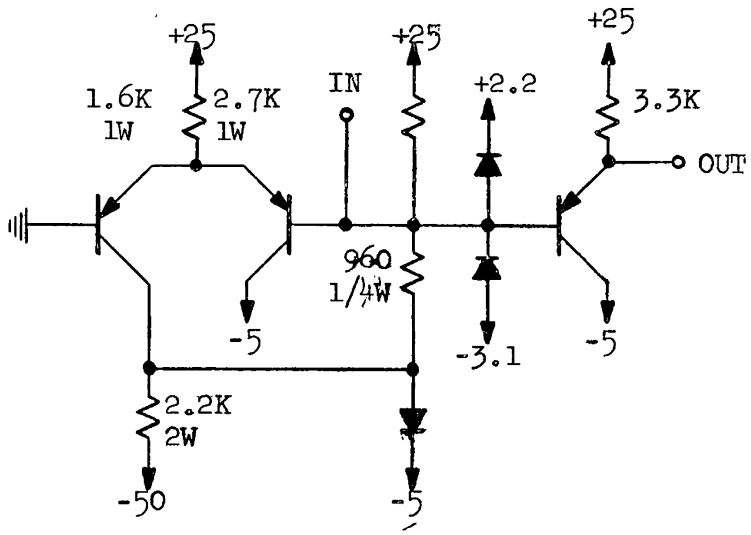


Figure 48
Simple Asymmetric Flipflop

this circuit is unsuitable for most applications:

1. Since the degree of coupling between input and output terminals is high (nearly unity), occurrence of an output signal following application of an input signal, indicates nothing about the condition of the flipflop (i.e., that it has been set, or that it will be set, or even that it is in working order).

2. The output divider has to be stiff (i.e., low impedance) in order to drive a reasonable load, and the input signal must move both this divider and the two transistors connected to it, in order to set the flipflop. It turns out that the resulting input impedance is so extremely low as to overload almost every source available.

Both of these disadvantages are somewhat alleviated by the use of a double divider, with one branch feeding the internal transistor and input point, and the other branch feeding the output emitter follower. Coupling between input and output terminals is thereby reduced to about 0.1 and although occurrence of an output signal does not indicate that the new state will hold, it does indicate that at least part of the flipflop has reacted. Moreover, the impedance of the inside divider branch may be made much higher than that of the outside branch, so that the impedance seen by the input source is quite high.

Design of the double divider Schmidt type flipflop (shown in Figure 49) was undertaken with the aid of a special-purpose computer analysis program (a predecessor of 1206).

Gating the input to the asymmetric flipflop requires the somewhat complicated circuit shown in Figure 50 and both the signal and gate amplitudes must then be at least 1.2 volts in order to guarantee 0.6 volts at the flipflop input.

This, together with the fact that both g and $\bar{g}$ must be provided, indicates that the Schmidt kind of flipflop is somewhat unwieldy and of limited usefulness.

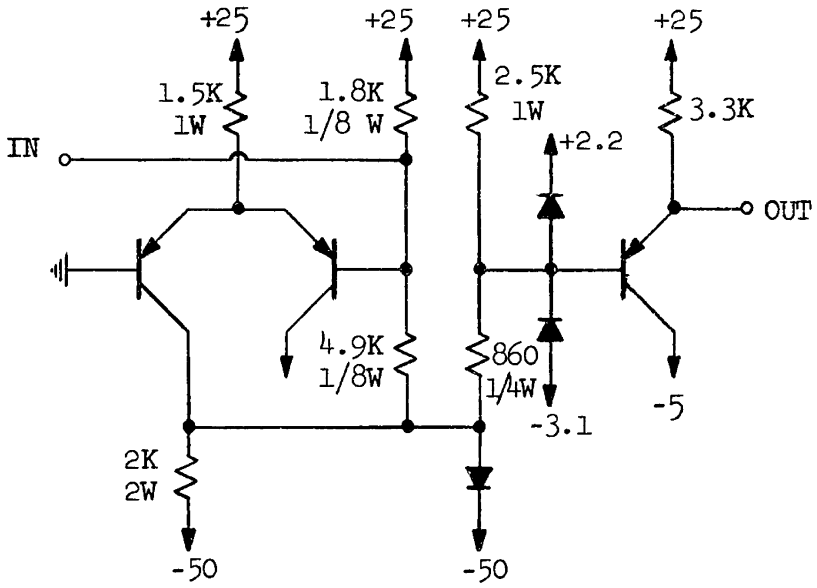


Figure 49

Asymmetric Flipflop (This Is S-866)

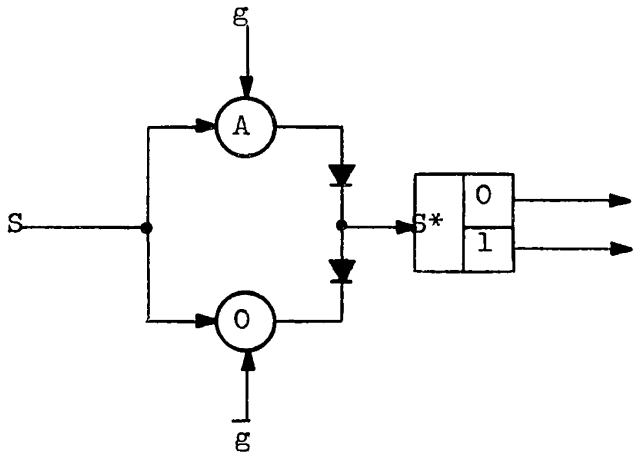


Figure 50

Gated Asymmetric Flipflop

5.3.2. F-Element

The F-Element is the first successful attempt to provide a realization of a flipflop integral with its gate, which has the high sensitivities (0.6v, 1.2 ma) associated with other kinds of restoring circuits (e.g., NOT). Its topology stems from that of the EXCLUSIVE-OR circuit. One form for the Boolean expression defining a gated flipflop (F-Element) is

$$F' = F\bar{G} \vee GS = (F \vee G)\ (\bar{G} \vee S)$$

which may be transformed to

$$\bar{F}' = (\bar{F} \vee G)\ (\bar{G} \vee \bar{S})$$

where the prime denotes the new state; F is the F-element state, S is the signal state and G is the gate state.

Using techniques exactly analogous to those described for the EXCLUSIVE-OR circuit, the F-Element realized is as shown in Figure 51. Multiple inputs are very simply provided by duplicating the portion within the dotted outline.

$$\left[\text{cf: 2 input F-function: } \bar{F}' = (\bar{F} \vee G_1 \vee G_2)\ (\bar{G}_1 \vee \bar{S}_1)\ (\bar{G}_2 \vee \bar{S}_2)\right]$$

5.3.3 C-Element

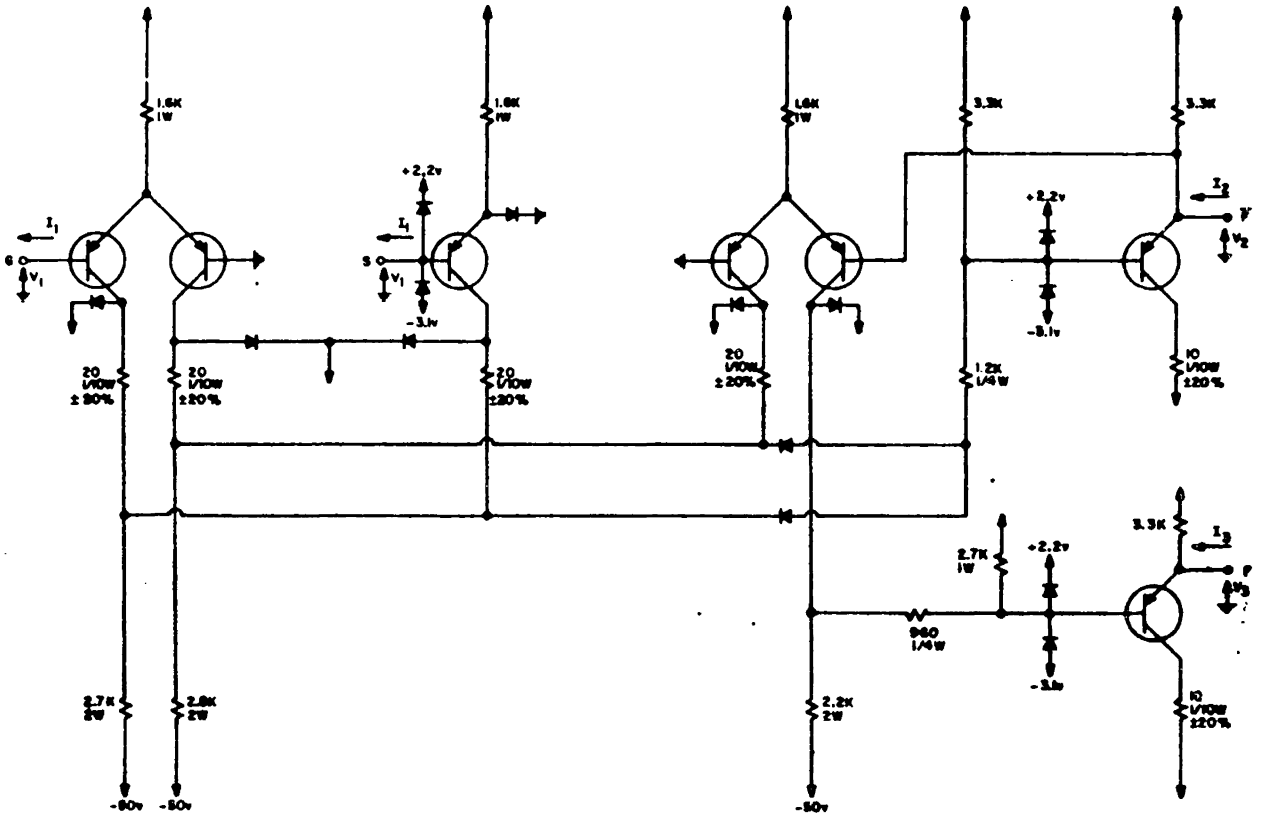
This is a flipflop with special gating features designed for certain speed-independent applications. In its basic form it has two inputs (A,B) and one or two outputs. The Boolean C-function may be written:

$$C' = AB \vee AC \vee BC$$

i.e., the output will agree with the inputs A and B when they agree with each other, and will retain its last state when the inputs disagree with each other.

Given the Schmidt kind of flipflop of Section 5.3.1, a C-Element may be simply constructed as shown in Figure 52.

Alternatively, it may be formed using an Eccles-Jordan flipflop and push-pull signals, as shown in Figure 53.



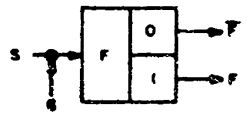
WHEN NOT SPECIFIED

UP VOLTAGE +25v
DOWN VOLTAGE -5v
RESISTORS 1/2W ±5%

POWER SUPPLIES ±3%
+25v 90.8 ma. MAX.
-80v 46.5 ma. MAX.
-8v 34.5 ma. MAX.
+2.2v -4.2 ma. MAX.
-3.1v -3.9 ma. MAX.

TRANSISTORS
6F 4808 (CURVE OF APRIL 23, 1958)
0.98 ≤ α ≤ 1

DIODES
S-577 (CURVE OF FEB. 18, 1958)
V_1 ±0.6v MAX. REQ'D
I_1 1.2 ma. MAX. REQ'D
V_2 ±2.8v to ±3.2v
$-I_2$ 6.7 ma. (PULLING +)
I_2 16 ma. (PULLING −)
V_3 ±2.8v to ±3.8v
$-I_3$ 6.7 ma. (PULLING +)
I_3 22 ma. (PULLING −)



LOGICAL SYMBOL

Figure 51

UNIVERSITY of ILLINOIS — GRADUATE COLLEGE — DIGITAL COMPUTER
FOR M.W. BY J.G. CHECKED APPROVED APPROVED DATE 3-4-59
TITLE — SINGLE INPUT F-ELEMENT
IM-850

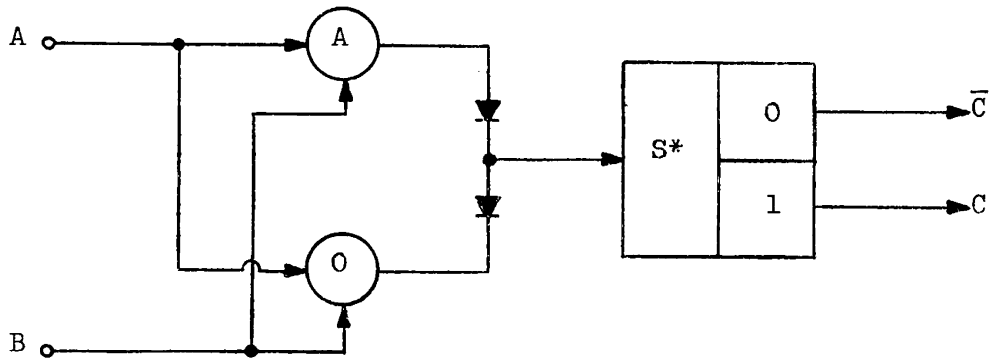


Figure 52

C-Element from Schmidt Type Flipflop

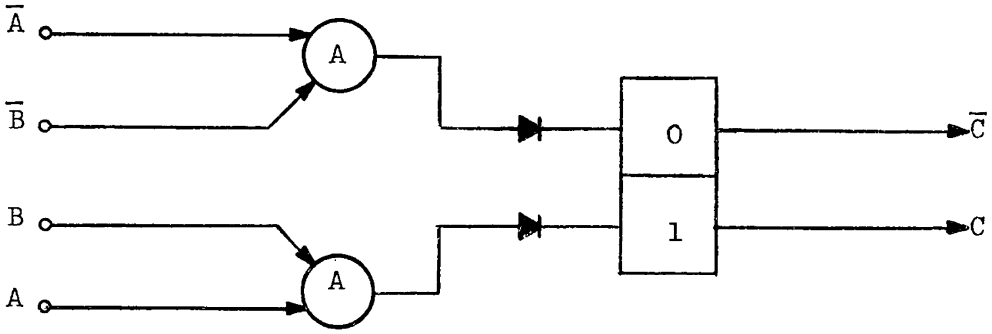


Figure 53

C-Element from Eccles-Jordan Flipflop

Using standard circuits both of these arrangements are uneconomical and require input signals of at least 1.2v. An integrated realization of the C-Element like that obtained for the F-Element is required. Inspection of the C-function

$$C' = AB \vee AC \vee BC$$

$$\text{or } C' = (A \vee B)\ (A \vee C)\ (B \vee C)$$

indicates that analogue addition is not applicable for generating C' because each of the variables is used more than once.

Although no completely integrated form for the C-Element has yet been discovered, circuits corresponding to Figures 52 and 53 have been designed, with the desired input sensitivities of 0.6v, by the use of switching pre-amplifiers and diode logic.

An interesting alternative method is obtained upon reconsidering the C-function:

$$C' = AB \vee AC \vee BC$$

This is recognized as the majority function of A, B, C and suggests that a transformation into ternary logic may allow the formation of C' by analogue addition. It is unfortunate that the simple resulting circuit (Figure 54) turns out to have rather tight tolerances. (It was abandoned on this account).

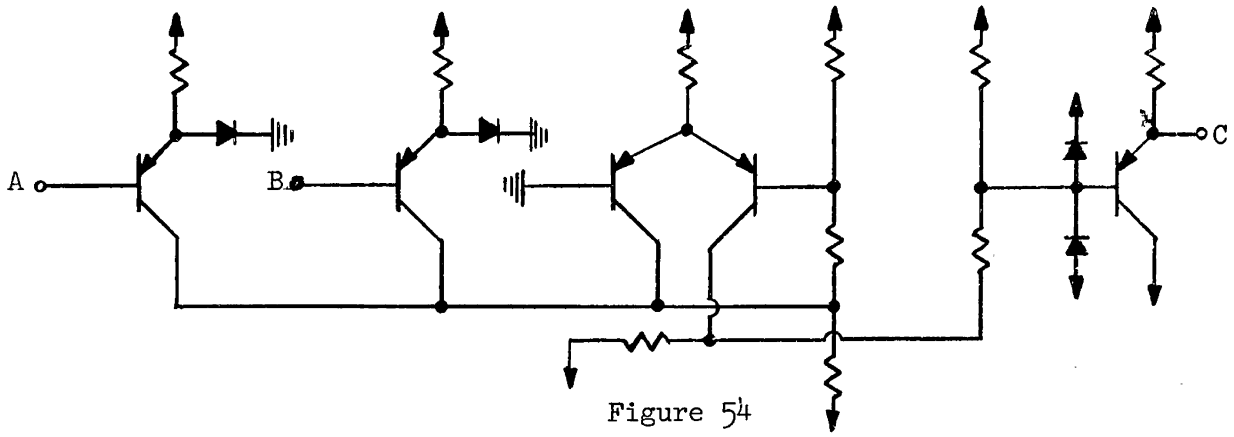


Figure 54

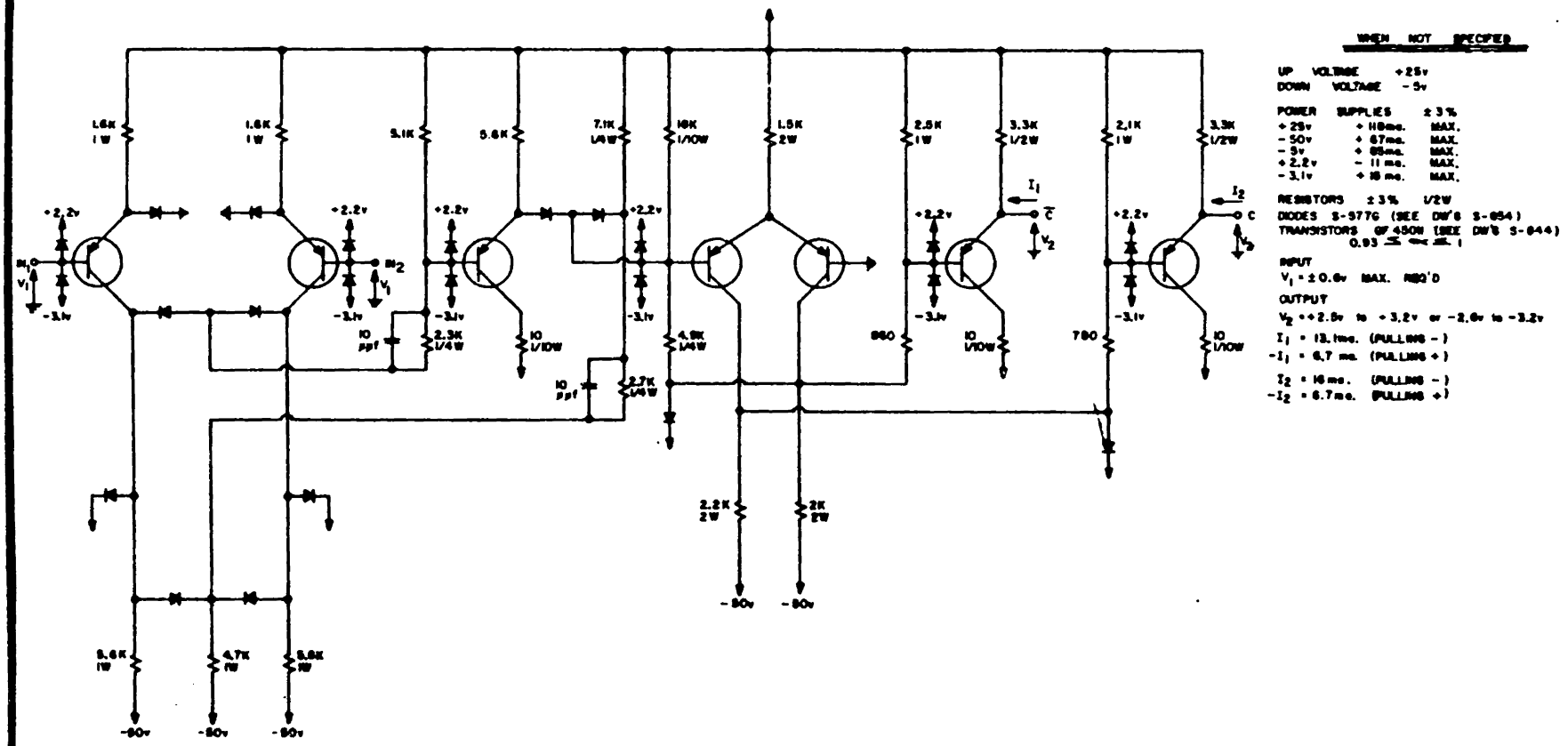
C-Element using Ternary Logic

The circuit finally adopted, corresponding to the logical diagram of Figure 52, is shown in Figure 55. This is seen to have two collector delays and therefore an operation time of about 30 μs.

5.4 Miscellaneous

5.4.1 Selectors

In the interconnection of registers it is common to require a method of route selection out of a number of alternatives. This selection would ordinarily be done with AND-OR complexes and an n-way selector would evidently require 2n transistors per bit (Figure 56). Subject to the proviso that the selection be only 1-out-of-n (i.e., not m-out-of-n) this number can be reduced to (1 + n) transistors per bit. The corresponding circuit, shown in Figure 57, is called a 'selector'. An additional practical requirement is that the selector driver "0" levels be more negative than the signal "0" level to ensure



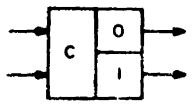


Figure 55

UNIVERSITY of ILLINOIS — GRADUATE COLLEGE — DIGITAL COMPUTER	
FOR N.J. BY J.O. CHECKED APPROVED APPROVED DATE 8-28-59	M-870
TITLE — C ELEMENT	

that the signal input transistor holds down at most one of the diode AND circuits (the selected one).

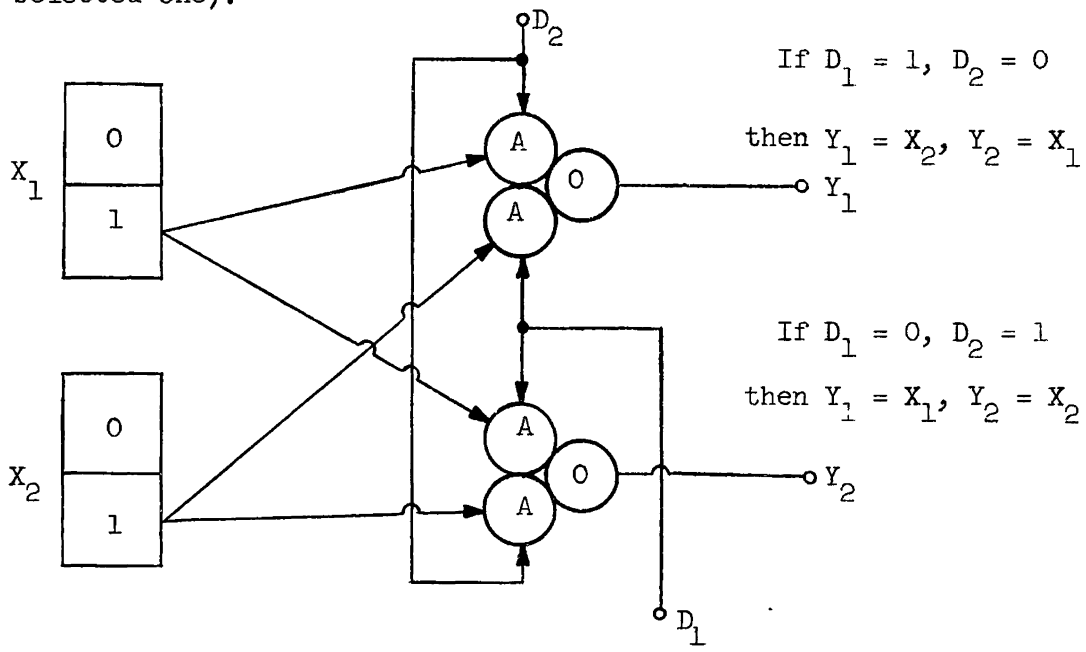


Figure 56

2-Bit Register with Selector

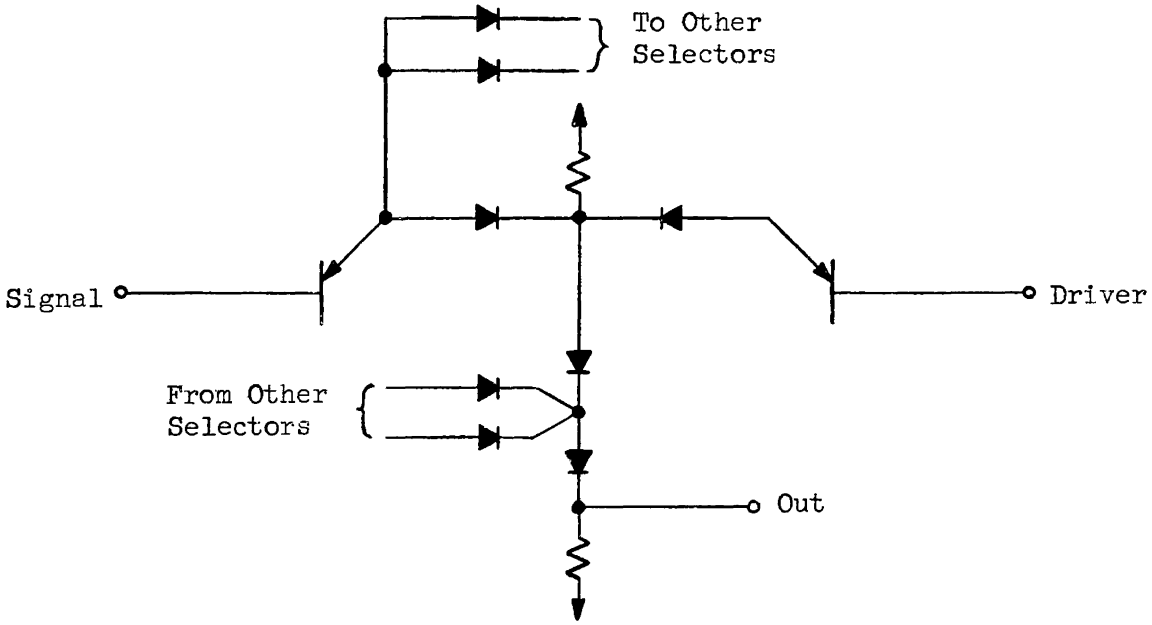


Figure 57

Selector

In some cases it is possible to incorporate the signal input transistor into the output circuit of a restoring circuit (say an F-element of the register) and this reduces the transistor count to 1 transistor per bit per way. Figure 58 shows a selector attached, for simplicity, to a NOT circuit.

If required, a special selector can be attached to a modified restoring circuit so that the selected output is a fully restored signal (see Figure 59).

5.4.2. Reply Circuits

In a truly asynchronous circuit each operation is initiated by the completion of the preceding one, and certain of the basic circuits are therefore required to provide some kind of reply signal indicating that they have reacted. As an example, consider the arrangement shown in Figure 60. Here a Schmidt kind of flipflop with gate (cf. Figure 52) is being monitored with fast (i.e., non-restoring) circuits. For this arrangement;

G = 0, R = 0

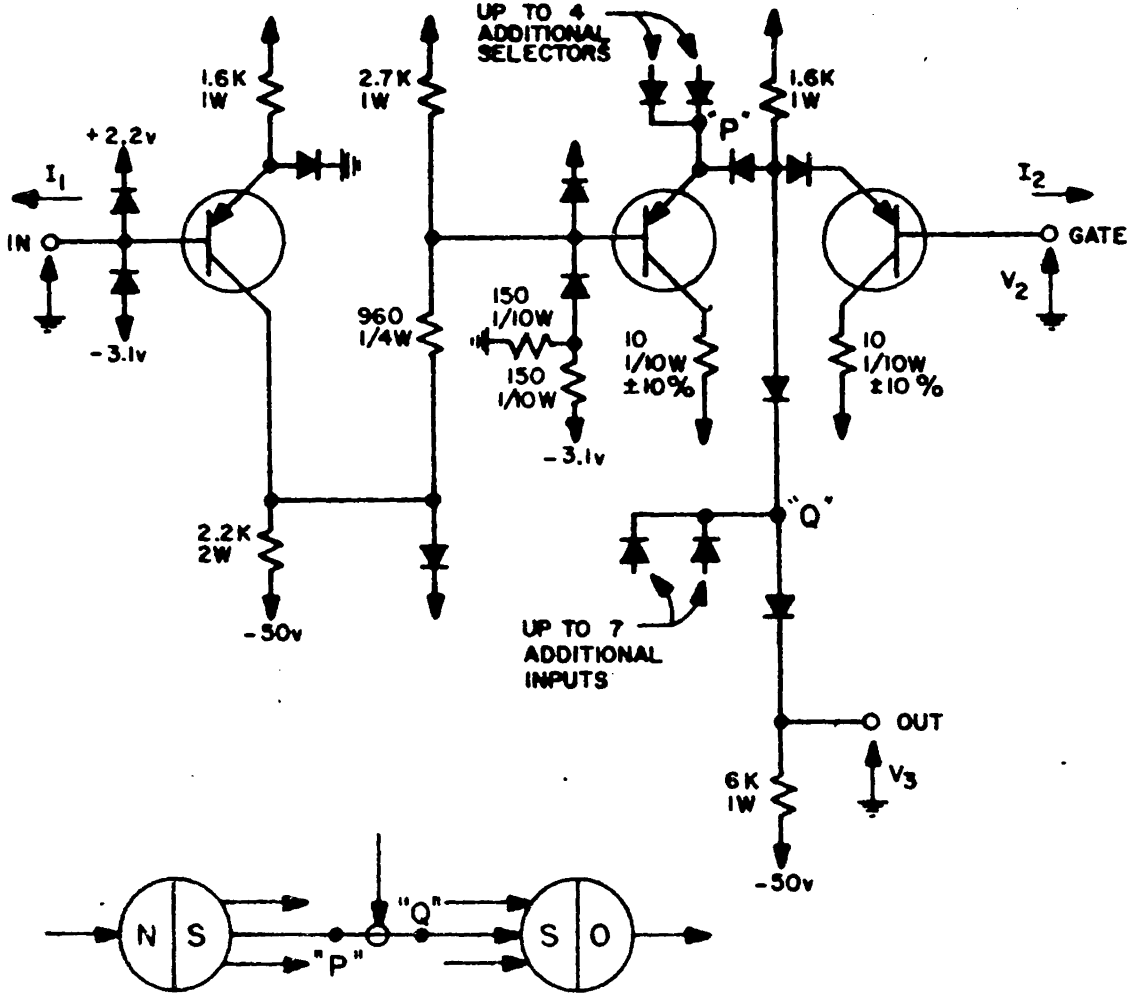
G = 1, S not set, R = 0

G = 1, S set, R = 1

5.4.3. Drivers

Driving the gates and selectors in a register of some 50 to 100 bits presents a special problem. At almost 2 ma per circuit, 100 ma or more may be required from the driver. Ideally we want the driver to appear as a voltage source to the load, and, given NPN and PNP transistors, we could construct a complementary emitter follower tree to approximate a voltage source quite well. However NPN transistors having characteristics anything like those of the GF 45011 PNP transistor were not available at the time this project began; indeed, they are not readily available at the time of writing.

A single-ended PNP emitter follower tree has an asymmetrical output impedance characteristic; i.e., during a "1"-"0" transition it appears as a voltage source, while during a "0"-"1" transition it is current limited by the emitter resistors. The effects of this may be compensated in practice by



WHEN NOT SPECIFIED

- UP VOLTAGE +25v
  DOWN VOLTAGE -5v
  POWER SUPPLIES ±3%

+25v	+46.2 ma.	MAX.
-50v	+31.1 ma.	MAX.
-5v	+22.5 ma.	MAX.
+2.2v	-4.2 ma.	MAX.
-3.1v	+10.6 ma.	MAX.

RESISTORS ±3% 1/2 W

DIODES S-577G (SEE DWG S-854)
TRANSISTORS GF 45011 (SEE DWG-844)
$0.93 \leq \sim \leq 1$

$V_1 = \pm 0.6v$	MAX.	REQ'D
$I_1 = 1.2$ ma.	MAX.	REQ'D
$V_2 = \pm 2.0v$	MAX.	REQ'D
$I_2 = 1.2$ ma.	MAX.	REQ'D

FANOUT	MIN. $\lvert V_3 \rvert$ +	MIN. $\lvert V_3 \rvert$ -
1	2.06v	1.38v
2	2.06v	1.3v
3	2.06v	1.25v

FOR EACH ADDITIONAL SELECTOR CONNECTED TO POINT "P" ADD

+25v	12.6 ma.	MAX.
-50v	9.3 ma.	MAX.
-5v	14.6 ma.	MAX.

ADDITIONAL SELECTORS CONNECTED TO POINT "Q" DO NOT EFFECT THE POWER REQUIREMENT

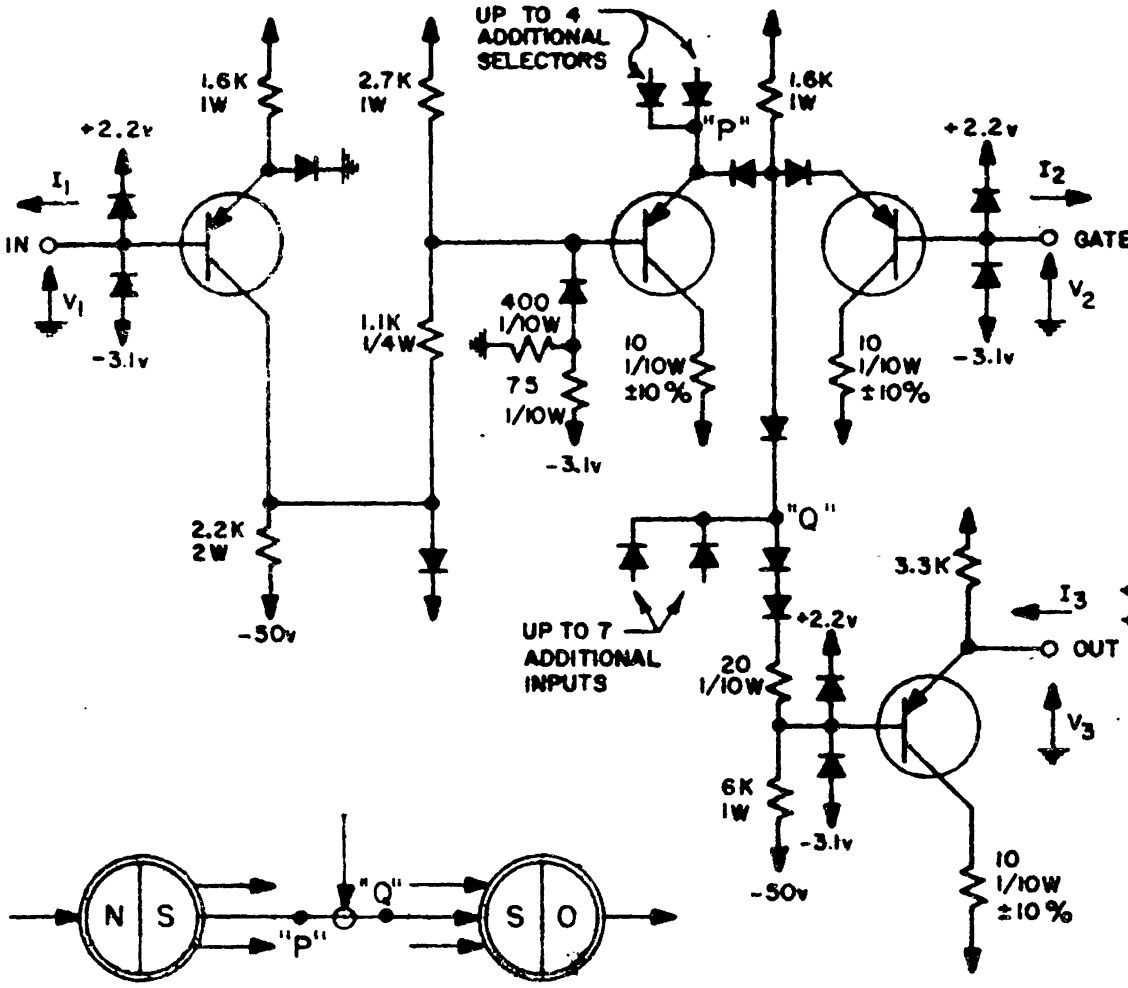
Figure 58

UNIVERSITY OF ILLINOIS —— GRADUATE COLLEGE —— DIGITAL COMPUTER

FOR N.W. BY J.O. CHECKED [illegible] APPROVED [illegible] DATE 5-13-59

TITLE—NOT CIRCUIT WITH DEGENERATE OUTPUT SELECTOR

S-863



WHEN NOT SPECIFIED

UP VOLTAGE +25v
DOWN VOLTAGE -5v
POWER SUPPLIES ±3%

+25v	+ 55.2 ma.	MAX.
-50v	+ 31.1 ma.	MAX.
- 5v	+ 31.4 ma.	MAX.
+2.2v	- 4 ma.	MAX.
- 3.1v	+ 6.6 ma.	MAX.

RESISTORS ±3% 1/2 W

DIODES S-577G (SEE DW'G S-854)
TRANSISTORS 6F4501I (SEE DW'G S-844)
$0.93 \leq \alpha \leq 1$

$V_1 = \pm 0.6v$ MAX. REQ'D
$I_1 = 1.2$ ma. MAX. REQ'D
$V_2 = -3.1v, +2.9v$ MIN. REQ'D
$I_2 = 1.3$ ma. MAX. REQ'D
$V_3 = \pm 2.5v$ to $\pm 3.2v$
$+I_3 = 6.7$ ma. (PULLING +)
$+I_3 = 17$ ma. (PULLING -)

A TOTAL OF 5 SELECTORS MAY BE CONNECTED TO POINT "P"

A TOTAL OF 8 INPUTS MAY BE CONNECTED TO POINT "Q" IN EACH SELECTOR. POWER REQUIREMENTS REMAIN AS STATED ABOVE

FOR EACH SELECTOR CONNECTED TO POINT "P" ADD

+25v	26.6 ma.	MAX.
-50v	9.3 ma.	MAX.
- 5v	23.6 ma.	MAX.

Figure 59

UNIVERSITY OF ILLINOIS —— GRADUATE COLLEGE —— DIGITAL COMPUTER

FOR N.W. BY J.Q. CHECKED [illegible] APPROVED [illegible] DATE 5-13-59

TITLE — NOT CIRCUIT WITH RESTORED OUTPUT SELECTOR

S-864

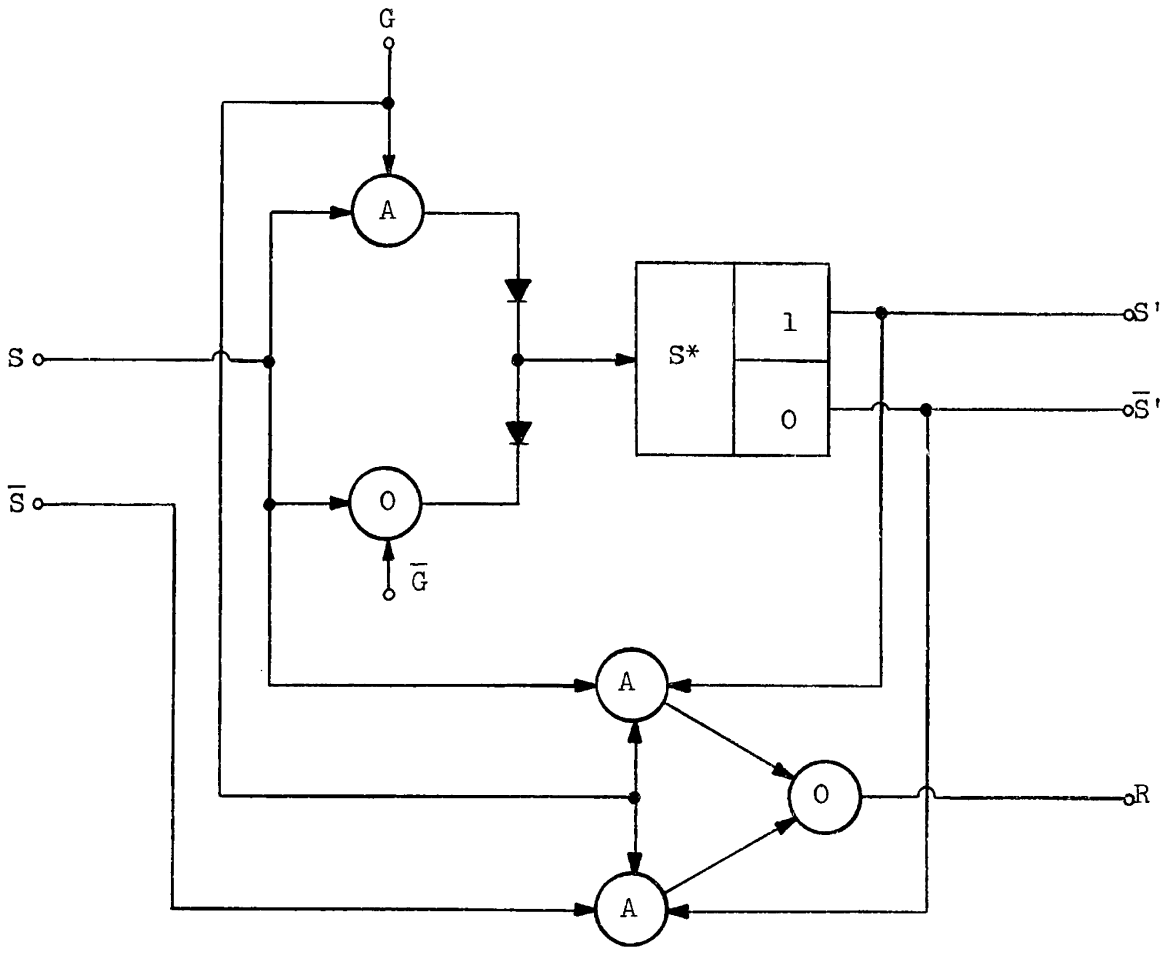


Figure 60
Gated Flipflop with Reply

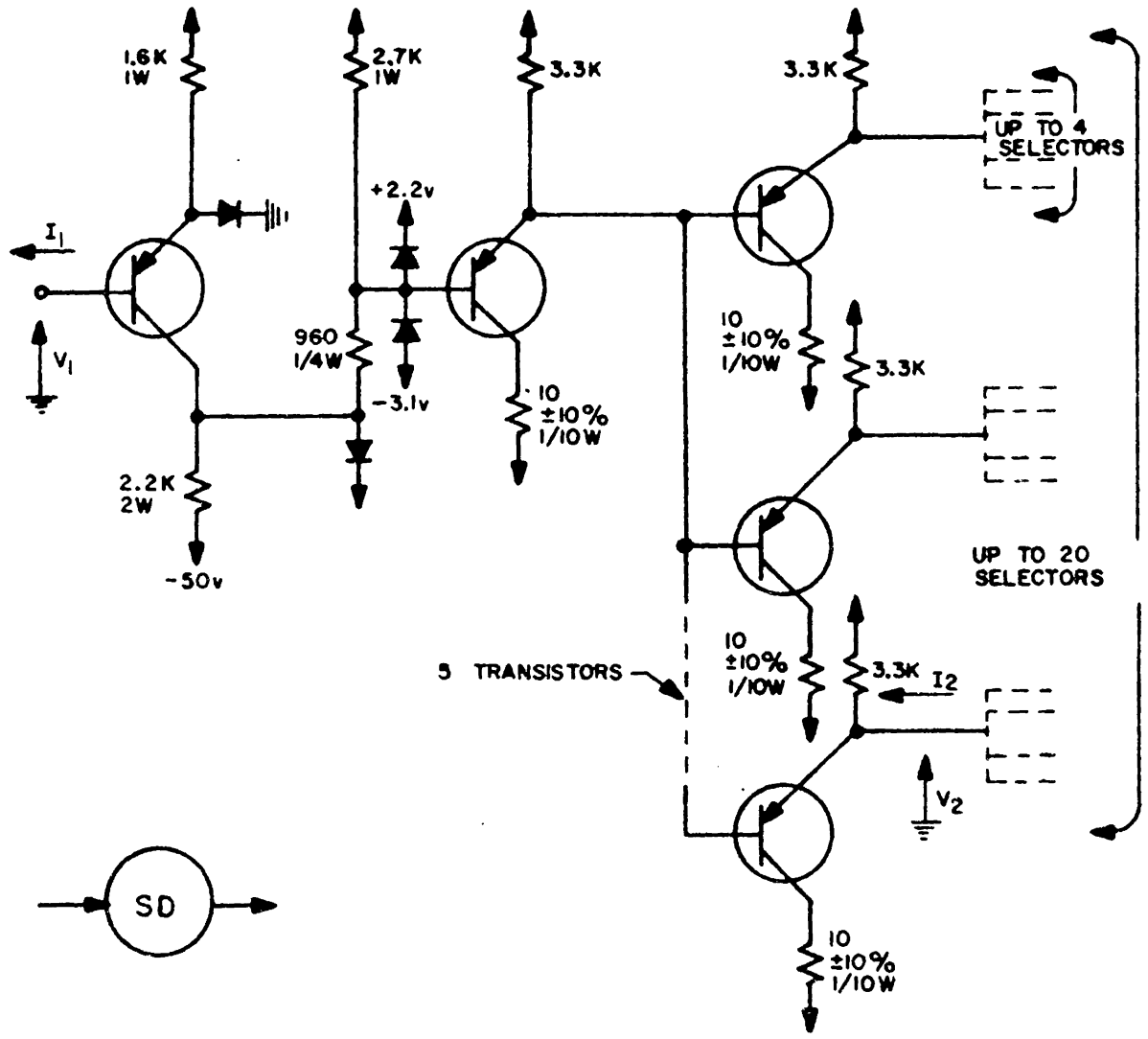
providing sufficient overcurrent (from these emitter resistors) to charge the capacity of the worst expected load in some reasonable time (say 25 mμs). Since the transient dissipation in an emitter follower is somewhat uncertain, some additional derating is commonly allowed and, as a result, the overall efficiency of an emitter follower driver (in terms of transistors per load watt) is rather low. Figure 61 shows such a driver intended for driving 20 degenerate selectors (see Section 5.4.1).

A more efficient arrangement, but one which is current limited in both directions, is a parallel array of collector followers. Figure 62 shows an 18 bit gate (i.e., F-element) driver. In order to avoid the additional

collector delay of a switching input stage, an emitter follower-Zener diode arrangement is used to provide the positive level shift necessary to switch the collector follower stages. Although it requires a much larger input to operate than the driver of Figure 61, there are fewer transistors in this circuit and it lends itself more readily to push-pull gating (see next section.)

5.4.4. Push-Pull Driving

With certain precautions regarding overlapping signals, gates between registers may sometimes be operated in a push-pull fashion, thereby reducing shift times by at least 1 driver delay plus rise time. A simple modification to the collector follower driver of Figure 62 results (Figure 63) in a circuit which delivers push-pull output signals. Connecting additional drivers to the common emitter point P can enable sequencing between several gates and the provision of a STOP condition, when all gates are closed.



WHEN NOT SPECIFIED

UP VOLTAGE +25v
DOWN VOLTAGE -5v

POWER SUPPLIES	±3%	
+25v	+91ma.	MAX.
-50v	+22ma.	MAX.
-5v	+71ma.	MAX.
+2.2v	-4.2ma.	MAX.
-3.1v	-3.7ma.	MAX.

RESISTORS ±3% 1/2W

DIODES S-577G (SEE DW'G S-854)

TRANSISTORS GF 45011 (SEE DW'G S-844) $0.93 \leq \alpha \leq 1$

$V_1 = \pm 0.6v$ MAX. REQ'D
$I_1 = 1.2ma.$ MAX. REQ'D
$V_2 = +2.75v$ to $+3.7v$, or
$V_2 = -2.0v$ to $-2.9v$
$I_2 = 7.1ma.$ (PULLING −)
$-I_2 = 6.7ma.$ (PULLING +)

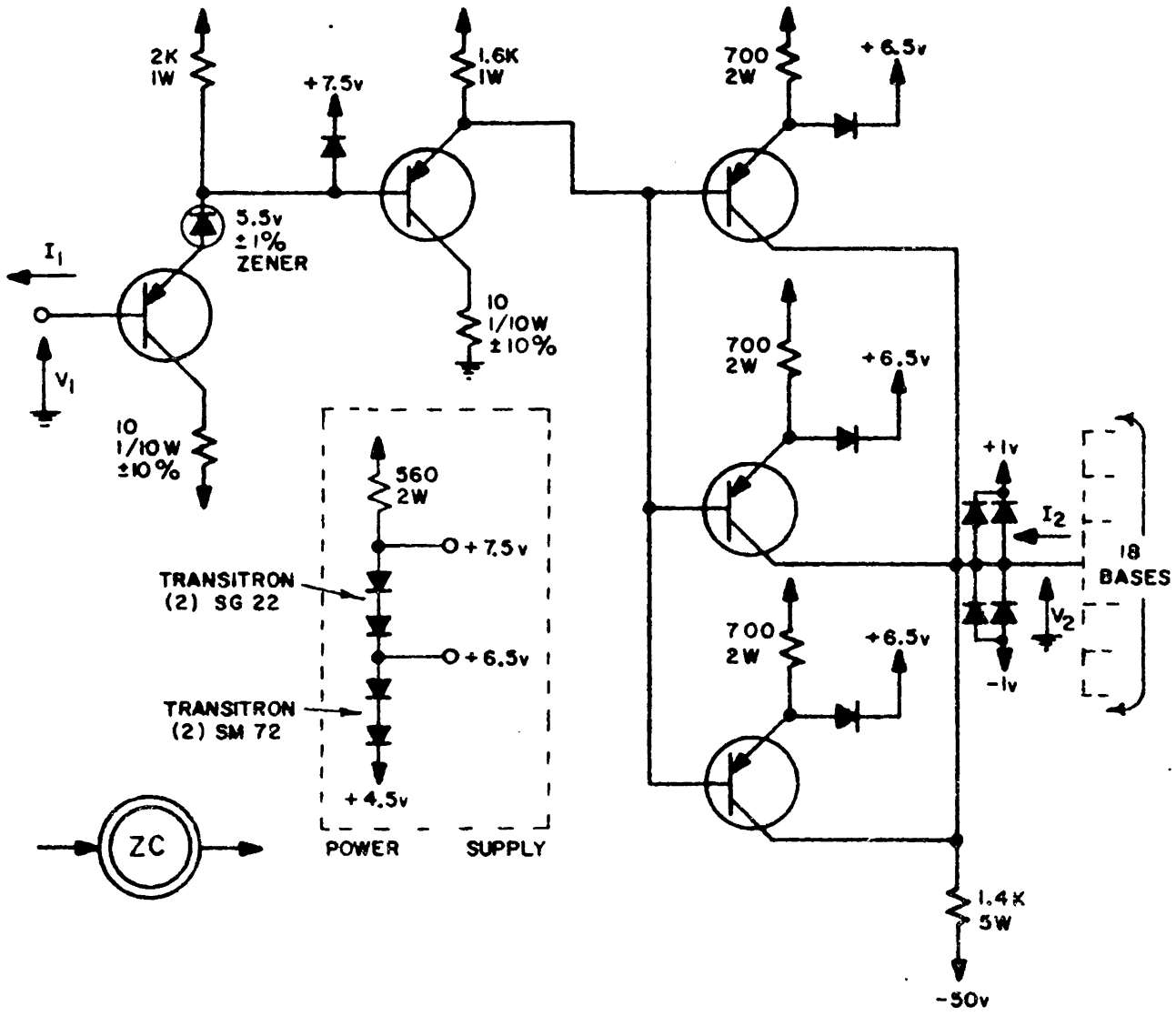
Figure 61

UNIVERSITY OF ILLINOIS —— GRADUATE COLLEGE —— DIGITAL COMPUTER

FOR N. W. BY J. O. CHECKED [illegible] APPROVED [illegible] DATE 6-3-59

TITLE — 20 BIT - DRIVER FOR DEGENERATE OUTPUT SELECTORS

S-874



WHEN NOT SPECIFIED

UP VOLTAGE + 25v
DOWN VOLTAGE - 5v

POWER SUPPLIES	±3%
+25v	+158ma. MAX.
-50v	+41 ma. MAX.
- 5v	+15 ma. MAX.
+4.5v	-140ma. MAX.
+ 1v	- 58 ma. MAX.
- 1v	- 38 ma. MAX.

RESISTORS ±3% 1/2 W
TRANSISTORS GF 45011 (SEE DW'G S-844)
0.93 ≤ α ≤ 1
DIODES S-577 (SEE DW'G S-854)
V_1 = ± 2.15v MAX. REQ'D
I_1 = 0.96 ma. MAX.

WITHOUT LOAD
V_2 = +2.1v, ± 0.1v to -2v, ± 0.1v

WITH LOAD
V_2 = +2.1v, ± 0.1v to -1.5v, ± 0.5v
$-I_2$ = 35ma. (PULLING +)
I_2 = 33ma. (PULLING -)

REMARK: NOTE NON-STANDARD INPUT

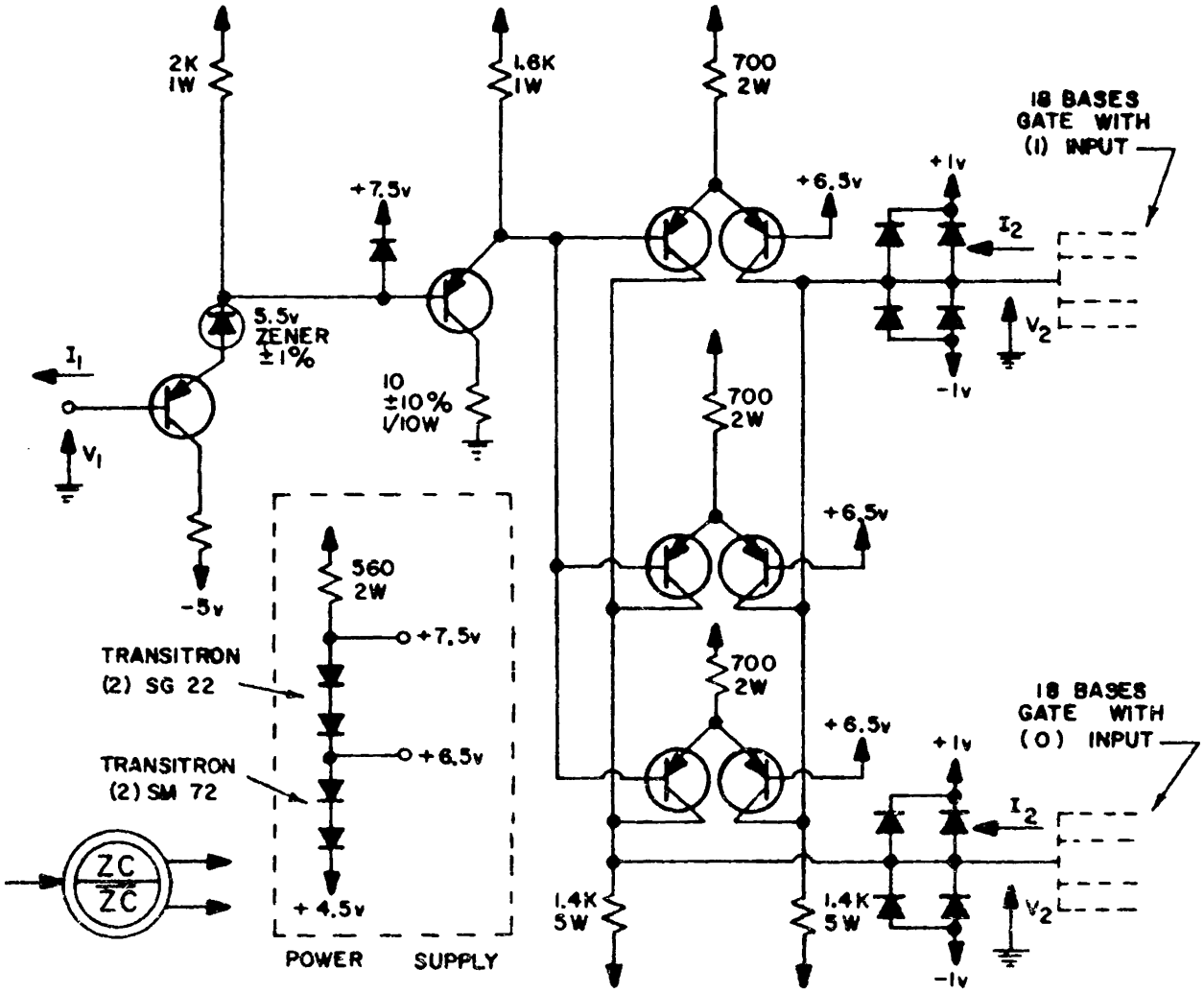
Figure 62

UNIVERSITY OF ILLINOIS —— GRADUATE COLLEGE —— DIGITAL COMPUTER

FOR N. W. BY J. O. CHECKED [illegible] APPROVED [illegible] DATE 6-3-59

TITLE—18 BIT-F ELEMENT DRIVER WITH ZENER DIODE

S-872



WHEN NOT SPECIFIED

UP VOLTAGE +25v
DOWN VOLTAGE −50v

POWER SUPPLIES	±3%	
+25v	+158 ma.	MAX.
−50v	+41 ma.	MAX.
−5v	+15 ma.	MAX.
+4.5v	−140 ma.	MAX.
+1v	−58 ma.	MAX.
−1v	−38 ma.	MAX.

RESISTORS ±3% 1/2W
TRANSISTORS GF 4501I (SEE DW'G S-844)
$0.93 \leq \alpha \leq 1$
DIODES S-577G (SEE DW'G S-854)
$V_1 = \pm 2.15v$ MAX. REQ'D
$I_1 = 0.96$ ma. MAX.

WITHOUT LOAD
$V_2 = +2.1v, \pm 0.1v$ to $-2v, \pm 0.1v$

WITH LOAD
$V_2 = +2.1v, \pm 0.1v$ to $-1.5v, \pm 0.5v$
$-I_2 = 35$ ma. (PULLING +)
$I_2 = 33$ ma. (PULLING −)

REMARK: NOTE NON-STANDARD INPUT

Figure 63

UNIVERSITY OF ILLINOIS —— GRADUATE COLLEGE —— DIGITAL COMPUTER
FOR N.W. BY J.Q. CHECKED [signature] APPROVED [signature] DATE 6-3-59 S-873
TITLE — 18 BIT-F ELEMENT PUSH-PULL DRIVER WITH ZENER DIODE

6. COMPUTER USE FOR CIRCUIT DESIGN

6.1. Principles of Circuit Analysis and Synthesis

In Section 3.3 it was seen that satisfactory circuit operation demands that certain inequalities between functions of circuit parameters (supply voltages, resistors, transistor parameters) be satisfied under "worst case" conditions. In general, these inequalities are quite cumbersome to handle, especially when nonlinear relationships occur: emitter-base voltage as a function of emitter current, or α as a function of emitter current (if this is high) are examples of nonlinear relationships. The procedure of finding a successful circuit requires that the calculation be made many times. Under these circumstances machine calculation by Illiac is most useful and a certain number of routines have been written to this end.

The input parameters which the routines use in their calculations are those over which the designer has some control. Direct control is available over resistor values, power supply voltages, and load current. Direct control is also available to the designer over transistor characteristics and power supply and resistor tolerances, but only over a limited range of variation, this range being determined by currently available hardware. Voltage drop values are also entered as input parameters since these are specified after the type of diode or transistor is decided upon. There must be enough input parameters to completely specify the circuit, however, since these routines are analytic programs.

It should be mentioned that all analytic programs calculate only the static dc conditions existing in a circuit. Going beyond this would mean a considerably longer program and would also necessitate a very detailed study of hihg-frequency transistor behavior. Therefore, the pulse response of a circuit is mostly studied on an experimental basis.

Apart from the topology and the spread curves of semiconductor elements we shall assume that the circuit problem is completely defined by a certain number of independent circuit variables R_i (resistors, etc.) which we want to choose in optimum fashion, with the limitation that for each variable there is a (rather wide) prescribed range:

$$\underline{R}_i \leq R_i \leq \overline{R}_i \ .$$

Furthermore, we shall introduce a certain number of auxiliary parameters A_j representing transistor alphas, return voltages, etc. For these, too, there is a prescribed (narrow) range:

$$\underline{A}_j \leq A_j \leq \overline{A}_j .$$

Here, however, we are not allowed to choose: the problem is rather to find the best R's for all possible combinations of the A's within their range. It should be noted that the range for each return voltage is known as soon as the transient behavior of the power supplies is given. For an alpha the range is usually from some value α_{min} to the value 1; α_{min} is determined by the aging behavior of the type of transistor used.

The analysis programs (1206, SIR KITTSOLVER) verify that under given boundary conditions (inputs) and for assumed circuit values, the circuit inequalities are satisfied. The synthesis programs (SINDY, PETITE PILOT, etc.) try to find circuit values which give optimum tolerance conditions. The next sections will describe these programs more in detail.

6.2. Description of 1206

The over-all operation of the program begins by reading the data tape which describes the circuit to be analyzed. During the reading process a program is set up which will evaluate all branch currents once the node voltages are known. Then the program proceeds to adjust the node voltages by a multi-dimensional Newton method until the sum of the currents into each node is zero.

The types of components which may be used are those for which the current can be determined from the applied voltage either by a formula or by a table. This means practically any d.c. characteristic can be handled except perhaps some multi-valued type or types which depend on the past history of the component. A formula is included for resistors as are tables for Q5-250 and Q10-600 diodes and GF45011 emitter-base drop. Provisions exist for six other tables and for three other formulas. In addition, formulas exist for evaluating a branch current as α or $1 - \alpha$ times the current in some other branch for use with transistors.

All computations are performed in floating point so no special scaling is required. The electrical quantities used are volts, milliamperes and kilohms. The maximum running time depends on the number of variables and on the initial approximations of the node voltages. However, the time will probably be less than 15 minutes for all cases and will usually be less than 5 minutes.

The maximum capabilities of the program are shown in the table.

Table of Maximum Values for 1206

30	Branches
13	Variable Nodes (2 minimum)
10	Fixed Nodes
20	Different Resistor Values
65	Terms in Node Current Summation
42	Words total for Special Formulas I, II, III.

6.3. Description of SIR KITTSOLVER

Two types of nodes in the circuit are distinguished, constant nodes and variable nodes. The voltages at the constant nodes are never changed throughout the calculation and they therefore represent supply voltages or other sources of constant voltage. The variable nodes are the nodes at which the voltage is to be computed. The solution is obtained by an iterative procedure in which one iteration consists of the following steps. At a given variable node the sum of the current ΣI into the node is calculated, then a small variation V in the voltage at the node is tentatively made and the resultant increment ΣI in the current sum is calculated. The node voltage V is then corrected according to the following relation

$$V \rightarrow V - \lambda(\Sigma I) \frac{\delta V}{\delta \Sigma I},$$

where λ is a constant of the program. A record is kept of the magnitude of the maximum ΣI, ΣI max, obtained during the iteration. When all variable nodes have been processed as just described the quantity ΣI max is compared against a number F which is a constant of the program and if ΣI max $<$ F, then the iteration procedure is stopped and the solution is printed, otherwise a new iteration is begun.

Nodes in the circuit may be connected in the three ways illustrated in the figures below. In these figures, nodes are labeled by letters, branches by numbers, and transistors by numbers.

In Figure 64 the current flowing in branch 1 is given by

$$i_1 = \pm \frac{V_B - V_A}{R_1} ,$$

where R_1 and the sign convention are specified on the data tape. If $|V_B - V_A| \geq R_1$ then i_1 is automatically set to $\pm$ 1/2; the sign being consistent with the sign of the true current. In Figure 64b the current flowing from C to D is determined from a voltage-current table. This table consists of two parts, the first representing the so-called "upper" diode curve and the second representing the

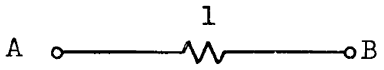


Figure 64a
Resistor Branch

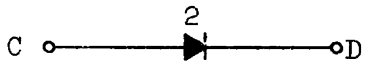


Figure 64b
Diode Branch

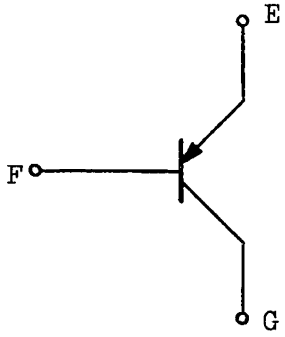


Figure 64c
Transistor

"lower" diode curve. Typical upper and lower curves are indicated in Figure 65. The particular diode curve to be used is specified on the data tape. A total of twenty points, arbitrarily spaced, on each (20 for the upper, 20 for the lower) curve are used to make up the table. Linear interpolation is used to obtain values between table entries. If, during the calculation, a voltage drop across

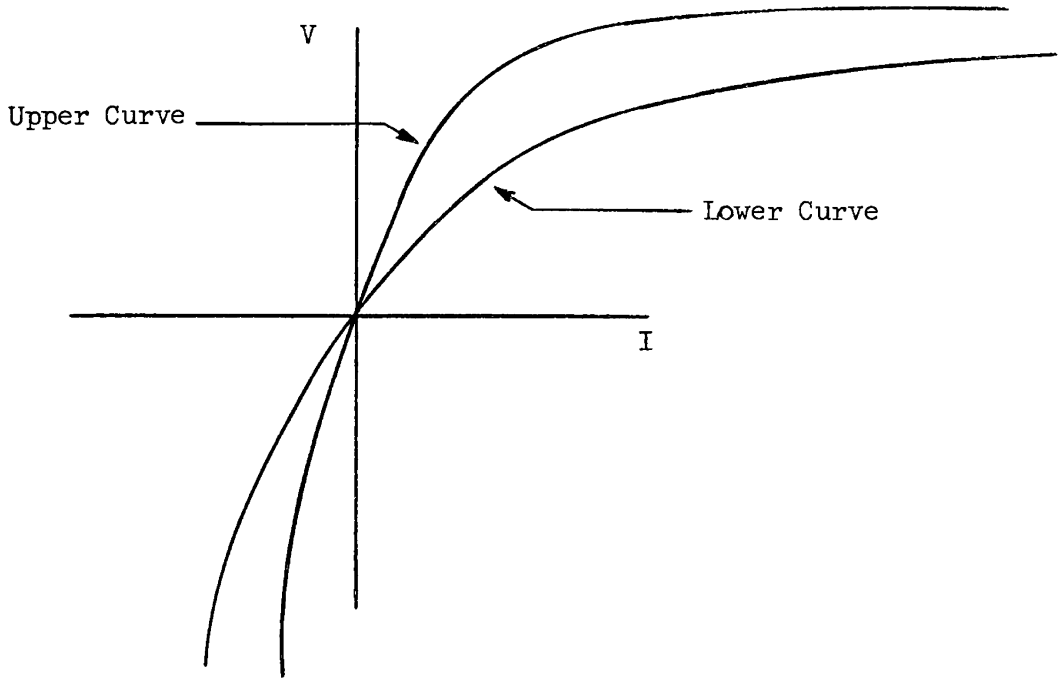


Figure 65
Typical Diode Curve

the diode occurs which is outside the range of the table, then the current through the diode is automatically set to that value given by the first or last point in the table according to which end of the range was exceeded. Commonly used diode tables are on the master program tape. Additional tables may be read in with the data. In Figure 64c the emitter current is obtained from an emitter-base drop table in which the emitter current is tabulated for different values of the voltage drop from emitter to base. As with the diode table there are twenty points corresponding to the upper curve and twenty points corresponding to the lower curve. Values between tabulated points are obtained by linear interpolation. The particular table to be used is specified on the data tape and, as with the diode, frequently used tables are on the master program tape while additional tables may be read in with the data. The base current i_b is obtained from the emitter current i_e according to the formula $i_b = (1-\alpha)i_e$, and the collector current i_c is given by $i_c = \alpha i_e$. The parameter α is also specified on the data tape. Finally, there is a special branch, not indicated in the above figure,

which is a constant current source and can be joined to any node.

6.4. Description of SINDY

This is the so-called "single divider synthesis" program. For the circuit of Figure 66, this program finds values for R_1, R_2, R_3, which satisfy a given set of requirements. These requirements are that, given the supply voltages E_1, E_2, a change in current from 0 to I milliamps entering node 1 will produce an output voltage swing of V_{2-} to V_{2+} under all tolerances and for all load currents up to some I_2 max. Printing will be suppressed for solutions having I_2 max. less than a specified I_2 min. Node 1 carries a positive bumping diode returned to the specified voltage V_{1+}, and the program uses this voltage to obtain maximal gain divider solutions.

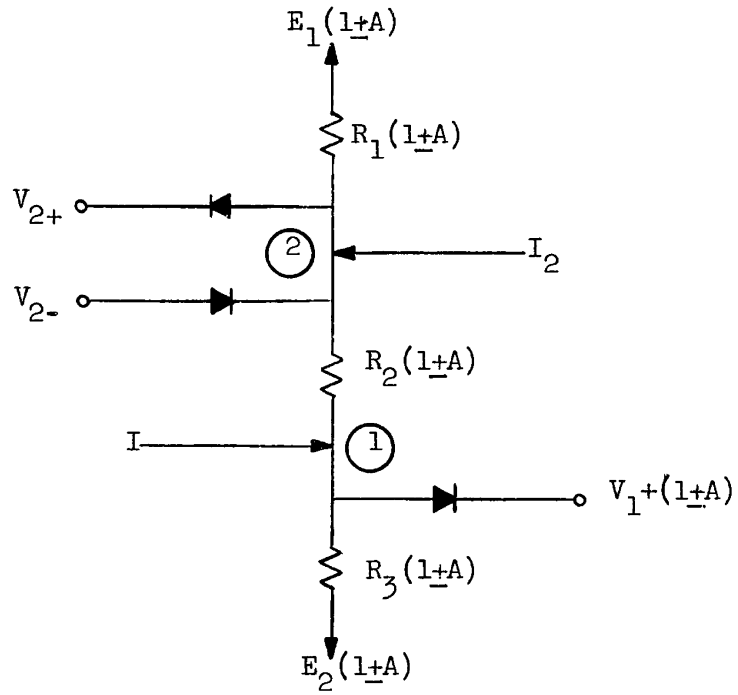


Figure 66
Single Divider Computed by SINDY

A flow diagram for SINDY is shown in Figure 67 below.

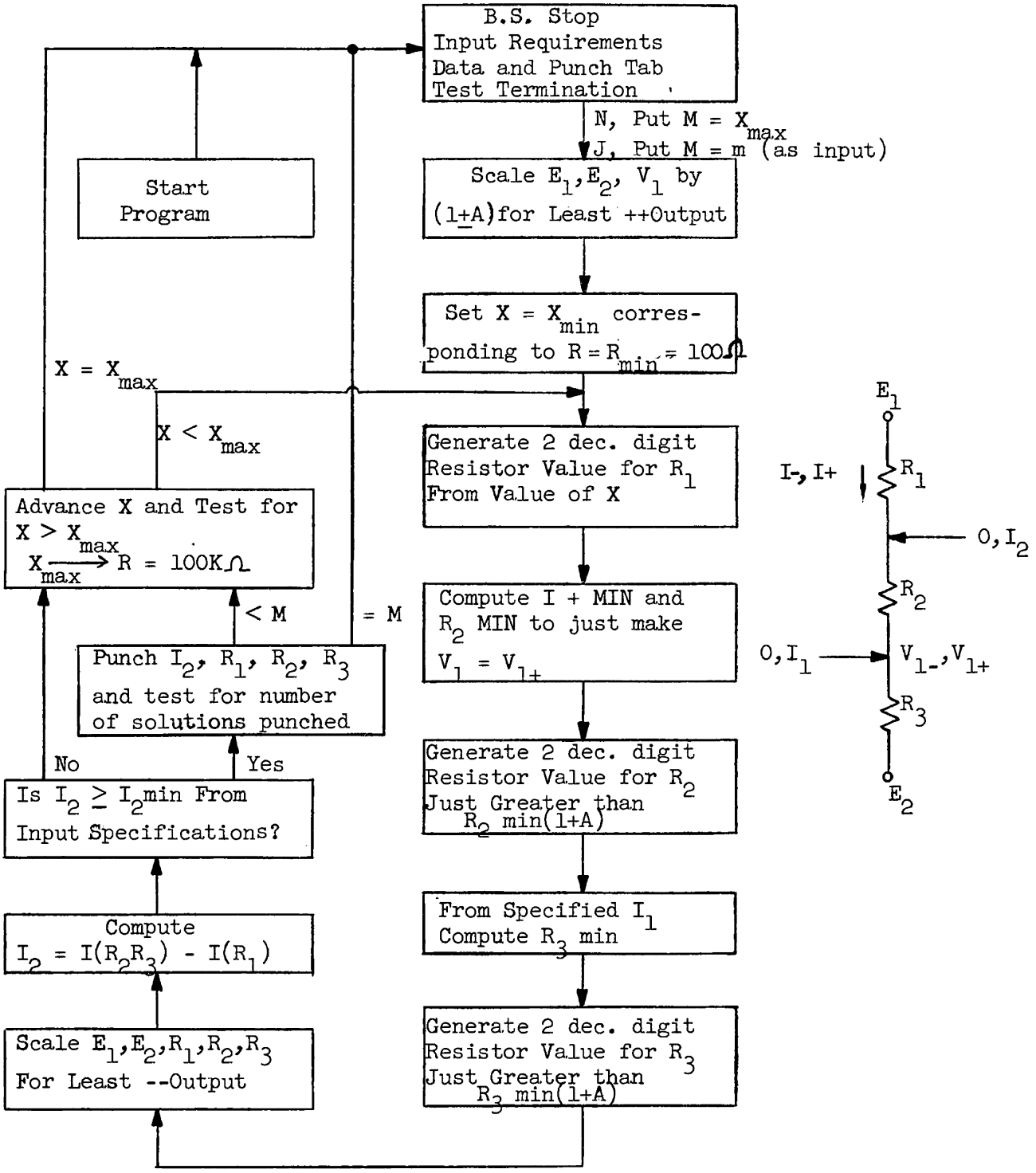


Figure 67

Flow Diagram for SINDY

The input data are E_1, E_2, V_{2+}, V_{2-}, V_{1+}, I, I_{2min}, A and a termination symbol N or J. If the symbol N is read, then the program sets M (number of solutions to be punched before reading next data set) equal to X_{max} (the number of 2 decimal digit resistor values between the limits on R). This guarantees that all solutions will be punched before the program is reset for the next data. If the symbol J is read then an additional integer m is read and the program sets M equal to m so that after m solutions are punched, the program resets and prepares to read the next data set.

6.5. Description of the Satisfactory Operation of a Circuit by Inequalities

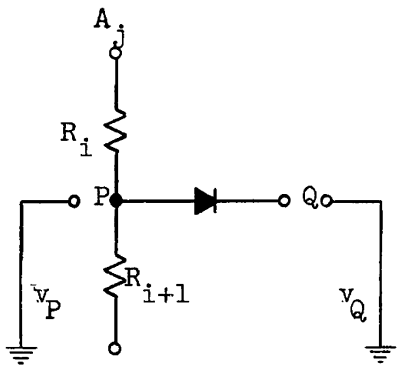


Figure 68
Example of Circuit Giving Inequality

It is easily seen that the statement that a given circuit operates satisfactorily is equivalent to a series of inequalities between currents or voltages. In the adjoining figure we may define satisfactory operation to mean that diode D conducts a current

$$i_{PQ} \geq i^{0}_{PQ}$$

when the applied voltages are $v_P(\ldots R_i \ldots, \ldots A_j \ldots)$, $v_Q(\ldots R_i \ldots, \ldots A_j \ldots)$. This means that the i_{PQmin} of the spread-curves of D must be greater than i^{0}_{PQ}. It should be noted that v_P and v_Q etc. may not only depend on the R's and A's but on the "states" applied to given inputs of the circuit i.e. in general we would have to write the input states as parameters:

$$v_P = v_P(\ldots S_g \ldots, \ldots R_i \ldots, \ldots A_j \ldots)$$

where the Σ Boolean variables S_g ($G = 1 \ldots \Sigma$) represent the combination of zeros and ones applied to the circuit.

Happily all the special cases can be written in a normalized form (note that the combination of S's are absorbed into k)

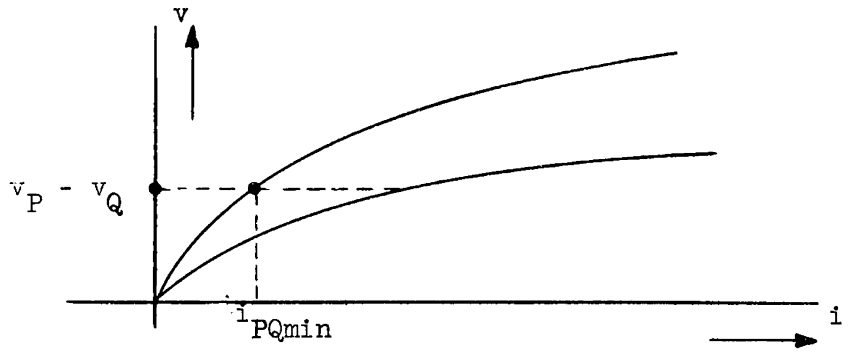


Figure 69

Diode Spread Curve

$$i = 1...n$$

$$j = 1...m$$

$$k = 1...N$$

$$f_k\ (...R_i...,...A_j...) \leq F_k$$

where F_k is a numerical constant. Note that it is not advantageous to normalize all F_k's to 1 since in some cases it may be necessary to consider a sub-group of the F_k's as variables which can be modified in order to obtain better tolerance conditions (see section 6.9).

It should also be noted that in the case of nonlinear elements defined by spread-curves, the above form is still valid provided we use in the calculation of f_k the worst case curve. In practice this is of academic interest only, but this remark allows the discussion of the next sections to be taken in a more general sense.

Finally it may be useful to note that for many design problems $n \sim m \sim N = 10$.

6.6. Definition of the Optimum Set of R's in a Simple Static Case

Suppose that the inequalities $f_k \leq F_k$ do not depend on nonlinear characteristics, i.e., that f_k is a (perhaps rather complicated) algebraic

function of the R's. Suppose furthermore that the A's have fixed values, then $f_k = f_k(...R_i...)$. Consider the hypersurface $f_k(...R_i...) = F_k$ in R-space: it has the property of separating the variable space into regions for which $f_k > F_k$ and into regions for which $f_k \leq F_k$. The N "walls" $f_k = F_k$ may define a common "inside" region: in this region all points satisfy the circuit inequalities. If this region has common points with the hyper-rectangle defined by $\underline{R}_i \leq R_i \leq \overline{R}_i$ (i = 1...n), these common points all represent solutions which give a working circuit. The figure below shows a case with n = 2, N = 3. To find the optimum circuit we would like to construct a point $(R_1....R_n)$ which is, in some sense, as far away as possible from the walls.

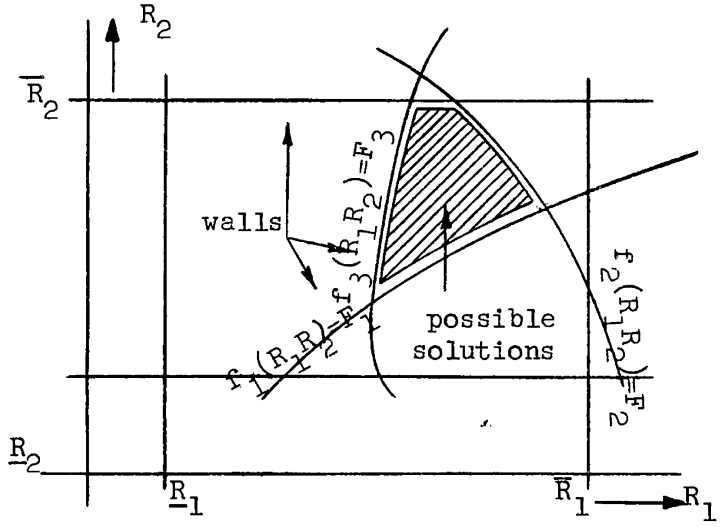


Figure 70

Graphical Optimization

Many methods of constructing this point can be imagined. Most of them have the common fault that the "best solution" maximizes the distance to the nearest wall instead of maximizing the ratio of this distance to an appropriately defined "average value" of the R's. Furthermore it is evident that only "local optimization" is possible.

The method adopted for the computer program searches for a solution R_i such that a "hypercross" centered at this point has fairly large arms. It is by no means certain that one obtains - even locally - a maximum armlength. The iterative steps are as follows:

1. Suppose that $(\ldots R_i^1 \ldots)$ is a point inside the region of possible solutions (a breadboard experiment may be used to determine this starting point!).

2. Draw a parallel to the R_1 -axis through $(\ldots R_i^1 \ldots)$ and find its intersections with all the walls. Take the intersections nearest to $(\ldots R_i^1 \ldots)$ and construct the midpoint. Set $(\ldots R_i^2 \ldots)$ equal to the coordinates of this midpoint.

3. Draw a parallel to the R_2-axis through $(\ldots R_i^2 \ldots)$ and find its intersections with all the walls. Take the intersections nearest to $(\ldots R_i^2 \ldots)$ and construct the midpoint. Set $(\ldots R_i^3 \ldots)$ equal to the coordinates of this midpoint.

4. Etc.

The iteration is stopped when, on two successive passes through a complete cycle of shifts in all n directions, the variations are less than a given quantity. $(\ldots R_i \ldots)$ is then taken as the last point in the iteration scheme.

Note that this method of "maximum individual drift" suffers from the two disadvantages mentioned above. The adjoining figure shows some steps for the configuration of the preceding figure.

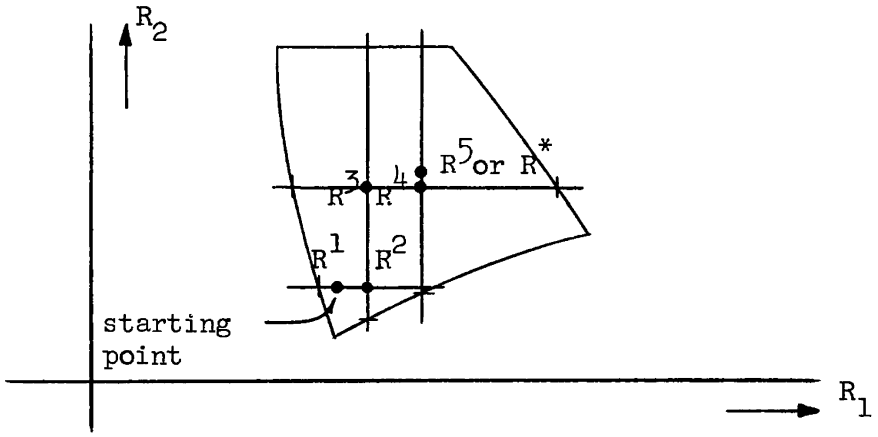


Figure 71

Iterative Steps in Optimization

6.7. Inclusion of Auxiliary Parameters

Suppose now that the A's are no longer fixed. This means that each one of the walls becomes "smeared out". Since a computer can only treat discrete cases it becomes necessary to represent each range $(\underline{A}_j, \overline{A}_j)$ by a finite number γ of points. The iterative steps described in the last section remain the same except that each one of the N walls $f_k = F_k$ is split up into γ^m walls $F_k = f_k(\ldots R_i \ldots, \underline{A}_1, \underline{A}_2 \ldots \underline{A}_m) \ldots F_k = f_k(\ldots R_i \ldots, \overline{A}_1, \overline{A}_2, \ldots \overline{A}_m)$ corresponding to all combinations of the representative points in each range. Visibly $\gamma = 4$ is already quite awkward when $m = 10$ since $4^{10} \sim 10^6$. Note however that $\gamma = 2$ (which obviously means taking the endpoints of each range) is not advisable since the walls farthest "in" or "out" do not necessarily correspond to the extreme values of the A's.

6.8 Inclusion of Spread-Curves for Nonlinear Elements

In the case of nonlinear elements, the iterative steps still remain the same, but this time the geometrical interpretation (although possible) becomes uninteresting. In order to attack this type of problem it is necessary to have available as a subroutine a nonlinear equation solver. This subroutine does the following:

> Given a set of R's, A's and the "upper" or "lower" spread-curve for each semiconductor, calculate the voltages at all the interior nodes and the currents in all interior branches.

Since the circuit inequalities were given in the first place as inequalities between precisely these interior voltages or currents (and, perhaps, constants), it is evident that one can decide, for each set of R's and A's, whether the circuit works. The variability of the A's can again be introduced by repeating the sub-routine for a given set of R's exactly γ^m times and checking whether in all γ^m cases all inequalities are satisfied. Obviously we now know whether or not for all A's and a given set of R's the circuit will work as long as the combination of "upper" and "lower" curves used in the subroutine is valid. Again the question of quantizing the interval between a given "upper" and "lower" curve comes up. In practice this would lead to too great a complexity and therefore for a given set of R's only the $\gamma^m . 2^\sigma$ combinations of A's and the

"upper" and "lower" parts of the σ spread-curves are tried. It is easy to see that nothing is changed in the search for the optimum solution: all one has to do is to walk along parallels to the R_i-axis and determine for each point $(\ldots R_{i-1}, R_i \pm x, R_{i+1}\ldots)$ (x variable) whether - for all γ^m 2^σ combinations of A's and spread-curves - the circuit inequalities are satisfied. The midpoint of the points for which the inequalities become equalities is the next point in the iterative scheme.

6.9 Determination of Tolerances at the Optimum Point

The computer gives, simultaneously with the coordinates $(\ldots R_i^*\ldots)$ of the optimum point, the half-lengths d_i^* of each arm of the hypercross. Let π_i be the commercially available tolerance on R_i (in general $\pi_i = \pi$ independent of i!). Then we can define "overswing factors" λ_i such that

$$d_i^* = R_i^* \pi_i \lambda_i .$$

if $\underline{\lambda} = \text{Min}\ (\ldots\lambda_i\ldots)$, $\underline{\lambda}$ can be used as a measure of the quality of the optimization. Visibly if $\underline{\lambda} < 1$, the circuit cannot be built with commercial elements.

A second measure of the quality can be obtained by trying to fit a hyperrectangle - centered at $(\ldots R_i\ldots)$ with sides ratios $\pi_1:\pi_2:\pi_3\ldots$ - inside the walls. The half-lengths of the sides, $d_{i\ \text{rect.}}$, would then give a "simultaneous worst case" overswing

$$\underline{\lambda}\ \text{rect.} = \text{Min}\ \left(\ldots\frac{d_{i\ \text{rect.}}^*}{R_i^*\ \pi_i}\ldots\right).$$

Such a rectangle can be directly constructed by drawing the diagonals of an arbitrarily small rectangle of sides ratios $\pi_1:\pi_2:\pi_3\ldots$ and finding their intersections with the walls. Unhappily there are 2^{n-1} diagonals in n-space and this method is therefore cumbersome.

Still another quality estimate can be made by assuming that the walls lie entirely outside the solid formed by constructing hyperplanes connecting the endpoints of the arms of the hypercross. It can be seen that under this assumption $\underline{\lambda}/\sqrt{n}$ is a lower bound on the "simultaneous worst case overswing".

It should be noted (see Figure for n = 2) that all these quality calculations as well as the iterative process itself assume that the walls are

reasonably well behaved, i.e. do not have "fingers" or "teeth" coming in. This reasonable behavior is, of course, a function of how the circuit inequalities are set up; in some cases it may be necessary to choose them a priori in a way which seems to guarantee smoothness of the walls.

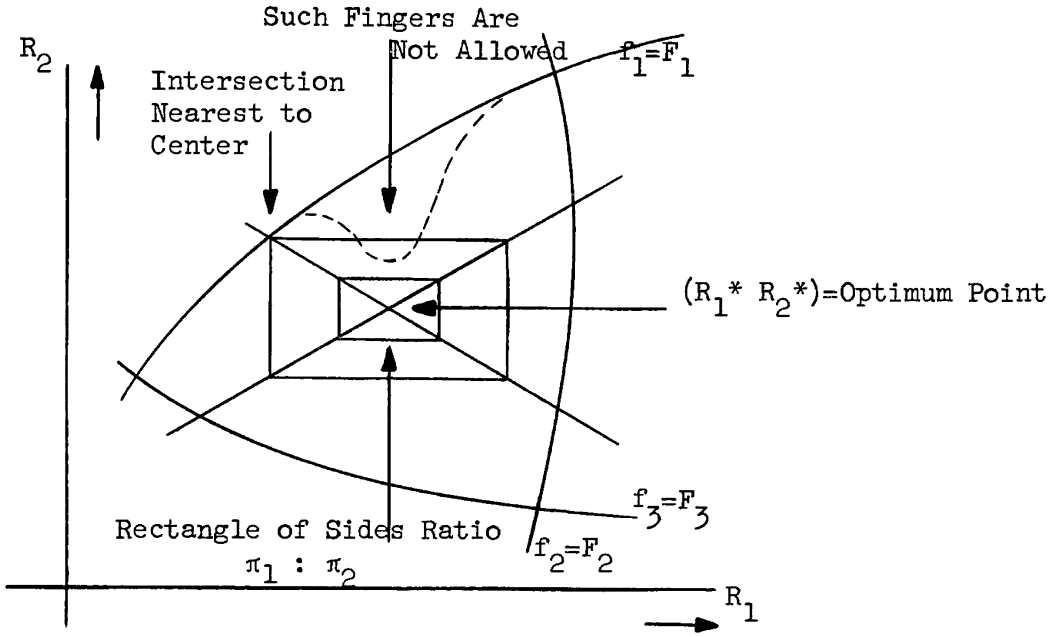


Figure 72

Tolerances at Optimum Point

It was mentioned before that some circuit inequalities might be considered modifiable. Suppose in particular that the F's contain a subgroup $G_1 \ldots G_e \ldots G_\mu$ (where $\mu << m!$) with the property that $\underline{G}_e \leq G_e \leq \overline{G}_e$ but that inside the range any value is acceptable. One can then repeat the calculations of $\underline{\lambda}$ for combinations of the - quantized - G's and decide at the end "how much G for how much λ" one is willing to trade. In particular it may happen that for an initial set of G's $\underline{\lambda} < 1$, then such a calculation would allow to examine the feasibility of a circuit as a function of the G's.

6.10 Inclusion of Transient Conditions

In general the circuit designer not only demands optimum static performance (i.e., the "maximum individual drift" property) but must also impose two further conditions:

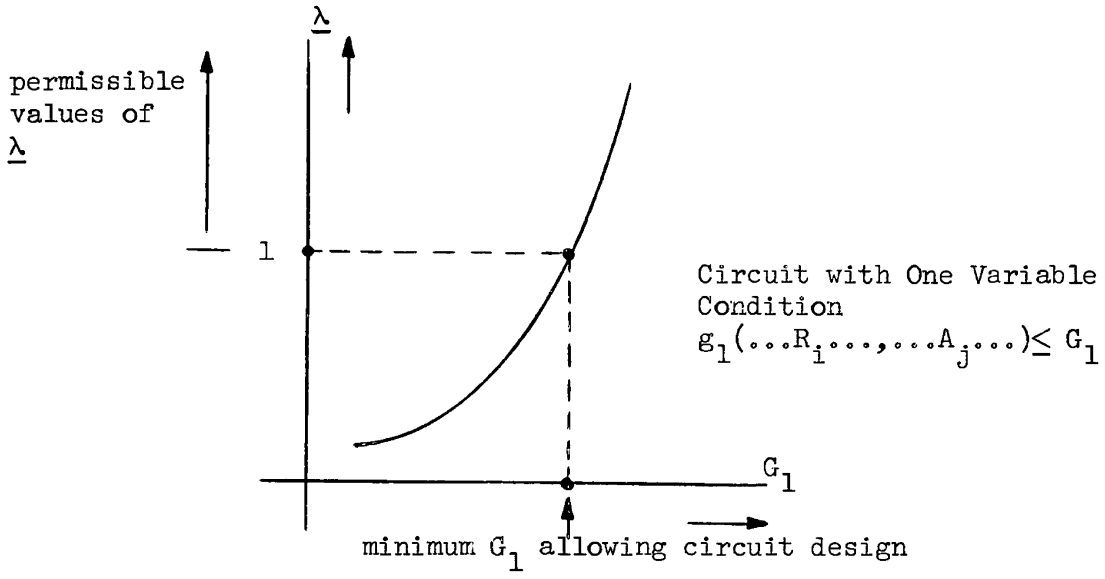


Figure 73

Influence of Auxiliary Parameter on Tolerance

1. The circuit must be capable of changing its state with given boundary conditions (gating currents, etc.).

2. The transients during the change of state may not upset a subgroup of the circuit inequalities and additional inequalities must perhaps be satisfied during the change.

These two conditions can again be expressed as inequalities between interior voltages or currents, the only difference being that all voltage divider networks must be considered shunted by stray capacitances (or perhaps speed up capacitors!) and that, of course, diffusion and depletion capacitances in transistors must be considered. Furthermore it must be realized that certain diodes act like short-circuits immediately after having conducted heavy forward currents. In principle however there is no difficulty in adjoining these "dynamic inequalities" to those already present, remembering that it is only their "R-part" which is used in the optimization: capacitances are fixed and equal to their worst case value.

6.11 Inclusion of the Speed Function

It can be established that to a good approximation the operation time θ ($\sim$ delay + 1/2 rise time) is a function of the R's and the A's as well as of a set of dynamic parameters T_h. Practically it is quite sufficient to define (see Section).

a) for diodes: Their "intrinsic time constant" T_D. In the idealized case of a planar diode with linear minority carrier distribution, the minority charge Q accumulated during the forward conduction (which has to be discharged before the diode "unhooks") is given by

$$Q = T_D \, i_{fwd} \quad .$$

b) for transistors: T_T: The "intrinsic time constant" of the emitter-base diode. This T_T takes account of the "quasi Miller effect" when one tries to turn off a conducting transistor.

T_B: The base delay of the (non-saturated) transistor, approximately $T_B \, f_{ac} = 1$.

C_C: The collector capacitance (depletion layer capacitance, header and wiring).

Then it can be seen that $\theta = \theta \, (\ldots R_i \ldots, \ldots A_j \ldots, \ldots T_h \ldots)$ which means that the class of circuits with operation times less than T is described by simply adding one more circuit inequality: $\theta \, (\ldots R_i \ldots, \ldots A_j \ldots, \ldots T_h \ldots) \leq T$.

7. HARDWARE SPECIFICATIONS

7.1. Transistor Specifications

Transistors are of the type Western Electric GF 45011 or the equivalent Texas Instruments X 310. Both satisfy the following specifications:

Parameter	Test Conditions	Initial Spec.	End of Life Spec.
BV_{CB}	I_E = 0 I_C = -100 μAdc	≥ -30 Vdc	≥ -25 Vdc at -500 μAdc
I_{CBO}	I_E = 0 V_{CB} = -20 Vdc	≤ -5.0 μAdc	≤ -10 μAdc at -20 Vdc
$DC(1-\alpha)$	I_E = 10 ma DC V_{CB} = -4 Vdc	≤ .04	≤ .06 at 10 ma DC, -4 Vdc
V_{EB}	I_E = 10 ma DC V_{CB} = -4 Vdc	.30 -.45 Vdc	.30-.50 Vdc at 10 ma DC, -4 Vdc
BV_{EB}	I_E = -100 μAdc V_{CB} = 0	≥ -4.5 Vdc	≥ -4.1 Vdc at -500 μAdc
C_D	I_E = 0 V_{CB} = -10 Vdc	≤ 2.0 μμf	same
h_{fe}	I_E = 10 ma DC V_{CB} = -10 Vdc f = 100 mcps	≥ 8 db	same
r'_b	I_E = 10 ma DC V_{CB} = -10 Vdc f = 250 mcps	≤ 150 ohms ≥ 100 ohms	same

P	25° C ambient	$\geq$ 200 mw	same

where

BV_{CB} = base-collector breakdown voltage

I_{CBO} = "open-emitter" collector current

$DC(1-\alpha)$ = $(1-\alpha)$ for DC conditions i.e. I_C/I_E

V_{EB} = emitter-base forward drop

BV_{EB} = emitter-base breakdown voltage

C_D = collector depletion layer capacitance

h_{fe} = grounded emitter forward current gain, i.e. AC $\frac{\alpha}{1-\alpha}$ at given frequency in db

r'_b = base spread resistance

P = collector dissipation

Derating: The maximum collector dissipation allowed to account for temperatures up to 40° C (ambient) is 120 mw. The maximum emitter-base breakdown voltage actually used in the circuits is 3.2v.

7.2. Diode Specifications

The diodes are of the type TRANSITRON S577G and correspond to the following specifications:

A. Static characteristics
   1. For a current of 5 milliamperes in the forward direction, the voltage across the diode shall be .39 $\pm$ .02v.
   2. For a current of 10 milliamperes in the forward direction, the voltage across the diode shall be 0.43 $\pm$ 0.02v.
   3. For a current of 100 microamperes in the reverse direction, the voltage across the diode shall be greater than 25v.

B. Transient characteristics
   1. From being initially biased 5v in the reverse direction, each diode shall switch so as to conduct 10 milliamperes in the

forward direction in not more than 35×10^{-9} seconds. The circuit resistance for this test shall be 100 ohms.

2. From initially conducting 10 milliamperes in the forward direction, each diode shall be switched so that it is biased 5 volts in the reverse direction. Within 40×10^{-9} seconds, after switching to the specified reverse bias, the current in the reverse direction shall not exceed 600 microamperes, and within 160×10^{-9} seconds, the reverse current shall not exceed 50 microamperes. The circuit used for this test shall be that used for JAN-256.

C. Each diode shall be capable of dissipating 80 milliwatts at an ambient temperature of 25° C.

Derating: The maximum reverse rating used in the circuits is 17v (at 100 μa). The maximum forward current 25 ma.

7.3. Resistor Specifications

All resistors which carry currents which vary by more than 20 per cent (collector to base stepdown resistors) must be carbon deposited 1 per cent resistors. An exception to this rule are the collector (stabilization) resistors in emitter-followers.

All resistors which carry current which vary by less than 20 per cent (emitter resistors, collector load resistors) may be non-inductive wire-ground resistors accurate to 1 per cent dc-wise.

Derating: A 50 per cent derating is applied for power (constant rating up to $100^{\circ}C/2!$). For aging, voltage shock, humidity, etc., a factor of three is allowed on tolerance, i.e., it is assumed that the resistors are at all times within 3 per cent of their nominal value.

7.4. Power Supply Specifications

At the input to each circuit a 1 per cent stability must be guaranteed for dc to 1 mc variations. This stability must also apply to long term drift.

Cut-out circuits must be provided such that a failure in one part of the machine automatically shuts down the whole machine.

Derating: A 3 per cent variation of voltage is allowed at the inputs to the circuit after the RC input filter.

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