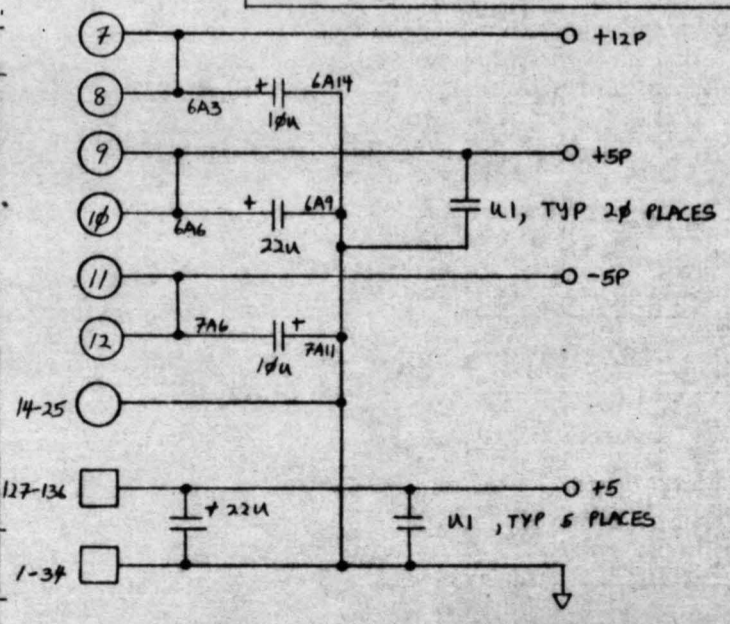
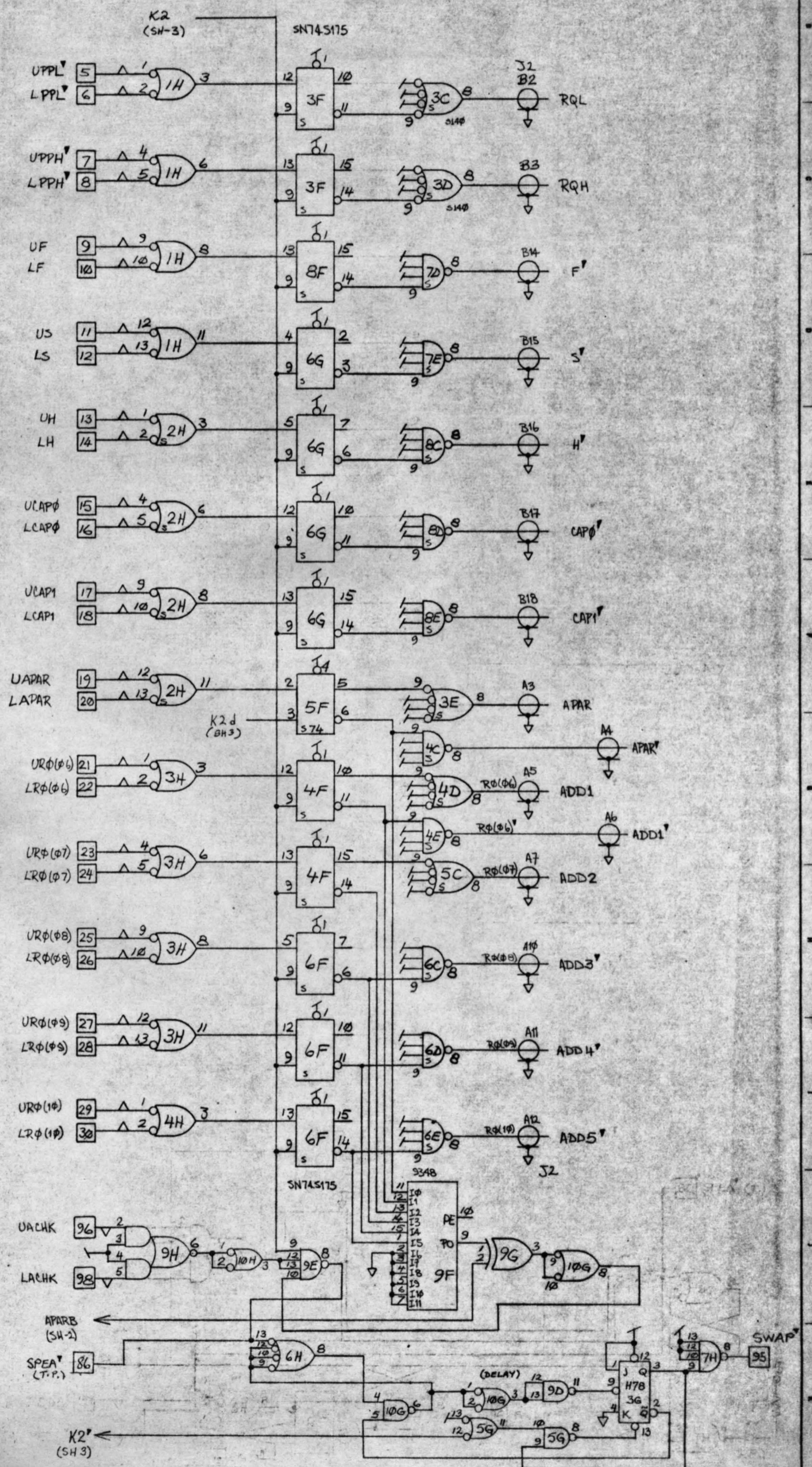
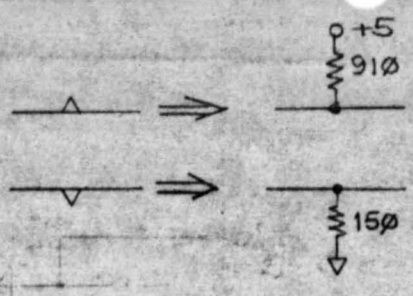


- NOTES:
- ① CINCH D825 CONNECTOR, PIN 1.
  - ⊗ POWER FROM MPMBM +5 OTHER GATES ARE POWERED FROM +5P.



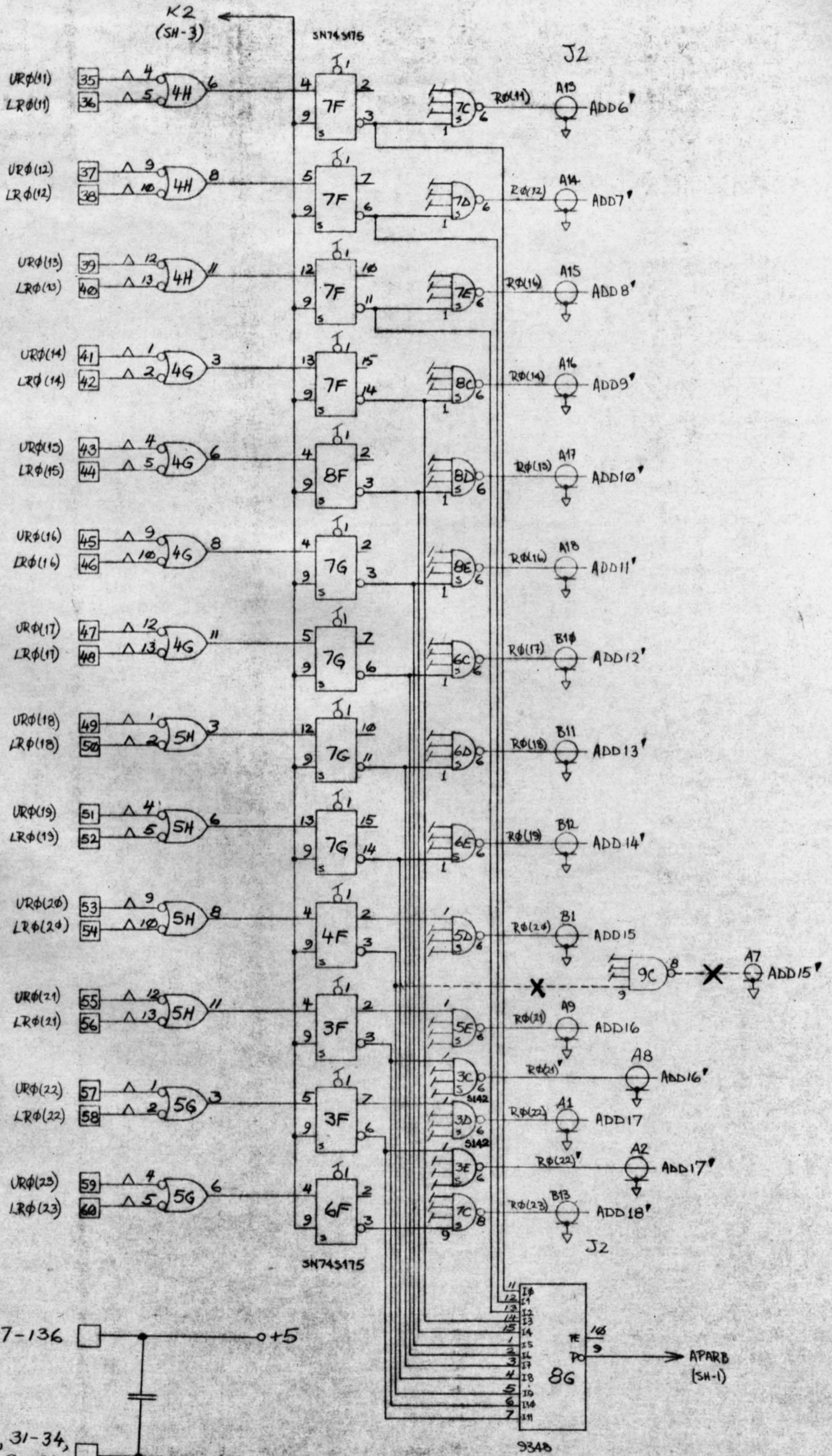
	RELEASED	REVISIONS
	PCANDESTRAH H. HATSU YAMA MPMBM AI Lphi 58.2	TITLE <b>MPMBM LOCAL CONTROL</b>



Drives cable to FM

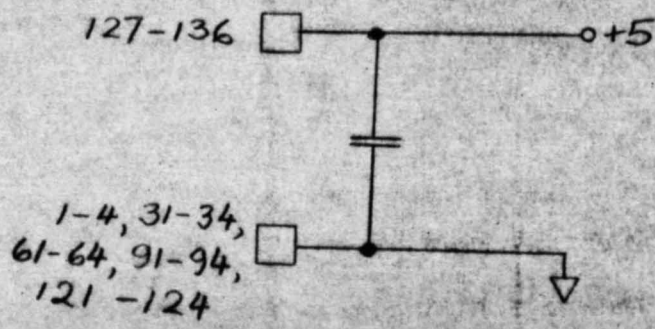
RELEASED DATE: _____ BY: _____	REVISIONS NO. _____ DATE: _____ BY: _____
THE ALPHA SYSTEM BCC-500 MODEL: _____ SERIAL: _____ OPERATOR: _____ MAINTENANCE: _____	REQUEST/ADDRESS REGISTER MPMBM A2 LPH55.1

A2



Drives cable to FM

RELEASED	REVISIONS
1	REQUEST/ADDRESS REGISTER
2	MPMBM, A2
3	LDφ550, 1

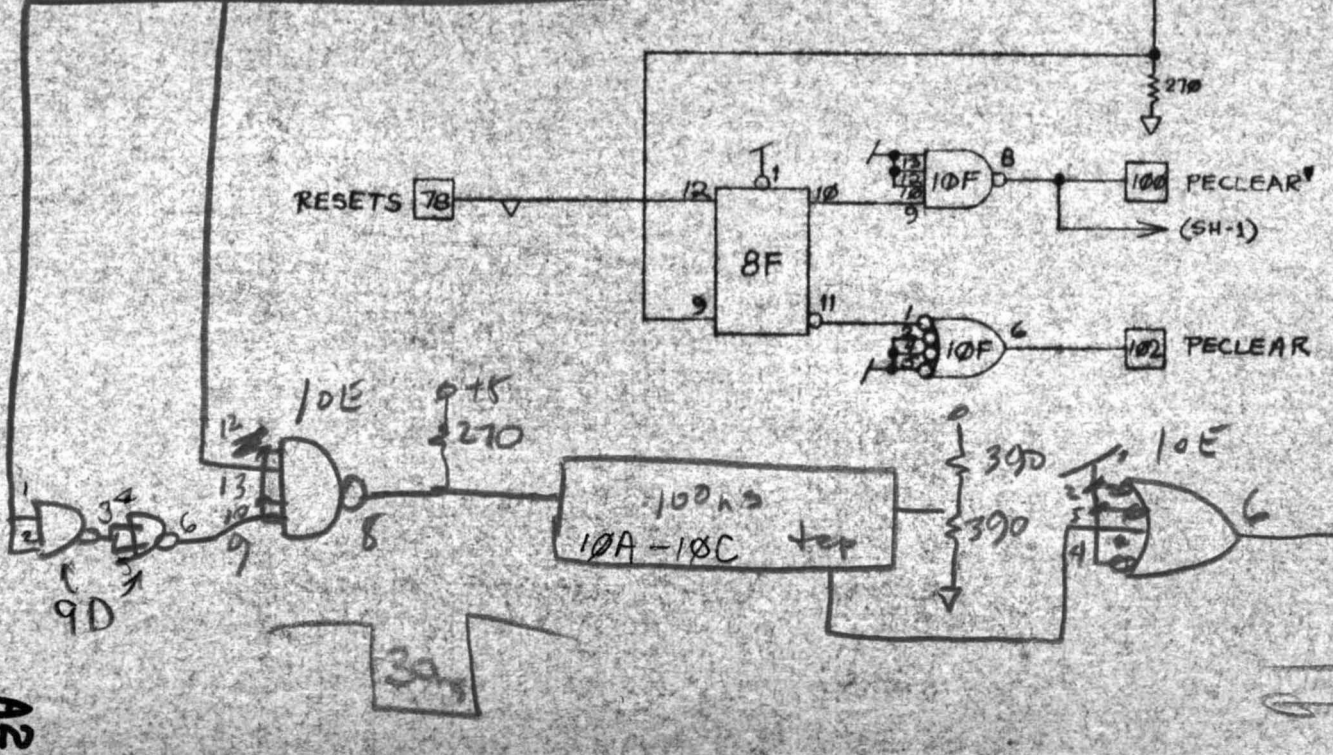
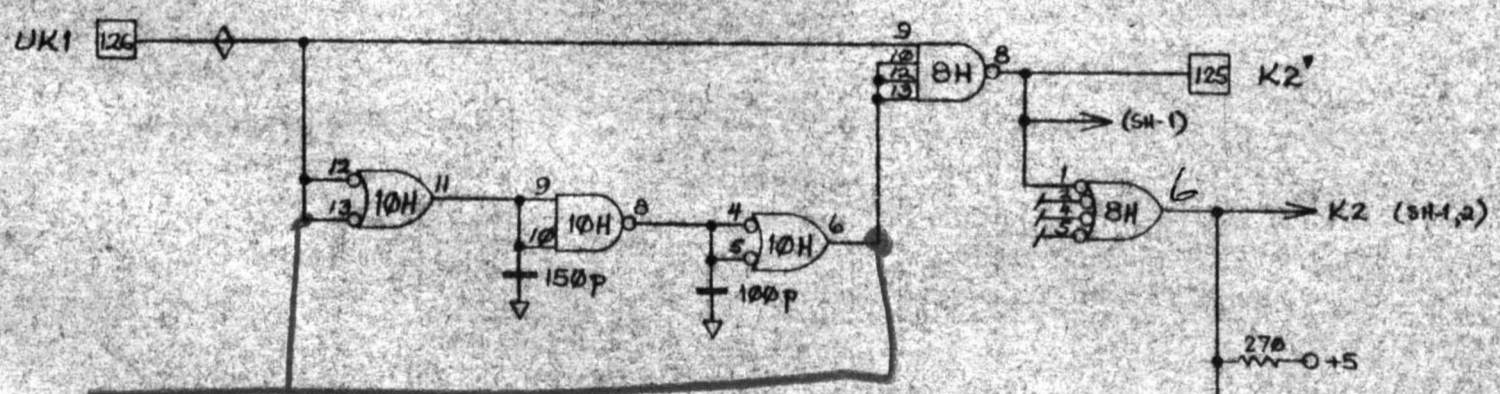
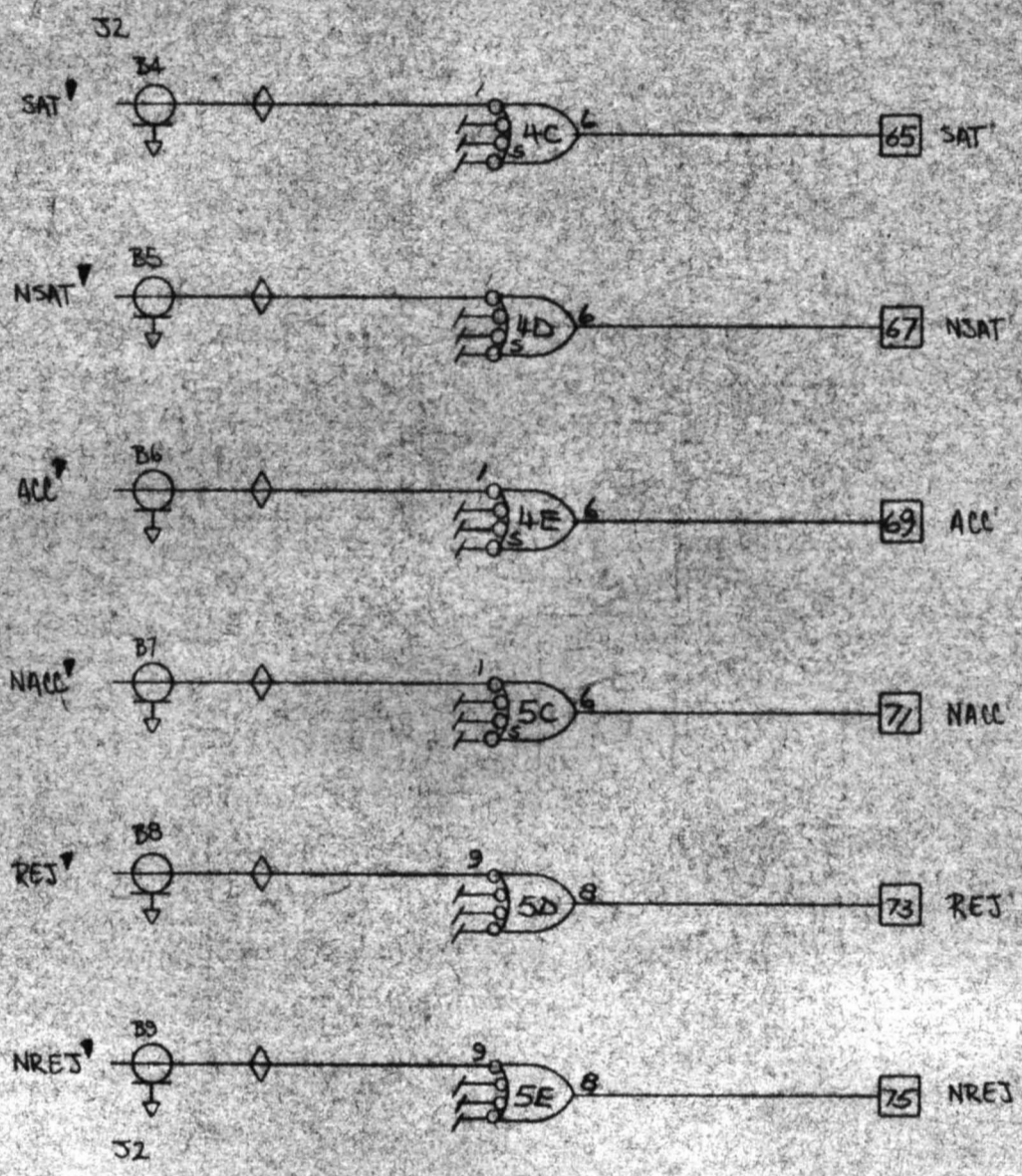
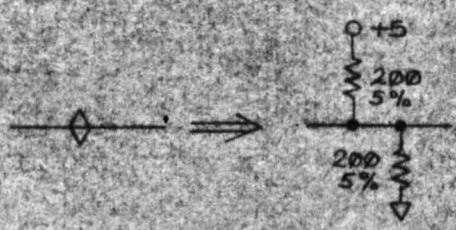


The Alpha System BCC-500

MPMBM, A2

LDφ550, 1

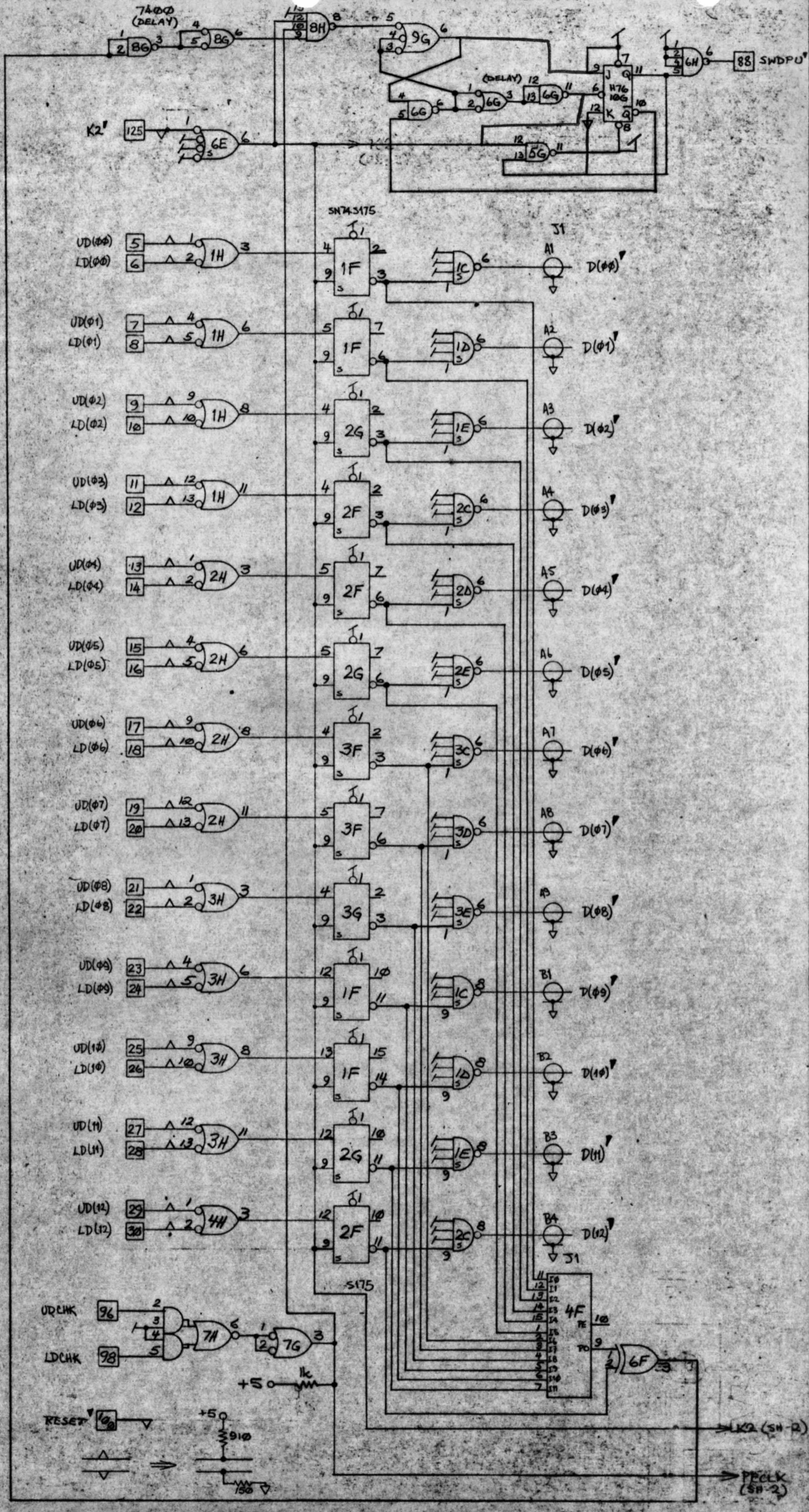
receives from FM



basically a later K2

66 DINHIBIT

	RELEASED AB Cooper 4 ESI MPMEM, A2 L01955.1
Request/Address Register	A2



drives cable to FM

<p>The Alpha System RCC-500</p>	<p>ABSTRACTED</p>
	<p>REPRODUCTION</p>
<p>DATA REGISTER</p>	<p>MPMBM, A3</p>
<p>1 3</p>	<p>101054-1</p>

A3

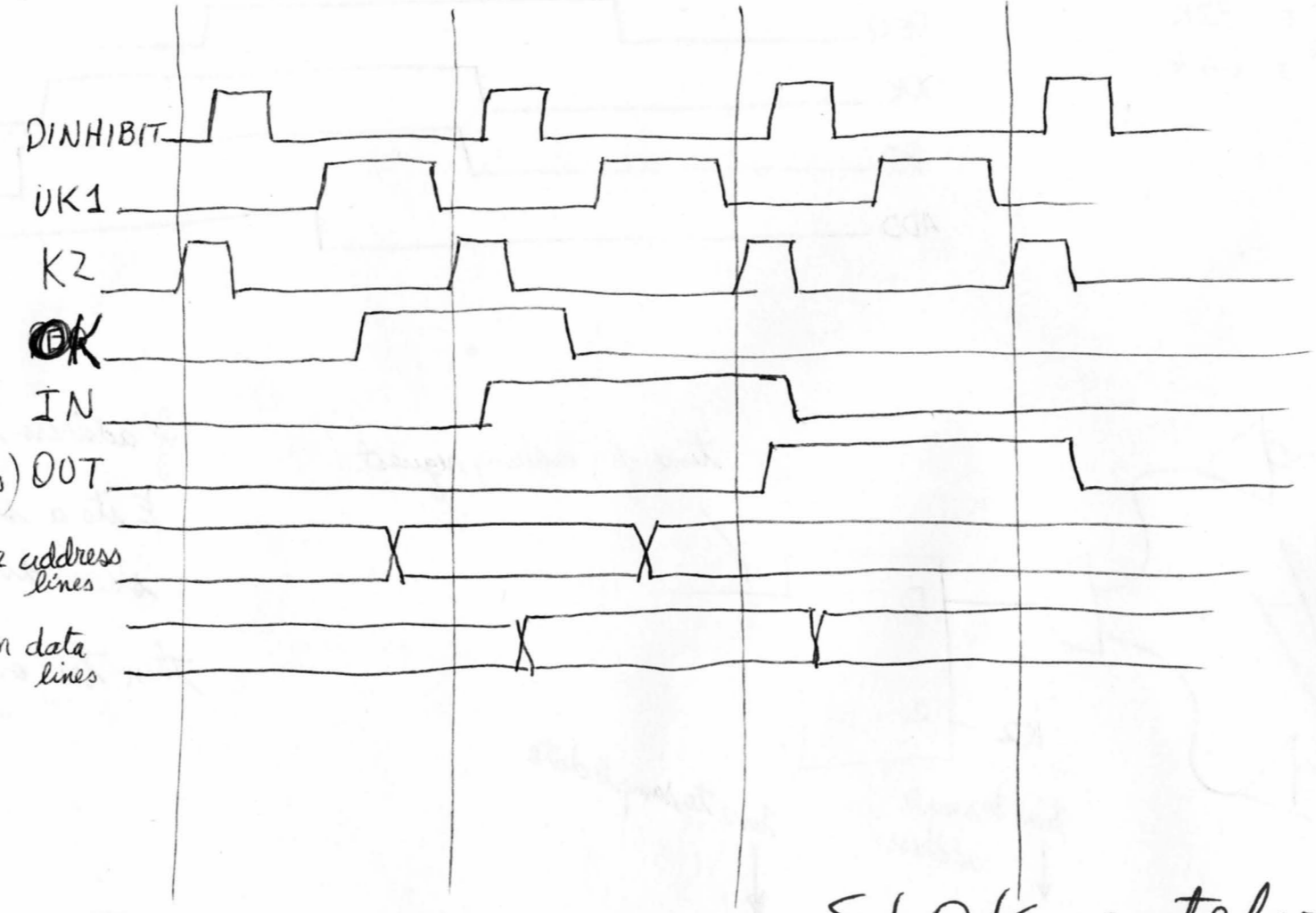
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MAY 4, 1978 9:31:34  
THURSDAY  
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MAY 4, 1978 9:31:34  
THURSDAY  
@CROSSBY:KEY:9S7M  
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@CROSSBY:KEY:9S7M

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MAY 4, 1978 9:31:34  
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@CROSSBY:KEY:9S7M

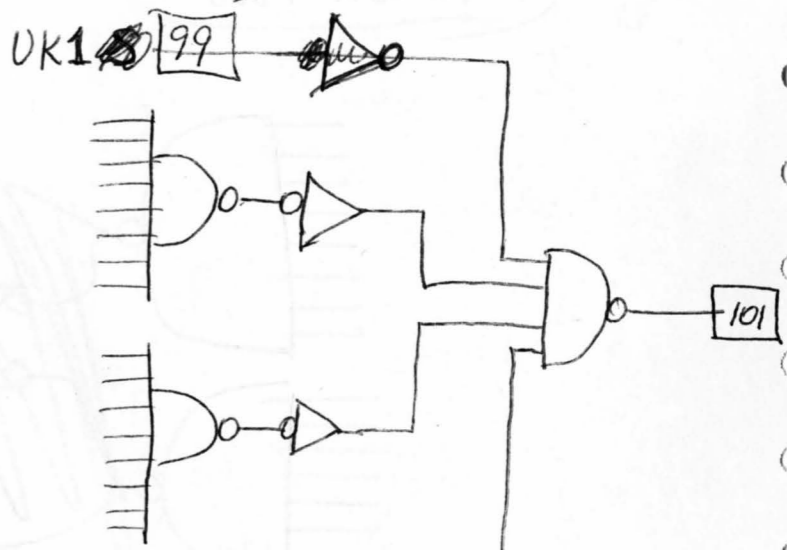
fetch requests go as  
RQH, F  
store requests go as  
RQH, S

to F.M.  
(when address is valid)  
(when data is valid)

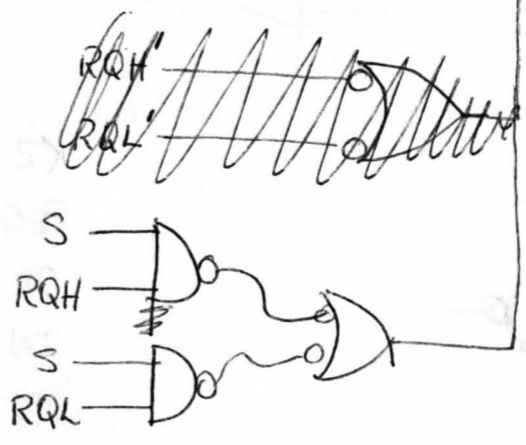


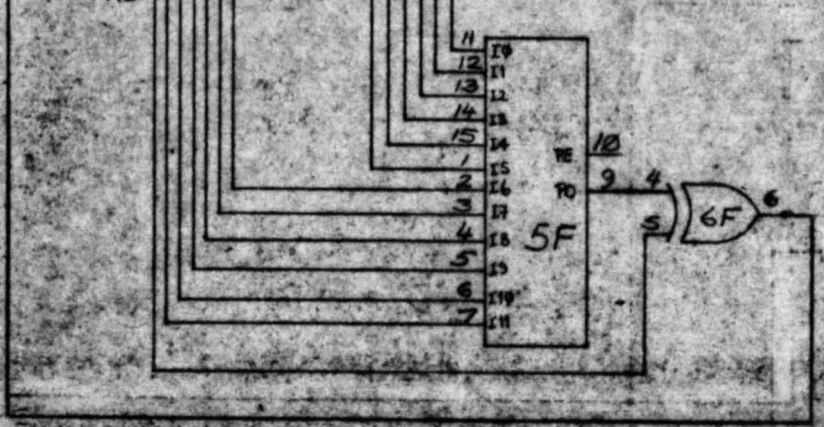
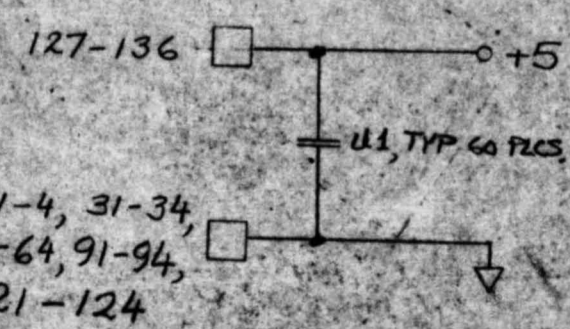
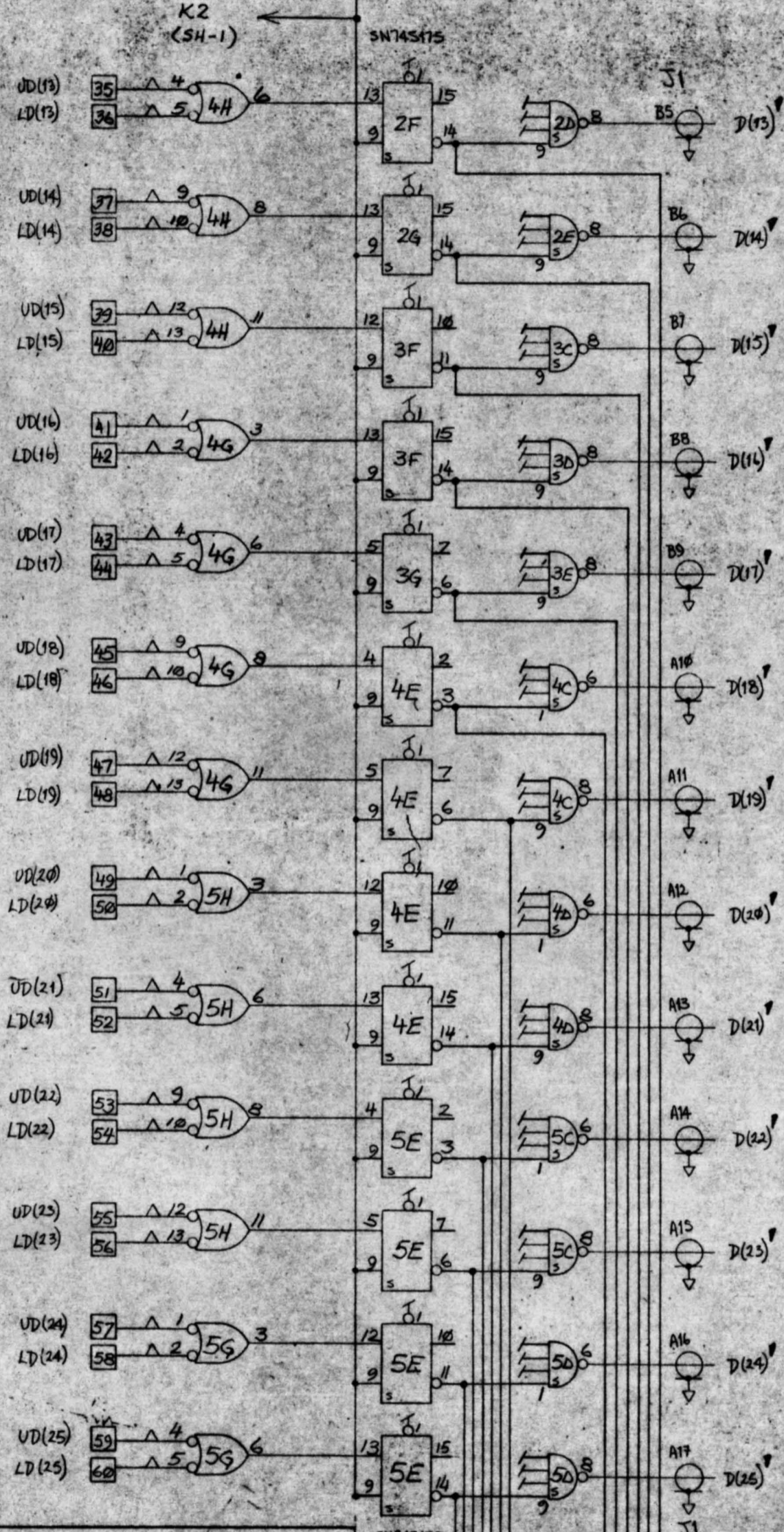
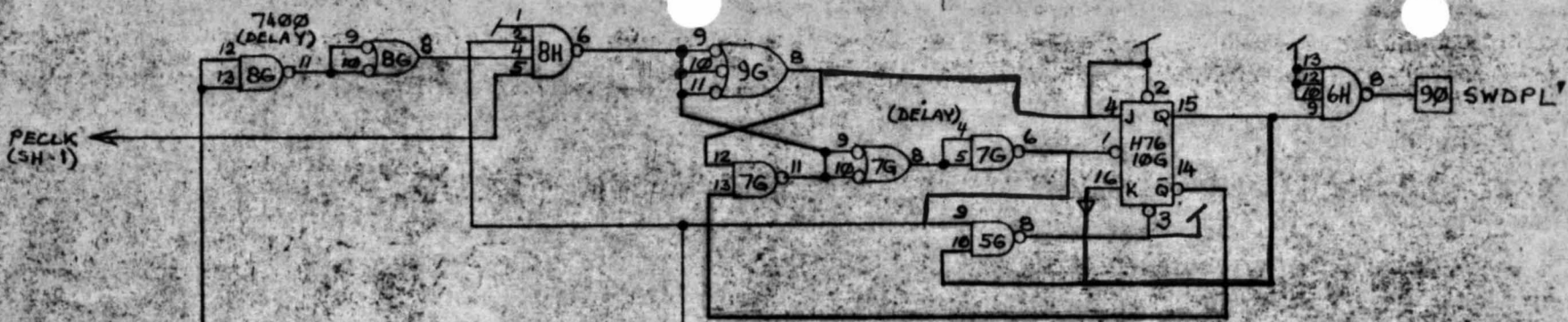
~~to check what M5CH is storing:~~  
sample the data lines on backpanel  
decode — clock  
UK1 —

$$\text{decode} = \text{addr}6 \wedge 5 \wedge (\text{RQH} \vee \text{RQL})$$



SLOK catcher  
ckt: placed on AZ  
to decode addresses 6 & 7.

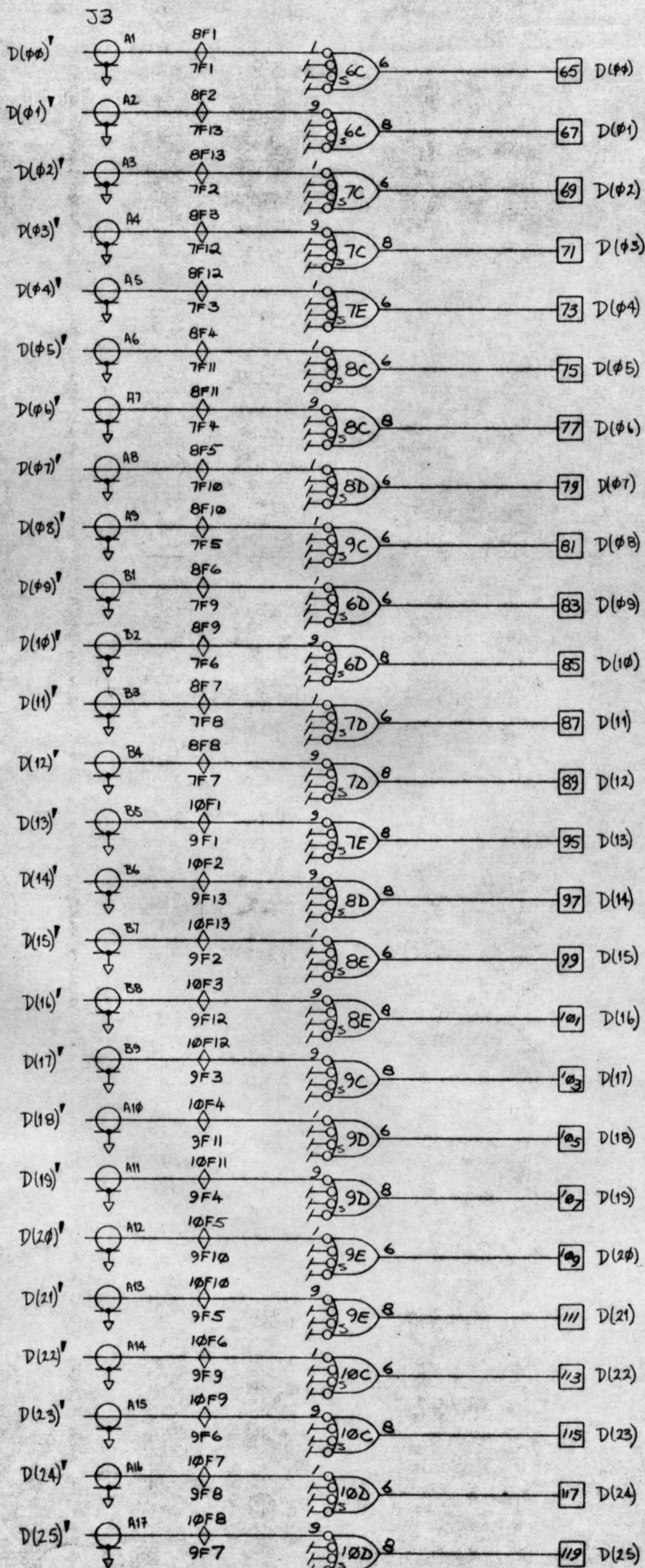
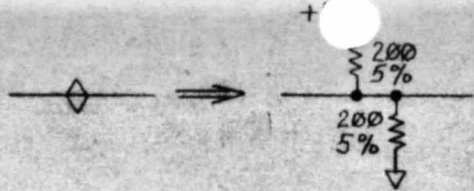




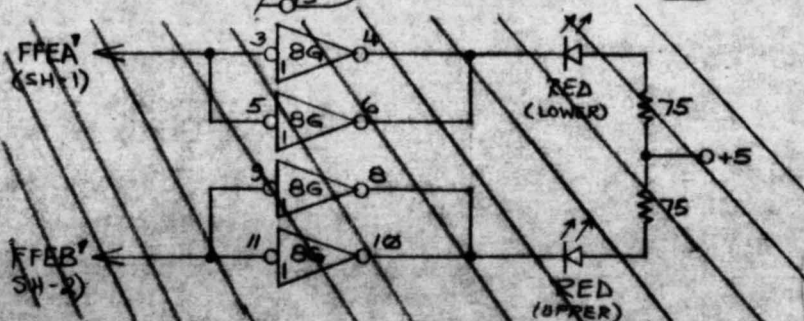
drives cable to FM

<p>The Alpha Systems REC-500</p>	<p>RELEASED</p>
<p>AE Form 1041 REV. 1-64</p>	<p>REVISIONS</p>
<p>DATE: 1-64</p>	<p>NO.:</p>
<p>MPMBM A3</p>	<p>DATA REGISTER</p>
<p>2 3</p>	<p>101054-1</p>

A3



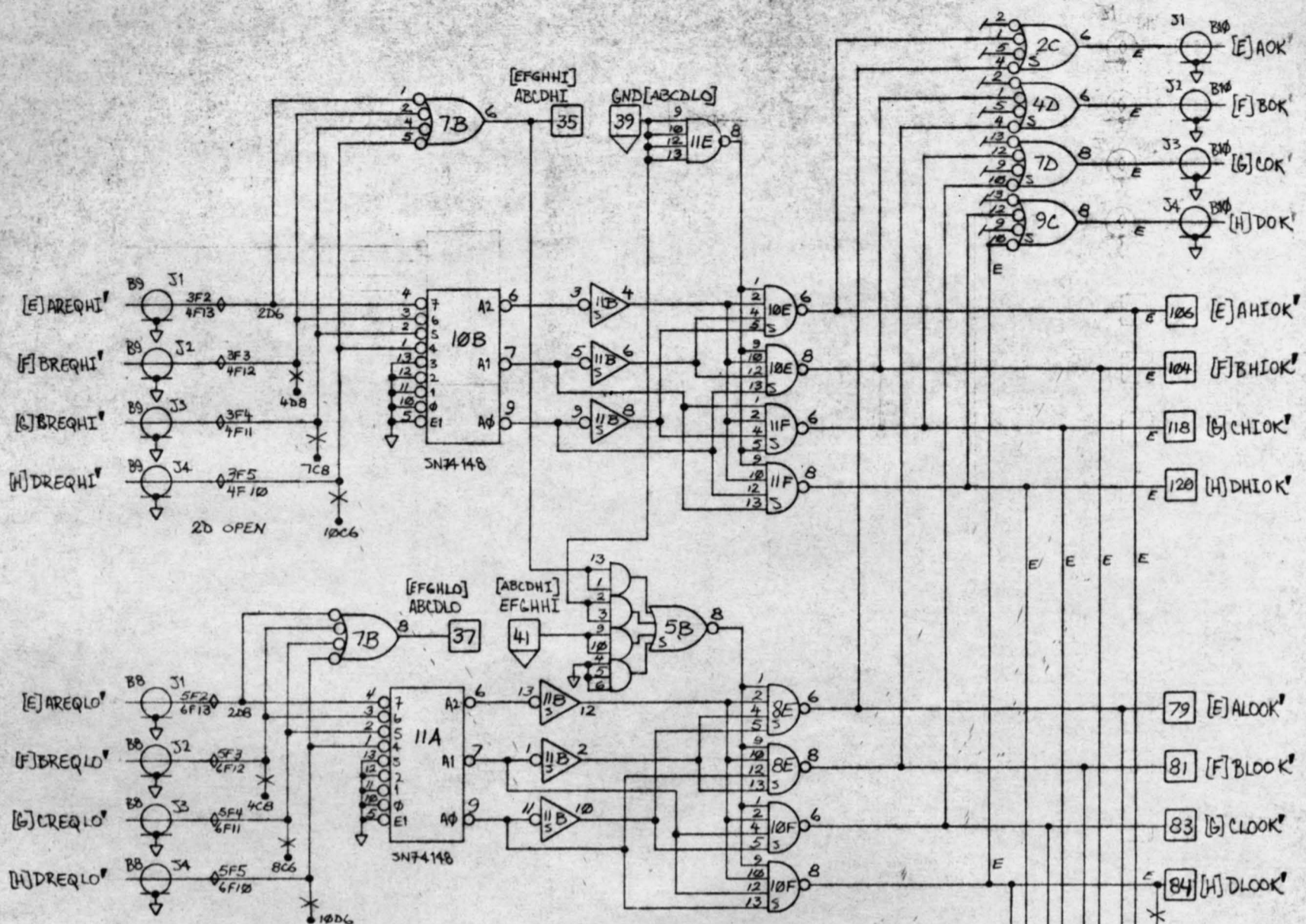
received from FM



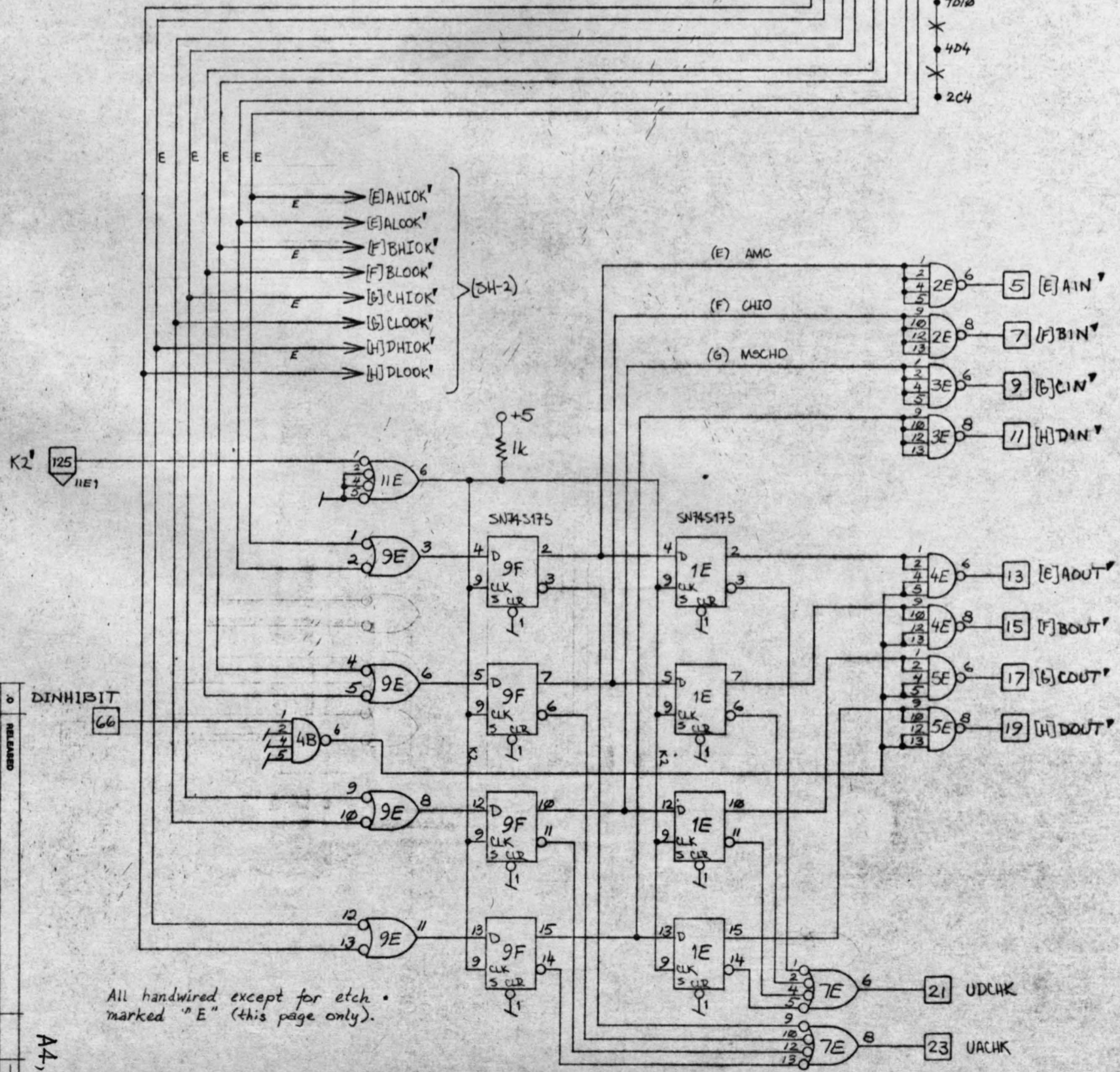
RELEASED	DATE	BY
REVISION	DATE	BY
 The Alpha System BCC-300	AB Electronics K. E. H. S. A.	DATA REGISTER MPMBM, A3
3	3	L61654-1

A3





receives requests from processors —  
drives responses to "

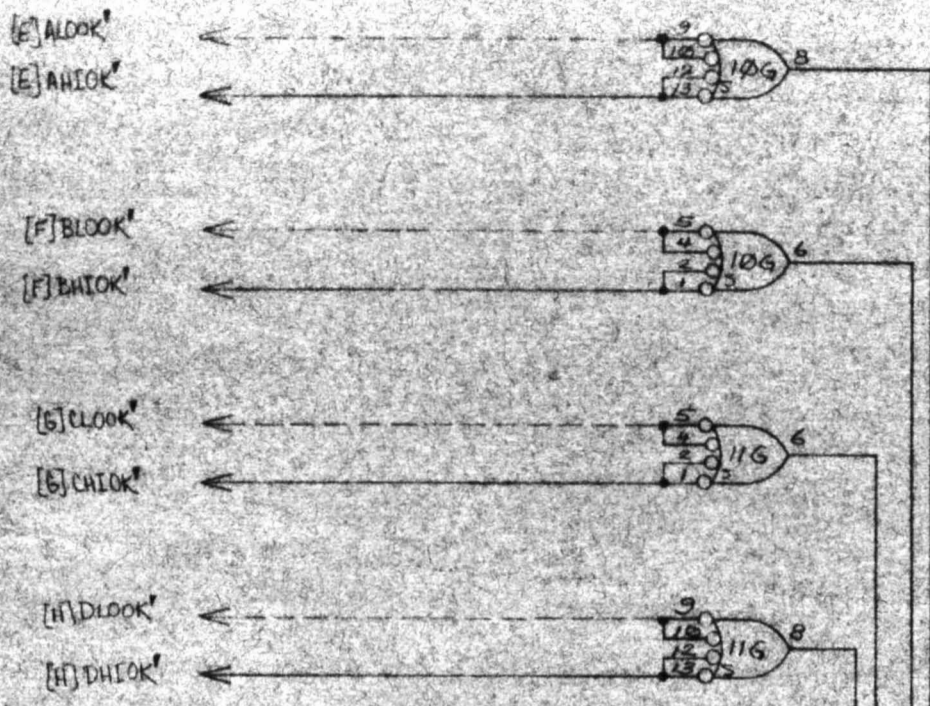


All handwired except for etch.  
marked "E" (this page only).

RELEASED	REVISIONS
1. EBM 2. EBM 3. EBM 4. EBM	REQUEST CARD MASTER Lφ1047.1
DATE	APPROVED

A4, A5

(SH-1)



- [E]APPH
- [E]APPL
- [E]AF\*
- [E]AS\*
- [E]AH\*
- [E]ACAPP\*
- [E]ACAPP\*
- [E]ACAPP\*
- [E]AFCL\*

Signal	A8	A5	A2	A7	A4	A3	A4	A5	A10
[E]APPH	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[E]APPL	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[E]AF*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[E]AS*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[E]AH*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[E]ACAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[E]ACAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[E]ACAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[E]AFCL*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3

- [F]BPPH
- [F]BPPL
- [F]BF\*
- [F]BS\*
- [F]BH\*
- [F]BCAPP\*
- [F]BCAPP\*
- [F]BCAPP\*
- [F]BFCL\*

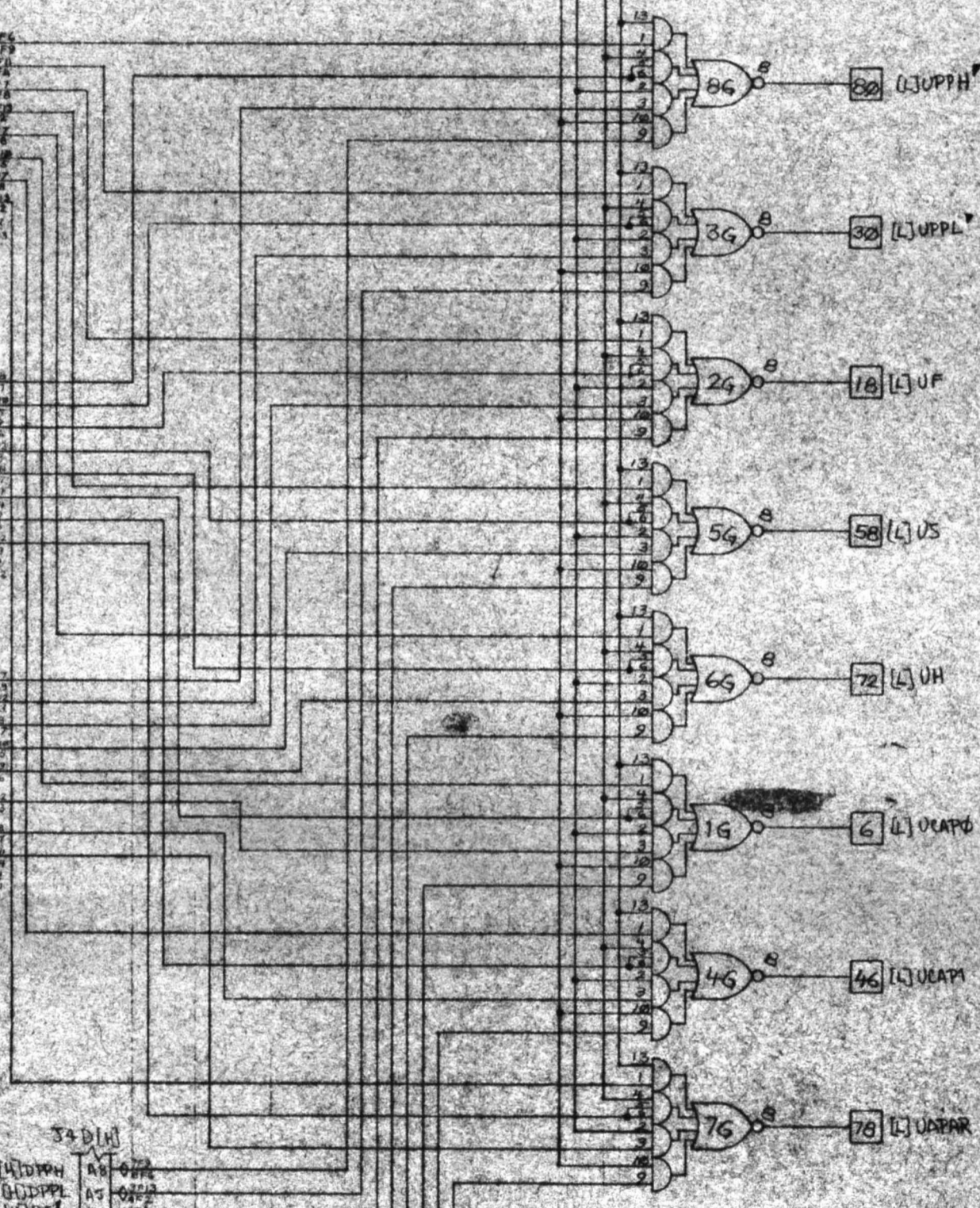
Signal	A8	A5	A2	A7	A4	A3	A4	A5	A10
[F]BPPH	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[F]BPPL	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[F]BF*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[F]BS*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[F]BH*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[F]BCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[F]BCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[F]BCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[F]BFCL*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3

- [G]CPPH
- [G]CPPL
- [G]CF\*
- [G]CS\*
- [G]CH\*
- [G]CCAPP\*
- [G]CCAPP\*
- [G]CCAPP\*
- [G]CFCL\*

Signal	A8	A5	A2	A7	A4	A3	A4	A5	A10
[G]CPPH	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[G]CPPL	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[G]CF*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[G]CS*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[G]CH*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[G]CCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[G]CCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[G]CCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[G]CFCL*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3

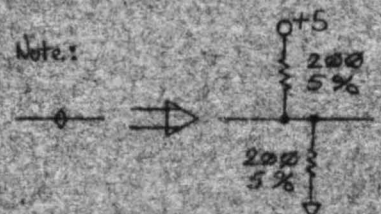
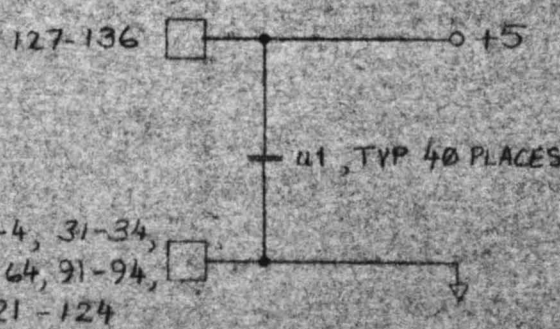
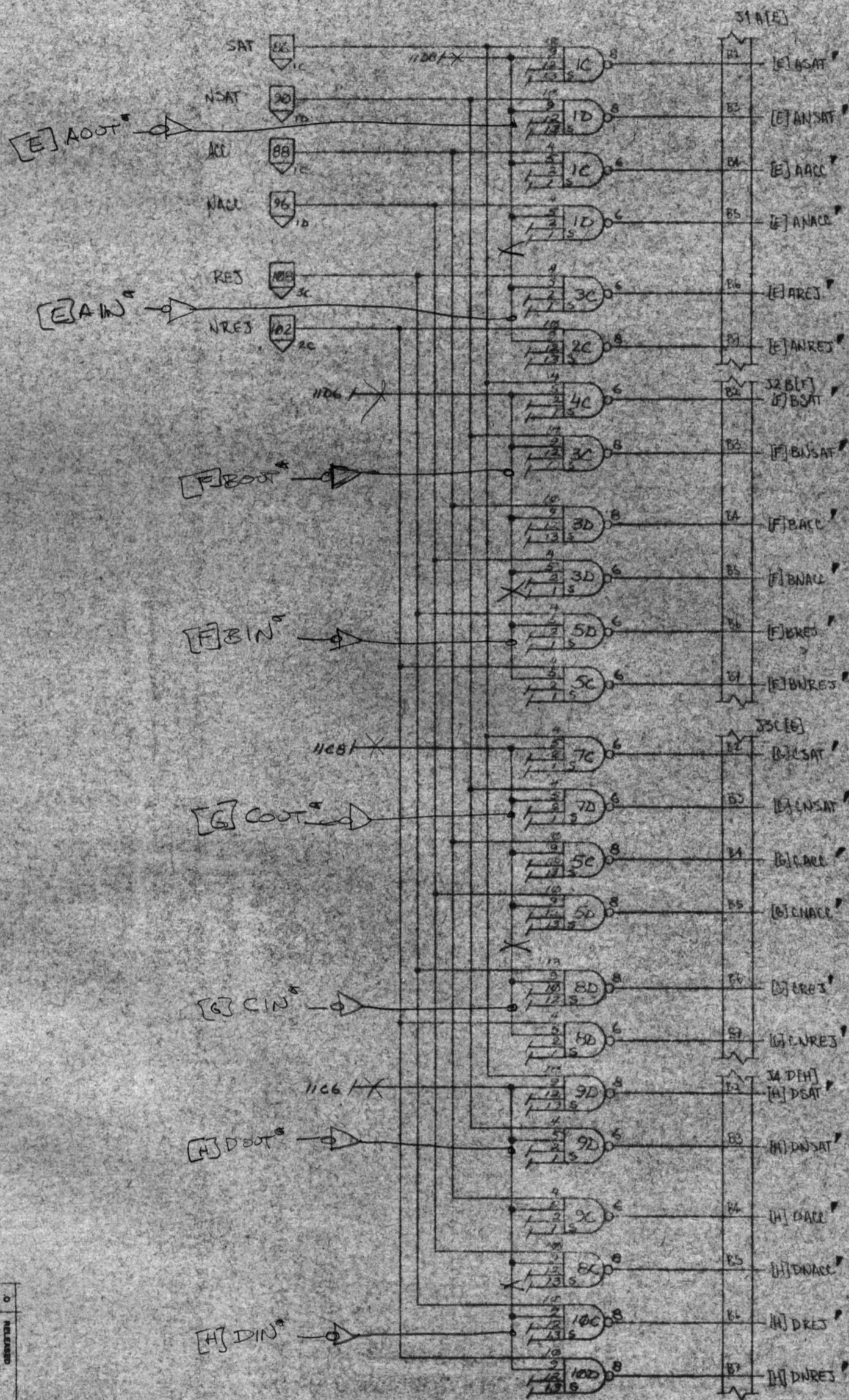
- [H]DPPH
- [H]DPPL
- [H]DH\*
- [H]DS\*
- [H]DH\*
- [H]DCAPP\*
- [H]DCAPP\*
- [H]DCAPP\*
- [H]DHCL\*

Signal	A8	A5	A2	A7	A4	A3	A4	A5	A10
[H]DPPH	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[H]DPPL	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[H]DH*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[H]DS*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[H]DH*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[H]DCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[H]DCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[H]DCAPP*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3
[H]DHCL*	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3	0/2/3



The Alpha System RSC 500	
REQUEST CARD	MRB/M
2	24
1818 47 0	MASTER

A4, A5

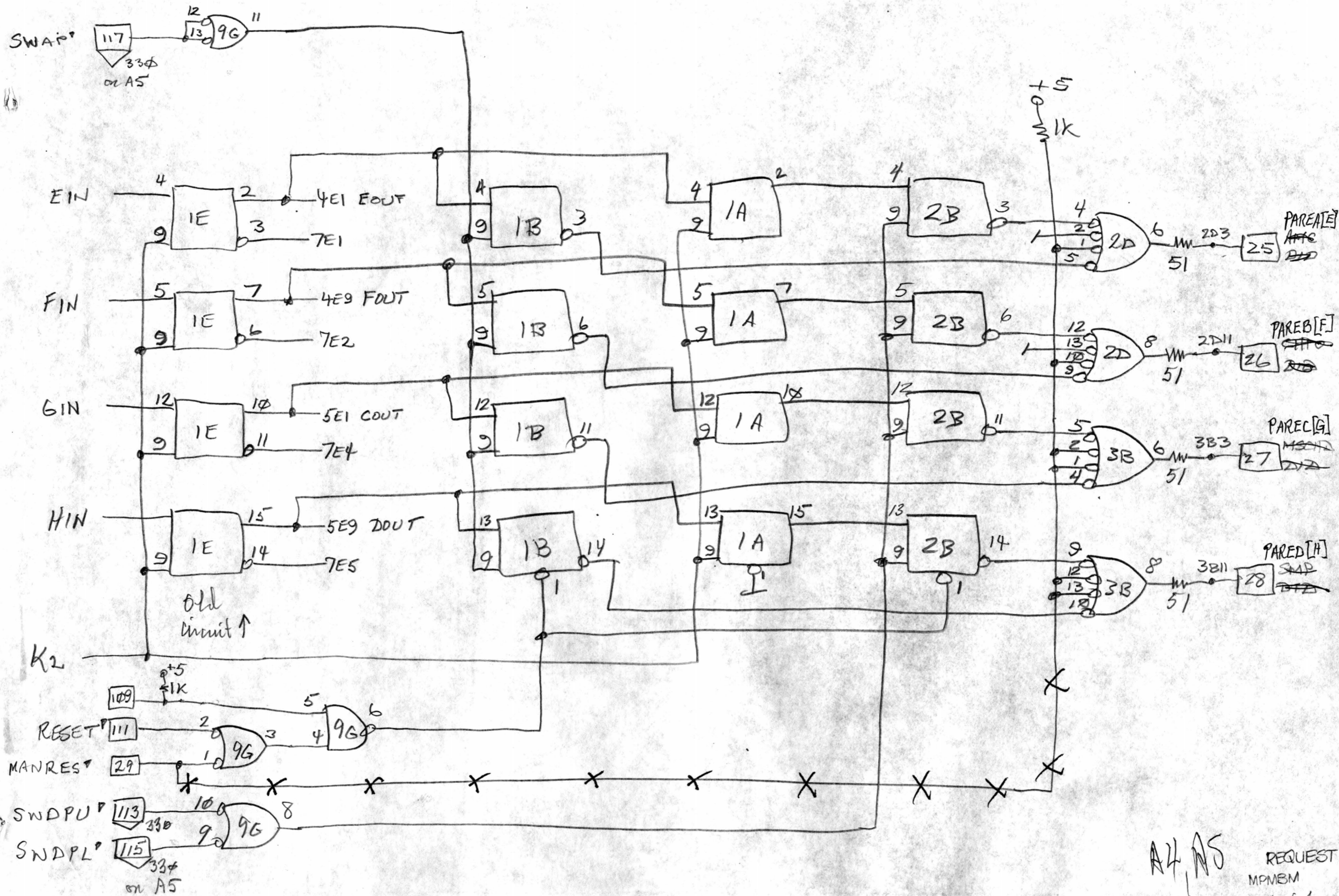


pencil - suggested change -  
 ABG 12 AUG 74

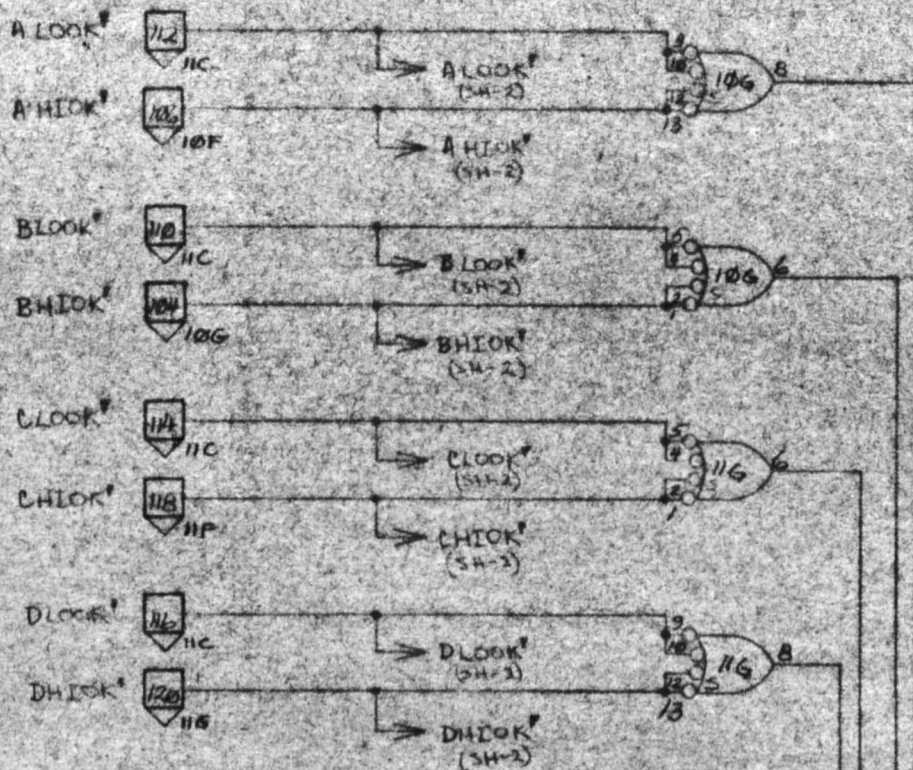
reduces confusion looking at processor responses,  
 no logical change at all

REQUEST CARD 4-DIE-4J	REVISIONS 3 24 2010 47.0
ABG 12 AUG 74 EDEN MPM/MA MASTER	3 24 2010 47.0

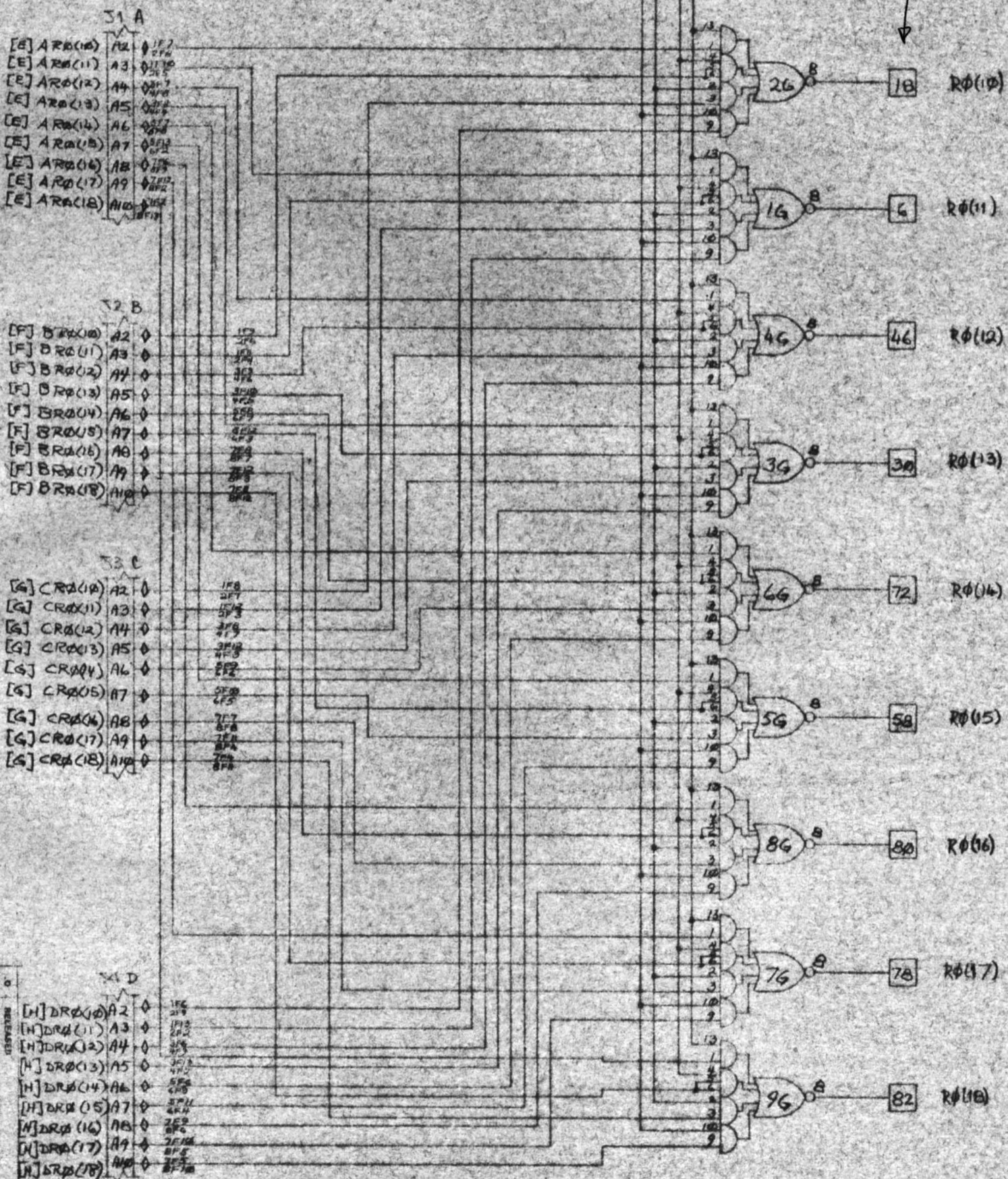
A4, A5



A4, AS  
 REQUEST CARD  
 MPMEM  
 SH. 4 of 4 L01047.1



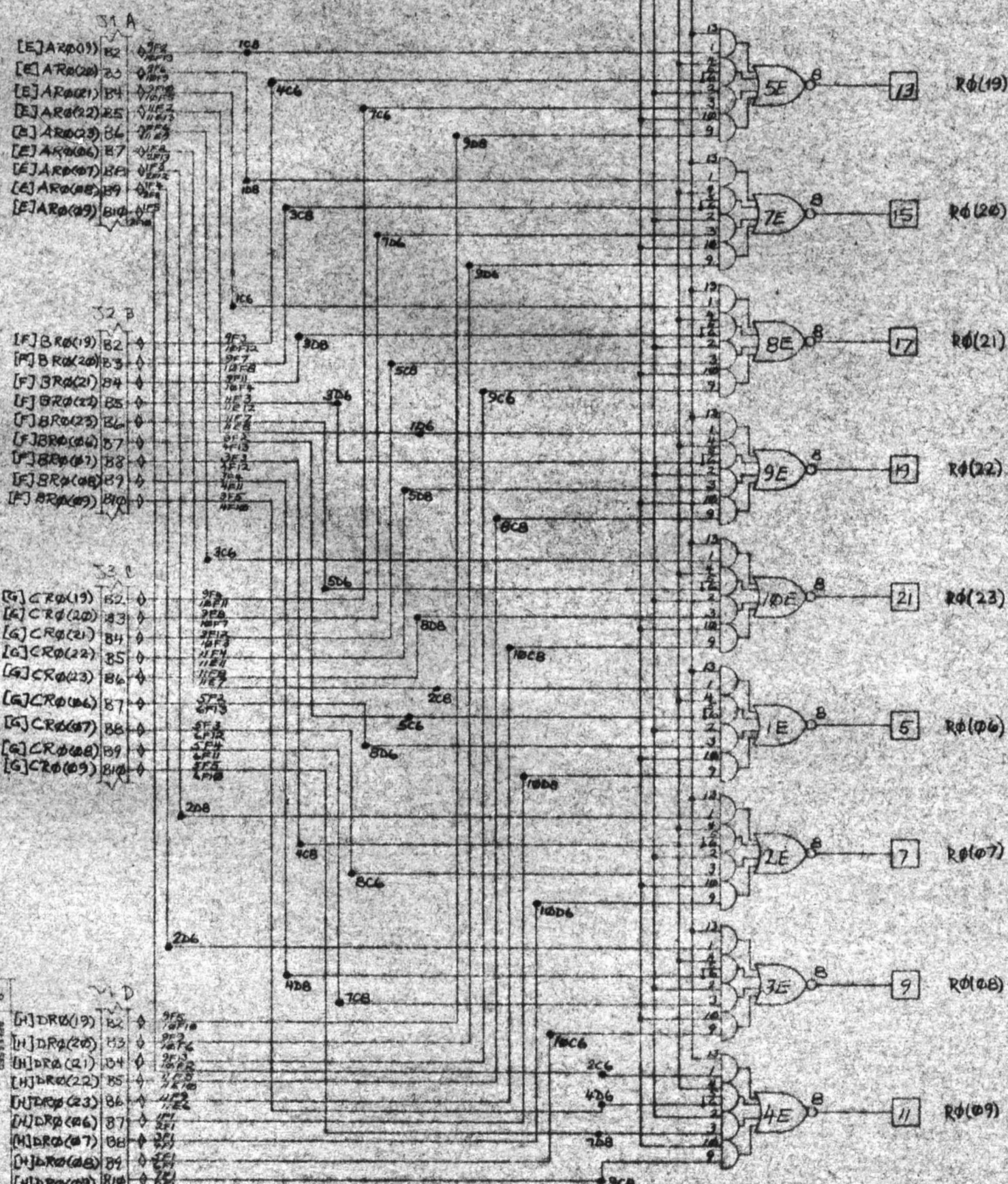
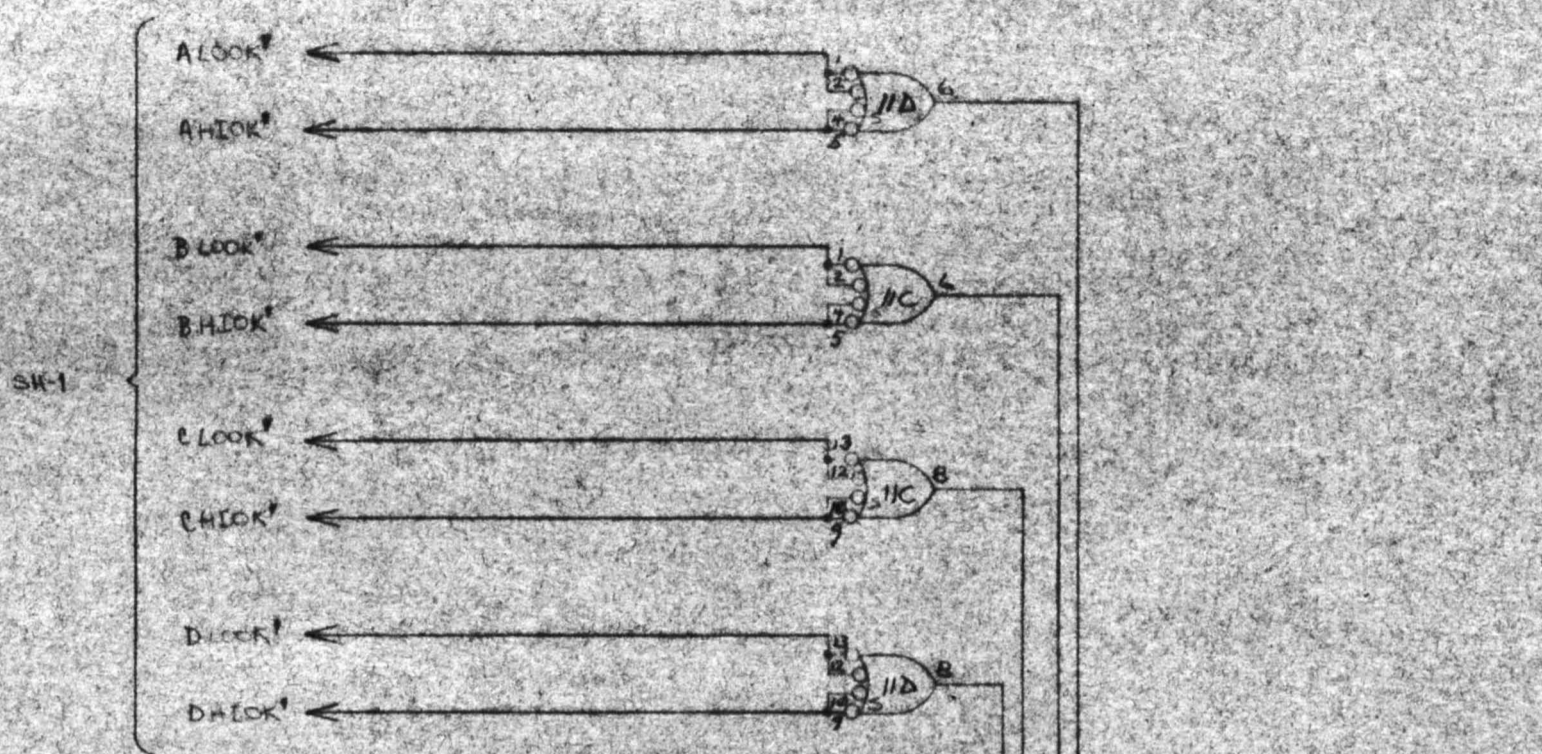
Normally hi - except when gate on & incoming address bit is '0'.



mixes signals from processor onto backpanel

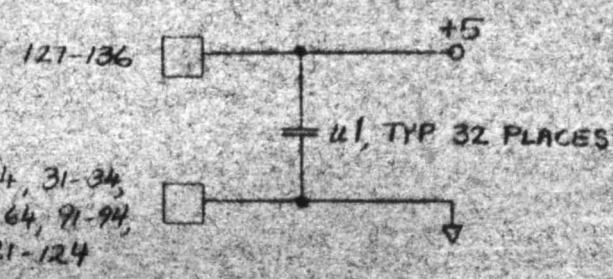
Etch, this page

RELEASED  
 ADDRESS (BITS 06-23)  
 NEW MPMM AB J A7  
 1  
 2  
 LP 1055.D  
 [E-H]  
 A-D  
 No 7



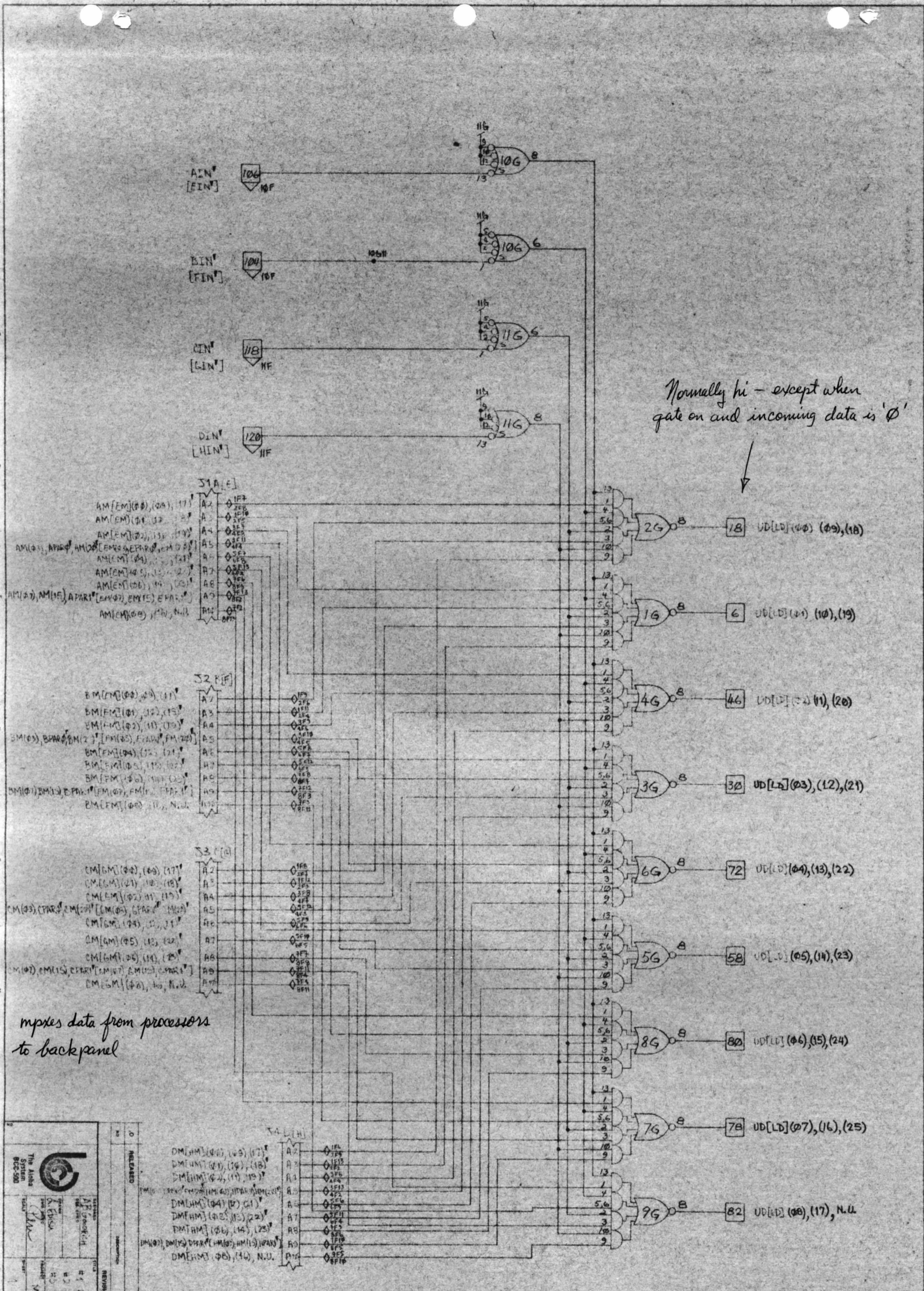
*Wires addresses from processor to backpanel*

Handwired, this page



A67

ADDRESS	REVISED
(BTS 4-1-23)	
M/PM/BM	
A6 X A7	
2	
2	
141053.0	

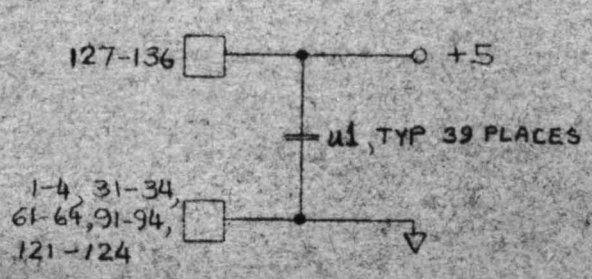


Normally hi - except when gate on and incoming data is '0'

mpxes data from processors to backpanel

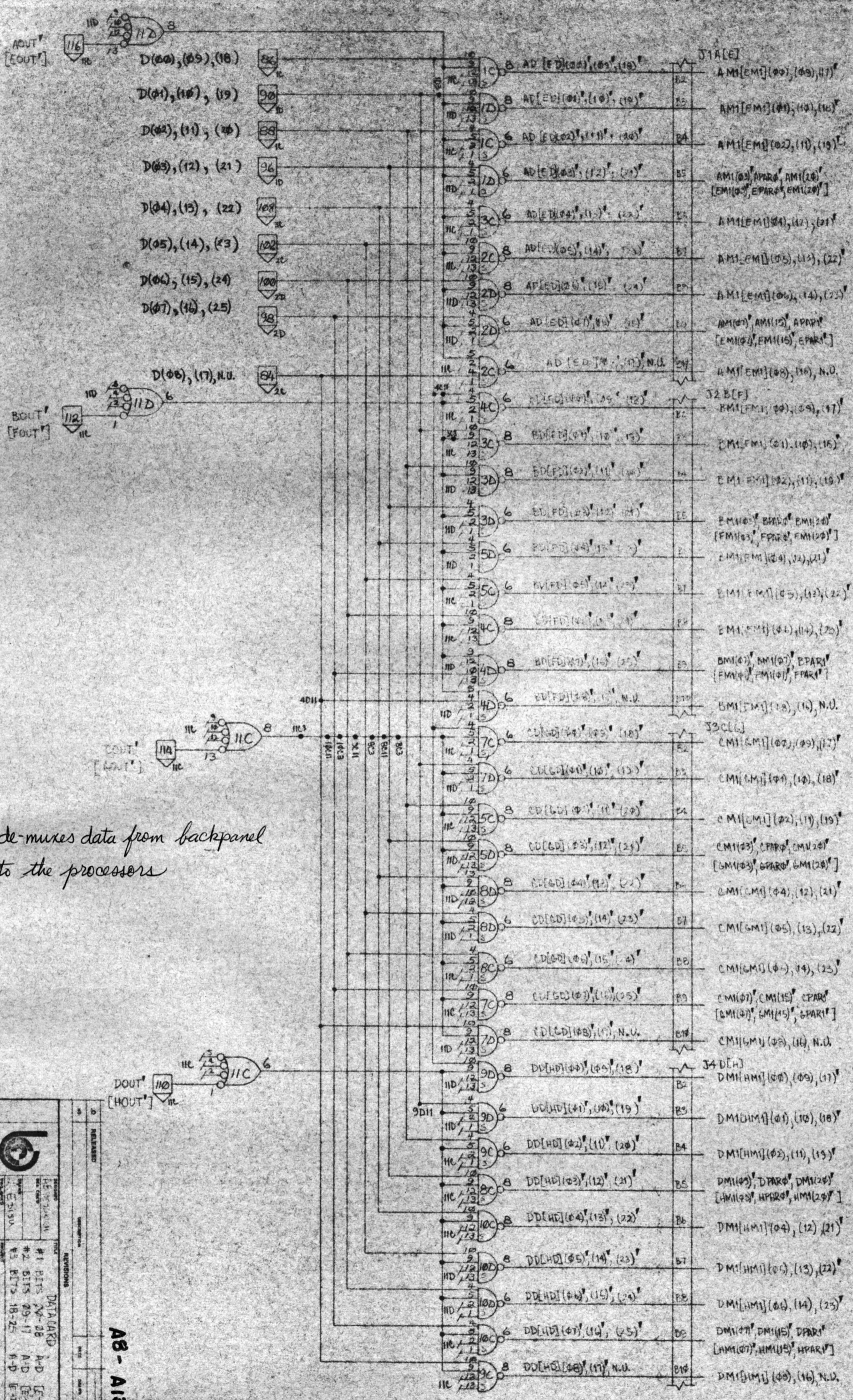
REVISED	DATE
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AB-A13



Note: BECKMAN 899-1-R200

#1 Pos. A8, A9  
 #2 Pos. A10, A11  
 #3 Pos. A12, A13



*de-muxes data from backpanel to the processors*

RELEASED DATE: 10/1/52 BY: MPPBM	REVISIONS #1 BITS 20-08 #2 BITS 20-17 #3 BITS 18-25 MPPBM MASTER 101052-0

**AB- A13**