

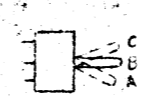
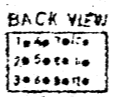
GND 103, 101, 99, 77, 67, 45, 43, 61, 57, 55, 53, 51, 49, 47, 45, 43, 41, 39, 37, 35, 33, 31, 29, 27, 25, 23, 21, 19, 17, 15, 13, 11, 9, 7, 5, 3, 1, 0

-5 83, 84, 85, 86 +5

GND 127-136

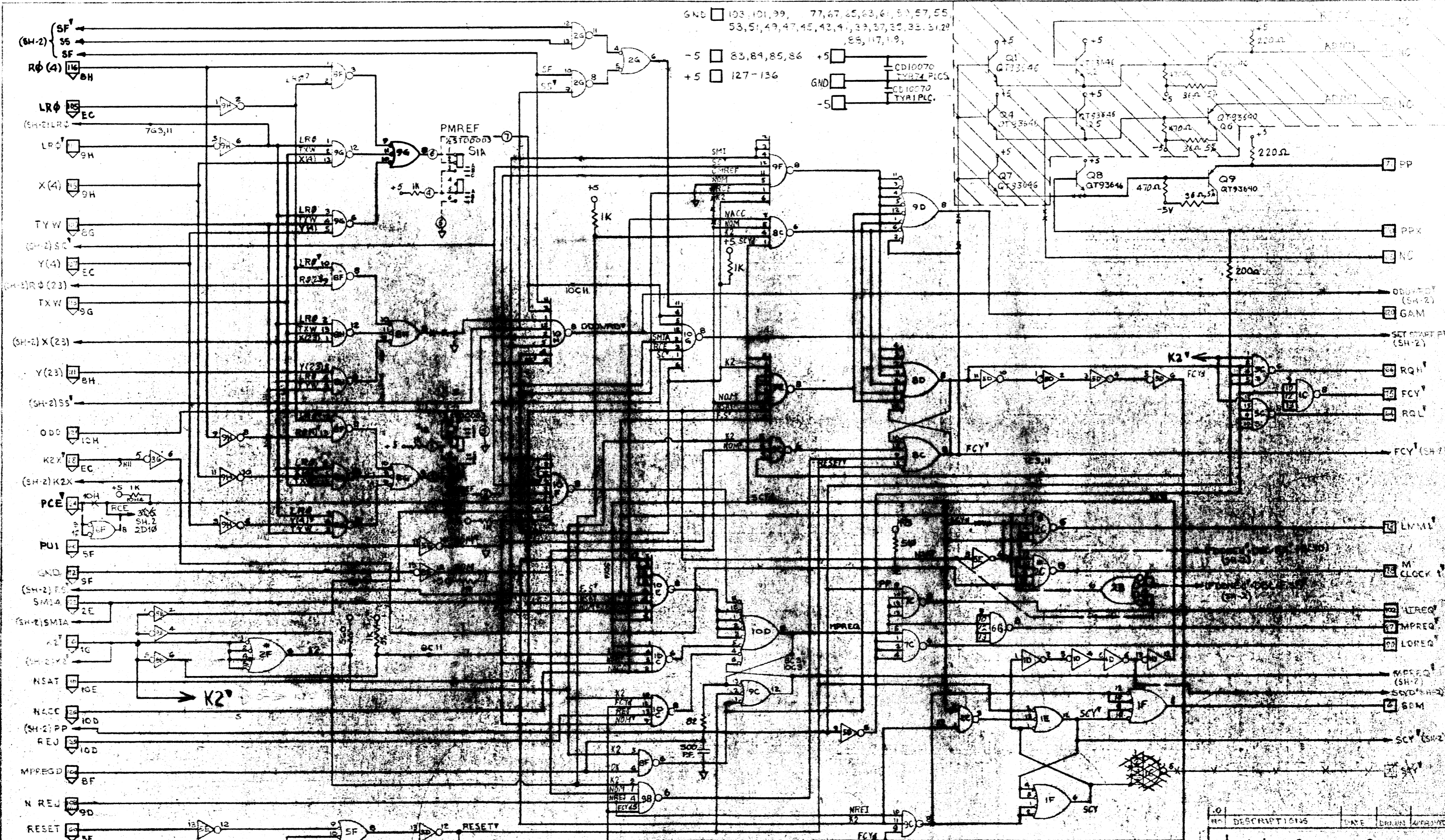
0B10070  
1YB74 P.C.S.  
0C10070  
1YA1 P.C.

NOTES UNLESS OTHERWISE SPECIFIED  
RESISTORS ARE 10% 1/8W CARB. COMP  
J-JUMPER AS REQUIRED  
\*\*CUT PC CONDUCTOR  
\* FAST IC'S MODULES

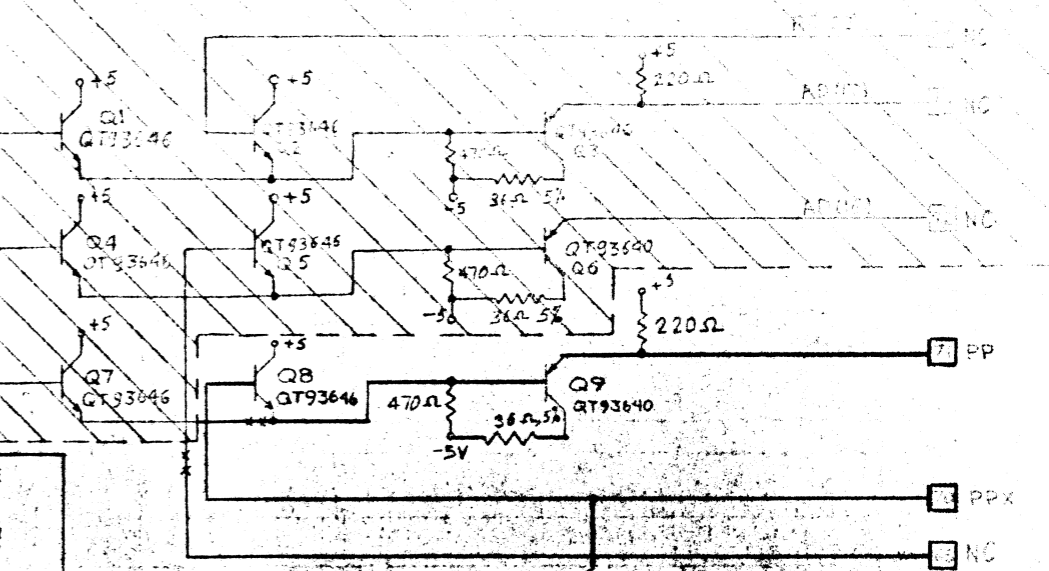


ST0005  
SIA#B: FUNCTION OF SWITCH POSITIONS  
A. ALL REFERENCES TO PRIVATE MEMORY  
B. ALL REFERENCES AS SPECIFIED BY THE MICROCODE  
C. ALL REFERENCES TO CENTRAL MEMORY.

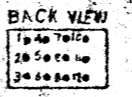
Berkeley Computer Corporation			
DATE	DESIGNED BY	APPROVED BY	REVISED BY
MEMORY INTERFACE			M4
CPU-1			LC024



GND □ 103, 101, 99, 77, 67, 65, 63, 61, 59, 57, 55, 53, 51, 49, 47, 45, 43, 41, 39, 37, 35, 33, 31, 29, 27, 25, 23, 21, 19,  
 -5 □ 83, 84, 85, 86 +5 □  
 +5 □ 127-136

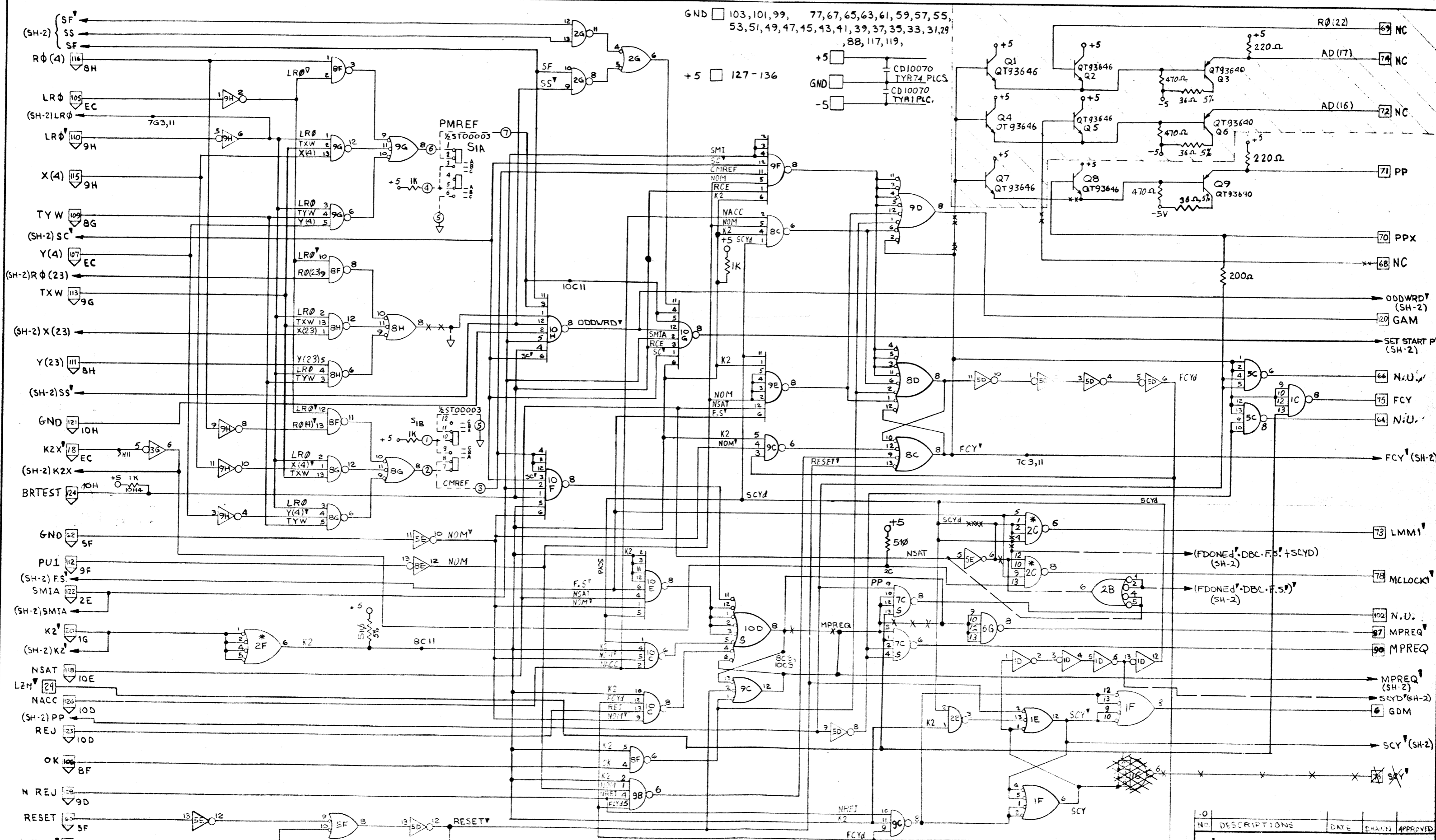


**NOTES** UNLESS OTHERWISE SPECIFIED  
 RESISTORS ARE 10%, 1/8W, CARB. COMP  
 J—JUMPER AS REQUIRED  
 \*\* CUT PC CONDUCTOR  
 \* FAST IC'S MODULES



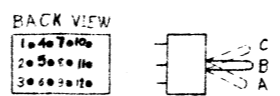
**ST00003**  
 SIA#18: FUNCTION OF SWITCH POSITIONS  
 A. ALL REFERENCES TO PRIVATE MEMORY  
 B. ALL REFERENCES AS SPECIFIED BY THE MICROCODE  
 C. ALL REFERENCES TO CENTRAL MEMORY

NO.	DESCRIPTIONS	DATE	DESIGNER	APPROVED
Berkeley Computer Corporation				
1	MEMORY INTERFACE			
2	CPU-1			



GND □ 103, 101, 99, 77, 67, 65, 63, 61, 59, 57, 55, 53, 51, 49, 47, 45, 43, 41, 39, 37, 35, 33, 31, 29, 88, 117, 119,  
 +5 □ 127-136

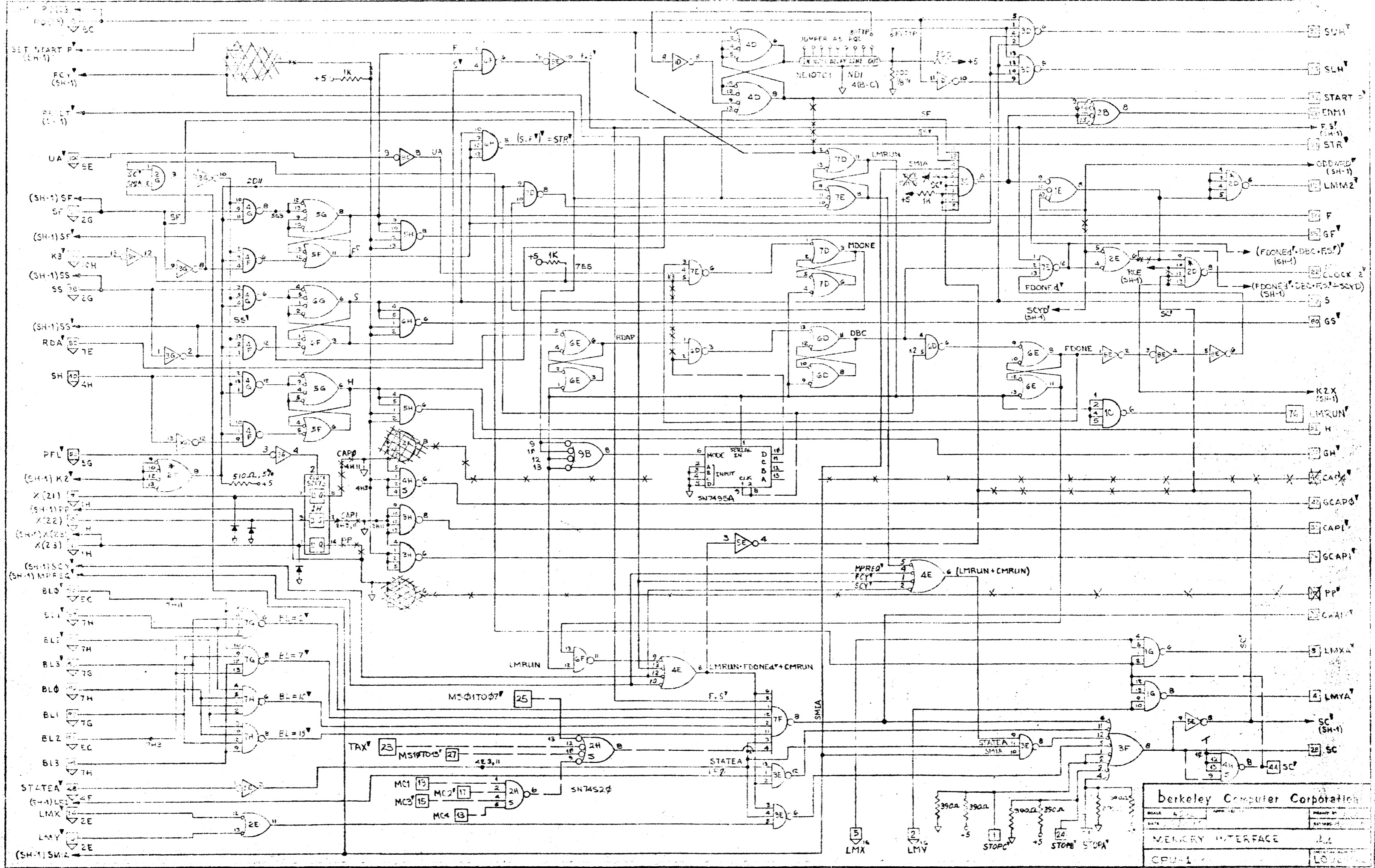
NOTES UNLESS OTHERWISE SPECIFIED  
 RESISTORS ARE 10%, 1/8W. CARB. COMP  
 J—JUMPER AS REQUIRED  
 \*\*CUT PC CONDUCTOR  
 \* FAST IC'S MODULES



ST00003  
 SIA:IB: FUNCTION OF SWITCH POSITIONS  
 B. ALL REFERENCES TO PRIVATE MEMORY  
 A. ALL REFERENCES AS SPECIFIED BY THE MICROCODE  
 C. ALL REFERENCES TO CENTRAL MEMORY.

A4

NO.	DESCRIPTIONS	DATE	DRAWN	APPROVED
Berkeley Computer Corporation				
SCALE: NONE	APPROVED BY:	DATE: 23 JULY 69	DRAWN BY: M.H.	REVISED: 8-15-69
MEMORY INTERFACE			A4	
MASTER			DRAWING NUMBER L00240.2	



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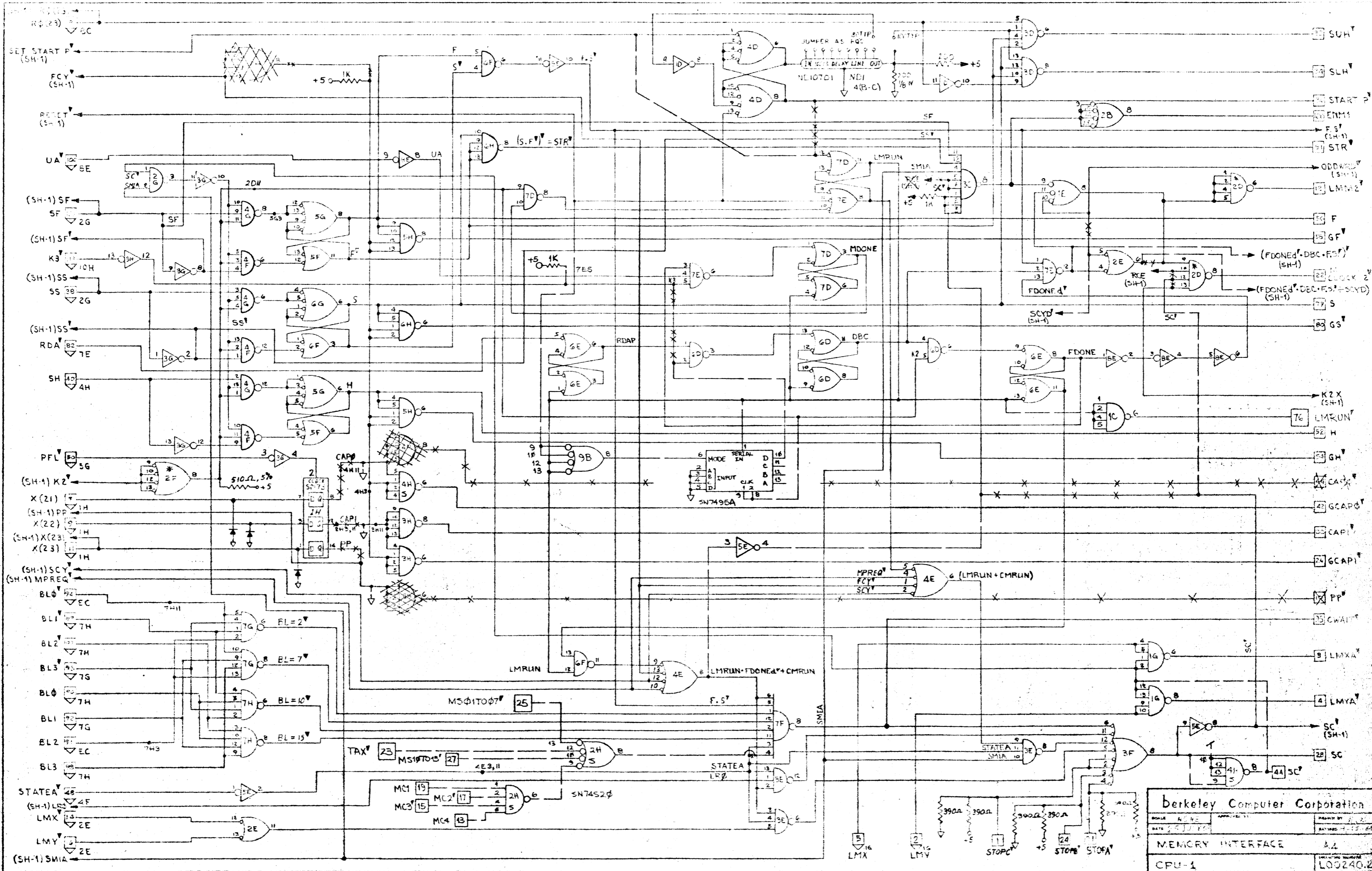
SCALE: 4:1

DATE: \_\_\_\_\_

MEMORY INTERFACE

CPU-1

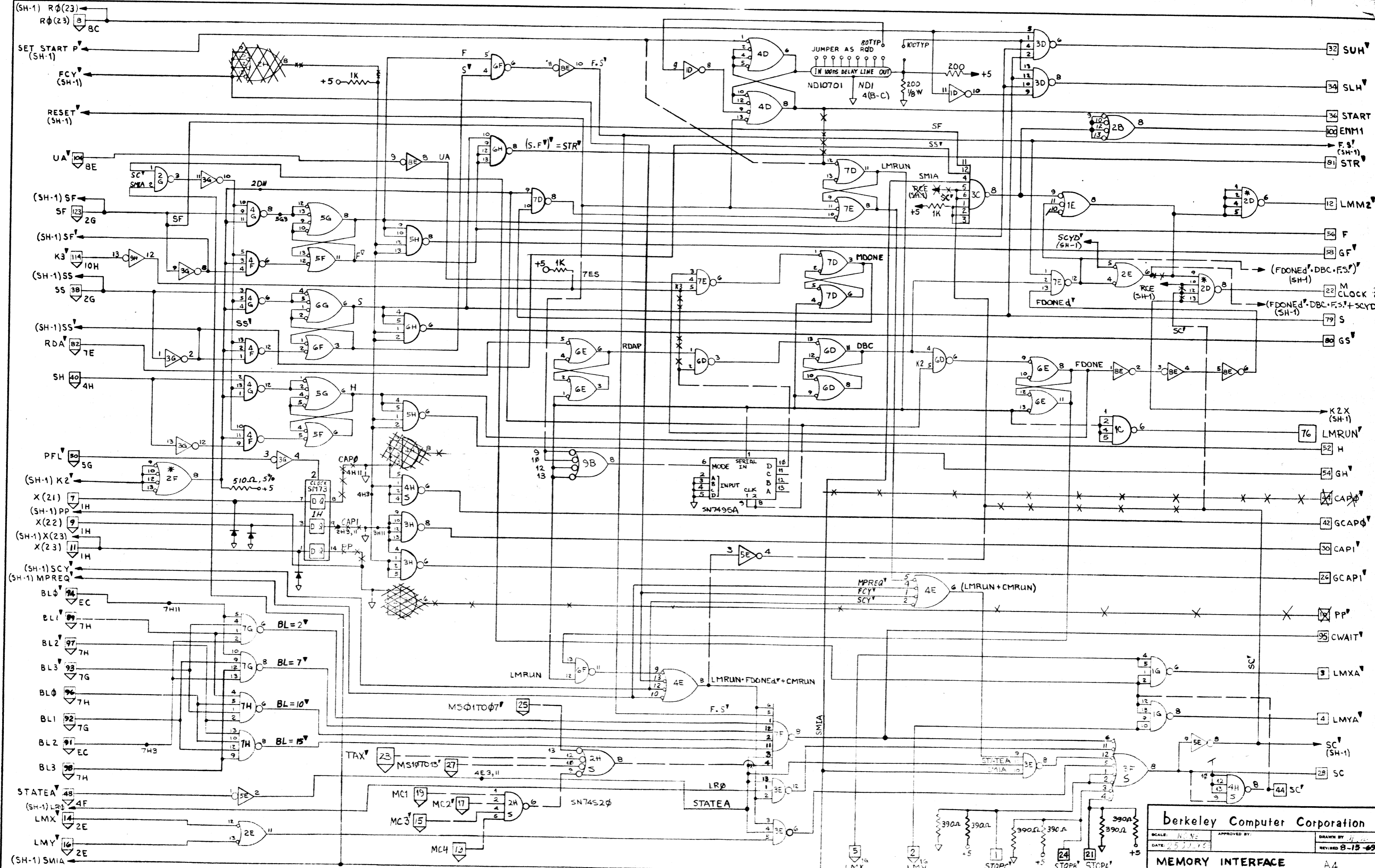
SH 2 QF 2



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SCALE: AS SHOWN	APPROVED BY:	DESIGNED BY: J. Z.
DATE: 5/5/74	REVISION: 1-13-74	
MEMORY INTERFACE		3.2
CPU-1		LOG240.2

SH 2 OF 2



**berkeley Computer Corporation**

SCALE: NONE	APPROVED BY:	DRAWN BY: J. J. ...
DATE: 2-5-75	REVISED: 8-15-69	REVISED: 8-15-69
<b>MEMORY INTERFACE</b>		A4
<b>MASTER</b>		DRAWING NUMBER L00240.2

SH 2 OF 2