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Model 980B Computer Maintenance Manual

Memory, Memory Controller And Direct Memory Access Channel (DMAC)

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2-1 - 2-4	0				
Alphabetical Index Div	0				
Index-1 - Index -6	0				
User's Resp	0				
Bus. Reply	0				
Cover Blank	0				
Cover	0				

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

INTRODUCTION

This manual describes the memory system and the Direct Memory Access Channel (DMAC) for the Texas Instruments Model 980B Computer. Section I provides a detailed discussion of the memory controller and memory circuit boards, and includes block diagrams, interface signal definitions, and detailed theory of operation. Section II discusses the DMAC interface. Detailed electrical schematic diagrams for the circuit boards are contained in Model 980B Maintenance Manual Electrical Drawings, TI Part Number 943012-9704. Parts lists for the assemblies are contained in Model 980B Maintenance Manual Parts Lists and Assembly Drawings, TI Part Number 943012-9703. This manual is part of a complete set of manuals that supplies information for maintaining and repairing the computer. The manual set is specifically defined in Model 980B Maintenance Manual System Description, TI Part Number 943012-9701.

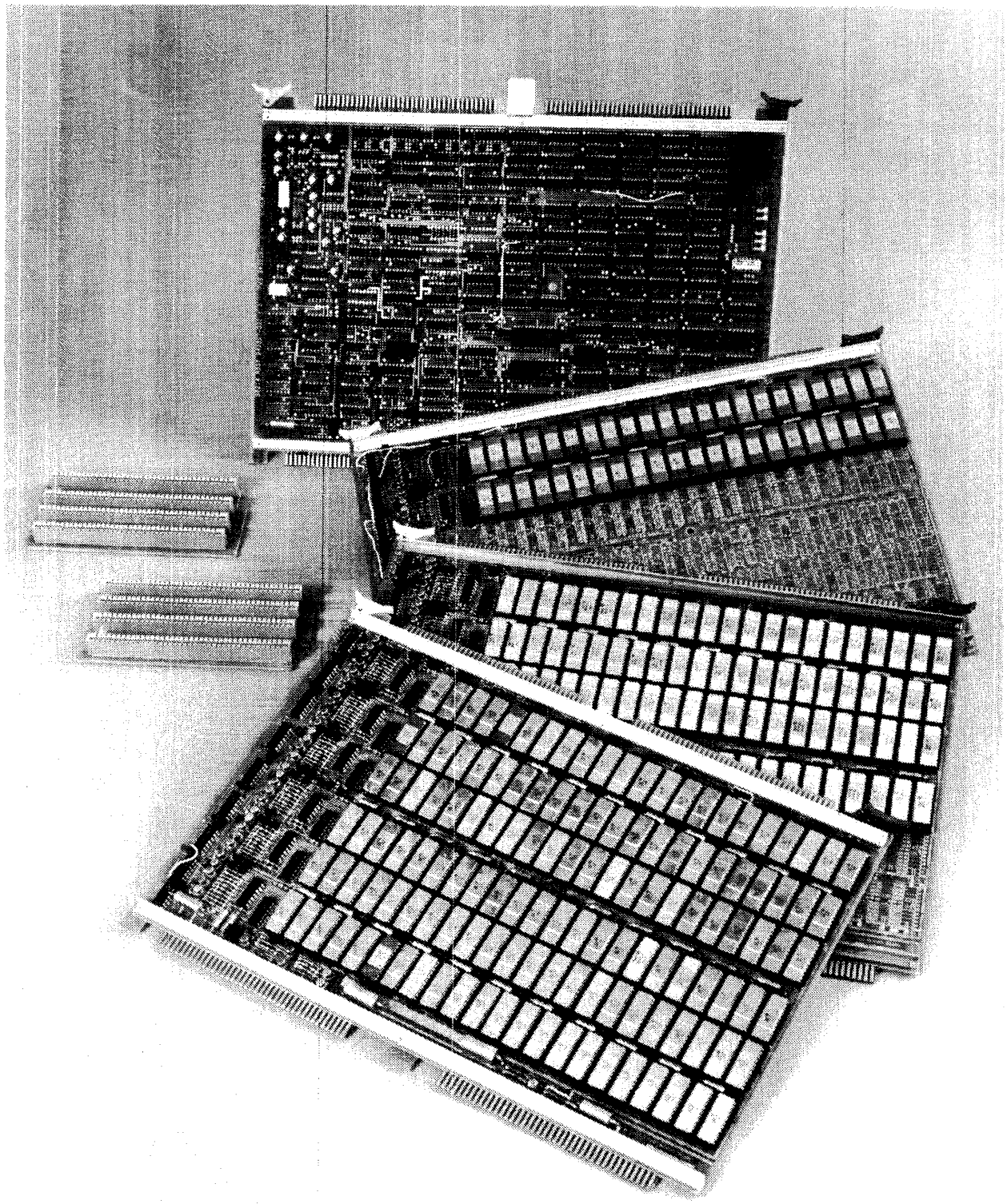

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Figure 1-1. Model 980B Computer Memory System

SECTION I

MEMORY SYSTEM

1.1 INTRODUCTION

The memory system for the Texas Instruments Model 980B Computer consists of a single memory controller circuit board, one, two, or three memory circuit boards, and the interconnecting boards to interface the memory controller to the memory boards as illustrated in figure 1-1. The standard memory configuration offers 8,192 words (8K) of memory and includes one memory circuit board. Optional configurations offer additional memory capacity in increments of 8K words to a maximum capacity of 65,536 words that employs three memory circuit boards. The following paragraphs provide an overview description of the memory system capabilities. The remainder of this section of the manual describes the theory of operation for the memory controller and the memory, and defines the interface between them and the interface between the controller and the requesting interface.

1.1.1 MEMORY FEATURES

The memory system receives data and addresses from either the Central Processing Unit (CPU) or the Direct Memory Access Channel (DMAC) of the computer and performs all data transfer and control operations required to store, retrieve and maintain data within the memory. In addition, the memory system provides the following features:

- A Privileged Instruction Feature (PIF) that, when enabled, prevents execution of certain specified instructions.
- A protected memory area whose size is program controlled.
- A temperature-dependent circuit to maintain data in memory when main power is off.
- Error detecting/correcting logic that corrects single-bit errors and detects double-bit errors that occur during a memory read.
- Error indicators that pinpoint the exact memory integrated circuit that caused a correctable memory error.

1.1.2 PHYSICAL DESCRIPTION

Memory control circuitry is TTL family integrated circuit packages and discrete component circuits. Memory storage is performed by a high-density Metal Oxide Semiconductor (MOS) integrated circuit package that provides random access for read or write operations on 4096 individually addressable bits. Each memory package is a 22-pin dual-inline-package (DIP) that is socket-mounted on the memory circuit board for easy replacement in the event of a circuit failure.

1.1.2.1 CIRCUIT BOARDS. The printed wiring boards for the memory system are 14-1/4 inches wide and 10-1/4 inches high. Two connectors, P1 and P2, are formed along the bottom edge of the board by printed conductor contacts. The contacts are numbered from 1 through 80 with the even numbered contacts on the component side of the circuit board. An additional tab, slightly offset from center along the bottom edge of the board, prevents the circuit board from being inserted into the chassis connectors when the board is backward. As an additional reminder, one of the ejector tabs on the top of edge of the card is colored and the other tab is white. The colored tab should always be toward the right (as viewed from front of computer) of the chassis. Two additional connectors, P3 and P4, are formed along the top edge of each circuit board. These connectors are identical to P1 and P2 and provide the interface connection between the memory controller and the memory circuit boards.

1.1.2.2 LOCATION. Figure 1-2 illustrates the placement of the circuit boards within the computer chassis. If only one memory board is used, it must be inserted into the location designated for Memory Board 1 (M1). Similarly, two memory boards must occupy locations designated for Memory Board 1 and Memory Board 2 (M1 and M2). Each memory board may contain either 8K, 16K or 24K words of memory. However, if three memory boards are used and each board contains 24K words, only 65K words of memory will be recognized and usable by the controller.

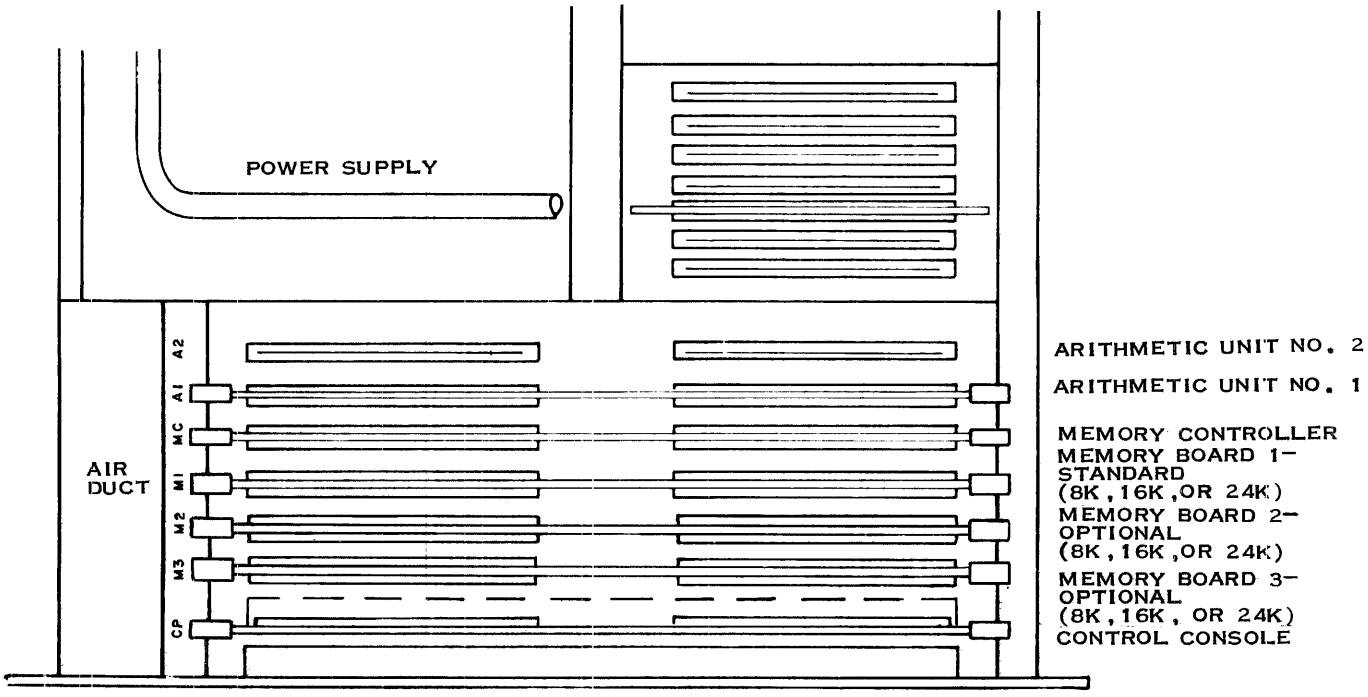

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Figure 1-2. Memory System Chassis Locations

1.2 MEMORY CONTROLLER CIRCUIT BOARD

The memory controller circuit board selects data and controls data transfer between the computer memory circuit boards and either the Central Processing Unit (CPU) or the Direct Memory Access Channel (DMAC). In addition, the memory controller supplies a Privileged Instruction Feature (PIF), a system clock circuit to coordinate the activities of the controller, memory, and CPU, plus a refresh system to maintain data in the dynamic memory during standby (power loss) operation as well as full power operation. The following paragraphs define the interfaces between the memory controller and the other system components, and describe the operation of the controller circuits for coordination of memory activities.

1.2.1 MEMORY CONTROLLER EXTERNAL INTERFACE

The memory controller provides the interface for the memory system with all computer components external to the memory system. Both the computer arithmetic unit and the Direct Memory Access Channel can request memory operations. In addition, the computer power supply and control panel both supply control signals that modify or regulate the operation of the memory system. Table 1-1 defines each signal and its function. Figure 1-3 illustrates these external interface signals.

Table 1-1. Memory Controller External Interface Signals

Signature	Pin No.	Definition
SYSCLK-	P2-23	A system clock signal from the memory controller to the AU. This signal is gated on the AU and supplied I/O interfaces as a system clock. The signal is a 4-MHz, one one-third duty cycle clock. I/O clock from the AU is IOCLK-.
GCLK-	P2-24	This is a gated system clock supplied to the AU.
MEM00	P1-52	Memory Read Data from the memory controller to the DMAC or the AU interface. Read data from main memory is held on these lines by buffer latches until the next memory read cycle is nearly complete.
MEM01	P1-51	
MEM02	P1-33	
MEM03	P1-30	
MEM04	P1-36	
MEM05	P1-35	
MEM06	P1-23	
MEM07	P1-24	
MEM08	P1-34	
MEM09	P1-32	
MEM10	P1-31	

Table 1-1. Memory Controller External Interface Signals (Continued)

Signature	Pin No.	Definition
MEM11 MEM12 MEM13 MEM14 MEM15	P1-28 P1-50 P1-48 P1-47 P1-42	
DMFCH-	P2-28	DMAC Fetch - A single line from the DMAC interface that instructs the memory controller to initiate a memory read cycle.
DMSTR-	P2-27	DMAC Store - This line from the DMAC interface instructs the memory controller to initiate a memory write cycle.
DMAACR-	P2-67	DMAC Access Request - This line from the DMAC interface indicates to the memory controller that the DMAC interface requires access to memory.
DMACCB	P2-31	DMAC Access Granted - indicates to the DMAC interface that the memory controller has given access to the DMAC in response to a DMAACR- signal.
RFACCB-	P2-24	Refresh Access Granted - indicates to the DMAC interface that a refresh cycle is in progress; DMAC gates off the system clock during refresh cycles in response to this signal.
WDPB	P2-61	Write Data Parity Bit - a parity bit generated by the memory controller from data being written into memory from the DMAC interface. When low, this line indicates to the DMAC interface that the data contains an odd number of "1" data bits.
RDPB	P1-65	Memory Read Data Parity Bit - a parity bit generated by the memory controller from data being read from memory. When low, this line indicates to the DMAC interface that the data contains an odd number of "1" data bits.

Table 1-1. Memory Controller External Interface Signals (Continued)

Signature	Pin No.	Definition
DWD00	P2-16	DMAC Write Data - 16 input data lines from the DMAC interface that supply data to be stored into memory during a DMAC Store operation.
DWD01	P2-18	
DWD02	P2-19	
DWD03	P2-20	
DWD04	P2-17	
DWD05	P2-21	
DWD06	P2-22	
DWD07	P2-25	
DWD08	P2-29	
DWD09	P2-30	
DWD10	P2-33	
DWD11	P2-37	
DWD12	P2-47	
DWD13	P2-48	
DWD14	P2-50	
DWD15	P2-52	
DA00	P1-20	DMAC Memory Address - 16 input lines from the DMAC interface that specify to the memory controller the location in memory that will be accessed during a DMAC memory operation (store or fetch).
DA01	P1-19	
DA02	P1-18	
DA03	P1-16	
DA04	P2-53	
DA05	P2-54	
DA06	P2-46	
DA07	P2-49	
DA08	P2-41	
DA09	P2-45	
DA10	P2-10	
DA11	P2-69	
DA12	P2-65	
DA13	P2-62	
DA14	P2-59	
DA15	P2-58	
MERR	P1-49	Memory Error - This signal from the memory controller indicates to the AU that an uncorrectable error has occurred in data read from memory and that the data on the MRDxx data bus is incorrect.
ST4G	P1-62	Status Bit 4 - When high, this signal enables the Privileged Instruction Feature decoding circuit and memory protect inspection.

Table 1-1. Memory Controller External Interface Signals (Continued)

Signature	Pin No.	Definition
ST9G	P1-29	Status Bit 9 - When high, this signal instructs the memory controller to add a bias address to the address on the ALUB lines before using the address for a memory access. The bias address value is the lower limit of the usable memory when memory protect is used (ST4G).
GOIO-	P1-38	This signal, when low, indicates that the first word of a WDS instruction (to load the memory protect limit registers) is stable on the ALUB data lines.
TERMIO-	P1-37	When low, this signal indicates that the second word of a WDS instruction is stable on the ALUB data lines.
INAQ-	P1-69	When low, this signal indicates that the current memory operation is fetching an instruction for the AU.
CPUCR-	P2-52	CPU Cycle Request - When low, this signal from the AU initiates a memory cycle if CPU has access.
CPUSTR	P2-55	CPU Store- This signal indicates to the memory controller whether a memory cycle requested by the AU should be a read or a write cycle (High = Write; Low = Read).
ENMALOAD-	P1-21	Address Load Enable - This signal from the AU indicates to the memory controller that the data on the ALUBxx bus is an address rather than data. The controller then loads the data into its address register after passing it through the address bias circuit.
ENMAINC-	P2-66	Address Increment - This signal from the AU increments the address currently contained in the memory controller address register to allow sequential access to contiguous memory locations.

Table 1-1. Memory Controller External Interface Signals (Continued)

Signature	Pin No.	Definition
ALUB00 ALUB01 ALUB02 ALUB03 ALUB04 ALUB05 ALUB06 ALUB07 ALUB08 ALUB09 ALUB10 ALUB11 ALUB12 ALUB13 ALUB14 ALUB15	P1-59 P1-60 P1-63 P1-67 P1-66 P1-64 P1-54 P1-57 P1-61 P1-58 P1-56 P1-55 P1-41 P1-43 P1-44 P1-45	Write Data and Address - These 16 lines from the AU supply either data to be written into a specified memory location, or an address to specify a memory location for either a fetch or store operation. The use of this bus is defined by the state of the ENMALOAD interface signal.
CPUCC-	P1-25	Cycle Complete - This signal from the memory controller indicates to the AU that the current memory operation (read or write to memory) is complete.
INSTV-	P1-76	A low active signal that indicates to the AU that the current instruction being sent from memory to the AU is an illegal instruction; this signal is generated only if PIF is activated by ST4G.
ADRV-	P1-53	Memory Protect Address Violation - This signal from the memory controller indicates to the AU that the last store operation attempted to write into an area in protected memory and was, therefore, not honored. This signal is generated only if PIF is activated by ST4G.
STPCK-	P2-26	Stop Clock - When low, this signal from the AU indicates that the operator CLOCK/STEP switch is in the OFF (center) position or that the AU is waiting for CPUCC after requesting a memory cycle. This signal disables generation of the GCLK in the memory controller.

Table 1-1. Memory Controller External Interface Signals (Continued)

Signature	Pin No.	Definition
STEPULS-	P1-46	System Clock Step - This signal from the operator panel CLOCK/STEP switch indicates that the switch has been moved to the STEP (momentary down) position. This signal enables the memory controller error display latch (unlocks LATCH).
MRESET-	P2-15	Master Reset - This signal from the computer power supply indicates that AC power has been interrupted. The signal initializes the memory controller during power application, and inhibits the start of a new memory cycle if a power failure or power removal is imminent.
POFF-	P2-42	Power Failing - This signal indicates to the memory controller that interruption of power to the computer is imminent. The controller then prevents memory access from the DMAC interface so that the CPU may execute its power down routine before main power is removed.
+5 STBY	P1-7, 8 P2-73, 74	Standby Power - +5 Vdc that remains on to power the memory controller circuits during refresh bursts when main power has failed and the memory is being maintained by the battery.
+5 MAIN	P1-3, 4, 77, 78 P2-3, 4, 77, 78	Main Power - +5 Vdc to power the memory controller circuits during normal operation when ac power is present in the power supply.
GND	P1-1, 2, 39, 40 79, 80 P2-1, 2, 39, 40 79, 80	Ground

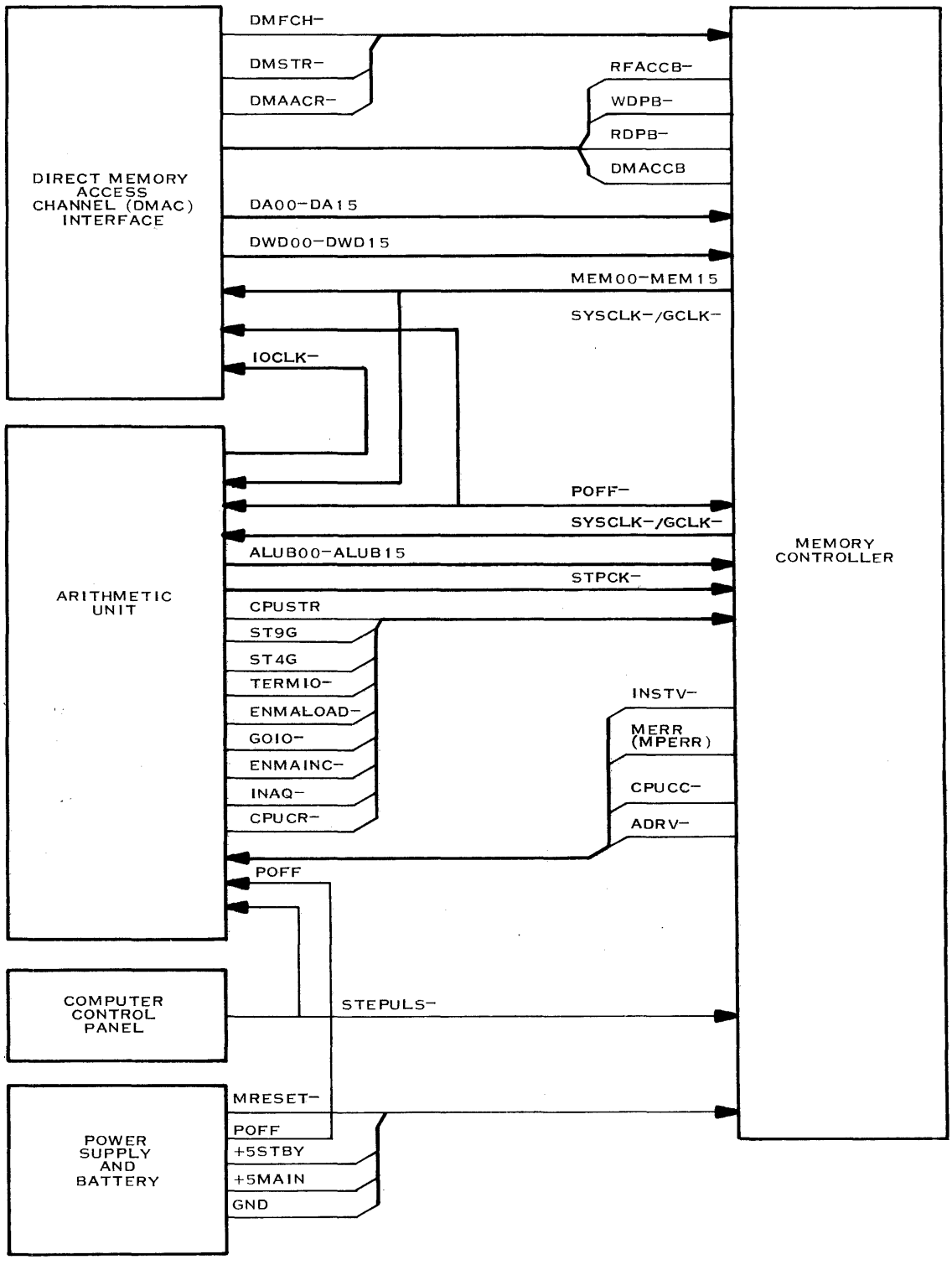


Figure 1-3. Memory Controller External Interface and Power Connections

1.2.2 MEMORY CONTROLLER TO MEMORY INTERFACE

The memory controller generates a set of control signals to initiate data transfer between the memory controller and the memory circuit boards. The interface may be implemented with one, two or three memory circuit boards. The interface signals are carried through the top edge connectors of the memory controller and the memory circuit boards. Special interconnect boards complete the connection between the memory controller and one, two or three memory boards. For the three different configurations, the interconnect board part numbers are as follows:

	Right (P3)	Left (P4)
One Memory Circuit Board -	943718	943718
Two Memory Circuit Boards* -	943706	943705
Three Memory Circuit Boards** -	943716	943714

Figure 1-4 illustrates the interface signals between the controller and the memory boards. Table 1-2 lists these signals and defines their function.

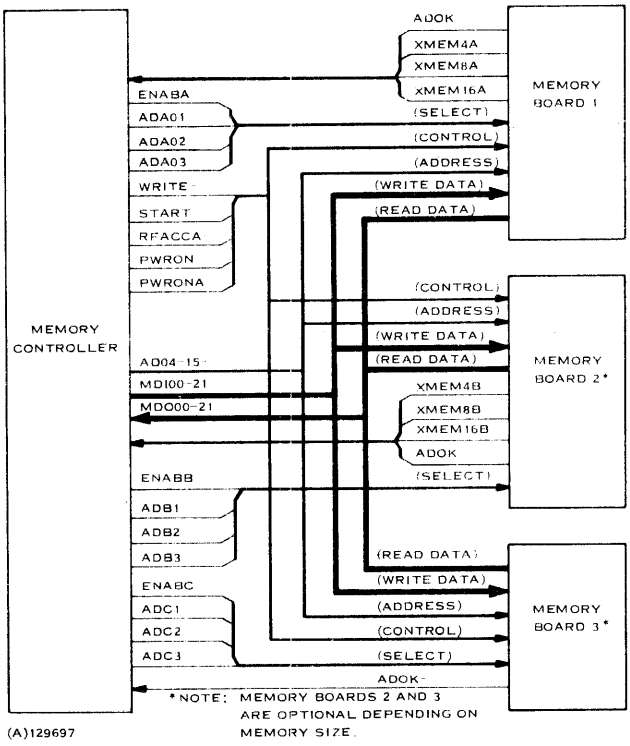


Figure 1-4. Memory Controller-to-Memory Interface

* Can be used for 1 or 2 memory boards.
**Can be used for 1, 2, or 3 memory boards.

Table 1-2. Memory Controller to Memory Interface Signals

Signature	Pin No.	Definition
MDO00	P4-51	Memory read data output from memory to memory controller.
MDO01	43	
MDO02	35	
MDO03	27	
MDO04	19	
MDO05	13	
MDO06	09	
MDO07	05	
MDO08	P4-04	
MDO09	P3-75	
MDO10	71	
MDO11	63	
MDO12	55	
MDO13	47	
MDO14	39	
MDO15	P3-31	
MDO16	P3-23	Error check bits from memory during a read operation.
MDO17	17	
MDO18	13	
MDO19	09	
MDO20	05	
MDO21	P3-04	
MDI00-	P4-53	Memory write data input from memory controller to memory.
MDI01-	45	
MDI02-	37	
MDI03-	29	
MDI04-	21	
MDI05-	15	
MDI06-	11	
MDI07-	07	
MDI08-	P4-03	
MDI09-	P3-77	
MDI10-	73	
MDI11-	65	
MDI12-	57	
MDI13-	49	
MDI14-	41	
MDI15-	P3-33	

Table 1-2. Memory Controller to Memory Interface Signals (Continued)

Signature	Pin No.	Definition
MDI16- MDI17- MDI18- MDI19- MDI20- MDI21-	P3-25 19 15 11 07 P3-03	Error check bits to memory during a write operation.
AD04- AD05- AD06- AD07- AD08- AD09- AD10- AD11- AD12- AD13- AD14- AD15-	P4-73 69 77 75 67 61 71 63 65 59 55 P4-57	Least significant 12 bits of address from CPU or DMAC used as a store or fetch address when accessing a memory location. The most significant six bits of this address (AD04-AD09) can also be generated internal to the controller for use during refresh cycles.
ADOK-	P4-39	A low active signal indicating that the memory board has accepted an address as valid.
ENABA	P4-72	Memory Board Select to enable bank decoder on board 1.
ENABB	P4-54	Memory Board Select to enable bank decoder on board 2.
ENABC	P4-58	Memory Board Select to enable bank decoder on board 3.
ADA01 ADA02 ADA03	P4-74 P4-76 P4-78	A 3-bit code sent to memory board 1 to indicate which bank (0-5) of memory chips is to be cycled. ADA03 is the least significant bit of the code.
ADB1 ADB2 ADB3	P4-62 P4-60 P4-52	A 3-bit code sent to memory board 2 to indicate which bank (0-5) of memory chips is to be cycled. ADB3 is the least significant bit of the code.

Table 1-2. Memory Controller to Memory Interface Signals (Continued)

Signature	Pin No.	Definition
ADC1 ADC2 ADC3	P4-48 P4-50 P4-56	A 3-bit code sent to memory board 3 to indicate which bank (0-5) of memory chips is to be cycled. ADC3 is the least significant bit of the code.
XMEM4A- XMEM8A- XMEM16A-	P3-27 P3-29 P3-21	A 3-bit complement code from memory board 1 that designates to the memory controller the size of the memory contained on the memory board. Valid codes are: 16- 8- 4- 1 0 1 8K memory 0 1 1 16K memory 0 0 1 24K memory
XMEM4B- XMEM8B- XMEM16B-	P3-28 P3-30 P3-22	A 3-bit complement code from memory board 2 that designates to the memory controller the size of the memory contained on the memory board. Valid codes are the same as for XMEM__A-. No memory size code is required from memory board 3.
WRITE-	P4-64	When a logic one, this signal indicates that a read cycle is to be performed from the addressed memory location. When this line is a logic zero, the memory performs a write operation.
START	P4-70	This signal initiates a memory cycle in the addressed memory board. A discrete clock driver on the memory board changes the signal level to +12 Vdc (active) and 0 Vdc (inactive) to drive the clock input of the MOS memory chips.
RFACCA-	P4-68	When coincident with START, this signal initiates a refresh cycle in all of the memory chips. The refresh address is determined by the address lines from the memory controller.

Table 1-2. Memory Controller to Memory Interface Signals (Continued)

Signature	Pin No.	Definition
PWRON	P3-37	This signal to the memory boards turns on +5 Vdc (switched) to the logic elements. When computer main power drops, this signal drops, disabling power to the logic elements except during refresh bursts.
PWRONA	P4-66	This signal lags PWRON and leads PWRON- and disables memory clock when +5 Vdc (switched) is not stable. During normal power conditions, this signal is a logic one.
GND	P3-1, 2, 35, 36, 45, 46, 79, 80 P4-1, 2, 17, 18, 41, 42, 79, 80	Signal Ground

1.2.3 MEMORY CONTROLLER TEST INTERFACE

The memory controller circuit board also provides for test monitoring and control of the circuits for checkout and maintenance purposes. Table 1-3 defines the function of each of these checkout signals.

Table 1-3. Memory Controller Test Interface Signals

Signature	Pin No.	Definition
CARRYA	P1-17	Output from the CPU Address Register and Counter that indicates a carry-out from the least significant eight bits.
CARRYB	P2-69	Input to the most significant eight bits of the CPU Address Register and Counter. Allows the counter to be incremented by 256 word jumps.
BSFT-	P2-57	Input that, when low, places bits 10-15 of the data word in place of ECC bits 16-21 during a store operation, and places ECC bits 16-21 into bits 10-15 during a read. Replaced bits are discarded.

Table 1-3. Memory Controller Test Interface Signals (Continued)

Signature	Pin No.	Definition
EXCRST-	P2-11	Input that, when low, clears the clock counter circuit.
ECDA-	P1-27	Input that, when low, disables the error correction logic.
EXTOSC-	P2-13	Allows connection of an external oscillator to replace the clock oscillator for the system clock.
SWRST-	P2-12	Allows input of a POWER ON reset signal.
EXTTMR-	P2-43	Allows connection of an external timer to generate refresh requests during full power operation.
OSCENAB	P2-14	Input that, when low, disables the internal oscillator in the system clock circuit. This input must be low in order to use the EXTOSC- input.
TMRRST-	P2-44	Input that, when low, resets the Refresh Request Timer.

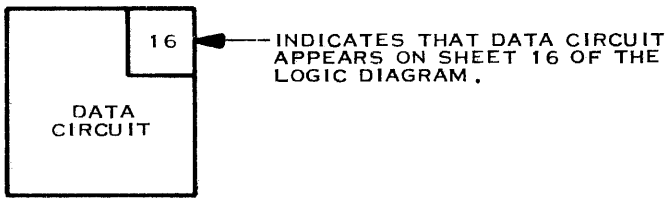
NOTE: CARRYA and CARRYB are connected together by a backplane connection when controller is plugged into computer chassis.

1.2.4 MEMORY CONTROLLER BLOCK DIAGRAM

To aid in understanding the flow of data and control lines through the memory controller, figure 1-5 illustrates the major functional circuits within the controller and their interrelationship. This diagram is the basis of the detailed theory discussion that appears later in this section. The block diagram is a generalized version of the logic diagrams for the memory controller. The following paragraphs describe the format and special conventions used on the diagram to provide better understanding of information contained on the diagram.

1.2.4.1 LOGIC DIAGRAM PAGE NUMBER. Each functional block on the diagram represents a logic or electrical circuit that is represented in detail in the logic diagram for the memory controller. To facilitate location of the circuit within the logic diagram, the sheet number of the logic diagram that

contains the major portion of the functional circuit appears in the upper right corner of the functional block as illustrated below:



1.2.4.2 EXTERNAL ORIGINS AND DESTINATIONS. Signals that leave or enter the circuit board through connector pins have their origins or destinations indicated in parentheses as follows:

(CPU)	Central Processing Unit
(MEM)	Memory Circuit Board
(DMAC)	Direct Memory Access Channel
(TEST)	Special Test Fixture Connection
(PWR SUP)	Power Supply

1.2.4.3 MULTIPLE SIGNAL PATHS. Bold lines represent a large group of signals or a data bus. Lines that carry both the true and false sense signal are labeled with the false sense indicator (a dash) in parentheses following the signature:

SIGNAL(-)

1.2.5 CONTROL CIRCUITS

The memory controller has two major control circuits that coordinate data transfers and refresh cycles throughout the memory system. The Access Control circuit determines the origin of a memory cycle to be either from the CPU or DMAC interfaces or a result of a memory refresh cycle. Concurrently, the Memory Cycle Control circuit determines whether the cycle will be a store or a fetch operation and indicates the end of the memory cycle. The following paragraphs explain the operation of these control circuits.

1.2.5.1 ACCESS CONTROL. Access Control determines the origin of a memory access and generates gating signals that select input data and addresses. Refresh cycle requests receive highest priority and are always recognized. DMAC request receive next consideration. In the absence of either of these two memory requests, the circuit enables CPU memory access. Figure 1-6 illustrates the Access Control logical decision paths.

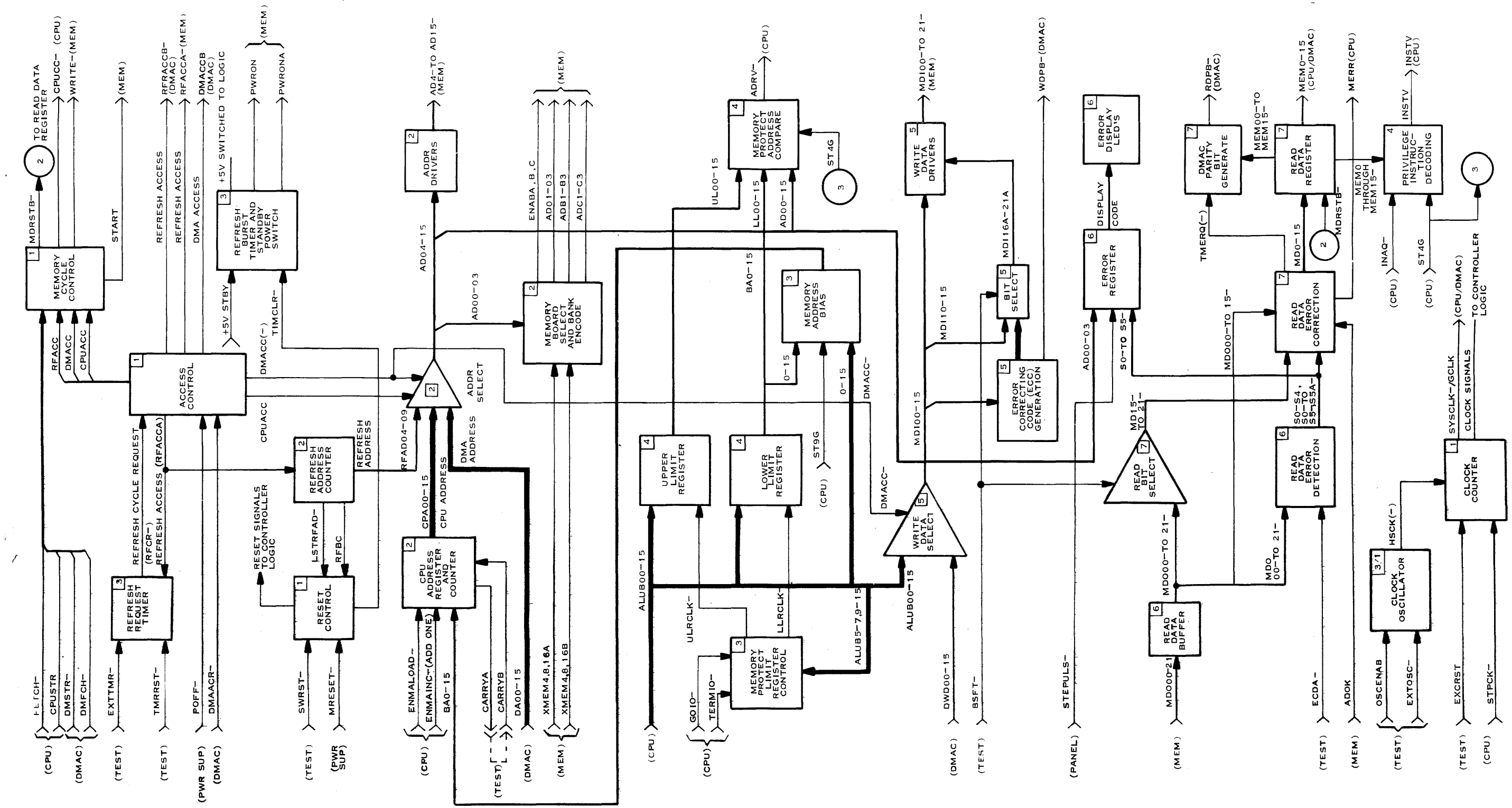


Figure 1-5. Memory Controller Block Diagram

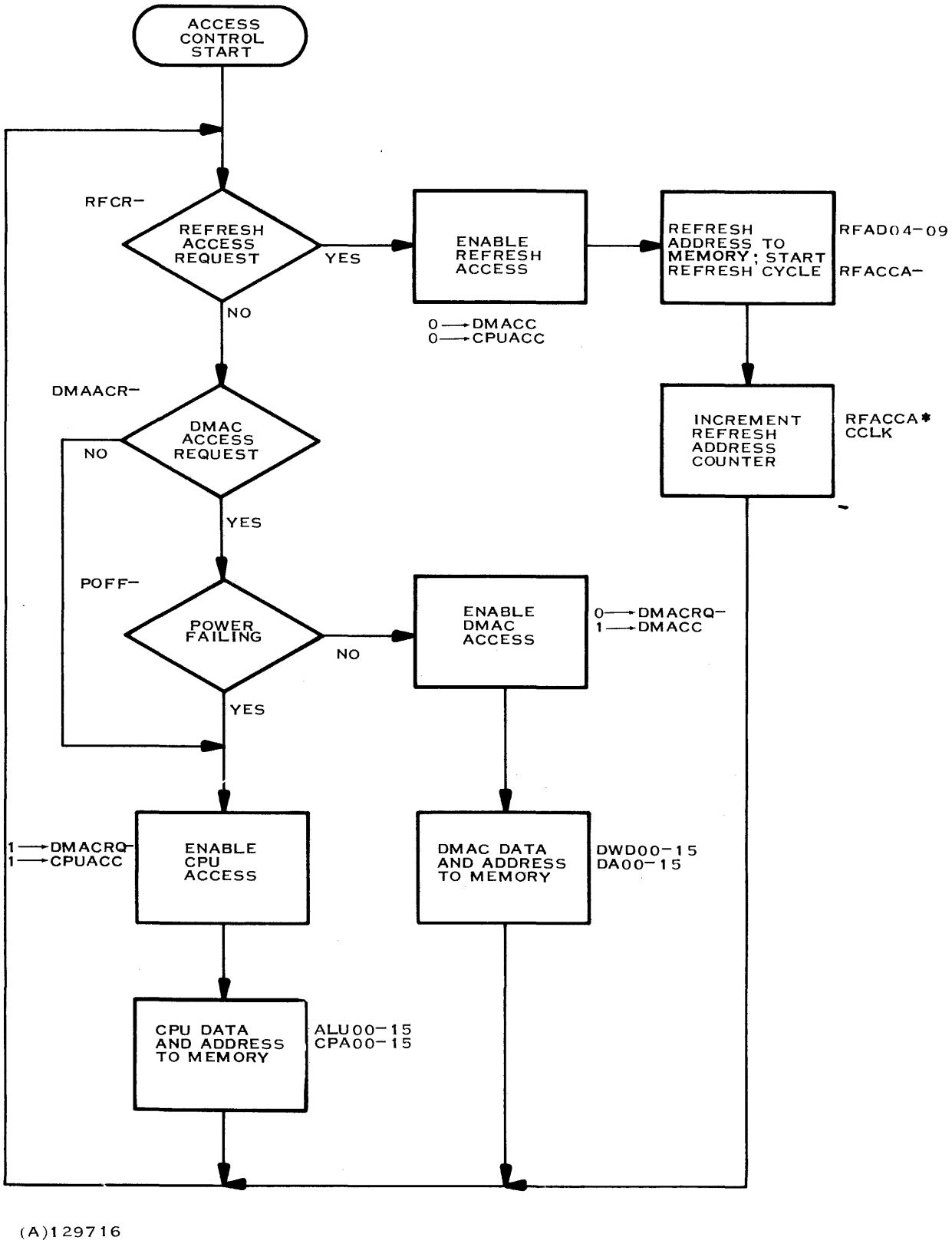


Figure 1-6. Access Control Logic Flowchart

Circuit Description. Access Control consists of three flip-flops and associated gating circuitry as illustrated in figure 1-7. A refresh request from the Refresh Request Timer disables the input gates to the two access control flip-flops (CPUACC and DMACC) clearing both flip-flops with the next clock pulse. With both flip-flops clear, the circuit produces four refresh cycle recognition signals: RFACC-, RFACCA, RFRACCB- and RFACCA-. The first two signals are internal gating signals. RFRACCB- returns to the DMA Controller to disable system clock pulses during a refresh cycle so that the DMA Controller is unaware of the refresh cycle. RFACCA- is forwarded to the memory boards to initiate the refresh cycle. During standby operation, refresh access is continually granted during a refresh burst because MRSTQ- is low, disabling the access control flip-flops.

DMACRQ-FF. In the absence of a refresh request, the DMACRQ- FF sets or clears the access control flip-flops. This flip-flop clears when it receives a memory request from the DMAC interface (DMAACR-), and no power failure is about to occur (POFF-). Clearing this flip-flop sets the DMACC FF on the next clock pulse to enable DMAC data and address into memory. In the absence of a DMAC request, or if a power failure is about to occur, the DMACRQ- FF sets. Setting this flip-flop sets the CPUACC FF to gate data and address from the CPU into memory. Enabling CPU data during a power failure allows the CPU to store certain program parameters before power fails.

1.2.5.2 MEMORY CYCLE CONTROL. Memory Cycle Control monitors the store and fetch signals from both the CPU and the DMAC interfaces and generates the gating signals required to transfer data through the controller to or from the specified area in memory. This circuit also receives inputs from the Access Control circuit to enable requests from either the DMAC or the CPU interface. The control logic consists of two state-control flip-flops, CYCQ0 and CYCQ1, plus the combinational logic required to define the four possible controller states and generate the gating signals required during each controller state. All memory operations must progress through each of the four controller states, and require three phase 2 clock times to perform the cycle. Figure 1-8 illustrates the logic flow within the controller that produces the required gating signals. The following paragraphs describe the decisions within each state.

State 0. Controller State 0 (CYCQ0 and CYCQ1 both clear) monitors the inputs to the controller to determine what type of cycle is to be requested. Upon entering the state, the controller clears the CPU Cycle Complete flip-flop (CPUCCQ) that was set at the end of the previous memory cycle. The controller then determines which interface has access to memory and whether that interface has requested access to memory. If the DMAC interface has access and has generated a memory request, the controller enters State 2 (CYCQ0 set; CYCQ1 clear). If the CPU has access and has requested memory, the controller enters State 2. A refresh cycle also places the controller in State 2.

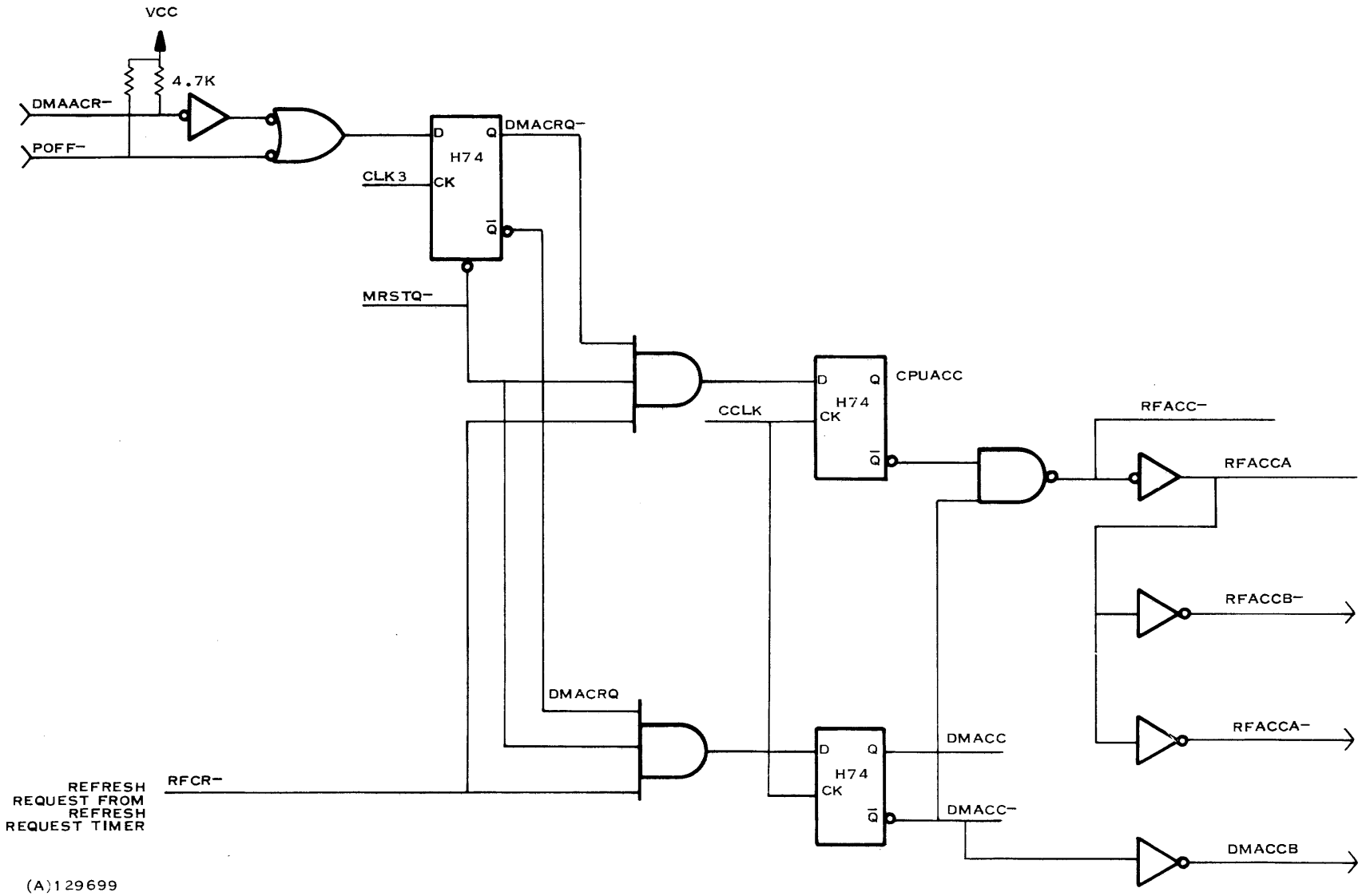


Figure 1-7. Access Control Simplified Logic Diagram

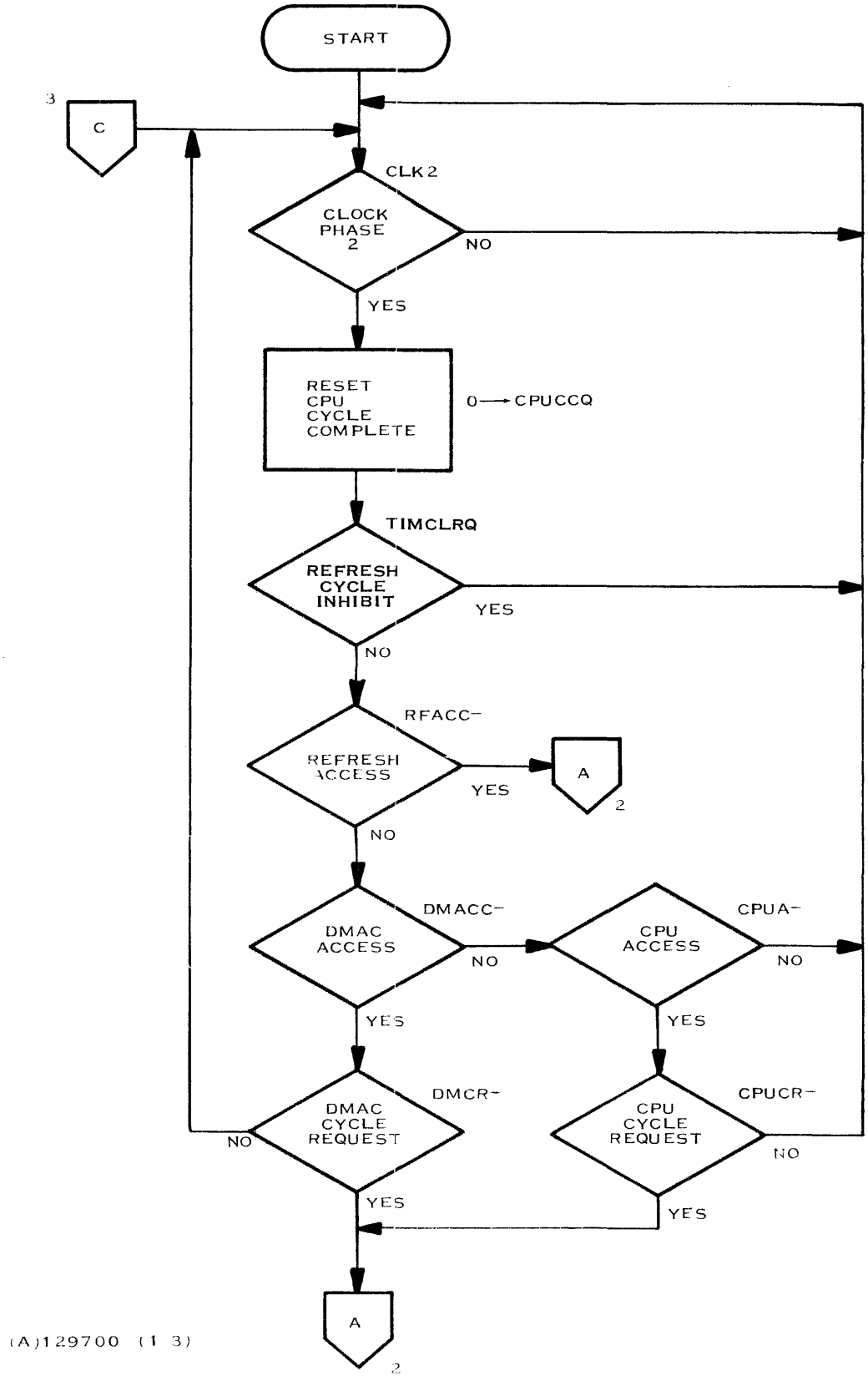


Figure 1-8. Memory Cycle Control Logic Flowchart (Sheet 1 of 3)

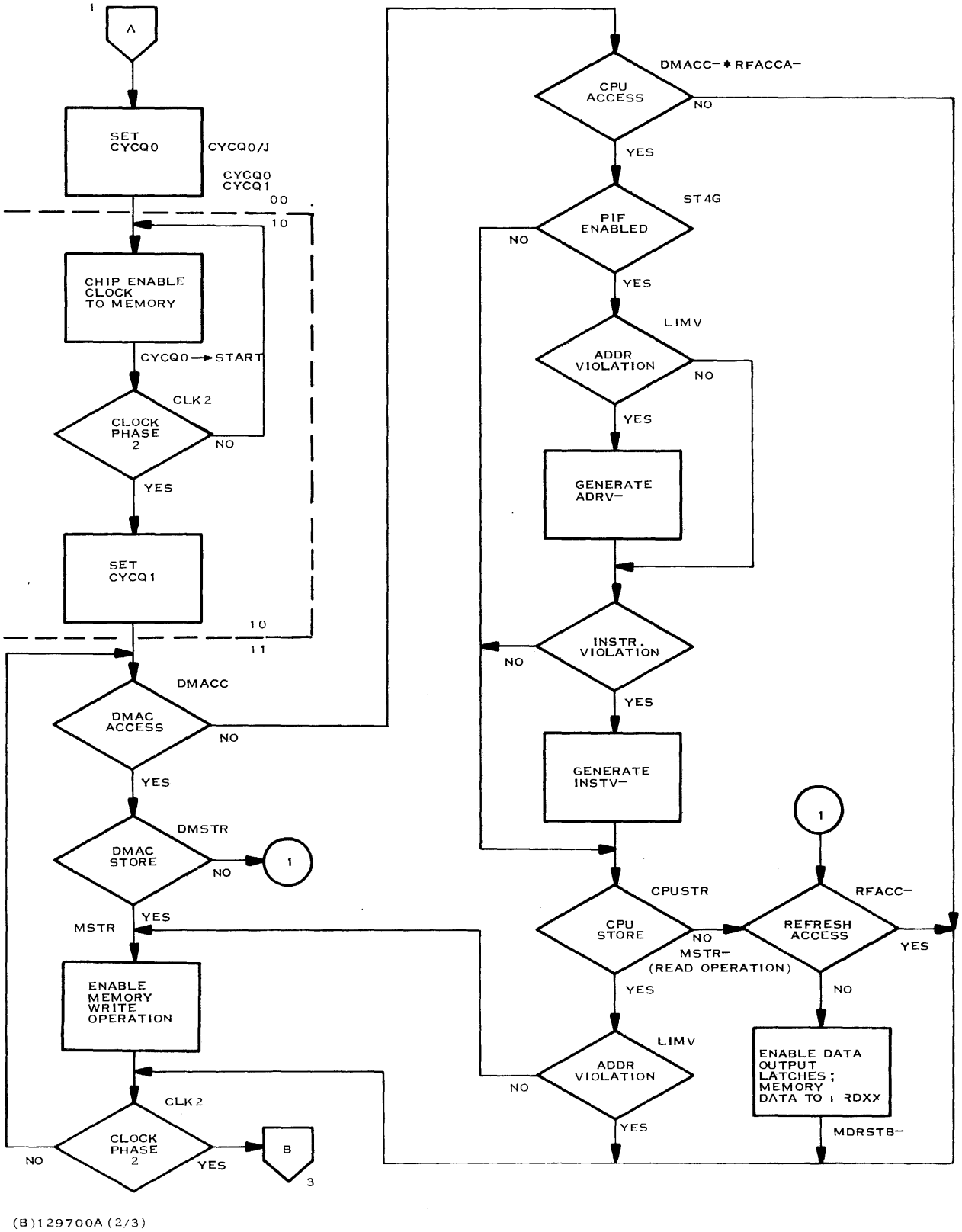


Figure 1-8. Memory Cycle Control Logic Flowchart (Sheet 2 of 3)

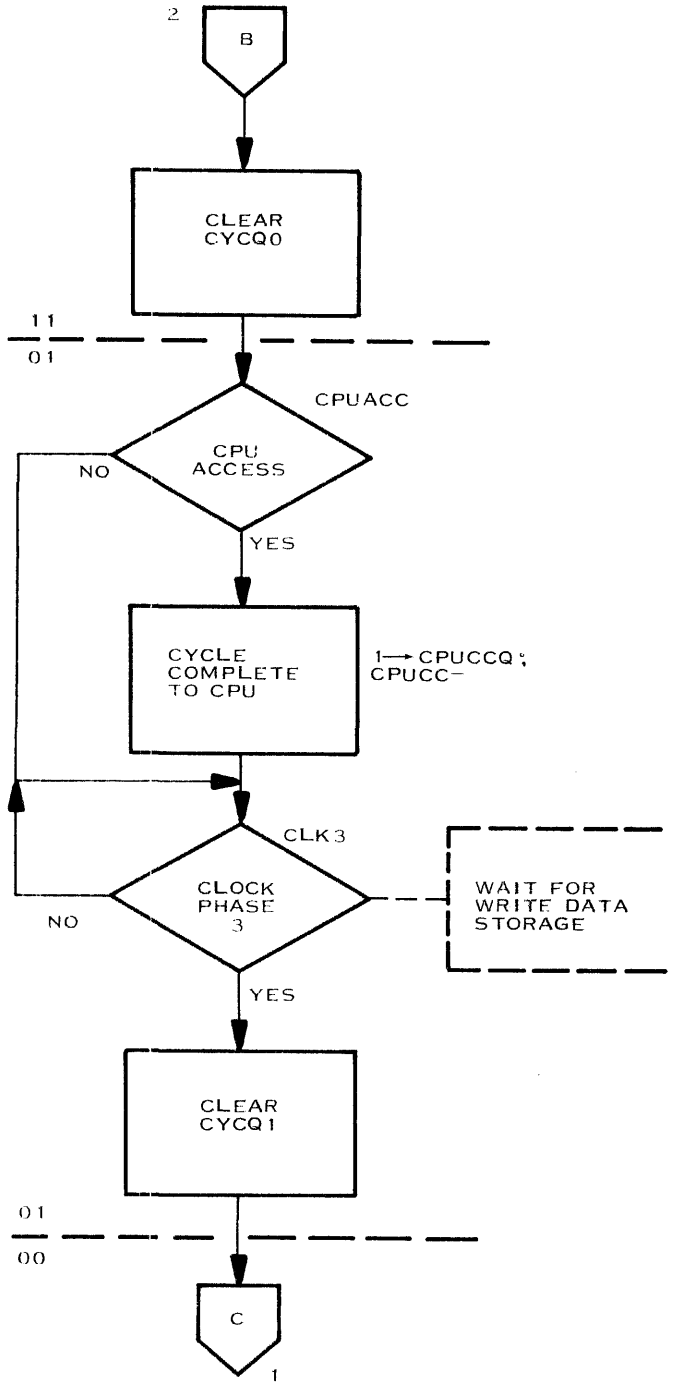


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Figure 1-8. Memory Cycle Control Logic Flowchart (Sheet 3 of 3)

State 2. Setting the CYCQ0 flip-flop immediately produces a chip enable signal (START) to the memory boards. This signal remains high as long as CYCQ0 is set. The controller waits for a phase 2 clock pulse before entering State 3.

State 3. In State 3 (CYCQ0 set; CYCQ1 set) the controller determines if the operation is a store or a fetch operation. If the operation is a fetch, the controller generates MDRSTB- to transfer memory data to the output data latches for placement on the memory bus to the requesting interface (DMAC or CPU). If the operation is a store, the controller produces a WRITE- signal to the memory boards if the operation is not intended for a protected area in memory while the Privileged Instruction Feature is enabled. Store operations to protected memory do not produce a WRITE- signal; the memory boards perform a non-destructive read operation. In all cases the controller enters State 1 with the next phase 2 clock pulse.

State 1. In State 1 (CYCQ0 clear; CYCQ1 set) the controller sets the CPU Cycle Complete flip-flop (CPUCCQ), if the cycle is a CPU memory access. The controller then waits for the phase 3 clock pulse to return it to the State 0 wait mode.

1.2.6 MEMORY STORE

If Memory Cycle Control determines that the operation is a store, then the controller will receive both data and address from the interface selected by Access Control. The controller then examines the address to determine the destination of the store operation, and generates the addressing signals required to properly route the data to the correct location in memory. Concurrently, the controller examines data for memory and generates an Error Checking and Correcting (ECC) code that is stored along with the data in memory. The Error Checking and Correcting circuits are discussed separately, later in this section. The following paragraphs explain the function of each major circuit involved in the memory store operation. Although the addressing circuits are used during both store and fetch operations, they will be described only in reference to store operations. Their function is identical for a fetch operation.

1.2.6.1 MEMORY ADDRESS BIAS. The Memory Address Bias circuit is a selectable adder that allows the addition of the address from the AU to the lower bound address of usable memory for the currently executing program sequence. This feature allows addresses from the AU to be relative to the usable memory area, rather than an absolute memory address. If status bit 9 (ST9G) from the AU is set, the circuit adds the contents of the Lower Limit Register plus one to the incoming address from the AU. If status bit 9 is not set, the circuit passes the incoming address from the ALUB00-15 lines to the CPU Address Register without modification.

The address adder consists of four SN74181 Arithmetic-Logic Unit (ALU) networks and an SN74182 look-ahead network. When ST9G is low, the ALUB inputs to the adder are enabled to the outputs so that no address bias is created. If ST9G is high, the ALU networks add the ALUB inputs to the LL inputs from the Lower Limit register. The carry input to the ALU networks is permantly wired for a carry in. Therefore, the output from the ALU networks contains a biased address (BA00-15) that is the sum of the ALUB and LL lines plus one.

1.2.6.2 CPU ADDRESS REGISTER AND COUNTER. The CPU uses the same bus lines to carry both data and addresses to the memory controller. Therefore, the memory controller must retain the address from the CPU while the data is being transferred. The CPU Address Register performs this function, and also allows the CPU to transmit a single increment signal to access consecutive memory locations instead of sending new addresses for each location. If the data on the ALUB0-15 bus from the CPU is an address, the CPU activates ENMALOAD. This signal, together with the recognized CPU request, gates the address from the address bias network into the address register. This address remains in the register until replaced or modified by another CPU command. The output from the register is then available to the Address Select circuit for transfer to the memory boards, and to the memory protect circuit. To access the next consecutive memory location, the CPU activates ENMAINC-. This signal enables the next clock pulse (GCLKA-) to increment the address in the register. For test and checkout purposes, the carry from the least significant byte to the most significant byte (CARRYB/CARRYA) is routed through the main chassis connector. This connection not only allows the carry signal to be monitored, but permits the address in the register to be jumped in 256 address blocks if connected to the proper test fixture. These two signals are normally connected together in the computer backplane.

1.2.6.3 ADDRESS SELECT. Address Select uses two access granted signals from Access Control to choose an address for a memory access. If the DMACC signal is active, the circuit enables the 16-bit address from the DMAC interface (DA00 to DA15) for use during the memory cycle. If the CPUACC signal is active, the circuit enables the 16-bit address from the CPU Address Register (CPA00 to CPA15). If neither access granted signal is active, the select circuit enables the 6-bit refresh address (RFAD04 to RFAD09) to the memory boards. The upper four bits are not required during a refresh cycle. Both access granted signals cannot be active at the same time.

1.2.6.4 ADDRESS DRIVERS. Twelve NAND gates receive the 12 least significant bits of the address from Address Select, invert the logic level of the address, and transmit the address to the memory boards. The selected memory board uses these address bits to select the required memory location.

1.2.6.5 MEMORY BOARD SELECT AND BANK ENCODE. This circuit receives the four most significant bits of a memory address (AD00 to AD03), compares that address with the size of the memory available from the first two memory boards, and selects the memory board that contains the address. In addition the circuit creates a 3-bit code that is sent to the selected memory board to designate the memory bank that will receive the 12-bit word address. Figure 1-9 illustrates the comparisons that produce the memory board enables and bank select codes.

Board 1. The circuit always transmits a 3-bit bank select code, comprised of address bits 1, 2 and 3, to memory board 1 (the memory board closest to the controller). If address bit 0 is a logic "0", the circuit also produces an enable (ENABA) to memory board 1 so that the memory board will decode the bank select code. However, if the bank select code exceeds the capacity of memory board 1, it will not recognize the address.

Board 2. The circuit also compares the four MSB's of the memory address with the memory size bits from memory board 1 to determine if the address is contained on memory board 2. By adding the memory address bits to the complement memory size code from board 1 with a logic zero in the MSB position, the circuit determines if the address is in excess of the capacity of memory board 1. If this subtraction process produces a result whose MSB is a logic "1", then the address is larger than the capacity of board 1. The

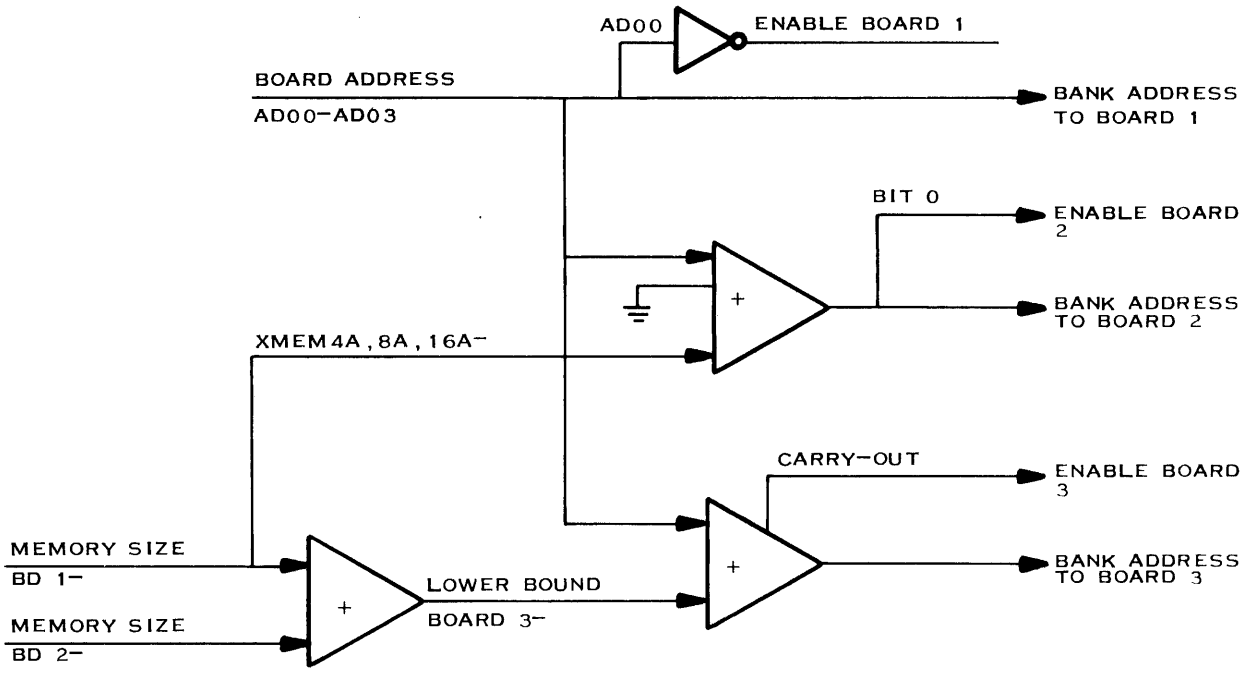

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Figure 1-9. Memory Board Select and Bank Encode Comparison Code

MSB of the result becomes the enable signal to board 2 (ENABB), while the other three resultant bits become the bank select code. If the address is sufficiently larger than the capacity of board 1 (approximately 40K), then the address could not be on board 2. The complement addition in that case may produce an overflow that leaves the MSB of the result at a logic "0", disabling the decoding circuits on board 2.

Board 3. To determine if the address is on board 3, the circuit adds the capacity of board 1 to the capacity of board 2. All addresses in excess of this result are on board 3. The circuit performs a complement addition of the address with the lower bound of board 3 (capacity of 1 + 2). If the addition produces a carry-out from the most significant bit, then the address is greater than the lower bound address. The carry-out signal from this addition becomes the decode enable signal for memory board 3 (ENABC). The three LSB's of the addition become the bank select code that is sent to board 3.

1.2.6.6 MEMORY PROTECTION. The memory controller offers a programmable area of protected memory for use when the Privileged Instruction Feature (PIF) is enabled. If status bit 4 (ST4G) from the AU is set, enabling PIF, then the controller monitors the memory address to ensure that it is within the area prescribed for that program routine. Two registers within the memory controller, the Upper Limit and the Lower Limit Registers, define the upper and lower bounds of the memory area in which memory accesses are permitted when the memory protection feature is active. Only those addresses that are greater than the lower bound address and less than the upper bound will be recognized. All other addresses produce an address violation (ADRV-) indication from the memory controller. This feature is only active for CPU memory cycles. The following paragraphs describe the circuits within the memory controller that perform the memory protection function.

Upper Limit Register. This 16-bit register is loaded under program control to define the upper bound of the usable memory area. When Limit Register Control determines that the data on the ALUB lines from the AU represents an upper limit, it generates ULRCLK- to load the data into the Upper Limit Register. The contents of the register are then available to the Address Compare circuit to determine an address violation.

Lower Limit Register. This 16-bit register is loaded under program control to define the lower bound of the usable memory area. When Limit Register Control determines that the data on the ALUB lines from the AU represents a lower limit, it generates LLRCLK- to load the data into the Lower Limit Register. The contents of the register are then available to the Address Compare circuit to determine an address violation.

Limit Register Control. The AU loads the limit registers by executing two Write Direct Single (WDS) instructions. A WDS to external register number zero loads the Lower Limit Register; a WDS to external register number one loads the Upper Limit Register. Figure 1-10 illustrates the control logic that monitors the AU instructions to determine the two WDS instructions and generate the load clock signals for the limit registers. When the circuit receives the GO pulse from the AU, it examines bit 10 of the data bus to determine if the instruction is a WDS. For a WDS instruction, the controller produces GOEN to enable the register number decode circuit. The decode circuit recognizes either register number zero or register number one (register number is contained in bits 5-7, 9, and 11-15 of WDS instruction). If all register number bits are zero, the LOW flip-flop sets; if all but bit 15 are zero, the UP flip-flop sets. Receipt of the TERM pulse from the AU completes one of two gates to produce a load clock (ULRCLK- or LLRCLK-) to one of the limit registers when the second word (data) of the WDS transfer is stable on the ALUB lines.

Address Compare. To detect an address violation, the output of the Address Select (AD00 through AD15) is compared to the upper and lower address limits. Four SN7485 comparator networks compare the address to the lower limit and produce signal AGTLLM if the address is greater than the lower limit. A second set of four SN7485 networks produce signal ALTULM if the memory address is less than the upper limit. These two signals produce a limit violation signal (LIMV) if the address falls outside of the address limits. The LIMV signal combines with cycle complete (CPUCC) and the PIF enable status bit (ST4G) to generate the address violation signal (ADRV-) to the AU. LIMV also inhibits the WRITE- signal to memory when ST4G is set, so that memory performs a non-destructive read operation in the protected area.

1.2.6.7 WRITE DATA SELECT. Write Data Select uses DMAC access granted (DMACC-) to determine which of two 16-bit inputs to transfer to the write drivers for transmission to the memory boards. If DMACC- is low, the circuit selects the data input from the DMAC interface for storage into memory. If DMACC- is high, the circuit selects the input from the CPU interface (ALUB00 to ALUB15). In addition to being transferred as write data to the memory boards, the selected 16 bits are input to the ECC Generation circuit.

1.2.6.8 WRITE DATA DRIVERS. Twenty-two inverter-driver circuits receive 16 data bits from the Write Data Select circuit and six more ECC bits from the ECC Generation circuit, invert the logic levels of the bits, and transmit them to the memory boards. The selected memory board then stores this bar (low active) data into the addresses area in memory.

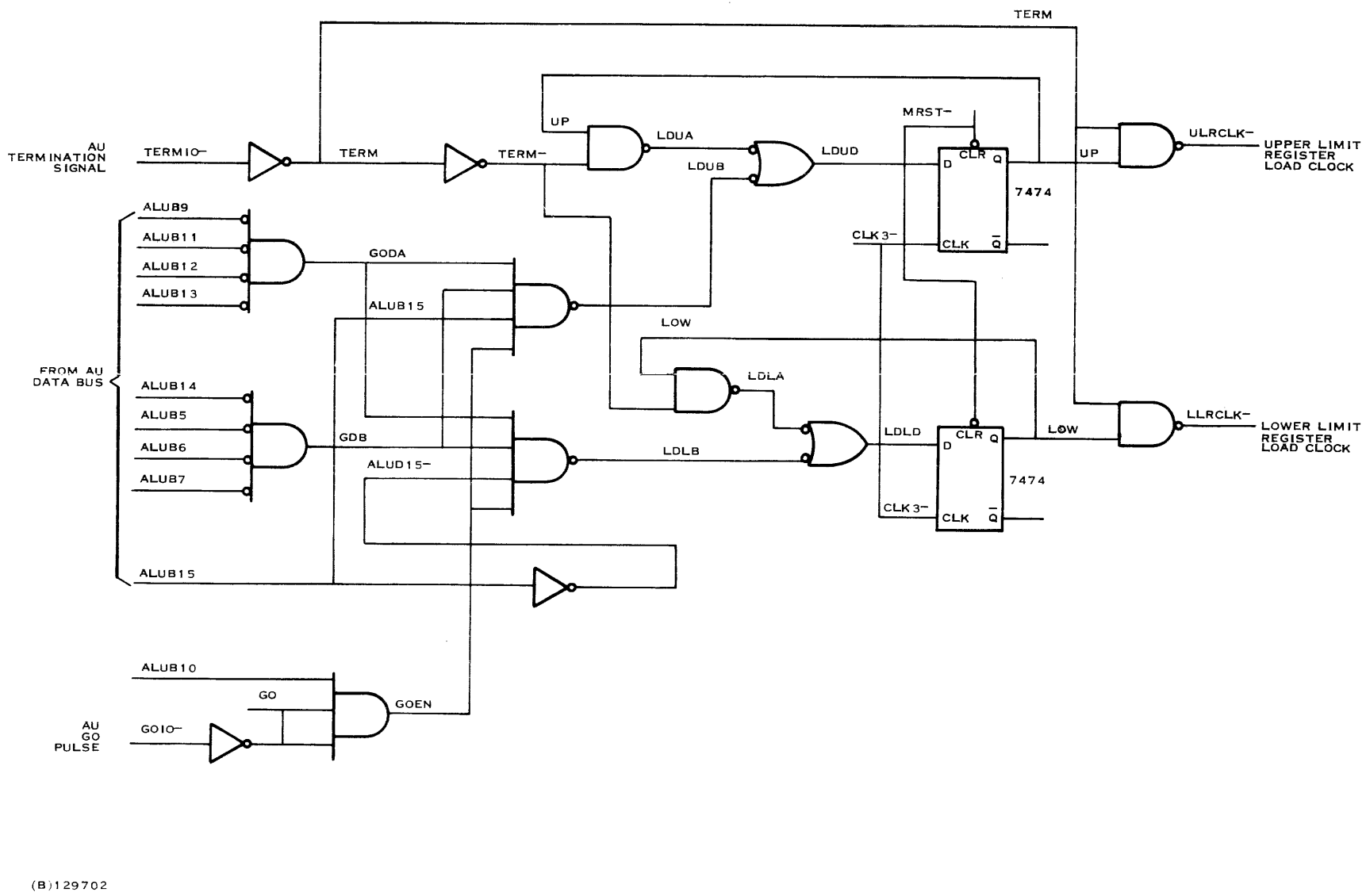

Figure 1-10. Limit Register Control Simplified Logic Diagram

1.2.7 MEMORY FETCH

If Memory Cycle Control determines that the operation is a fetch, then the controller receives address bits from and transmits memory data to the interface selected by Access Control. The following paragraphs describe the major functional circuits involved in the fetch operation excluding the error correction logic and the addressing circuits. Both of these area are covered elsewhere in this section.

1.2.7.1 READ DATA BUFFERS. Twenty-two inverter-buffer circuits receive true (high active) data from the memory chips during a memory read cycle (16 data bits and 6 ECC bits), invert the logic levels of the data, and apply the inverted data to the Read Data Select and Read Data Error Detection circuits.

1.2.7.2 READ DATA SELECT. Read Data Select receives input data from the Read Data Buffers (22 bits) and uses one control signal (BSFT-) to select the configuration of data bits to be sent to the Error Correction circuit and ultimately to the requesting interface. BSFT- is a maintenance signal that, when low, causes Read Data Select to place the ECC bits (16 through 21) in the data word in place of the six least significant bits (10 through 15). The six least significant data bits are discarded. When high, BSFT- enables the 16-bit data word from memory without change. BSFT- is generated by a special test fixture during checkout, and can be produced for maintenance purposes by connecting a jumper wire from terminal TP4 to terminal TP5 on the memory controller circuit board.

1.2.7.3 READ DATA REGISTER. The Read Data Register is a 16-bit register that receives corrected (if error correction is enabled) data that has been read from memory. The Read Data Register then holds the data for transmission to the requesting interface (DMAC or CPU). The Memory Data Register Strobe pulse (MDRSTB-) from Memory Cycle Control loads the data into the register. The data is then available at the circuit board output connector pins for sampling by the requesting interface. The inverted data output from the register is sent to the DMAC Parity Bit Generation circuit to develop a parity bit for use by the DMAC interface, and to the Privileged Instruction Decoding circuit for detection of a PIF violation.

1.2.7.4 DMAC PARITY BIT GENERATION. This circuit receives inverted data from the Read Data Register and develops an odd parity bit that, when high, indicates that the data word sent to the DMAC interface contains an even number of "1" bits. The parity bit is generated from the data actually sent to the DMAC interface. The DMAC interface does not receive the MERR signal indicating that an uncorrectable error occurred during the read cycle.

Therefore, if an uncorrectable error occurs, the DMAC interface has no separate indication that the data is bad. To inform the DMAC interface of a faulty data word, the output of the TMERQ FF in the Error Correction circuit is input to the Parity Generation circuit. When an uncorrectable error occurs, the TMERQ input forces the Parity Generation circuit to produce an incorrect parity bit. When the DMAC interface checks the parity of the incomming word and detects the parity error, it will know that the data is incorrect.

1.2.7.5 PRIVILEGED INSTRUCTION DECODING. When status bit 4 (ST4G) enables the Privileged Instruction Feature, the memory controller monitors each instruction as it is read from memory to determine if it is an illegal instruction. Illegal instructions when PIF is active are: Idle (IDL), Read Direct Single (RDS), Write Direct Single (WDS), Load Status Block (LSB), Load Status Block and Reset Interrupt (LSR), Automatic Transfer Initiate (ATI), and any register-to-register instruction that has a destination of the status register (bits 12-15 equal to 1000). If any of these illegal instructions is detected, the memory controller sends an instruction violation signal (INSTV-) to the AU.

Figure 1-11 illustrates the circuit that detects the illegal instructions. When ST4G is high, the circuit waits for an indication from the AU that the current memory cycle is for an instruction (INAQ-). The cycle complete signal (CPUCC) during the last 167 nanoseconds of the memory cycle completes the AND gate that generates INSVEN to enable the circuit. The circuit then examines the output of the Read Data Register to determine if the instruction that was retrieved from memory is a legal instruction. If the circuit detects the code of one of the illegal instructions, it activates INSTV- to the AU to indicate that the instruction being transferred to the AU is an illegal instruction.

1.2.8 ERROR CHECKING AND CORRECTION

To ensure accurate storage and retrieval of data, the memory controller generates a 6-bit code during a store operation, and checks that code during a read operation on the data. This code enables the controller to detect and correct single-bit errors, and to detect double-bit errors. The probability of encountering greater than two errors in any 22-bit memory word is slight. Therefore, the controller makes no provision for errors greater than two bits. The following paragraphs describe the controller circuits that produce and check the Error Checking and Correction (ECC) bits, and that use the results of that check to correct data read from memory.

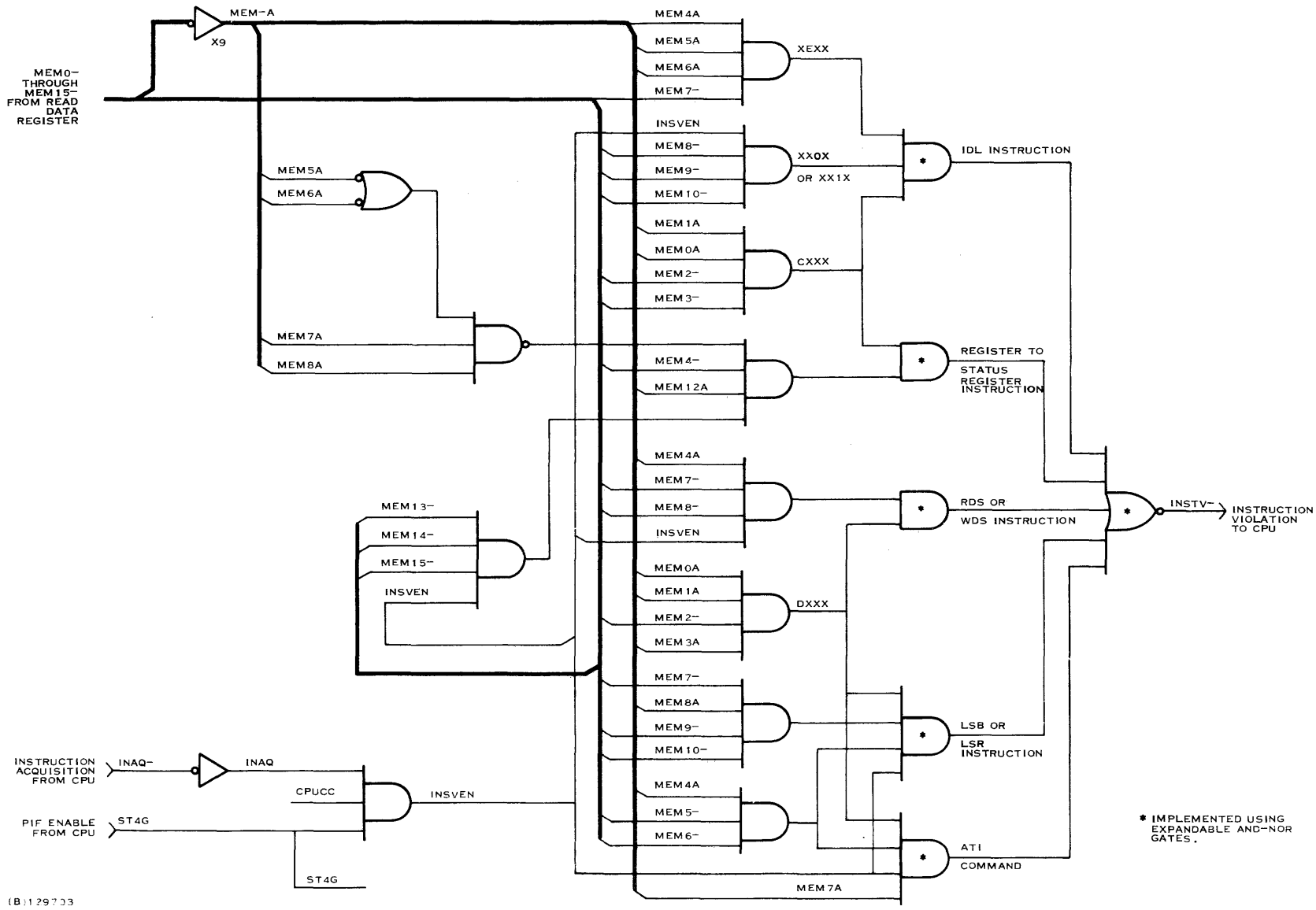

Figure 1-11. Privileged Instruction Feature Decoding Circuit Simplified Diagram

1.2.8.1 ECC BIT GENERATION. During a store operation the ECC Generation circuit receives the 16-bit data word, and using a modified Hamming code, produces six check bits that are stored along with the data word as bits 16 through 21. The controller uses the check bits to identify any bit in error if a 1-bit error occurs in the data when it is read from memory. Each check bit is an odd parity bit for selected bit-groups within the data word, such that each bit in the data word participates in either three or five of the parity bits. If an error occurs in data read from memory, then the check bits generated from the read data will not match the check bits stored with the data. Examination of the bits that vary isolates the bit in error in the data word. Data errors produce three or five mismatched bits. If only one bit is mismatched, the check bit is in error. Figure 1-12 illustrates the generation patterns for each of the check bits. This circuit also produces a parity bit to the DMAC interface to indicate that the data word contains an odd number of "1" bits (WDPB-).

1.2.8.2 BIT SELECT. The Bit Select circuit allows maintenance and checkout personnel to select either the ECC bits or the six least significant data bits for storage into bits 16 through 21 of the memory word. The BSFT- signal controls this selection. When low, this signal selects bits 10 through 15 of the data word; when high, this signal selects the ECC bits. BSFT- is

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DATA BIT / CHECK ** BIT
							X	X	X	X	X	X*	X	X	X	16
X		X		X		X	X	X		X		X*		X		17
X	X			X	X			X	X			X*	X			18
X	X	X	X					X	X	X	X					19
X	X	X	X	X	X	X	X								X	20
X			X		X	X		X			X		X	X	X	21

*BITS 16, 17 AND 18 MISMATCHED INDICATES DATA BIT 3 IN ERROR.

**EACH CHECK BIT IS ODD PARITY FOR THOSE DATA BITS MARKED WITH X IN THE CORRESPONDING ROW.

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Figure 1-12. Error Correction Check Bit Generation

normally high when the memory controller is inserted into the computer chassis, since the pin is not connected. The connector pin for this signal is used for memory checkout in a special test fixture. However, for on-site maintenance BSFT- can be activated by connecting a jumper wire from terminal TP4 to terminal TP5 on the memory controller as illustrated in figure 1-13. This feature with its corresponding effect on Read Data Select allows display of the ECC bits on the computer control panel for error isolation within the ECC bits.

1.2.8.3 READ ERROR DETECTION. This circuit receives the 22-bit memory word and examines the data to determine if an error has occurred. The circuit generates ECC bits from the 16-bit data word and compares the resulting ECC bits with the ECC bits read from memory. If any of the bits fail to compare, the circuit generates error syndrome bits (S0- through S5-) corresponding to the ECC bit that failed. The controller decodes these signals in the Read Data Error Correction circuit to determine the bit in error.

ECC Bit 21. The circuit that produces the S5- error indicator is markedly different from the circuit that generated the stored ECC bit 21. Bit 21 is generated as an odd parity bit for bits 0, 1, 2, 4, 7, 9, 10, 12 and 15 of the data word before being stored in memory. Selection of these bits to form bit 21, however, is an algorithm for determining parity for the entire 22 bits. Bit

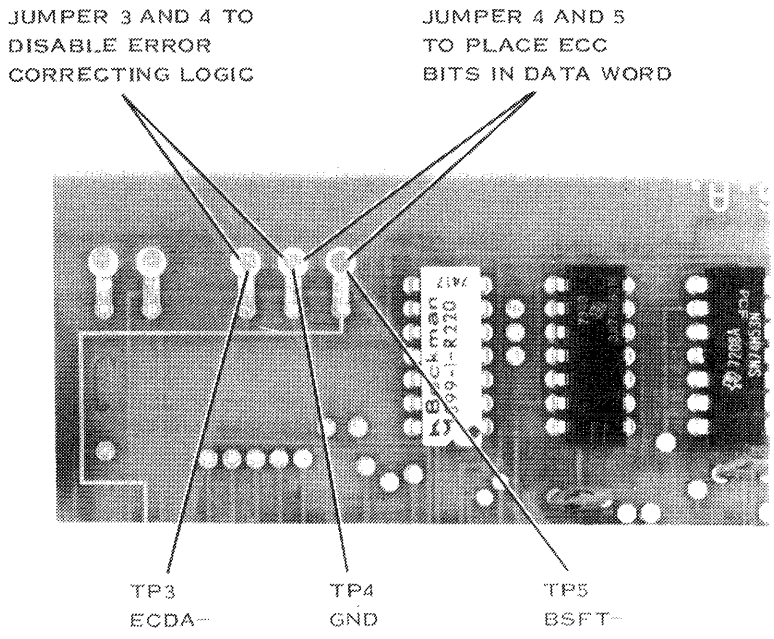

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Figure 1-13. BSFT- Jumper Connection for Maintenance Use

21, therefore, indicates odd parity for all other bits in the memory word. Instead of using the algorithm to generate bit 21 during error detection, the circuit checks parity of the whole 22-bit memory word. If that parity is incorrect, then an odd number of bit errors has occurred. The circuit assumes that only one error occurred and generates the S5- error signal to indicate that a correctable error occurred.

ECC Disable. An external input (ECDA-) to the S5- circuit allows a special test fixture to disable the error correction circuit by holding S5- high. The S5- signal, when low, gates the error syndrome bits into the error correcting circuit, so that holding this signal high disables error correction. Error correction can also be disabled without a special test fixture by connecting a jumper wire from terminal TP4 to terminal TP3 on the memory controller board to hold S5- high.

1.2.8.4 READ DATA ERROR CORRECTION. If a single-bit error is detected, the S5- signal from the Error Detection circuit enables the Error Correction circuit. The Error Correction circuit receives all of the syndrome bits (S0- through S5-) and decodes them to determine which bit is in error. The decode circuit then generates a low-level signal to the input of an Exclusive OR gate, together with the inverted sense memory bit. The low-level signal passes the data bit through the Exclusive OR gate unchanged. Bits not in error pass through similar gates, except that the correction signal input is high and causes the correct bits to be inverted. The output of the 16 Exclusive OR gates, then, represents true memory data. Since the noninverted bit was wrong when input to the circuit, it becomes correct at the output of the circuit because all other bits were inverted. Figure 1-14 provides a simplified illustration of the correction gates.

If a double-bit error occurred during the write-read process, the Error Correction circuit cannot correct the data. Instead, bit S5- high enables the syndrome bits to set MERRQ FF so that a memory error signal (MERR) will be sent to the requesting interface along with the data. MERRQ FF also sets if a single-bit error occurs and the error correcting logic has been disabled as described in the description of the Read Data Error Detection circuit.

If more than two errors occur, the action taken depends on the number of errors. For an even number of errors the data is not changed and the memory error signal is generated as if it were a double-bit error. An odd number of errors is treated as a single-bit error. However, the bit that is changed by the correction circuit is not necessarily one of the bits in error.

1.2.8.5 ERROR REGISTER. The Error Register is a 10-flip-flop register that monitors the most significant four bits of the current memory address and the six syndrome bits from the Read Data Error Detection circuit (S0- through S5-). If any error occurs during the read cycle that is detected by the controller, a strobe to this register transfers the syndrome bits and the

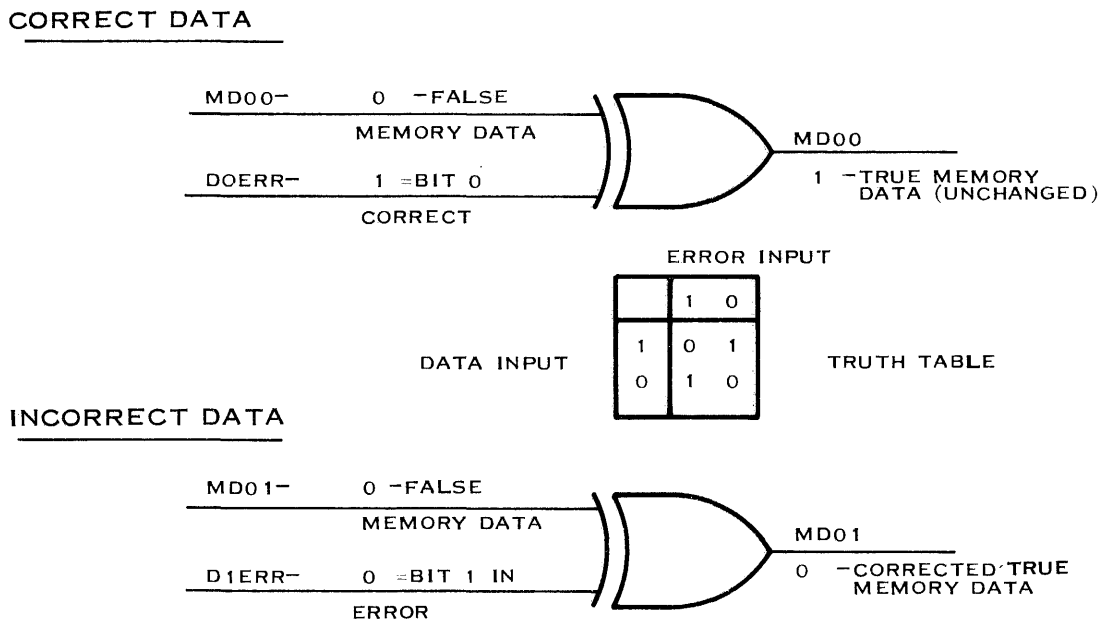

Figure 1-14. Error Correcting Gate

four address bits into the Error Register. The register then sinks current to drive the Error Display LED's corresponding to the address bits that are one and the syndrome bits that are zero. The LED's light only if enabled by connecting TP1 to TP2 with a jumper wire, and can be used to determine the location of a faulty memory chip.

1.2.8.6 ERROR DISPLAY LED's. Ten light-emitting diodes (LED's), mounted on the top edge of the memory controller, light to indicate which of the memory integrated circuit packages in the memory system produced an error during the last read operation. The LED's are mounted in two groups as illustrated in figure 1-15. A jumper is connected from TP1 to TP2 on the controller board to supply power to the LED's.

Bank Error Indicators. The upper row of indicators (CR7 to CR10) designate which bank of memory chips produced the error. These indicators display the four most significant bits of the memory address used in the fetch operation. Table 1-4 lists the possible display patterns of these indicators and the bank that corresponds to each pattern. Using fully implemented memory boards, banks 0 through 5 are on the first memory board (closest to the controller board), banks 6 through 11 are on the next memory board, and banks 12 through 15 are on the last memory board. Each bank is a physical row of 22 memory chips on the memory board, with the lowest numbered

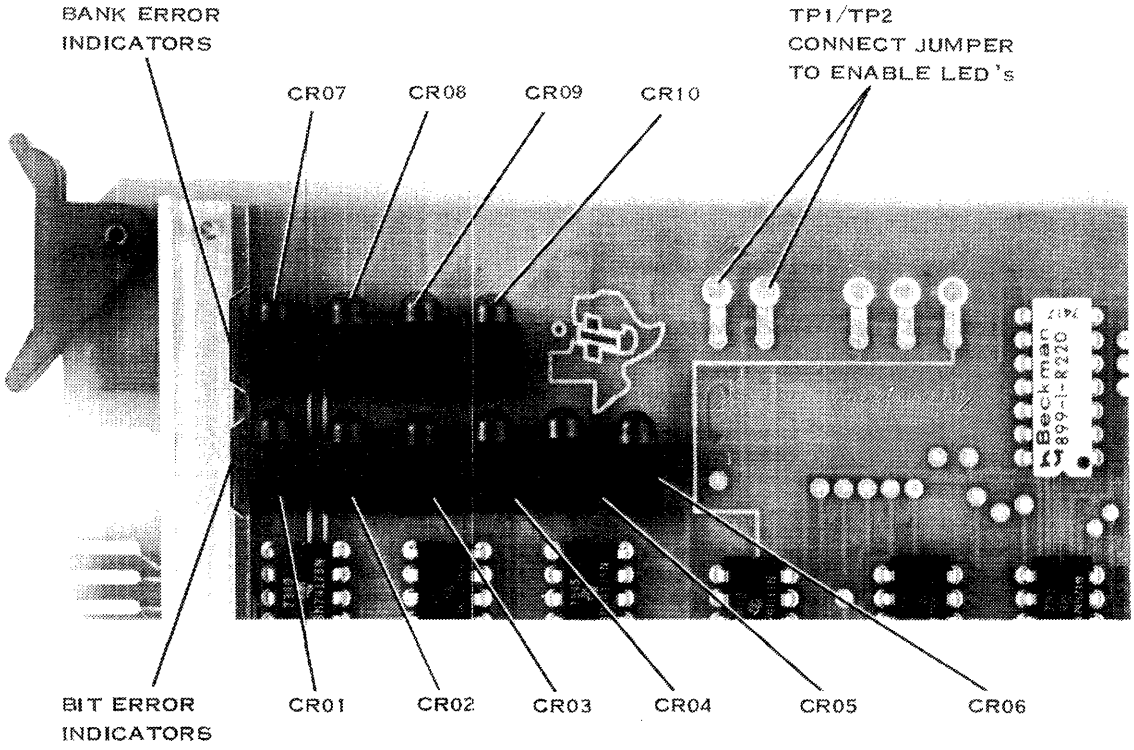

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Figure 1-15. Bank and Bit Error Indicators

bank at the top of the board and the highest numbered bank on the bottom of the board. Therefore, the bank error indicators isolate the error to a physical row of memory chips on one of the memory boards. If the memory boards are not fully implemented, the banks are numbered consecutively without skipping any bank number, and without assigning a bank number to a vacant row.

Bit Error Indicators. The second row of LED's (CR01-CR06) indicate which bit in the memory word was in error. Since each memory chip corresponds to one bit of the memory word (4096 words wide), the LED's also isolate the faulty memory chip within the bank of chips indicated by the bank error indicators. The Bit Error Indicators are only valid for single bit memory errors.

Table 1-4. Bank Error Indicator Decode

Led Pattern				Bank in Error
CR07	CR08	CR09	CR10	
-	-	-	-	0
ON	-	-	-	1
-	ON	-	-	2
ON	ON	-	-	3
-	-	ON	-	4
ON	-	ON	-	5
-	ON	ON	-	6
ON	ON	ON	-	7
-	-	-	ON	8
ON	-	-	ON	9
-	ON	-	ON	10
ON	ON	-	ON	11
-	-	ON	ON	12
ON	-	ON	ON	13
-	ON	ON	ON	14
ON	ON	ON	ON	15

The display pattern is not a binary representation of the bit number, but instead displays the ECC bits that did not correspond to the ECC of the word read from memory. Table 1-5 lists each valid display pattern and the corresponding bit in error. Errors in bit 0, 8 or any of the check bits are special case codes. However, the remaining bit errors can be recognized through a simple system of decoding the display LED's. CR01 is always lighted when a single bit error occurs. If CR06 is lighted and is not the only other LED lighted, then LED's CR03, CR04 and CR05 form a binary code that designates which data bit, 1 through 7, produced the error. Similarly, of CR02 is lighted and is not the only other LED lighted, the LED's CR03, CR04 and CR05 again form a binary code that designates which data bit, 9 through 15, produced the error. When CR02 and CR06 are lit, CR05 is read to determine if bit 0 or 8 is in error. When facing the component side of the memory

Table 1-5. Bit Error Indicator Decode

Led Pattern*						Bit in Error
CR01	CR02	CR03	CR04	CR05	CR06	
ON	ON	-	-	-	ON	00
ON	-	-	-	ON	ON	01
ON	-	-	ON	-	ON	02
ON	-	-	ON	ON	ON	03
ON	-	ON	-	-	ON	04
ON	-	ON	-	ON	ON	05
ON	-	ON	ON	-	ON	06
ON	-	ON	ON	ON	ON	07
ON	ON	-	-	ON	ON	08
ON	ON	-	-	ON	-	09
ON	ON	-	ON	-	-	10
ON	ON	-	ON	ON	-	11
ON	ON	ON	-	-	-	12
ON	ON	ON	-	ON	-	13
ON	ON	ON	ON	-	-	14
ON	ON	ON	ON	ON	-	15
ON	-	-	-	-	ON	16
ON	-	-	-	ON	-	17
ON	-	-	ON	-	-	18
ON	-	ON	-	-	-	19
ON	ON	-	-	-	-	20
ON	-	-	-	-	-	21

*Except for bits 0 or 8 and 16-21, CR03 - CR05 form a binary code that defines bit in error within group indicated by either CR06 or CR02.

- indicates off.

circuit board, the chip corresponding to bit 0 is the left-most chip in each bank; the chip corresponding to bit 21 is the right-most chip in each bank. The memory chips are mounted in sockets for easy replacement.

1.2.9 MEMORY REFRESH

Data is stored in the MOS memory chips as capacitive charges. These charges drain away over time at a rate that is proportional to the temperature of the circuit. In order to maintain the data within the memory chips, these charges must be restored periodically by performing a refresh cycle for each memory location. The memory chip performs the read cycle internally and, since the chip select is not supplied during refresh cycles, no data output occurs from the chip. Memory, therefore, requires only an address and a clock to perform a refresh cycle. The address for refresh cycles consists of the six most significant bits of the 12-bit address normally available to the chip, so that each refresh cycle restores the information in 1/64 of the memory chip. During normal computer operation under worst case temperature conditions, memory must be refreshed every two milliseconds to prevent loss of data. When operating under standby battery power, the refresh period varies from two milliseconds to eight milliseconds as the temperature within the chassis drops due to the inactive logic circuits. The memory controller coordinates these refresh operations and transmits the required refresh address to the memory circuit boards for the refresh cycle. The major controller functional areas involved in the refresh cycle are the Refresh Request Timer, the Refresh Address Counter, portions of Access Control, and the Refresh Burst Timer. The following paragraphs describe the operation of those components exclusive to the refresh operation.

1.2.9.1 REFRESH REQUEST TIMER. The Refresh Request Timer generates a request for a refresh cycle to the Access Control circuitry every 31 microseconds during full power operation of the computer. The timer is non-functional during standby operation since its input to the Access Control circuit is disabled by a master reset level signal when standby power (+5VSW) is turned on. This reset level (MRSTQ-) is produced by the Reset Control circuitry. The timer circuit consists of an oscillator circuit that produces a 32-KHz output plus some associated gating circuits as illustrated in figure 1-16. During normal operation, the oscillator produces one TMR pulse every 31.2 microseconds. The TMRQ FF sets between TMR pulses so that when the TMR pulse occurs a refresh access request is generated. When the Access Control circuitry recognizes the request, it returns a refresh access signal (RFACCA) to the timer circuit that clears the TMRQ FF. This FF is then prepared for the next timer cycle. Refresh access requests have priority over all other memory requests, so that they are recognized immediately during normal power operation. Memory cycles in progress are not interrupted, but are allowed to complete before the refresh cycle is performed. An external input, TMRRST-, resets the oscillator and disables its output when the input is at a low level. A second input, EXTTMR-,

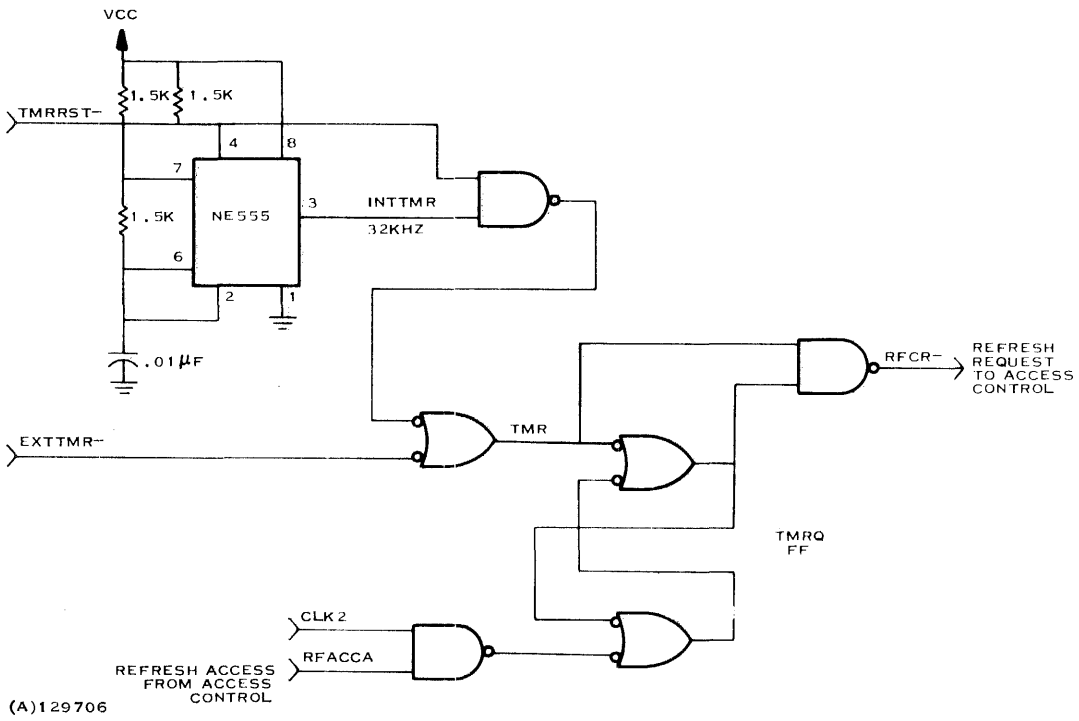


Figure 1-16. Refresh Request Timer Simplified Logic Diagram

allows an external circuit to provide request pulses in lieu of the internal oscillator. These inputs are used only for test purposes.

1.2.9.2 REFRESH ADDRESS COUNTER. The Refresh Address Counter (see figure 1-17) produces sequential addresses that are transferred to the memory circuit boards as the most significant six bits of the 12-bit word address applied to the memory chips. This address selects 1/64 of the available memory locations for refreshing during each refresh cycle. The counter uses two 4-bit binary counter integrated circuits. A clock pulse and the Refresh Access signal (RFACCA) from Access Control increment the counter following each refresh cycle to ensure that a new address will be ready for the next refresh cycle. During normal power operation, the counter supplies one address every 31.2 microseconds. The counter is never cleared during normal operation, so that it cycles through four sets of addresses before the counter rolls over to contain all zeroes (the least significant six bits of the 8-bit counter are used for the address; the upper two bits are not used during normal power operation).

During standby power operation, the memory controller is not running continuously so that spacing the refresh cycles evenly apart is not practical. Instead, a burst of 64 addresses is produced at periodic intervals (defined by the ambient temperature) to refresh the entire memory in a short period of time. Following the burst, the memory controller power is removed until

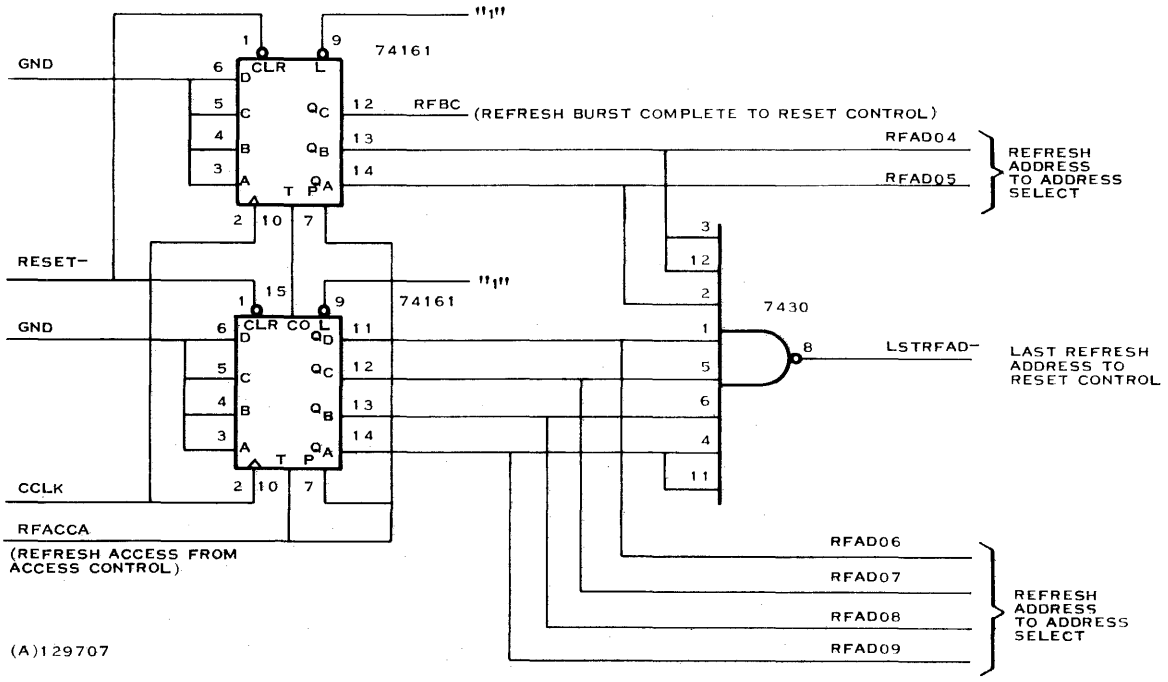


Figure 1-17. Refresh Address Counter

another burst is required. The timing of these refresh bursts is determined by the Refresh Burst Timer circuitry. At the start of each refresh burst, the Reset signal generated by application of +5VSW power clears the counter to zero. The Refresh Access signal (RFACCA) remains high throughout the entire burst, so that the counter is incremented with each clock (CCLK) (for a total of 64 clock pulses). When the counter reaches address $3F_{16}$, the circuit sends a Last Refresh Address (LSTRFAD-) to the Reset Control circuit to reset MRSTQ FF. The next clock pulse produces address 40_{16} from the counter. The output signal generated from the seventh bit of the counter indicates to the Reset Control circuit that the Refresh Burst is Complete (RFBC). This signal sets the TIMCLR FF to clear the Refresh Burst Timer and turn off power to the memory controller and memory boards. CCLK occurs at the end of each 750 nanosecond memory cycle.

1.2.9.3 REFRESH BURST TIMER. The Refresh Burst Timer determines the refresh rate of the memory circuits when the memory is operating on standby power from the battery. The timer is a discrete component circuit that monitors the temperature of ambient air within the computer chassis and adjusts the refresh rate to ensure maintenance of data within the memory chips while using as little battery power as possible. The refresh rate varies from once every 8 milliseconds at 25 degrees Centigrade to once every 2 milliseconds at 70 degrees Centrigrade. Figure 1-18 illustrates a simplified form of the timer circuit.

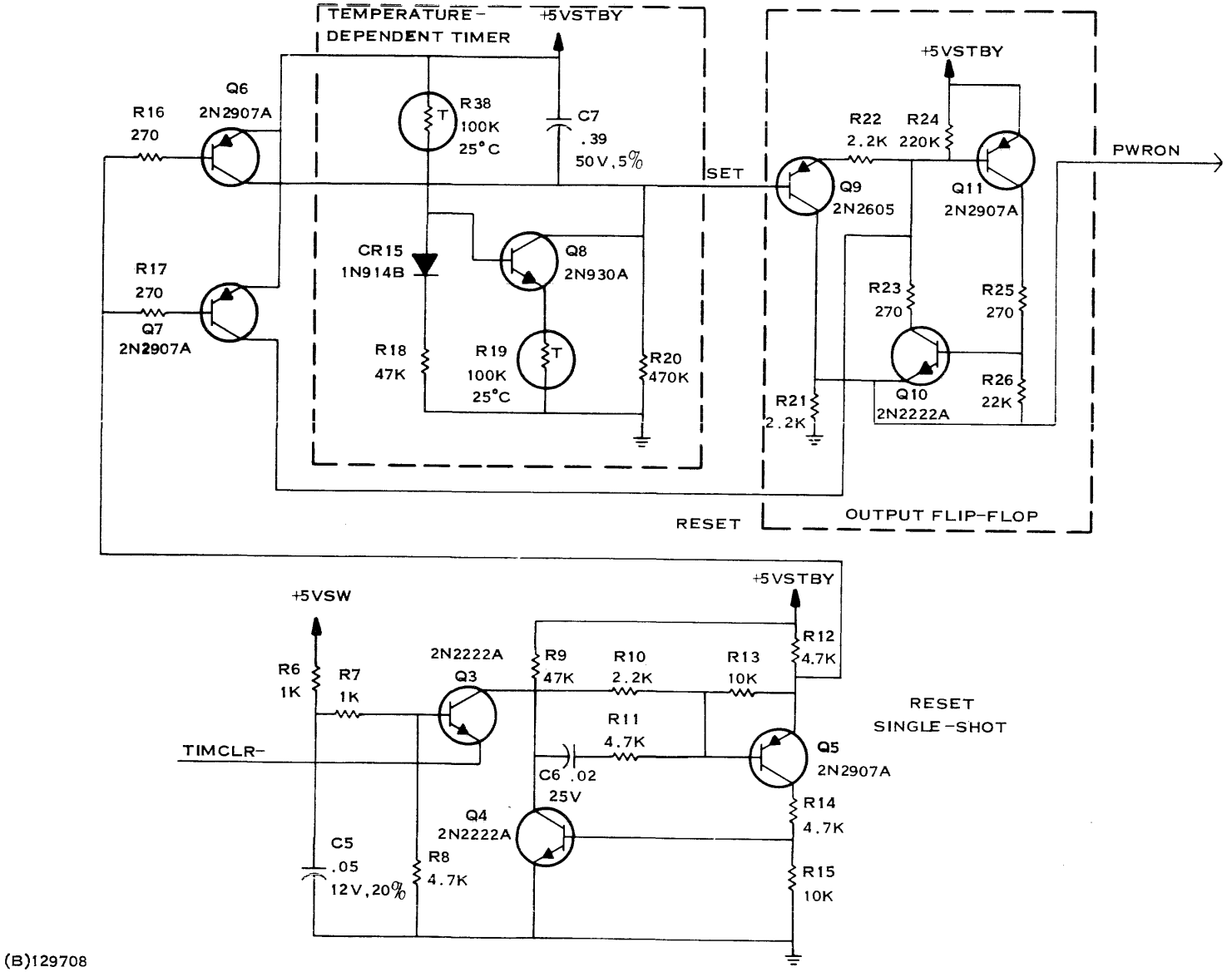


Figure 1-18. Refresh Burst Timer

Circuit Description. The Refresh Burst Timer is a monostable multivibrator circuit with the stable state producing an active PWRON signal to the memory boards. This state is the normal state during computer operation with full power. The circuit is composed of three smaller circuits: a single-shot, a temperature-dependent timer, and an output flip-flop. Transistors Q3, Q4 and Q5 and their associated circuitry form the single-shot circuit. Thermistors R38 and R19, transistor Q8 and capacitor C7 determine the time between refresh bursts. Transistors Q9, Q10 and Q11 form a latching circuit that holds PWRON high during normal operation and during refresh bursts.

Circuit Operation. When a primary power failure occurs, the battery supplies power to the output flip-flop to maintain the PWRON signal high. The Refresh Address Counter, using standby power, cycles through a refresh burst. When the burst is complete, the counter circuit generates RFBC (Refresh Burst Complete) to Reset Control, which in turn produces TIMCLR- to the timer circuit. As TIMCLR- goes low, Q3 turns on, triggering Q5 to produce a pulse approximately 0.2 milliseconds long to the bases of Q6 and Q7. Both transistors turn on, discharging the timing capacitor C7, and clearing the output flip-flop. PWRON drops, turning off all logic circuits in the memory controller and the memory circuit boards that are powered by +5VSW.

When the reset pulse from the single-shot is complete, C7 charges through resistor R20. The temperature-controlled circuit consisting of R38, R19 and Q8 provides a charging path for C7. As the temperature increases, the resistance of R38 (and R19) decreases, raising the bias on transistor Q8 to drive it further toward saturation. This variation in conductance of Q8, together with the variable resistance of R19, cause C7 to charge faster at higher temperatures than it does at lower temperatures. When C7 charges to 1.3 volts, transistor Q9 turns on to drive PWRON high. PWRON then enables +5VSW to the memory controller and memory circuits for another refresh burst. This is the stable state of the circuit. It will remain in this state until another TIMCLR- pulse clears the timer (at the end of the refresh burst during standby operation).

1.2.9.4 STANDBY POWER SWITCH. The Standby Power Switch responds to the PWRON signal from the Refresh Burst Timer to apply or remove +5 volts to the memory controller logic curcuits. The discrete component circuit that performs this function is illustrated in figure 1-19. PWRON from the timer, when high, turns on transistor Q12. This action then turns on Q13, Q15 and Q16 connecting the 5-volt source to the VCCSW output to the control circuits. In addition, turning Q12 on, turns Q15 off, allowing PWRONA to be sent to the memory circuit boards. The circuit remains on as long as PWRON is high to supply power during both normal and standby operation. When PWRON drops, Q12 turns off to remove power from the control circuits and disable the PWRONA signal to the memory circuit boards.

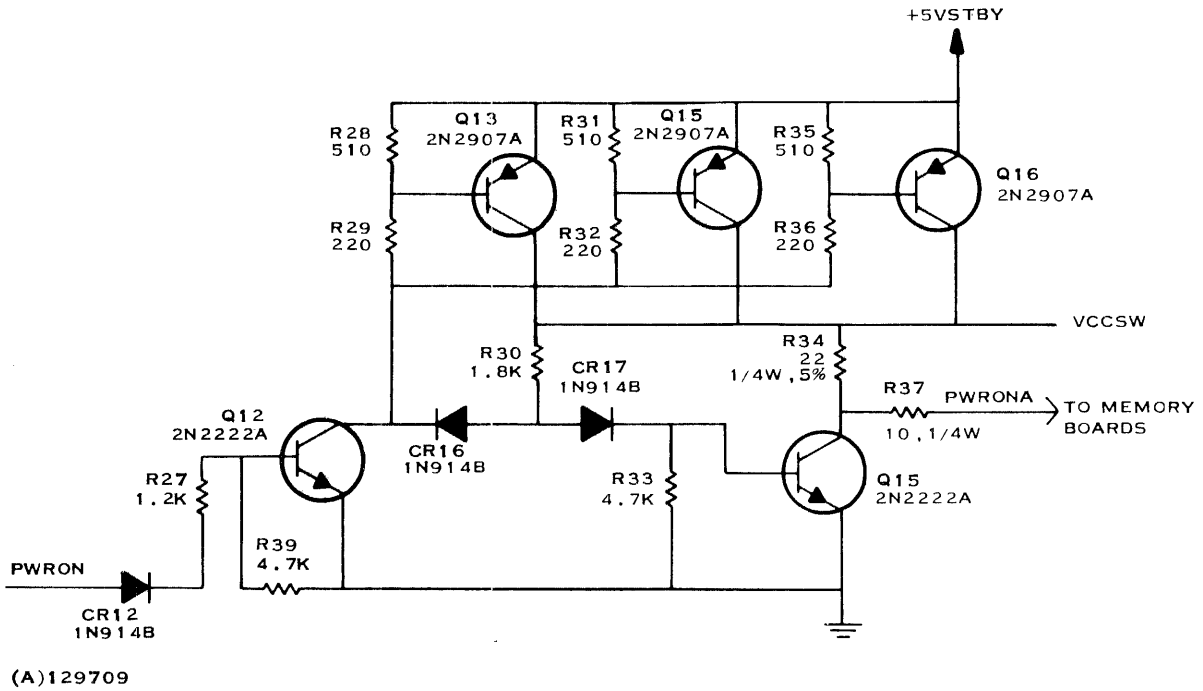


Figure 1-19. Standby Power Switch Schematic Diagram

1.2.10 RESET CONTROL

Reset Control produces two reset signals to initialize the controller logic, plus a separate reset pulse to clear the Refresh Burst Timer at the completion of a refresh burst in standby operation. Three conditions produce an initialization reset to the controller logic: a master reset from the power supply, a system reset condition, or the application of power to the controller logic through the +5V switched voltage source. Figure 1-20 illustrates the Reset Control logic circuit.

1.2.10.1 MASTER RESET. When power is out of tolerance, or a power failure is imminent, MRESET- goes low to set MRSTQ FF at the next clock. MRSTQ forces Access Control to grant refresh access and also generates a reset pulse (RESET-) that is one clock period long. The RESET- pulse initializes Memory Cycle Control to State 00 and resets the Refresh Address Counter to zero. A burst of 64 refresh cycles begins at the end of the RESET- pulse. The last refresh address signal (LSTRFAD-) from the counter signifies that the last (64th) refresh cycle of the burst is in progress. If power is again stable (MRESET- high), LSTRFAD- clears MRSTQ, and the controller enters normal operation.

However, if MRESET- is still low at the end of the last refresh cycle, RFBC (Refresh Burst Complete) from the counter sets the TIMCLR FF at the next

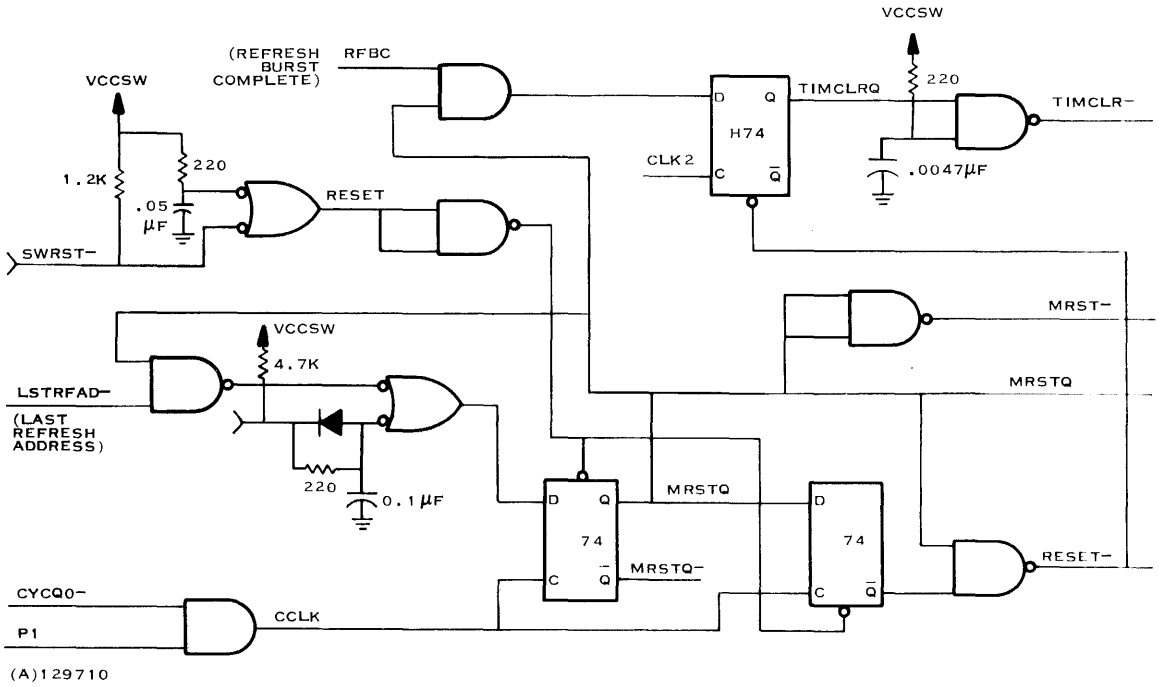


Figure 1-20. Reset Control Simplified Logic Diagram

CLK2 pulse. TIMCLR inhibits further memory cycles and clears the refresh interval timer to turn off VCCSW. When the timer times out, VCCSW is turned on. An RC delay on VCCSW sets the MRSTQ FF and forces a RESET- pulse to initiate another refresh burst. The only time the controller may enter normal operation is on the clock at the end of the last refresh cycle of a burst.

1.2.10.2 OTHER RESETS. Receipt of a test power on reset signal (SWRST-) or the initial application of power to the logic circuits through the VCCSW circuitry sets the MRSTQ FF to produce the same series of events described for Master Reset. In addition, when VCCSW initially comes on, the TIMCLR- output is inhibited to ensure that it doesn't reset the Refresh Burst Timer prematurely. The signal SWRST- is only used during factory tests.

1.2.11 CLOCK GENERATION

Two functional circuits within the controller combine to produce all of the clock pulses required by the controller plus system clock pulses for the CPU. The Clock Oscillator circuit produces a constant clock input for the Clock Counter. The Clock Counter generates three phased clock pulses with periods of 250 nonoseconds. The following paragraphs describe the operation of these circuits.

1.2.11.1 CLOCK OSCILLATOR. The Clock Oscillator is a discrete component circuit composed of a 12-MHz crystal and a TTL multivibrator circuit as illustrated in figure 1-21. The oscillator portion of the circuit is powered by a voltage source (+5STBY) that is present at all times as long as battery power holds out. This constant operation allows the control logic to have clock pulses immediately at the start of a refresh burst without the usual delay required for an oscillator to stabilize. The circuit, however, presents a low power drain on the battery. The output transistor of the oscillator circuit (Q2) is, however, powered by a switched voltage source so that the oscillator produces no output when the controller is not functioning. The oscillator circuit also provides an enable/disable gate (OSCENAB) for the output signal, and provision for an external oscillator to supply clock pulses instead of the internal circuit (EXTOSC-). These inputs are used for test and checkout purposes only.

1.2.11.2 CLOCK COUNTER. The Clock Counter receives the output from the Clock Oscillator and divides it by three to produce output signals that have a one-third duty cycle and a period of 250 nanoseconds. The circuit produces three phase-shifted clock signals: P1, CLK2 and CLK3. The circuit copies CLK3 as the system clock signal, SYSCLK-, and forwards that signal to the AU. When enabled by the CLOCK switch on the control panel, this circuit also copies CLK3 as the gated system clock signal, GCLK-,

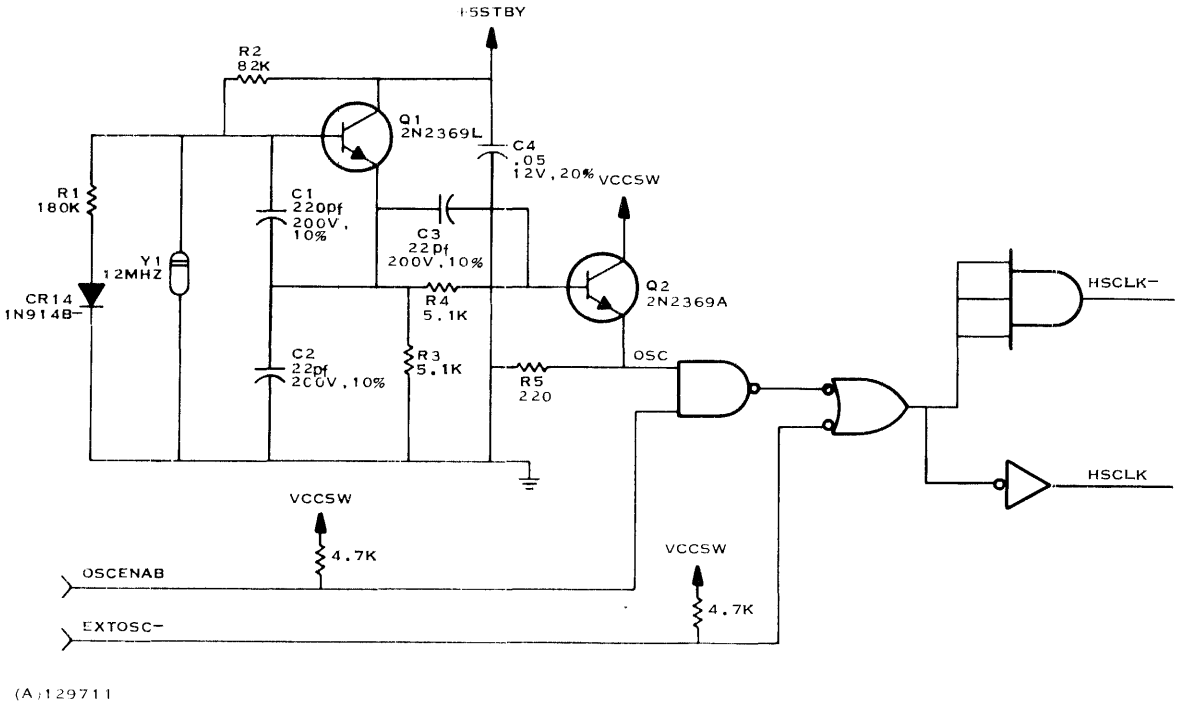


Figure 1-21. Clock Oscillator Schematic Diagram

and forwards that signal to the AU. Figure 1-22 illustrates the components of the counter circuit; figure 1-23 shows the relationship between the signals internal to the counter circuit.

Circuit Operation. The high-speed clock signal (HSCLK) from the oscillator becomes the clock input to the counter flip-flops, P1, P2, and P3. The first oscillator pulse sets P1, the second pulse clears P1 and sets P2, and the third pulse sets P3 and clears P2. The cycle begins again with the fourth oscillator pulse. The outputs of the three flip-flops become three phased clock signals that are used throughout the memory controller, P1, CLK2 and CLK3, respectively.

An input from the CLOCK switch on the computer operator panel controls the generation of the gated system clock signal, GCLK-. If the CLOCK switch is in the ON position, STPCK- will be high. This signal gates the output of the P3 FF to become the gated system clock signal. If the CLOCK switch is in the OFF position, STPCK- disables GCLK-.

1.3 MEMORY CIRCUIT BOARD

The memory circuit board contains either two banks (8K memory), four banks (16K memory) or six banks (24K memory) of Metal Oxide Semiconductor (MOS) memory circuits. Each bank of memory chips represents storage capability for 4096 22-bit words (16 data bits, 6 error correcting bits). In addition, the circuit board contains all the logic circuits necessary to access a particular location within the memory banks at the direction of the memory controller circuit board. These functions include address decoding and generation of chip enable and chip select signals from the control signals supplied by the memory controller. Figure 1-24 illustrates the relationship of the main component circuits within the memory circuit board. The following paragraphs describe the function and operation of these component circuits.

1.3.1 MEMORY SIZE JUMPERS

When the memory circuit board is constructed, jumper wires are connected between points E5-E6, E7-E8, or E9-E10 as required to produce a memory size code that describes the storage capability of the board. The code is a complement code created by grounding those signals connected by jumper wires. The following jumper wire configurations produce valid memory size codes:

E5-E6	E7-E8	E9-E10	
NO	YES	NO	8K Memory
YES	NO	NO	16K Memory
YES	YES	NO	24K Memory

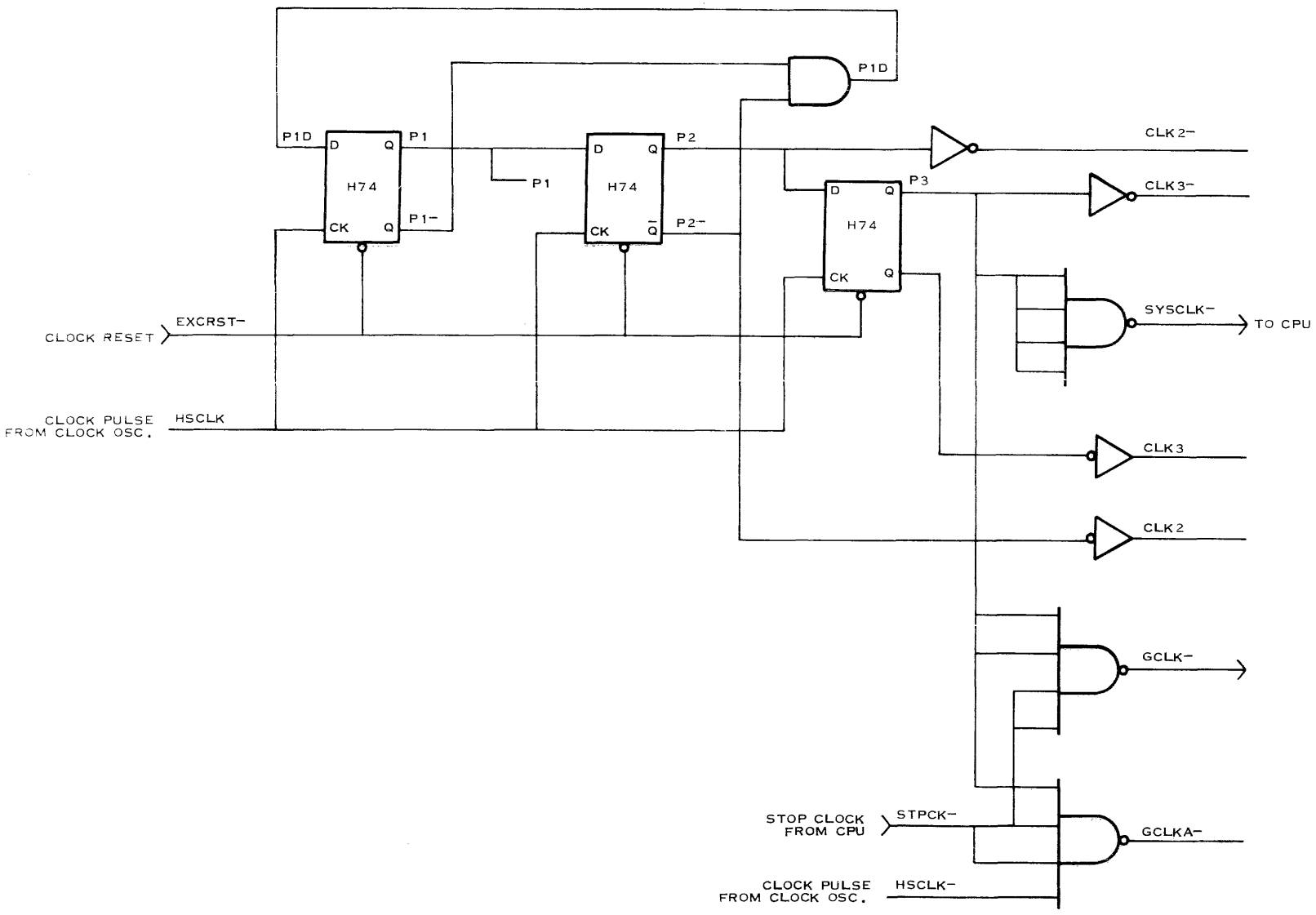


Figure 1-22. Clock Counter Circuit Simplified Logic Diagram

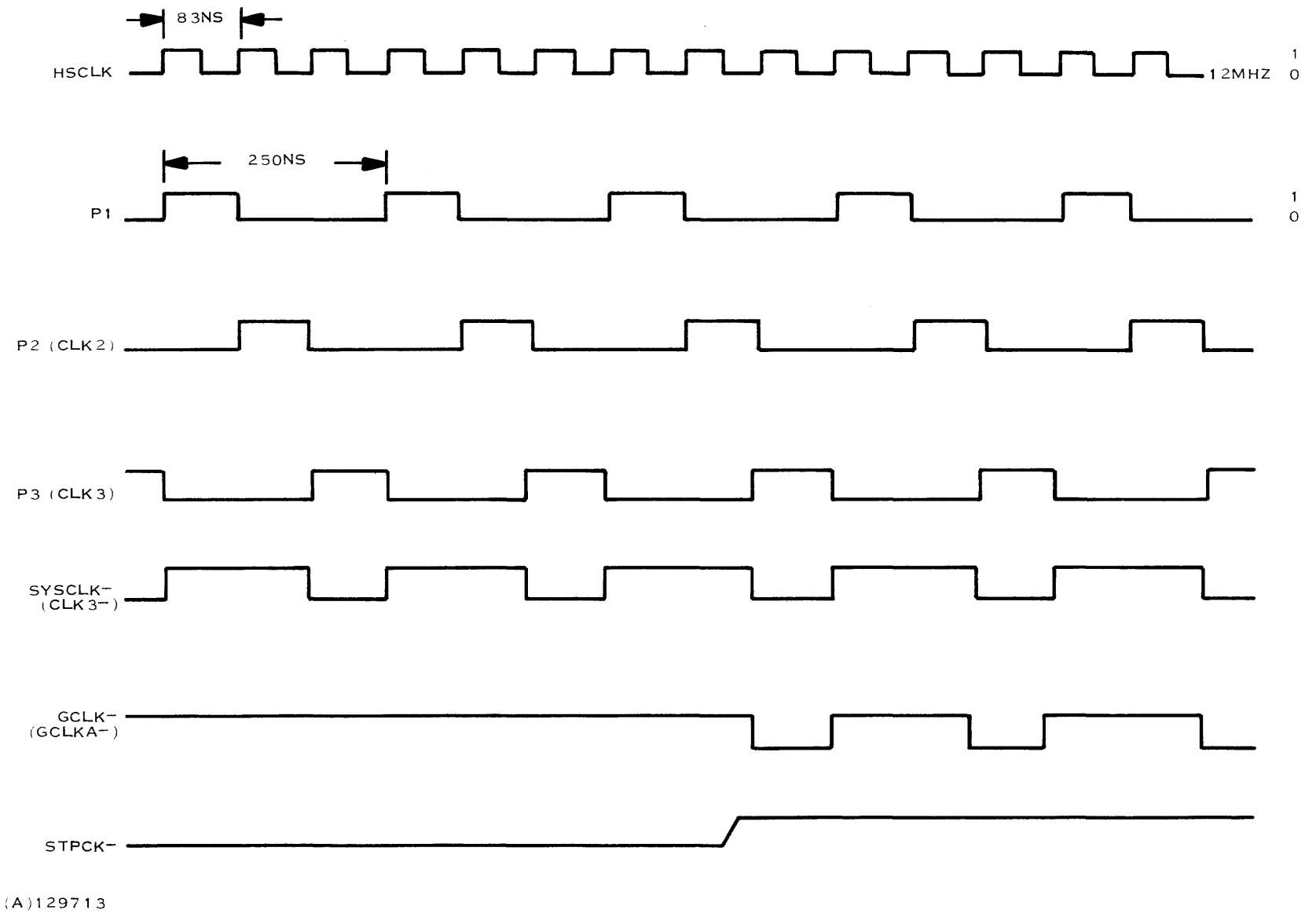


Figure 1-23. Clock Counter Circuit Timing Diagram

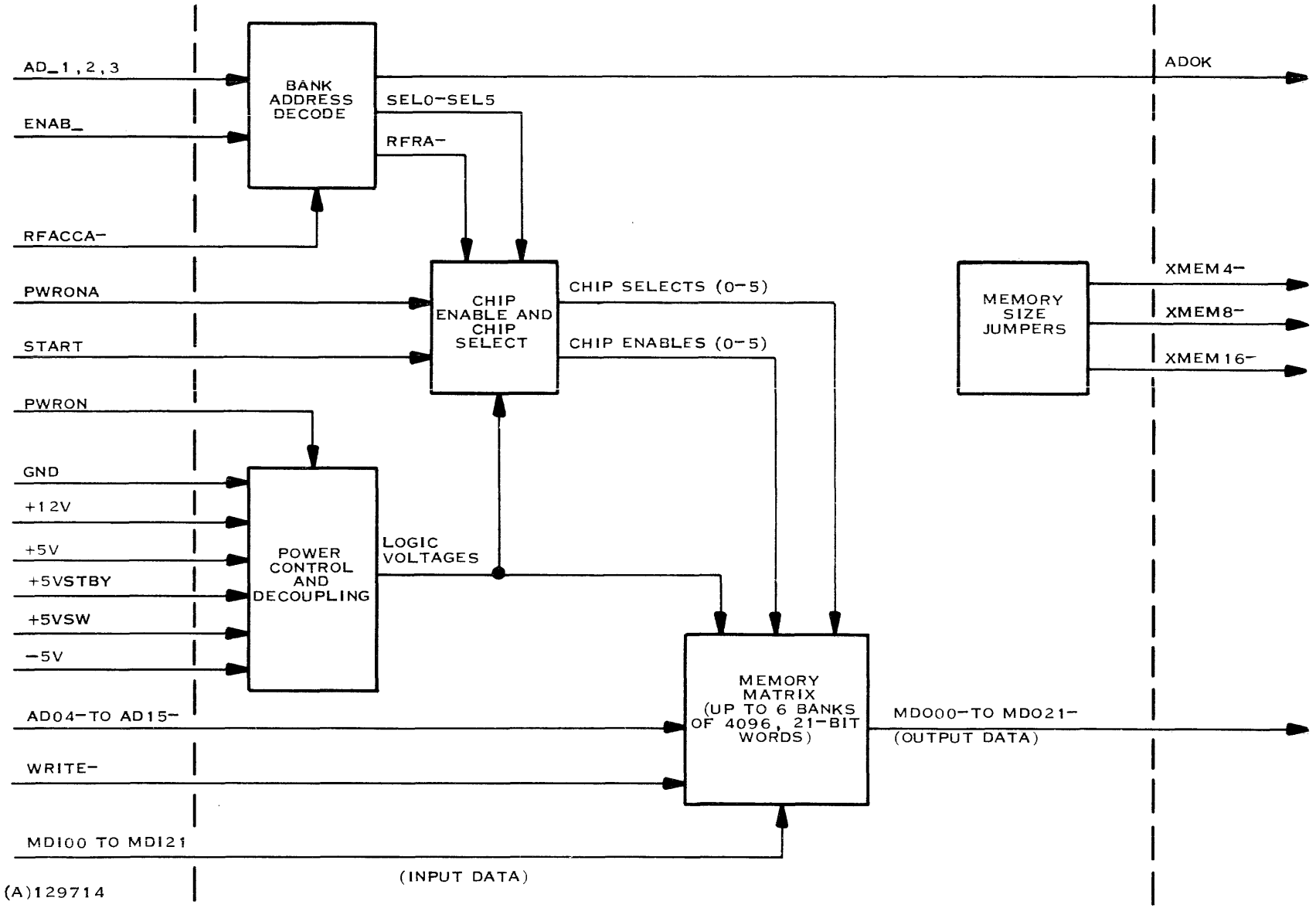


Figure 1-24. Memory Board Block Diagram

1.3.2 POWER CONTROL AND DECOUPLING

The memory board contains decoupling capacitors for all logic voltages that it receives, plus a 1-transistor circuit to produce -3 Vdc from a -5 Vdc input, and a +5 Vdc switching circuit that is activated by PWRON from the memory controller. This switching circuit removes power from the control logic during power-off conditions except during refresh bursts.

1.3.3 BANK ADDRESS DECODE

Bank Address Decode receives the bank address from the memory controller, decodes that address to generate a memory cycle enable signal to the selected memory bank, and returns an address valid indication (ADOK-) to the memory controller if the memory board contains the proper number of banks to recognize that address. A bank address of 6 or 7 is invalid for all memory boards and will not produce an ADOK- signal. Similarly, an address of 4 or 5 is illegal for 16K and 8K memory boards, and an address of 2 or 3 is illegal for 8K memory boards. Figure 1-25 illustrates the Bank Address Decode Circuit.

If the board is selected by DECENB from the memory controller, an integrated circuit binary decoder receives the 3-bit bank select code from the memory controller and produces a low-level output corresponding to the decimal value of the code. This output produces a bank select signal that is sent to the chip enable pulse shaping circuit corresponding to the selected bank. In addition, all valid output pins from the decoder are wire-ANDed together. If any of the valid outputs goes low (active), a low-active address valid indication (ADOK-) is sent to the memory controller.

During refresh cycles a bank select signal is generated for all banks on the memory board. This feature enables all chips on the board to receive the refresh address and perform a refresh cycle at the same time. The refresh access signal also disables chip select so that the data inputs and outputs to the memory chips are disabled during refresh cycles to prevent storing of extraneous information. Each refresh address services 1/64 of the memory locations, or 64 bits in each memory chip.

1.3.4 CHIP ENABLE PULSE SHAPER

The chip enable pulse shaper circuit is a transistor circuit that ensures fast rise and fall times for the chip enable clock pulse with enough driving capability to supply the chip enable to an entire bank of memory chips. Figure 1-26 illustrates the circuit that is duplicated six times on the fully implemented memory board, once for each bank of memory chips.

If enabled by the SELn signal from the bank address decode circuit, the pulse shaper responds to the START pulse from the memory controller. When START is low (inactive), the circuit is at rest. Transistor Q4 is off; transistor Q5 is on to provide a low-level output to the chip enable input of the memory chips in its associated memory bank. When START goes high,

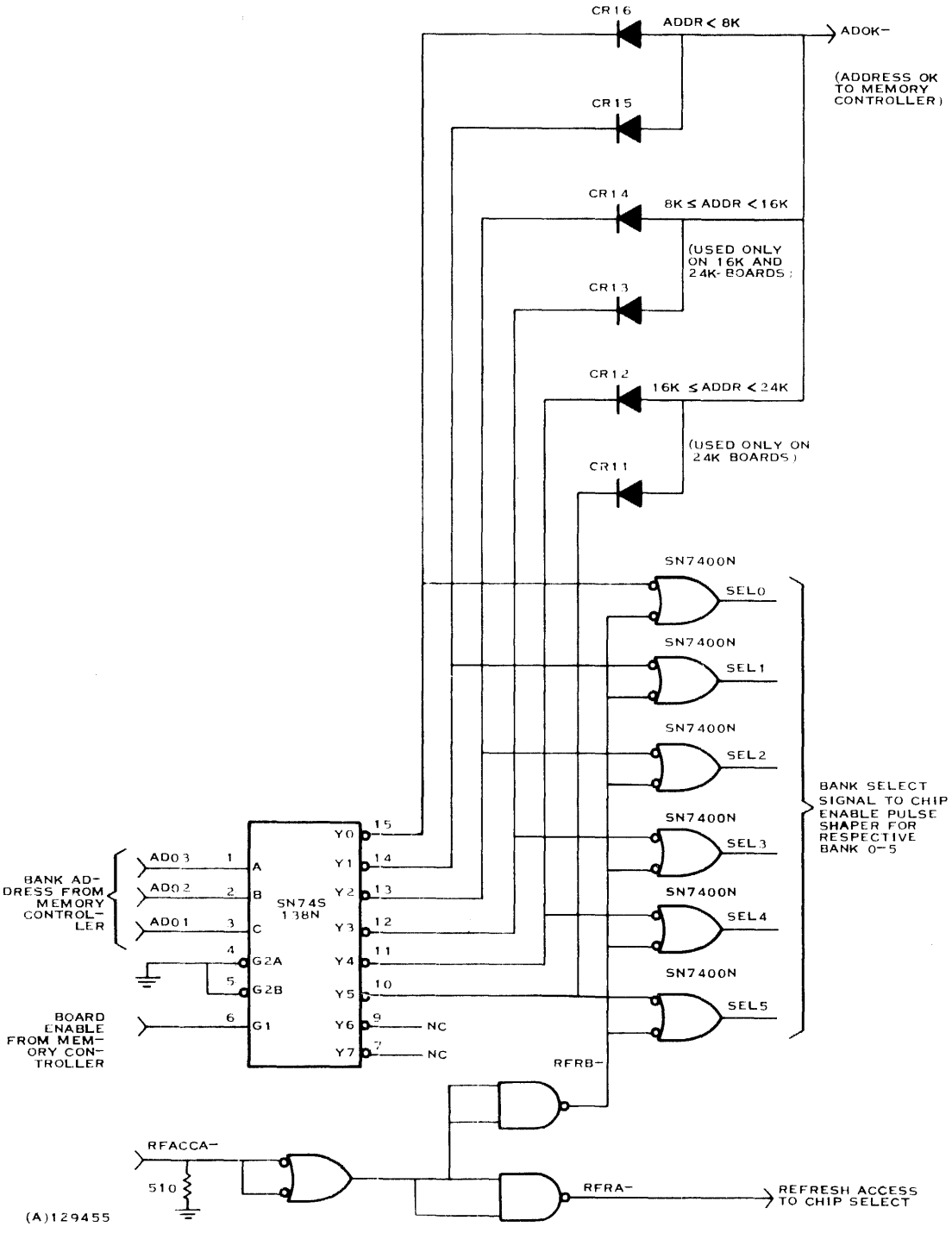


Figure 1-25. Bank Address Decode Circuit

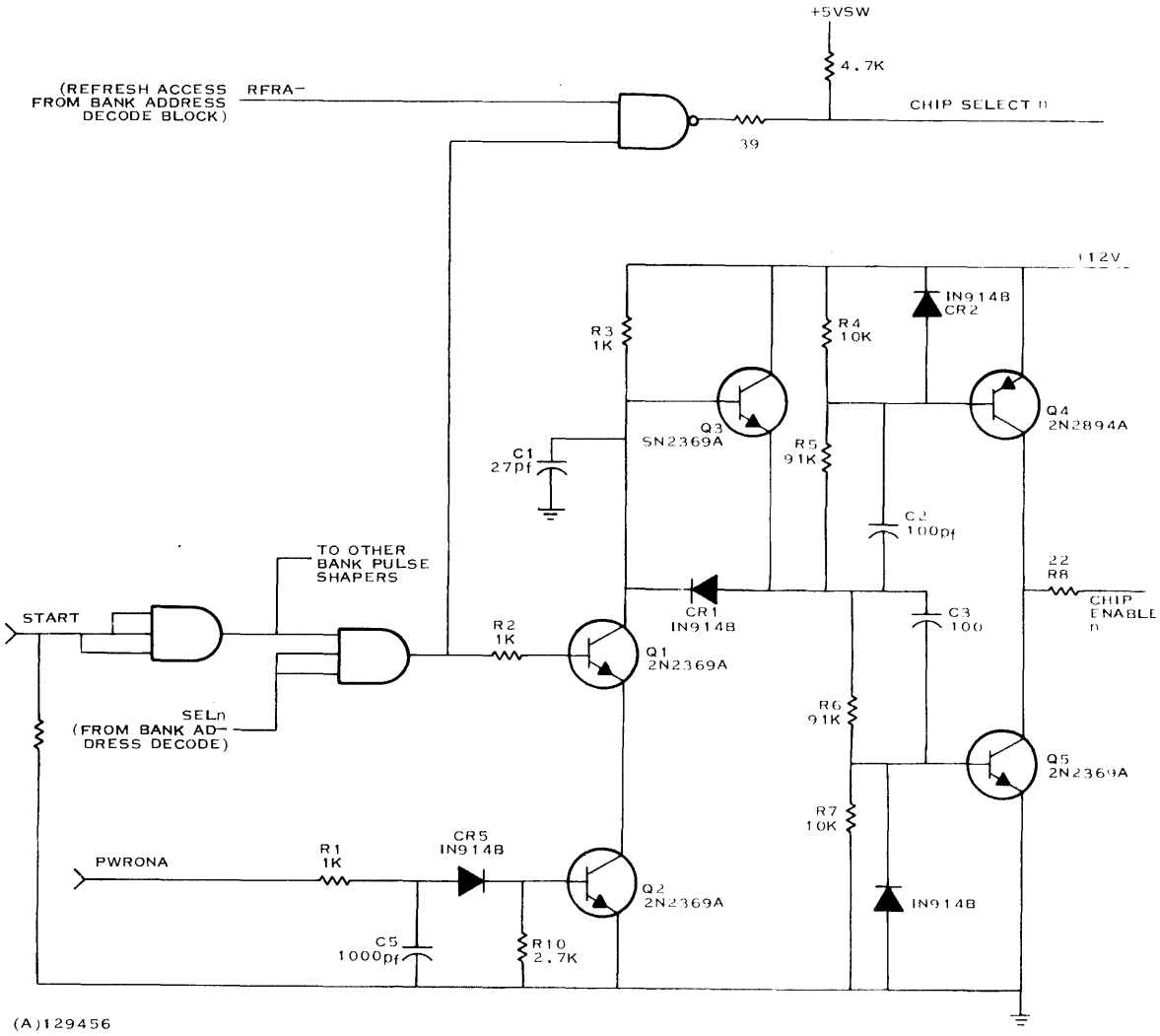


Figure 1-26. Chip Enable Pulse Shaper-Divider

transistor Q1 turns on. This action reduces the voltage on the bases of transistors Q4 and Q5 so that Q5 turns off and Q4 conducts the 12-volt supply for output to the chip enable inputs of the memory chips. When START returns to the inactive state, Q1 turns off. Transistor Q3 turns on, bypassing resistor R3 to turn on Q5 more quickly. The chip enable output drops as Q5 turns on and Q4 turns off. The circuit awaits another START pulse. Transistor Q2 and the PWRONA input disable the chip enable circuit during power transitions. During normal operation conditions, PWRONA is high and Q2 is on to enable operation of Q1.

1.3.5 CHIP SELECT

The chip select signal during normal memory accesses follows the START pulse from the memory controller. During refresh cycles, chip select is disabled.

1.3.6 MEMORY MATRIX

The memory chips are arranged in a matrix that contains 2, 4 or 6 banks (depending upon whether the board has 8K, 16K or 24K words of memory, respectively) of 22 memory chips. A particular memory cycle accesses one bit from each of the memory chips in a single bank to produce an operation on one 22-bit word. Figure 1-27 illustrates the arrangement of the chips in the matrix and the routing of the data and control lines to the chips in each bank.

1.3.6.1 MEMORY WRITE. During a memory write operation, the incoming WRITE- signal line is low. This signal is buffered and applied to all memory chips on the circuit board. Similarly, the incoming address from the memory controller is supplied to all chips on the board, after passing through individual drivers for each bank of memory chips. Incoming data on the MDI__ lines is also distributed to all chips on the memory board. Bit 0 becomes the data input to chip 0 in all six banks on the memory board; bit 21 becomes the data input to chip 21 in all six banks on the memory board. The chip select and chip enable signals, derived from the Bank Address Decode circuit, determine which of the six banks will receive the write data. When the chip enable signal goes high, the data on the MDIxx lines is stored in the location specified by the address lines in the bank corresponding to the active chip enable signal.

1.3.6.2 MEMORY READ. During a memory read operation, the incoming WRITE- signal line is high. Distribution of input signals is the same as for the write operation, except that no valid data is present on the MDIxx lines. Instead, the selected memory chips produce a data output. The data outputs from all chips in a specific bit position are wired-OR'ed together, so that an output from any bank of chips appears on the MDOxx- lines. For example, the outputs from chip 0 in all six banks are wired together. Data output from any of the position 0 chips will be transmitted as data on the MDO00- line. Data output from the chips is enabled by the chip select.

1.3.6.3 MEMORY CHIP. The heart of the memory system is an integrated circuit package containing 4096 single bits of storage (4096 x 1 matrix). The integrated circuit is a dynamic, random access memory circuit packaged in a 22-pin dual-inline-package. Each package has a single data input, a single data output, and 12 address inputs to select one of the 4096 storage locations within the package. In addition, a chip select input enables the data in, data

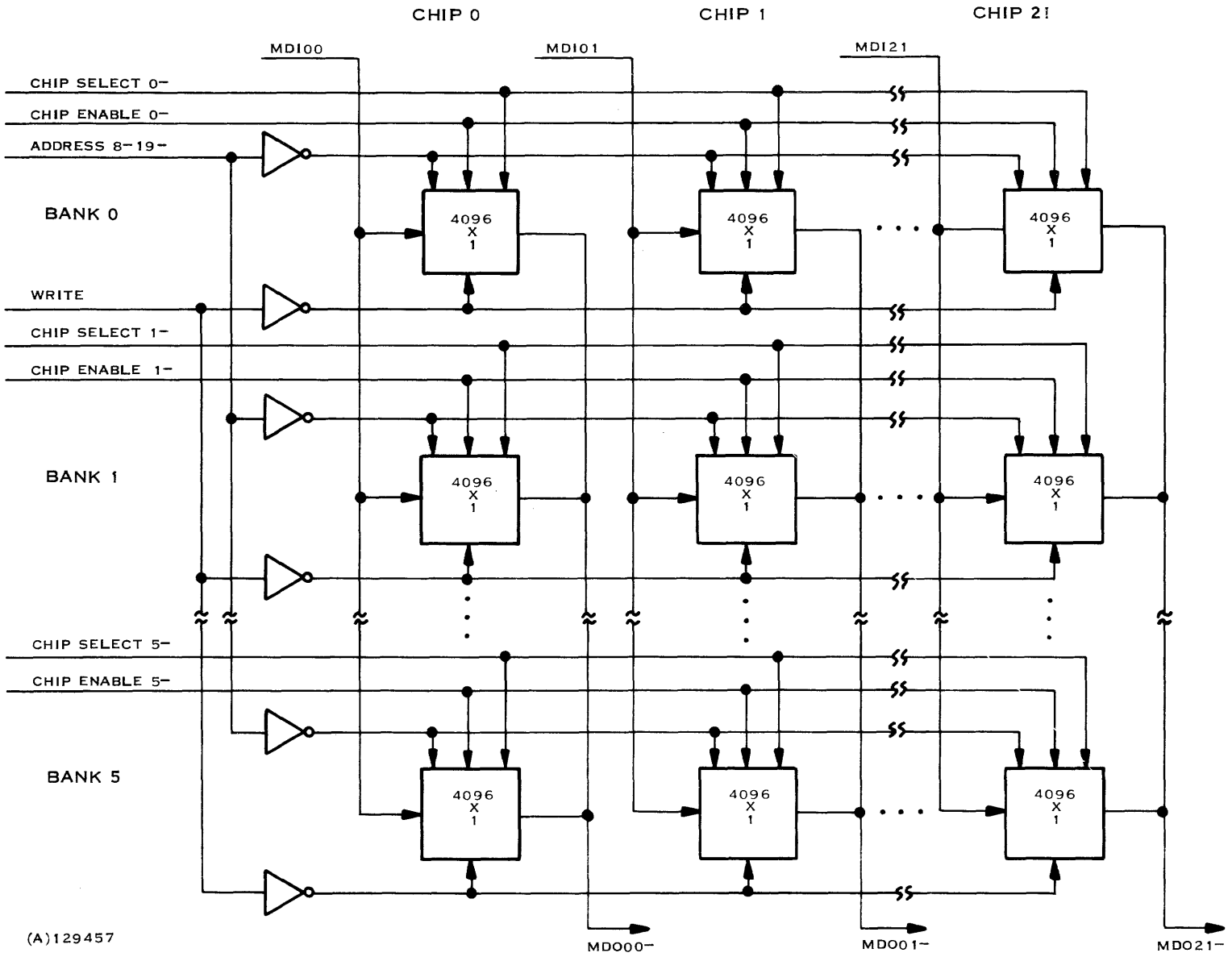
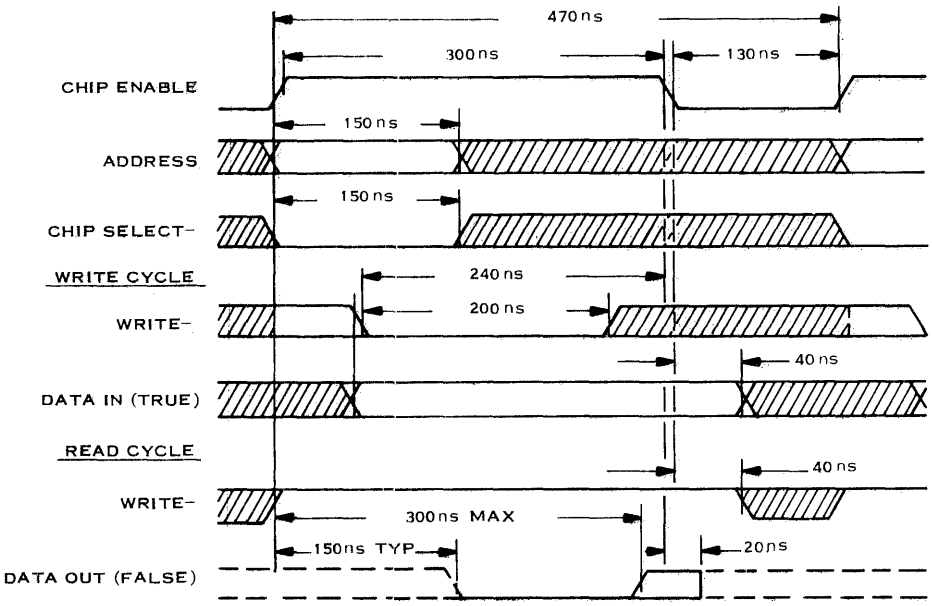


Figure 1-27. Memory Matrix Addressing and Data Paths

out and read/write terminals of the chip, and a chip enable (clock) pulse input allows the chip to perform a memory cycle (either a read or a write). The state of a read/write input line to the chip determines which type of memory cycle will be performed. Figure 1-28 illustrates the optimum timing for a read and write cycle within the chip. Worst-case time for either a read or a write cycle is 470 nanoseconds. Input data to the chip is inverted when it is read from the chip.



NOTES: 1. INPUT TIMING: CHIP ENABLE MEASURED AT 10% AND 90%: ALL OTHER INPUTS EITHER 0.6V(LOW) AND 2.2V(HIGH)
2. OUTPUT TIMING: MEASURED AT 0.4V(LOW) AND 2.4V(HIGH)

(A)129458

Figure 1-28. Memory Chip Optimum Timing Diagram

SECTION II

DIRECT MEMORY ACCESS CHANNEL INTERFACE

2.1 GENERAL

The DMAC interface consists of a single, three layer, printed circuit board that performs the following functions:

1. Provides a memory address register for Direct Memory Access Port (DMAP) access to memory.
2. Provides a write data register for DMAP data transfer to memory.
3. Buffers read data from memory to the DMAP.
4. Buffers all control signals between the CPU or Memory Controller and DMAP.

2.2 THEORY OF OPERATION

The DMAC interface acts primarily as a cable driver and receiver for handling signals between the Memory Controller and the DMAP. The DMAP and related DMAP signal requirements are described in DMAP Expander Maintenance Manual, TI Part Number 216759-9701. The following discussion references the electrical schematic drawing of the DMAC circuit board, TI Drawing Number 966392. This drawing may be found in the Model 960/980 Computers, Direct Memory Access Channel Manual, TI Part Number 966312-9701. Theory of operation for each interface function is included in a subsequent subparagraph. Figure 2-1 shows the timing relationships of the major interface signals.

2.2.1 MEMORY ADDRESS REGISTER

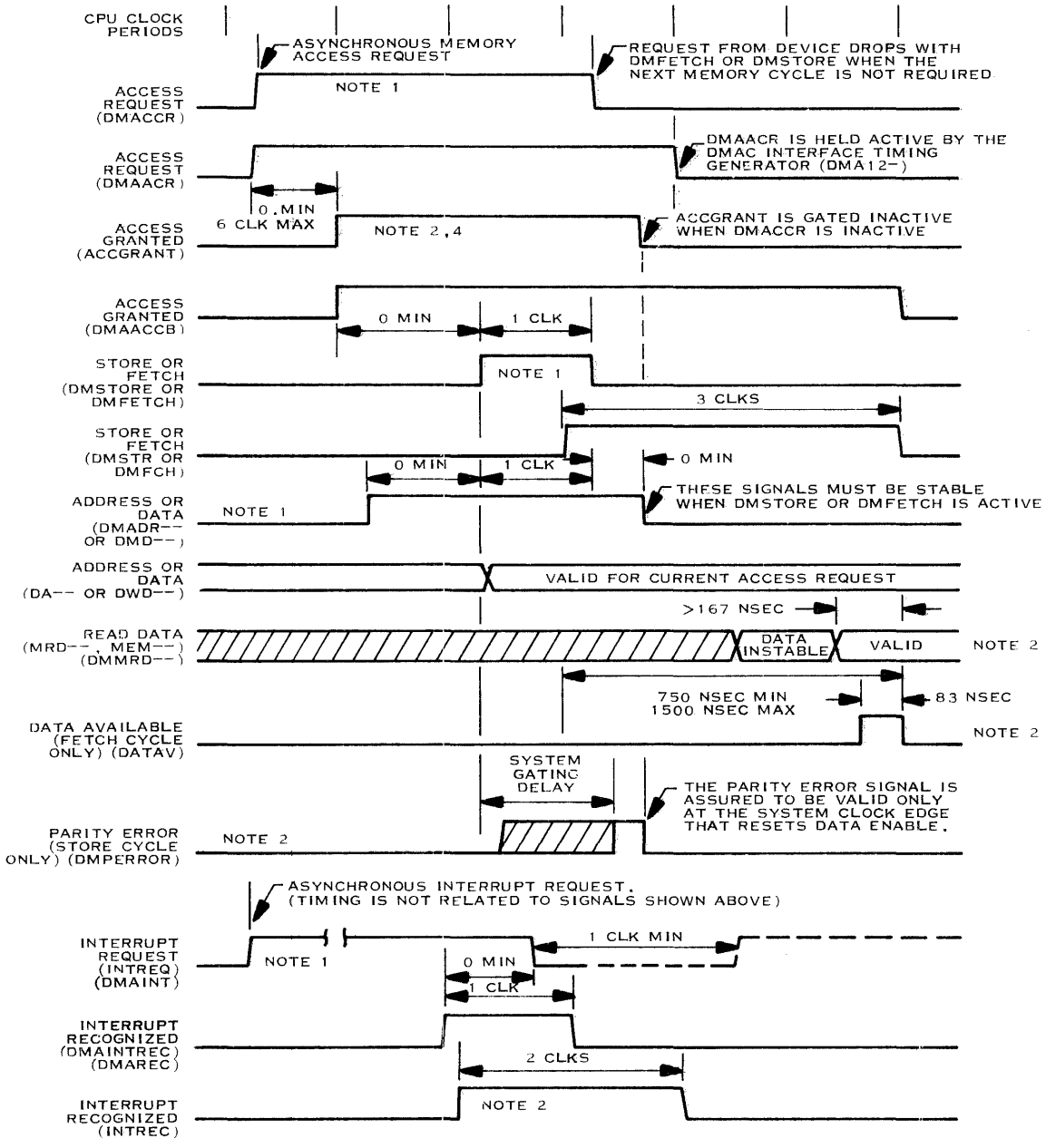
Since memory addresses (DMADR) that are presented by the DMAP to the memory controller may not be used immediately, these addresses are retained in a register (DA--) which is loaded when the DMAP requests a memory cycle (DMFETCH + DMSTORE).

2.2.2 WRITE DATA REGISTER

Similarly, data (DMD--) being written by the DMAP into memory is retained in a register (DWD--) that is loaded when the DMAP requests a memory store cycle (DMSTORE).

2.2.3 READ DATA BUFFERS

Read data from the memory controller (MRD--) to the DMAP (DMMRD--) is buffered by a set of non-inverting gates. The signature of read data on the 980B backpanel is MEM--.



NOTES:
1. FROM DEVICE CONTROLLER.
2. TO DEVICE CONTROLLER

} OTHER SIGNALS SHOWN ABOVE INTERFACE WITH THE 980 MEMORY CONTROL AND AU LOGIC.

3. SIGNALS ARE SHOWN IN THE TRUE SENSE.
4. ACCGRANT MAY DROP DURING REFRESH MEMORY CYCLES.
5. SYSTEM CLOCK (CK3D1) IS 4-MHZ. CK3D1 IS INHIBITED DURING MEMORY REFRESH CYCLES.
6. THE DEVICE CONTROLLER TIMING SHOWN ABOVE IS GENERALIZED. SEE BITC OR DEVICE CONTROLLER DOCUMENTATION FOR MORE DETAIL.

(A)132841

Figure 2-1. DMAC Interface Controller (966390) Timing (980B)

2.2.4 SYSTEM CLOCK

CK3D1 - is the system clock to the DMAP. CLK3D1- is generated by gating CK3C1 and RFRACCB- to prevent clock transitions during memory refresh cycles. CK3C1 is generated by inverting CLK3A1-. CLK3A1- is called IOCLK- on the 980B backpanel. The source for IOCLK- is on a CPU logic board (AUI). The source for RFRACCB- is on the Memory Controller.

2.2.5 ATI STORBES

An ATI storbe indicates that an ATI command is valid on the MRD-- data lines. ROM44 and ROM45 are gated with MRESET- and CKC31 to produce ATISTB1- and ATISTB2- respectively. ROM44 and ROM45 are called ENATI1 and ENATI2 respectively on the 980B backpanel. Their source is on a CPU logic board (AUI). The strobes sent to the DMAP are 83 nanoseconds wide (low active) and MRD-- data lines are valid for at least 83 nanoseconds before and after these strobes.

2.2.6 INTERRUPT RECOGNIZED

The signal to the DMAP that designates an interrupt has been recognized is INTREC-. This signal is a buffered flip-flop output. INTREC is preset by DMAINTREC from the CPU (AUI) and is reset by CK3A1- after the CPU removes the DMAINTREC signal. DMAINTREC is called DMAREC on the 980B backpanel.

2.2.7 ACCESS GRANTED

The ACCGRANT - signal indicates that memory access has been granted to the DMAP. This signal is the inverse of DMAACCB from the Memory Controller and is gated with memory access request (DMACCRA) from the DMAP. The Memory Controller responds with the DMAACCB signal after it receives an access request (DMAACR-).

2.2.8 PARITY ERROR

The DMPERROR- signal indicates that the parity of write data DWD-- stored on the DMAC interface differs from the DWD parity bit (DWD16) stored on the DMAC interface. This is the exclusive OR function of WDPB generated on the DMAC interface and DWD16.

The DMMRD16 signal is read data parity and is odd when no memory error is present in read data.

2.2.9 MASTER RESET

The DMRESET- signal is the buffered CPU signal MSTRST-. The MRESET- signal is supplied from the power supply and is sent directly to the DMAP. MRESET- is also used on the DMAC interface to inhibit ATI storbes when power fails.

2.2.10 MEMORY CYCLE TIMING

The two flop-flops located zone D5 (Z18) time the read data available pulse (DATAV-) which is sent to the DMAP and time the store and fetch pulses (DMSTR-, DMFCH-) which are sent to the Memory Controller.

2.2.11 FETCH AND STORE

The DMFETCH- and DMSTORE- signals are supplied from the DMAP. These signals set either DMSTR or DMFCH latch outputs that are then enabled by DMCRENAB and DMAACCB to become the DMSTR- or DMFCH- signals which are supplied to the Memory Controller. Fetch and store signals may be sent by DMAP to the DMAC interface only when ACCGRANT- is active.

2.2.12 ACCESS REQUEST

The DMAACR- signal is the DMAP access request (DMACCR-) that is enabled by MSTRST-. DMAACR- is also held active by DMSTRFCH or the signal DMA12- from the timing generator.

2.2.13 OPTION SELECT

Terminal posts E1, E2, E3 located in zone D4, must be wired properly for use in the 980B Computer. P1-13 must be wired to ground by wiring terminal E1 to terminal E3. The flip-flop (Z1) connected to E2 is not used by the 980B Computer.

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.

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- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.

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  Tx-yy

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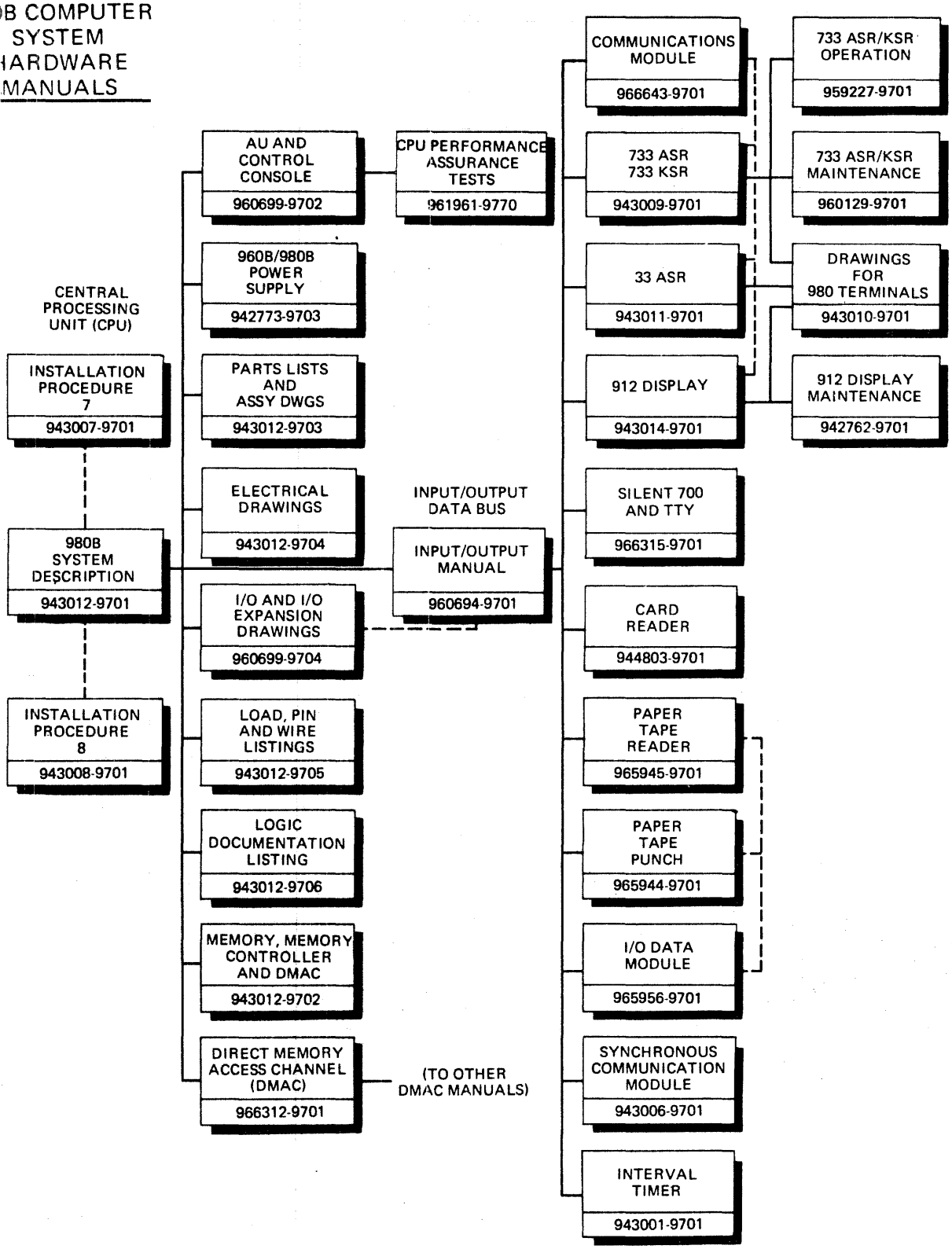

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