TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 980B Computer
Maintenance Manual
System Description

Digital Systems Division

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SECTION I

INTRODUCTION

The Texas Instruments Model 980B System Manual provides the reader with an overview of the complete computer system. This manual is the first of four hardware manuals which are supplied to the customer with each computer. The second manual of this four manual series is entitled Input/Output Manual For The Model 980 Computer (TI Part No. 960694-9701). This Input/Output Manual describes the I/O bus system of the Model 980. The third and fourth manuals of this series describe the Direct Memory Access Channel (DMAC) of the Model 980. These manuals are entitled Direct Memory Access Channel Manual For The Model 960/980 Computer (TI Part No. 966312-9701) and Direct Memory Access Channel Controller Manual For The Model 960/980 Computer (TI Part No. 966312-9702). The first manual provides a functional description of the DMAC system with information concerning possible expansion configurations, interface cards, and general timing. The second manual provides general information concerning command structure, device specifications, and installation.

Additional manuals are supplied with the Model 980B Computer System. These manuals describe computer programming, document the software packages, and describe the peripherals for use with the Model 980B System. The Model 980B manual set is designed to provide the user with sufficient information to assemble, install, and operate the Model 980B Computer System.

SECTION II

SYSTEM DESCRIPTION

The Texas Instruments Model 980B Computer (figure 2-1) is an advanced design of the Texas Instruments Model 980A Computer. The Model 980B is a general purpose computer which features outstanding performance and low cost. Medium and large scale TTL-integrated circuits are used with an MOS-semiconductor memory to provide the highest reliability and performance.

Large multilayer printed circuit boards and packaging simplicity provides excellent serviceability. Some of the Model 980B system applications include:

- Real-time process control
- Scientific data processing
- Communications systems

A variety of Model 980B input/output options are available to provide an extremely flexible computer system. To satisfy the requirements of a variety of specialized applications, a complete software package is available.
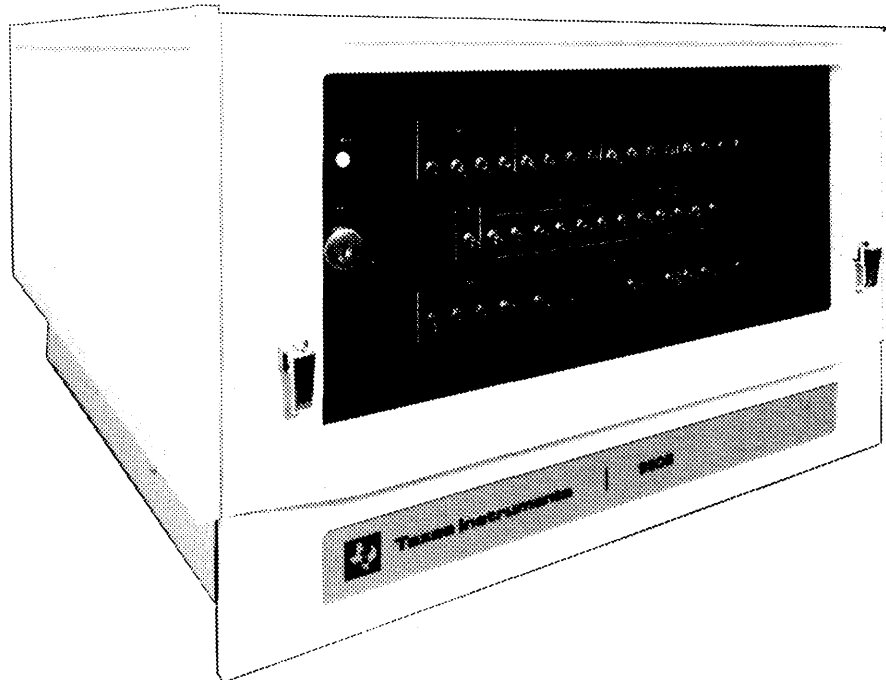
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Figure 2-1. Texas Instruments Model 980B Exterior View

2.1 SYSTEM FUNCTIONAL ORGANIZATION

A functional diagram of the Model 980B Computer System is illustrated in figure 2-2. Each major function of this system is described in separate paragraphs which follow.

2.1.1 SEMICONDUCTOR MEMORY

The standard semiconductor (MOS) memory of the Model 980B has a storage capacity ranging from 8,192 to 65,536 words. Space is provided within the Model 980B chassis for the maximum configuration (65,536 words of directly addressable error-correcting memory). An optional battery system protects memory against accidental power loss.

2.1.2 CENTRAL PROCESSING UNIT

The Central Processing Unit (CPU) can address the memory, perform arithmetic and logic functions, and sequence and control the exchange of information between memory and other computer elements. The CPU features an instruction set of 98 basic instructions, 16-bit word length operations, 8 addressable hardware registers, a 4-level priority interrupt structure and an arithmetic unit with a ROM controller.

2.1.3 DIRECT MEMORY ACCESS CHANNEL

The Direct Memory Access Channel (DMAC) is the interface between the computer and high-speed automatic computer peripherals, such as: disc
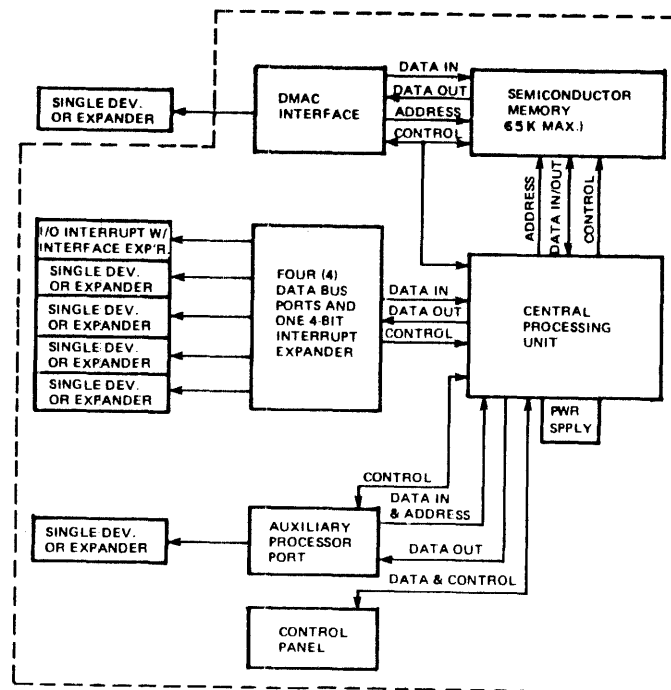
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Figure 2-2. Model 980B Computer System Functional Diagram

storage units, line printers, and magnetic tape units. By using a separate controller for each device, concurrent operation of high-speed peripherals is achieved.

2.1.4 INPUT OUTPUT BUS

The Input/Output Bus (I/O Bus) is a 16-bit parallel bus controlled by the CPU to allow programmed data transfers between the CPU and medium speed peripheral devices such as a teletype or card reader.

2.1.5 AUXILIARY PROCESSOR PORT

The Auxiliary Processor Port (APP) allows auxiliary devices to be used with the Model 980B to implement additional operations.

2.2 SYSTEM PERFORMANCE SPECIFICATIONS

Model 980B system performance specifications are identified and listed in table 2-1.

Table 2-1. Model 980B System Performance Specifications

Characteristic	Specification
Organization	16-bit word length Two's-complement arithmetic 8 addressable registers Single-level indirect addressing Implementation - TTL series 74, and LSI Integrated Circuits Bipolar ROM control for CPU

Performance	4-mHz System Clock
	750-nanosec memory read cycle
	750-nanosec memory write cycle
	500-nanosec memory access
	Execution times (Program Counter relative):
	    Add 1.75 microseconds
	    Multiply 6.25 microseconds
	    Divide 7.75 microseconds

Memory	Dynamic MOS/LSI semiconductor array memory 750-nanosec read cycle 750-nanosec write cycle Internal storage for a maximum of 65,536 words in 8,192 word increments Power failure protector/Auto Restart Switch initiated ROM Bootstrap Loader

Table 2-1. Model 980B System Performance Specifications (Continued)

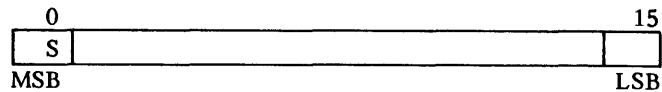| Characteristic	Specification
Input/Output	One direct memory access channel (expandable to 8) Burst rate, 1 million words per second at DMA port One processor-controlled I/O bus with 4 ports (expandable to 256 ports)
Instruction Set (98 basic instructions)	24 Memory referencing instructions 13 Register-to-register instructions 22 Single and double register shift instructions 20 "Skip if Test True" instructions 1 Idle instruction 2 I/O bus Read/Write direct instructions 2 Byte string manipulation instructions (move and compare) 4 Test bit and skip if equal instructions 2 Status block manipulating instructions 4 Set bit instructions 2 Register file manipulating (load/store) instructions 1 Direct memory access channel instruction 1 Auxiliary processor initiate (API) instruction
Other Features	Memory protect/privileged instruction feature (standard) Memory Error Correction Expanded interrupt option (to 64 priority interrupts - optional) Auxiliary processor option (optional) Internal expansion chassis for DMAC, I/O and auxiliary processors (optional) Internal battery for maintaining memory contents when power is off (optional) Automatic power fail-restart (standard)

2.3 SYSTEM DATA PROCESSING

This paragraph describes Model 980B acceptance, processing, and storage of data. Since the Model 980B is available in numerous configurations, the subparagraphs which follow briefly describes the handling capability of available Model 980B equipment configurations.
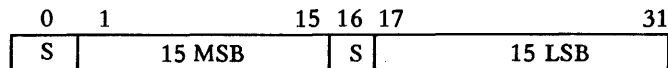
2.3.1 DATA AND INSTRUCTION FORMATS

Model 980B data and instruction words are both 16 bits in length. Bit positions within a word are numbered 0 through 15 from left to right as indicated:

```
0                                                    15
┌─┬─────────────────────────────────────────────┬──┐
│S│                                             │  │
└─┴─────────────────────────────────────────────┴──┘
MSB                                              LSB
```

Data is represented in binary two's-complement form with bit 0 indicating the algebraic sign(s). A logic zero in the first bit position indicates a positive sign. The range of integers representable in one 16-bit word is from -2^{15} to $+2^{15}-1$.

Double length operands (products from multiplication, dividends for divides, and quantities for double-length arithmetic shifts) have the following format:

```
0   1              15  16 17                    31
┌─┬────────────────┬─┬────────────────────────┐
│S│    15 MSB      │S│        15 LSB          │
└─┴────────────────┴─┴────────────────────────┘
```

Input, output, and status register related instructions are 32 bits long and occupy two consecutive 16-bit words. The register-to-memory instructions may be 16, 32, or 48 bits long.

2.3.2 MEMORY

The basic unit of memory is a 16-bit word plus 6 check bits for error correction. Semiconductor (MOS) memory is standard for the 980B. Three modules of up to 24,576 words each can be plugged into the CPU enclosure giving the 980B an internal storage capacity of 65,536 words. (See figure 2-3.) The CPU can directly address all 65,536 words of memory.

An internal battery in the Model 980B is provided to maintain the contents of the semiconductor memory in the event main power is interrupted. Use of the battery permits the contents of the memory to be preserved for several hours or days. The interval of time that the contents will be preserved is determined by the memory size and ambient temperature.

A memory cycle is stolen periodically to refresh the semiconductor memory. A 750-nanosecond cycle is unavailable every 31 microseconds. This interval represents approximately 2.0 percent of the total available time. An estimated performance reduction should be accounted for during time critical instruction sequences.

2.3.3 ASSIGNED MEMORY LOCATIONS

The Model 980B memory has certain reserved locations which are assigned to interrupt and input/output status information. These locations with corresponding functions are listed in table 2-2.
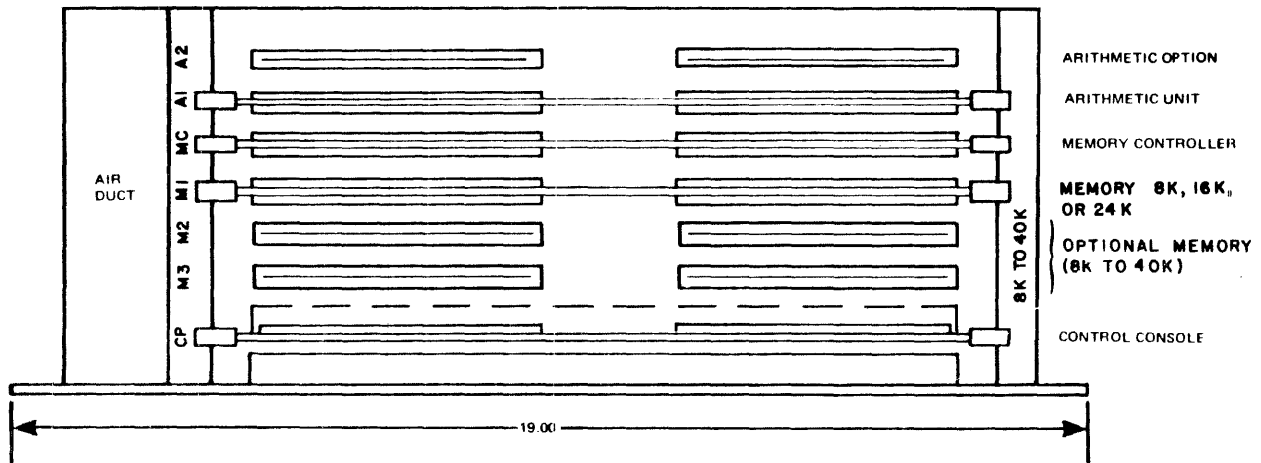
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Figure 2-3. Model 980B Memory Card Slot Locations Top View

Table 2-2. Assigned Interrupt and Input/Output Memory Locations

Hexadecimal Memory Address	Function
0-1	POWER-UP TRAP ADDRESS
2-3	INTERNAL INTERRUPT TRAP ADDRESS
4-5	DIRECT MEMORY ACCESS CHANNEL INTERRUPT TRAP ADDRESS
6-7	INPUT/OUTPUT BUS INTERRUPT TRAP ADDRESS
8-87	EXTERNAL PRIORITY TRAP ADDRESS (OPTIONAL)
96-97	DIRECT MEMORY ACCESS CHANNEL STATUS
98-99	STATUS, DMAC DEVICE CONTROLLER 0
9A-9B	STATUS, DMAC DEVICE CONTROLLER 1
9C-9D	STATUS, DMAC DEVICE CONTROLLER 2
9E-9F	STATUS, DMAC DEVICE CONTROLLER 3
A0-A1	STATUS, DMAC DEVICE CONTROLLER 4
A2-A3	STATUS, DMAC DEVICE CONTROLLER 5
A4-A5	STATUS, DMAC DEVICE CONTROLLER 6
A6-A7	STATUS, DMAC DEVICE CONTROLLER 7

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2.3.4 BOOTSTRAP LOADER

The Model 980B incorporates as a standard feature the capability of entering 256 words of program into main memory, starting at location zero (0), by the actuation of the LOAD switch on the control panel. These 256 words are permanently contained in four Read Only Memory (ROM) packages located on the control panel circuit board. The standard 256 program words consist of a loader control routine and seven bootstraps for all commonly used peripheral devices.

2.3.5 PRIVILEGED INSTRUCTION FEATURE AND PROTECTED MEMORY

The Model 980B has a Privileged Instruction Feature (PIF) which allows certain instructions and areas of memory to be protected. The PIF hardware is located on the memory controller circuit board and has three operational features which are defined in separate paragraphs which follow.

2.3.5.1 INTERRUPT. The PIF causes an internal interrupt and prevents execution if an attempt is made to read or write in protected memory when the PIF is enabled.

2.3.5.2 PROTECTED AREA. The PIF defines a protected area in memory and causes an internal interrupt if an attempt is made to read or write in protected memory when PIF is enabled. The protected area is defined by two registers in the memory controller which can be loaded with the I/O write direct instruction.

2.3.5.3 ADDRESS BIAS. The PIF automatically adds an address bias to all CPU generated memory addresses if the bias feature of PIF is enabled.

2.3.6 REGISTER ORGANIZATION

The Model 980B has eight directly addressable hardware registers. These eight registers with related designations and functions are listed in table 2-3.

Table 2-3. Register Designations and Functions

Number	Designation	Function
0	A	Primary arithmetic register
1	E	Secondary (extension) arithmetic register
2	X	Index register
3	M	Maintenance register
4	S	Storage register
5	L	Link register
6	B	Base register
7	PC	Program counter

2.3.7 PROGRAM STATUS BLOCK

In addition to the registers listed in the previous section, there is another register under program control which is identified as the status register. The status register together with the program counter constitutes the status block. The status register is used to hold the condition of the computer and instruction execution results at any time and to enable or disable interrupts. Table 2-4 lists the status register bits with related functions.

Table 2-4. Status Register Bit Functions

Bits	Function
0-1	Compare Indicators - Indicate result of last compare operation as follows: 00 - less than 01 - equal to 10 - greater than 11 - not allowed
2	Overflow Indicator - Turned on or off by instructions which cause overflow.
3	Carry Indicator- Turned on by any add, subtract, or complement instruction which results in a carry into sign bit (bit 0) of register. If these instructions do not result in a carry into the sign bit, carry indicator is turned off.
4	Privileged Instruction and Memory Protect Control. 0 - Disabled 1 - Enabled
5	Memory Protect Address Violation - May not be set under program control. The results are as follows: 0 - No Violation 1 - Violation
6	PIF Instruction Violation May not be set under program control. The results are as follows: 0 - No Violation 1 - Violation
7	I/O Bus Interrupt Control 0 - Disabled 1 - Enabled

Table 2-4. Status Register Bit Functions (Continued)

Bits	Function
8	Expanded Interrupt Feature Control 0 - Disabled 1 - Enabled
9	PIF Lower Limit Address Bias 0 - Disabled 1 - Enabled
10	Index Control 0 - Post Indexing 1 - Pre-indexing
11	Memory Parity Error Interrupt Control 0 - Disabled 1 - Enabled
12	DMAC Interrupt Control 0 - Disabled 1 - Enabled
13	Not Used
14	Memory Parity Error Indicator - May not be set under program control. The results are as follows: 0 - No Error 1 - Error
15	Power Fail Indicator - A one millisecond warning that power failure is imminent. May not be set under program control. The results are as follows: 0 - Power Up 1 - Power Failure imminent

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2.3.8 PRIORITY INTERRUPT

The Model 980B features a priority interrupt system that provides added program control of input/output operations, provides immediate response to abnormal conditions, and allows immediate recognition of special external conditions. The interrupt system has four priority levels to provide the programmer flexible control of the computer system. The four interrupts with related priorities are listed in table 2-5.

Table 2-5. Model 980B Interrupts and Priorities

Interrupt	Priority	Trap Address	Remarks
Internal	1	2_{16}	Includes illegal op code, PIF violation, memory parity error, and power failure
External Priority (optional)	2	8_{16} TO 87_{16}	Option which allows up to 64 external interrupts with priority
DMAC	3	4_{16}	Direct Memory Access Channel interrupt
I/O	4	6_{16}	Input/Output Bus interrupt

2.3.8.1 INTERNAL INTERRUPT. An internal interrupt provides immediate attention to the following conditions:

1. Uncorrectable memory error

2. Power failure

3. Privileged Instruction Feature violation

4. Illegal operational code execution

The memory error interrupt protects the user against possible data transmission errors. If a MERR signal is generated for this condition, status register bit 14 is set to logic one and if memory error interrupt control bit (status register bit 11) is set to a logic one, an interrupt is generated which causes the CPU to perform a trap; otherwise, the memory error is ignored. The MERR signal should indicate a double bit error (an uncorrectable condition) and does not occur for correctable single-bit errors. If three or more bits are in error (an unlikely condition) the operation of the error correct circuitry varies, as do system indications.

The power failure interrupt allows the user to program an orderly power-up and power-down sequence. When power failure is imminent (1 millisecond to loss of power) an internal interrupt is generated and status register bit 15

is set to a logic one. When power is restored the status register is cleared and the instruction in memory location zero (0) is executed.

The privileged instruction feature violation interrupt occurs when PIF is enabled by setting status register bit 4 and a PIF violation occurs. Status register bits 5 and 6 indicate to the user the type of violation that has occurred.

The illegal operational code execution interrupt occurs when the CPU attempts to execute an illegal or undefined operational code. The programmer will note that this interrupt occurs when status register bits 5, 6, 14, 15, are all zero's.

When an internal interrupt is detected, a trap to memory location 2 is taken. The instruction in location 2 is executed; however, the program counter remains unchanged unless the instruction specifies a program counter change, i.e., branch or store status block, etc. If the instruction does not modify the program counter, the following instruction is executed from the normal program sequence. All other interrupts are locked out for the duration of the trap instruction plus the following instruction. The internal interrupt cannot be disabled. If the machine traps because an illegal operation occurs and an illegal instruction is located in memory location 2, the machine is halted. When an internal interrupt is recognized, bits 4 to 9, 12, 14 and 15 of the status register are cleared to zero after the instruction in the trap location is executed.

2.3.8.2 EXTERNAL PRIORITY INTERRUPT. The Model 980B has provision for an optional interrupt system that is expandable to 64 interrupts. These 64 interrupts have a priority structure. An interrupt generated by this external priority option causes the CPU to trap to one of 64 double-word trap locations if status register bit 8 is set to a logic one. Note that only 32 of these interrupts are supported in standard CPU with provision for further user expansion.

2.3.8.3 DIRECT MEMORY ACCESS CHANNEL INTERRUPT. The Direct Memory Access Channel (DMAC) interrupt is taken when a DMAC device changes status. Status register bit 12 is set to a logic one to enable the DMAC interrupt trap. The DMAC interrupt causes a trap to location 4. The instruction in memory location 4 is executed; however, the program counter remains unchanged unless the instruction specifies a program counter change. If the program counter remains unchanged, the following instruction is executed from the normal program sequence. All other interrupts are locked out for the duration of the trap instruction plus the following instruction. When a DMAC interrupt is recognized, bits 7 and 12 of the status register are cleared to zero after execution of the instruction in the trap location.

2.3.8.4 INPUT/OUTPUT BUS INTERRUPT. The I/O Bus devices can initiate an I/O interrupt which causes the CPU to trap to memory location 6. The instruction in memory location 6 is executed; however, the program counter remains unchanged unless the instruction specifies a program

counter change. If the program counter remains unchanged, the following instruction is executed from the normal program sequence. All other interrupts are locked out for the duration of the trap instruction plus the following instruction. If bit 7 of the status register is zero, no I/O interrupts are recognized. Once an interrupt is recognized, bit 7 of the status register is cleared to zero after execution of the instruction in the trap location.

2.3.9 INPUT/OUTPUT BUS

The I/O Bus structure is shown in figure 2-4. The basic Model 980B chassis has four I/O ports available for peripheral device controllers. The I/O expansion option allows up to 9 additional I/O ports in the Model 980B chassis for a total of 13 internally and up to 256 I/O ports total with an external chassis. Available I/O devices for the Model 980B are listed in table 2-6. Additional I/O Bus information is available in the Input/Output Manual for the Model 980 Computer (TI Part No. 960694-9701).

2.3.10 DIRECT MEMORY ACCESS CHANNEL

The computer provides high speed input/output through the Direct Memory Access Channel (DMAC). A single direct memory access port is included in the basic DMAC for input/output through one peripheral controller. A direct memory access port expander may be added to the DMAC. This port expander allows up to eight high-speed input/output peripheral devices. The DMAC is activated under program control and, once started, performs the designated input/output function independently of the program. An interrupt may be generated when the input/output function is completed and the status of the task is automatically stored in memory. Peripheral devices which are available for the Model 980B DMAC port are listed in table 2-7. The DMAC input/output operation is initiated by the Automatic Transfer Instruction (ATI).

A complete description of the DMAC system and DMAC controllers is included in the Direct Memory Access Channel Manual (TI Part No. 966312-9701) and the Direct Memory Access Channel Controller Manual (TI Part 966312-9702), respectively.
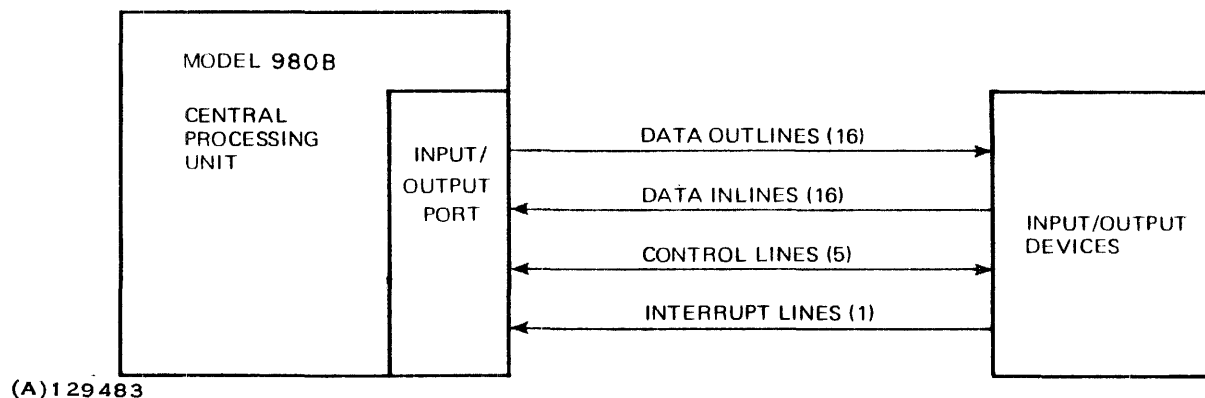

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Figure 2-4. Model 980B Input/Output Bus Structure Functional Diagram

Table 2-6. Model 980B Input/Output Equipment Characteristics

Equipment	Characteristic
Teleprinter	Teletype, TI Silent 700 Model 30, 30 cps
Teleprinter	TTBE, Teletype ASR 33TBE, 10 cps
Paper-Tape Punch	75 cps
Paper-Tape Reader	300 cps
Video Terminal	CRT display with keyboard
Card Reader	300 cpm
Card Punch	100 cpm
A/D Converter	Wide Range, High Speed, High Level
General Purpose Module	16 Lines In/out
Line Printer	132 Column, 100 cps
D/A Converter	General Purpose

Table 2-7. Model 980B Direct Memory Access
Channel Equipment Characteristics

Equipment	Characteristic
Card Reader	High Speed, 600 cpm
Line Printer	80 Column, 356 lpm,
Magnetic Disc	Fixed Head, High Reliablity, 57K to 1835K words
Magnetic Disc-Type 31	Moving Head, Cartridge, 1.14 to 4.56 million words
Magnetic Disc-Type 44	Moving Head, Cartridge 4.56 to 18.24 million words
Magnetic Tape Transport	9 Track, 800 bpi, 37.5 ips

2.3.10.1 DATA HANDLING. When transferring data between memory and a single device, the maximum transfer rate is 10^6 words per second. When memory access is granted to more than one device, none requiring successive memory cycles, four system clock cycles must elapse between servicing the first device and granting access to the second device. The maximum data transfer rate for these conditions is 8×10^5 words per second.

The DMAC services access requests from multiple devices on a priority basis. Priority for data transferred from the devices is selectable by the user; however, an interrupt from any device has priority over access requests for data transfer. The DMAC has priority over the CPU when both require memory access at the same time.

2.3.10.2 CONTROLLER INTERRUPTS. The DMAC interrupt is taken when the DMAC interrupt line to the CPU is on and status register bit 12 is logic one. When interrupt lines from the device controllers to DMAC are

turned on, bits are set in the DMAC interrupt status register to indicate the interrupt source. One or more bits set in the DMAC interrupt status register will cause the DMAC interrupt line from the DMAC to the CPU to turn on. If the CPU has the DMAC interrupt masked, further interrupts from other device controllers will only cause more bits to be set in the DMAC interrupt status register. The device controllers interrupt line remain on until the interrupt recognized (reset) signal is received.

As the CPU traps to the DMAC interrupt trap location (4_{16}), the interrupt recognized signal to the DMAC is turned on. The DMAC responds with interrupt recognized to each controller that has set an interrupt bit in the DMAC status register. The DMAC and device controller status words are then stored in dedicated memory. After status words are stored, the DMAC trap is executed and control is transferred to the proper interrupt service routine. The DMAC interrupt is masked upon trapping to the trap location to protect the interrupt routine. Masking of individual device controller interrupts is controlled by a bit in the device initialization list.
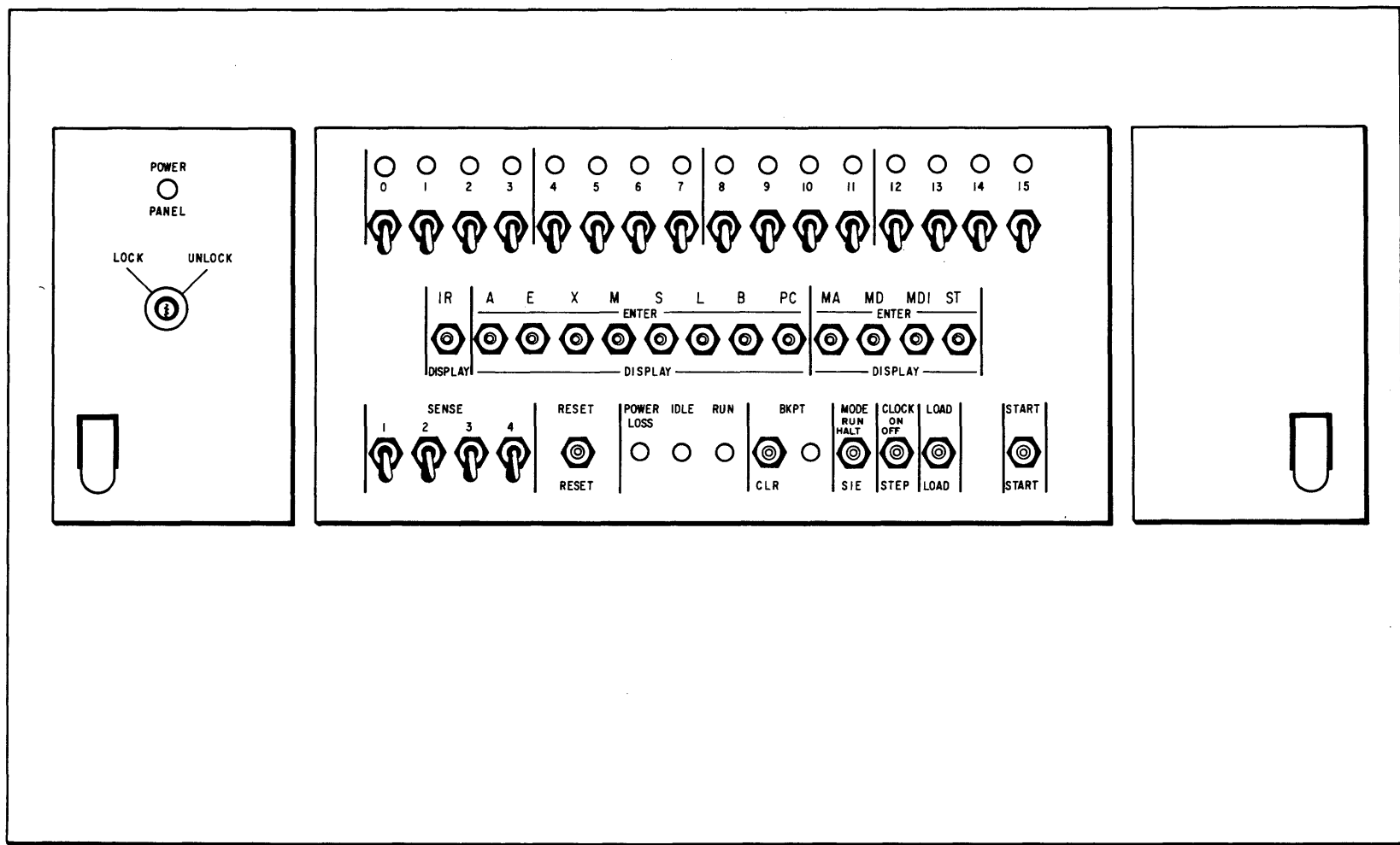
2.3.11   CONTROL CONSOLE

The Model 980B computer control console is shown in figure 2-5. Except for the console lock switch, all controls are two or three position toggle switches. An incandescent lamp is used for ac power indication. All other indicators on the console use light emitting diodes. The functions of all switches and indicators are described in paragraphs which follow.

2.3.11.1   DATA INDICATORS.   Sixteen Data indicators at the top of the console display machine data. The content of a memory location or of any of eleven machine registers can be displayed while the system is in the HALT mode. Data can be entered manually into memory or into any of ten machine registers. When a manual entry is executed, the value is displayed. When the system is in the RUN or SIE (Single Instruction Execution) mode, the present instruction address is continually displayed.

2.3.11.2   POWER INDICATOR.   The POWER indicator is lighted when system ac power is on.

2.3.11.3   POWER LOSS INDICATOR.   The POWER LOSS (memory power failure) indicator is on when memory power is lost and ac power is restored. The POWER LOSS indicator is turned off by activating the System RESET switch.

2.3.11.4   IDLE INDICATOR.   The IDLE indicator is lighted, and the RUN indicator is extinguished, when an IDLE instruction causes the computer to halt. The IDLE indicator is then extinguished when the computer enters the RUN or SIE MODE.

Figure 2-5.   Model 980B Control Console Front Panel Switches and Indicators

2.3.11.5 RUN INDICATOR. The RUN indicator is lighted when the system is placed in the RUN MODE and the START switch is activated. When the system is removed from the RUN MODE, the RUN indicator is extinguished.

2.3.11.6 BKPT INDICATOR. The BKPT (Breakpoint) Indicator is lighted when the memory address register content is the same as the data switches and the computer is in the RUN or SIE MODE. The BKPT indicator is extinguished by setting the CLR position of the BKPT switch.

2.3.11.7 CONTROL SWITCHES. The Console PANEL LOCK/UNLOCK key operated switch must be in the UNLOCK position to permit use of the console. With this switch in the LOCK position, all console controls are disabled except the data switches (0 through 15), SENSE switches (1 through 4) and BKPT/CLR. The BKPT indicator will continue to monitor the use of the memory address that is specified by the data switch settings. The BKPT/CLR switch will reset the BKPT indicator; however, the breakpoint feature cannot be activated. The DISPLAY indicators will continue to function as described above provided the system is in the RUN MODE. The RUN indicator is extinguished by an IDLE instruction when the console PANEL LOCK/UNLOCK switch is in the LOCK position.

2.3.11.8 DATA SWITCHES. The sixteen data switches are two-position toggle switches that are used for data entry and BKPT (breakpoint) address selection. Each switch is placed in the up position for a logic one, or down for a logic zero.

2.3.11.9 IR SWITCH. The IR switch is used to display instruction register data on the indicators. The switch has a normal center position, a momentary up position, and a momentary down position. When pushed to the DISPLAY (down) position, the content of the instruction register is displayed. The up position of the switch is nonfunctional. The display function is only active while the computer is in the HALT MODE.

2.3.11.10 PC, A, B, E, L, M, S, X, ST, MA AND MD DISPLAY AND ENTER SWITCHES. These switches control the following data DISPLAY and ENTER functions, respectively: Program Counter; Registers A, B, E, L, M, S, X and ST; Memory Address register; and Memory Data. Each switch has a normal center position, a momentary up position, and a momentary down position. When any of these switches is pushed to the ENTER (up) position, the current setting of the 16 DATA switches is loaded into the associated register or memory location. The entered value is displayed by the display indicators. The Memory Data (MD) is entered into the address specified by the contents of the Memory Address (MA) register. If the switch is pushed to the DISPLAY (down) position, the content of the associated register or memory is displayed. All switches in this group only function when the computer is in the HALT MODE.

2.3.11.11 MDI SWITCH. The Memory Data and Increment Address (MDI) switch functions as the MD switch that is described in the preceding paragraph for entering or displaying memory data except each time MDI is actuated to either ENTER or DISPLAY, the Memory Address Register is incremented. It is used for loading or displaying consecutive memory locations.

2.3.11.12 SENSE SWITCHES. The four SENSE switches are two-position toggle switches that are used by the two sense switch instructions (SSE and SSN). Each SENSE switch is placed in the up position for a logic one or down for a logic zero.

2.3.11.13 RESET SWITCH. The system RESET switch is used to reset major system registers. This switch has a normal center position and a momentary down position. When the switch is pushed to the RESET (down) position, the program counter, status register, memory address register, and display register are cleared. This function can occur if the computer is in the HALT or RUN MODE.

2.3.11.14 BKPT SWITCH. The Breakpoint (BKPT) switch is a three-position toggle switch. If the computer is in the RUN or SIE MODE and the BKPT switch is in the center position, the BKPT indicator is lighted when the setting of the data switches is contained in the memory address register. The indicator may be extinguished by pushing the BKPT switch to the CLR (down) position (computer in any mode) without affecting system operation. When the BKPT switch is in the BKPT (up) position and the computer is in the RUN MODE, the computer will HALT and the BKPT indicator is lighted if the setting of the DATA switches is contained in the memory address register. The instruction which uses the breakpoint address is completed before the computer will HALT.

2.3.11.15 MODE SWITCH. The MODE control switch is a three position toggle switch. To start program execution, the MODE switch is placed in the up (RUN) position and the START switch is actuated (placed in momentary down position). The RUN mode is entered and the RUN indicator is lighted when the START switch is actuated. When the MODE switch is placed in the center (HALT) position, the system halts when the instruction in progress is completed. To execute a single instruction, the MODE switch is placed in the down (SIE) position and the START switch is actuated.

2.3.11.16 CLOCK SWITCH. The CLOCK control is a three-position toggle switch with a normal center position (OFF) an up position (ON) and a momentary down position (STEP). For normal system operation, this switch is in the up (ON) position and the system clock is free running. When the CLOCK switch is placed in the center (OFF) position, the arithmetic unit clock is stopped. Each time the CLOCK switch is pushed to the momentary down (STEP) position, a single system clock pulse is generated for the arithmetic

unit. The operation of this switch can be disabled by moving a jumper wire on the console printed circuit board.

2.3.11.17 LOAD SWITCH. The LOAD (store bootstrap loaders in memory) switch is two-position toggle switch with a normal center position and momentary up position. If the system is halted and this switch is pushed to the up position, 256 words of optional firmware program will be loaded into memory. The memory location of the first word will always be zero.

If the MODE switch is in the RUN position, the computer will begin execution at the address in the program counter. If the MODE switch is in the HALT position the computer will not begin execution until the MODE switch is placed in the RUN position and the START switch is actuated (momentary down position).

2.3.11.18 START SWITCH. The START switch is a two-position toggle switch with a normal center position and momentary down position. If the system is in the HALT mode and this switch is pushed to the down (START) position, the RUN or SIE setting of the MODE switch will be enabled.

2.4 SYSTEM PHYSICAL CONFIGURATION

The Model 980B mainframe chassis (figure 2-6) contains space for the system power supply and a connector plate with mating connectors for the control console, system power supply, and 13 printed circuit boards. Supply voltage circuits between the power supply connector and printed circuit board connectors are etched on the connector plate. All other interconnections are wire-wrapped on the back of the connector plate.

2.4.1 CHASSIS MOUNTING

The Model 980B is available in two mounting configurations. The basic model is supplied in the rack-mounted configuration. The optional mounting configuration is the table top (stand alone) enclosure. The mounting dimensions for the Model 980B are included in Section III of this manual.

2.4.2 MAINFRAME PRINTED CIRCUIT COMPLEMENT

The area immediately behind the front panel contains space for the control console and six large (10.5 inches high by 14.25 inches wide) printed circuit boards. Each printed circuit board slot is identified by markings located on the top edge of this card cage.

The control console and each large printed circuit board plugs into two 80-pin connectors. The basic system is shipped with the control console, one 8K memory board, the memory controller board, and two arithmetic boards located in the card cage for the large boards as shown in figure 2-6.

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BASIC MODEL 980B MAINFRAME WITH OPTIONAL EXPANSION CHASSIS INSTALLED
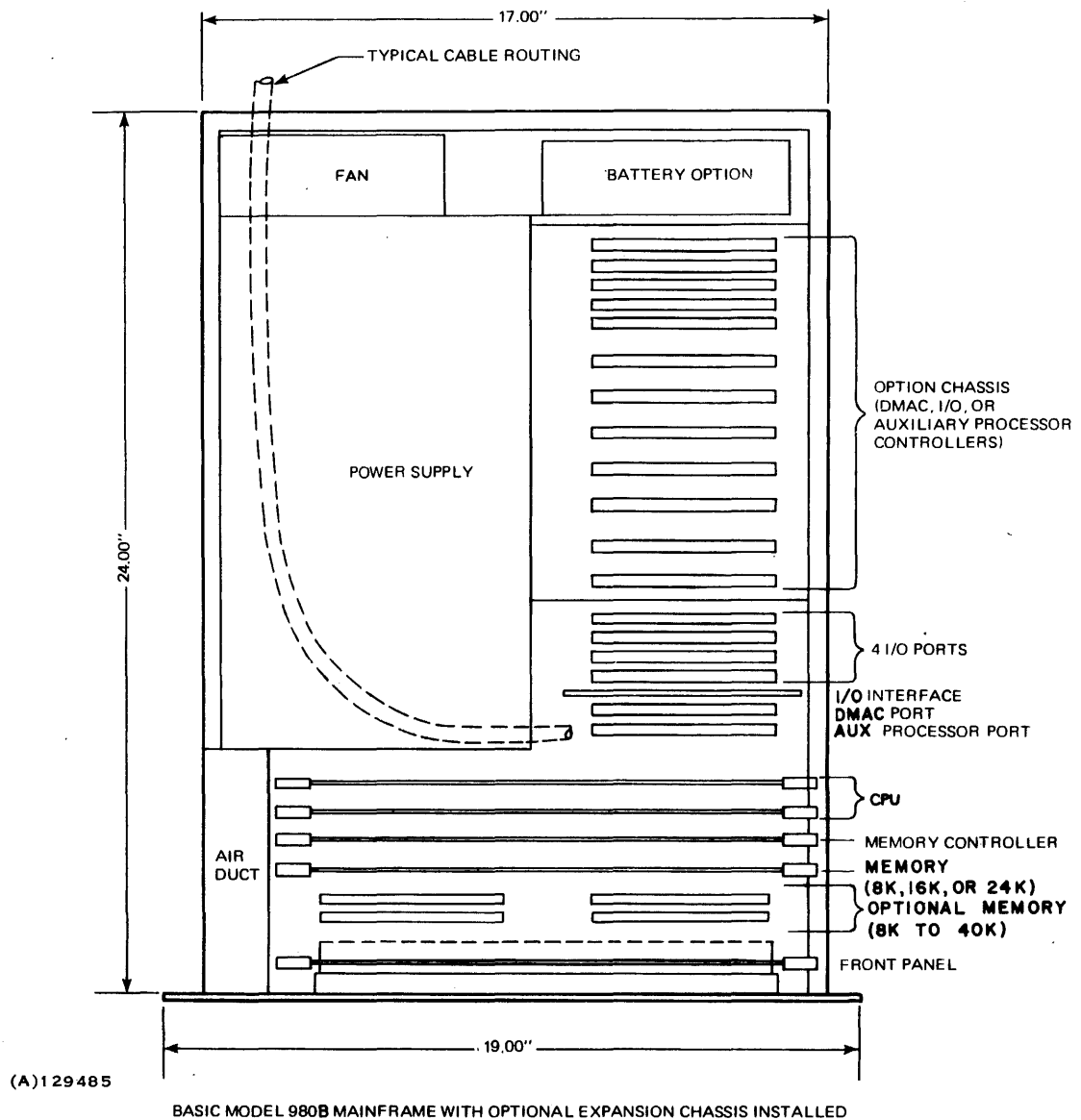
Figure 2-6. Model 980B Mainframe Chassis Layout

The second card cage is located adjacent to the power supply and behind the large card cage. This card cage accepts seven (10.5 inches high by 7 inches wide) printed circuit boards. These smaller printed circuit boards plug into single 80 pin connectors. In this physical area, only the I/O interface card is supplied with the basic Model 980B. The remaining connectors are available as optional APP, DMAC, and I/O Controller cards. The mainframe printed circuit card complement is listed in table 2-8.

An additional optional expansion chassis can be placed to the rear of the small card cage. This chassis can be configured for various DMAC, I/O, or APP devices. Figure 2-7 includes the connector and card cage dimensions.

Table 2-8. Mainframe Printed Circuit Board Complement

Connector Designation	Printed Circuit Board
BASIC PRINTED CIRCUIT BOARDS	
CP	Control Console
M1	8K, 16K, or 24K Memory
MC	Memory Controller
A1	Arithmetic Unit 1
A2	Arithmetic Unit 2
IO0	I/O Interface
OPTIONAL PRINTED CIRCUIT BOARDS	
M2	8K, 16K, or 24K Memory
M3	8K, 16K, or 24K Memory
DMA	DMAC Interface
IO1	I/O Controller
IO2	I/O Controller
IO3	I/O Controller
IO4	I/O Controller

2.4.3 BATTERY OPTION

The mainframe chassis contains space for mounting a battery which provides
supply voltages required to preserve the contents of semiconductor memory
when system ac power is off. A cable from the battery mates with a connec-
tor on the system power supply. The mating connector and battery charging
circuits are included in the basic system power supply; therefore, the battery
option is installed by mounting the battery pack and connecting the battery
cable. The battery is charged continuously when system ac power is on.

2.4.4 POWER SUPPLY

The system power supply is a self-contained, removable unit which provides
all regulated voltages required by the mainframe circuits. Electrically, the
power supply provides six regulated outputs and two unregulated outputs.
Regulated outputs from the power supply are +5V, -5V, +5V Standby (STBY),
+12V, +15V, and -15V. The +5V STBY, -5V, and +12V are battery main-
tained in case a primary power failure (115V ac, 47-63 Hz) occurs. The un-
regulated ±35V ac line is used for external rectification, filtering and regula-
tion.

The power supply is self contained except for an external mounted battery.

The 960B/980B Power Supply input power requirements are listed in table
2-9 and output power characteristics are listed in table 2-10.
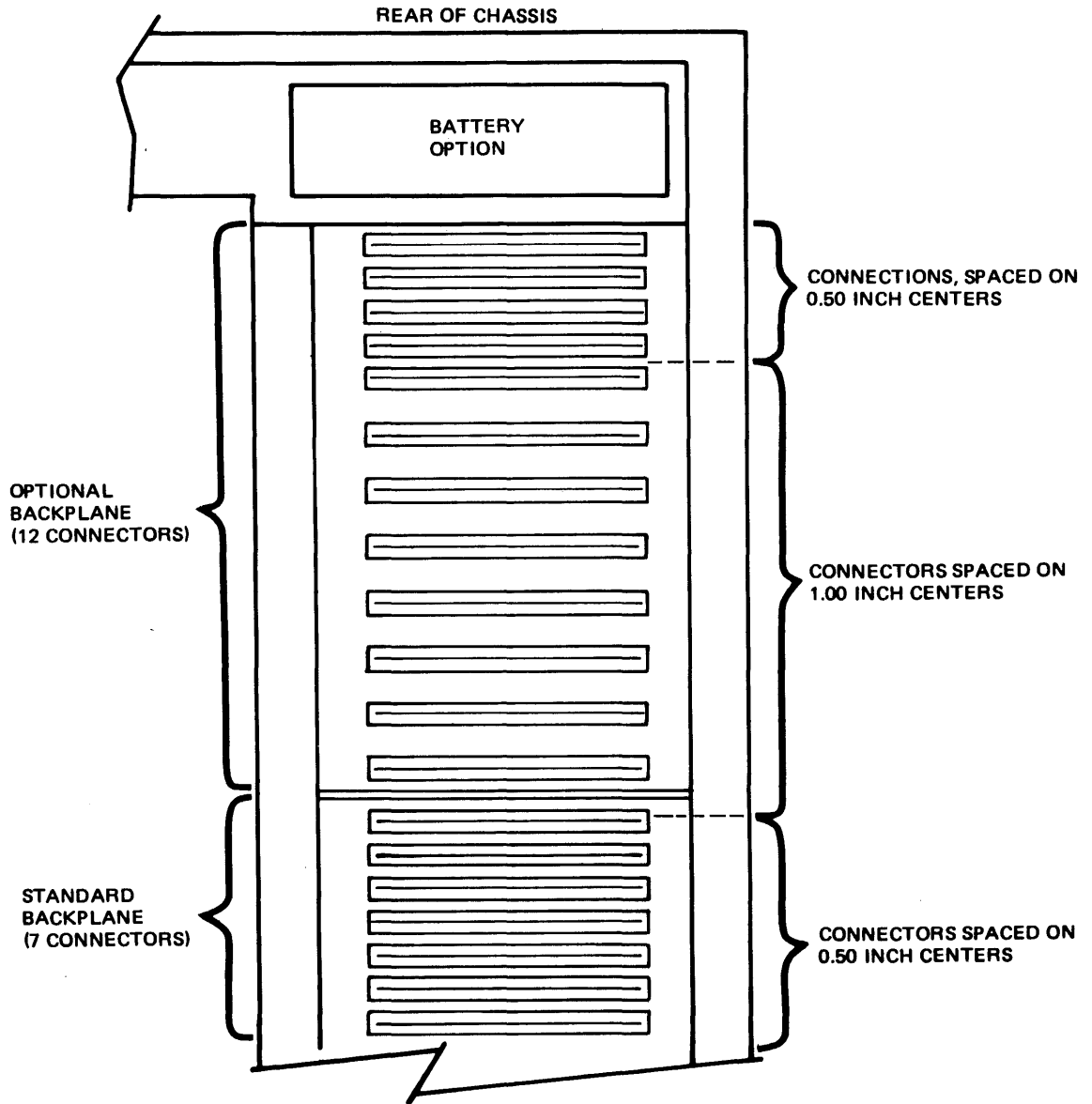
NOTE: ALL CONNECTORS CONTAIN 80 PINS WITH 0.125 INCH BETWEEN PIN CENTERS.
CARD THICKNESS IS 0.063± 0.006 INCHES. CONNECTOR WILL ACCEPT
MAXIMUM CARD WITH OF 5.080 INCHES. CARD CAGE ACCEPTS MAXIMUM
CARD WIDTH OF 7.010 INCHES AND HEIGHT OF 10.5 INCHES.

(A)129486

Figure 2-7. Model 980B Connector and Card Cage Dimensions

Table 2-9.   Power Supply Electrical Characteristics

Characteristic	Specification

Voltage	100 + 15 percent Vac
	    - 10 percent Vac
	200 + 15 percent Vac
	    - 10 percent Vac

Frequency	47 - 63 Hz
Current	5 A at 115 Vac max

Table 2-10.   Power Supply Output Power Characteristics

Nominal Voltage (Volts)	Voltage Tolerance (Percent)	AC Operation Full Load Current (Amperes)	Battery Operation (Standby Memory Protect) 32K
-5.0	±5		17mA*
+5 MAIN	±2	30.0	Regulator Off
+5 STBY	±2		30mA*
+12	±3		200mA
+15	±5	0.35	-
-15	±5	0.35	-

*Maximum currents exceed 25° Centigrade refresh requirements.

In addition to providing power to the computer, the power supply provides cooling air to the system. The power supply is thermally protected and all regulators are current-limited, short-circuit proof and have overvoltage protection.

Temperature, humidity, shock, and other environmental characteristics of the power supply are listed in table 2-11.

NOTE

After installing a new or replacement battery, operate the computer for 24 hours without depending on the battery to maintain memory. This 24 operating-hour period allows the battery to attain an acceptable charge level. Power failures that occur during this initial charging period may result in memory data loss due to insufficient standby power.

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Table 2-11. Power Supply Environmental Characteristics

Characteristic	Specification
Operating Temperature (Air entering unit)	0° to 50° Centigrade (Sea level, 60 Hz)*
Storage Temperature	-40° to 65° Centigrade
Humidity: Storage Operating	0 to 95 percent relative humidity 0 to 95 percent relative humidity, noncondensing
Altitude	0— 10,000 feet*
Shock: Operating Shipping	1G 30 G (applied to shipping carton)

* Upper operating temperature. Derate 2 degrees centigrade for
each 2500 feet of altitude and an additional 5 degrees centigrade
for 50 Hz.

Standby power is provided to maintain memory in the event of ac power loss.
Standby power is much lower than normal operating power and is used only
to refresh the computer memory. There are two 5 Ampere-hour, 12 volt,
jelled electrolyte, lead-acid batteries that supply standby power. These
batteries are mounted outside the power supply, but inside the computer.
The power supply contains a battery test circuit and a battery charger. A
discharged battery can be charged to 80 percent of capacity in 20 hours, and
to 100 percent of capacity in 48 hours. Standby time is determined by bat-
tery age, ambient temperature, and quantity of memory. Battery charge
and discharge curves are illustrated in figure 2-8 and figure 2-9, respec-
tively. A voltage controlled latch is provided to indicate the battery is low
enough to cause possible loss of memory in the standby mode. Indication is
given by the POWER LOSS indicator on the control console of the computer.
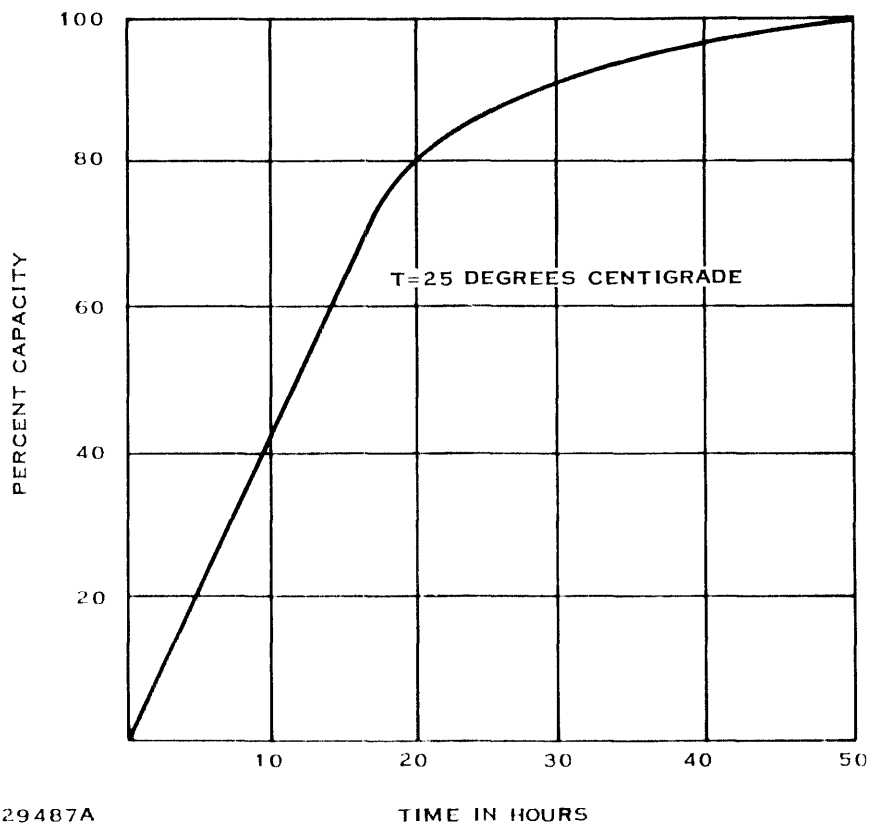
(A)129487A

Figure 2-8. Standby Battery Curve Charge

Digital Systems Division
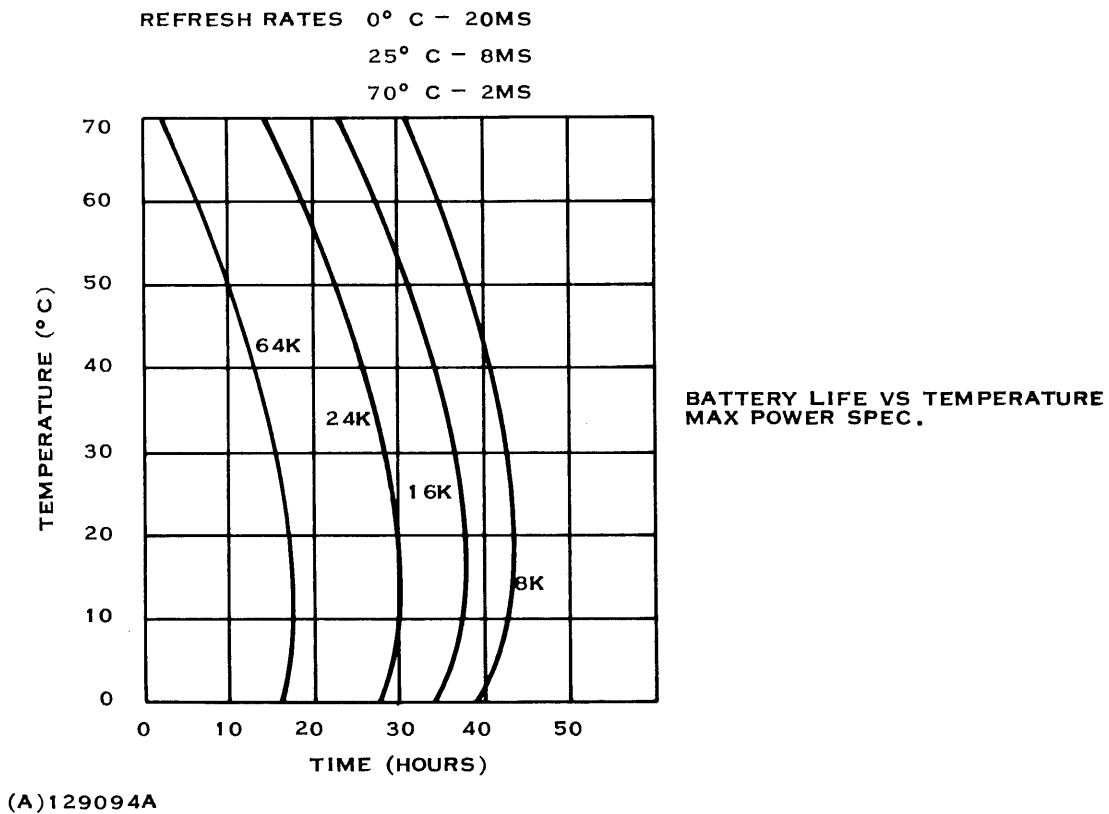
Figure 2-9. Standby Battery Discharge Curve

SECTION III

INSTALLATION

3.1 GENERAL

The Model 980B Computer system is a flexible system; therefore, this computer hardware is available for purchase and delivery to the customer in many configurations. The "Sales Order" that is shipped with the system lists each major Model 980B system component that has been purchased and shipped to the customer.

Figure 3-1 illustrates a typical Model 980B Computer configuration. This typical configuration is not necessarily the same as the configuration that is

(A)129488
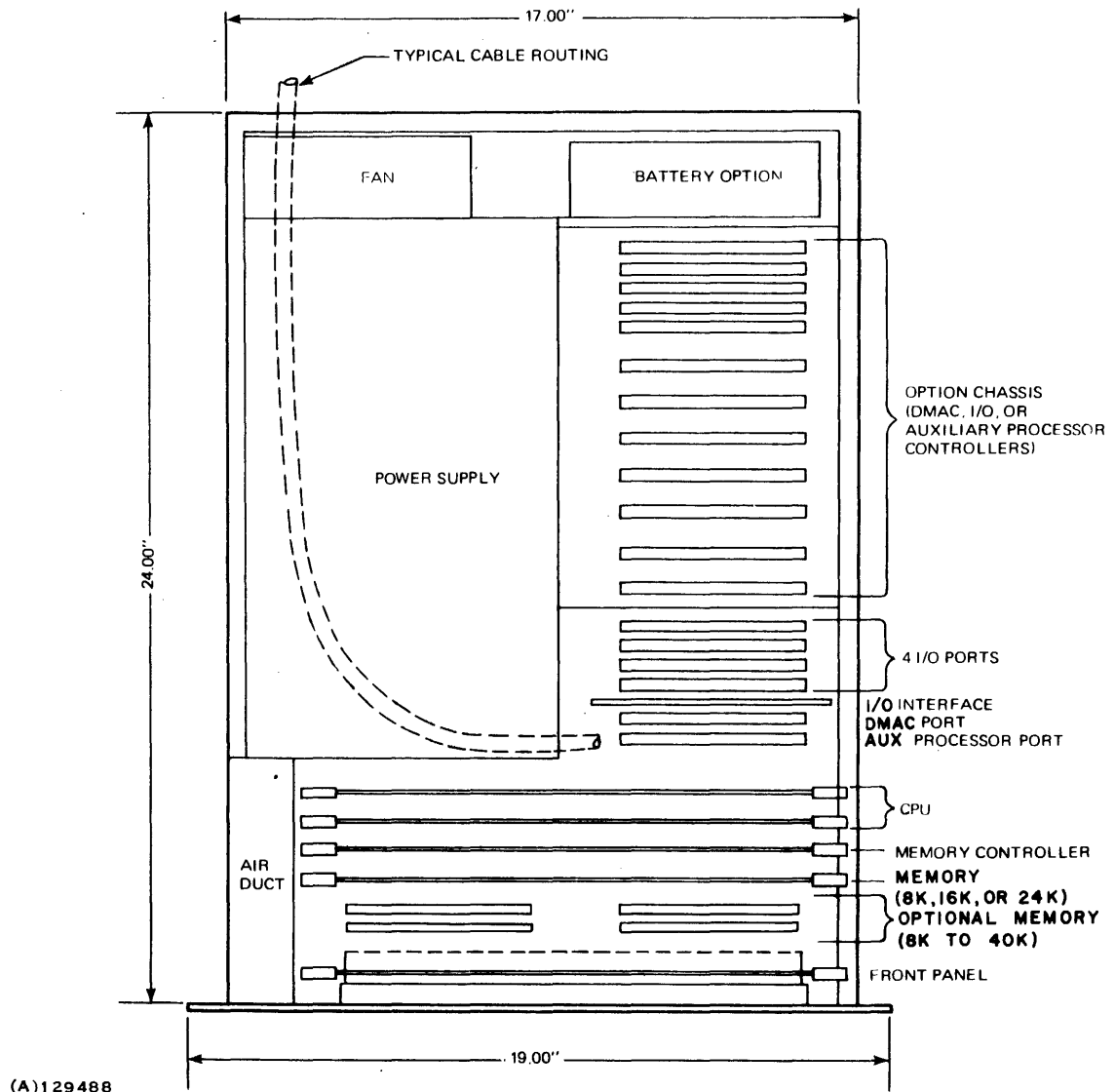
Figure 3-1. Model 980B Mainframe with Options

delivered to the customer. In this figure, major components of the Model 980B system are clearly illustrated and identified.

The nomenclature that appears on the Model 980B Computer chassis identifies the function and location of each printed circuit board. This nomenclature is printed on the computer chassis adjacent to the corresponding card slot that the related printed circuit board occupies. The functional nomenclature appears on both the Model 980B Computer chassis and each printed circuit card ejector. This duplication of nomenclature permits quick identification of the card and the associated slot that the printed circuit card occupies.

Direct Memory Access Channel (DMAC) and Input/Output (I/O) expansion cabling and connections are illustrated in figures 3-2 and 3-3, respectively.

3.2 REQUIREMENTS

Before the Model 980B Computer installation is implemented, certain environmental, physical, and electrical requirements should be noted. These requirements are identified in separate subparagraphs which follow.

3.2.1 ENVIRONMENTAL REQUIREMENTS

The recommended ambient temperature range for system operation (at sea level and 60 Hz) is 0 degrees to 50 degrees Centigrade. Humidity may range from 0 percent to 95 percent relative humidity (noncondensing) during operation. Storage temperature and ranges are -40 degrees to 65 degrees Centigrade and 0 percent to 95 percent relative humidity (noncondensing), respectively. Altitudes of 0 to 10,000 feet are acceptable. The upper temperature operating limit must be derated 2 degrees Centigrade for each 2500 feet of altitude and 5 degrees Centigrade for 50 Hz operation.

3.2.2 PHYSICAL REQUIREMENTS

The Model 980B Computer is made available to the customer in several physical configurations. The computer chassis is available in a table top configuration or a configuration suitable for installation in a standard 19-inch rack mount cabinet. The physical dimensions of the chassis for the rack mount installation are as follows:

Front Panel		Chassis	
Height:	12.25 inches (31.1 cm)	Height:	12.25 inches (31.1 cm)
Width:	19.0 inches (48.2 cm)	Width:	17.00 inches (43.2 cm)
		Length:	24.00 inches (61 cm)
		Weight:	75 lbs. (34.1 kg)

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DMAC EXPANSION CABLE
(TI PART NO. 217079)

980 COMPUTER

DMAC EXPANDER KIT (966555-002)

EXTERNAL EXPANSION

980 COMPUTER

INTERNAL EXPANSION
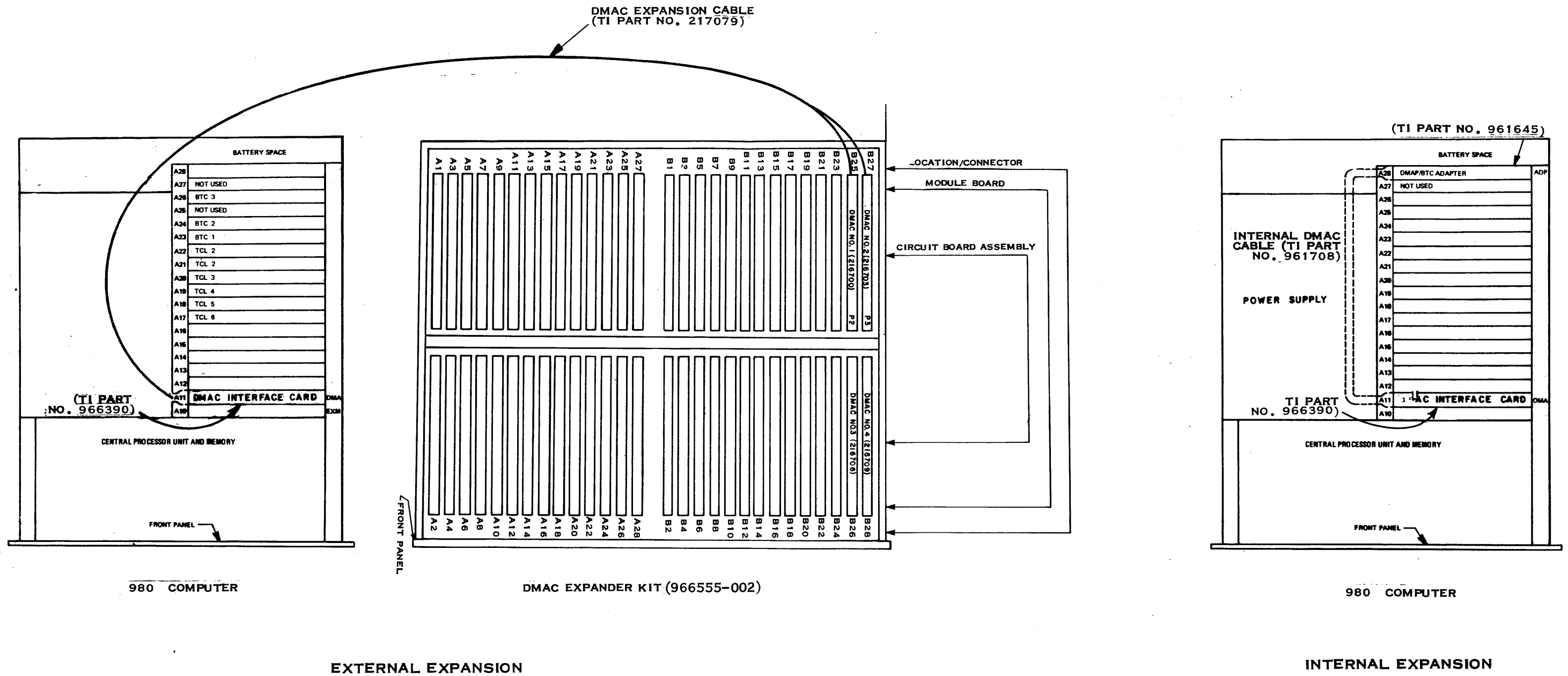
(B)129489

Figure 3-2. DMAC Expansion Cabling
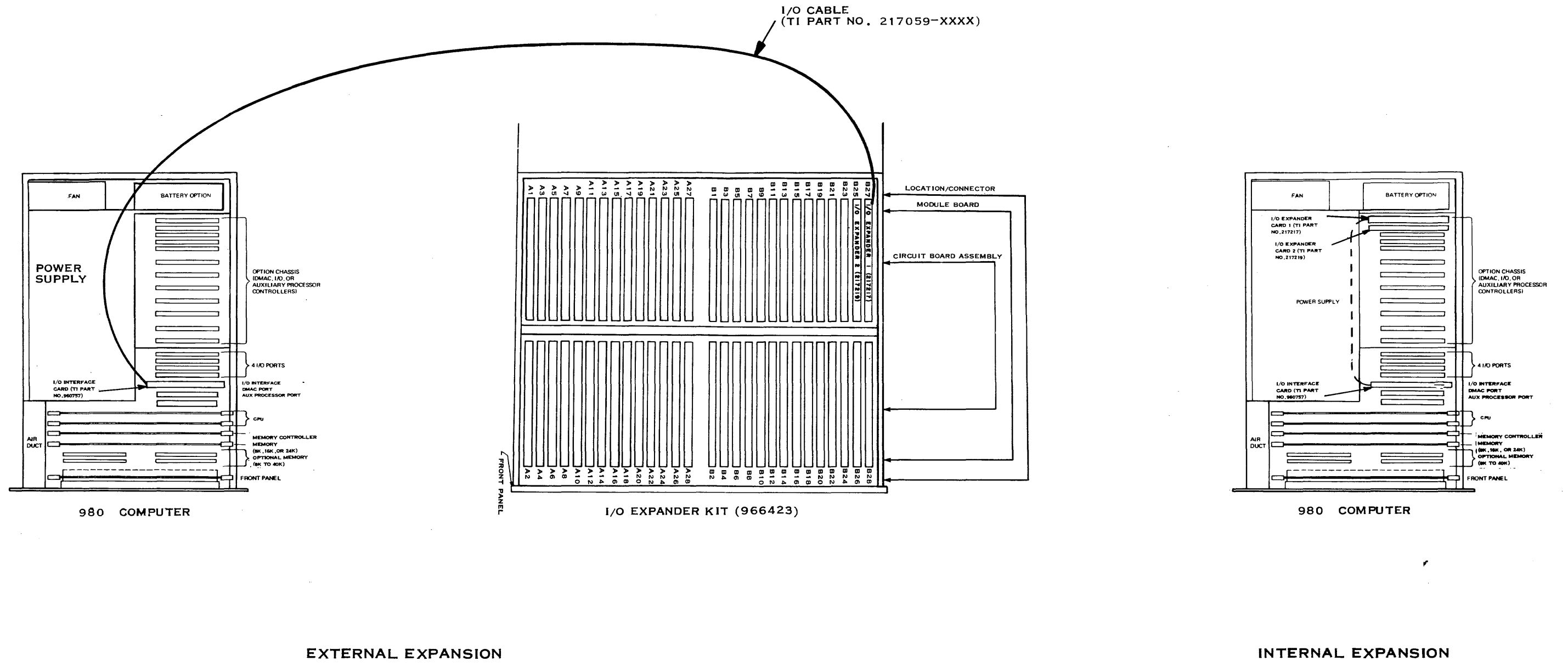
Figure 3-3. Input/Output Expansion Cabling

(B)129490

When the Computer is to be installed in a standard rack mount cabinet, it is necessary to install special drawer slides in the equipment cabinet and on the computer chassis. These slides are delivered with the Model 980B. Procedures for installing these slides are provided in a separate paragraph.

3.2.3 POWER REQUIREMENTS

The power requirements for the Model 980B Computer are listed in table 2-9.

3.3 INSTALLATION

After the Model 980B is unpacked as specified in the "Unpacking Instructions" that are located on the shipping carton, install the computer as specified in the subsequent subparagraphs which follow.

NOTE

Before proceeding with the subsequent steps of this procedure, read the complete procedure to avoid a duplication of effort and undue delay.

The computer is designed for installation in several mechanical configurations. If the computer is to be installed as a "stand alone/table top" model, disregard the mechanical installation instructions specified in paragraph 3.3.1.

3.3.1 MECHANICAL INSTALLATION

The computer is delivered with a right-hand drawer slide and a left-hand drawer slide. Be sure that the correct slide is selected before proceeding with the slide installation (manufacturer's label appears right side up and forward when installed). Each slide is mounted on the computer chassis with bolts. The second channel is mounted in a standard equipment rack using small angle brackets. If the Model 980B is to be used in a rack mount configuration, install the slides on the Model 980B chassis as illustrated in figure 3-4 and install the slides in the standard equipment cabinet as illustrated in figures 3-5 and 3-6. Using the slides installed in the cabinet and on the chassis, mount the Model 980B chassis in the equipment cabinet.

With the top of the Model 980B exposed, use the "Sales Order" that is included in the shipping carton to confirm that all printed circuit cards and system cables that were purchased for the system are included.

3.3.2 ELECTRICAL INSTALLATION

Prior to shipping the Model 980B to the customer, a "Model 980B System Interconnection" document (table 3-1) is prepared for shipment with the Model 980B. This document lists all peripheral kits supported by standard Model 980B software along with the cable, interface card, and standard card slot.
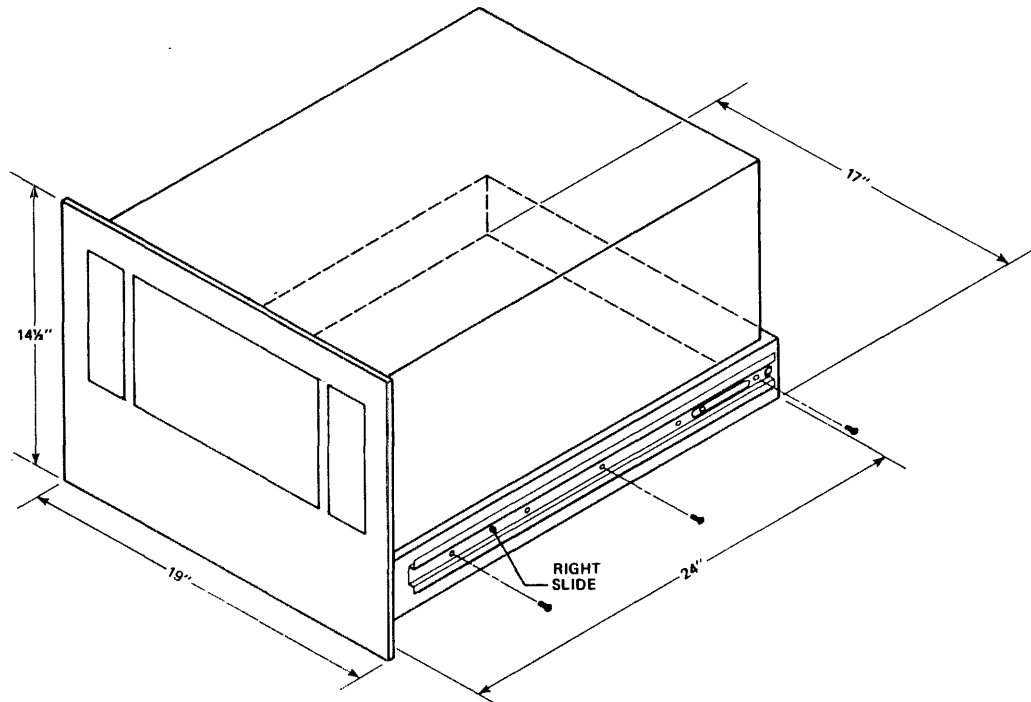
(A)129491

CHASSIS: 24" LONG X 17" WIDE
FRONT PANEL: 14½" HIGH X 19" WIDE

Figure 3-4. Model 980B Chassis Mounted Drawer Slides Installation

A "Software Installation Procedure" is shipped with the CPU to verify the software systems. Nonstandard interconnections will also be noted in this procedure.

Hardware installation and interconnections to nonstandard peripheral hardware must be supported by customer written software.

Detailed information concerning the interconnection of DMAC peripherals is contained in the DMAC Maintenance Manual (TI Part No. 216759-9701).

Confirm that each printed circuit card is installed in the correct card location and that each system cable is connected to the proper printed circuit card and/or peripheral hardware.

Verify that ac power is available and confirm that the voltage and frequency of the ac source are correct. Turn off the ac power circuit breaker at the power source. Connect the ac power cord from the Model 980B to the power source. (The power input circuit breaker should be located between the power source and the Model 980B system.) Turn ON the ac power circuit breaker at the power source. Turn ON the ac power circuit breaker at the rear of the Model 980B. Turn ON the battery switch at the rear of the Model 980B. If the POWER LOSS indicator is illuminated, place the control console RESET switch in the down position. The console POWER LOSS indicator should go out. Depress the BATTERY TEST switch on the rear of

ITEM	PART NUMBER	DESCRIPTION	STANDARD EQUIPMENT CABINET 197014-0001	197014-0002	197014-0003
1	976051-0001	FRAME		X	X
	-0002				
	-0003		X		
2	217252-0001	ANGLE, TAPPED	X	X	X
3	976067-0001	PANEL, REAR	X	X	X
4	976070-0002	PANEL, TOP COVER	X	X	
	-0001				X
5	976075-0002	DOOR, REAR	X		
	-0001			X	X
6	976072-0002	DOOR, SIDE	X		
	-0003			X	
	-0001				X
7	976059-0001	BRACKET, SIDE DOOR	X	X	X
8	232314-0200	LATCH, ADJUSTABLE	X	X	X
9	232314-0220	LATCH, ADJUSTABLE JR.	X	X	X
10	232314-0100	HINGE, PULL PIN	X	X	X
		PANEL WIDTH (INCHES)	19	19	19
		OVERALL WIDTH (INCHES)	25	25	25
		PANEL HEIGHT (INCHES)	43	57	57
		OVERALL HEIGHT (INCHES)	56	70	70
		USABLE DEPTH (INCHES)	24	24	30

(A)129492
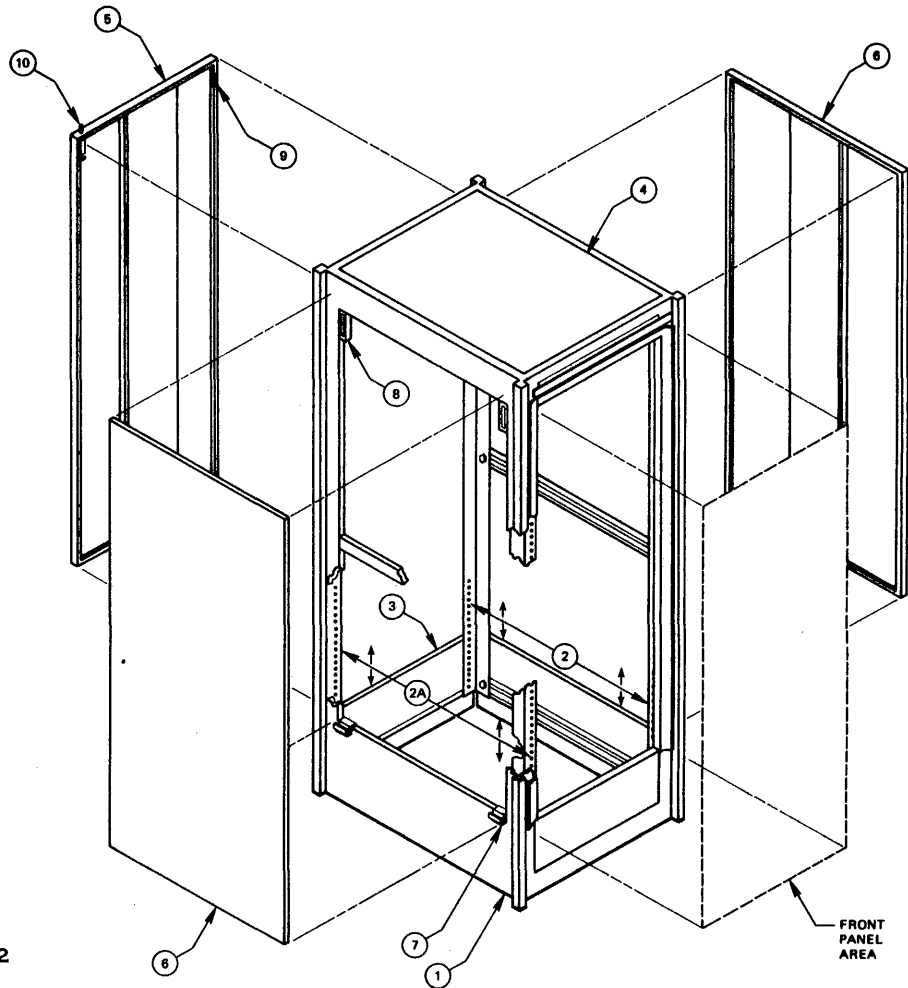
Figure 3-5.   Model 980B Rack Mount Drawer Slides Installation

RIGHT REAR ANGLE
STANDARD EQUIPMENT CABINET

INSERT
RIGHT SLIDE
960/980

0.625 INCHES

RIGHT FRONT ANGLE
STANDARD EQUIPMENT CABINET

(A)129493
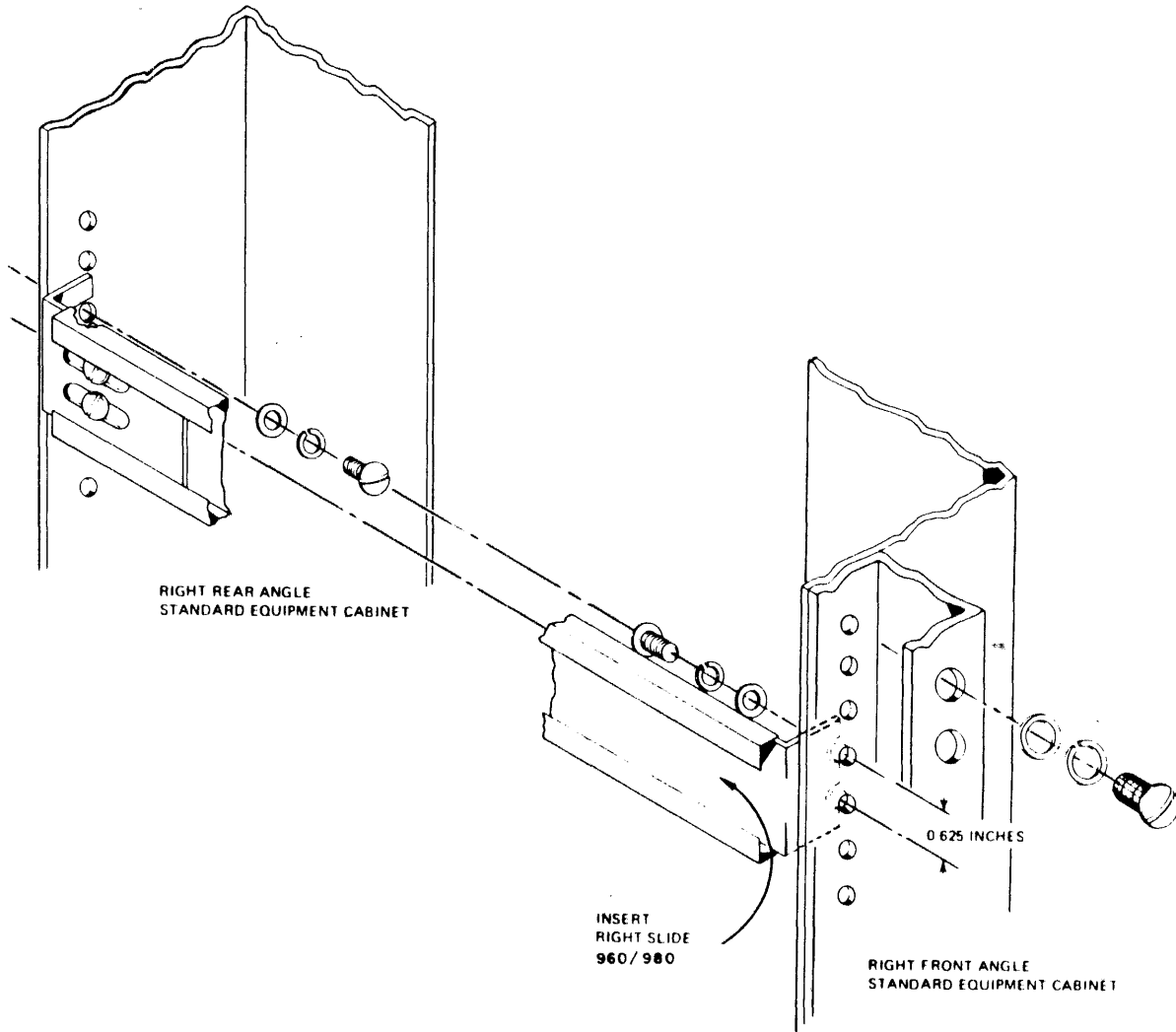
Figure 3-6. Model 980B Detailed Rack Slide Installation

the power supply and observe that the POWER LOSS indicator on the console
remains extinguished. The Model 980B system is now ready for checkout
prior to use. The Model 980B "Software Installation Instructions" should be
implemented at this time. These instructions are delivered with the system.

Table 3-1. Model 980B System Interconnection

Peripheral	TI Kit Part No.	Interface Card Part No.	TI Cable Part No.
Card Reader	966323-0001	217556-0001	966324-0020
Printer, 300 cps	964569-0001	217570-0001	965938-0015
Printer, 150 cps	965940-0001	217570-0001	965939-0015
Printer, 75 cps	965943-0001	217564-0001	961702-0015
Paper Tape Punch and Reader	964568-0001	217570-0001 and 217564-0001	965939-0015
Teletype	965910-0001	217394-0005	
Teleprinter	966330-0001	217394-0001	966331-0030

SECTION IV

SUPPORT DOCUMENTATION

4.1 MAINTENANCE MANUAL DESCRIPTION

The Texas Instruments Model 980B Computer Maintenance Manual is a nine volume document that contains functional and theoretical descriptions of system hardware. This maintenance manual is designed to provide the user with sufficient information to perform maintenance on the Model 980B and the remaining eight volumes can be purchased as required.

The theory of operation for each major functional unit in the Model 980B system is described in a separate volume of the maintenance manual. Maintenance instructions are included in these separate volumes when applicable. These volumes contain sufficient detail to analyze and correct system malfunctions.

NOTE

Personnel that perform maintenance on the Texas Instruments Model 980B Computer system should obtain a Transistor-Transistor Logic (TTL) catalog such as "The Integrated Circuits Catalog for Design Engineers" that is published by Texas Instruments (Catalog CC-401 is available from Texas Instruments, Box 5012, Dallas, Texas 75222). This catalog or a later edition contains detailed information concerning the integrated circuits used in the Model 980B Computer System.

4.2 MAINTENANCE MANUAL ORGANIZATION

The complete Model 980B Maintenance Manual consists of nine volumes which are described in subsequent paragraphs of this section of the manual.

4.2.1 SYSTEM DESCRIPTION (943012-9701)

This manual contains a description of all manuals of the Model 980B maintenance manuals. A basic description of system hardware and performance characteristics, a system installation instruction, and a discussion of the support documentation are also included in this manual which is supplied with the Model 980B Computer.

4.2.2 ARITHMETIC UNIT AND CONTROL CONSOLE (960699-9702)

This manual contains detailed descriptions of the Model 980B Control Console and Arithmetic Unit (AU) assemblies. The AU contains the central processor

data bus structure and a controller which controls the control console and execution of all basic instructions.

4.2.3 MEMORY, MEMORY CONTROLLER, and DMAC (943012-9702)

This manual contains information concerning the semiconductor memory, memory controller, and direct memory access (DMAC) port. The memory controller generates signals which are supplied to the memory to execute a memory cycle in response to a fetch or store command from the DMAC port or Central Processing Unit (CPU). In addition, the memory controller performs memory parity checks, detects memory addressing violations, detects privileged instruction violations, and provides address biasing functions.

4.2.4 INPUT/OUTPUT AND INPUT/OUTPUT EXPANSION (960699-9704)

This manual contains detailed descriptions of the Model 980B Input/Output (I/O) Bus, I/O expansion, and Auxiliary Processor Port (APP). Use of the I/O and APP is discussed and timing diagrams are illustrated in this manual.

4.2.5 POWER SUPPLY (942773-9703)

This manual contains a description of the system power supply which provides all regulated voltages used by mainframe hardware.

4.2.6 PARTS LISTS AND ASSEMBLY DRAWINGS (943012-9703)

This manual contains an assembly drawing for each printed circuit board and all major subassemblies in the Model 980B system. A parts list for each assembly drawing is also included in this volume. The parts list contains a list of all parts and components in each assembly.

4.2.7 ELECTRICAL DRAWINGS (943012-9704)

This manual contains electrical schematics and logic diagrams for circuits which are predominantly composed of discrete components and for logic circuits and electrical connections which are not documented in the form of a tabular computer list. In cases where the electrical connections have been excluded from the electrical or logic drawing and the computer tabulations, point-to-point wire lists are included as an aid for signal tracing during trouble analysis.

4.2.8 LOAD, PIN, AND WIRE LISTS (943012-9705)

These computer generated tables list interconnection of circuits in the arithmetic unit, and backplane of the Model 980B. The content and use of these lists are described.

4.2.9 LOGIC DOCUMENTATION LIST (943012-9706)

The documentation list, otherwise known as the logic implementation list, is included in this manual of the Model 980B maintenance manuals. The content and use of this list is further defined at the beginning of this manual.

4.3 PERIPHERAL DOCUMENTATION

Separate documentation is delivered to the customer for each peripheral device that is included in the Texas Instruments Model 980B Computer System. When applicable, this documentation includes:

1. Installation Instructions

2. Operating Instructions

3. Peripheral Device Specifications

4. Interface and Controller Specifications

5. Controller Maintenance Instructions

6. Drawings and Parts Lists

7. Logic Implementation List

8. Performance Demonstration Test

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.

- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.

- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.

- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word "See" followed by the referenced entry.

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USER'S RESPONSE SHEET

Manual Title: Model 980B Computer Maintenance Manual

System Description (943012-9701)

Manual Date: 1 May 1977 _____ Date of This Letter: _____

User's Name: _____ Telephone: _____

Company: _____ Office/Department: _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

Location in Manual   **Comment/Suggestion**

_____   _____

                       _____

                       _____

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_____   _____

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                       _____

                       _____

_____   _____

                       _____

                       _____

                       _____

NO POSTAGE NECESSARY IF MAILED IN U.S.A.
FOLD ON TWO LINES (LOCATED ON REVERSE SIDE), TAPE AND MAIL

CUT ALONG LINE

980B COMPUTER SYSTEM HARDWARE MANUALS

```
743 KSR                    743 KSR
                           OPERATION
947976-9701                984030 9701

                           743 KSR
                           MAINTENANCE
                           984025-9701

COMMUNICATIONS            733 ASR/KSR
MODULE                    OPERATION
966643-9701               959227-9701

AU AND        CPU PERFORMANCE   733 ASR        733 ASR/KSR
CONTROL       ASSURANCE         733 KSR        MAINTENANCE
CONSOLE       TESTS
960699-9702   961961-9770       943009-9701    960129-9701

960B/980B                                       DRAWINGS
POWER                     33 ASR                FOR
SUPPLY                                          980 TERMINALS
942773-9703               943011-9701           943010-9701

CENTRAL       PARTS LISTS
PROCESSING    AND                               912 DISPLAY
UNIT (CPU)    ASSY DWGS       912 DISPLAY       MAINTENANCE
              943012-9703     943014-9701       942762-9701

INSTALLATION
PROCEDURE
7
943007-9701

              ELECTRICAL    INPUT/OUTPUT      SILENT 700
              DRAWINGS      DATA BUS          AND TTY

              943012-9704                     966315-9701

980B                        INPUT/OUTPUT
SYSTEM                      MANUAL
DESCRIPTION
943012-9701   I/O AND I/O   960694-9701       CARD
              EXPANSION                       READER
              DRAWINGS
              960699-9704                     944803-9701

INSTALLATION  LOAD, PIN                       PAPER
PROCEDURE     AND WIRE                         TAPE
8             LISTINGS                         READER
943008-9701   943012-9705                     965945 9701

              LOGIC                           PAPER
              DOCUMENTATION                   TAPE
              LISTING                         PUNCH
              943012-9706                     965944-9701

              MEMORY, MEMORY                  I/O DATA
              CONTROLLER                      MODULE
              AND DMAC
              943012-9702                     965956-9701

              DIRECT MEMORY                   SYNCHRONOUS
              ACCESS CHANNEL  (TO OTHER       COMMUNICATION
              (DMAC)          DMAC MANUALS)   MODULE
              966312-9701                     943006-9701

                                              INTERVAL
                                              TIMER
                                              943001-9701
```

(B-130951C)