TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Direct Memory Access Port Expander

Maintenance Manual

MANUAL NO. 216759-9701
ORIGINAL ISSUE 15 SEPTEMBER 1970
REVISED AND REISSUED 1 JANUARY 1977

Digital Systems Division

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES DESTROY SUPERSEDED PAGES

Note: The portion of the text affected by the changes is indicated by a vertical bar in the outer margins of the page.

Direct Memory Access Port Expander
Maintenance Manual (216759-9701)

Original Issue . . . . . 15 September 1970
Revised and Reissued . . . . . 15 May 1974 (ECN 384469)
Revised and Reissued . . . . . 1 May 1976 (ECN 408281)
Revised and Reissued . . . . . 1 January 1977 (ECN 419660)

Total number of pages in this publication is 100 consisting of the following:

PAGE NO.	CHANGE NO.	PAGE NO.	CHANGE NO.	PAGE NO.	CHANGE NO.
Cover	0				
Eff. Pages	0				
iii - iv	0				
1-1 - 1-10	0				
2-1 - 2-8	0				
3-1 - 3-8	0				
4-1 - 4-2	0				
5-1 - 5-44	0				
6-1 - 6-20	0				
User's Resp . . .	0				
Bus. Reply	0				
Cover Blank . . .	0				
Cover	0				

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

INTRODUCTION

1.1 SCOPE OF MANUAL

This manual provides a description of the Direct Memory Access Port (DMAP) Expander. The expander consists of four printed wiring board assemblies. The description includes a brief discussion of the functional characteristics of the DMAC, and items which are pertinent to the interfacing of device controllers to the expander.

1.2 REFERENCE DOCUMENTS

1.2.1 DEVICE CONTROLLERS

Details of device controllers, which interface to the DMAC, are contained in a separate manual for each controller. The Direct Memory Access Channel Controller Manual, Part Number 966312-9702, also contains a brief introduction to each controller.

1.2.2 OTHER DMAC HARDWARE

The Direct Memory Access Channel Manual, Part Number 966312-9701, contains an introduction to the various pieces of hardware which are utilized in implementing a computer system with the DMAC expander.

1.2.3 DMAC EXPANDER CONFIGURATIONS

The various motherboards and chassis which have been assembled with the four expander cards and the device controllers, are documented in addendums to this manual. Each addendum contains a separate configuration with a figure depicting the card location and a LOAD LIST, for documenting the wiring of the motherboard which interconnects the expander to the device controllers. See table 6-1 for a list of the manual addendums.

1.3 GENERAL DESCRIPTION

The Direct Memory Access Port Expander is implemented on the following four printed wiring board assemblies.

Expander	Part Number
No. 1	216700-0001
No. 2	216703-0001
No. 3	216706-0001
No. 4	216709-0001

Of the four, two boards (No. 1 and No. 2) are double-ended, with edge connectors for the cable which interfaces the expanders to the DMA port of the computer. The other two boards (3 and 4) are single-edge connector boards.

1.4 FUNCTION

The function of the logic contained on the four expander cards is to expand the single DMA port of the 960 series or 980 series computers to eight ports, each port being functionally identical to the single port. The expander allows up to eight DMA device controllers to operate on a priority cycle stealing basis with the CPU. The expander identifies the device controller which has requested a DMA interrupt by storing a flag for the controller in a fixed memory location prior to further memory access by the CPU after the interrupt has been recognized by the CPU.

1.5 ELECTRICAL DESCRIPTION

1.5.1 SIGNAL CHARACTERISTICS

Signal levels are compatible with Texas Instruments Series 54/74 transistor-transistor logic (TTL) circuits. The logic ZERO (low) level is 0.0 to +0.4 volts dc. The logic ONE (high) level is +2.4 to +5.0 volts dc.

1.5.2 SIGNALS FROM CPU

Signals originating in the CPU that are buffered and/or used by the Expander and routed to the device controllers are given in table 1-1. Data lines are supplied in the true sense, and all other lines are supplied in the false sense.

Table 1-1. Signals from CPU

Signal	CPU/Expander	Expander/ Controllers
Memory Read Data	17 lines (twisted-pair line)	17 lines
Memory Access Grant	1 line (twisted-pair line)	8 lines
Channel Activate Strobes	2 lines (coaxial cable)	2 lines
Interrupt Acknowledge	1 line (twisted-pair line)	8 lines
Data Available	1 line (coaxial cable)	1 line
Parity Error	1 line (twisted-pair line)	1 line
System Clock	1 line (coaxial cable)	1 line
Master Reset	1 line (coaxial cable)	1 line
Free System Clock	1 line (coaxial cable)	1 line

The interface signals are defined in the following paragraphs. Definitions are the same for both the CPU/Expander Interface and for the Expander/ Controller Interface.

1.5.2.1 MEMORY READ DATA (TRUE SENSE). These lines are data from memory to the device controllers. MRD,00 is the most significant bit; MRD,15 the least significant bit; and MRD,16 the parity bit (odd).

1.5.2.2 MEMORY ACCESS GRANT (FALSE SENSE). As long as Memory Access Grant from the CPU is a logic ZERO, the DMAC may access memory. Once the DMAC acquires memory access, it is maintained as long as a memory access request is present.

1.5.2.3 CHANNEL ACTIVATE STROBES (FALSE SENSE). One strobe accompanies each word of the two-word channel activate sequence. A logic ZERO on one of the strobe lines indicates that the corresponding channel activate word is stable on the read data lines.

1.5.2.4 FREE RUNNING CLOCK (FALSE SENSE). This signal, CK3C1, is a 4-MHz clock just as System Clock, however this clock is not inhibited during CPU memory refresh.

1.5.2.5 INTERRUPT ACKNOWLEDGE (FALSE SENSE). A logic ZERO indicates that the CPU has recognized an interrupt request, that the Expander may store the interrupt word (indicating which channel(s) interrupted), and that the interrupting channel(s) may store status.

1.5.2.6 PARITY ERROR (FALSE SENSE). A logic ZERO indicates that the write data sent to the CPU (on a store cycle) was incorrect. This line is valid logically only when a device controller uses the parity line to the CPU (MWD,16).

1.5.2.7 DATA AVAILABLE (FALSE SENSE). A logic ZERO (strobe) on the Data Available line indicates that the output (read) data lines are stable.

1.5.2.8 SYSTEM CLOCK (FALSE SENSE). The system clock signal line is a 4 MHz clock from the CPU. This clock is a one-third duty cycle clock that remains True for 83 nanoseconds and False for 167 nanoseconds. The clock is modified by certain CPU operations, such as memory refresh cycles, prior to appearing at the interface. Clock variations are illustrated in figure 1-1. Waveforms a through e apply to the 960 CPU and waveforms a and d apply to the 980 CPU.

1.5.2.9 MASTER RESET (FALSE SENSE). This signal line is the master reset for initialization when required.

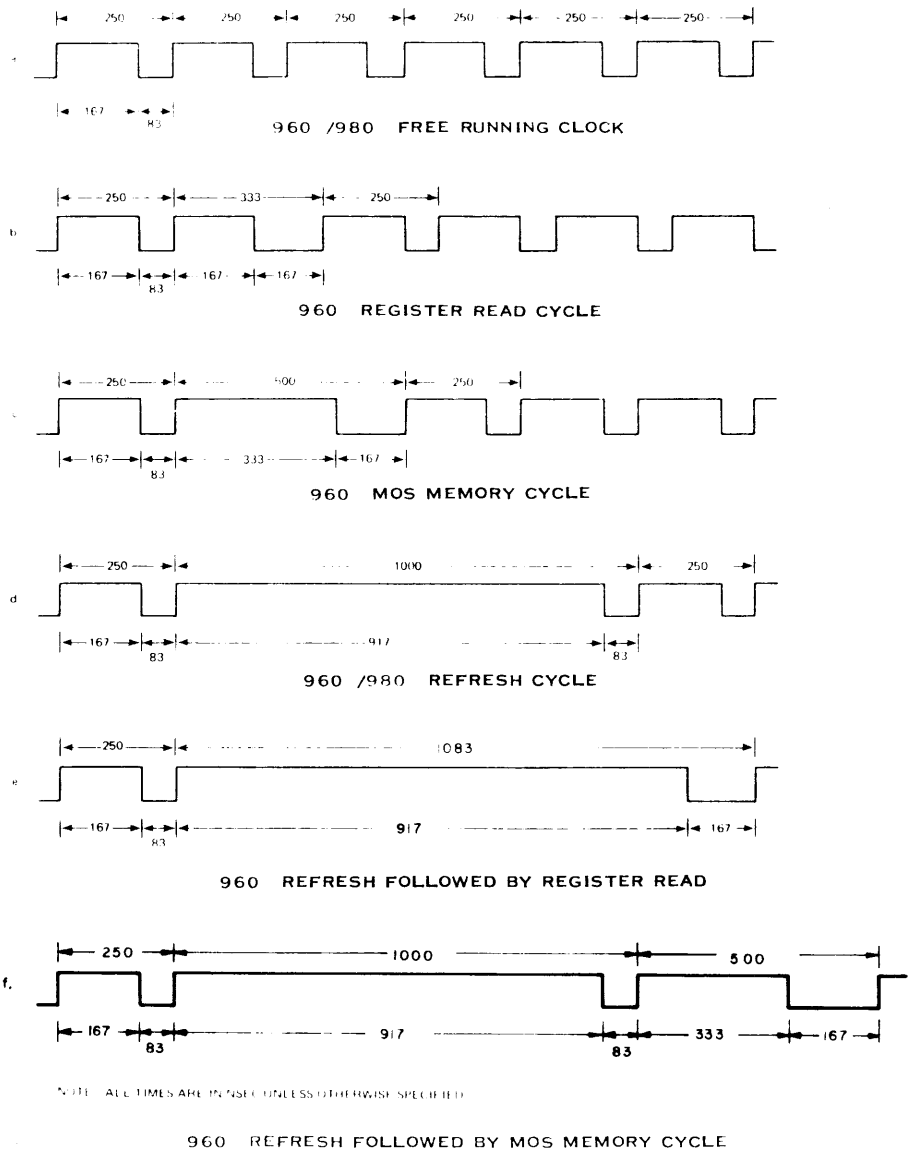


Figure 1-1. Computer Clock Cycle Variations

1.5.3 SIGNALS TO CPU

Signals originating in the device controllers that are buffered and/or used by the Expander and routed to the CPU are listed in table 1-2. Data and address lines are in the true sense and all other lines are in the false sense.

The interface signals are defined in the following paragraphs. Definitions are the same for both the CPU/Expander Interface and for the Expander/Controller Interface.

Table 1-2. Signals to CPU

Signal	CPU/Expander	Expander/ Controller
Memory Write Data	17 lines (twisted-pair line)	17 lines
Memory Address	16 lines (twisted-pair line)	16 lines
Memory Access Request	1 line (twisted-pair line)	8 lines
Interrupt Request	1 line (twisted-pair line)	1 line
Store Cycle Initiate	1 line (coaxial cable)	1 line
Fetch Cycle Initiate	1 line (coaxial cable)	1 line

1.5.3.1 MEMORY WRITE DATA (TRUE SENSE). These lines are input data to memory from the device controllers. MWD,00 is the most significant bit; MWD,15 is the least significant bit; and MWD,16 the parity bit (odd). Supplying the parity bit is optional since parity is generated in the computer before storing in memory. Since these lines are driven by open-collector gates, they are normally high. When being driven, these lines are in the true sense.

1.5.3.2 MEMORY ADDRESS (TRUE SENSE). Memory Address lines are from the device controller to memory. Since these lines are driven by open-collector gates, they are normally high. When being driven, these lines are in the true sense.

1.5.3.3 MEMORY ACCESS REQUEST (FALSE SENSE). A logic ZERO indicates that a memory cycle is being requested by a device controller, or by the Expander. The Expander output is logic ZERO as long as any memory access request from a device controller is a logic ZERO.

1.5.3.4 INTERRUPT REQUEST (FALSE SENSE). A logic ZERO indicates that one or more device controllers has requested an interrupt cycle (recognition) in order to store status. This signal remains a logic ZERO until interrupt recognition is received by the Expander and by the interrupting device controller(s).

1.5.3.5 MEMORY CYCLE INITIATE (FALSE SENSE). A logic ZERO on the STORE or FETCH line initiates the appropriate memory cycle. These lines are given by the open-collector gates to the Expander, but the Expander drives these lines with a power gate into a coaxial cable.

1.5.4 EXPANDER SIGNALS

Table 1-3 is a list of the expander signals that are used to interface the device controllers. These signals are found at the bottom (motherboard) end of the expander cards or at cable ports of some expansion chassis.

1.5.4.1 OUTPUT SIGNAL BUFFERING. All output signal lines should be buffered if the cable length exceeds 6 feet. Memory Read Data, Memory Access Grant, Interrupt Acknowledge, and Parity Error signal lines should be driven into a twisted pair by a noninverting driver (SN7408 or equivalent). Cable lengths of 6 feet or less do not require buffering of these lines. The Channel Activate Strobes, Data Available, System Clock, and Master Reset signal lines require noninverting drivers into 100-ohm coaxial cable. (The characteristic impedance may actually be somewhat less than 100 ohms.) These lines should be buffered regardless of cable length. Refer to figure 1-2.

1.5.4.2 INPUT SIGNAL BUFFERING. Any signal line which is an open-collector output from the external device controller(s) does not require buffering. This includes Memory Write Data, Memory Address, Memory Access Request, and Interrupt Request signal lines. The Store Cycle Initiate and the Fetch Cycle Initiate signal lines should be driven by the external device controller(s) into 100-ohm coaxial cable and terminated with 100-ohm parallel termination, then redriven by a (net) noninverting open-collector driver. Cable length should never exceed 20 feet.

1.5.5 POWER REQUIREMENTS

The DMAP Expander logic requires a maximum of 3.0 amperes at 5 volts dc. The logic for the standard DMAC Expansion Option (exclusive of cable port buffering) requires a maximum of 11.0 amperes at 5 volts dc.

Table 1-3. Expander Bottom Edge Signal Connections

Signature	Connector	Pin	Description/Comment
AG,0-	CB004	6	Access Grant, Channel 0
AG,1-	CB003	57	Access Grant, Channel 1
AG,2-	CB004	3	Access Grant, Channel 2
AG,3-	CB004	7	Access Grant, Channel 3
AG,4-	CB004	5	Access Grant, Channel 4
AG,5-	CB004	8	Access Grant, Channel 5
AG,6-	CB004	28	Access Grant, Channel 6

Table 1-3. Expander Bottom Edge Signal Connections (Continued)

Signature	Connector	Pin	Description/Comment
AG,7-	CB004	17	Access Grant, Channel 7
IRECOG,0-	CB003	61	Interrupt Recognition, Channel 0
IRECOG,1-	CB003	63	Interrupt Recognition, Channel 1
IRECOG,2-	CB003	67	Interrupt Recognition, Channel 2
IRECOG,3-	CB003	65	Interrupt Recognition, Channel 3
IRECOG,4-	CB003	59	Interrupt Recognition, Channel 4
IRECOG,5-	CB003	75	Interrupt Recognition, Channel 5
IRECOG,6-	CB003	54	Interrupt Recognition, Channel 6
IRECOG,7-	CB003	53	Interrupt Recognition, Channel 7
ARDEV,0-	CB004	51	Memory Access Request, Channel Channel 0
ARDEV,1-	CB004	49	Memory Access Request, Channel 1
ARDEV,2-	CB004	58	Memory Access Request, Channel 2
ARDEV,3-	CB004	52	Memory Access Request, Channel 3
ARDEV,4-	CB004	75	Memory Access Request, Channel 4
ARDEV,5-	CB004	69	Memory Access Request, Channel 5
ARDEV,6-	CB004	73	Memory Access Request, Channel 6
ARDEV,7-	CB004	74	Memory Access Request, Channel 7
DEVMWD,00	CB002	19	Write Data (to Memory) (MSB)
DEVMWD,01	CB002	21	Write Data
DEVMWD,02	CB002	22	Write Data
DEVMWD,03	CB002	23	Write Data
DEVMWD,04	CB002	73	Write Data
DEVMWD,05	CB002	76	Write Data

Table 1-3. Expander Bottom Edge Signal Connections (Continued)

Signature	Connector	Pin	Description/Comment
DEVMWD,06	CB002	71	Write Data
DEVMWD,07	CB002	69	Write Data
DEVMWD,08	CB002	70	Write Data
DEVMWD,09	CB002	72	Write Data
DEVMWD,10	CB002	68	Write Data
DEVMWD,11	CB002	66	Write Data
DEVMWD,12	CB002	9	Write Data
DEVMWD,13	CB002	11	Write Data
DEVMWD,14	CB002	14	Write Data
DEVMWD,15	CB002	15	Write Data (LSB)
DEVMWD,16	CB002	52	Write Data (Parity)
DEVMRD00	CB001	75	Read Data (from Memory) (MSB)
DEVMRD01	CB001	64	Read Data
DEVMRD02	CB001	76	Read Data
DEVMRD03	CB001	49	Read Data
DEVMRD04	CB001	55	Read Data
DEVMRD05	CB001	45	Read Data
DEVMRD06	CB001	73	Read Data
DEVMRD07	CB001	58	Read Data
DEVMRD08	CB001	74	Read Data
DEVMRD09	CB001	51	Read Data
DEVMRD10	CB001	43	Read Data
DEVMRD11	CB001	54	Read Data
DEVMRD12	CB001	66	Read Data
DEVMRD13	CB001	69	Read Data
DEVMRD14	CB001	61	Read Data
DEVMRD15	CB001	41	Read Data (LSB)
DEVMRD16	CB001	40	Read Data (Parity)

Table 1-3. Expander Bottom Edge Signal Connections (Continued)

Signature	Connector	Pin	Description/Comment
DEVATI1-	CB001	35	DMAC Activate Strobe (No. 1)
DEVATI2-	CB001	38	DMAC Activate Strobe (No. 2)
DATAV-	CB001	37	Data Available (with Fetch Cycle)
PARERR-	CB001	39	Parity Error (on Store Cycle)
CLOCK-	CB001	7	System Clock
RESET-	CB001	29	Master Reset
DEVFETCH-	CB001	16	Fetch Cycle Initiate
DEVSTORE-	CB001	18	Store Cycle Initiate
DEVADD,00	CB002	35	Memory Address (MSB)
DEVADD,01	CB002	56	Memory Address
DEVADD,02	CB002	50	Memory Address
DEVADD,03	CB002	55	Memory Address
DEVADD,04	CB002	16	Memory Address
DEVADD,05	CB002	20	Memory Address
DEVADD,06	CB002	6	Memory Address
DEVADD,07	CB002	3	Memory Address
DEVADD,08	CB002	8	Memory Address
DEVADD,09	CB002	4	Memory Address
DEVADD,10	CB002	5	Memory Address
DEVADD,11	CB002	7	Memory Address
DEVADD,12	CB002	12	Memory Address
DEVADD,13	CB002	10	Memory Address
DEVADD,14	CB002	13	Memory Address
DEVADD,15	CB002	17	Memory Address (LSB)
INTDEV,0-	CB001	57	Interrupt Request, Channel 0
INTDEV,1-	CB001	70	Interrupt Request, Channel 1
INTDEV,2-	CB004	56	Interrupt Request, Channel 2
INTDEV,3-	CB004	60	Interrupt Request, Channel 3

Table 1-3. Expander Bottom Edge Signal Connections (Continued)

Signature	Connector	Pin	Description/Comment
INTDEV,4-	CB004	71	Interrupt Request, Channel 4
INTDEV,5-	CB004	68	Interrupt Request, Channel 5
INTDEV,6-	CB004	55	Interrupt Request, Channel 6
INTDEV,7-	CB004	26	Interrupt Request, Channel 7
CK3OUT-	CB001	50	Free running clock (4 MHz)

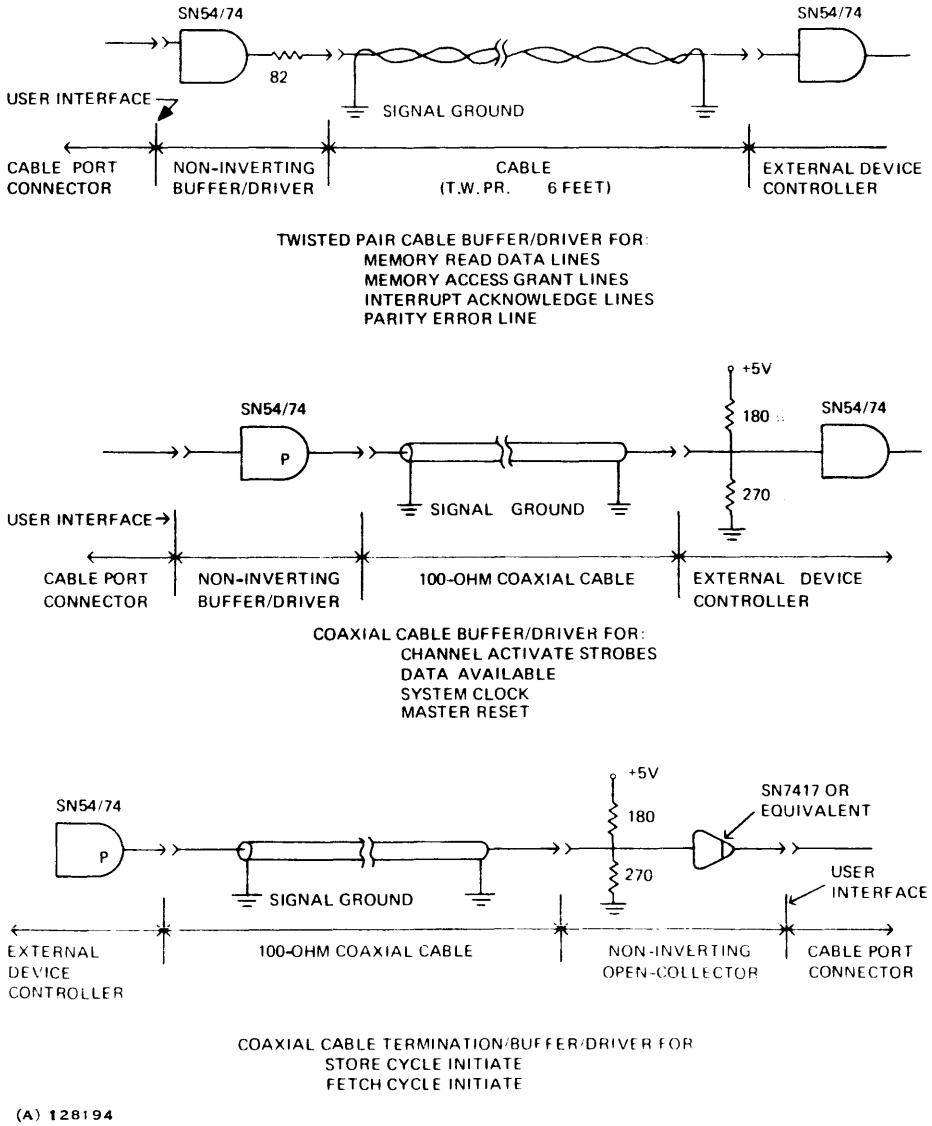


Figure 1-2. Cable Port Signal Buffering

SECTION II

DIRECT MEMORY ACCESS CHANNEL

2.1 GENERAL

The Direct Memory Access Channel for the Texas Instruments Model 960 and Model 980 Computers provides a means of transferring data between the computer memory and one or more peripheral devices. This capability is provided by:

- Direct Memory Access Channel Interface card in the 960 or 980 computer
- Direct Memory Access Port Expander
- Individual device controllers.

Refer to figure 2-1 for a functional block diagram of the Direct Memory Access Channel.

The DMAC Interface card in the 960 or 980 computer accepts signals from a device controller or from the DMAP Expander. The DMAP Expander enables the multiplexing of a maximum of eight device controllers into a single computer port.

The Central Processor Unit (CPU) communicates with the peripheral device controllers on the DMAC via an Automatic Transfer Instruction (ATI) in the 980 computer or an Activate Direct Access Channel (ADAC) command in the 960 computer. The device controllers communicate with the CPU via an interrupt request/acknowledge scheme.

Data transfer between memory and a peripheral device is accomplished on a memory cycle request basis. The Direct Memory Access Channel has priority over the CPU when both require memory access simultaneously.

Memory request from both the CPU and the DMAC are monitored by the memory controller of either the 960 or 980 computers and grant memory cycles to only one source at a time.

2.2 INSTRUCTION FORMAT

The Automatic Transfer Instruction in the 980 computer and the Activate Direct Access Channel Command in the 960 computer consist of two memory words. The format is given in the following two paragraphs.

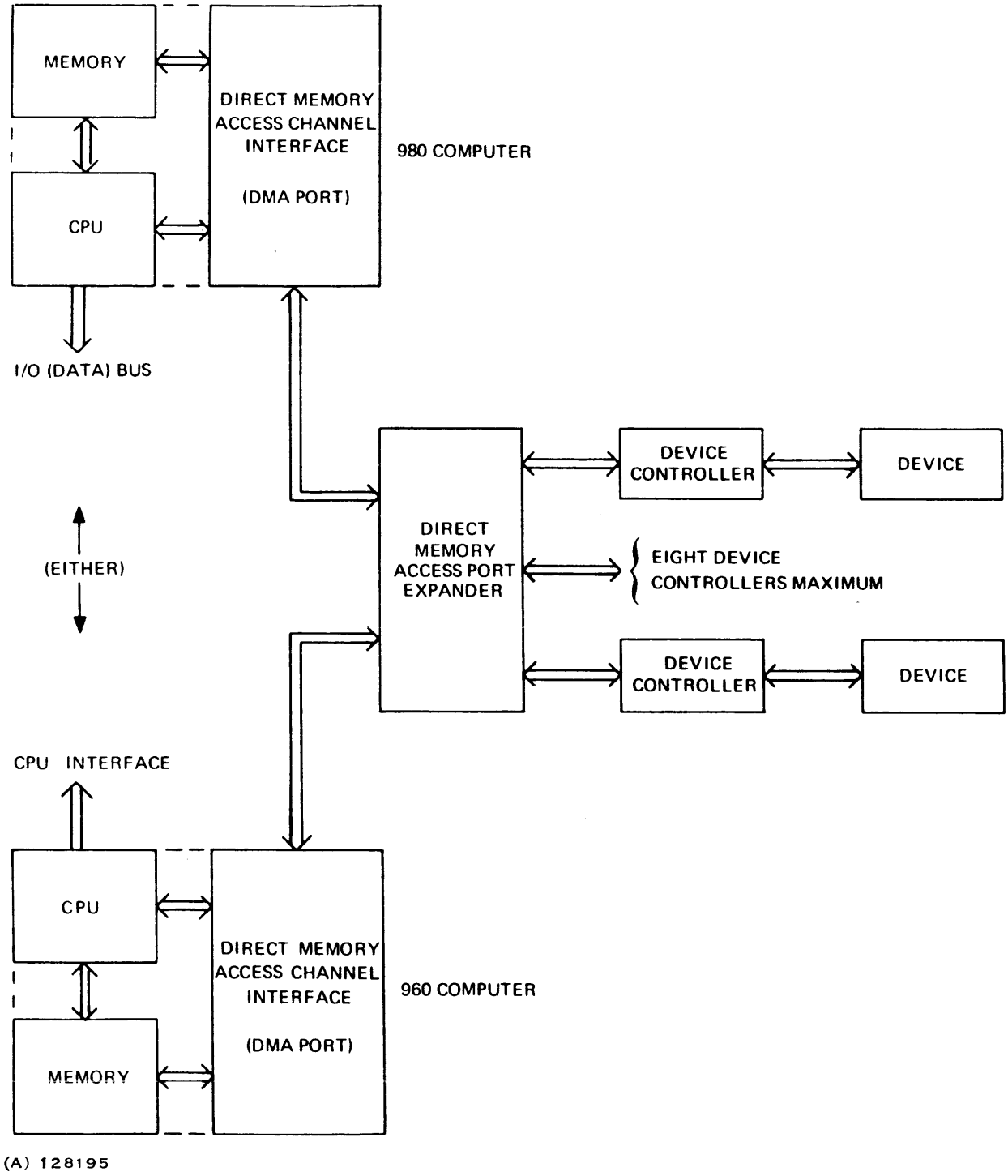
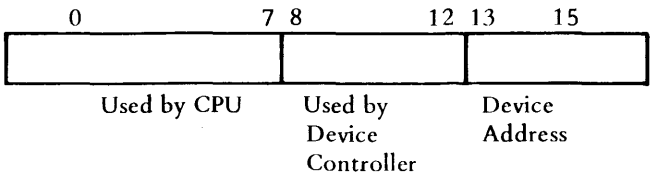


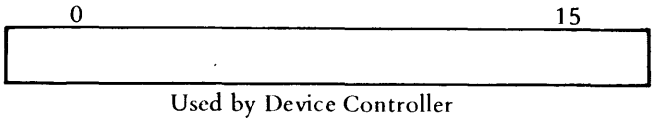
Figure 2-1. Direct Memory Access Channel

2.2.1 FIRST WORD



When the first word is stable on the read data lines from the CPU, a strobe is generated that instructs each device controller to decode the device address bits (13 through 15) to determine which device is being addressed. Bits 8 through 12 are accepted by a device controller only if those bits are defined for that device.

2.2.2 SECOND WORD



When the second word is stable on the read data lines, the CPU generates a second strobe which instructs the device addressed by the first word to accept the second word of the instruction. The second word may be defined as anything that is appropriate to a given controller. In general, this word is the address in memory of an initialization list for the addressed device controller.

All device address decoding is performed by the device controllers. They accept the appropriate bits of the first and second words when the corresponding strobes so indicate.

2.3 MEMORY ACCESS PRIORITY

The Expander accepts memory access requests from the device controller and in turn requests memory access from the computer. When memory access is granted by the computer, the device controllers are granted memory access on a priority basis. Channel 0 has the highest priority, and Channel 7 has the lowest priority. The memory access request from the Expander to the computer is the logical sum of the requests from the device controllers. The computer memory controller cannot distinguish between device memory access requests. The DMAC has priority over the CPU when both require memory access simultaneously.

2.4 INTERRUPTS/STATUS

The peripheral device controllers may interrupt the program being executed by the CPU at any time.

The device controller issues an interrupt request indicating the controller status needs to be processed by the CPU. The interrupt request from the device controller is registered by the Expander and an interrupt request is forwarded to the CPU. The interrupt request to the CPU is the logical sum of the interrupt requests from all device controllers. The Expander and each device controller must wait for an interrupt recognition signal before taking further action on an interrupt cycle. However, data transfers may be continued.

In order that interrupt recognition may be received by the DMAC device controller(s), the DMAC interrupt bit in the CPU status register must be armed, and the CPU must have trapped to the DMAC interrupt trap location. An interrupt request remains until interrupt recognition is received.

When interrupt recognition is received by the Expander, a memory access request is generated which has priority over all channel data transfer requests. The Expander has the next memory cycle available and uses this memory cycle to store the interrupt word in memory (location 0096_{16}). This word indicates which device controller(s) have interrupted by containing a logical ONE in each bit position corresponding to a channel whose interrupt request has been registered. That is, Bit 0 indicates that Channel 0 has interrupted, Bit 7 indicates that Channel 7 has interrupted, etc. Bits 8 through 15 are always zero.

As the Expander stores the interrupt word in memory, it also issues an interrupt recognition signal to each device controller whose interrupt request bit was present in the interrupt word. Once a device controller receives an interrupt recognition, it issues a normal memory access request and stores the status when memory access is granted through the channel priority scheme.

There is no priority among interrupt requests, the Expander registering all requests until interrupt recognition is received. However, storing of the interrupt (request) word does have priority over data transfer (memory access) requests.

If interrupts are not enabled within the controller, a device controller stores status through a normal memory (access request) cycle without issuing an interrupt.

Table 2-1 gives the memory locations in both the 960 and the 980 computers that are reserved for interrupt and status information storage. Device status is always stored in the even (lower) location of each pair. The odd location of each pair may be used for information pertinent to a device controller at the time of status storage.

Table 2-1. Pre-Assigned DMA Status Storage Locations

Hexadecimal Location	Use
96	DMAC interrupt word Bits 0 through 7 indicate that the corresponding channel has interrupted. Bits 8 through 15 are always zero.
98, 99	Status, Channel 0
9A, 9B	Status, Channel 1
9C, 9D	Status, Channel 2
9E, 9F	Status, Channel 3
A0, A1	Status, Channel 4
A2, A3	Status, Channel 5
A4, A5	Status, Channel 6
A6, A7	Status, Channel 7

2.5 DATA TRANSFER CAPABILITY

2.5.1 SINGLE CHANNEL

When transferring data between memory and a single device, the maximum data transfer rate is 10^6 words/second. A maximum of 1 microsecond is required to obtain memory access after a request is issued to the computer.

NOTE

Memory time allocations for refresh of semiconductor memories are not added into the listed access and transfer rates.

2.5.2 ALTERNATE CHANNELS

When more than one device controller is requesting memory access for one memory cycle at a time, the maximum data transfer rate is 8×10^5 words/second. This maximum transfer rate is achieved when memory cycle requests overlap, thus preventing the CPU from acquiring memory access. If the device controller memory cycle requests do not overlap, 1.25 microseconds maximum are required to gain access for each request.

2.6 CONTROLLER INTERFACE TIMING

Requests for memory access and an interrupt cycle may be issued by the device controllers at any time. The time that elapses before a memory cycle execution begins, or before interrupt recognition is dependent on the activity of the other device controllers, the Expander and the CPU. Refer to figure 2-2 for a definition of the signal relationship at the device controller interface.

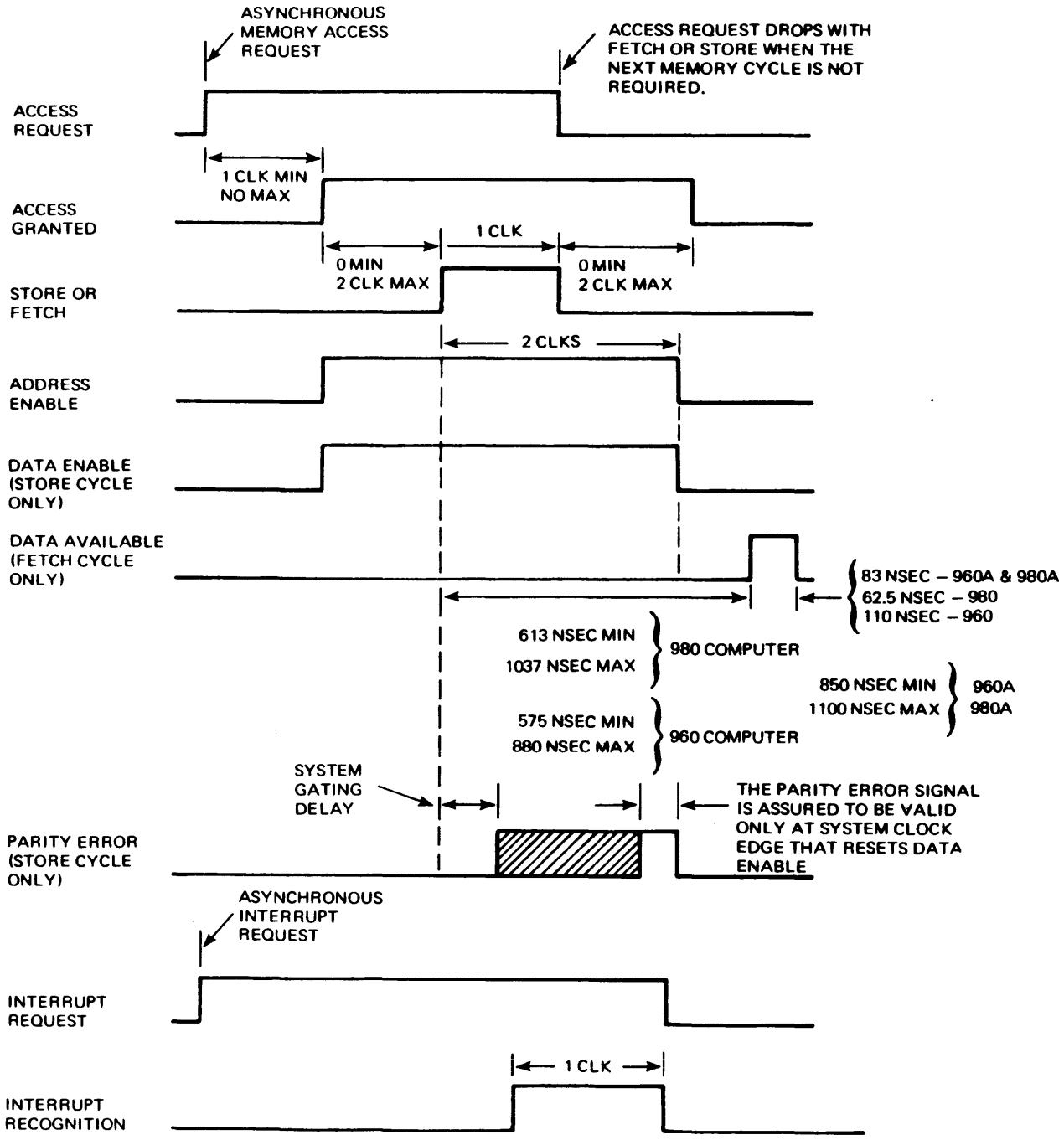
NOTE

All direct DMAC interfacing should use system clocks to achieve memory cycle stealing because of modification to the clock for such things as refreshing the semiconductor memory.

2.7 CHANNEL ADDRESSING

A device controller may be assigned any desired channel address as long as sufficient consideration is given to the system and operational aspects of the assignment. That is, the highest speed device controller, with respect to data transfer to or from memory, should be assigned the channel address with highest priority (Channel 0). The other device controllers should be assigned channel addresses of lower priority according to their respective data transfer rates. Channel 7 has the lowest priority.

The channel address assigned to a controller determines how to decode the first ATI or ADAC word device address bits, and where the controller status is to be stored. (Refer to paragraph 2.4.) The channel address also determines which request lines to drive and which acknowledge lines to monitor when using the channel addressing scheme.



NOTES:
1. SIGNALS ARE SHOWN IN THE TRUE SENSE.
2. CONTROLLER INTERFACE IS ASYNCHRONOUS TO THE COMPUTER.
3. SYSTEM CLOCK IS 3MHz (333 NSEC) FOR THE 960 COMPUTER AND 4MHz (250 NSEC) FOR THE 980, 960A, AND 980A COMPUTERS.

(A) 128196

Figure 2-2. Controller Interface Signal Relationship

SECTION III

THEORY OF OPERATION

3.1 GENERAL

The Direct Memory Access Port (DMAP) Expander consists of circuitry required to enable multiplexing of a maximum of eight device controllers into a single channel (port) in the 960 and 980 computer.

The two primary functions of the expander are:

- To monitor and process requests for memory access from the device controllers.
- To monitor and process interrupt requests from the device controllers.

The Expander circuitry provides the logic required to process memory access requests and interrupt requests as well as buffering for all signals between the device controllers and the 960 or 980 computer. Figure 3-1 is a block diagram of the Expander.

3.2 MEMORY ACCESS REQUESTS

Refer to the flow chart shown in figure 3-2. The Expander monitors the memory access request signal [AR, (N=0)] from each device controller. When any one or more devices present an access request, a memory access request signal is sent to the computer (1⟶DMAR). If the interrupt control circuitry indicates a request for an interrupt store cycle (ARINT), it is treated in the same manner as a device request. The interrupt store cycle request has priority over all device memory access requests.

When a memory access is granted by the computer (GRANT), the Expander grants memory access [AG(N=0-7)] to the channel with the highest priority request [XAG, (N=0-7)]. If the interrupt store cycle request (ARINT) is present, the memory access grant goes to the interrupt circuitry (AGINT), and device requests are delayed for one memory cycle. (See paragraph 3-3 for discussion of the interrupt circuitry.)

Once memory access is granted to a channel, the access grant [AG, (N)] may be turned off in two ways. In the first case, the channel with access initiates a memory cycle and then releases its request [AR, (N)]. The synchronized request [AR, (N=0-7)Q] resets the access granted flip-flop for that channel.

The second means of turning off the access grant flip-flop occurs when a device requests more than one memory cycle so that the request is not released after initiating a memory cycle (other than the last). In this case, the STORE or FETCH signal is delayed so that on the second clock after STORE or FETCH, the signal CHANGE, Q becomes true for one clock time.

If at this time a higher priority request is present at the output of the priority tree [XAG, (M<N)]; where N is the channel with memory access and M is the higher priority request], the access grant for channel N is turned off. If a higher priority request is not present, the device with access is permitted to keep memory access until its request is released or a higher priority request is registered. When a channel has memory access and a lower priority request is present, the lower priority request must be delayed until the channel with access releases its request. Once no higher priority channel has access granted, the lower priority channel may receive memory access.

When any channel is granted access, the signal SUMAG becomes a logic ONE and prevents granting of access to any other channel. SUMAG is the logical sum of access grant to all channels (and includes access grant for an interrupt store cycle). When access grant to a channel is turned off, SUMAG becomes a logic ZERO. Two clocks later $\overline{\text{LOADA, Q}}$ becomes a logic ONE which enables memory access to be granted to the highest priority request on the following clock.

As long as a memory access request is present from at least one device controller [AR, (N)], the request signal to the computer (DMAR) remains a logic ONE and the memory controller of the computer continues to grant memory access to the DMAC. Refer to figure 3-3 for an illustration of Expander memory control timing.

3.3 INTERRUPTS

Figure 3-4 is a flow chart of the Expander interrupt circuitry. Each interrupt request line from a device controller [INTDEV, (N)] is monitored at all times except during an interrupt store cycle. When an interrupt request is presented by a controller, the corresponding bit in the interrupt register [INTA, (N)Q] is set to a logic ONE. If the Expander is currently in an interrupt store cycle (AGINT=1), the interrupt register bit is not set until the store cycle is complete (AGINT=0).

Once an interrupt register bit [INTA, (N)] is set to a logic ONE, the corresponding interrupt line monitor [INTB, (N)Q] will reset to a logic ZERO on the following system clock. INTB, (N)Q remains reset until that interrupt request is released [INTDEV, (N)=0] and an interrupt store cycle is completed. This prevents any one interrupt from being registered a second time.

When any interrupt register bit is set, the logical sum of the interrupt register bits (SUMINTA) is sent to the CPU to indicate that at least one device controller has requested an interrupt cycle. SUMINTA remains a logic ONE until an interrupt recognition (INTREC) is received by the Expander. The time required to receive interrupt recognition is dependent on the software being executed, since an interrupt will not be recognized unless the appropriate bit has been set in the CPU status register and the CPU has trapped to the DMAC interrupt trap location.

When interrupt recognition (INTREC) is received from the CPU, and access request for an interrupt store cycle (ARINT, Q) is generated. This memory cycle request is ORed with the memory cycle requests from the device controllers as previously discussed. Since the interrupt store cycle request has the highest memory access priority, the interrupt circuitry will be granted the next available memory cycle (AGINT, Q).

When AGINT, Q is set to a logic ONE, an interrupt store cycle is initiated. The interrupt word (register) [INTA, (N=0-7)Q] is gated on the memory write data (MWD, 00-07) lines (INTA, 0Q⟶MWD, 00; INTA, 1Q⟶MWD, 01; etc.). Memory write data bits 8 through 15 (MWD, 08-MWD, 15) are forced to ZERO. The interrupt word address (hexadecimal 0096) is gated on the memory address lines (MAD, 00-15). The memory store cycle pulse (INTSTORE, Q) is set to logic ONE on the clock following AGINT, Q and remains set for one clock time. As INTSTORE, Q resets to a logic ZERO, interrupt recognition [IRECOG, (N)] is sent to those device controllers whose interrupt (request) bit was registered and stored in memory in location 0096_{16}. Interrupt recognition is also a one clock time signal.

As INTSTORE, Q resets to logic ZERO, interrupt complete signal (ICOMP, Q) is generated causing the interrupt register [INTA, (N)] to be reset on the following clock. As the interrupt register is reset, the interrupt store cycle request (ARINT, Q) and the grant for that cycle (AGINT, Q) are also reset to logic ZERO.

Once an interrupt cycle is complete and the interrupt register is reset, the interrupt requests may once again be registered. However, those interrupt request lines [INTDEV, (N)] that were registered and stored in the interrupt word in memory are inhibited as long as that line remains a logic ONE. That is, an interrupt request from a device controller must be released (reset to logic ZERO) before being enabled and registered again. The inhibit is INTB, (N)Q for each interrupt request line. Figure 3-5 is a timing illustration of the interrupt circuitry.

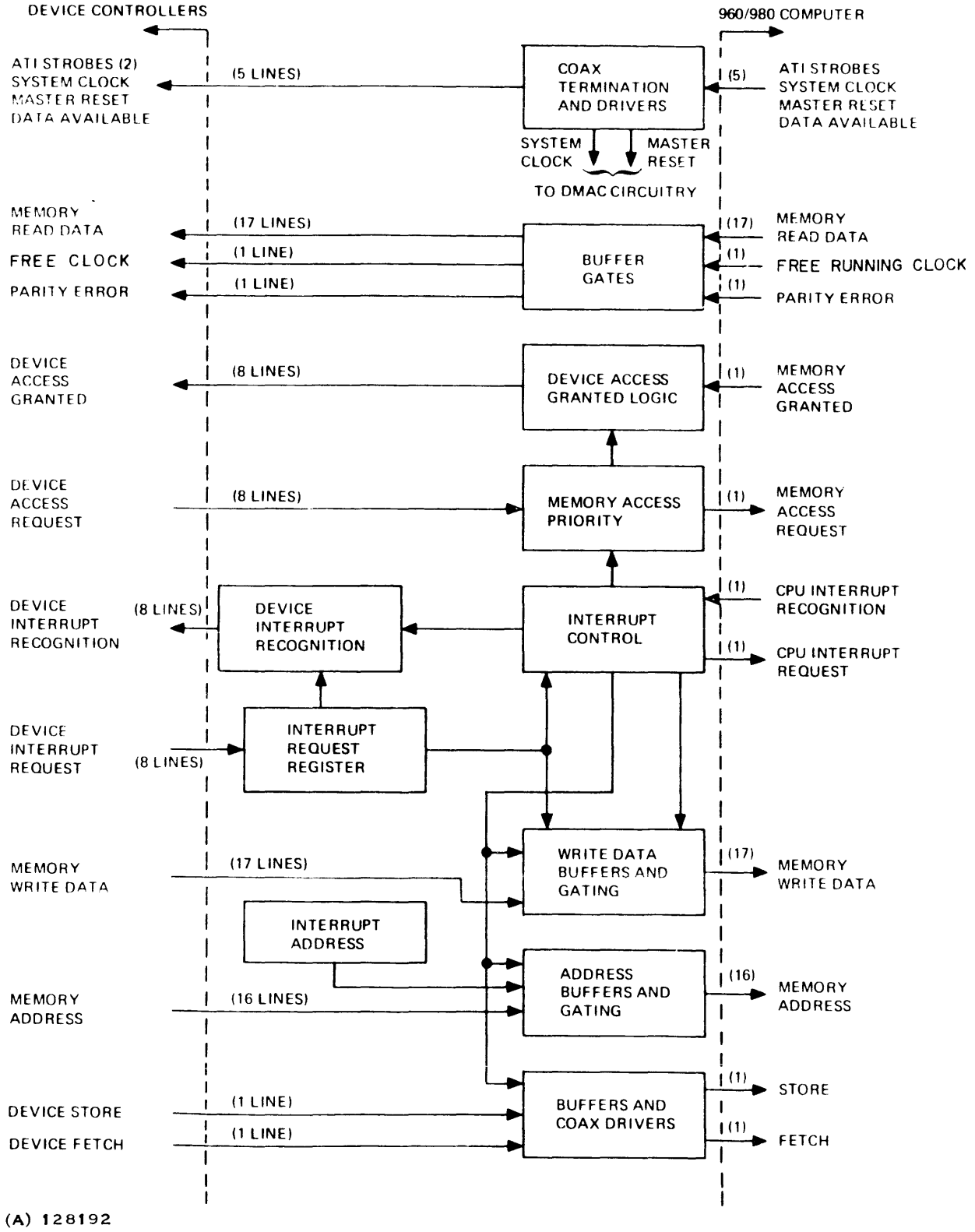


Figure 3-1. DMAP Expander Block Diagram

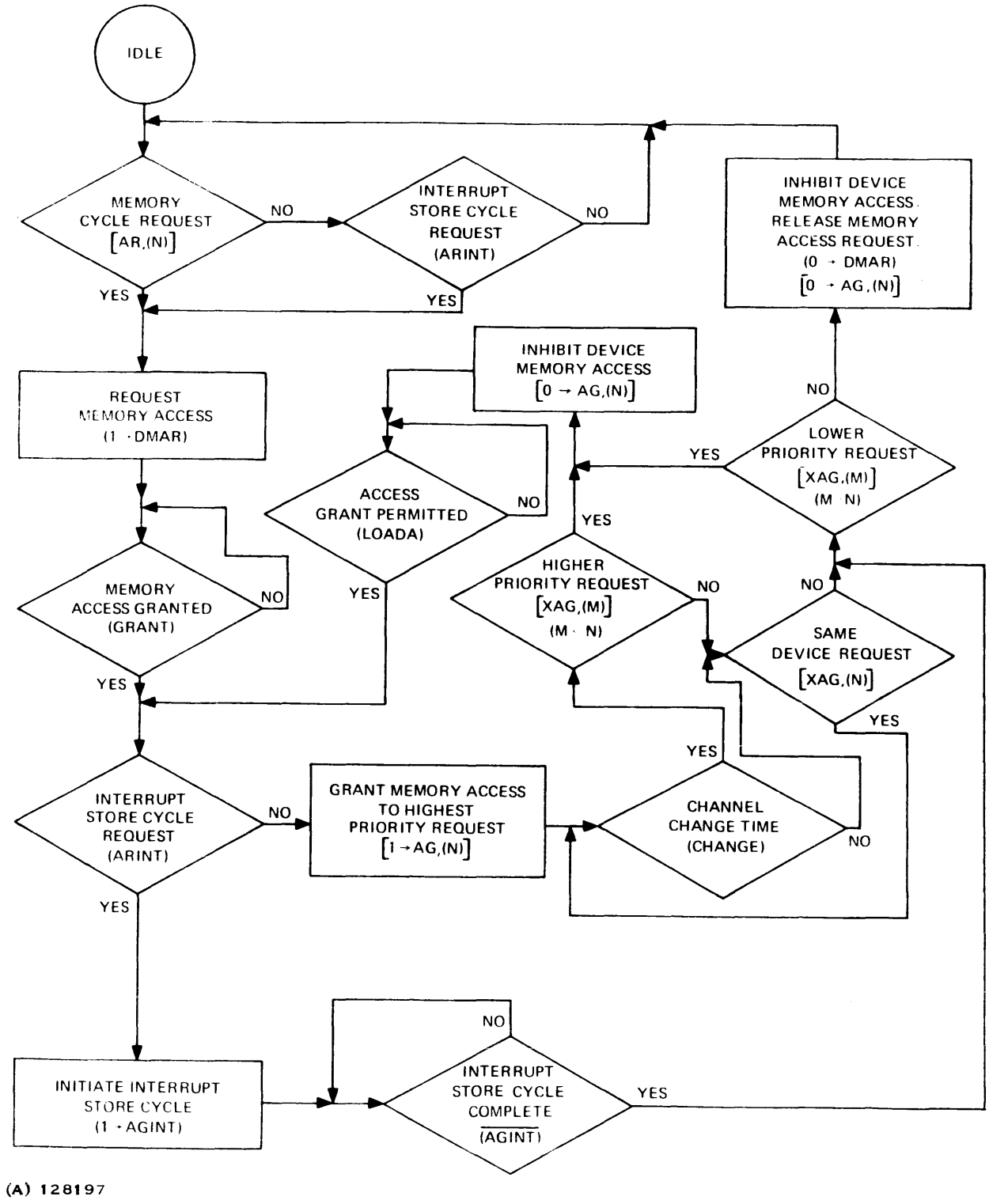
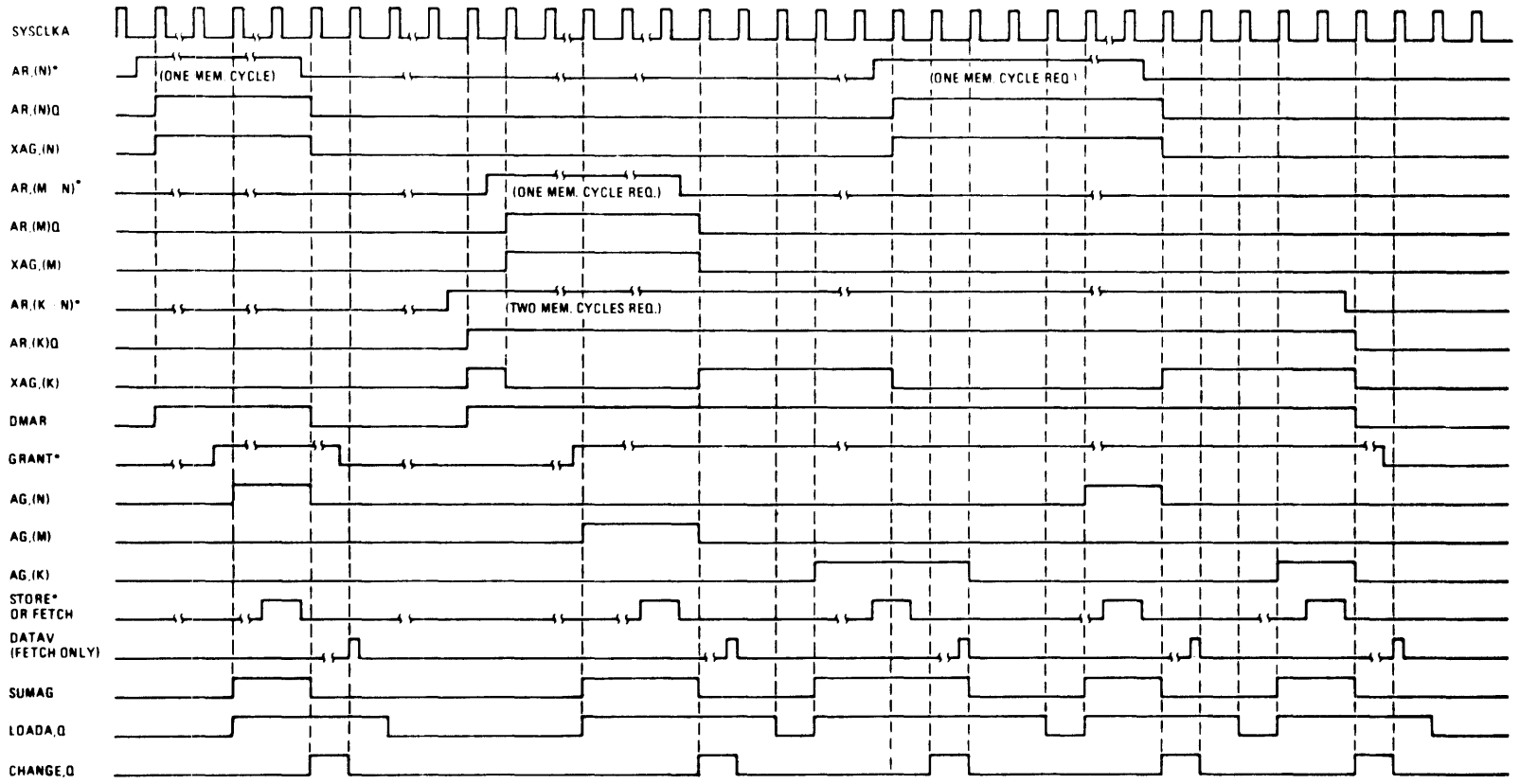


Figure 3-2. DMAP Expander Memory Access Monitor and Control



NOTES

1. SIGNALS MARKED BY AN (*) ARE ASYNCHRONOUS TO THE SYSTEM CLOCK.
2. ILLUSTRATION ASSUMPTIONS

   PRIORITY — CHANNEL M, HIGHEST
   CHANNEL K, LOWEST

   MEMORY REQUESTS — CHANNEL M, 1 REQUEST, 1 CYCLE REQUESTED
   CHANNEL N, 2 REQUESTS, 1 CYCLE PER REQUEST
   CHANNEL K, 1 REQUEST, 2 CYCLES REQUESTED

3. SYSTEM CLOCK IS 4MHz FOR THE 960A AND 980A CPU

(A) 128198

Figure 3-3. Memory Access Timing

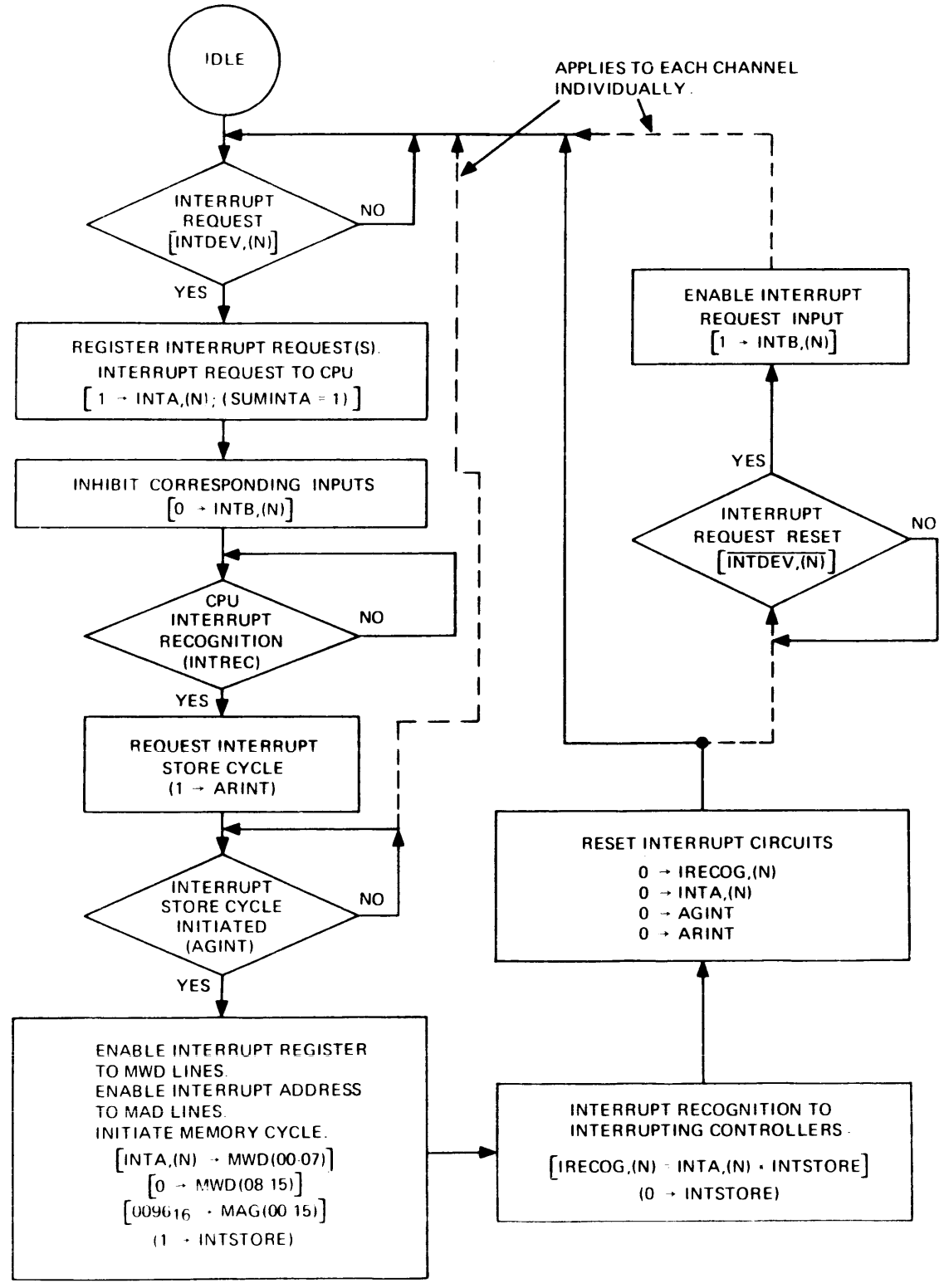
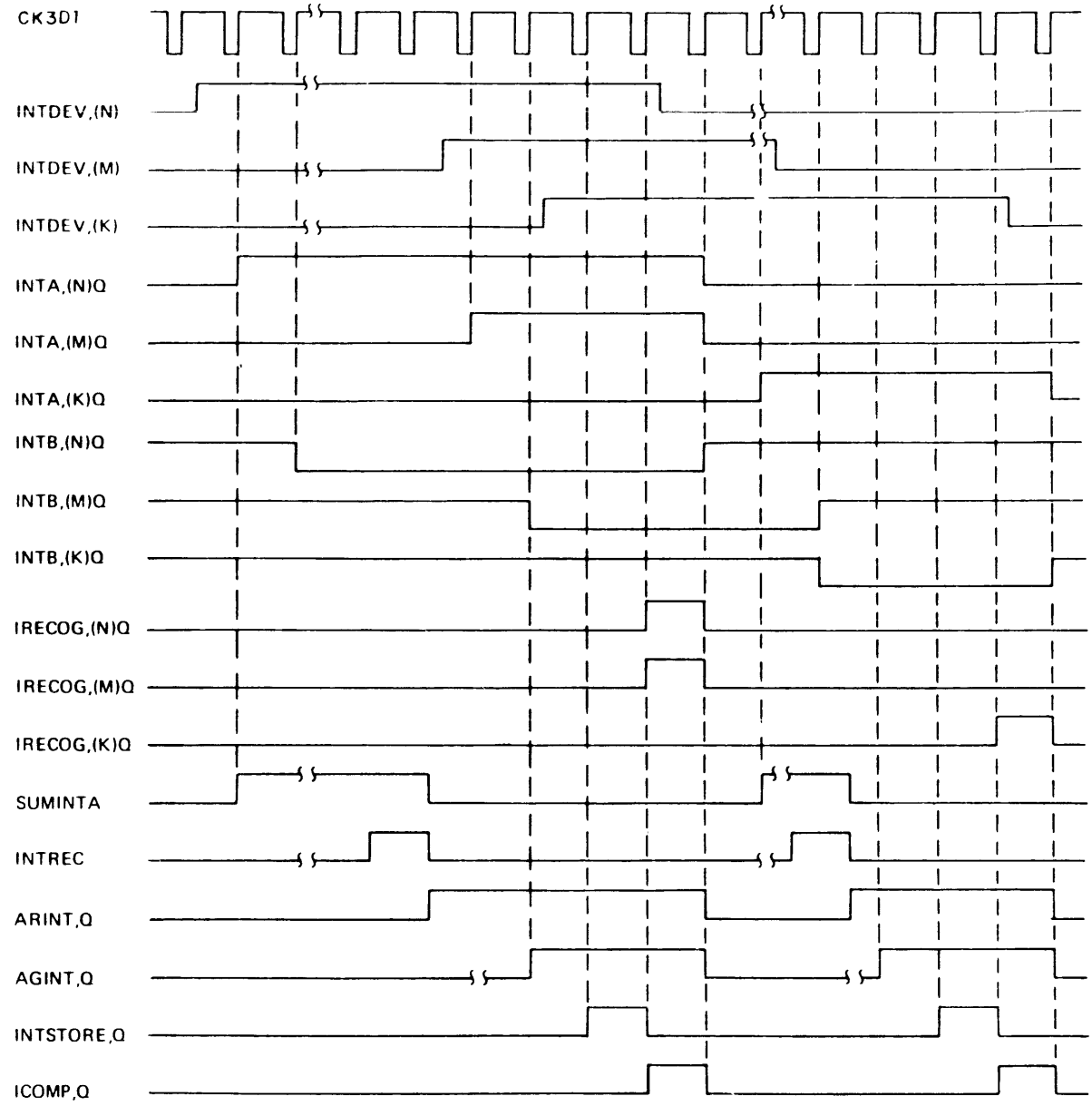


Figure 3-4. Interrupt Request Monitor and Control



NOTE:
1. NO PRIORITY EXISTS BETWEEN INTERRUPTS FROM VARIOUS CHANNELS.
2. DEVICE (M) INTERRUPTS AFTER DEVICE (N) BUT BEFORE THE STORE CYCLE BEINGS. DEVICE (K) INTERRUPTS DURING AN INTERRUPT STORE CYCLE.
3. CK3D1 IS THE 4 MHZ SYSTEM CLOCK.

(A) 128190

Figure 3-5. Interrupt Cycle Timing

SECTION IV

MAINTENANCE

4.1 GENERAL

This section combined with Section V provides the information required to troubleshoot the Expander and related circuitry. These sections include the connector pin numbering and printed circuit board network location designations. Reference figures 4-1, 4-2, and 4-3 to determine network location designation and connector pin numbering as used in the logic diagram.

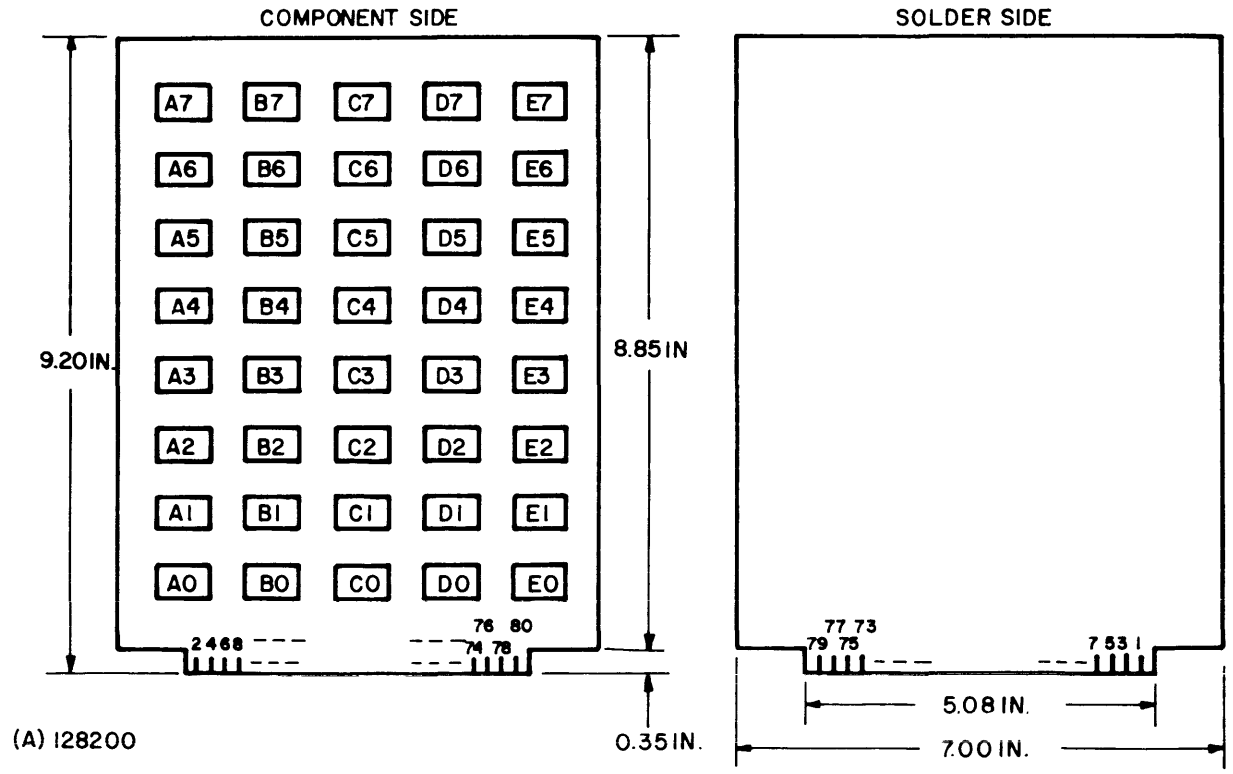


Figure 4-1. Single Connector Type 1 Printed Circuit Board, Outline and Circuit Locations

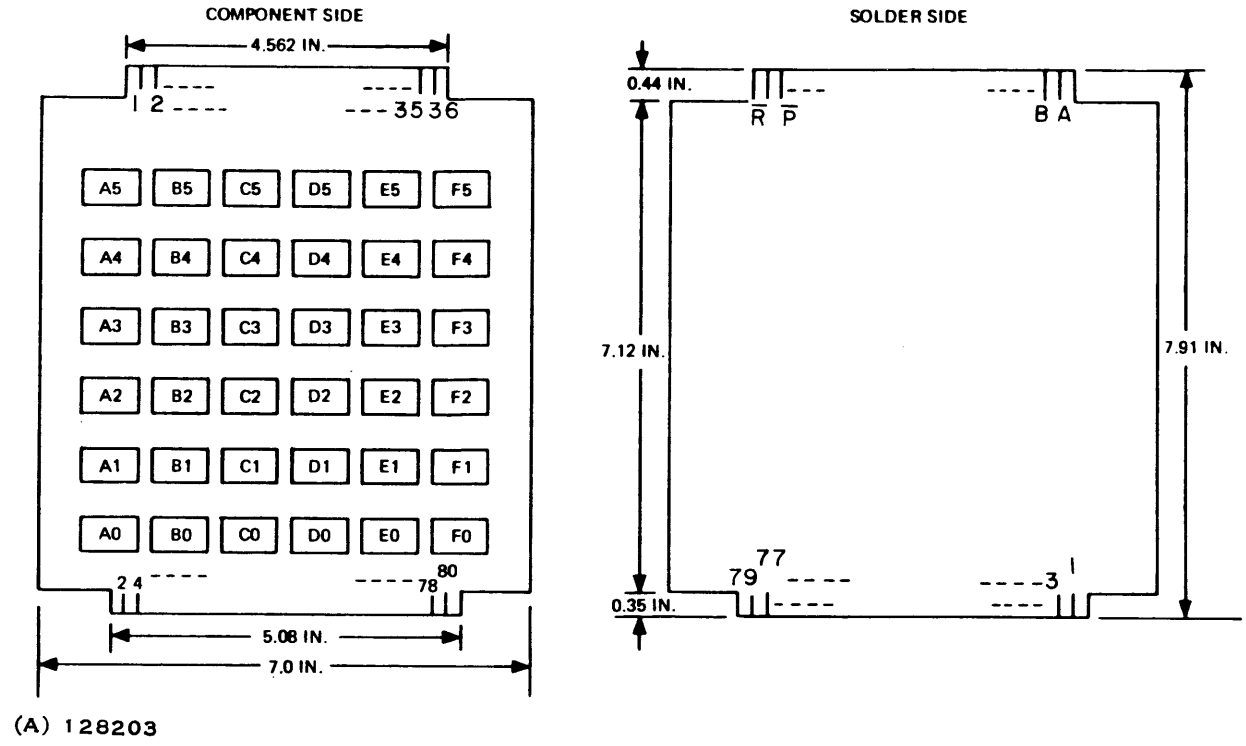


Figure 4-2. Double Connector Type 1 Printed Circuit Board, Outline and Circuit Locations

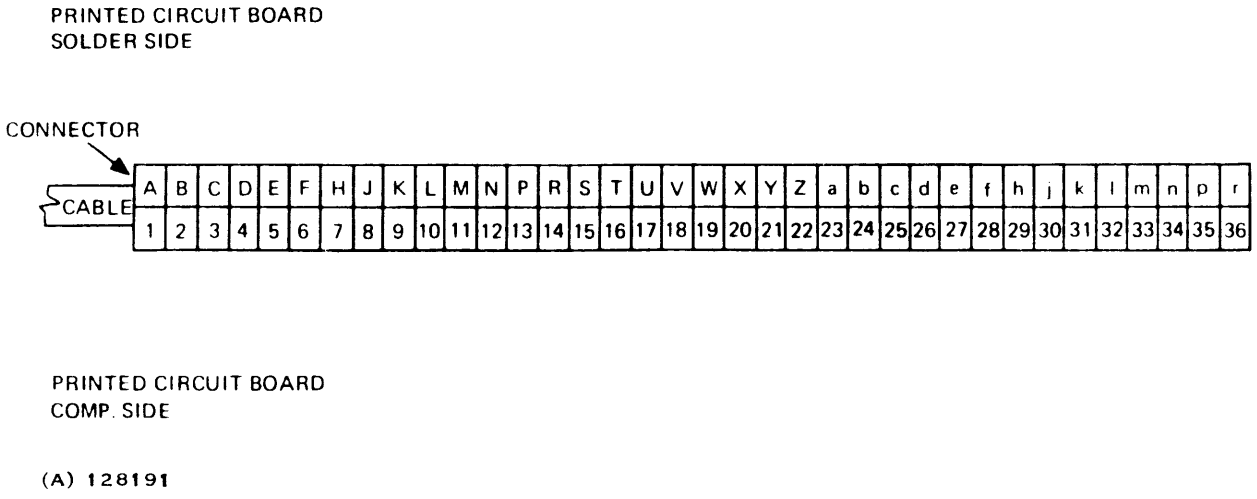


Figure 4-3. Interface Type 1 PC Board Connector, Top Edge Pin Numbering

SECTION V

DRAWINGS

This section contains the assembly drawings for the DMAP Expander printed circuit boards, the CPU to DMAP Expander Cable, and the logic diagrams for the DMAP Expander. Additionally included for reference are the assembly drawing and logic diagram for the DMAC Interface Card. Table 5-1 is a major signature list of the DMAP Expander logic.

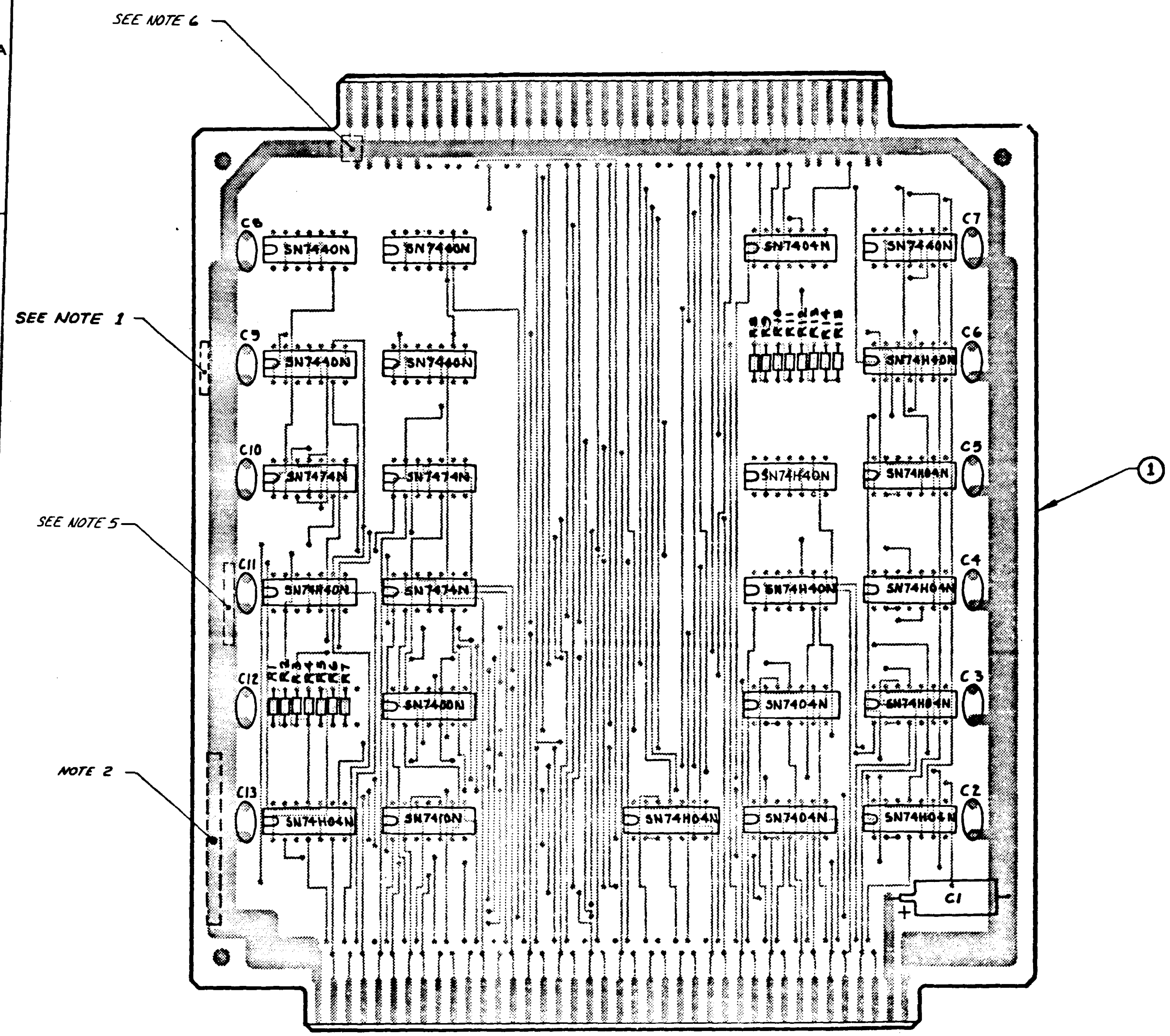
Table 5-1. Major Signature List, DMAP Expander Logic

Signature	Comment/Description
AGINT, Q	Access Grant for an Expander interrupt cycle
AG, (N)Q	Memory Access Grant for channel (N)
AR, (N)	Memory Access Request for channel (N)
ARINT, Q	Memory Access Request by the Expander for an interrupt cycle
ATI1;ATI2	Channel Activate Strobes accompanying first and second words of an Automatic Transfer Instruction (980) or an Activate Direct Access Channel command (960)
CLOCK-	System Clock (from CPU) to the device controllers
CPURUN	Indicates that the CPU is in the RUN mode and not IDLE
DATAV	Data Available
DMAR	DMAC Memory Access Request

Table 5-1. Major Signature List, DMAP Expander Logic (Continued)

Signature	Comment/Description
FETCH	Fetch Cycle Initiate
GRANT	Memory Access Grant from the CPU to the DMAC
ICOMP, Q	Interrupt Cycle complete
INHLOAD, Q-	Enables granting of memory access to the highest priority request
INTA, (N)Q	Interrupt Register, channel (N)
INSTORE, Q	Store Cycle Initiate for storing the Expander interrupt word
IRECOG, (N)Q	Interrupt recognition to Channel (N)
MAD, (N)	Memory Address Lines
MRD, (N)	Memory Read Data Lines
MWD, (N)	Memory Write Data Lines
PARERR	CPU detected a Parity Error on Memory Write Data during a store (DMAC) cycle
RESET-	Master Reset from the CPU to the device controllers
STORE	Store Cycle Initiate
SUMINTA	Logical sum of the controller interrupt requests
XAG, (N)	Output of memory access request priority logic. True output is highest priority request.

D 216700



REV	REVISIONS — DESCRIPTION	DATE	APPD
A	368935 (C) 2/1/71 CHG LM ITEM #7, P/N WAS 233516-3000 ADD: 1) REVION LEVEL BLOCK. 2) NOTE 2. 3) LM ITEM #14.	2-3-71	
B	371837 S. Pierce 1-19-72 REVISED W/CHG., F/D UPDATE TO AGREE W/ARTWORK	1-15-72	
C	374381 (D) S. Pierce 4-6-72 CHG: CLASS OF CHANGE ON DWG REV B, ECN 371837 WAS "E"	4-6-72	
D	368539 (E) 1-24-73 CHG: 1) LOCATION E3, SN74H40N WAS SN7440N. 2) LM ITEM 5, QTY WAS 6. 3) ITEM 13, QTY WAS 3 ADDED: LM ITEM 15.	1/27/73	
E	389028 (C) D Perez 1) ADDED NOTES 3 & 4	2/7/74	
F	388846 (C) 1) ADDED ITEM 16 TO L/M (2) UPDATED REV LEVEL BLK	3-12-74	
G	396476 (C) (1) UPDATED REV LEV BLK (2) ADDED PWB TO REV LEV BLK	4/25/74	
H	394313 (C) (1) ADDED NOTES 5 & 6 CALLOUTS ON F/D (2) UPDATED REV LEVEL BLOCK	7/4/75	
J	383789 (D) (1) UPDATED REV LEVEL BLOCK	11/5/75	
K	412966 (D) (1) UPDATED REV LEVEL BLOCK	5/12/76	

NOTES:
UNLESS OTHERWISE SPECIFIED
1. MARK APPROPRIATE ASSY REV LETTER APPROX WHERE SHOWN PER PROCESS 1 (FARSIDE)
2. MARK THE WORD "LOGIC 217812-9901" AND APPROPRIATE REV LETTER APPROX WHERE SHOWN PER PROCESS 1 (FARSIDE).
3. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF CARD IS .31
4. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF CARD IS .075
5. MARK APPROPRIATE SERIAL NUMBER WHERE SHOWN PER PROCESS 1 (FAR SIDE)
6. MARK LETTER "A" WHERE SHOWN PER PROCESS 1 (FAR SIDE). MARK NUMBER "1" WHERE SHOWN PER PROCESS 1 (COMPONENT SIDE).

REVISION LEVEL

PRINTED WIRING BOARD (216699-0001)									F	F	G	G
LOGIC DIAGRAM FOR -0001 ASSY (217812-9901)	*	A	B	C	C	C	D	E	F	F	-	G
ASSEMBLY	A	A	A	B	C	D	E	F	G	H	J	K

-0002	-0001	ITEM NO	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
QTY REQD							

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED

PROCESSES
1. RUBBER STAMP PER F-100, HEIGHT .12, COLOR BLACK

TEXAS INSTRUMENTS INCORPORATED INDUSTRIAL PRODUCTS DIVISION HOUSTON, TEXAS

BOARD ASSY, EXPANDER #1
DMAC
COMPUTER
SCALE 2:1 | SIZE D | 216700

LM

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/01/75

LIST OF MATERIAL

PAGE 1 of

PART NUMBER LM 216700-0001 REV K

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		216699-0001	PRINTED WIRING BOARD	
0002	00003.000	EA		222222-7404	NETWORK SN7404N	
0003	00001.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0004	00001.000	EA		222222-7410	NETWORK SN7410N	-SN7410N
0005	00005.000	EA		222222-7440	NETWORK SN7440N	-SN7440N
0006	00003.000	EA		222222-7474	NETWORK SN7474N	-SN7474N
0007	00005.000	EA		972975-0031	RES FIX COMP 180 OHMS 5 % 1/8 WATT	QPL- RC05G181JS
0007A					R1,R3,R8,R10,R12	
0008	00005.000	EA		972975-0035	RES FIX COMP 270 OHMS 5 % 1/8 WATT	QPL- RC05G271JS
0008A					R2,R4,R9,R11,R13	
0009	00005.000	EA		972975-0036	RES FIX COMP 300 OHMS 5 % 1/8 WATT	QPL- RC05G301JS
0009A					R5,R6,R7,R14,R15	
0010	00001.000	EA		972924-0015	CAP FIX TANT SOLID 47 MFD 10 % 20 VOLT	QPL-M39003/1-2295
0010A					C1	
0011	00012.000	EA		534348-0001	CAP FIX CERAMIC .10 MF 20/80 % 10V	CRL- UKI0-104
0011A					C2 THRU C13	
0012	00006.000	EA		240000-7404	NETWORK-SN74H04N	
0013	00004.000	EA		240000-7440	NETWORK-SN74H40N	
0014	REF	EA		217812-9901	DIAGRAM,LOGIC-DMAC EXPANDER	
0015	REF	EA		216696-9901	SOURCE TAPE,MASTER FILE-DMAC LOGIC	

DRAFTSMAN DATE	CKD DRAFTSMAN DATE	DESIGN ENGINEER DATE	TITLE BOARD ASSY,EXPANDER NO 1				
PROD MFG DATE	APPD PROJECT ENGINEER DATE	RELEASED DATE	PROJECT NO. 8000/8101		PART NUMBER LM 216700-0001	REV K

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/01/75

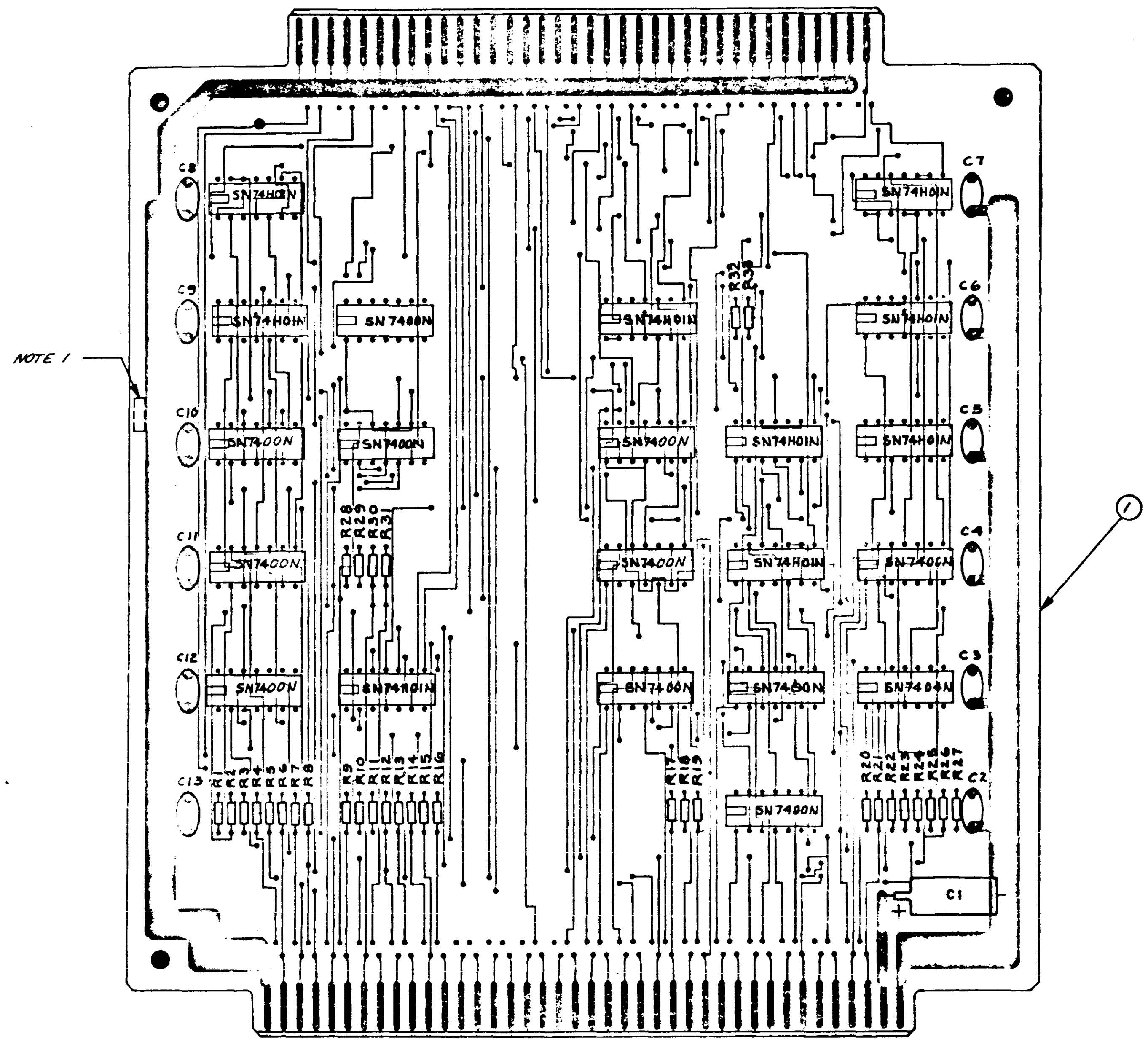
LIST OF MATERIAL

PAGE 2 of

PART NUMBER LM 216700-0001 REV K

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
2016	REF	EA		973567-9901	TEST PROC, DMAC EXPANDER BDS	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						BOARD ASSY, EXPANDER NO 1
MFG	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM 216700-0001 REV K



REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	370332 (A) 10/16/71 — ① F/D-CHG DESCRIPTIONS ON NETWORKS AT LOCATIONS A1, A2, A3, D2 • D3-SN74S00N WERE SN7400N. ② L/M - ADDED ITEM 8, ③ L/M - QTY ITEM 2 WAS 11	10-16-71	
B	371838 (E) J. Piercey 1-7-72 — CHG: 1) L.M. IT. 3, P/N WAS 222222-7401 2) ON F/D SN74H01N NETWORKS WERE SN7401N ADDED: REV. BLOCK ZONE D1	1-12-72	
C	372104 (E) D. Wilson 3-18-72 — ADDED: UPDATED REVISION BLOCK & 8100/8101 TO N/A	3-21-72	
D	374798 (B) 8-1-72 — ADD: NOTE 2 DELETE: CONNECTION BETWEEN P2-35 & GRD BUS	8/8/72	
E	368539 (E) 1-24-73 — ADDED: LM ITEM 15	1/27/73	
F	374168 (E) 2/5/74 — 1) DELETED NOTE 2 2) UPDATED REV. STATUS BLOCK		
G	NOTES 3 & 4 (1) ADDED		
H	388892 (C) (1) L/M, DELETED ITEM 8 (2) QTY OF ITEM 2 WAS 6 (3) OF F/D SN7400N WAS SN74S00N FIVE PLACES (4) L/M; ADDED ITEM 16 (5) UPDATED REV LEV BLK		
J	396469 (C) (1) UPDATED REV LEV BLK	4/30/74	
K	392__5 (B) (1) REVISED REV LEVEL BLOCK	9/74	
L	(1) REVISED REV LEVEL BLOCK		
M	(1) UPDATED REV LEVEL BLOCK	1/15/75	
N	412966 (D) G. Ganzal (1) UPDATED REV LEVEL BLOCK	5/7/76	

NOTES: UNLESS OTHERWISE SPECIFIED:
1. MARK APPROPRIATE REV LETTER APPROX WHERE SHOWN PER PROCESS 1 FARSIDE
3. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF CARD IS .31
4. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF CARD IS .075

REVISIONS											
PRINTED WIRING BOARD 216702-0001	-	-	-	F	G	G	G	H	J		L
LOGIC DIAG. FOR -0001 ASSY. (217812-9901)	B	C	C	C	C	D	E	F	F		G
ASSEMBLY	B	C	D	E	F	G	H	J	K	L	M

1 RUBBER STAMP PER F-100, HEIGHT .12, COLOR BLK

8960/8980	A	216699
8100/8101	A	216694

TEXAS INSTRUMENTS INCORPORATED

CARD ASSY, EXPANDER #2 DRAC COMPUTER

2/1 D 216703

LM

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/01/75

LIST OF MATERIAL

PAGE 1 of

PART NUMBER LM 216703-0001 REV N

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		216702-0001	PRINTED WIRING BOARD,EXPANDER #2	
0002	00011.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0003	00009.000	EA		240000-7401	NETWORK SN74H01N	
0004	00001.000	EA		222222-7404	NETWORK SN7404N	
0005	00001.000	EA		972924-0015	CAP FIX TANT SOLID 47 MFD 10 % 20 VOLT	QPL-M39003/1-2295
0005A					C1	
0006	00012.000	EA		534348-0001	CAP FIX CERAMIC .10 MF 20/80 % 10V	CRL- UK10-104
0006A					C2 THRU C13	
0007	00033.000	EA		972975-0036	RES FIX COMP 300 OHMS 5 % 1/8 WATT	QPL- RC05G301JS
0007A					R1 THRU R33	
0015	REF	EA		216696-9901	SOURCE TAPE,MASTER FILE-DMAC LOGIC	
0016	REF	EA		973567-9901	TEST PROC,DMAC EXPANDER BDS	

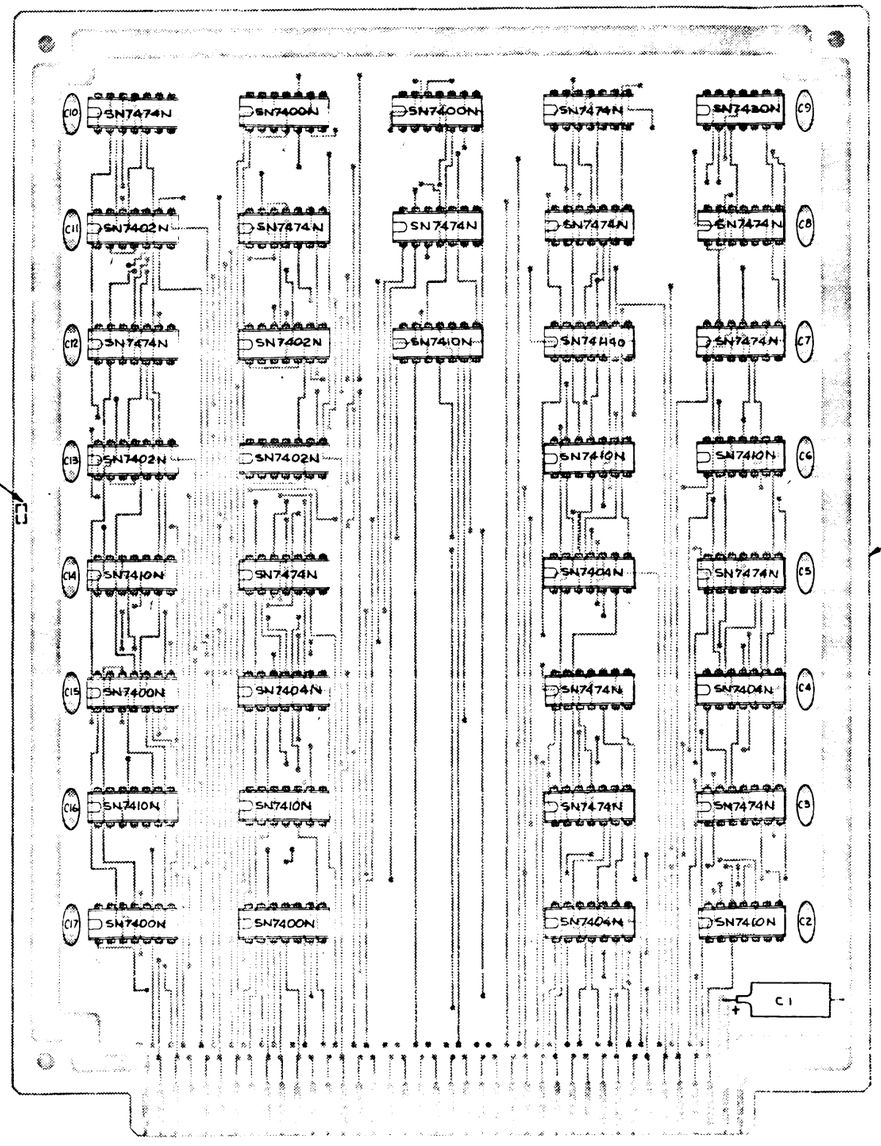
DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CARD ASSY,EXPANDER #2
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO. 8100/8101

PART NUMBER LM 216703-0001 REV N

5-9/5-10

T.I. 13849

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	372104(E) D. Wilson 3-20-72	3-21-72	
	ADDED: REV. BLOCK ZONE D1 & 8100/8101 TO N/A		
B	368539 (E) 1-24-73		
	ADDED: LM ITEM 15.		
C	CN38302 B(C), A Drawing (1) ADDED NOTES 2 AND 3		
D	368847 (E) (1) ADDED ITEM 16 TO L/M (2) UPDATED REV LEVEL BLK	2-13-73	
E	CN392308 (B) (1) ADDED (1) UPDATED REV LEVEL BLOCK.	4-9-74	
F	CN38378910 (1) UPDATED REV LEVEL BLOCK	1-7-75	
G	CN41296610 (1) UPDATED REV LEVEL BLOCK	5-24-76	



NOTES:
1. MARK APPROPRIATE ASSY REV LETTER APPROX WHERE SHOWN PER PROCESS 1 (FARSIDE)
2. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF CARD IS .31
3. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF CARD IS .075

REVISIONS														
LOGIC DIAG FOR -0001 ASSY. (217812-9901)	C	C	C	D	E	F	F
ASSEMBLY	*	Δ	B	C		E	F	G

1. RUBBER STAMP PER F-100, HT .12 COLOR BLACK

A	216694	5-24-70	
A	216694		

TEXAS INSTRUMENTS

BOARD ASSY EXPANDER NO. 3
DMAC
COMPUTER
2/1 D 216706

LM

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/01/75

LIST OF MATERIAL

PAGE 1 of

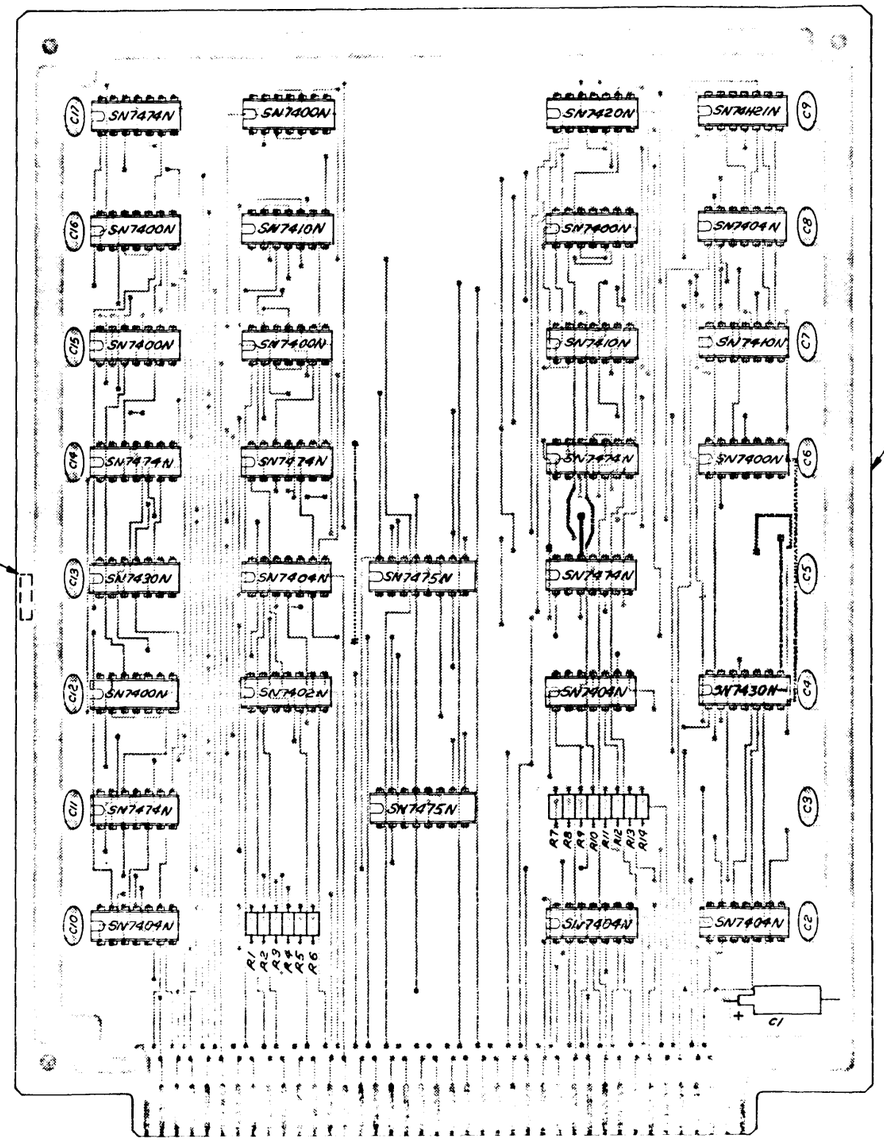
PART NUMBER LM 216706-0001 REV G

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		216705-0001	PRINTED WIRING BOARD-EXPANDER #3	
0002	00005.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0003	00004.000	EA		222222-7402	NETWORK SN7402N	TI--SN7402N
0004	00004.000	EA		222222-7404	NETWORK SN7404N	
0005	00007.000	EA		222222-7410	NETWORK SN7410N	-SN7410N
0006	00001.000	EA		222222-7430	NETWORK SN7430N	-SN7430N
0007	00001.000	EA		240000-7440	NETWORK-SN74H40N	
0008	00013.000	EA		222222-7474	NETWORK SN7474N	-SN7474N
0009	00001.000	EA		972924-0015	CAP FIX TANT SOLID 47 MFD 10 % 20 VOLT	QPL-M39003/1-2295
0009A					C1	
0010	00016.000	EA		534348-0001	CAP FIX CERAMIC .10 MF 20/80 % 10V	CRL- UKI0-104
0010A					C2 THRU C17	
0015	REF	EA		216696-9901	SOURCE TAPE,MASTER FILE-DMAC LOGIC	
0016	REF	EA		973567-9901	TEST PROC,DMAC EXPANDER BDS	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						BOARD ASSY, EXPANDER NO 3
APPD MFG	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER LM 216706-0001 REV G

TI 17549



LTR	DESCRIPTION	DATE	APPD
A	372104(E) D Wilson 3-20-72	3-22-72	[illegible]
	ADDED: REV BLOCK ZONE D1 & B100 & B101 TO N/A.		
B	368539 (E) 1-24-73 [illegible]	1/24/73	[illegible]
	ADDED: LM ITEM 15.		
C	C: 389228(E). Dtd 2/6/74 (1) ADDED NOTES 2 AND 3	2/7/74	[illegible]
D	388848(E) D Rev (1) ADDED ITEM 16 TO C/M'S: UPDATED REV LEVEL BLOCK	[illegible]	[illegible]
E	CN392309(B) [illegible] (1) UPDATED REV LEVEL BLOCK	[illegible]	[illegible]
F	CN397143(C) [illegible] (1) ITEM 11 WAS 233751-9906 (2) UPDATED REV LEVEL BLOCK	[illegible]	[illegible]
G	[illegible] (1) UPDATED REV LEVEL BLOCK	11/3/77	[illegible]
H	CN412366(D) [illegible] (1) UPDATED REV LEVEL BLOCK	[illegible]	[illegible]

NOTES:
1. MARK APPROPRIATE ASSY REV LTR APPROX WHERE SHOWN PER PROCESS 1. (FARSIDE)
2. MAXIMUM COMPONENT HEIGHT FROM COMPONENT SIDE OF CARD IS .31
3. MAXIMUM LEAD LENGTH FROM CONDUCTOR SIDE OF CARD IS .075

REVISIONS																
PWB 216708											E	E	F	F		
LOGIC DIAG FOR -0001 ASSY (217812-9901)	C	C	C	D	E	F	F	F	G							
ASSEMBLY	*	A	B	C	D	E	F	G	H							

1. RUBBER STAMP PER F-100, HEIGHT .12 COLOR BLACK

SN7400 A 216709
SN7474 A 216709

BOARD ASSY, EXPANDER NO 4
DNAC COMPUTER
211 216709

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/01/75

LIST OF MATERIAL

PAGE 1 of

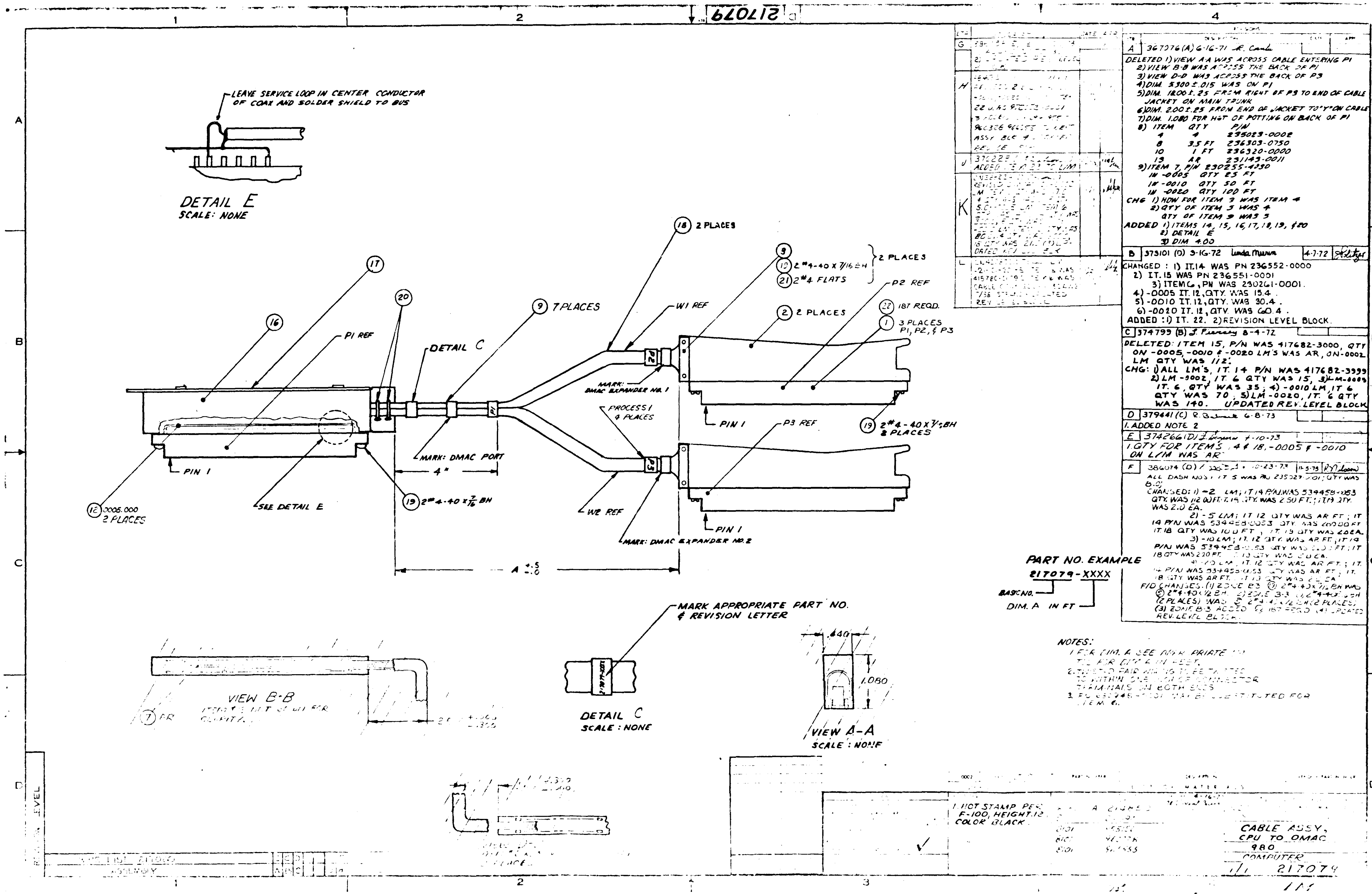
LM PART NUMBER 216709-0001 REV H

PRINT REV NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		216708-0001	PRINTED WIRING BOARD-EXPANDER #4	
0002	00007.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0003	00006.000	EA		222222-7404	NETWORK SN7404N	
0004	00002.000	EA		222222-7430	NETWORK SN7430N	-SN7430N
0005	00001.000	EA		222222-7402	NETWORK SN7402N	TI--SN7402N
0006	00003.000	EA		222222-7410	NETWORK SN7410N	-SN7410N
0007	00006.000	EA		222222-7474	NETWORK SN7474N	-SN7474N
0008	00002.000	EA		222222-7475	NETWORK-SN7475N	
0009	00001.000	EA		222222-7420	NETWORK SN7420N	-SN7420N
0010	00001.000	EA		240000-7421	NETWORK-SN74H21N	
0011	00008.000	EA		972975-0049	RES FIX COMP 1.0 K OHMS 5 % 1/8 WATT	QPL- RC05G102JS
0011A					R7 THRU R14	
0012	00006.000	EA		972975-0036	RES FIX COMP 300 OHMS 5 % 1/8 WATT	QPL- RC05G301JS
0012A					R1 THRU R6	
0013	00001.000	EA		972924-0015	CAP FIX TANT SOLID 47 MFD 10 % 20 VOLT	QPL-M39003/1-2295
0013A					C1	
0014	00016.000	EA		534348-0001	CAP FIX CERAMIC .10 MF 20/80 % 10V	CRL- UK10-104
0014A					C2 THRU C17	
0015	REF	EA		216696-9901	SOURCE TAPE,MASTER FILE-DMAC LOGIC	
0016	REF	EA		973567-9901	TEST PROC,DMAC EXPANDER BDS	

ARTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						BOARD ASSY, EXPANDER NO 4
PD. MFG	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

LM PART NUMBER 216709-0001 REV H

5-17/5-18



217079
LEAVE SERVICE LOOP IN CENTER CONDUCTOR OF COAX AND SOLDER SHIELD TO BUS
DETAIL E
SCALE: NONE
18 2 PLACES
17
16
20
P1 REF
DETAIL C
9 7 PLACES
W1 REF
9
10 2 #4-40 X 7/16 BH
21 2 #4 FLATS
2 PLACES
P2 REF
2 2 PLACES
22 187 REQD.
1 3 PLACES P1, P2, & P3
MARK: DMAC EXPANDER NO. 1
PROCESS 1 4 PLACES
PIN 1
P3 REF
19 2 #4-40 X 1/2 BH 2 PLACES
MARK: DMAC PORT
4"
PIN 1
12 .0005.000 2 PLACES
SEE DETAIL E
19 2 #4-40 X 7/16 BH
W2 REF
PIN 1
MARK: DMAC EXPANDER NO. 2
A ±.5 / -.0
PART NO. EXAMPLE
217079-XXXX
BASIC NO.
DIM. A IN FT
MARK APPROPRIATE PART NO. & REVISION LETTER
VIEW B-B
DETAIL C
SCALE : NONE
.440
1.080
VIEW A-A
SCALE : NONE
A 367076 (A) 6-16-71
DELETED 1) VIEW A-A WAS ACROSS CABLE ENTERING P1
2) VIEW B-B WAS ACROSS THE BACK OF P1
3) VIEW D-D WAS ACROSS THE BACK OF P3
4) DIM. .5300±.015 WAS ON P1
5) DIM. 12.00±.25 FROM RIGHT OF P3 TO END OF CABLE JACKET ON MAIN TRUNK
6) DIM. 2.00±.25 FROM END OF JACKET TO "Y" ON CABLE
7) DIM. 1.080 FOR HGT OF POTTING ON BACK OF P1
8) ITEM QTY P/N
4 4 235023-0002
8 3.5 FT 236303-0750
10 1 FT 236320-0000
13 AR 231143-0011
9) ITEM 7, P/N 230255-4030
IN -0005 QTY 25 FT
IN -0010 QTY 50 FT
IN -0020 QTY 100 FT
CHG 1) HDW FOR ITEM 3 WAS ITEM 4
2) QTY OF ITEM 3 WAS 4
QTY OF ITEM 9 WAS 5
ADDED 1) ITEMS 14, 15, 16, 17, 18, 19, & 20
2) DETAIL E
3) DIM 4.00
B 373101 (D) 3-16-72 4-7-72
CHANGED : 1) IT. 14 WAS PN 236552-0000
2) IT. 15 WAS PN 236551-0001
3) ITEM 6, PN WAS 230261-0001.
4) -0005 IT. 12, QTY. WAS 15.4 .
5) -0010 IT. 12, QTY. WAS 30.4 .
6) -0020 IT. 12, QTY. WAS 60.4 .
ADDED : 1) IT. 22. 2) REVISION LEVEL BLOCK.
C 374799 (B) 8-4-72
DELETED: ITEM 15, P/N WAS 417682-3000, QTY ON -0005, -0010 & -0020 LM'S WAS AR, ON -0002 LM QTY WAS 112.
CHG: 1) ALL LM'S, IT. 14 P/N WAS 417682-3999 2) LM -0002, IT. 6 QTY WAS 15, 3) LM-0005 IT. 6, QTY WAS 35, 4) -0010 LM, IT 6 QTY WAS 70, 5) LM -0020, IT. 6 QTY WAS 140. UPDATED REV. LEVEL BLOCK
D 379441 (C) 6-8-73
1. ADDED NOTE 2
E 374266 (D) 7-10-73
1. QTY FOR ITEMS 4 & 18, -0005 & -0010 ON L/M WAS AR
F 386074 (D) 10-23-73 11-5-73
NOTES:
CABLE ASSY, CPU TO OMAC 980
COMPUTER
217079

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/24/76 **LIST OF MATERIAL** PAGE 1 of

LM PART NUMBER 217079-0002 REV L

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
	00187.000	EA		972053-0002	SLEEVE,SOLDER,TAB TERMINAL	RCH--C-704-02
0001	00003.000	EA		231447-0800	CONNECTOR PC 36 PIN	VIK-2VH-36/1CN-5
C001A					P1,P2,P3	
0002	00002.000	EA		214080-0001	CONNECTOR-COVER	
0003	00002.000	EA		214081-0001	CLAMP	
C006	00028.000	FT		772228-0001	CABLE COAXIAL 80 OHM UL STYLE 1371	GOA-GWN1013
C009	00007.000	EA		418201-0001	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL- MS3368-1-9
0011	REF	EA		217080-9901	WIRE LIST,PT-TO-PT-CPU TO DMAC	
0012	00005.000	FT		411400-0018	WIRE,BARE TINNED,18AWG, COPPER BUS	IWP- 18-630
0014	00193.000	FT		966760-2896	WIRE,TWISTED PAIR #28 WHT/BLU IPVC	UL - 1472 7STR UL&CSA
0016	00001.000	EA		216138-0001	COVER,CONNECTOR	
0017	00001.000	EA		216136-0001	HOOD,CONNECTOR	
0018	00013.000	FT		972436-0019	INSULATION SLEEVING PVC CHLORIDE	LFS- HT-105C-24
0019	00010.000	EA		972988-0016	SCREW 4-40 X .438 PAN HEAD CRES	
0020	00002.000	EA		418212-0040	STRAP,TIEDOWN,ADJUSTABLE,PLASTIC	QPL- MS3367-4-9
0021	00004.000	EA		411027-0804	WASHER .125 X .312 X .032 FLAT CRES	QPL- MS15795-804
0022	00187.000	EA		972053-0002	SLEEVE,SOLDER,TAB TERMINAL	RCH--C-704-02
0023	REF	EA		973585-9901	UNIT TEST PROCEDURE	

RAFTSMAN DATE	CKD. DRAFTSMAN DATE	DESIGN ENGINEER DATE	TITLE		
	5/25/76		CABLE ASSY,CPU TO DMAC-2FT		
APPD. MFG. DATE	APPD. PROJECT ENGINEER DATE	RELEASED DATE	PROJECT NO. 7503	LM PART NUMBER 217079-0002	REV L

TI 13849

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/24/76

LIST OF MATERIAL

PAGE 1 of

LM PART NUMBER 217079-0010 REV L

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00003.000	EA		231447-0800	CONNECTOR PC 36 PIN	VIK-2VH-36/1CN-5
0001A					P1 P2 P3	
C002	00002.000	EA		214080-0001	CONNECTOR-COVER	
0003	00002.000	EA		214081-0001	CLAMP	
0006	00092.000	FT		772228-0001	CABLE COAXIAL 80 OHM UL STYLE 1371	GOA-GWN1013
0009	00007.000	EA		418201-0001	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL- MS3368-1-9
0011	REF	EA		217080-9901	WIRE LIST,PT-TO-PT-CPU TO DMAC	
0012	00005.000	FT		411400-0018	WIRE,BARE TINNED,18AWG, COPPER BUS	IWP- 18-630
0014	00633.000	FT		966760-2896	WIRE,TWISTED PAIR #28 WHT/BLU IPVC	UL - 1472 7STR UL&CSA
0016	00001.000	EA		216138-0001	COVER,CONNECTOR	
0017	00001.000	EA		216136-0001	HOOD,CONNECTOR	
C018	00013.000	FT		972436-0019	INSULATION SLEEVING PVC CHLORIDE	LFS- HT-105C-24
0019	00010.000	EA		972983-C016	SCREW 4-40 X .438 PAN HEAD CRES	
0020	00002.000	EA		418212-0040	STRAP,TIEDOWN,ADJUSTABLE,PLASTIC	QPL- MS3367-4-9
C021	00004.000	EA		411027-0804	WASHER .125 X .312 X .032 FLAT CRES	QPL- MS15795-804
0022	00187.000	EA		972053-0002	SLEEVE,SOLDER,TAB TERMINAL	PCH--C-704-02
C023	REF	EA		973585-9901	UNIT TEST PROCEDURE	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CABLE ASSY,CPU TO DMAC- 10 FT
APPD MFG	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO
						LM 217079-0010 REV L

TI 13849

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/24/76

LIST OF MATERIAL

PAGE 1 of

LM PART NUMBER 217079-0005 REV L

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00003.000	EA		231447-0800	CONNECTOR PC 36 PIN	VIK-2VH-36/1CN-5
0001A					P1 P2 P3	
0002	00002.000	EA		214080-0001	CONNECTOR-COVER	
0003	00002.000	EA		214081-0001	CLAMP	
0006	00052.000	FT		772228-0001	CABLE COAXIAL 80 OHM UL STYLE 1371	GOA-GWN1013
0009	00007.000	EA		418201-0001	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL- MS3368-1-9
0011	REF	EA		217080-9901	WIRE LIST,PT-TO-PT-CPU TO DMAC	
0012	00005.000	FT		411400-0018	WIRE,BARE TINNED,18AWG, COPPER BUS	IWP- 18-630
0014	00358.000	FT		966760-2896	WIRE,TWISTED PAIR #28 WHT/BLU IPVC	UL - 1472 7STR UL&CSA
0016	00001.000	EA		216138-0001	COVER,CONNECTOR	
0017	00001.000	EA		216136-0001	HOOD,CONNECTOR	
0018	00013.000	FT		972436-0019	INSULATION SLEEVING PVC CHLORIDE	LFS- HT-105C-24
0019	00010.000	EA		972988-0016	SCREW 4-40 X .438 PAN HEAD CRES	
0020	00002.000	EA		418212-0040	STRAP,TIEDOWN,ADJUSTABLE,PLASTIC	QPL- MS3367-4-9
0021	00004.000	EA		411027-0804	WASHER .125 X .312 X .032 FLAT CRES	QPL- MS15795-804
0022	00187.000	EA		972053-0002	SLEEVE,SOLDER,TAB TERMINAL	RCH--C-704-02
0023	REF	EA		973585-9901	UNIT TEST PROCEDURE	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CABLE ASSY,CPU TO DMAC- 5 FT
APPD. MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

LM PART NUMBER 217079-0005 REV L

TEXAS INSTRUMENTS
INCORPORATED

DATE 05/24/76

LIST OF MATERIAL

PAGE 1 of

LM PART NUMBER 217079-0020 REV L

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00003.000	EA		231447-0X00	CONNECTOR PC 36 PIN	VIK-2VH-36/1CN-5
0001A					P1 P2 P3	
0002	00002.000	EA		214080-0001	CONNECTOR-COVER	
0003	00002.000	EA		214081-0001	CLAMP	
0006	00180.000	FT		772228-0001	CABLE COAXIAL 80 OHM UL STYLE 1371	GOA-GWN1013
0009	00007.000	EA		418201-0001	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL- MS3368-1-9
0011	REF	EA		217080-9901	WIRE LIST,PT-TO-PT-CPU TO DMAC	
0012	00005.000	FT		411400-0018	WIRE,BARE TINNED,18AWG, COPPER BUS	IWP- 18-630
0014	01200.000	FT		966760-2896	WIRE,TWISTED PAIR #28 WHT/BLU IPVC	UL - 1472 7STR UL&CSA
0016	00001.000	EA		216138-0001	COVER,CONNECTOR	
0017	00001.000	EA		216136-0001	HOOD,CONNECTOR	
0018	00013.000	FT		972436-0019	INSULATION SLEEVING PVC CHLORIDE	LFS- HT-105C-24
0019	00010.000	EA		972988-0016	SCREW 4-40 X .438 PAN HEAD CRES	
0020	00002.000	EA		418212-0040	STRAP,TIEDOWN,ADJUSTABLE,PLASTIC	QPL- MS3367-4-9
0021	00004.000	EA		411027-08C4	WASHER .125 X .312 X .032 FLAT CRES	QPL- MS15795-804
0022	00187.000	EA		972053-0002	SLEEVE,SOLDER,TAB TERMINAL	RCH--C-704-02
0023	REF	EA		973585-9901	UNIT TEST PROCEDURE	

DRAFTSMAN DATE	CKD. DRAFTSMAN DATE	DESIGN ENGINEER DATE	TITLE
			CABLE ASSY,CPU TO DMAC- 20 FT
APPD.-MFG. DATE	APPD. PROJECT ENGINEER DATE	RELEASED DATE	PROJECT NO.
			LM PART NUMBER 217079-0020 REV L

TI 13849

A 217080 E

PROJ NO.	SIZE	NEXT ASSY DWG NO.
8980	D	217079
8960	D	217079
7502		217079
7503		217079

REVISIONS

LTR	DESCRIPTION	DATE	APPD
A	296097(D) 6/18/70 D. Macias CHG 1) COMPONENT CONNECTION FOR FINISH STATION TO (A) SH 2, WIRE #4 WAS -B, #5 WAS -2, #6 WAS -C, & WIRE #7 WAS -3; (B) SH 3, WIRE #10 WAS -35 & #12 WAS -36; (C) SH 4, WIRE #7 WAS -e, #8 WAS -27, & #12 WAS -23; (D) SH 5, WIRE #13 WAS -d & #15 WAS -f; (E) SH 6, WIRE #1 WAS P2-W, #5 WAS -a, #7 WAS -e, #9 WAS -c, #11 WAS -f, & #17 WAS -n; (F) SH 7 WIRE #7 WAS -6. 2) COMPONENT CONNECTION FOR START STATION TO (A) SH 2, WIRE #8 WAS -a, (B) SH 5, WIRE #17 WAS -b, #19 WAS -d, #21 WAS -e, & #23 WAS -f; (C) SH 7, WIRE #1 WAS -h, #3 WAS -j, #5 WAS -k, #7 WAS -l, #9 WAS -m, & #11 WAS -n. 3) SH 5, SIGNATURE FOR WIRE #19 WAS "MRD 6". ADDED 1) 960, D, 217079 TO N/A BLOCK. 2) SH 4, REMARKS TO WIRES #4 & 6.	6/24/70	[illegible]
B	368295 (C) 11-25-70 [illegible] CHG: SH. 5, IT. 20 FINISH STA. WAS P2-12	12-1-70	[illegible]
C	369464 (C) 6-24-71 [illegible] REVISED & REDRAWN WITH CHANGES SH 2 THRU 7 TO CORRECT WIRE COLORS.	—	—
D	374799 (B) L. PIERCEY 8/4/72 CHG: 1) WIRE DESCR. "CABLE" WAS "TEF". 2) IN DESCR. "BLU" WAS "BLK", N/A LM ITEM NO WAS 15. 3) SH 4. WIRE # 8, FINISH STATION WAS P3-35. 4) SH 4, WIRE #8, REMARK WAS "THIS PIN HAS TWO CONNECTIONS". 5) SH 7, WIRE #8, FINISH STATION WAS P3-35. ADDED: 1) SH 4, WIRES #15 & 16, & REMARK TO WIRES 4 & 6. 2) SH 7, REMARK TO WIRE #12	8/7/72	D. Booth
E	386073 (C) [illegible] 10/23/73 CHANGE 1) ALL WHT/BLU WIRES WAS BLU (SH 2 THRU 7)	10-26-73	[illegible]
F	CN384777 (C) [illegible]	3/4/74	[illegible]
G	CN394165 (C) [illegible]	1/25/75	[illegible]

REV STATUS OF SHEETS							
REV	G	F	F	F	G	F	F
SHEET	1	2	3	4	5	6	7

DR 4-16-70 U. [illegible]	APPD [illegible] 5-[illegible]	TITLE WIRE LIST, PT TO PT. CPU TO DMAC	TEXAS INSTRUMENTS INCORPORATED INDUSTRIAL PRODUCTS DIVISION HOUSTON TEXAS
CKD 5-4-70 [illegible]	APPD [illegible]		SCALE NONE
ENGR [illegible]	RELEASE [illegible] 5/6/70		SIZE A · 217080 · REV G · SHEET 1 OF 7

TI-4260-A

MANUAL NO. 216759-9701

TI-13218

TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

A

SHEET 2

217080

REV F

WIRE NO.	DESCRIPTION	TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LM ITEM NO.
1	#18 BUS	AR	GRD BUS	P1 - 1	P1 - 36		12
2	#18 BUS		GRD BUS	P1 - A	P1 - $\overline{R}$		12
3	#28CABLE WHT		MRD 01	- 34	P2 - H		14
4	BLU			- BUS	- 7		
5	WHT		MRD 03	- 33	- K		14
6	BLU			- BUS	- 9		
7	WHT		MRD 05	- 32	- M		14
8	BLU			- BUS	-11		
9	WHT		MRD 07	- 31	- P		14
10	BLU			- BUS	-13		
11	WHT		MRD 09	- 30	- S		14
12	BLU			- BUS	-15		
13	WHT		MRD 11	- 29	- U		14
14	BLU			- BUS	-17		
15	WHT		MRD 13	- 28	- W		14
16	BLU			-BUS	-19		
17	WHT		MRD 15	-27	- Y		14
18	BLU			- BUS	-21		
19	WHT		GRANT-	-26	- $\overline{F}$		14
20	#28 CABLE BLU			- BUS	-28		
21	COAX COND		ATI2IO	-25	- $\overline{J}$		6
22	SHIELD			_ BUS	-30		
23	COAX COND		DATAVAIL	-24	- $\overline{A}$		6
24	SHIELD	AR		P1 - BUS	P 2 - 23		

WIRE NO.	DESCRIPTION		TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LM ITEM NO.
25	COAX COND		AR	MRESTOP	P1 - 23	P2 - $\overline{D}$		6
26	SHIELD				BUS	P2 - 26		
27	#28 CABLE	WHT		MAD01	- 22	P3 - $\overline{E}$		14
28		BLU			- BUS	- 27		
29		WHT		MAD03	- 21	- $\overline{C}$		14
30		BLU			- BUS	- 25		
31		WHT		MAD05	- 20	- $\overline{A}$		14
32		BLU			- BUS	- 23		
33		WHT		MAD07	--19	- Y		14
34		BLU			- BUS	- 21		
35		WHT		MAD09	- 18	- W		14
36		BLU			- BUS	- 19		
37		WHT		MAD10	- 17	- V		14
38		BLU			- BUS	- 18		
39		WHT		MAD13	- 16	- S		14
40		BLU			- BUS	- 15		
41		WHT		MAD15	- 15	- P		14
42		BLU			- BUS	- 13		
43		WHT		MWD01	- 14	- M		14
44		BLU			- BUS	- 11		
45		WHT		MWD03	- 13	- K		14
46		BLU			- BUS	- 9		
47		WHT		MWD05	- 12	- H		14
48	#28 CABLE	BLU	AR		P1 - BUS	P3 - 7		

TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON TEXAS

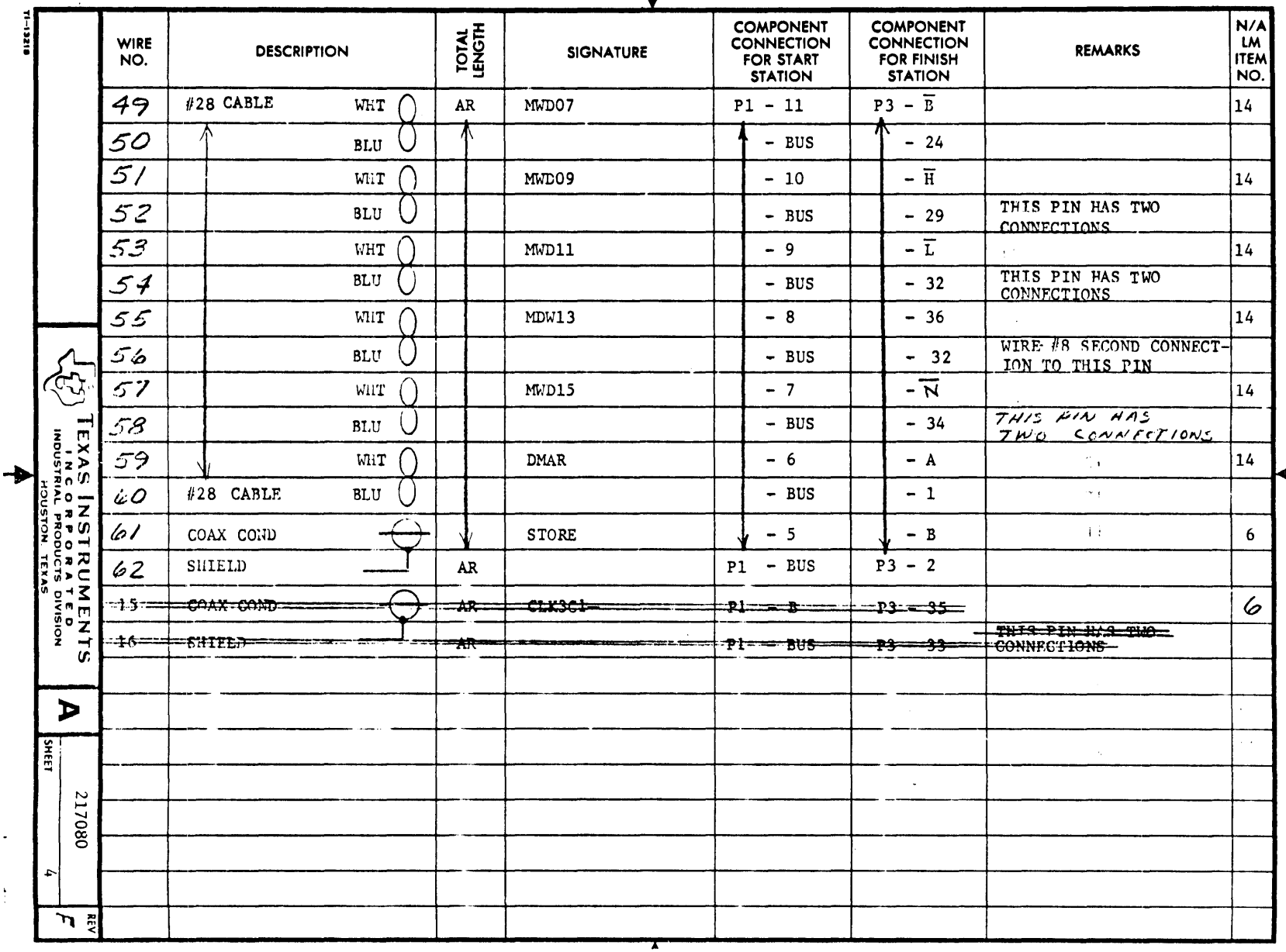
A

SHEET 3

217080

REV F

71-13218



TI-13218

TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

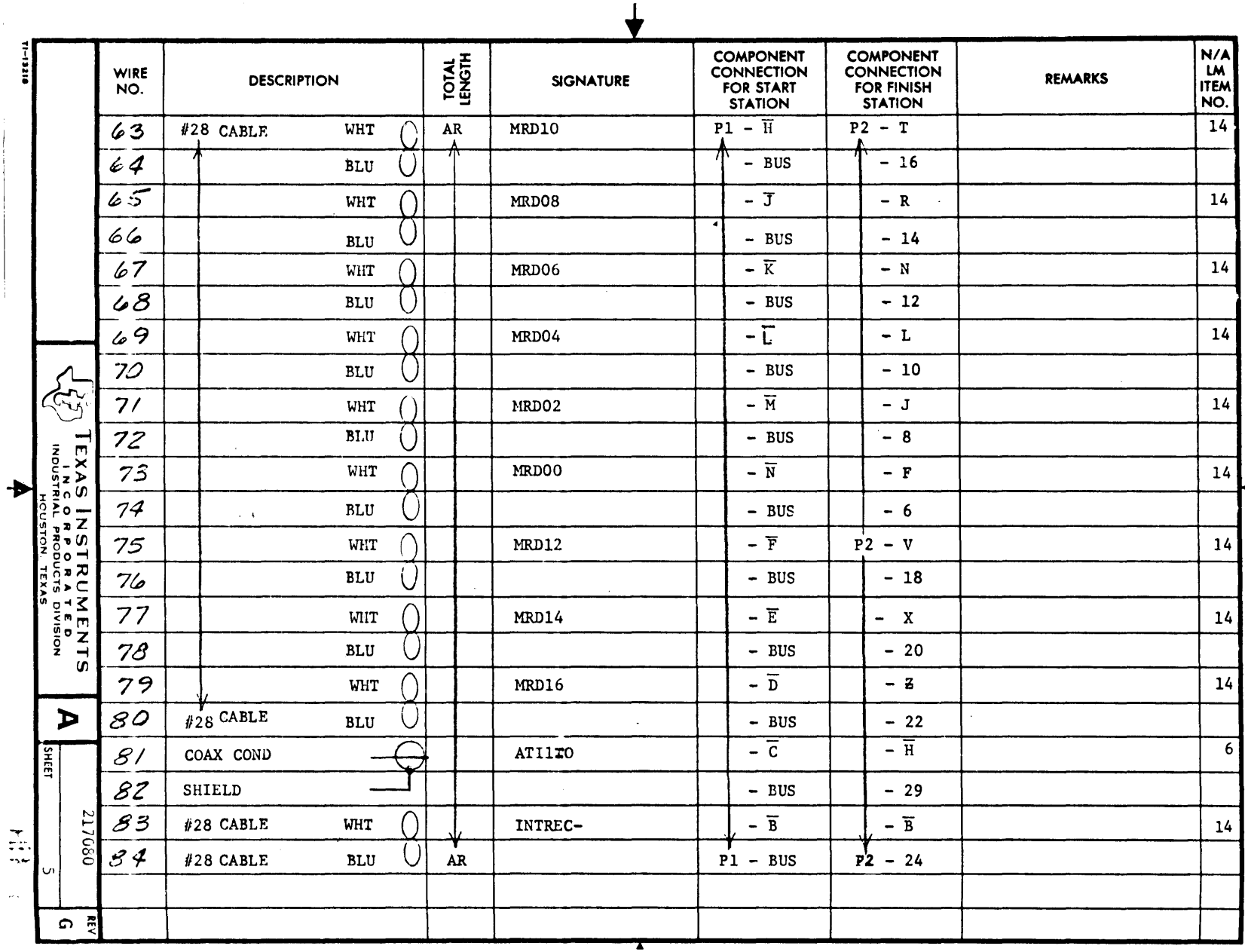
A

SHEET 4

217080

F REV

WIRE NO.	DESCRIPTION	TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LM ITEM NO.
49	#28 CABLE WHT	AR	MWD07	P1 - 11	P3 - $\overline{B}$		14
50	BLU			- BUS	- 24		
51	WHT		MWD09	- 10	- $\overline{H}$		14
52	BLU			- BUS	- 29	THIS PIN HAS TWO CONNECTIONS	
53	WHT		MWD11	- 9	- $\overline{L}$		14
54	BLU			- BUS	- 32	THIS PIN HAS TWO CONNECTIONS	
55	WHT		MDW13	- 8	- 36		14
56	BLU			- BUS	- 32	WIRE #8 SECOND CONNECTION TO THIS PIN	
57	WHT		MWD15	- 7	- $\overline{N}$		14
58	BLU			- BUS	- 34	THIS PIN HAS TWO CONNECTIONS	
59	WHT		DMAR	- 6	- A		14
60	#28 CABLE BLU			- BUS	- 1		
61	COAX COND		STORE	- 5	- B		6
62	SHIELD	AR		P1 - BUS	P3 - 2		
~~15~~	~~COAX COND~~	~~AR~~	~~CLK3C1~~	~~P1 - B~~	~~P3 - 35~~		~~6~~
~~16~~	~~SHIELD~~	~~AR~~		~~P1 - BUS~~	~~P3 - 33~~	~~THIS PIN HAS TWO CONNECTIONS~~	



WIRE NO.	DESCRIPTION		TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LM ITEM NO.
63	#28 CABLE	WHT	AR	MRD10	P1 - $\overline{H}$	P2 - T		14
64		BLU			- BUS	- 16		
65		WHT		MRD08	- $\overline{J}$	- R		14
66		BLU			- BUS	- 14		
67		WHT		MRD06	- $\overline{K}$	- N		14
68		BLU			- BUS	- 12		
69		WHT		MRD04	- $\overline{L}$	- L		14
70		BLU			- BUS	- 10		
71		WHT		MRD02	- $\overline{M}$	- J		14
72		BLU			- BUS	- 8		
73		WHT		MRD00	- $\overline{N}$	- F		14
74		BLU			- BUS	- 6		
75		WHT		MRD12	- $\overline{F}$	P2 - V		14
76		BLU			- BUS	- 18		
77		WHT		MRD14	- $\overline{E}$	- X		14
78		BLU			- BUS	- 20		
79		WHT		MRD16	- $\overline{D}$	- Z		14
80	#28 CABLE	BLU			- BUS	- 22		
81	COAX COND			AT11TO	- $\overline{C}$	- $\overline{H}$		6
82	SHIELD				- BUS	- 29		
83	#28 CABLE	WHT		INTREC-	- $\overline{B}$	- $\overline{B}$		14
84	#28 CABLE	BLU	AR		P1 - BUS	P2 - 24		

TI-12210

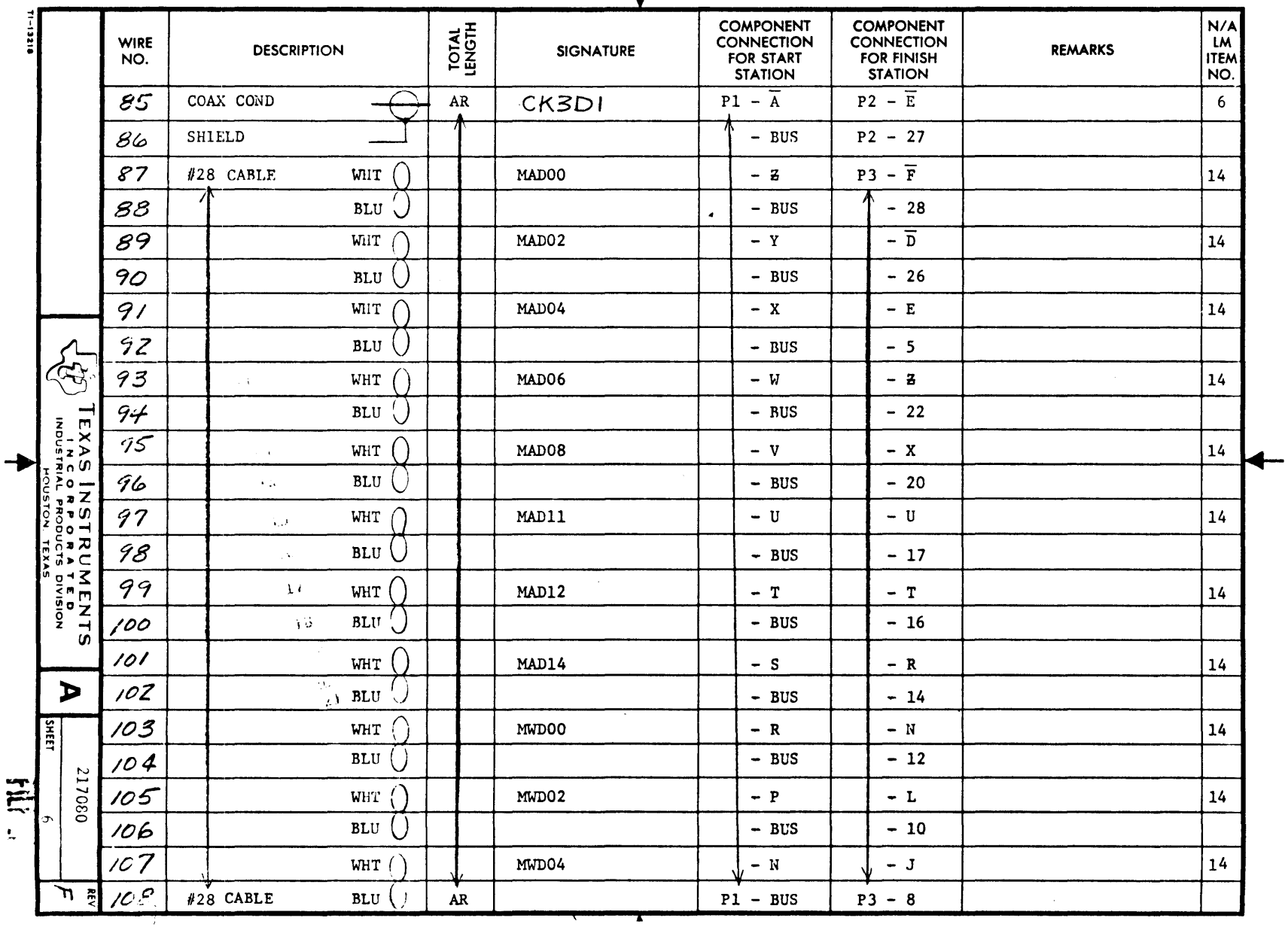
TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

A

SHEET 5

217080

REV G



TI-13218

WIRE NO.	DESCRIPTION	TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LM ITEM NO.
85	COAX COND	AR	CK3D1	P1 - $\overline{A}$	P2 - $\overline{E}$		6
86	SHIELD			- BUS	P2 - 27		
87	#28 CABLE WHT		MAD00	- Z	P3 - $\overline{F}$		14
88	BLU			- BUS	- 28		
89	WHT		MAD02	- Y	- $\overline{D}$		14
90	BLU			- BUS	- 26		
91	WHT		MAD04	- X	- E		14
92	BLU			- BUS	- 5		
93	WHT		MAD06	- W	- Z		14
94	BLU			- BUS	- 22		
95	WHT		MAD08	- V	- X		14
96	BLU			- BUS	- 20		
97	WHT		MAD11	- U	- U		14
98	BLU			- BUS	- 17		
99	WHT		MAD12	- T	- T		14
100	BLU			- BUS	- 16		
101	WHT		MAD14	- S	- R		14
102	BLU			- BUS	- 14		
103	WHT		MWD00	- R	- N		14
104	BLU			- BUS	- 12		
105	WHT		MWD02	- P	- L		14
106	BLU			- BUS	- 10		
107	WHT		MWD04	- N	- J		14
108	#28 CABLE BLU	AR		P1 - BUS	P3 - 8		

TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

A

SHEET 6

217080

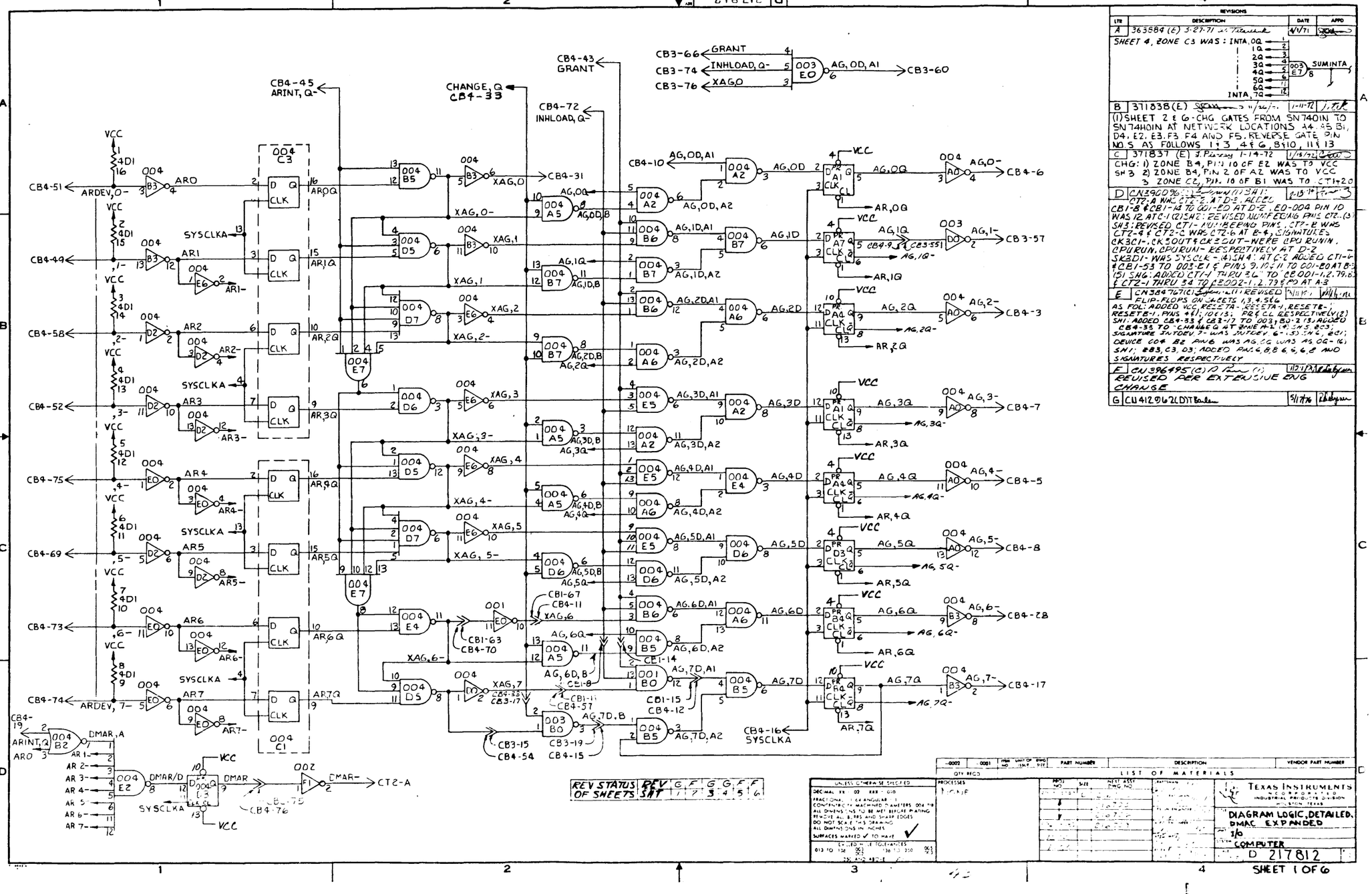
F REV

WIRE NO.	DESCRIPTION	TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LM ITEM NO.
109	#28 CABLE WHT	AR	MWD06	P1 - M	P3 - F		14
110	BLU			- BUS	- 6		
111	WHT		MWD08	- L	- D		14
112	BLU			- BUS	- 4		
113	WHT		MWD10	- K	- $\overline{K}$		14
114	BLU			- BUS	- 31		
115	WHT		MWD12	- J	- $\overline{R}$		14
116	BLU			- BUS	- 29	Second connection to this pin	
117	WHT		MWD14	- H	- $\overline{P}$		14
118	BLU			- BUS	- 34	Second connection to this pin	
119	WHT		MWD16	- F	- $\overline{M}$		14
120	BLU			- BUS	- 33		
121	WHT		INTRQST	- E	- $\overline{J}$		14
122	#28 CABLE BLU			- BUS	- 30		
123	COAX COND		FETCH	- D	- C		6
124	SHIELD			- BUS	P3 - 3		
125	#28 CABLE WHT		PAR ERROR	- C	P2 - $\overline{C}$		14
126	#28 CABLE BLU			- BUS	- 25		
127	COAX COND		CK3C1	- B	- $\overline{N}$		14
128	SHIELD	AR		P1 - BUS	P2 - 34		

TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

A | SHEET 7 | 217080 | REV F

TI-13218



REV STATUS OF SHEETS	REV	G	F	G	G	F	F
	SHT	1	2	3	4	5	6

LTR	REVISIONS: DESCRIPTION	DATE	APPD
A	363584 (E) 3-27-71 J. Thrasher SHEET 4, ZONE C3 WAS : INTA, 0Q 1Q 2Q 3Q 4Q 5Q 6Q INTA, 7Q 003 E7 SUMINTA	4/1/71	
B	371838(E) (1) SHEET 2 & 6 - CHG GATES FROM SN74OIN TO SN74HOIN AT NETWORK LOCATIONS A4, A5, B1, D4, E2, E3, F3, F4 AND F5. REVERSE GATE PIN NOS AS FOLLOWS 1 & 3, 4 & 6, 8 & 10, 11 & 13	1-11-72	
C	371837 (E) J. Pinney 1-14-72 CHG: 1) ZONE B4, PIN 10 OF E2 WAS TO VCC SH 3 2) ZONE B4, PIN 2 OF A2 WAS TO VCC 3 ZONE C2, PIN 10 OF B1 WAS TO CT1+2.0	1/14/72	
D	CN 390 (1) SH 1: CT2-A WAS CT2-2. AT D-3. ADDED CB1-8 & CB1-13 TO 001-E0 AT D-2, E0-004 PIN 10 WAS 12. AT C-1 (2) SH 2: REVISED NUMBERING PINS CT2-(3) SH 3: REVISED CT1-10, 11: BEANG PINS. CT7-B WAS CT2-4 & CT3-2 WAS CT2-6 AT B-4. SIGNATURES: CK3C1-, CK3OUT & CK3OUT-WERE CPU RUNIN. CPURUN, CPURUN- RESPECTIVELY AT D-2. SK3D1- WAS SYSCLK-. (4) SH 4: AT C-2 ADDED CT1-6 & CB1-53 TO 003-E1 & PINS 9, 10, 11 TO 001-E0 AT B-3. (5) SH 6: ADDED CT1-1 THRU 26 TO CB001-1, 2, 79, 6 & CT2-1 THRU 34 TO CB002-1, 2, 79 & P0 AT A-3	1-15-72	
E	CN 396 476 (C) (1) REVISED FLIP-FLOPS ON SHEETS 1, 3, 4, 5 & 6 AS FOL: ADDED VCC, RESET A-, RESET B-, RESET A-1, PINS 4 & 1; 10 & 13; PR & CL RESPECTIVELY (2) SN1: ADDED CB4-33 & CB3-17 TO 003, B0-2 (3) ADDED CB4-33 TO CHANGE Q AT ZONE A4. (4) SH 5, B-3: SIGNATURE ON DEV 7- WAS ON DEV 6-. (5) SH 6, E-3: DEVICE 004 B2 PIN 6 WAS AG, 6Q- WAS AG, 0Q- (6) SN 1: B3, C3, D3: ADDED PIN 6, 8, 8, 6, 6, 6, 8 AND SIGNATURES RESPECTIVELY	11/21/71	
F	CN 396 495 (C) (1) REVISED PER EXTENSIVE ENG CHANGE	1/21/72	
G	CN 412 962 (D)	5/17/72	

-0002 QTY REQ	-0001 QTY REQ	ITEM NO.	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER

LIST OF MATERIALS

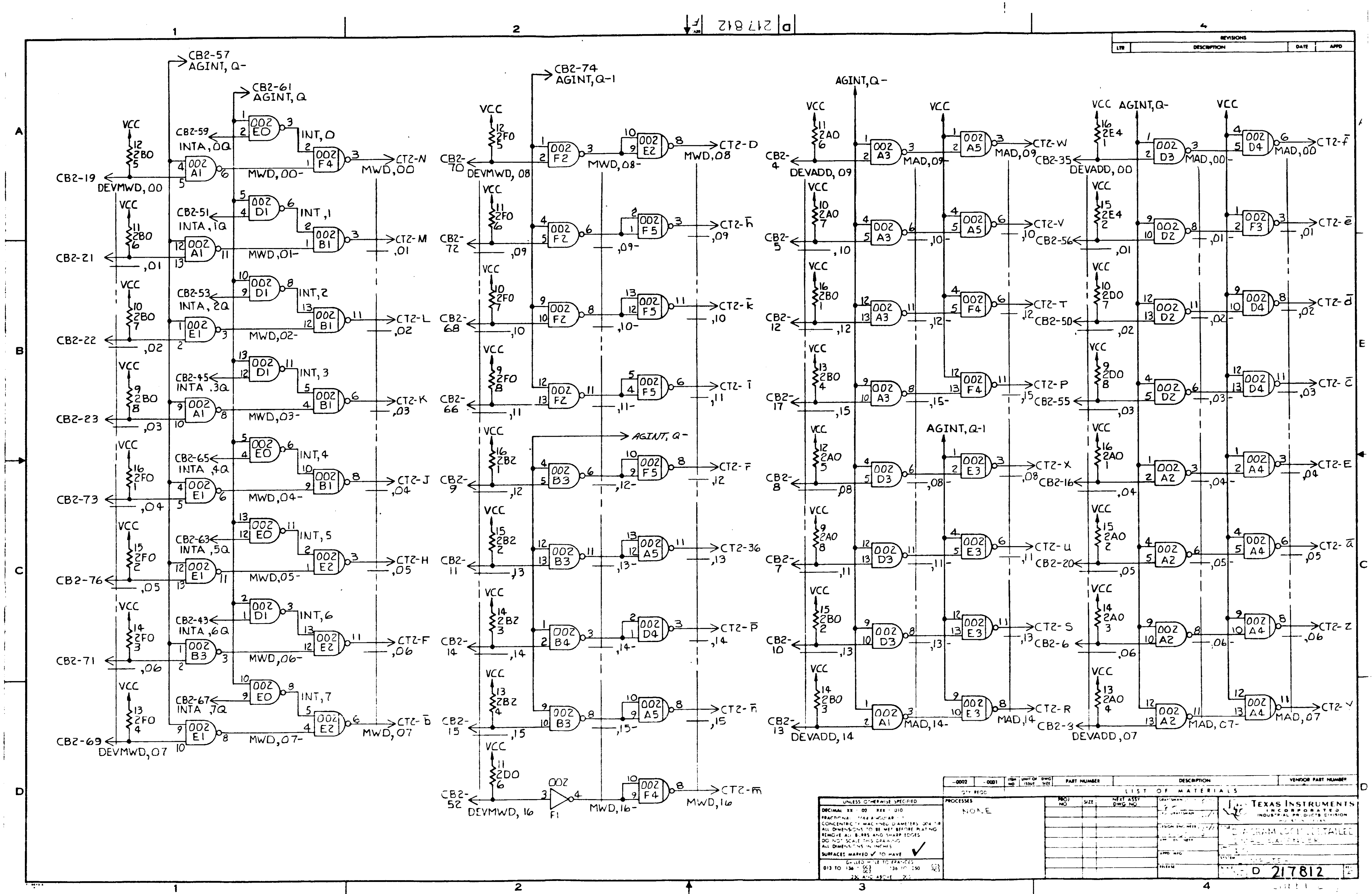
UNLESS OTHERWISE SPECIFIED
DECIMAL XX ± .02 XXX ± .010
FRACTIONS ± ANGULAR ±
CONFORM TO MACHINED PARTS .004 TIR
ALL DIMENSIONS TO BE MET BEFORE PLATING
REMOVE ALL BURRS AND SHARP EDGES
DO NOT SCALE THIS DRAWING
ALL DIMENSIONS IN INCHES
SURFACES MARKED √ TO HAVE
EXCEPTIONS TO TOLERANCES
.013 TO 125 ±.003 .126 TO 250 ±.005
250 AND OVER ±.010

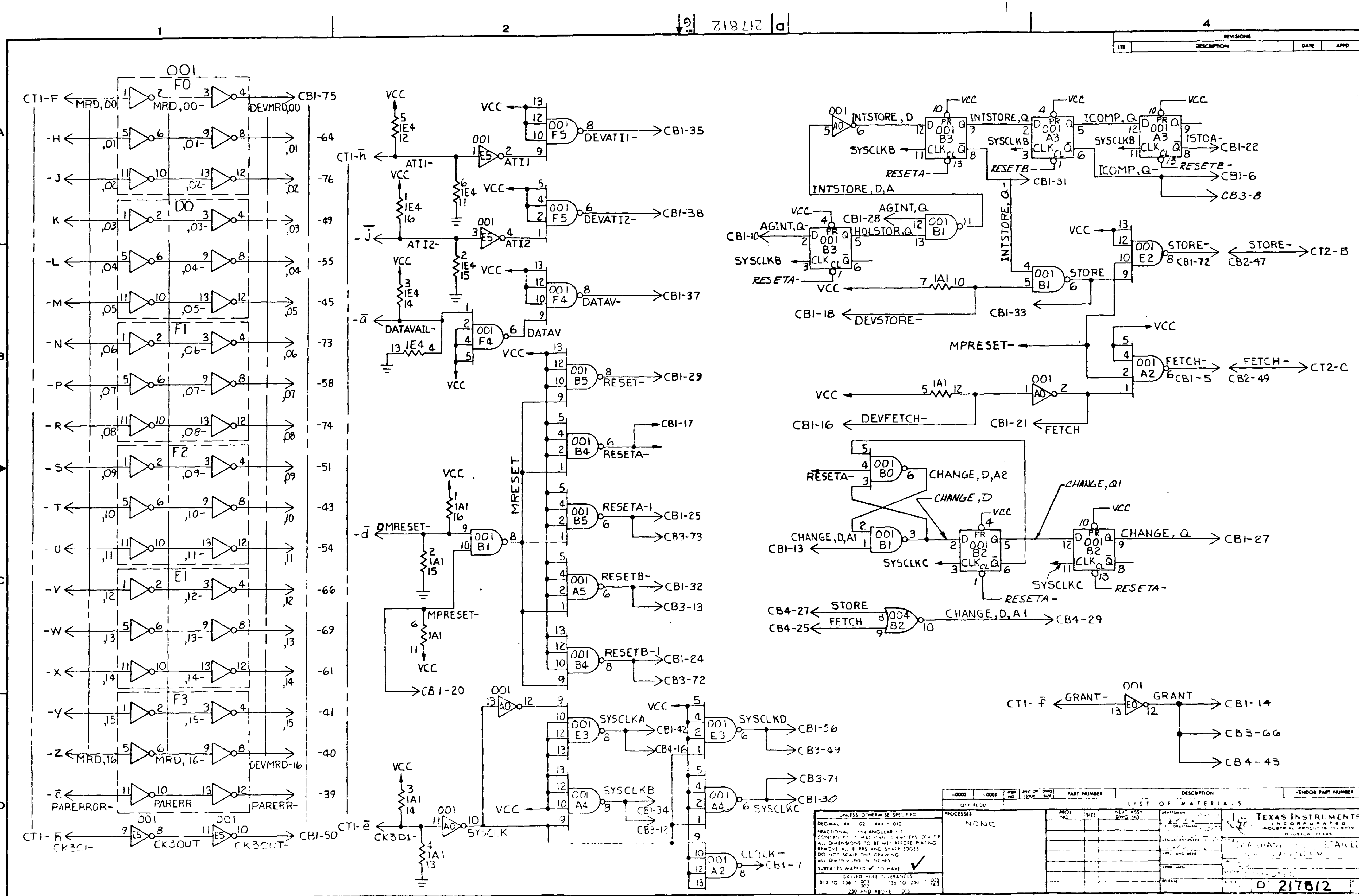
PROCESSES
FINISH

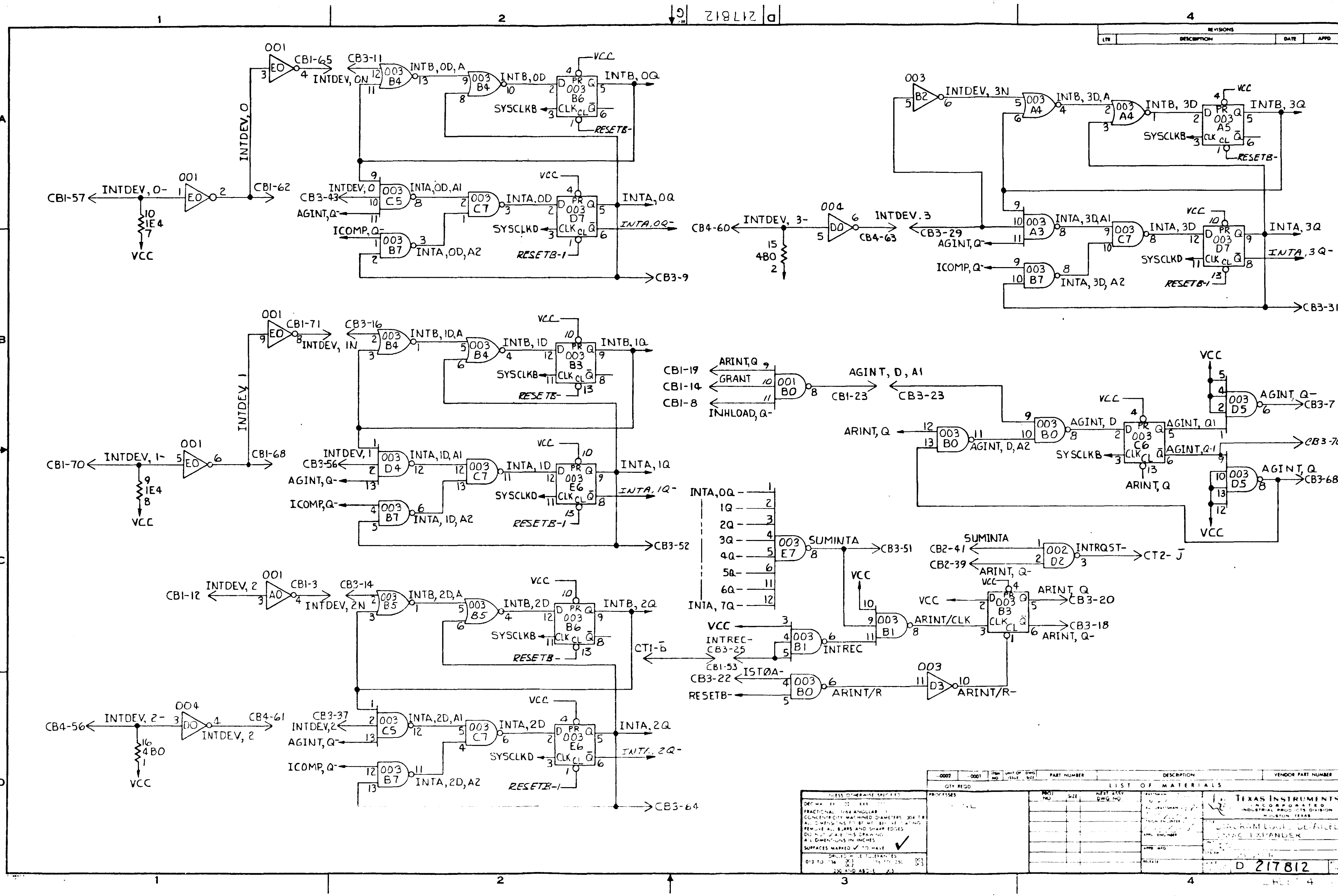
PROJ NO. | SIZE | NEXT ASSY DWG NO. | PATTERN | FSCM NO. | MATERIAL

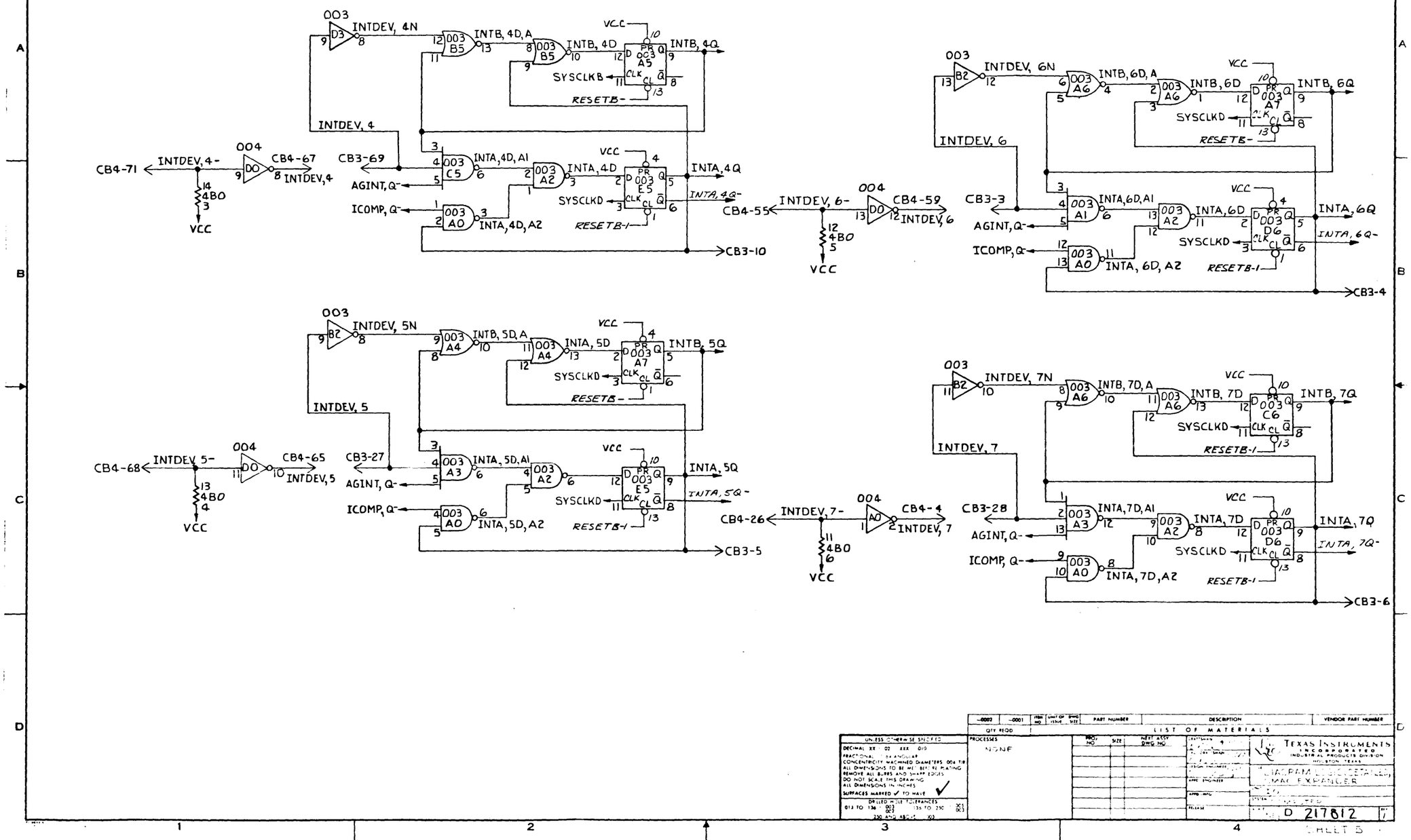
TEXAS INSTRUMENTS INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

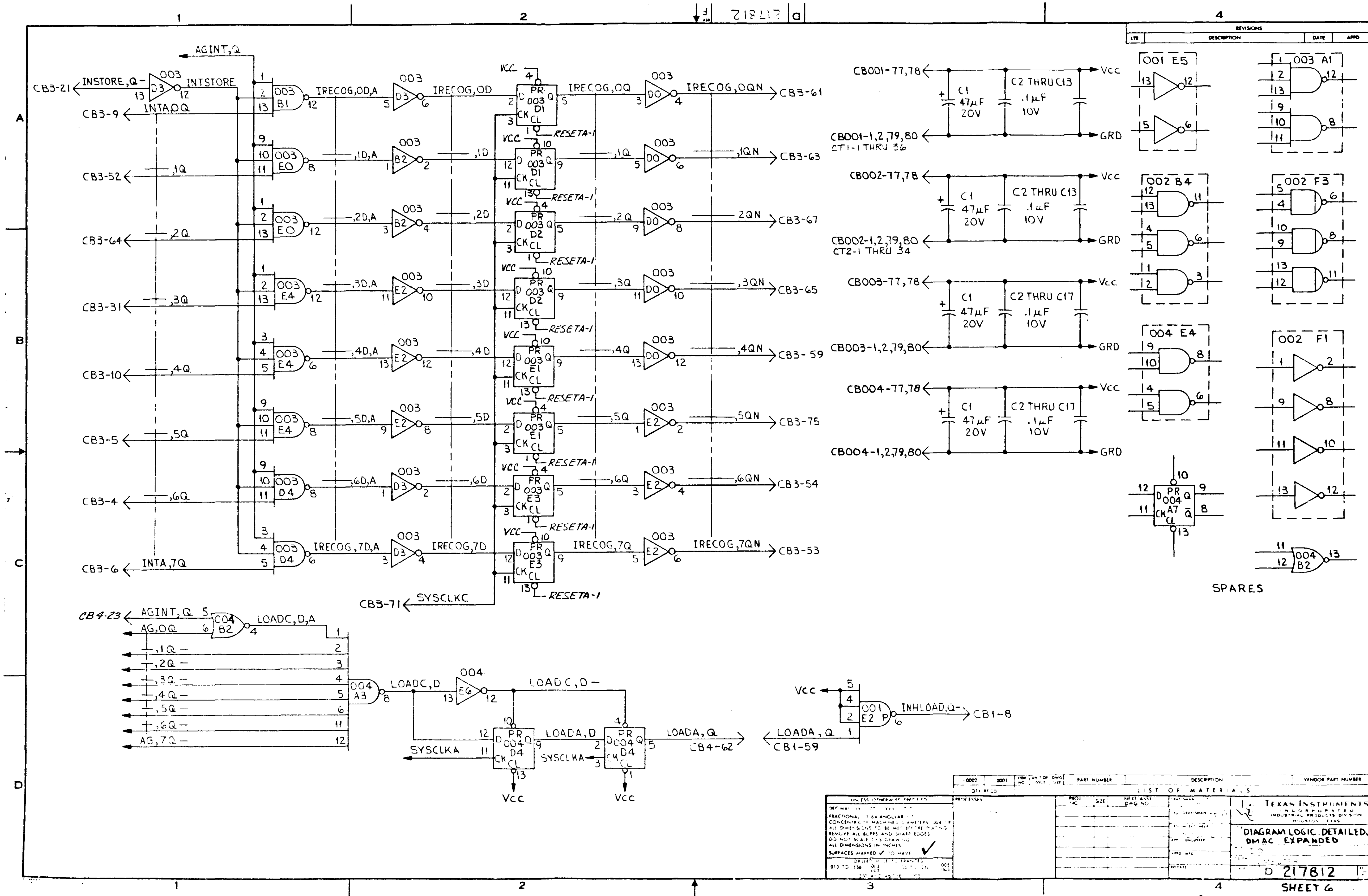
DIAGRAM LOGIC, DETAILED, DMAC EXPANDED
I/O
COMPUTER
D 217812
SHEET 1 OF 6


D 217812
CB2-57 AGINT, Q-
CB2-61 AGINT, Q
CB2-74 AGINT, Q-1
AGINT, Q-
AGINT, Q-1
VCC
CB2-19 DEVMWD, 00
CB2-21 ,01
CB2-22 ,02
CB2-23 ,03
CB2-73 ,04
CB2-76 ,05
CB2-71 ,06
CB2-69 DEVMWD, 07
CB2-59 INTA, 0Q
CB2-51 INTA, 1Q
CB2-53 INTA, 2Q
CB2-45 INTA, 3Q
CB2-65 INTA, 4Q
CB2-63 INTA, 5Q
CB2-43 INTA, 6Q
CB2-67 INTA, 7Q
INT, 0
INT, 1
INT, 2
INT, 3
INT, 4
INT, 5
INT, 6
INT, 7
MWD, 00-
MWD, 01-
MWD, 02-
MWD, 03-
MWD, 04-
MWD, 05-
MWD, 06-
MWD, 07-
CT2-N MWD, 00
CT2-M ,01
CT2-L ,02
CT2-K ,03
CT2-J ,04
CT2-H ,05
CT2-F ,06
CT2-b MWD, 07
CB2-70 DEVMWD, 08
CB2-72 ,09
CB2-68 ,10
CB2-66 ,11
CB2-9 ,12
CB2-11 ,13
CB2-14 ,14
CB2-15 ,15
CB2-52 DEVMWD, 16
MWD, 08-
MWD, 16-
CT2-D MWD, 08
CT2-h ,09
CT2-k ,10
CT2-l ,11
CT2-f ,12
CT2-36 ,13
CT2-p ,14
CT2-n ,15
CT2-m MWD, 16
CB2-4 DEVADD, 09
CB2-5 ,10
CB2-12 ,12
CB2-17 ,15
CB2-8 ,08
CB2-7 ,11
CB2-10 ,13
CB2-13 DEVADD, 14
MAD, 09
MAD, 14-
CT2-W MAD, 09
CT2-V ,10
CT2-T ,12
CT2-P ,15
CT2-X ,08
CT2-U ,11
CT2-S ,13
CT2-R MAD, 14
CB2-35 DEVADD, 00
CB2-56 ,01
CB2-50 ,02
CB2-55 ,03
CB2-16 ,04
CB2-20 ,05
CB2-6 ,06
CB2-3 DEVADD, 07
MAD, 00-
MAD, C7-
CT2-f MAD, 00
CT2-e ,01
CT2-d ,02
CT2-c ,03
CT2-E ,04
CT2-a ,05
CT2-Z ,06
CT2-Y MAD, 07
REVISIONS
LTR DESCRIPTION DATE APPD
LIST OF MATERIALS
PART NUMBER DESCRIPTION VENDOR PART NUMBER
UNLESS OTHERWISE SPECIFIED
PROCESSES NONE
TEXAS INSTRUMENTS INCORPORATED
D 217812


D 217812
001 F0
CT1-F MRD,00 MRD,00- DEVMRD,00 CB1-75
001 D0
F1
F2
E1
F3
MRD,16 MRD,16- DEVMRD-16
PARERROR- PARERR PARERR-
CT1-h CK3C1- CK3OUT CK3OUT- CB1-50
VCC
CT1-h ATI1- ATI1 DEVATI1- CB1-35
CT1-J ATI2- ATI2 DEVATI2- CB1-38
DATAVAIL- DATAV DATAV- CB1-37
RESET- CB1-29
MRESET
RESETA- CB1-17
RESETA-1 CB1-25 CB3-73
RESETB- CB1-32 CB3-13
RESETB-1 CB1-24 CB3-72
DMRESET-
MPRESET-
CB1-20
CT1-e CK3D1- SYSCLK
SYSCLKA CB1-42 CB4-16
SYSCLKB CB1-34 CB3-12
SYSCLKD CB1-56 CB3-49
SYSCLKC CB3-71 CB1-30
CLOCK- CB1-7
INTSTORE,D INTSTORE,Q ICOMP,Q ISTOA- CB1-22
SYSCLKB RESETA- RESETB- CB1-31
ICOMP,Q- CB1-6 CB3-8
INTSTORE,D,A
AGINT,Q CB1-28 HOLSTOR,Q
CB1-10 AGINT,Q-
RESETA-
STORE- CB1-72 STORE- CB2-47 CT2-B
STORE
CB1-18 DEVSTORE- CB1-33
MPRESET-
FETCH- CB1-5 FETCH- CB2-49 CT2-C
CB1-16 DEVFETCH- CB1-21 FETCH
CHANGE,D,A2
CHANGE,D
CHANGE,Q1
CHANGE,Q CB1-27
CHANGE,D,A1 CB1-13
SYSCLKC RESETA-
CB4-27 STORE
CB4-25 FETCH
CHANGE,D,A1 CB4-29
CT1-f GRANT- GRANT CB1-14 CB3-66 CB4-43
REVISIONS
LTR DESCRIPTION DATE APPD
PART NUMBER DESCRIPTION VENDOR PART NUMBER
LIST OF MATERIALS
PROCESSES NONE
TEXAS INSTRUMENTS
INCORPORATED
D 217812


D 217812
INTDEV, 0-
CB1-57
CB1-62
INTDEV, 0
CB1-65
INTDEV, 0N
CB3-11
INTB, 0D, A
INTB, 0D
INTB, 0Q
SYSCLKB
RESETB-
INTDEV, 0
CB3-43
AGINT, Q-
INTA, 0D, A1
INTA, 0D
INTA, 0Q
SYSCLKD
INTA, 0Q-
ICOMP, Q-
INTA, 0D, A2
RESETB-1
CB3-9
VCC
INTDEV, 1-
CB1-70
CB1-68
INTDEV, 1
CB1-71
INTDEV, 1N
CB3-16
INTB, 1D, A
INTB, 1D
INTB, 1Q
CB3-56
INTA, 1D, A1
INTA, 1D
INTA, 1Q
INTA, 1Q-
INTA, 1D, A2
CB3-52
INTDEV, 2
CB1-12
CB1-3
INTDEV, 2N
CB3-14
INTB, 2D, A
INTB, 2D
INTB, 2Q
INTDEV, 2-
CB4-56
CB4-61
CB3-37
INTA, 2D, A1
INTA, 2D
INTA, 2Q
INTA, 2Q-
INTA, 2D, A2
CB3-64
INTDEV, 3N
INTB, 3D, A
INTB, 3D
INTB, 3Q
INTDEV, 3-
CB4-60
INTDEV, 3
CB4-63
CB3-29
INTA, 3D, A1
INTA, 3D
INTA, 3Q
INTA, 3Q-
INTA, 3D, A2
CB3-31
CB1-19
CB1-14
CB1-8
ARINT, Q
GRANT
INHLOAD, Q-
AGINT, D, A1
CB1-23
CB3-23
AGINT, D
AGINT, Q1
AGINT, Q-1
AGINT, Q-
CB3-7
CB3-70
AGINT, D, A2
AGINT, Q
CB3-68
INTA, 0Q
1Q
2Q
3Q
4Q
5Q
6Q
INTA, 7Q
SUMINTA
CB3-51
CB2-41
CB2-39
ARINT, Q-
INTRQST-
CT2-J
ARINT/CLK
CB3-20
CB3-18
INTREC-
CB3-25
INTREC
CT1-D
CB1-53
CB3-22
IST0A-
RESETB-
ARINT/R
ARINT/R-
TEXAS INSTRUMENTS
LIST OF MATERIALS
D 217812


003
INTDEV, 4N
INTB, 4D, A
INTB, 4D
INTB, 4Q
SYSCLKB
RESETB-
INTDEV, 4
004
CB4-71
INTDEV, 4-
CB4-67
INTDEV, 4
4B0
VCC
CB3-69
INTA, 4D, AI
INTA, 4D
INTA, 4Q
AGINT, Q-
ICOMP, Q-
INTA, 4D, A2
SYSCLKD
RESETB-1
INTA, 4Q-
CB3-10
CB4-55
INTDEV, 6-
CB4-59
INTDEV, 6
INTDEV, 6N
INTB, 6D, A
INTB, 6D
INTB, 6Q
INTDEV, 6
CB3-3
INTA, 6D, AI
INTA, 6D
INTA, 6Q
INTA, 6D, A2
INTA, 6Q-
CB3-4
INTDEV, 5N
INTB, 5D, A
INTA, 5D
INTB, 5Q
INTDEV, 5
INTDEV, 5-
CB4-65
CB4-68
INTDEV, 5
CB3-27
INTA, 5D, AI
INTA, 5Q
INTA, 5D, A2
INTA, 5Q-
CB3-5
CB4-26
INTDEV, 7-
CB4-4
INTDEV, 7
INTDEV, 7N
INTB, 7D, A
INTB, 7D
INTB, 7Q
INTDEV, 7
CB3-28
INTA, 7D, AI
INTA, 7D
INTA, 7Q
INTA, 7D, A2
INTA, 7Q-
CB3-6
PROCESSES
NONE
TEXAS INSTRUMENTS
INCORPORATED
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS
D 217812
SHEET 5



AGINT,Q
CB3-21 INSTORE,Q- 003 D3 INTSTORE
CB3-9 INTA,0Q
003 B1 IRECOG,0D,A 003 D3 IRECOG,0D
VCC PR 003 D1 CK CL
IRECOG,0Q 003 D0 IRECOG,0QN CB3-61
RESETA-1
CB3-52 ,1Q 003 E0 ,1D,A 003 B2 ,1D ,1Q ,1QN CB3-63
CB3-64 ,2Q 003 E0 ,2D,A 003 B2 ,2D ,2Q ,2QN CB3-67
CB3-31 ,3Q 003 E4 ,3D,A 003 E2 ,3D ,3Q ,3QN CB3-65
CB3-10 ,4Q 003 E4 ,4D,A 003 E2 ,4D ,4Q ,4QN CB3-59
CB3-5 ,5Q 003 E4 ,5D,A 003 E2 ,5D ,5Q ,5QN CB3-75
CB3-4 ,6Q 003 D4 ,6D,A 003 D3 ,6D ,6Q ,6QN CB3-54
CB3-6 INTA,7Q 003 D4 IRECOG,7D,A 003 D3 IRECOG,7D IRECOG,7Q 003 E2 IRECOG,7QN CB3-53
CB3-71 SYSCLKC
CB4-23 AGINT,Q AG,0Q 004 B2 LOADC,D,A
,1Q ,2Q ,3Q ,4Q ,5Q ,6Q AG,7Q
004 A3 LOADC,D 004 E6 LOADC,D-
SYSCLKA 004 D4 LOADA,D SYSCLKA 004 D4 LOADA,Q CB4-62
Vcc Vcc
Vcc 001 E2 INHLOAD,Q- CB1-8
LOADA,Q CB1-59
CB001-77,78 C1 47μF 20V C2 THRU C13 .1μF 10V Vcc
CB001-1,2,79,80 CT1-1 THRU 36 GRD
CB002-77,78 C1 47μF 20V C2 THRU C13 .1μF 10V Vcc
CB002-1,2,79,80 CT2-1 THRU 34 GRD
CB003-77,78 C1 47μF 20V C2 THRU C17 .1μF 10V Vcc
CB003-1,2,79,80 GRD
CB004-77,78 C1 47μF 20V C2 THRU C17 .1μF 10V Vcc
CB004-1,2,79,80 GRD
001 E5
003 A1
002 B4
002 F3
004 E4
002 F1
PR 004 A7 CK CL
004 B2
SPARES
REVISIONS
LTR DESCRIPTION DATE APPD
LIST OF MATERIALS
PART NUMBER DESCRIPTION VENDOR PART NUMBER
TEXAS INSTRUMENTS INCORPORATED INDUSTRIAL PRODUCTS DIVISION HOUSTON, TEXAS
DIAGRAM LOGIC DETAILED, DMAC EXPANDED
D 217812
SHEET 6

SECTION VI

CONNECTOR PLATE WIRING INFORMATION

Information concerning backpanel wiring for controllers contained in the various DMAC Expansion Configuration options is shown in table 6-1. Also included are configuration charts for these options to aid in controller card insertion.

The kits include the wired connector plate, the four DMAC expander card assemblies, and the connecting cable. They do not include the chassis nor the DMAC device controllers, which are purchased separately. Load Lists and Pin Lists for the various configurations are also available.

Table 6-1. Configuration Information

External DMAC Expansion Configuration Options		DMAC Expander	FHD (DDC)	MHD (DIABLO)	979 Transport (T.I.)	Line Printer	DMAC/BTC Adaptor	DMAC Port Pairs	I/O Bus Expander	I/C Bus Connectors	Blank Connectors	*Note Number	Appendix	Appendix Dash No. (216759)
DMAC Expansion Kit Part Number	Wired Connector Plate Part Number													
966555-0001	966437-0001	1	1	1	1	1	1						J	9711
966555-0002	966437-0002	1									24		K	9712
966555-0003	966437-0003	1	2	1	1	1								
960328-0001	240788-0003	1	1	1	1	1								
960328-0002	240788-0004	1		1	1						16			
960328-0003	240788-0007	1		2							16			
960328-0005	240788-0009	1				1	1	1			29	1		
960328-0006	240788-0010	1	1		2	1								
960328-0008	240788-0011	1	2								15	2		
216694-0002	216695-0002	1						2			20			
216694-0003	216695-0003	1	*	*		1		1				3		
216694-0004	216695-0004	1			1	1		1						
216694-0006	216695-0006	1									12	2		
216694-0007	216695-0007	1	1									2		
955156-0004	240788-0005	1	*	*	1	1			1	8		3		
955156-0007	240788-0006	1	1		1			2	1	10				

*NOTES

1. Kit additionally contains wiring for 3 unassigned BTC kits for user custom applications.
2. Kit additionally contains wiring for 2 unassigned BTC kits for user custom applications.
3. Wiring for MHD and FHD controllers is such that either, but not both, kit may be installed.

Accessory Kit, DMAC Expander 966555-0001 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP No. 2	216709-0001	EXP No. 4	B28
B25	216700-0001	EXP No. 1	216706-0001	EXP No. 3	B26
B23	961646-0001	PADDLE	217070-0001	LP No. 2	B24
B21	217073-0001	LP No. 3	217067-0001	LP No. 1	B22
B19					B20
B17	961644-0001	DDC No. 3	966462-0001	BTC No. 3	B18
B15					B16
B13	961624-0001	DDC No. 2	966464-0001	BTC No. 2	B14
B11					B12
B9	961622-0001	DDC No. 1	966466-0001	BTC No. 1	B10
B7					B8
B5	961632-0001	MHD No. 4	966462-0001	BTC No. 3	B6
B3					B4
B1	961630-0001	MHD No. 3	966464-0001	BTC No. 2	B2

Accessory Kit, DMAC Expander 966555-0001 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27					A28
A25	961628-0001	MHD No. 2	966466-0001	BTC No. 1	A26
A23					A24
A21	961626-0001	MHD No. 1	961636-0001	MHD No. 6	A22
A19					A20
A17	240652-0001	TCL No. 5	961634-0001	MHD No. 5	A18
A15					A16
A13	240650-0001	TCL No. 4	966462-0001	BTC No. 3	A14
A11					A12
A9	240648-0001	TCL No. 3	966464-0001	BTC No. 2	A10
A7					A8
A5	240646-0001	TCL No. 2	966466-0001	BTC No. 1	A6
A3					A4
A1	240644-0001	TCL No. 1	240654-0001	TCL No. 6	A2

A2 Not Used

For 966555-0002

Accessory Kit, DMAC Expander 966555-0002 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27	216703-0001	EXP 2	216709-0001	EXP 4	A28
A25	216700-0001	EXP 1	216706-0001	EXP 3	A26
A23					A24
A21					A22
A19					A20
A17					A18
A15					A16
A13					A14
A11					A12
A9					A10
A7					A8
A5					A6
A3					A4
A1					A2

Accessory Kit, DMAC Expander 966555-0003 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	216700-0001	EXP 1	216706-0001	EXP 3	B26
B23	961646-0001	PADDLE	217070-0001	LP 2	B24
B21	217073-0001	LP 3	217067-0001	LP 1	B22
B19					B20
B17	961626-0001	MHD 1	961634-0001	MHD 5	B18
B15					B16
B13	961628-0001	MHD 2	961636-0001	MHD 6	B14
B11					B12
B9	961630-0001	MHD 3	966466-0001	BTC 1	B10
B7			966464-0001	BTC 2	B8
B5	961632-0001	MHD 4	966462-0001	BTC 3	B6
B3					B4
B1	961626-0001	MHD 1	961634-0001	MHD 5	B2

Accessory Kit, DMAC Expander 966555-0003 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27					A28
A25	961628-0001	MHD 2	961636-0001	MHD 6	A26
A23					A24
A21	961630-0001	MHD 3	966466-0001	BTC 1	A22
A19			966464-0001	BTC 2	A20
A17	961632-0001	MHD 4	966462-0001	BTC 3	A18
A15					A16
A13	240644-0001	TCL 1	966466-0001	BTC 1	A14
A11			966464-0001	BTC 2	A12
A9	240646-0001	TCL 2	966462-0001	BTC 3	A10
A7					A8
A5	240648-0001	TCL 3	240652-0001	TCL 5	A6
A3					A4
A1	240650-0001	TCL 4	240654-0001	TCL 6	A2

Accessory Kit, DMAC Expander 960328-0001 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	216700-0001	EXP 1	216706-0001	EXP 3	B26
B23	217067-0001	LP 1	217070-0001	LP 2	B24
B21	217073-0001	LP 3			B22
B19					B20
B17	961622-0001	DDC 1	961644-0001	DDC 3	B18
B15					B16
B13	961624-0001	DDC 2	966466-0001	BTC 1	B14
B11					B12
B09	966462-0001	BTC 3	966464-0001	BTC 2	B10
B07					B08
B05	966462-0001	BTC 3	966466-0001	BTC 1	B06
B03					B04
B01	961626-0001	MHD 1	966464-0001	BTC 2	B02

Accessory Kit, DMAC Expander 960328-0001 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27					A28
A25	961628-0001	MHD 2	961632-0001	MHD 4	A26
A23					A24
A21	961630-0001	MHD 3	961634-0001	MHD 5	A22
A19					A20
A17	966462-0001	BTC 3	961636-0001	MHD 6	A18
A15					A16
A13	240644-0001	TCL 1	966466-0001	BTC 1	A14
A11					A12
A09	240646-0001	TCL 2	966464-0001	BTC 2	A10
A07					A08
A25	240648-0001	TCL 3	240652-0001	TCL 5	A06
A03					A04
A01	240650-0001	TCL 4	240654-0001	TCL 6	A02

Accessory Kit, DMAC Expander 960328-0002 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	216700-0001	EXP 1	216706-0001	EXP 3	B26
B23					B24
B21	966462-0001	BTC 3	966466-0001	BTC 1	B22
B19					B20
B17	961632-0001	MHD 4	966464-0001	BTC 2	B18
B15					B16
B13	961630-0001	MHD 3	961636-0001	MHD 6	B14
B11					B12
B09	961628-0001	MHD 2	961634-0001	MHD 5	B10
B07					B08
B05	961626-0001	MHD 1	966466-0001	BTC 1	B06
B03					B04
B01	966462-0001	BTC 3	966464-0001	BTC 2	B02

Accessory Kit, DMAC Expander 960328-0002 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27					A28
A25	240648-0001	TCL 3	240654-0001	TCL 6	A26
A23					A24
A21	240646-0001	TCL 2	240652-0001	TCL 5	A22
A19					A20
A17	240644-0001	TCL 1	240650-0001	TCL 4	A18
A15					A16
A13					A14
A11					A12
A09					A10
A07					A08
A05					A06
A03					A04
A01					A02

Accessory Kit, DMAC Expander 960328-0003 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	216700-0001	EXP 1	216706-0001	EXP 3	B26
B23					B24
B21	966462-0001	BTC 3	966466-0001	BTC 1	B22
B19					B20
B17	961932-0001	MHD 4	966464-0001	BTC 2	B18
B15					B16
B13	961630-0001	MHD 3	961636-0001	MHD 6	B14
B11					B12
B09	961628-0001	MHD 2	961634-0001	MHD 5	B10
B07					B08
B05	961626-0001	MHD 1	966466-0001	BTC 1	B06
B03					B04
B01	966462-0001	BTC 3	966464-0001	BTC 2	B02

Accessory Kit, DMAC Expander 960328-0003 (A1)

Location	Assembly	Modules	Assembly	Module	Location
A27					A28
A25	961630-0001	MHD 3	961636-0001	MHD 6	A26
A23					A24
A21	961628-0001	MHD 2	961634-0001	MHD 5	A22
A19					A20
A17	961626-0001	MHD 1	961632-0001	MHD 4	A18
A15					A16
A13					A14
A11					A12
A09					A10
A07					A08
A05					A06
A03					A04
A01					A02

Accessory Kit, DMAC Expander 960328-0005 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	216700-0001	EXP 1	216706-0001	EXP 3	B26
B23	217073-0001	LP 3			B24
B21	217070-0001	LP 2	966462-0001	BTC 3	B22
B19	217067-0001	LP 1			B20
B17		PORT B	966464-0001	BTC 2	B18
B15		PORT A			B16
B13	961646-0001	PADDLE	966466-0001	BTC 1	B14
B11					B12
B09					B10
B07					B08
B05					B06
B03					B04
B01					B02

Accessory Kit, DMAC Expander 960328-0005 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27			966462-0001	BTC 3	A28
A25					A26
A23			966464-0001	BTC 2	A24
A21					A22
A19			966466-0001	BTC 1	A20
A17					A18
A15					A16
A13					A14
A11					A12
A09			966462-0001	BTC 3	A10
A07					A08
A05			966464-0001	BTC 2	A06
A03					A04
A01			966466-0001	BTC 1	A02

Accessory Kit, DMAC Expander 960328-0006 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	216700-0001	EXP 1	216706-0001	EXP 3	B26
B23	217067-0001	LP 1	217070-0001	LP 2	B24
B21	217073-0001	LP 3			B22
B19					B20
B17	961622-0001	DDC 1	961644-0001	DDC 3	B18
B15					B16
B13	961624-0001	DDC 2	966466-0001	BTC 1	B14
B11					B12
B09	966462-0001	BTC 3	966464-0001	BTC 2	B10
B07					B08
B05	966462-0001	BTC 3	966466-0001	BTC 1	B06
B03					B04
B01	240644-0001	TCL 1	966464-0001	BTC 2	B02

Accessory Kit, DMAC Expander 9606528-0006 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27					A28
A25	240646-0001	TCL 2	240654-0001	TCL 6	A26
A23					A24
A21	240648-0001	TCL 3	240652-0001	TCL 5	A22
A19					A20
A17	966462-0001	BTC 3	240650-0001	TCL 4	A18
A15					A16
A13	250644-0001	TCL 1	966466-0001	BTC 1	A14
A11					A12
A09	240646-0001	TCL 2	966464-0001	BTC 2	A10
A07					A08
A05	240648-0001	TCL 3	240654-0001	TCL 6	A06
A03					A04
A01	240650-0001	TCL 4	240652-0001	TCL 5	A02

Accessory Kit, DMAC Expander 960328-0008 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	216700-0001	EXP 1	216706-0001	EXP 3	B26
B23					B24
B21	961622-0001	DDC 1	961644-0001	DDC 3	B22
B19					B20
B17	961624-0001	DDC 2	966466-0001	BTC 1	B18
B15					B16
B13	966462-0001	BTC 3	966464-0001	BTC 2	B14
B11					B12
B09	961622-0001	DDC 1	961644-0001	DDC 3	B10
B07					B08
B05	961624-0001	DDC 2	966466-0001	BTC 1	B06
B03					B04
B01	966462-0001	BTC 3	966464-0001	BTC 2	B02

Accessory Kit, DMAC Expander 960328-0008 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27					A28
A25	966462-0001	BTC 3	966466-0001	BTC 1	A26
A23					A24
A21			966464-0001	BTC 2	A22
A19					A20
A17					A18
A15					A16
A13	966462-0001	BTC 3	966466-0001	BTC 1	A14
A11					A12
A09			966464-0001	BTC 2	A10
A07					A08
A05					A06
A03					A04
A01					A02

A2 Not Used

For 216694-0001

Accessory Kit, DMAC Expander 216694-0001 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27	216703-0001	EXP 2	216709-0001	EXP 4	A28
A25	216700-0001	EXP 1	216706-0001	EXP 3	A26
A23	216779-0001		216782-0001		A24
A21	216785-0001		216776-0001		A22
A19	216773-0001		217070-0001	LP 2	A20
A17	217073-0001	LP 3	217067-0001	LP 1	A18
A15	216827-0001		216830-0001		A16
A13	216821-0001		216824-0001		A14
A11	216815-0001		216818-0001		A12
A09	216809-0001		216812-0001		A10
A07	216803-0001		216806-0001		A08
A05	216797-0001		216800-0001		A06
A03		Port 2A		Port 2B	A04
A01		Port 1A		Port 1B	A02

A2 Not Used

For 216694-0002

Accessory Kit, DMAC Expander 216694-0002 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27	216703-0001	EXP 2	216709-0001	EXP 4	A28
A25	216700-0001	EXP 1	216706-0001	EXP 3	A26
A23		PORT 2A		PORT 2B	A24
A21		PORT 1A		PORT 1B	A22
A19					A20
A17					A18
A15					A16
A13					A14
A11					A12
A09					A10
A07					A08
A05					A06
A03					A04
A01					A02

A2 Not Used

For 216694-0003

Accessory Kit, DMAC Expander 216694-0003 (A2)

Location	Assembly	Module	Assembly	Module	Location
A27	216703-0001	EXP 2	216709-0001	EXP 4	A28
A25	216700-0001	EXP 1	216706-0001	EXP 3	A26
A23	217067-0001	LP 1	217070-0001	LP 2	A24
A21	217073-0001	LP 3			A22
A19		PORT B			A20
A17		PORT A	966464-0001	BTC 2	A18
A15					A16
A13	966462-0001	BTC 3	966466-0001	BTC 1	A14
A11					A12
A09	961626-0001	MHD 1	961632-0001	MHD 4	A10
A07	961622-0001	DDC 1	961644-0001	DDC 3	A08
A05	961628-0001	MHD 2	961634-0001	MHD 5	A06
A03	961624-0001	DDC 2			A04
A01	961630-0001	MHD 3	961636-0001	MHD 6	A02

A2 Not Used

For 216694-0004

Accessory Kit, DMAC Expander 216694-0004 (A2)

Location	Assembly	Module	Assembly	Module	Location
A27	216703-0001	EXP 2	216709-0001	EXP 4	A28
A25	216700-0001	EXP 1	216706-0001	EXP 3	A26
A23	217067-0001	LP 1	217070-0001	LP 2	A24
A21	217073-0001	LP 3			A22
A19		PORT B			A20
A17		PORT A	966464-0001	BTC 2	A18
A15					A16
A13	966462-0001	BTC 3	966466-0001	BTC 1	A14
A11					A12
A09	240664-0001	TCL 1	240650-0001	TCL 4	A10
A07					A08
A05	240646-0001	TCL 2	240652-0001	TCL 5	A06
A03					A04
A01	240648-0001	TCL 3	240654-0001	TCL 6	A02

A2 Not Used

For 216694-0006

Accessory Kit, DMAC Expander 216694-0006 (A2)

Location	Assembly	Module	Assembly	Module	Location
A27	216703-0001	EXP 2	216709-0001	EXP 4	A28
A25	216700-0001	EXP 1	216706-0001	EXP 3	A26
A23					A24
A21	966462-0001	BTC 3	966462-0001	BTC 3X	A22
A19					A20
A17	966464-0001	BTC 2	966464-0001	BTC 2X	A18
A15					A16
A13	966466-0001	BTC 1	966466-0001	BTC 1X	A14
A11					A12
A09					A10
A07					A08
A05					A06
A03					A04
A01					A02

A2 Not Used

For 216694-0007

Accessory Kit, DMAC Expander 216694-0007 (A2)

Location	Assembly	Module	Assembly	Module	Location
A27	216703-0001	EXP 2	216709-0001	EXP 4	A28
A25	216700-0001	EXP 1	216706-0001	EXP 3	A26
A23					A24
A21	966462-0001	BTC 3	966462-0001	BTC 3X	A22
A19					A20
A17	966464-0001	BTC 2	966464-0001	BTC 2X	A18
A15					A16
A13	966466-0001	BTC 1	966462-0001	BTC 1X	A14
A11					A12
A09	961644-0001	DDC 3	966462-0001	*BTC 3Y	A10
A07					A08
A05	961624-0001	DDC 2	966464-0001	*BTC 2Y	A06
A03					A04
A01	961622-0001	DDC 1	966466-0001	*BTC 1Y	A02

*BTCY Assigned to DDC Controller

A2 Not Used

For 216694-0008

Accessory Kit, DMAC Expander 216694-0008 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27	216703-0001	EXP 2	216709-0001	EXP 4	A28
A25	216700-0001	EXP 1	216706-0001	EXP 3	A26
A23					A24
A21		Port 1A		Port 1B	A22
A19		Port 2A		Port 2B	A20
A17					A18
A15		Port 3A		Port 3B	A16
A13		Port 4A		Port 4B	A14
A11					A12
A09		Port 5A		Port 5B	A10
A07		Port 6A		Port 6B	A08
A05					A06
A03		Port 7A		Port 7B	A04
A01		Port 8A		Port 8B	A02

Accessory Kit, DMAC Expander 955156-0004 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	216700-0001	EXP 1	216706-0001	EXP 3	B26
B23	217067-0001	LP 1	217070-0001	LP 2	B24
B21	217073-0001	LP 3			B22
B19			961636-0001	MHD 6	B20
B17					B18
B15	961628-0001	MHD 2	961634-0001	MHD 5	B16
B13	961622-0001	DDC 1	961644-0001	DDC 3	B14
B11	961626-0001	MHD 1	961632-0001	MHD 4	B12
B09			961624-0001	DDC 2	B10
B07	966466-0001	BTC 1	961630-0001	MHD 3	B08
B05					B06
B03	966464-0001	BTC 2	966462-0001	BTC 3	B04
B01					B02

Accessory Kit, DMAC Expander 955156-0004 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27	966466-0001	BTC 1	217535-0001	BOOT	A28
A25					A26
A23	966464-0001	BTC 2	966462-0001	BTC 3	A24
A21					A22
A19	240644-0001	TCL 1	240650-0001	TCL 4	A20
A17					A18
A15	240646-0001	TCL 2	240652-0001	TCL 5	A16
A13					A14
A11	240648-0001	TCL 3	240654-0001	TCL 6	A12
A09	980 I/O	I/O 6	980 I/O	I/O 3	A10
A07	980 I/O	I/O 8	980 I/O	I/O 5	A08
A05	980 I/O	I/O 12	980 I/O	I/O 9	A06
A03	980 I/O	I/O 14	980 I/O	I/O 11	A04
A01	217217-0001	I/O EXP 1	217219-0001	I/O EXP 2	A02

Accessory Kit, DMAC Expander 955156-0007 (A2)

Location	Assembly	Module	Assembly	Module	Location
B27	216703-0001	EXP 2	216709-0001	EXP 4	B28
B25	326700-0001	EXP 1	216706-0001	EXP3	B26
B23		PORT 2A		PORT 2B	B24
B21		PORT 1A		PORT 1A	B22
B19					B20
B17	240652-0001	TCL 5	240654-0001	TCL 6	B18
B15					B16
B13	240648-0001	TCL 3	240650-0001	TCL 4	B14
B11					B12
B09	240644-0001	TCL 1	240646-0001	TCL 2	B10
B07					B08
B05	966464-0001	BTC 2	966462-0001	BTC 3	B06
B03					B04
B01	217535-0001	BOOT	966466-0001	BTC 1	B02

Accessory Kit, DMAC Expander 955156-0007 (A1)

Location	Assembly	Module	Assembly	Module	Location
A27					A28
A25	966464-0001	BTC 2	966462-0001	BTC 3	A26
A23					A24
A21	961644-0001	DDC 3	966466-0001	BTC 1	A22
A19					A20
A17	961622-0001	DDC 1	961624-0001	DDC 2	A18
A15	217073-0001	LP 3			A16
A13	217067	LP 1	217070-0001	LP 2	A14
A11		I/O PORT 9		I/O PORT 10	A12
A09		I/O PORT 7		I/O PORT 8	A10
A07		I/O PORT 5		I/O PORT 6	A08
A05		I/O PORT 3		I/O PORT 4	A06
A03		I/O PORT 0		I/O PORT 2	A04
A01	217217-0001	I/O EXP 1	217219-0001	I/O EXP 2	A02

USER'S RESPONSE SHEET

Manual Title: Direct Memory Access Port Expander

Maintenance Manual (216759-9701)

Manual Date: 1 May 1976 **Date of This Letter:** _____

User's Name: _____ **Telephone:** _____

Company: _____ **Office/Department:** _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

CUT ALONG LINE

Location in Manual	Comment/Suggestion
_____	_____
	_____
	_____
	_____
_____	_____
	_____
	_____
	_____
_____	_____
	_____
	_____
	_____

NO POSTAGE NECESSARY IF MAILED IN U.S.A.
FOLD ON TWO LINES (LOCATED ON REVERSE SIDE), TAPE AND MAIL

FOLD

FIRST CLASS
PERMIT NO. 7284
DALLAS, TEXAS

BUSINESS REPLY MAIL
NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY

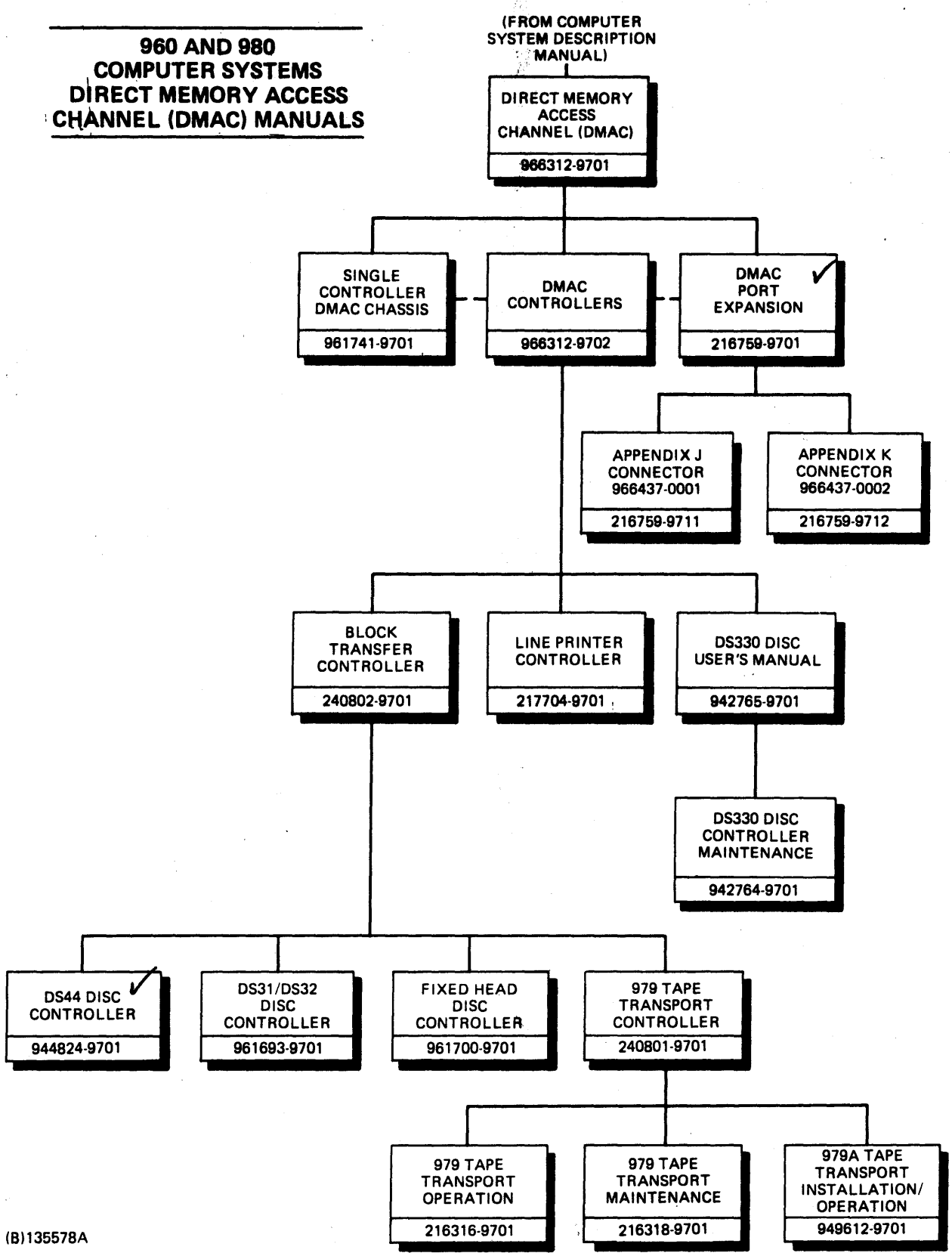
TEXAS INSTRUMENTS INCORPORATED
DIGITAL SYSTEMS DIVISION

P.O. BOX 2909 · AUSTIN, TEXAS 78769

ATTN: TECHNICAL PUBLICATIONS
MS 2146

FOLD

960 AND 980 COMPUTER SYSTEMS DIRECT MEMORY ACCESS CHANNEL (DMAC) MANUALS



(B)135578A

TEXAS INSTRUMENTS
INCORPORATED
DIGITAL SYSTEMS DIVISION
POST OFFICE BOX 2909 AUSTIN, TEXAS 78769