TEXAS INSTRUMENTS

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Model 980 Computer

Input/Output and Auxiliary Processor Port Manual

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PREFACE

This manual provides users of the Model 980A and 980B Computers with information about the input/output (I/O) bus and I/O bus expansion hardware. It also contains information for the personnel who install and maintain this hardware.

The description of the I/O bus includes interfaces, signals, and transfer of data. The functioning of the expansion system and the physical characteristics of the I/O bus are also presented. Individual sections cover the installation, operating instructions, and principles of operation of the I/O bus system.

An entire section is devoted to the auxiliary processor port on the Model 980 Computer chassis.

Related publications, including maintenance manual volumes and assembly language programming manuals, are as follows:

Title	TI Part Number
Model 980A Computer Maintenance Manual: System Description	960699-9701
Model 980B Computer Maintenance Manual: System Description	943012-9701
Model 980 Computer Maintenance Manual: Input/Output and Input/Output Expansion	960699-9704
Model 980 Computer Input/Output Data Module User's Manual	965956-9701
Model 980 Computer Assembly Language Programmer's Reference Manual	943013-9701
Model 980 Computer Assembly Language Input/Output	961961-9734

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SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

Input/output operations in the Texas Instruments Model 980 Computer are handled by an input/output (I/O) bus system. The fundamental element of this system is a 16-bit in, 16-bit out, parallel bus which is used to transfer single data words between the Central Processing Unit (CPU) and low- and medium-speed peripheral devices.

Signal lines are provided for transmission of data to or from the computer, control of data transfer, timing, and indication of hardware interrupt status. The I/O expander provides signal fanout and fanin capabilities required to permit several device controllers to share the I/O bus. The I/O expander may be located either within the 980 computer chassis or in a separate external chassis. Data and status transfers are initiated by two software instructions, one to read data and one to write data.

A separate section discusses the software instructions and the theory of operation of the auxiliary processor port in the 980 computer.

The functional diagram in figure 1-1 shows the relation of the I/O bus to the rest of the computer.

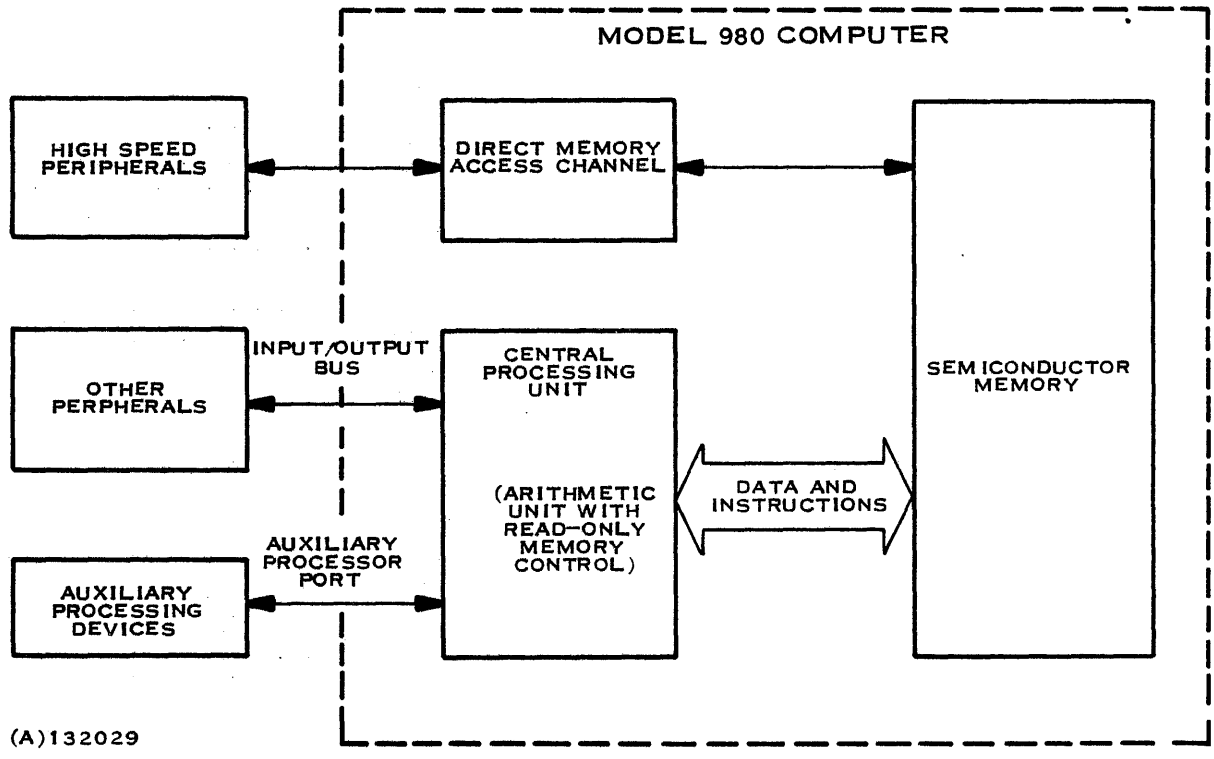


Figure 1-1. Model 980 Computer System Functional Diagram

1.2 I/O BUS CONFIGURATIONS

In order to complete the I/O interface between the CPU and peripheral hardware devices, any of three configurations may be used:

- *Basic I/O Bus.* Handles up to four devices. Five I/O ports on the computer chassis accommodate the I/O interface printed circuit card and up to four I/O device controller printed circuit cards.

- *Internal expansion.* Handles up to 13 devices. An optional expansion back panel in the 980 computer chassis accommodates additional printed circuit cards. I/O expander cards are required in addition to the interface and controller cards to provide I/O bus expansion.

- *External expansion.* Handles up to 256 devices. Expansion is accomplished in an I/O expansion chassis separate from the 980 computer chassis. Multiple expansion chassis are used if a large number of devices interface with the CPU.

1.3 INTERFACE DESCRIPTION

The computer communicates with the device controllers through 16 output lines (data or address), 16 input data lines, and a number of control and status lines. These lines may be expanded for communication with a number of controllers.

A simplified block diagram of the expanded interface between the 980 CPU I/O port and device controllers is shown in figure 1-2. If an expander is not included, the computer I/O interface module is required only for reading I/O interrupt line status.

1.3.1 **SIGNALS.** The functions of the data, control and status signals are summarized in table 1-1.

1.3.2 **I/O DATA TRANSFERS.** All data and status transfers between the computer and the device controllers connected to the I/O port are initiated by the 980 via two software instructions: Write Direct Single (WDS) and Read Direct Single (RDS). The WDS instruction is used to perform a 16-bit write to the addressed external device, and the RDS instruction performs a 16-bit read from the addressed external device. In each case, there is one instruction for each 16-bit data transfer.

1.3.3 **INSTRUCTION FORMAT.** Both WDS and RDS are two-word instructions within the 980 computer. A data word containing a character and/or control information is associated with each WDS or RDS instruction. When one of these instructions is executed, the first word is applied to the I/O data bus. During the second word, the 980 either sends a 16-bit data or command word to the device controller, or accepts a data or status word.

The WDS and RDS instructions are discussed in more detail in Section III.

1.3.4 **DATA TRANSFER CYCLES.** To start a data transfer cycle, the first word of the RDS or WDS instruction from the CPU is enabled to the output (write) data bus. A strobe pulse (GO) is generated which indicates to the external device, specified by the ER field of the instruction, that a valid GO word (same as the first word of the instruction) is on the output data bus. The external device examines bit 10 of the first word. If this bit is reset (logic 0), the device recognizes an RDS instruction; if it is set (logic 1), the device recognizes a WDS instruction.

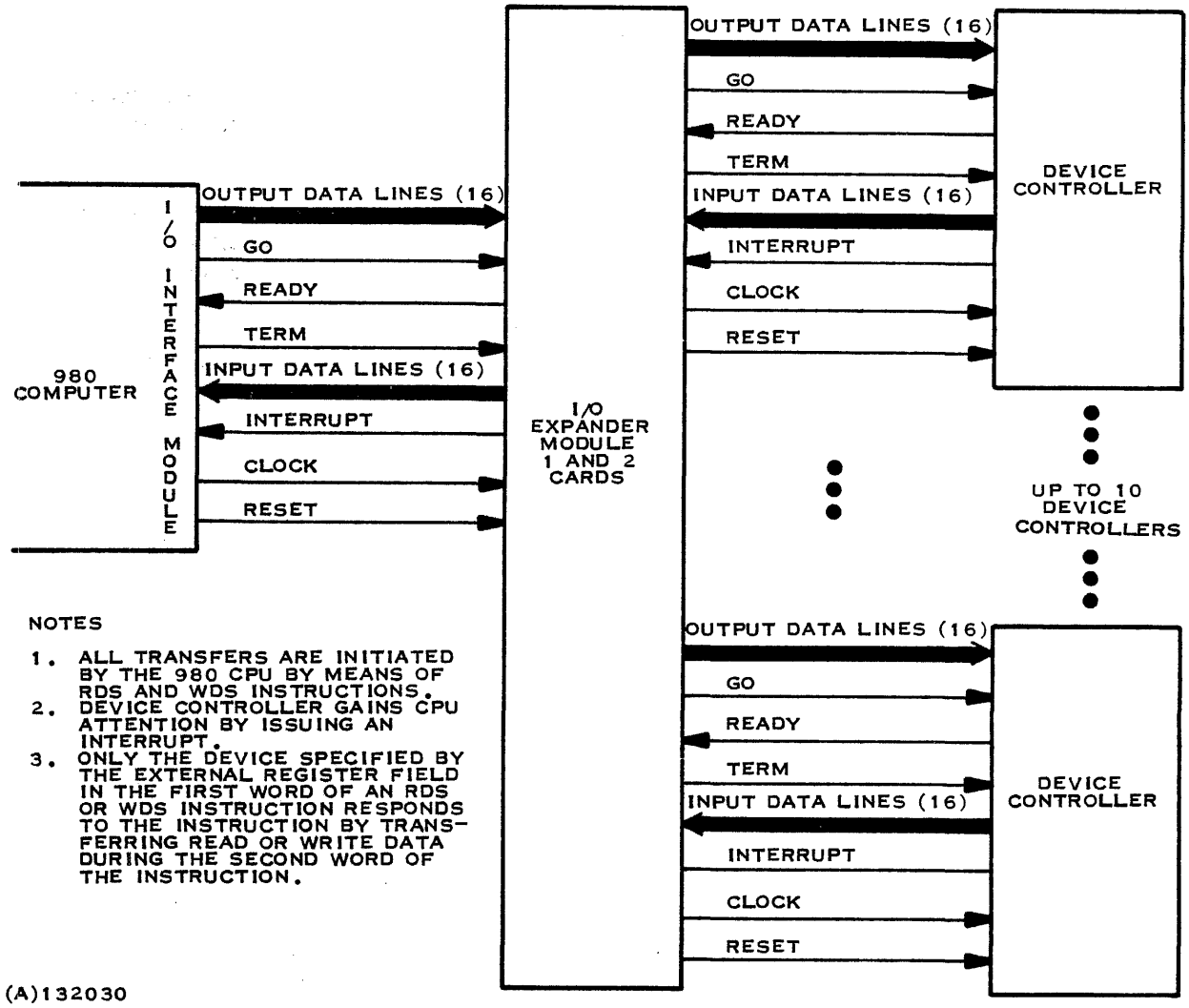


Figure 1-2. 980 I/O System, Simplified Interface Diagram

If an RDS instruction is recognized, the device controller loads the data or status word on the input (read) data lines (as directed by the command portion of the GO word). The device controller then sends a READY pulse to the CPU. The CPU acknowledges the read data transfer by sending a TERM pulse back to the originating controller.

If a WDS instruction is recognized, the device acknowledges the GO word by sending back a READY pulse. The CPU then loads a data or command word on the output data lines and sends a TERM pulse to the device controller.

Table 1-1. 980 I/O Bus System Interface Signals

Interface Signal	Function
Output Data Bus	Data signals, written from the computer into the data buffer of an output device controller.
Input Data Bus	Data signals, read into the computer from the data buffer of an input device controller.
Ready	Signal indicating that a device is ready for a data transfer to or from the computer.
Go	Signal indicating that an instruction is present on the output data lines.
Term	Signal indicating termination of the transfer of a single word of data.
Clock	Signal used to control the timing of operations related to data transfer.
Reset	Signal that resets all controllers so that none of them have access to the computer for data transfer immediately after the reset.
Interrupt	Signal indicating that a controller has requested an interrupt and is waiting to gain the attention of the CPU or has the attention of the CPU.

1.4 PHYSICAL CHARACTERISTICS OF BASIC I/O BUS CONFIGURATION

The basic 980 I/O bus consists of five I/O ports numbered IO0 through IO4 (figure 1-3). The printed circuit cards fit into slots in the chassis so that the cards plug into the port connectors properly. Normally, the I/O interface card (TI part no. 960757-0001) is placed in slot IO0 and I/O controller cards are placed in slots IO1 through IO4. Interrupt multiplexing for ports IO1 through IO4 is accomplished on the I/O interface card located in slot IO0.

Interrupts from I/O ports IO1 through IO4 are wired to IO0 where these interrupts are ORed on the I/O interface card. From the I/O interface card, the interrupts are supplied to the CPU as a single interrupt (figure 1-4).

The I/O interface card logic can be read with an RDS instruction to determine the port number of the device controller which generated the interrupt.

The 980 computer card slots in the basic I/O bus configuration with the I/O interface card in slot IO0 is illustrated in figure 1-3.

Detailed information about the available I/O controller cards manufactured by Texas Instruments is included in the user's manuals for the associated peripheral devices.

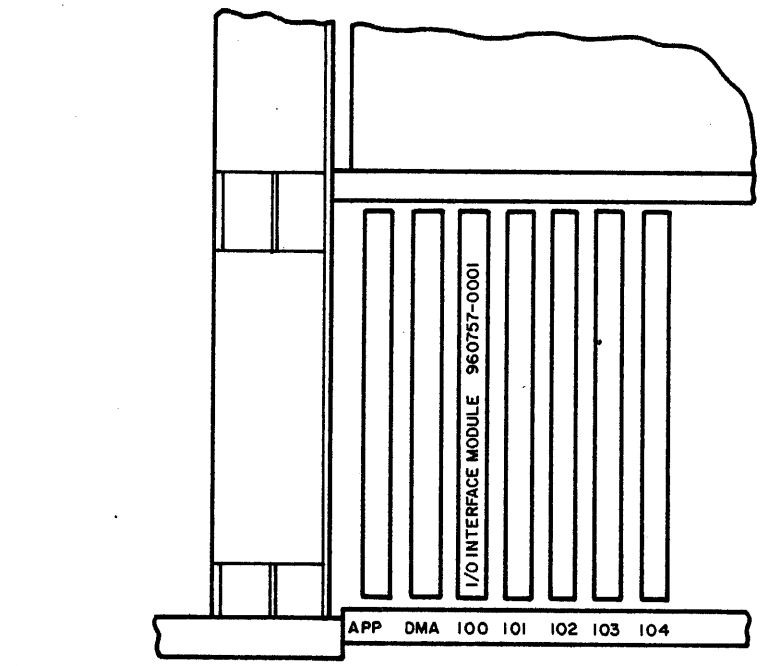


Figure 1-3. Printed Circuit Card Ports, 980 Computer Chassis

1.5 EXPANSION

Bus and group expansion are discussed in the following paragraphs.

1.5.1 BUS EXPANSION. Since there are 4 groups of 64 possible external register numbers available to address the I/O controllers, up to 256 (4 X 64) I/O devices may be connected to the Model 980 through the I/O structure. Input/output expansion is accomplished internal to the Model 980 mainframe by use of an optional internal I/O expansion kit (TI part no. 960703-0001), or externally by use of a separate I/O expander chassis kit (TI part nos. 966796-0001 through 966796-0004) that is designed for installation in a standard equipment rack. Two additional cards (I/O expander 1 and 2 cards) are utilized when the I/O bus is expanded. Figure 1-5 illustrates the I/O interface card, I/O expansion cable, and the two I/O expander cards.

These three cards provide I/O bus and control signal buffering, group decoding, and interrupt ORing of all individual ports for the expansion back panel. They also provide register address and group decoding for reading of all the interrupt lines in the expansion I/O slots using the RDS instruction to determine the slot number of the interrupting device.

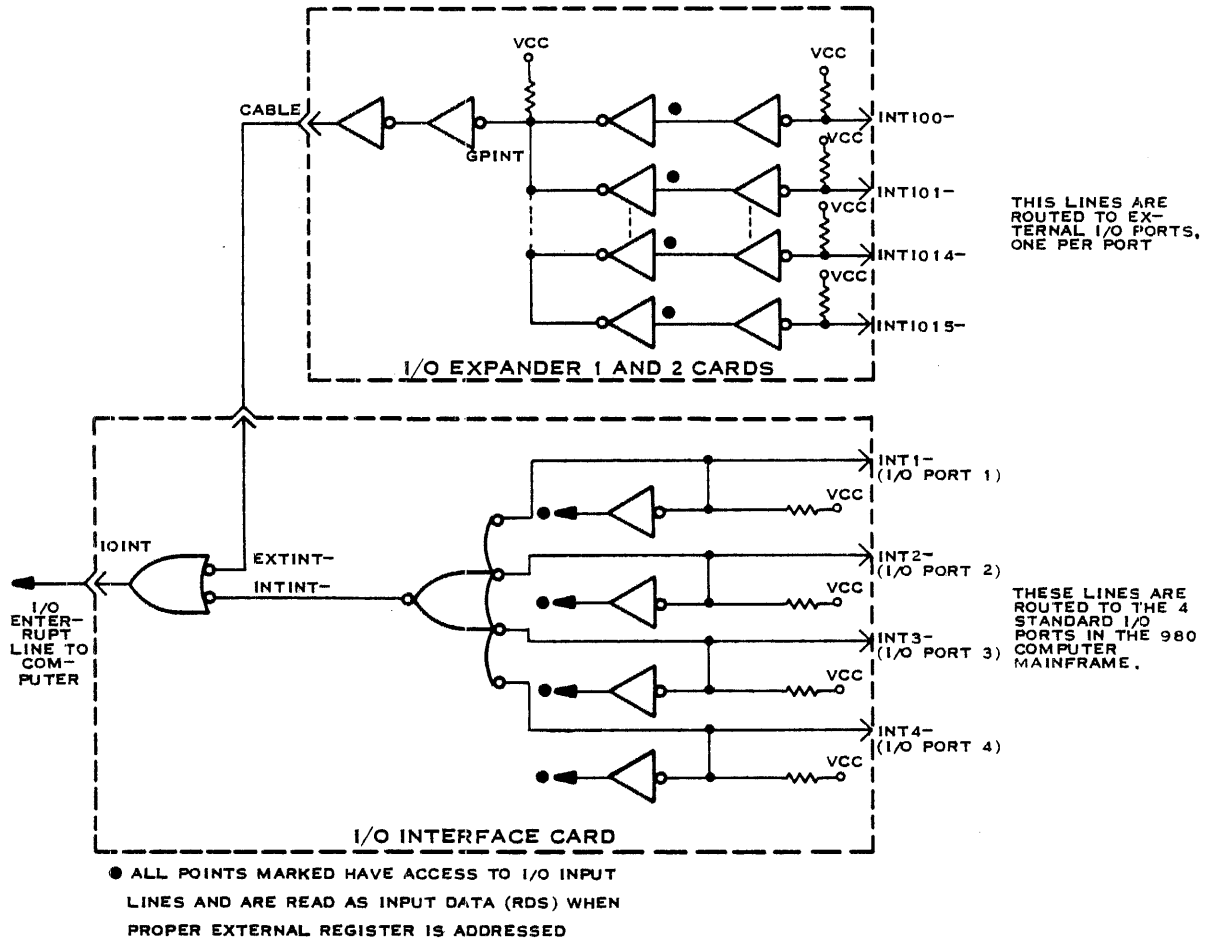


Figure 1-4. I/O Interrupts to CPU

1.5.1.1 **Internal Expansion.** When expansion is accomplished internally, I/O expander 1 and I/O expander 2 are installed in the optional expansion back panel (TI part no. 960744-0004) of the Model 980 (see figure 1-6). A cable (TI part no. 217059-0002) from the I/O interface card is connected to I/O expander 1 to complete the expansion signal interface.

Figure 1-7 shows a block diagram of the interconnect and address setting. Refer to figure 1-8 for a functional block diagram of how the I/O bus internal expansion is implemented.

The optional expansion back panel contains 12 ports which can be wired to accommodate any combination of I/O, DMAC, and API devices.

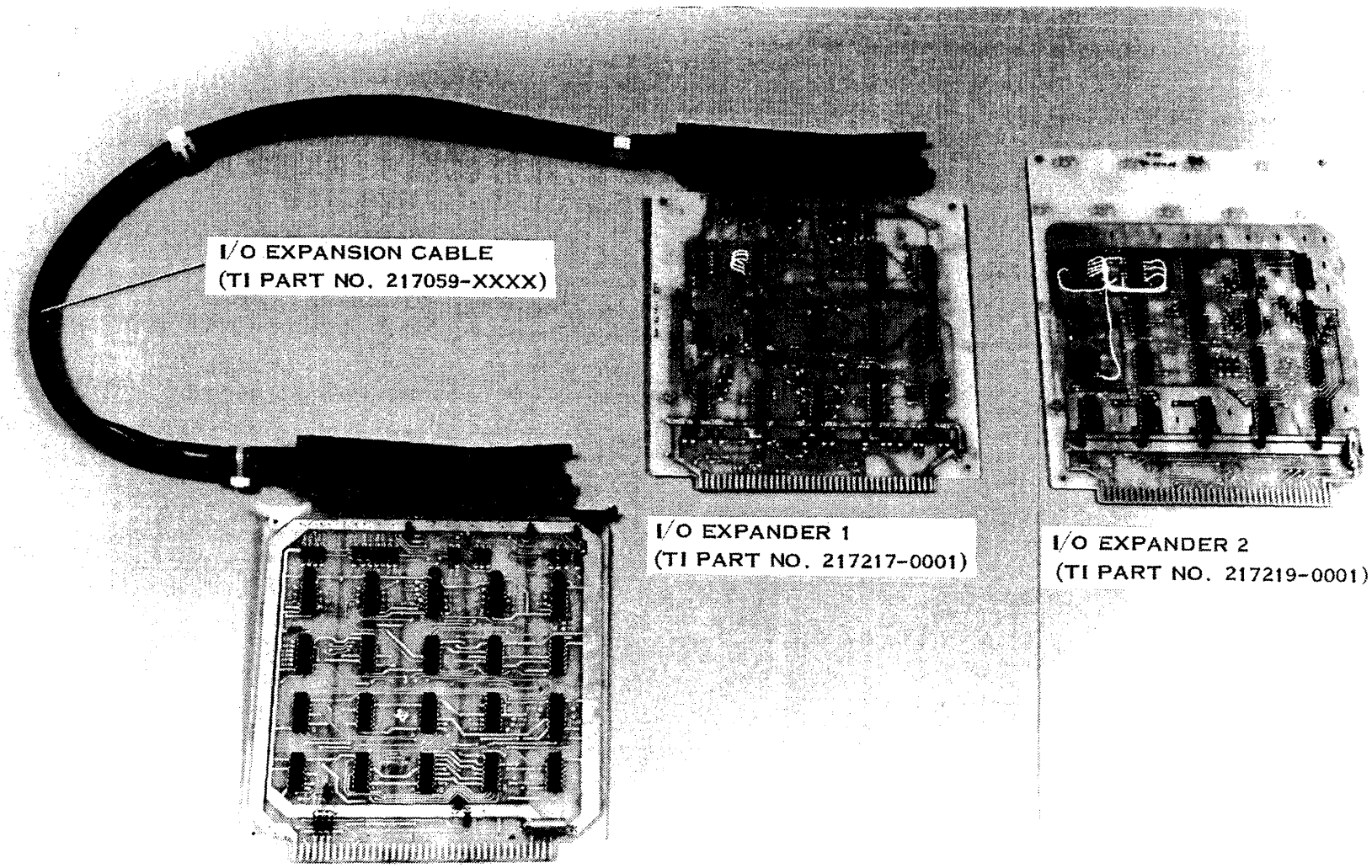


Figure 1-5. I/O Expander Cards and Expansion Cable

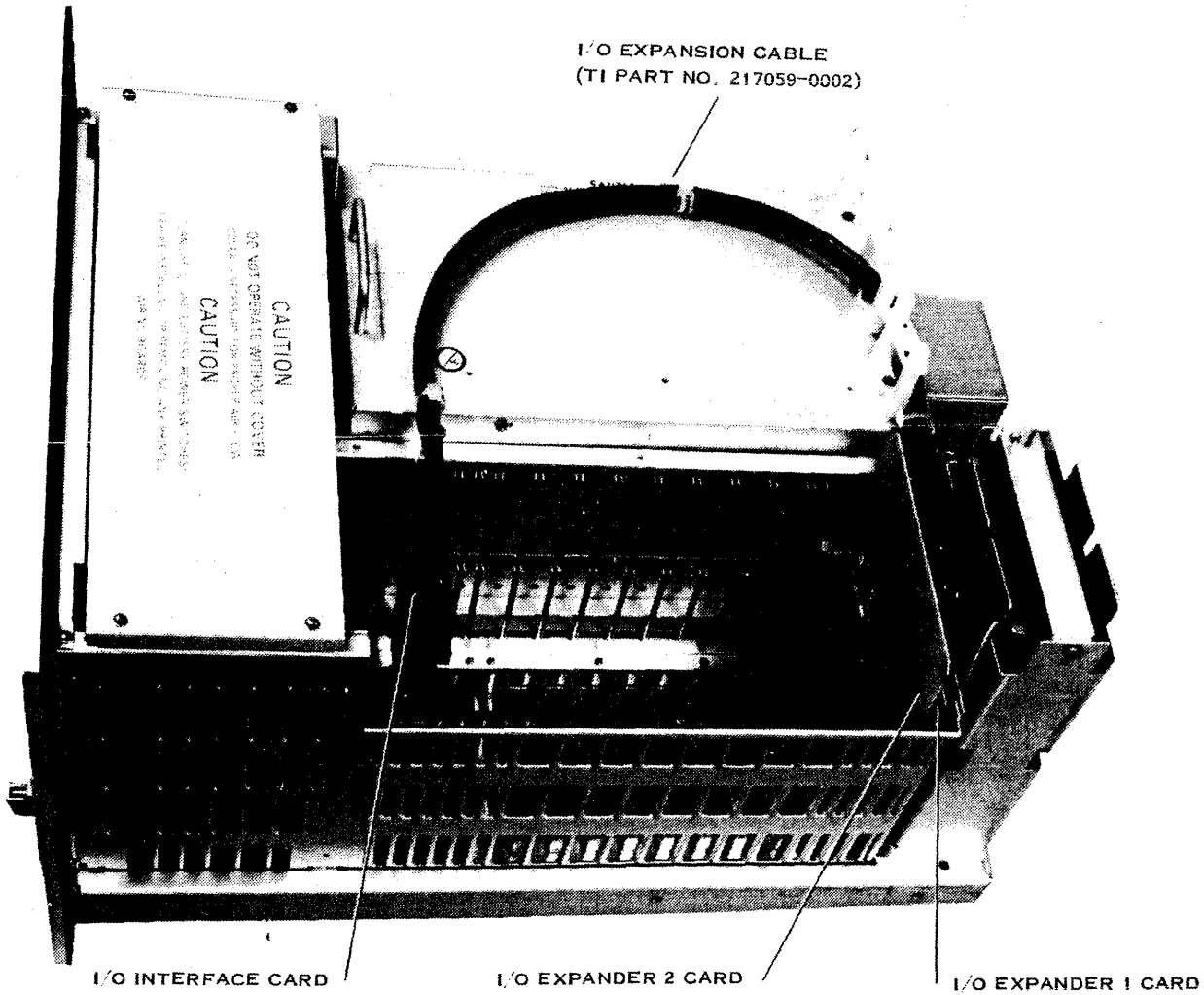


Figure 1-6. Internal I/O Expansion

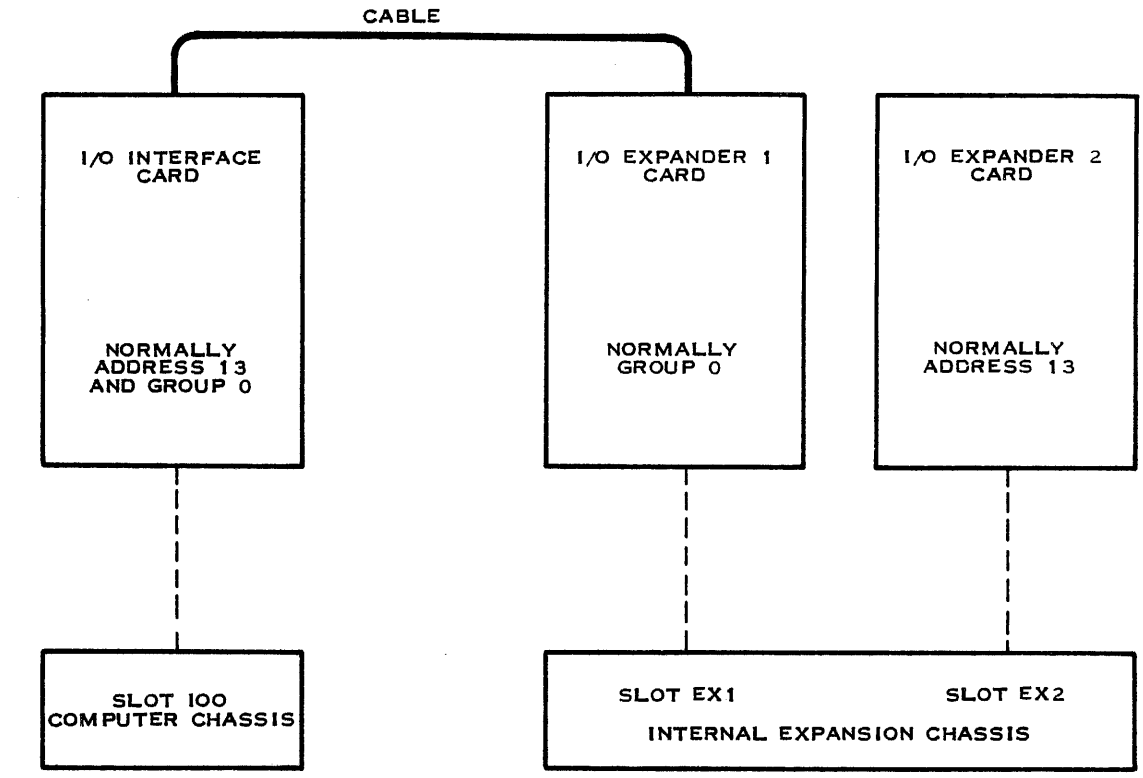


Figure 1-7. Internal I/O Expansion

The standard configuration of the optional internal I/O expansion kit (TI part no. 960703-0001) is wired to permit 9 of the 12 ports to be used for I/O devices. Two of the remaining ports (EX1 and EX2) are required for I/O expanders 1 and 2, respectively. The remaining one port (REG) is reserved for the optional ±15 volt regulator card (TI part no. 226855-0001) which is required if device controller interface cards requiring ±15 volts will be used in the internal expansion.

The addition of the nine optional I/O ports provides a total of 13 I/O ports available for external device interfaces within the Model 980 Computer mainframe.

1.5.1.2 **External Expansion.** When expansion is accomplished outside the Model 980 mainframe, I/O expander 1 and I/O expander 2 are installed in the separate I/O expander chassis. A cable (TI part no. 217059-XXXX) from the I/O interface board to I/O expander 1 completes the expansion signal interface (figure 1-9). The four X's in the part number indicate that it may be any of several different dash numbers. Refer to table 1-2 for a list of available cables.

The I/O expander chassis has 10 ports for device interface boards and two ports, EXP1 and EXP2, for the I/O expander 1 and 2 cards.

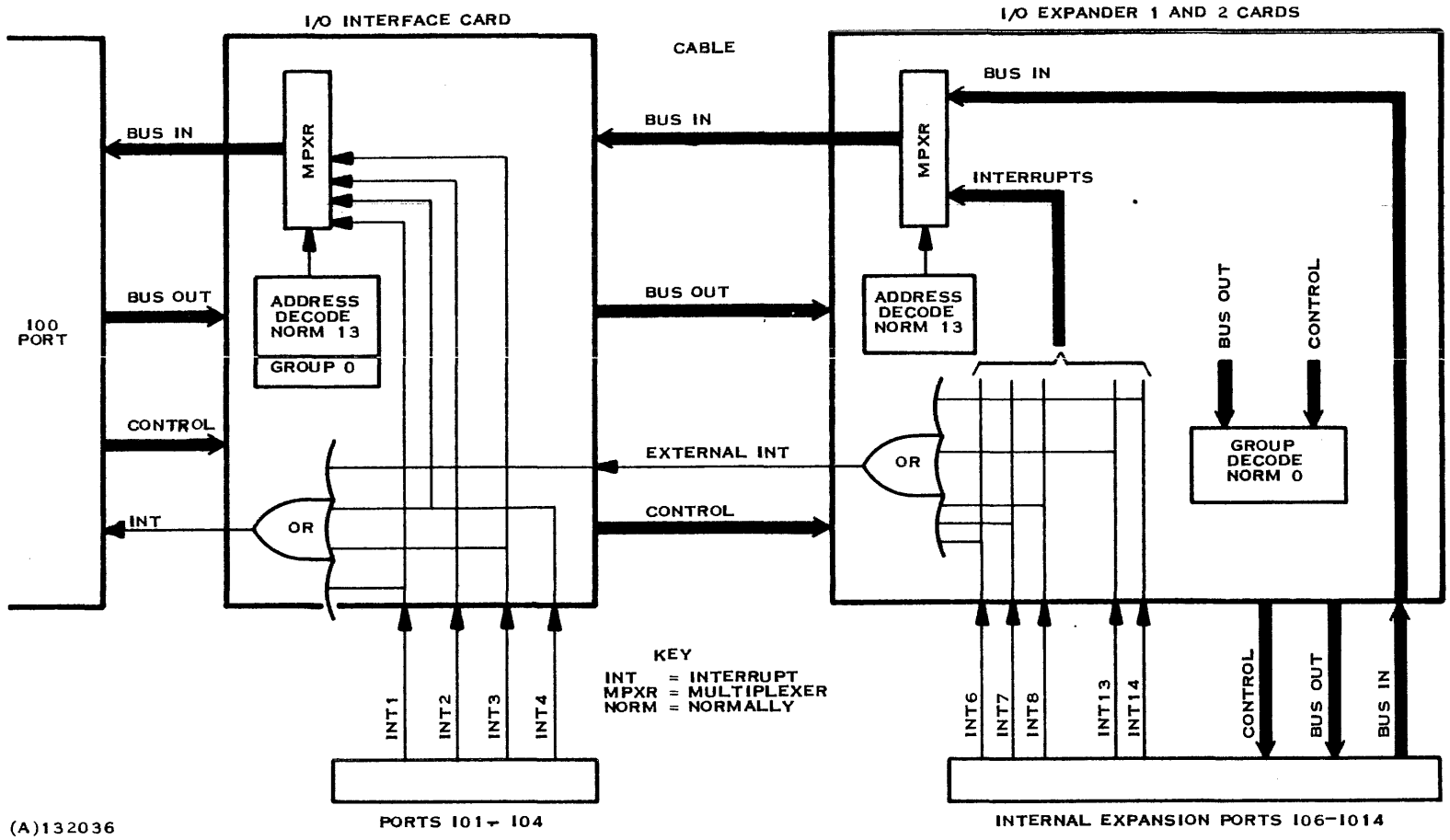


Figure 1-8. Internal Expansion, Functional Block Diagram

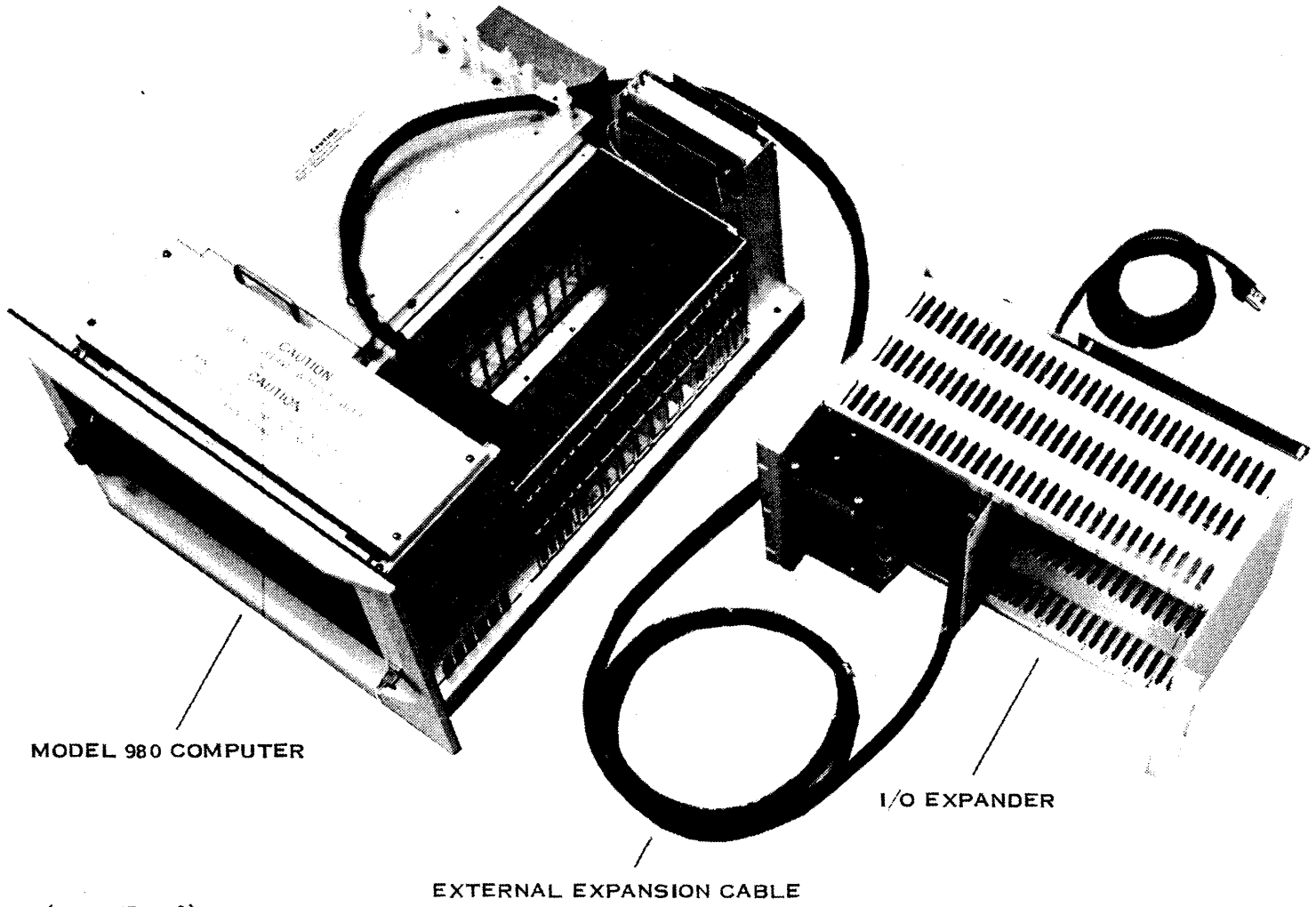


Figure 1-9. External I/O Expansion

Table 1-2. Part Numbers for Cable Assembly, CPU to I/O Bus Expander

Part No.	Length
217059-0002	2 ft
217059-0006	6 ft
217059-0012	12 ft
217059-0020	20 ft

The I/O expander chassis kit comes in four models (TI part nos. 966796-0001 through 966796-0004). The configurations are as follows:

TI Part Number	AC Power	+5 V	±15 V
966796-0001	115 V	Yes	Yes
966796-0002	115 V	Yes	No
966796-0003	230 V	Yes	Yes
966796-0004	230 V	Yes	No

Figure 1-10 shows the configuration for a single external I/O expansion with no internal expansion.

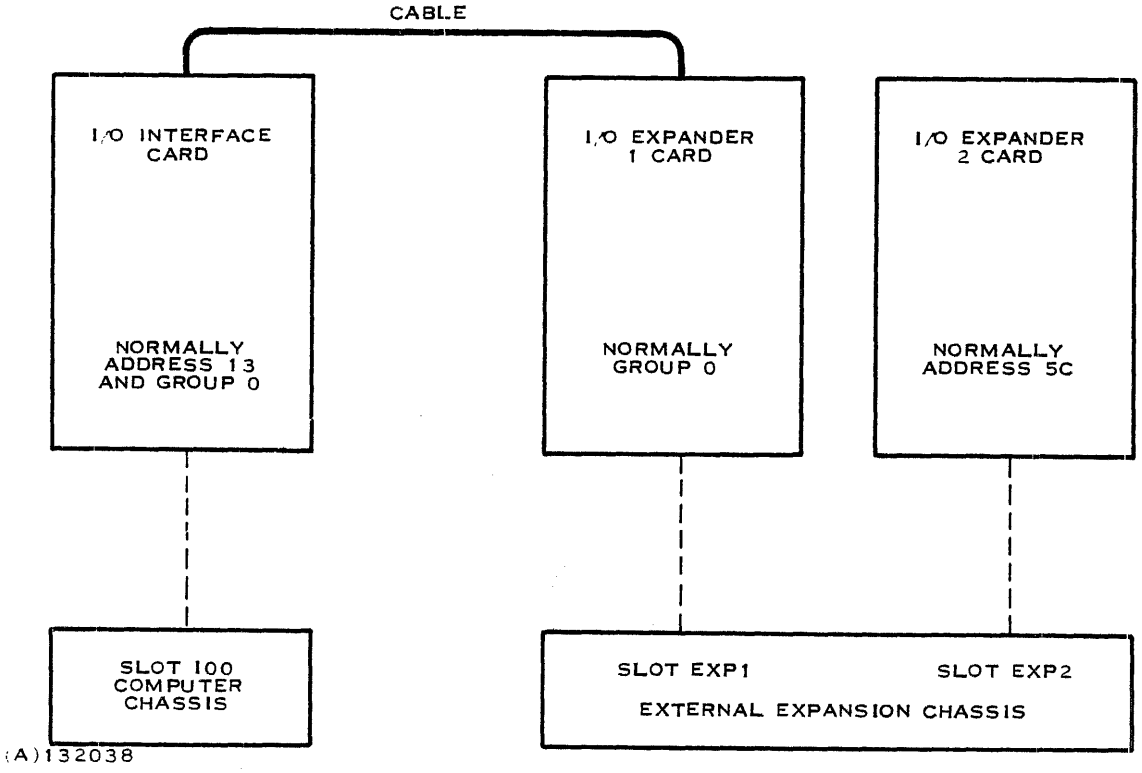
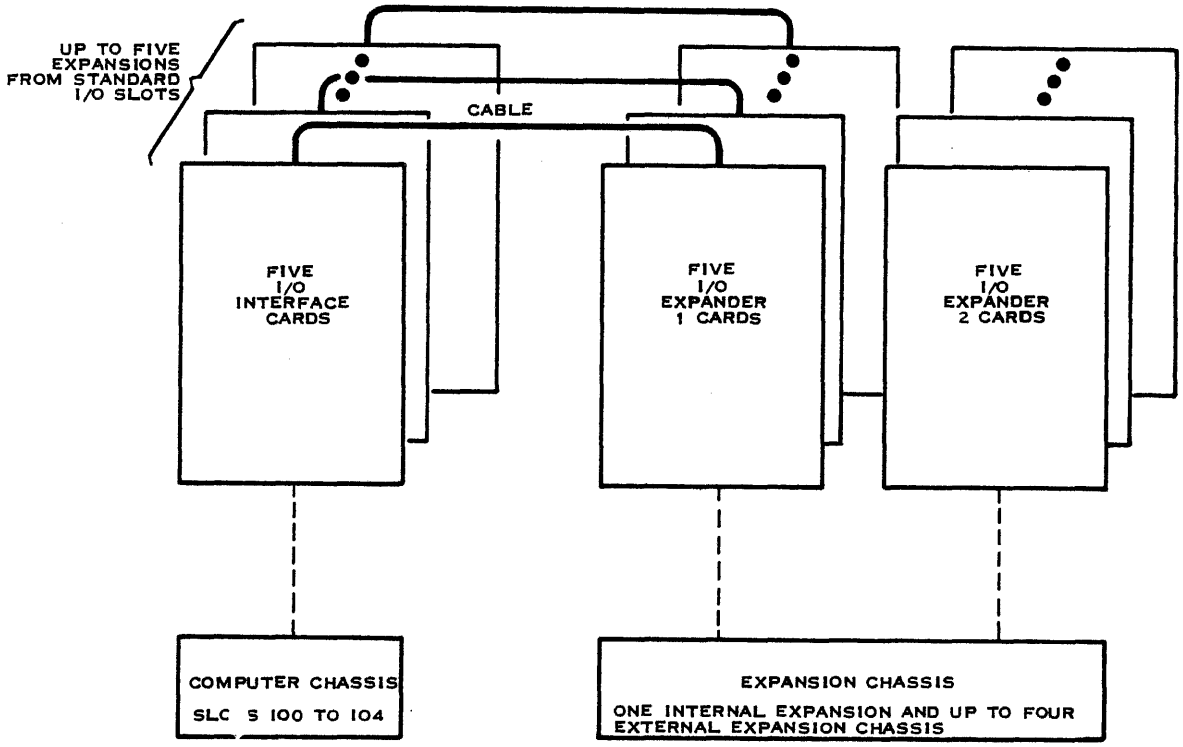


Figure 1-10. Single External I/O Expansion Configuration With No Internal Expansion

1.5.1.3 **Multiple Expansion.** For large I/O systems, more than one expansion chassis may be required. Up to four additional I/O interface cards may be installed in the basic I/O ports. Each I/O interface card is cabled to another expansion chassis. Also, the I/O interface card may be installed in any of the I/O ports in an expansion chassis to provide greater expansion capability.

Figure 1-11 shows a configuration of one internal and four external expansion units and their normal addresses and group codes. Figure 1-12 shows expansion from an external expansion chassis. Note that the group code must be the same whether or not interrupts are being used.

1.5.2 **GROUP EXPANSION.** There are four possible groups of peripheral devices identified by the contents of bits 5 and 6 of the first word of the WDS and RDS instructions. By assigning them different group numbers, four I/O controllers with the same external address number may be operated separately. Groups are assigned by hardwiring one of the four combinations of bits 5



NORMAL ADDRESS AND GROUP ASSIGNMENTS

I/O INTERFACE CARD			I/O EXPANDER 1 CARD GROUP	I/O EXPANDER 2 CARD ADDRESS	I/O EXPANSION CHASSIS
SLOT NO.	ADDRESS	GROUP			
100	13	0	0	13	INTERNAL
101	5C	0	0	5C	EXTERNAL 1
102	5D	0	0	5D	EXTERNAL 2
103	5E	0	0	5E	EXTERNAL 3
104	5F	0	0	5F	EXTERNAL 4

(A)132039

Figure 1-11. Multiple I/O Expansion

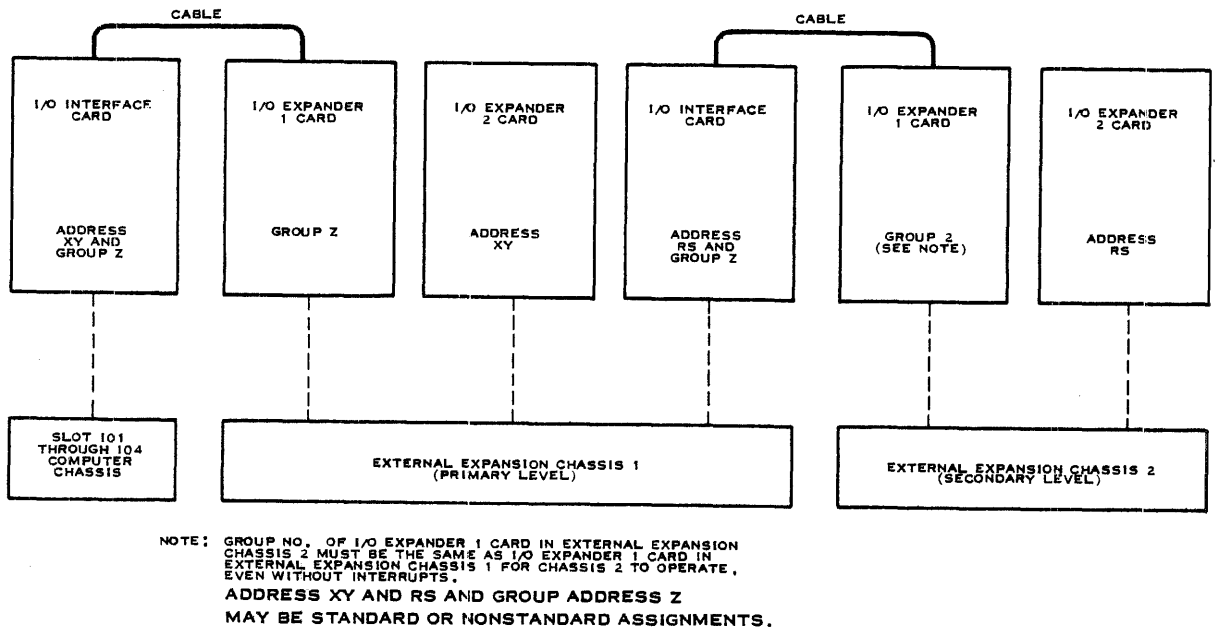


Figure 1-12. Multilevel I/O Expansion

and 6 on the I/O expander 1 card. Logic circuits decode the contents of bits 5 and 6. As a result of the decoding, GO, TERM and READY control signals are either gated to or inhibited from the other expansion ports on that back panel. The combination of 4 groups and 64 possible register addresses yields a total of 256 (4 X 64) port addresses with group expansion. Group decoding is also performed on the I/O interface card so that its register address can be reused with different groups. This is done because the I/O interface card is normally plugged into one of the five connector ports designated IO0 through IO5, in which no group decoding is performed.

On the Model 980A only, there is no group decoding done on the Privileged Instruction registers 0 and 1; therefore, these registers may not be used in any other group expansion for a read (RDS) input. On the Model 980B, group decoding is done on the Privileged Instruction registers 0 and 1. Privileged Instruction registers 0 and 1 are located on the memory controller card.

When expansion is performed from a primary expansion chassis, the secondary expansion chassis must have the same group number as the primary chassis. This is required because of the gating or inhibiting of the control signals GO, TERM and READY by the I/O expander 1 card in the primary chassis. Refer to figure 1-13 for an example of two-level external expansion.

NOTE

Most I/O expander 1 cards are delivered with group decode strapped to VCC; therefore, their control signals GO, TERM and READY are always enabled for any group.

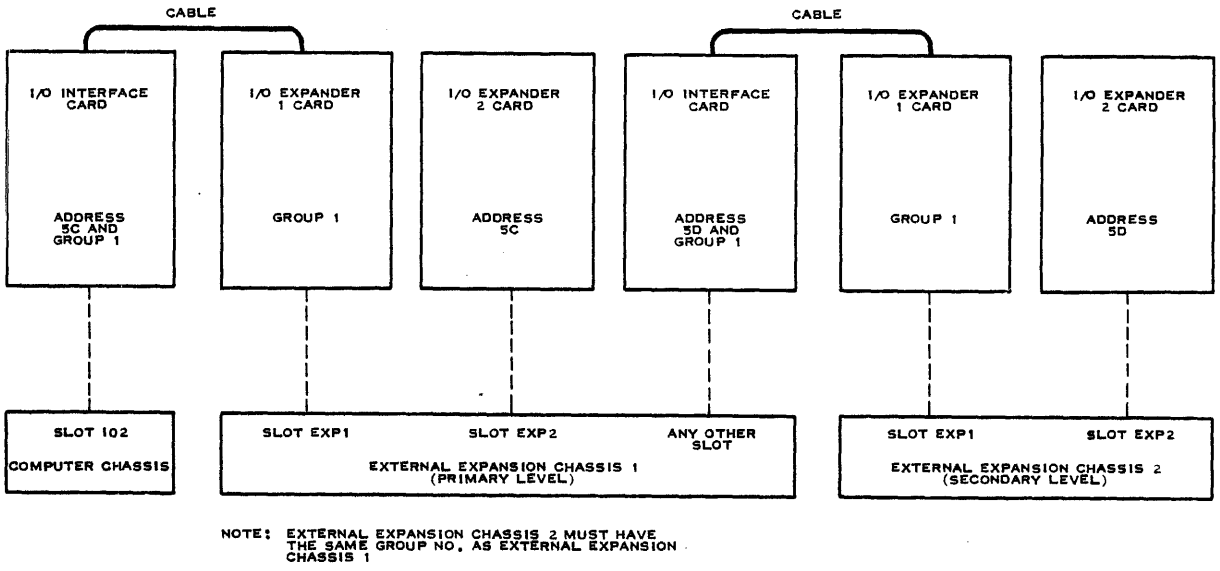


Figure 1-13. Example of Two-Level I/O Expansion

1.6 INTERRUPTS AND INTERRUPT EXPANSION

The following paragraphs discuss the functions of the interrupts for the basic I/O bus configuration and the expanded bus configurations.

1.6.1 COMPUTER CHASSIS INTERRUPTS. There is a single interrupt line for each I/O port on the 980 computer chassis. The interrupt lines for ports IO1 through IO4 are wired through the computer back panel to the IO0 port. These four interrupt lines and the external interrupt from the expansion cable are logically ORed on the I/O interface card. (See figure 1-4.)

When one or more device controllers produce an interrupt through the device interface cards and the I/O ports, the I/O interface card is slot IO0 produces an interrupt to the computer, which then traps to memory location 6 (dedicated for this purpose) if interrupts are enabled. Status register bit 7 can be set to 1 to enable I/O bus interrupts.

After the interrupt trap has occurred, the I/O data bus interrupt service routine causes the I/O interface card to be read by means of an RDS instruction specifying register 13 (the external register normally designated for reading interrupts). In this way, the programmer can find out the port number of the device that caused the interrupt.

Table 1-3 lists the interrupt bit locations for ports IO1 through IO4. Note that more than one device may cause an interrupt so that more than one bit may be set. If a device has an interrupt pending, then its interrupt bit location is set to logical 1. An interrupt bit stays set until the associated device is serviced, at which time the bit is reset to logical 0. The I/O interface card can be read repeatedly without resetting any of the interrupt location bits.

Table 1-3. Device Interrupt Bit Locations for Computer Chassis I/O Ports

Port	Interrupt Bit Location
IO0	–
IO1	Bit 1
IO2	Bit 2
IO3	Bit 3
IO4	Bit 4

1.6.2 **INTERRUPT EXPANSION.** Interrupt expansion, a function provided by the I/O expansion cards, is a means for determining the source of interrupt without reading the status of each I/O device. The I/O interface card and I/O expander 2 card, in response to RDS instructions, cause interrupt values to be gated onto the input data bus to be read into the CPU as a 16-bit data word.

There is an interrupt line for each port in the I/O expansion back panel. These lines are ORed on the I/O expander 2 card. The resultant signal is sent to the I/O expander 1 card, then over the expansion cable to the I/O interface card, which produces an I/O bus interrupt to the computer. Figure 1-4 shows the ORing and signal routing of the interrupts.

After the computer has trapped to the I/O bus interrupt, the programmer can interrogate the I/O interface card to determine the source of the interrupt. If the computer system has internal expansion, then when the programmer reads register 13 (the register containing the interrupt expander address in the normal configuration), he gets the interrupt status of ports IO1 through IO4 in bits 1 through 4. If the internal I/O expander cards are also set on group 0, register 13 (the normal selection for these cards), the interrupt status of internal expansion ports IO6 to IO14 is also gated in and read in bits 6 through 14 of the interrupt status word. In this way, the source of the interrupt may be identified. Table 1-4 gives the device interrupt bit locations for the internal expansion chassis I/O ports. If the system has external as well as internal expansion, the configuration is similar to the one shown in figure 1-14.

As an example of how the interrupting device is identified, suppose a device in external expansion chassis slot IO9 interrupted. After reading register 13 (hexadecimal) to determine the source of the interrupt, the programmer would find out that bit 1 was set. This tells him that the device in slot IO1 interrupted, but because there is an I/O interface card in that slot, he reads register 5C (hexadecimal), group 0 on the external expander cards with an RDS instruction. He would see that bit 9 is set, indicating that the controller card in slot 9 is the source of the interrupt. Table 1-5 shows the device interrupt bit locations for external expansion ports.

Note that the I/O interface card in slot IO1 is also set to register 5C, group 0, the same register and group as its expander cards. Even though no information can be read from it because of its slot location, it does not use up another address.

Table 1-4. Device Interrupt Bit Locations for Internal Expansion Chassis I/O Ports

Port	Interrupt Bit Location
REG	None
IO6	Bit 6
IO7	Bit 7
IO8	Bit 8
IO9	Bit 9
IO10	Bit 10
IO11	Bit 11
IO12	Bit 12
IO13	Bit 13
IO14	Bit 14
EX2	–
EX1	–

NOTE

The "Skip on Ready" option is not to be used with the RDS instruction which reads the interrupt expander.

1.7 EXTERNAL REGISTER ASSIGNMENTS

Each I/O controller has one or more external register numbers assigned which may be selected using switches or jumpers, A list of standard external register number assignments for controllers operated through the I/O structure is provided in figure 1-15 and table 1-6. Users may change the external register assignments for special applications.

NOTE

The standard group number assignment for all I/O controllers is 0. Group numbers and register numbers can be changed on the individual cards, by jumper wires on some and by pencil switches on others.

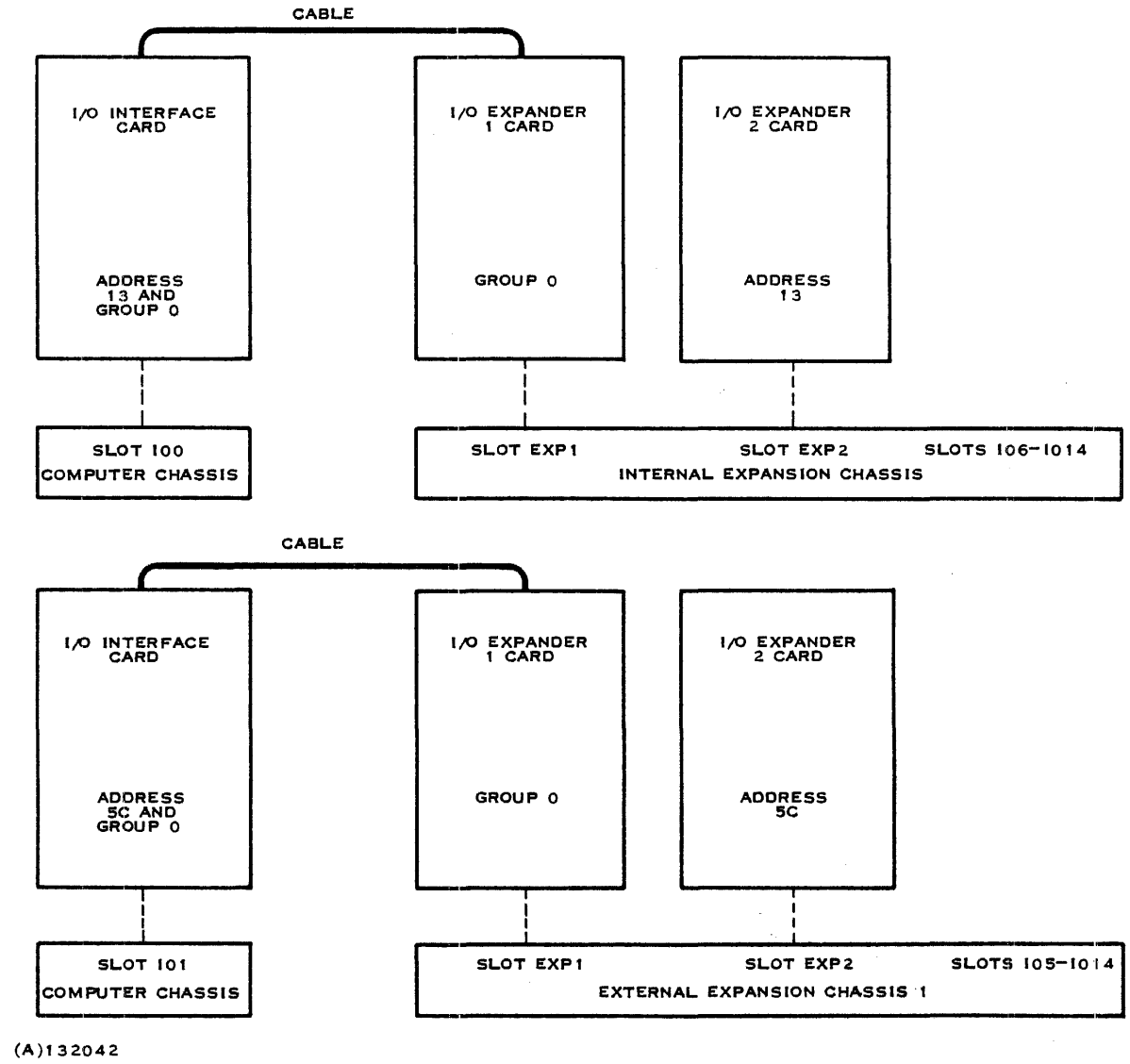


Figure 1-14. Internal and External I/O Expansion

1.8 EQUIPMENT SPECIFICATIONS

The characters of the 980 computer input/output bus are listed in table 1-7.

Pullups on the I/O interface card keep the False interrupt signals high when controllers are not in the basic I/O ports. Pullups for all other open collector outputs are located in the CPU.

Standard pin numbers for 980 computer 80-pin back panel connectors are illustrated in figure 1-16.

All signals at the I/O bus interface are compatible with Texas Instruments Series 54/74 transistor-transistor logic (TTL) circuits. The logic 0 (low) level is 0.0 to +0.4 volts dc. The logic 1 (high) level is +2.4 to +5.0 volts dc.

Table 1-5. Device Interrupt Bit Locations for External Expansion Chassis I/O Port

Port	Interrupt Bit Location
IO5	Bit 5
IO6	Bit 6
IO7	Bit 7
IO8	Bit 8
IO9	Bit 9
IO10	Bit 10
IO11	Bit 11
IO12	Bit 12
IO13	Bit 13
IO14	Bit 14
EX2	–
EX1	–

BITS 12,13,14,15 (HEX)

BITS 9, 10, 11, (SEE NOTE 4)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CUSTOMER USE		TTY 1 (SEE NOTES 1 AND 5)	TTY 2 (SEE NOTE 1)	INTERVAL TIMER	COMMUNI-CATION MODULE 1 (SEE NOTES 2 AND 5)	COMMUNI-CATION MODULE 2 (SEE NOTE 2)	CUSTOMER USE			TTY 1 (SEE NOTE 1)	TTY 2 (SEE NOTE 1)	CUSTOMER USE	COMMUNI-CATION MODULE 3 (SEE NOTE 2)	COMMUNI-CATION MODULE 4 (SEE NOTE 2)	
1	PRIV. INST. FEATURE (SEE NOTE 3)	PRIV. INST. FEATURE (SEE NOTE 3)	TTY 1 (SEE NOTES 1 AND 5)	TTY 2 (SEE NOTE 1)	INTERVAL TIMER	COMMUNI-CATION MODULE 1 (SEE NOTE 2)	COMMUNI-CATION MODULE 2 (SEE NOTE 2)				TTY 1 (SEE NOTE 1)	TTY 2 (SEE NOTE 1)		COMMUNI-CATION MODULE 3 (SEE NOTE 2)	COMMUNI-CATION MODULE 4 (SEE NOTE 2)	
2	TAPE READER	TAPE PUNCH		INTERNAL INTERRUPT EXPANDER	CUSTOMER USE				TAPE READER							CARD READER
3	TAPE READER	TAPE PUNCH							TAPE PUNCH		TTY 1 (SEE NOTE 1)	TTY 2 (SEE NOTE 1)				CARD READER
4	CARD PUNCH	CUSTOMER USE			A TO D D TO A	A TO D D TO A	A TO D D TO A						A TO D D TO A	A TO D D TO A	A TO D D TO A	
	CARD PUNCH				A TO D D TO A	A TO D D TO A	A TO D D TO A						A TO D D TO A	A TO D D TO A	A TO D D TO A	
5	LOW SPEED LINE PRINTER (SEE NOTE 5)												EXTERNAL INTERRUPT EXPANDER 1	EXTERNAL INTERRUPT EXPANDER 2	EXTERNAL INTERRUPT EXPANDER 3	EXTERNAL INTERRUPT EXPANDER 4
	LOW SPEED LINE PRINTER (SEE NOTE 5)				VECTORED INTERRUPT	VECTORED INTERRUPT	VECTORED INTERRUPT	VECTORED INTERRUPT	VECTORED INTERRUPT	VECTORED INTERRUPT	CUSTOMER USE					

RDS - BIT 10 0

WDS - BIT 10 1

NOTES

1. TTY 1 33 ASR, SILENT 700 OR TTY 2 CRT (HAZELTINE) } OLDER INTERFACES
2. THE COMMUNICATIONS MODULE INTERFACES WITH THE 733 ASR/KSR, 33 ASR, OR 912 VIDEO DISPLAY TERMINAL.
3. 980A COMPUTER DOES NO GROUP DECODE ON PIF REGISTERS.
4. BIT 10 IN THIS COLUMN ALWAYS REFERENCED TO ZERO.
5. INDICATES PRIMARY DEVICE ADDRESS.

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Figure 1-15. External Register Number Assignments

Table 1-6. Standard 980 External Register/Function Details

Register Number (Bits 9-15)	Device	Function
00	PIF - Privileged Instruction Feature*	Out - Set lower memory boundary
01	PIF - Privileged Instruction Feature*	Out - Set upper memory boundary
02	TTY1 - ASR33, Silent 700 or CRT (primary) old interface part no. 217394	In - Read data Out - Write data
03	TTY2 - (Secondary) old interface part no. 217394	In - Read data Out - Read data
04	Interval Timer	
05	Communication Module (primary addr.) 33 ASR, 733 ASR/KSR or CRT New Interface part no. 966637	In - Input data and status Out - Output data and commands
06	Communication Module (secondary addr.)	In - Input data and status Out - Output data and commands
07	Customer use	
08	Customer use	
0A	TTY1 - ASR-33, Silent 700 or CRT (primary) old interface part no. 217394	In - Read status Out - Write command
0B	TTY2 - Secondary (old interface part no. 217394)	In - Read status Out - Write command
0C	Customer use	
0D	Communication Module (secondary addr.)	In - Input data and status Out - Output data and commands
0E	Communication Module (secondary addr.)	In - Input data and status Out - Output data and commands
10	PTR - Paper Tape Reader	In - Read status Out - Write command
11	PTP - Paper Tape Punch	In - Read status Out - Write command
13	INT - Interrupt expander address for internal expander; interrupt expander is relative to board location	In - Read interrupt
14	Customer use	
15	Customer use	
16	Customer use	
18	PTR - Paper Tape Reader	In - Read data
	PTP - Paper Tape Punch	Out - Write data

*The Model 980A Computer does no group decode on PIF register.

Table 1-6. Standard 980 External Register/Function Details (Continued)

Register Number (Bits 9-15)	Device	Function
1A	TTY1 - ASR33, 700 or CRT (primary old interface part no. 217394	Disconnect function
1B	TTY2 - (secondary) old interface part no. 217394	Disconnect function
1F	CDR - Card Reader	In - Read status and data Out - Write command
40	CDP - Card Punch	In - Read status Out - Write data and command
41	Customer use	
42	Customer use	
44-46	ADA - Analog to Digital Converter or Digital to Analog Converter	Data Module (See ADA User's Manual)
4C-4E		
50	LLP - Low Speed Line Printer	Data Module (See Line Printer User's Manual)
54	Vectored interrupt (I/O 1 and 2)	Set mask
55	Vectored interrupt (I/O 1 and 2)	Clear mask
56	Vectored interrupt (I/O 1 and 2)	Set interrupt (T)
57	Vectored interrupt (I/O 3 and 4)	Set mask
58	Vectored interrupt (I/O 3 and 4)	Clear mask
59	Vectored interrupt (I/O 3 and 4)	Set interrupt (T)
5C	Interrupt expander address for external expansion chassis 1	In - Read interrupts
5D	Interrupt expander address fsor external expansion chassis 2	In - Read interrupts
5E	Interrupt expander address for external expansion chassis 3	In - Read interrupts
5F	Interrupt expander address for external expansion chassis 4	In - Read interrupts

(T) - Test only

Table 1-7. Model 980 I/O Characteristics

Characteristic	Specification
I/O Instructions (2)	Read (1) and Write (1)
Word Length	16 Bits
Data Transfer	Parallel
Data Lines (32)	16 in and out
Control Lines	10 lines
Transfer Rate	130,000 words per second, maximum
I/O Bus Interrupt	1 interrupt
I/O Bus Interrupt Expansion	1 interrupt bit per I/O controller
I/O Ports:	
Basic CPU	4 maximum
CPU with Internal Expansion	13 maximum
CPU with External Expansion	256 maximum

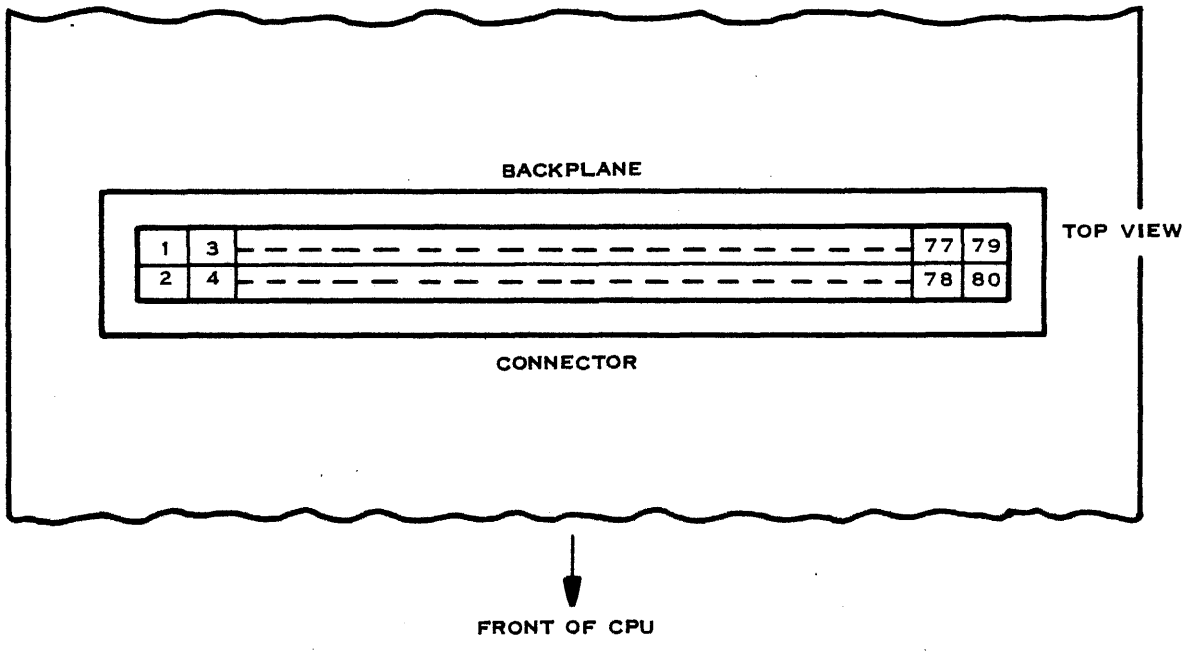


Figure 1-16. Input/Output Port Connector Pin Number

SECTION II

INSTALLATION

2.1 GENERAL

The I/O bus system is based on three hardware configurations, referred to as standard, internal expansion or external expansion. A particular site may have any one or all of these configurations.

2.2 STANDARD I/O PORTS

Installation of the standard configuration requires no hardware in addition to the I/O interface card (TI part no. 960757-0001) provided with the basic CPU. This interface card is placed in port IO0 and provides the signal interface for the standard I/O ports plus the first-level expansion (internal or external). This module is inserted with the component side facing the front of the computer. The module must be jumpered to select the group and module address. The module address is necessary to permit a read operation of the interrupt lines which are multiplexed at the I/O interface card. Refer to figure 2-1 and table 4-1 to establish the necessary jumper connections. Solder jumpers with 22 to 26 gauge, single conductor, insulated wire.

2.3 INTERNAL EXPANSION PORTS

An internal I/O expansion requires an optional, factory-wired connector panel installed behind the standard I/O back panel. This paragraph covers installation of the cables and buffer cards within a CPU with this internal expansion hardware already in place. When installing or removing

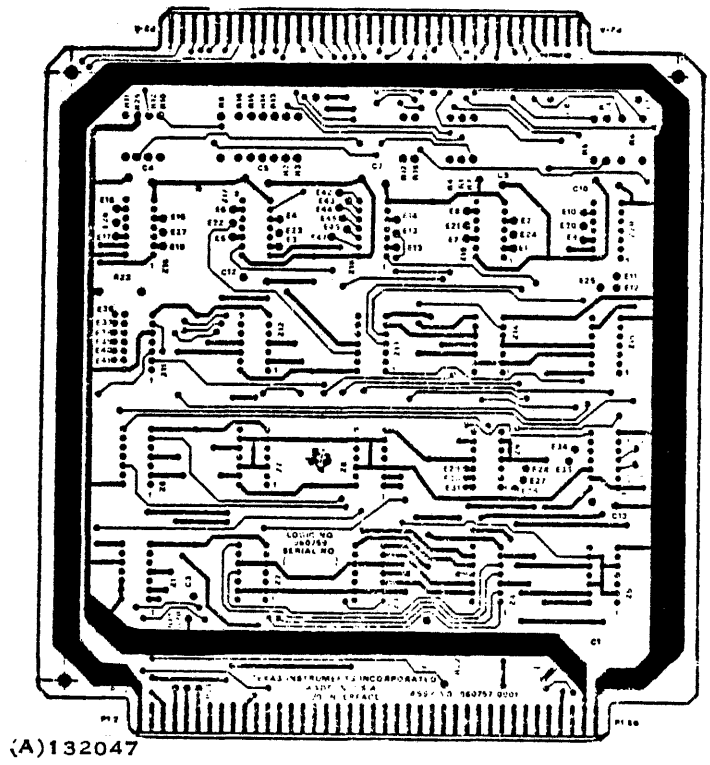


Figure 2-1. I/O Interface Card

a connector panel, refer to the I/O Expansion Kit drawing (TI part no. 960703-0001) provided with the hardware. This drawing is also included in the *Model 980 Computer Maintenance Manual: Input/Output and Input/Output Expansion,* Manual No. 960699-9704.

To configure an internal expansion, set up the address jumpers for the I/O interface card and install the module as specified in the section covering standard ports. Install the set of expander cards (I/O expander 1 card and I/O expander 2 card) as shown in figure 1-6. Connect the I/O expansion cable, TI part no. 217059-0002 as illustrated.

Expander 1 card jumpers determine the group of the internal expansion. Install jumpers of 22 to 26 gauge, insulated, single conductor wire and solder into place. The location of jumpers is determined from table 4-2 (the jumper schedule for the I/O expander 1 card) and figure 2-2. The group address selected generally is identical to the group address of the I/O interface card associated with this expansion. The I/O expander 1 card is installed in the last port of the internal expansion chassis labeled EX1. The Expander 2 card inserts into the adjacent slot marked EX2.

The I/O expander 2 card specifies the register address used to interrogate the interrupt lines and access the expanded slots. Install jumpers as described above. Refer to the illustration of the I/O expander 2 card (figure 2-3) and table 4-3 to determine the jumper locations. Again, this address is usually the same as the address specified on the associated I/O interface card.

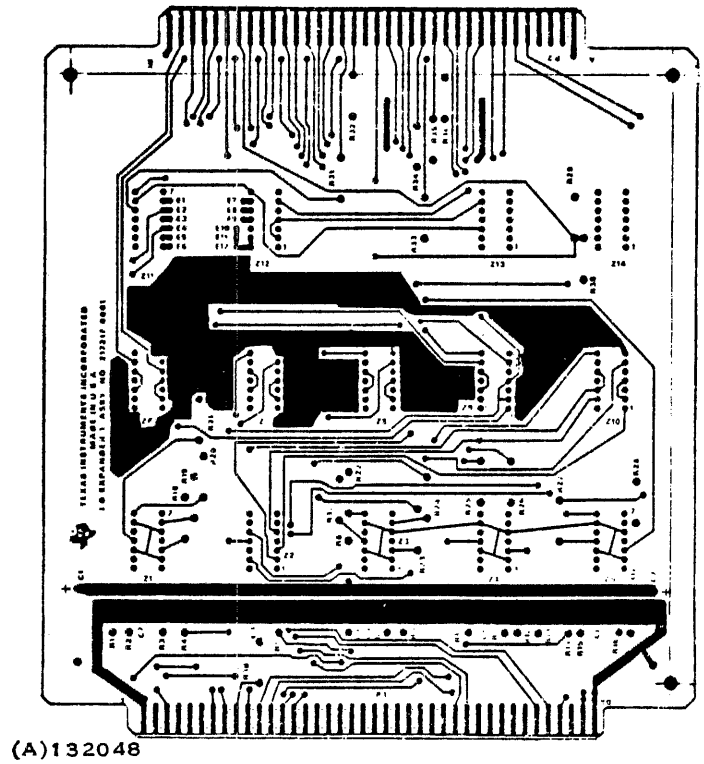
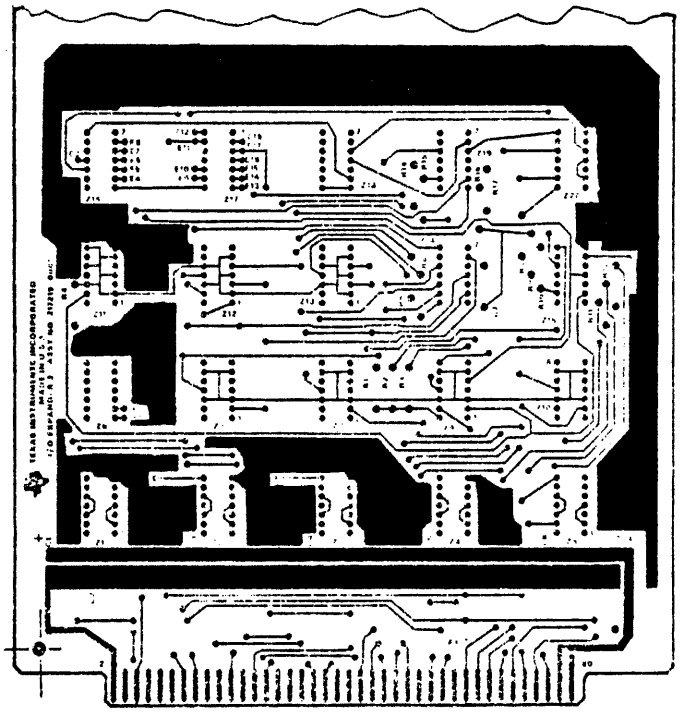


Figure 2-2. I/O Expander 1 Card



(A)132049

Figure 2-3. I/O Expander 2 Card

2.4 EXTERNAL EXPANSION PORTS

An external expansion includes a chassis, an I/O bus expansion cable, two I/O expander cards, and a wired connector panel for 10 I/O bus ports. The chassis assembly includes a power supply. This procedure details the interconnections required to install an external expansion.

- External Chassis – The external chassis is installed on the rear rails of the cabinet. Note that the air will not circulate properly over the equipment when installed on the front rails and will cause equipment damage. Place the external chassis so that the cards can be removed from the back of the cabinet and with the power supply located on the left side (as one faces the assembly).

- Cable assemblies are of various lengths as specified in table 1-2. Select a location for the chassis which can be reached by the cable provided.

- I/O expander 1 and 2 cards should be jumpered as described in the internal expansion ports description (paragraph 4.4). Install the cards as shown in figure 1-9 (I/O expander 1 card in slot EX1 and I/O expander 2 card in slot EX2, both with the component side facing away from the power supply). Note that generally the group and register addresses on the I/O expander 1 and 2 cards are the same as the associated I/O interface card. The associated I/O interface card is located in slot IO0 unless multiple expansion is employed. For multiple expansions, the I/O interface card may be located in a standard, external or internal port.

SECTION III

OPERATING INSTRUCTIONS

3.1 GENERAL

This section presents both hardware and software operating instructions for the 980 I/O bus and expansion system. The information is presented in two parts: information about the I/O expander chassis, and software instructions needed to operate and control the basic I/O bus and the expanded I/O bus.

3.2 EXTERNAL I/O EXPANDER CHASSIS

The external I/O expander chassis contains no controls or indicators. However, it has a power cord for connection to either 115 volts or 230 volts line power, as required chassis ac input power is fused.

3.3 SOFTWARE INSTRUCTIONS

Operation of the Model 980 Computer input/output bus structure is controlled by two software instructions, the Read Direct Single (RDS) and Write Direct Single (WDS) instructions. They are described briefly in the following paragraphs. For more detailed information about these instructions, refer to the following software program development manuals:

- *Model 980 Computer Assembly Language Programmer's Reference Manual,* Manual No. 943013-9701.
- *Model 980 Computer Assembly Language Input/Output,* Manual No. 961961-9734.

3.3.1 READ DIRECT SINGLE INSTRUCTION. The RDS instruction consists of two 16-bit words (WD1 and WD2) as illustrated in figure 3-1. The first word of the RDS instruction (WD1) is applied to the output bus and an output strobe (GO) is generated which indicates to the external device that its data must enter the input bus. This data is retained on the input bus until a release pulse (TERM) is generated by the Model 980.

The destination of the input data is controlled by the second word of the instruction (WD2). The format of the read direct instruction is illustrated in figure 3-1 and the control functions are described in separate subparagraphs which follow. The instruction fields are summarized in table 3-1.

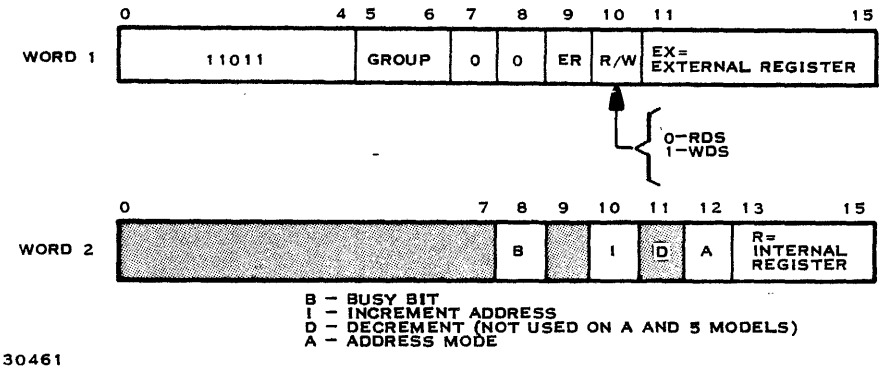


Figure 3-1. RDS/WDS Instruction Format

Table 3-1. WDS/RDS Instruction Field Breakdown

Word/Bit(s)	Explanation
1/0-4, 7, 8	Op-code bits.
1/5, 6	Group bits, used to define 1 of 4 groups. Each group can be used to specify up to 64 external devices. The group and external register fields combine to specify the external device involved in the WDS/RDS instruction. Typically, the group bits are zero unless the expansion of data bus ports exceeds 64.
1/9, 11-15	External register bits, used to specify 1 of 64 devices in the selected group.
1/10	Read/write bit, used to specify either a RDS or WDS instruction. A logic zero specifies a RDS instruction; a logic one specifies a WDS instruction.
2/0-7, 9, 11	Not used.
2/8	Busy bit, an optional field (B) used with external devices that may not be ready to transfer data when queried by the computer. If this bit is a logic one and successful data transfer takes place, the instruction following the WDS/RDS instruction is skipped. If this bit is a logic one and no data transfer takes place, the instruction following the WDS/RDS instruction is executed. If this bit is a logic zero, the device transfers data unconditionally and the instruction following the WDS/RDS instruction is executed.
2/10	Increment (I) field, used in conjunction with the A field (bit 12 of word 2) to increment or decrement the contents of the register specified by the R field (bits 13 of 15 of word 2). If both the I and A fields are logic ones, the address contained in the register specified by the R field is incremented by one each time a data word is transferred. If the A field is a logic one, but the I field is a logic zero, the address contained in the register specified by the R is decremented by one each time a data word is transferred.
2/11	Decrement (D) field, included for compatibility with earlier models of the computer. It performs no function in the 980.
2/12	Address (A) mode field, used to specify indirect addressing. If the A field is a logic zero, data is transferred to or from the register specified by the R field. If the A field is a logic one, data is transferred to or from the memory location specified by the contents of register R.
2/13-15	Register (R) field, used to specify 1 of 8 internal registers in the computer. The specified register holds the data or the address of data involved in the transfer.

SECTION IV

PRINCIPLES OF OPERATION

4.1 INTRODUCTION

This section describes the principles of operation of the Model 980 Computer input/output bus system and its associated electronic circuits. It includes a theoretical description of the I/O instructions, the I/O interface card and the I/O expander cards. A functional diagram of the I/O bus is illustrated in figure 4-1.

Refer to the *Model 980 Computer Maintenance Manual: Input/Output and Input/Output Expansion,* Manual No. 960699-9704, for detailed logic diagrams, assembly drawings, parts lists, and load, pin and wire lists related to the I/O bus and I/O expansion.

4.2 ARITHMETIC UNIT CONTROL

The Arithmetic Unit (AU) in the Model 980 Computer contains control and data path logic for the I/O bus. When an RDS or WDS instruction is acquired, the AU ROM controller gates the first word of the instruction on the I/O output data lines for 750 nanoseconds or three clock periods (250 nanoseconds). During the second clock period a GO signal is applied to the I/O bus which signifies that the I/O controllers should decode the external register lines to determine which controller or function is being addressed by the I/O instruction. The RDS and WDS timing is illustrated in figures 4-2 and 4-3, respectively.

The top two waveforms in figures 4-2 and 4-3 include the RDS/WDS word 1 and GO signal timing. If the "SKIP ON READY" option is used (RDS/WDS word 2, bit 8 equal to 1), the I/O controller should supply a READY signal to the AU within 750 nanoseconds as shown in figures 4-2 and 4-3. If the controller is ready or the command is issued without testing busy, then the AU produces a TERM signal to indicate acceptance of input data for the RDS instruction (figure 4-2) or to indicate that output data is available to the I/O controller for a WDS instruction (figure 4-3).

4.3 INPUT/OUTPUT INTERFACE

The I/O interface card which normally occupies card slot IO0 in the Model 980 mainframe provides a means to expand the I/O bus to other back panels. The I/O interface card also contains the logic necessary to OR the interrupt lines from the I/O ports in the Model 980 basic mainframe to form one I/O interrupt line to the CPU. Jumper wires enable the user to select the address to read the I/O interrupts.

In the normal configuration, the I/O interface card may be used in ports IO1 through IO4 for further expansion of the external expansion chassis. The card decodes the group number to allow the maximum use of the available device addresses. The card also functions as a buffer of both input and output signals from and to the expansion back panel.

A detailed diagram of the I/O interface logic is illustrated in the *Model 980 Computer Maintenance Manual: Input/Output and Input/Output Expansion.*

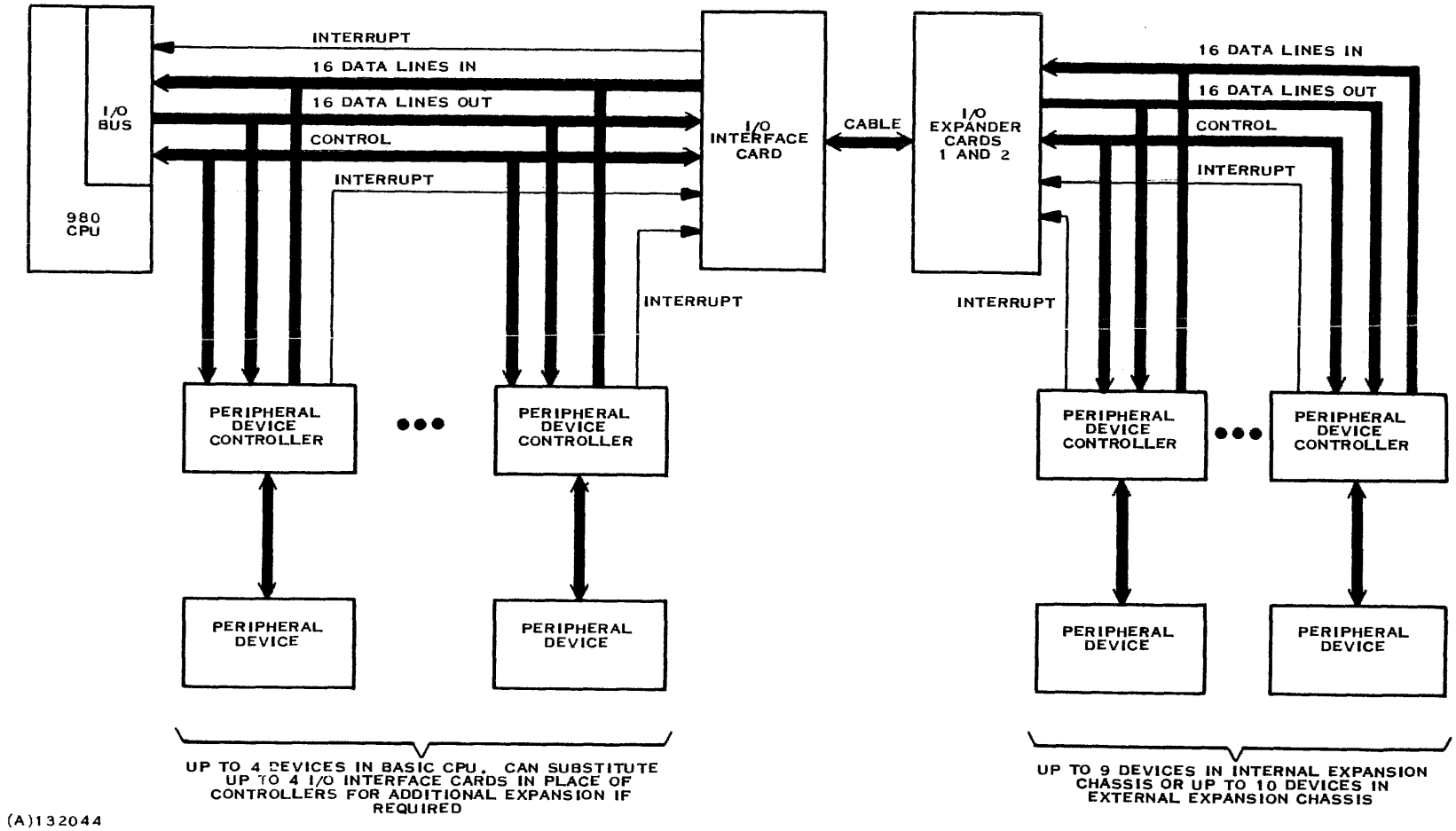


Figure 4-1. Model 980 Input/Output Bus Functional Diagram

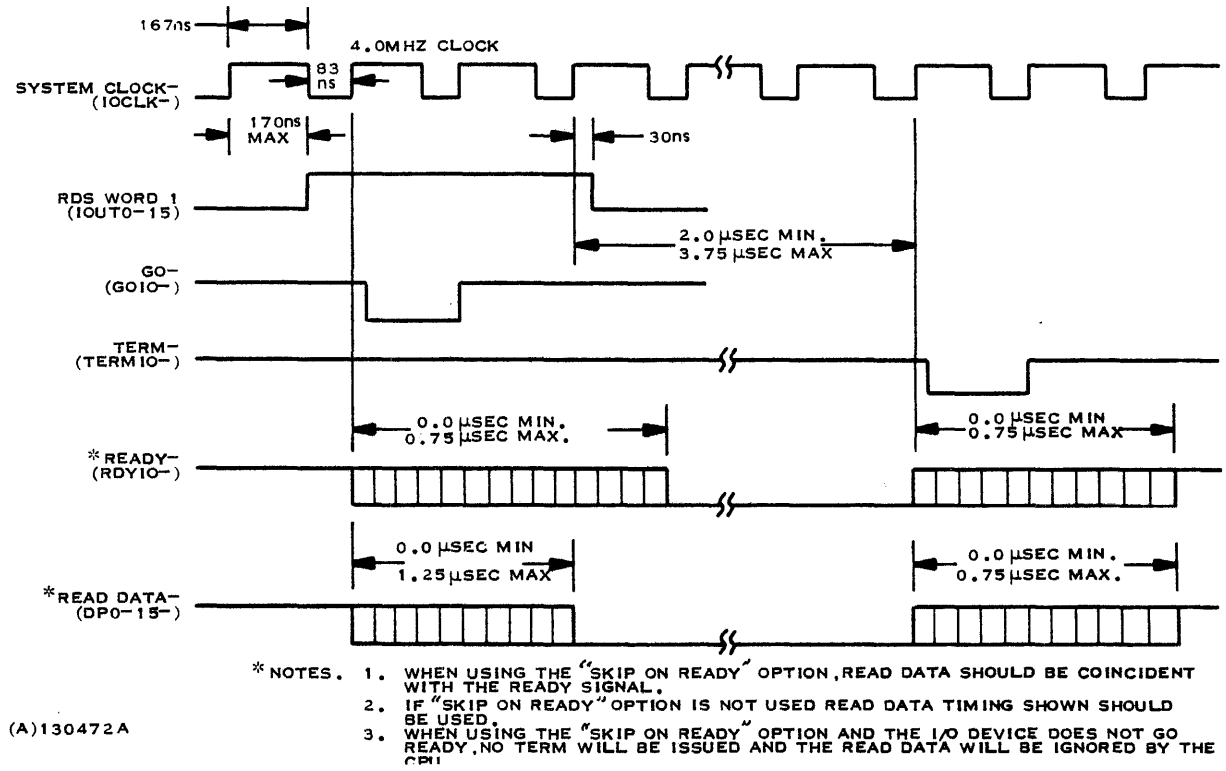


Figure 4-2. RDS Instruction Word Timing Diagram

Two types of symbols should be noted. When a connector pin symbol (→) is shown, the connector is labeled P1 or P2. This label is followed by a dash and the pin number. The P1 designation indicates the connector is a bottom connector and P2 designates a top connector which can complete the connection to a cable with the proper cable connector.

The jumper pad symbol (—o) indicates a pad that is provided to permit jumper wires to be inserted for address selection. Normally, the pad identifier (E19 for example) as shown is also reproduced on the component side of the printed circuit board. Refer to table 4-1 for the jumper address schedule.

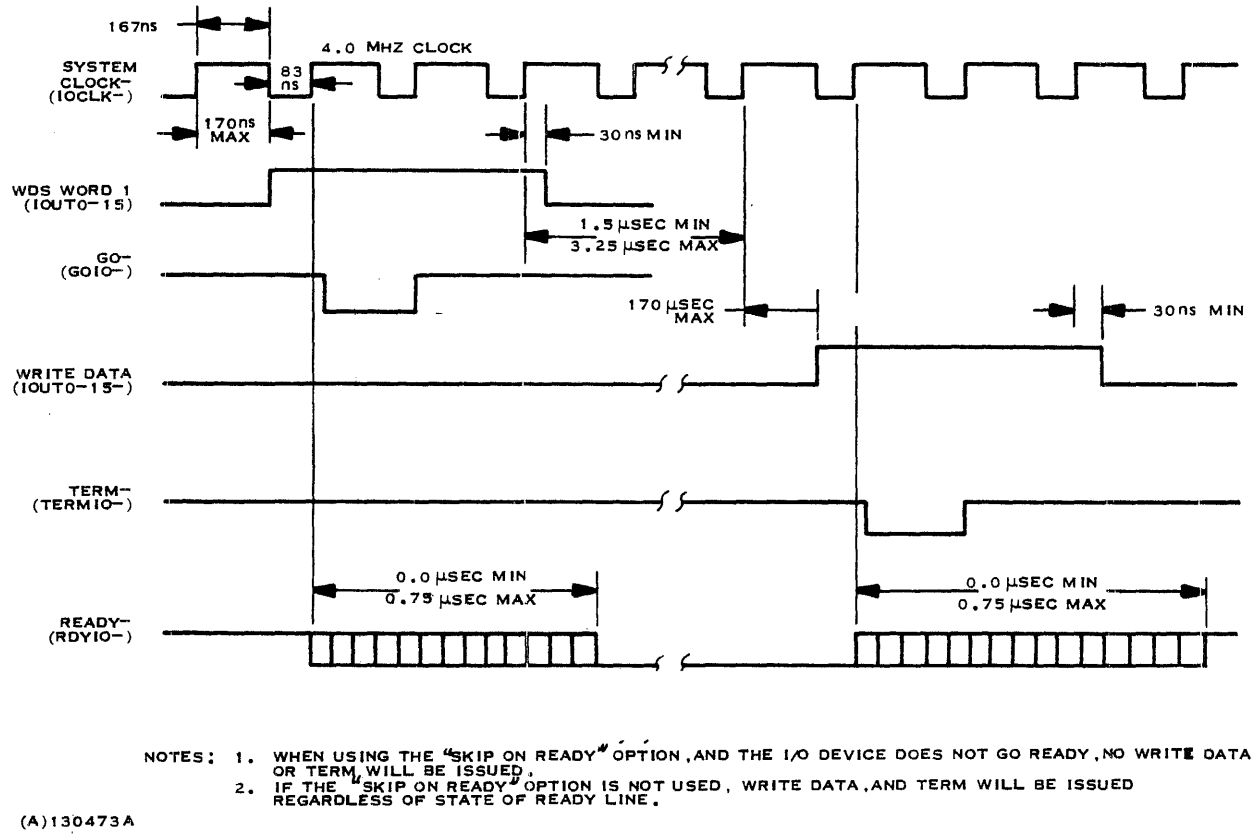


Figure 4-3. WDS Instruction Word Timing Diagram

Example:

As an example of jumper connections using table 4-1, the connections for address 13, group 0 are:

E-2 to E-24
E-4 to E-23
E-5 to E-22
E-7 to E-21
E-10 to E-20
E-13 to E-19
E-15 to E-27
E-17 to E-26

Table 4-1. Jumper Schedule for I/O Interface Card

Instruction Word 1 Bits								Explanation
Group Address Bits		External Register Address Bits						
5	6	9	11	12	13	14	15	
E-18	E-16	E-14	E-10	E-8	E-6	E-4	E-2	Jumpered when address bit true
E-17	E-15	E-13	E-9	E-7	E-5	E-3	E-1	Jumpered when address bit false
E-26	E-27	E-19	E-20	E-21	E-22	E-23	E-24	A jumper must start at each of these terminators and select either true or false sense for each of these address bits.

4.4 INPUT/OUTPUT EXPANSION

The I/O expander 1 and 2 cards are used with the I/O interface card to expand the Model 980 I/O bus. The electrical schematics of the I/O expander cards are illustrated in the *Model 980 Computer Maintenance Manual: Input/Output and Input/Output Expansion.* The expander cards provide buffered I/O bus signals to additional I/O back panels at the same logic level and pins as the mainframe I/O bus ports.

The I/O expander 1 card also provides group decoding for the expansion back panel. The result of the decode either gates or inhibits the GO, TERM and READY control signals to or from the expansion back panel. Table 4-2 gives the jumper schedule for the expander 1 card.

Example:

As an example of jumper connections using the table 4-2, the connections for group 0 are:

E-1 to E-8
E-3 to E-9
E-5 to E-7

The I/O expander 2 card provides register decoding for expansion interrupt inputs. It also contains the logic for interrupt ORing. Table 4-3 gives jumper schedule for the expander 2 card.

Example:

As an example of jumper connections using table 4-3, the connections for register address 13 are:

E-1 to E-4
E-9 to E-8
E-12 to E-3
E-13 to E-5
E-16 to E-6
E-18 to E-7

Table 4-2. Jumper Schedule for I/O Expander 1 Card

Group Bit			
5	6	7	Explanation
E-6	E-2	E-4	Jumpered when address bit true
E-5	E-1	E-3	Jumpered when address bit false
E-10*	E-11*	E-12*	Jumpered when address bit is not decoded (always selected)
E-7	E-8	E-9	A jumper must start at each of these terminals and select either true or false sense for each of these address bits if multiple groups are utilized.

*Normally, card is delivered with decode always enabled (VCC).

Table 4-3. Jumper Schedule for I/O Expander 2 Card

External Register Address Bits						
9	11	12	13	14	15	Explanation
E-11	E-9	E-17	E-15	E-13	E-1	Jumpered when address bit true
E-12	E-10	E-18	E-16	E-14	E-2	Jumper when address bit false
E-3	E-8	E-7	E-6	E-5	E-4	A jumper must start at each of these terminals and select true or false sense for each of these address bits.

Standard register addresses for I/O expansion are as follows:

Register Address	I/O Expansion Chassis
13	Internal
5C	External 1
5D	External 2
5E	External 3
5F	External 4

The register address is the hexadecimal equivalent of the binary value in bits 9 through 15 of the RDS/WDS instruction (first word). Bit 10 is always 0.

The cable between the I/O interface card and the I/O expander 1 card permits the transfer of signals to and from the I/O interface to access the basic I/O bus. Signals are transferred from the top edge connector of the I/O interface card to I/O expander 1. Except for SYSCLK-, these signals are transferred through twisted pairs of wires that are series-terminated with 82 ohms at the transmission end.

The SYSCLK- line is parallel-terminated at the receiving end with 390 ohms to Vcc and ground. Provisions are included at the I/O interface to disable the 16 data input lines (DP0-15) when an expansion cable is not connected to the top edge connector of the card. All output signals to the expansion back panel from I/O expanders 1 and 2 are driven by 74H40TTL networks.

4.5 I/O EXPANDER SIGNAL DESCRIPTIONS AND LOGIC

A simplified functional block diagram of the I/O expander is shown in figure 4-4. The I/O expander consists of the output data bus, the input data bus, interrupt lines, a clock, and control signals.

4.5.1 OUTPUT DATA BUS. The output data bus (WD(00-15)-) is a 16-bit data bus from the I/O interface card. This bus is connected to a NAND driver gate, and the driven signal bus (B(00-15)) may be fanned out to a maximum of 16 device controllers. (The maximum number of devices in the standard chassis configuration is 10 devices.)

4.5.2 INPUT DATA BUS. The input data bus (DP(00-15)-) is a 16-bit data bus from the 16 (maximum number) device controllers. The signals are fanned in to a single receiver on the I/O interface card. The fanin is accomplished in the expander back panel. In addition, an output signal from the control logic, INT EXST, is run into a NAND gate with the interrupt lines to produce an output that is tied into the data lines, DP(00-15)-. A NAND gate driver is included in the input data bus.

4.5.3 INTERRUPT LINES. Interrupt lines, one from each of the 16 device controllers, are run into inverters. This inverted output is used for two purposes. In one case, it is one of the inputs into a NAND gate whose output is the input data bus, the other input being the INT EXST control signal. In the other case, the inverted outputs are wire-ORed on an open collector inverter-driven bus to produce a single line, GPINT, to the I/O interface card. This signal indicates to the I/O interface module that one or more device controllers is signaling an interrupt to the CPU.

4.5.4 CLOCK. The Clock signal (XCXA from the I/O interface module and XCK- to the device controllers) is a one-third duty cycle clock in the False sense. The clock frequency is 4 MHz.

4.5.5 CONTROL SIGNALS AND LOGIC. The control signals include the GO, TERM, and RESET signals from the CPU and the READY signal to the CPU. These signals control the transfer of data between the CPU and the device controllers.

The RESET signal is sent to the device controllers through control and driver logic. The GO, TERM and RESET signals from the I/O interface module are input to control logic circuitry to produce a single signal, INT EXST, that is used to control gating of interrupt information onto the input data bus.

4.6 INPUT/OUTPUT SIGNALS

The Model 980 I/O bus signals are listed in table 4-4. These signals are listed as found in both the basic mainframe back panel and the expansion back panel. Pin numbers and descriptive remarks are also included.

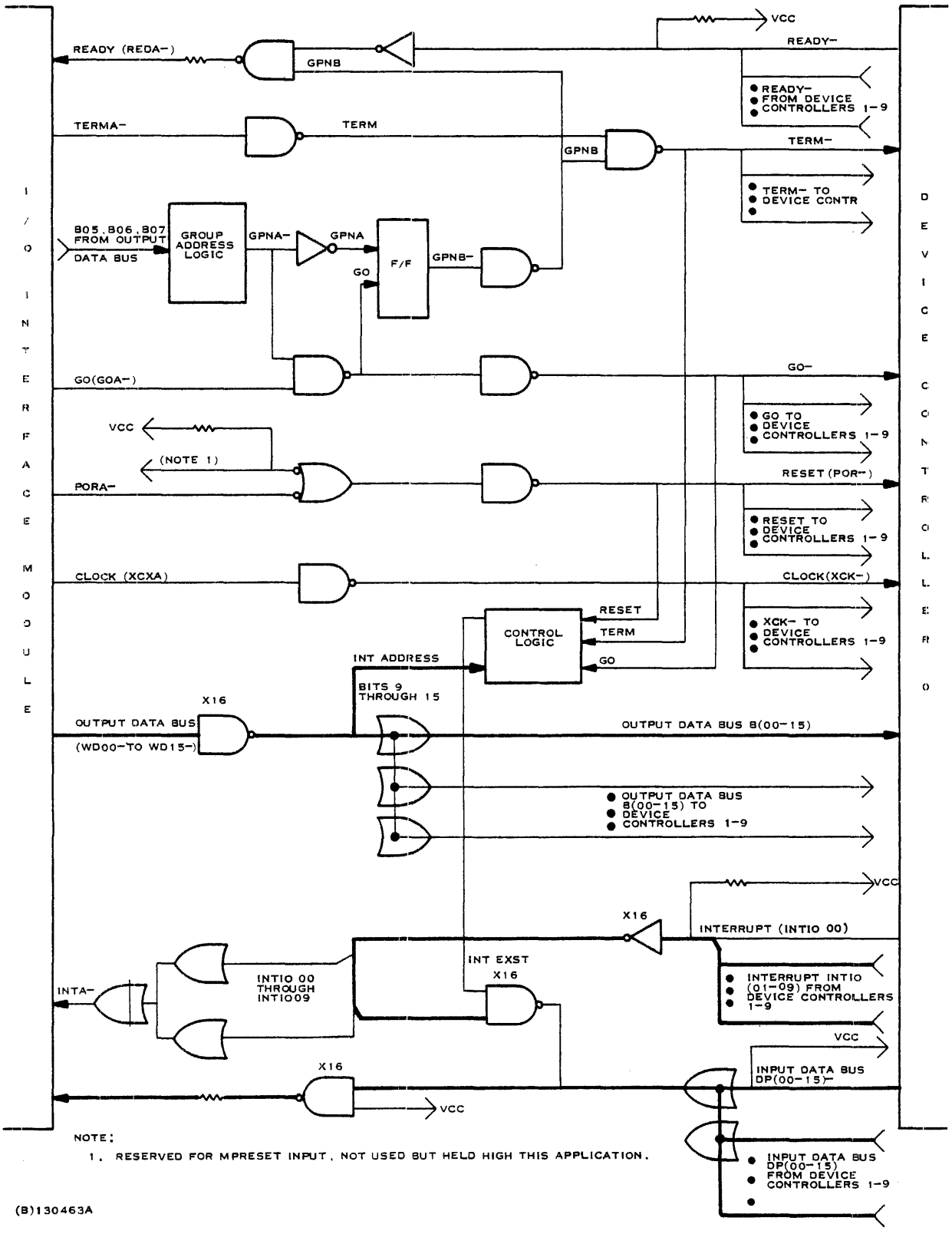
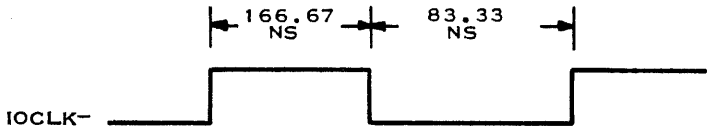


Figure 4-4. I/O Channel Expander, Simplified Block Diagram

Table 4-4. Input/Output Signals and Locations

Signal			
Mainframe Chassis	Expansion Chassis	Pin Number	Remarks
IOUT0	B00	25	The output data bus consists of IOUT (0-15). These signals are output as True data and are only valid during times indicated by the GOIO– and TERMIO– pulses.
IOUT1	B01	23	
IOUT2	B02	20	
IOUT3	B03	19	
IOUT4	B04	11	
IOUT5	B05	13	
IOUT6	B06	6	
IOUT7	B07	5	
IOUT8	B08	63	
IOUT9	B09	57	
IOUT10	B10	59	
IOUT11	B11	61	
IOUT12	B12	27	
IOUT13	B13	29	
IOUT14	B14	31	
IOUT15	B15	33	
DP0–	DP00–	73	The input data bus to the Model 980 consists of DP (0-15)–. The signals are wire-ORed to the input data bus and are driven by an open-collector regular TTL source. These signals are also gated by the I/O device and remain at a logic 1 while disabled. True data is transferred to the CPU as a logic 0.
DP1–	DP01–	75	
DP2–	DP02–	74	
DP3–	DP03–	55	
DP4–	DP04–	67	
DP5–	DP05–	69	
DP6–	DP06–	71	
DP7–	DP07–	65	
DP8–	DP08–	41	
DP9–	DP09–	43	
DP10–	DP10–	45	
DP11–	DP11–	39	
DP12–	DP12–	9	
DP13–	DP13–	15	
DP14–	DP14–	17	
DP15–	DP15–	7	
IOCLK–	XCK–	21	The IOCLK– signal is the I/O bus clock and is supplied in the False sense.



When the CPU is in the Clock mode, single clocks are supplied to the I/O bus as in the CPU.

Table 4-4. Input/Output Signals and Locations (Continued)

Signal			
Mainframe Chassis	Expansion Chassis	Pin Number	Remarks
GOIO–	GO–	47	The GOIO– signal is a 250 ns logic 0 pulse that is generated during the first word of an RDS or WDS instruction. This GOIO– signal indicates the external register number of the RDS or WDS instruction is present and stable on the IOUT (0-15) lines.
TERMIO–	TERM–	51	The TERMIO– signal is a 250 ns logic 0 pulse that indicates to an I/O device the termination of a single data word transfer. The TERMIO– signal, during an RDS instruction, acknowledges receipt of the data word by the CPU. During a WDS instruction, The TERMIO– signal indicates the presence of a stable data word on the IOUT (0-15) lines.
RDYIO–	READY–	37	The RDYIO– signal is a False signal supplied by the I/O device to indicate it is ready for a data transfer to or from the CPU. It is wire-ANDed to the I/O bus and is driven by a regular, open-collector, TTL source. A module may present RDYIO– if it is addressed and GO– (or GOIO–) is detected. RDYIO– must be removed when TERM– is detected. The RDYIO– signal need not be implemented for transfer of data which does not require use of SKIP on READY option with RDS or WDS instructions.
RESET–	POR–	49	The RESET– signal is a False signal that is used to reset all I/O controllers when power is first applied to the system or when the front panel RESET switch is pressed.
IOINT–	Not Applicable	35	Interrupts are False signals generated by the I/O controllers when operated in the interrupt mode and ready for data transfer. Once a controller interrupts, the controller should hold the interrupt condition until serviced. After being serviced, the controller must disable the related interrupt line until it is again ready for data transfer. Interrupt signals are driven by a regular open-collector TTL source.

Table 4-4. Input/Output Signals and Locations (Continued)

Signal			
Mainframe Chassis	Expansion Chassis	Pin Number	Remarks
			The IOINT– signal is the I/O interrupt that is sent to the CPU from the I/O interface card in I/O card location port IO0. This IOINT– is derived from the OR of the interrupts from I/O card ports IO1 through IO4 and the external interrupt from any expansion chassis.
INT1– INT2– INT3– INT4–	Not Applicable Not Applicable Not Applicable Not Applicable	35 35 35 35	Signals INT1 through INT4 are interrupts from ports IO1 through IO4, respectively. These negative logic signals terminate at the IO0 port at pins 8, 10, 12, and 53, respectively.
Not Applicable	INTIO0– to INTIO15–		Signals INTIO0– through INTIO15– are the interrupt signals supplied from I/O controllers when operated in an expansion chassis.
Not Applicable Not Applicable	+15 –15	3 54	+15 and –15 volts dc, respectively.
Not Applicable	+30	29, 30, 31, & 32	+30 volts is only found on the optional internal back panel at card slot REG. This voltage is required only if the ±15 volt optional regular card is used.
	VCC	77,78	+5 Vdc

SECTION V

AUXILIARY PROCESSOR PORT

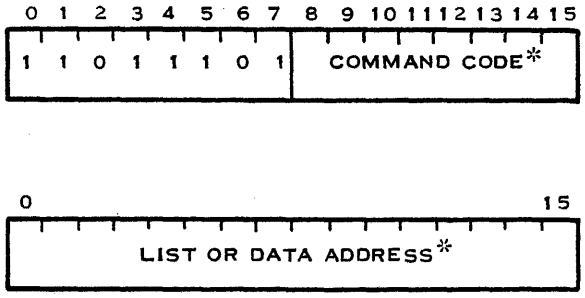
5.1 GENERAL

The Texas Instruments (TI) Model 980 Computer contains a Auxiliary Processor Port (APP) that is designed for use by external controllers which may be located internal or external to the computer chassis to perform optional operations under program control. These operations include special computer instructions sets, dual processor control, and floating point operations. The APP is activated by the Auxiliary Processor Initiate (API) instruction. A user-defined API external controller can be plugged into the APP of the Model 980 chassis if it is a single card, or the API expander can be used to allow the API controller to be placed in an expansion chassis. The API expander board provides buffered control and data lines to external chassis at the same logic levels that exist at the APP.

The details of the logic and electronic circuits of the Auxiliary Processor Port are specified in the Auxiliary Processor Port Specification, TI part no. 960683-9901.

5.2 INSTRUCTIONS

An auxiliary processor in the Model 980A Computer is activated by the Auxiliary Processor Initiate (API) instruction. This is a two word instruction with the following message format.



*THE FORMAT OF THESE BITS IS DETERMINED BY THE EXTERNAL DEVICE.

The first instruction word contains the operational code for the API instruction in bits 0 through 7 and the command code in bits 8 through 15. The second word contains the list or data address which may define the starting address for a list to define processor parameters or other data for the auxiliary processor.

API is not a privileged instruction. However, the Privileged Instruction Feature (PIF) trap occurs immediately if an auxiliary processor attempts to use protected memory when the PIF is enabled.

5.3 THEORY OF OPERATION

The APP is controlled by the CPU and is only active during the execution of an API instruction. The CPU applies a strobe (ENAPI1–) to the APP when the first API instruction word is available on the memory data output lines. A second strobe (ENAPI2–) is applied when the second

instruction word is present. The API strobes occur at approximately 1.0 microsecond intervals. If the external controller that is being addressed by the API instruction is available to the APP, the controller must provide an acknowledge (DEVTHERE) to the APP before the second API strobe occurs. The Central Processing Unit (CPU) then enters a wait state and allows the APP to access memory as desired. If an external controller does not accept the API instruction, the CPU executes an illegal operation code trap to location 2.

The CPU will exit the wait state for an acknowledged API instruction when one of the following three conditions exist. The first exit occurs when the external controller has completed a normal operation and has produced an API Operation Complete (APOPCOMP) signal. This signal allows the CPU to continue to the next sequential instruction. The second type of exit occurs when the CPU receives an interrupt of any type. When the CPU receives an interrupt, the APP notifies the external controller that an interrupt has occurred. The external controller can then abort the operation, store any intermediate results, and release the port to allow the CPU to process the interrupt. The time available for the API device to complete the process before releasing the APP is determined by the system configuration. After the interrupt is processed, the CPU executes the API instruction that was in progress when the interrupt occurred which allows the external controller to continue the operation and exit normally if no other interrupts occur. The third API abort condition occurs if the external API device attempts to address protected memory when the PIF is enabled. When this occurs, the CPU executes an immediate PIF trap and aborts the API operation. The APP also enables the address violation line to the external controller, which normally resets and waits for further API instructions.

The APP has access to three status register bits. Control lines are provided by the APP to allow status register bits as listed in table 5-1 to be set or reset.

5.3.1 **SIGNALS.** The APP output and input signals to the Model 980 arithmetic unit are listed in table 5-2 and table 5-3, respectively. All signals are standard TTL levels. All memory output data, memory output control lines, system clocks, and master resets should be loaded with only one TTL load. Input lines to the CPU from the APP should be driven by gates that can drive four TTL levels. All other output lines from the CPU to the APP can be loaded with four or less TTL loads.

A dash (–) at the end of a signature indicates a negative logic signal; i.e., a low output voltage state (0) is considered the active state and the inactive state is the high voltage state (1).

5.3.2 **TIMING.** The timing diagrams of the APP signals are illustrated in figures 5-1 and 5-2. The timing relationships that are illustrated in these figures apply to the signals at the APP back panel connector in the Model 980 CPU chassis. These figures are shown as mimimum or maximum limits.

Table 5-1. Status Register Bit Functions

Bit	Function
0-1	Compare Indicators. Indicates result of last compare operation as follows: 00–less than 01–equal to 10–greater than 11–not allowed
2	Overflow Indicator–Indicates overflow

Table 5-2. Auxiliary Processor Port Output Signals to CPU

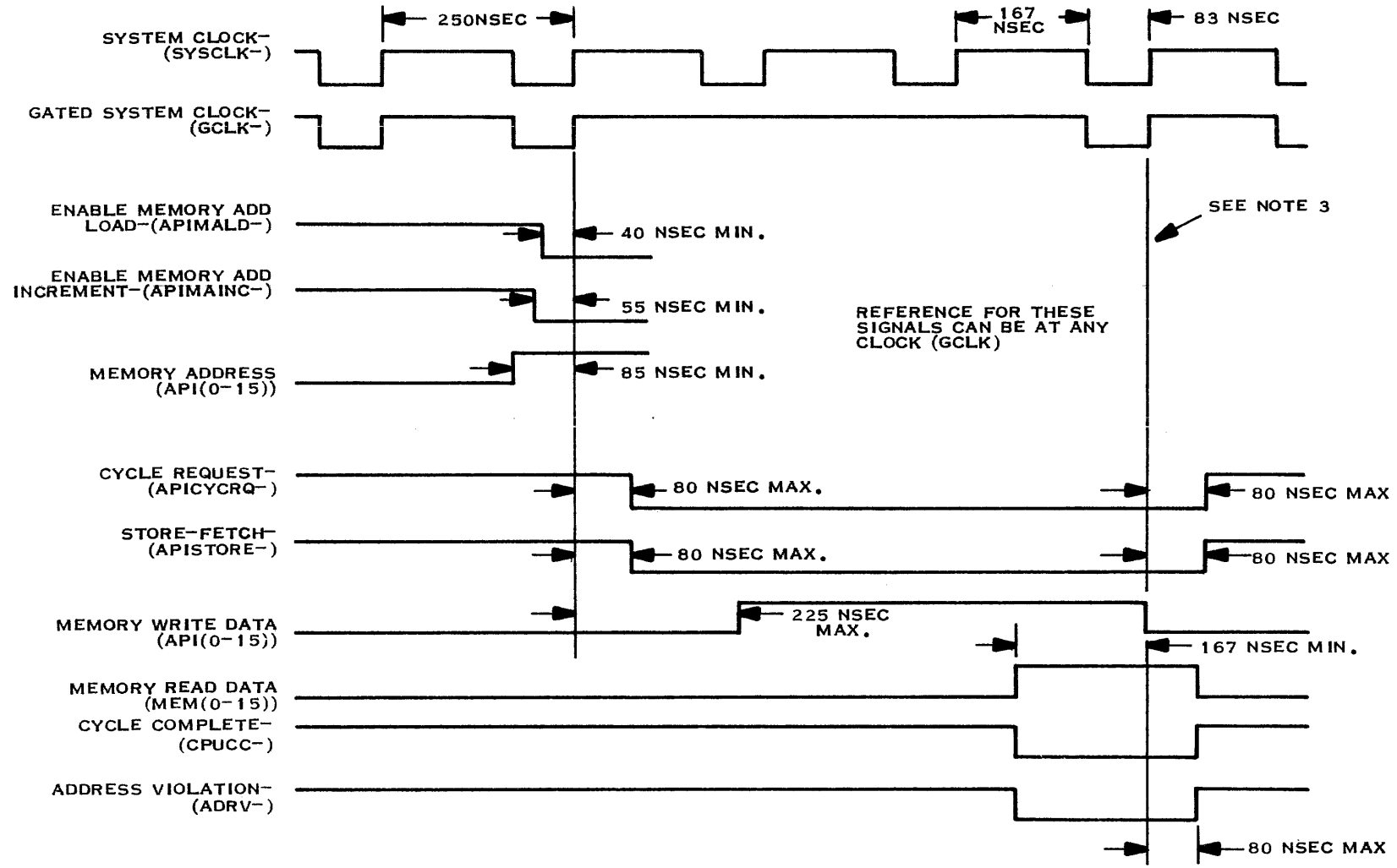
Signature	Pin	Description
API0–	6	
API1–	7	
API2–	19	
API3–	41	
API4–	42	
API5–	50	
API6–	51	
API7–	53	
API8–	55	API MEMORY INPUT DATA. Sixteen negative logic output lines which provide memory address and memory data to the Model 980 arithmetic unit.
API9–	59	
API10–	61	
API11–	62	
API12–	66	
API13–	67	
API14–	69	
API15–	71	
DEVTHERE–	73	DEVICE THERE. A negative logic output line that indicates to the CPU that an addressed API device can accept instructions. This signal must be given by the APP controller to the CPU before the second API strobe occurs to prevent the CPU from executing an illegal operational code trap to memory location 2.
INTABORT–	74	INTERRUPT ABORT. A negative logic signal that indicates to the CPU that the API device will allow the CPU to disable the APP, process interrupt(s), and re-execute the API instruction that was in progress.
APOPCOMP–	63	AUXILIARY PROCESSOR OPERATION COMPLETE. A negative logic signal which indicates that the API device has completed its operation. The CPU will then continue to execute subsequent instructions.
APICYCRQ–	64	AUXILIARY PROCESSOR CYCLE REQUEST. A negative logic signal that requests a memory cycle from the memory controller. This signal should stay at a logic 0 until Cycle Complete (CPUCC–) occurs for the requested memory cycle.
APISTORE–	38	AUXILIARY PROCESSOR STORE. A negative logic signal that indicates whether the requested memory cycle is a store (write) or fetch (read) cycle. A logic 0 on this line indicates a store cycle. Do not change this signal during a memory cycle until Cycle Complete occurs.
APIMAINC–	39	AUXILIARY PROCESSOR MEMORY ADDRESS INCREMENT. A negative logic signal that will cause the memory controller to increment the present memory address.
APIMALD–	29	AUXILIARY PROCESSOR MEMORY ADDRESS LOAD. A negative logic signal that cause the data word on the memory input lines [API (0-15)–] to be loaded into the memory address register.
APISTO–	21	API STATUS BIT 0. A negative logic signal which can be used to set or reset status register bit 0 in the CPU. When this line is at a low level, status register bit 0 is set to a 1 when the status register clock for bits 0 and 1 is enabled by APIS01CK–.
APIST1–	23	API STATUS BIT 1. A negative logic signal which can be used to set or reset status register bit 1 in the CPU. When this line is at a low level, status register bit 1 is set to a 1 when the status register clock for bits 0 and 1 is enabled by APIS01CK–.

Table 5-2. Auxiliary Processor Port Output Signals to CPU (Continued)

Signature	Pin	Description
APIST2–	25	API STATUS BIT 2. A negative logic signal which can be used to set or reset status register bit 2. When this line is at a low level, status register bit 2 is set to a 1 when the status register clock for bit 2 is enabled by APIS2CK–.
APIS01CK–	75	API STATUS BITS 0, 1 CLOCK. A negative logic signal that enables the CPU clock to status register bits 0 and 1.
APIS2CK–	72	API STATUS BIT 2 CLOCK. A negative logic signal that enables the CPU clock to status register bit 2.
POFF–	28	EXTERNAL CHASSIS POWER OFF. A negative logic signal to the CPU which can be used to set status register bit 15 and cause the CPU to execute an internal trap if power fails at the external chassis where the APP controller is located. This line should be driven by an open-collector gate since it is also available to other chassis. This line should be used in conjunction with MRESET– and should go high at least 50 microseconds before MRESET– occurs.
MRESET–	8	EXTERNAL MASTER RESET. A negative logic signal to the CPU which causes the CPU to reset. During operation, a relay is normally available in the external power supply chassis that can be connected to this line when desired. This line should only be driven by relay or transistor which can sink 50 milliamperes. This line should only be active 50 microseconds after POFF– occurs. Activation of this line can cause memory errors if this sequence does not occur.

Table 5-3. Auxiliary Processor Port Input Signals from CPU

Signature	Pin	Description
RESET–	31	MASTER RESET. A negative logic signal from the front panel RESET switch that is used to initialize the API device. During power up the power supply also causes this signal to go low.
SYSCLK–	35	SYSTEM CLOCK. A negative logic signal that is the free running system clock from the memory controller. Clock frequency is 4 megahertz with a 33.3 percent duty cycle (167 nanoseconds at logic 1, and 83 nanoseconds at logic 0).
GCLK–	33	GATED SYSTEM CLOCK. A negative logic signal identical to free-running SYSTEM CLOCK (SYSCLK–), except that during a memory cycle, pulses after the clock edge that initiates the memory cycle are inhibited. Clock pulses resume with the Cycle Complete (CPUCC–) signal from memory.
CPUCC–	10	CYCLE COMPLETE. A negative logic signal that indicates a memory cycle has been completed.
ENAPI1–	49	AUXILIARY PROCESSOR INITIATE STROBE 1. A negative logic signal that indicates API word 1 is stable on the memory output lines.
ENAPI2–	37	AUXILIARY PROCESSOR INITIATE STROBE 2. A negative logic signal that indicates API word 2 is stable on the memory output lines.
INTM	12	INTERRUPT. A positive logic signal that indicates the CPU has received an interrupt. At this time, API device should finish processing as soon as possible to allow the CPU to process the interrupt.
MEM0	20	MEMORY OUTPUT DATA. Sixteen positive logic data lines which provide memory output data.
MEM1	18	
MEM2	16	
MEM3	14	
MEM4	26	
MEM5	22	
MEM6	24	
MEM7	15	
MEM8	58	
MEM9	17	
MEM10	54	
MEM11	60	
MEM12	45	
MEM13	56	
MEM14	40	
MEM15	47	
ENAPI	13	ENABLE API. A positive logic signal that indicates the CPU is in the API state. This line can be used to gate cycle complete and other memory control signals.
ADRV–	5	ADDRESS VIOLATION. A negative logic signal from memory controller indicating protected memory has been addressed while PIF is enabled. On next system clock, CPU will leave API instruction state and execute PIF trap.
GROUND	1	CPU ground
GROUND	2	
GROUND	79	
GROUND	80	
VCC	78	CPU +5-volt supply
VCC	77	



NOTES:
1. ADDRESS VIOLATION (ADRV) WILL CAUSE THE CPU TO IMMEDIATELY TRAP TO LOCATION 2 AND ABORT THE API INSTRUCTION IN PROGRESS.
2. SEE FIGURE 5-2 FOR AP PORT CONTROL TIMING.
3. CAN BE DELAYED 250 TO 750 NSEC DUE TO MEMORY REFRESH WHICH OCCURS AT 31 µSEC INTERVALS.

Figure 5-1. Auxiliary Processor Port Memory Timing

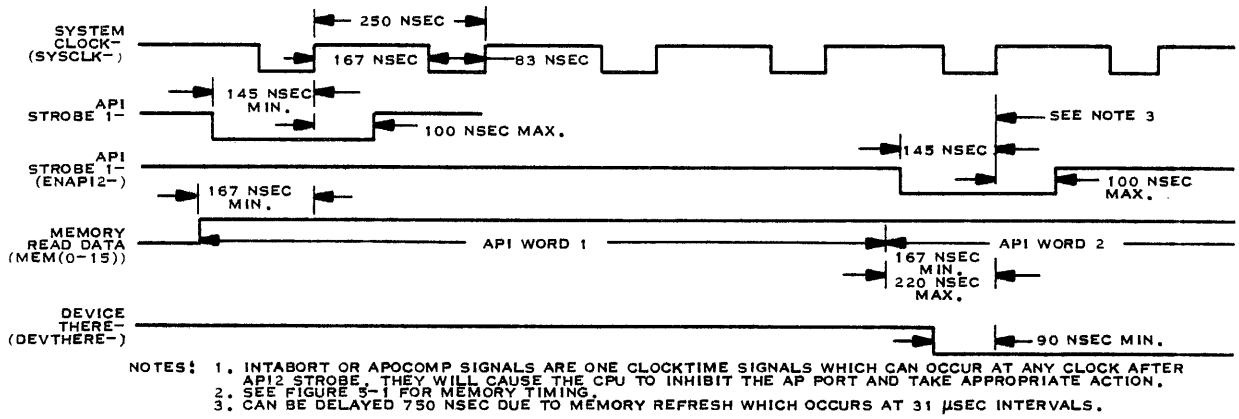


Figure 5-2. Auxiliary Processor Port Control Timing

SECTION VI

I/O BUS DEVICES

6.1 GENERAL

The following paragraphs describe the standard I/O bus modules used with a 980 computer system. Each description provides a brief summary of electrical and physical characteristics including the pin assignments for the external connector. This information is not sufficient for designing a hardware interface or device handler software routine. The paragraphs in this section provide references for additional sources of specifications. The modules discussed are as follows:

- I/O Data Module
- Vectored Interrupt Module
- Communications Module
- Full Duplex Synchronous Communication Module
- ±15-Volt Regulator Module
- Card Reader Controller
- Paper Tape Punch Interface Module
- Paper Tape Reader Interface Module
- Interval Timer

Typical environmental and reliability performance specifications for I/O bus modules are presented in table 6-1. When the environmental specifications are different, they are detailed in the paragraph which discusses the individual module.

6.2 I/O DATA MODULE

The I/O Data Module, TI part no. 961648-0001 through 961648-0005, provides the 980 computer with a 16-bit parallel, general purpose, DTL/TTL-compatible interface. The available configurations are detailed in table 6-2. In addition to the 16 input and 16 output lines, the interface may cause an I/O bus interrupt and supplies the external device with request and acknowledge signals.

Programming and interface requirement information is described in the *Model 980 Computer Input/Output Data Module User's Manual,* TI part no. 965956-9701. The external interface connector, top edge, is shown in table 6-3. The characteristics of the I/O data module are shown in table 6-4.

Table 6-1. Typical Environmental Specifications for I/O Bus Module Circuit Cards

Characteristic	Specification
Environmental	
Temperature	
Operating	0° to 70°C
Storage	−65° to 150°C
Humidity	
Operating	10% to 85% relative
Storage	0 to 90% relative
Operating Barometric Pressure	25 to 32 in. Hg

Table 6-2. I/O Data Module Configurations

961648 Assembly Dash Number	Interrupt Option Selected	Input Circuit Impedance (Ohms)	Pullup Resistor Source Voltage**	Pullup Resistor Value (Ohms)	Remarks
–0001	No	510	None	1000	
–0002	No	100	None	1000	
–0003	No	100	Internal (5 volts)	1000	Signal on input line 0 is inverted and jumpered to the top edge connector pin normally assigned to VCC EXT (R-)
–0004	Yes	100	None	1000	Interrupt occurs on positive to negative transition of IN0.
–0005	No	100	None	1000	

**User must select source when none is specified.

Table 6-3. Input/Output Data Module Signals and Connector Pin Assignments

Signal	Top Edge Connector Pin	Signal	Top Edge Connector Pin
IN00	3	OUT05–	26
IN01	4	OUT06–	35
IN02	2	OUT07–	36
IN03	1	OUT08–	29
IN04	7	OUT09–	27
IN05	10	OUT10–	19
IN06	6	OUT11–	20
IN07	5	OUT12–	31
IN08	15	OUT13–	32
IN09	17	OUT14–	28
IN10	14	OUT15–	30
IN11	11	OREADY–	33
IN12	12	OACK–	16
IN13	8	IREADY–	13
IN14	9	IACK–	34
IN15	18	+5 VOLTS	N–
OUT00–	25	VCCEXT	R–
OUT01–	24	MASTER RESET–	L–
OUT02–	21	OUTPUT REG CLEAR–	K–
OUT03–	23	GRD	A through J–
OUT04–	22		

Table 6-4. I/O Data Module Characteristics and Specifications

Characteristic	Description or Specification
Electrical	
Input Lines	16 data lines 2 control lines
Output Lines	16 data lines 2 control lines
Interrupts	I/O bus interrupts (input and output)
Optional Features	Input receiver impedance Output transmitter source voltage Interrupt option (external input) Module address Output register reset +5 Vdc supplied to device
Electrical Power Requirement	+5 volts dc at 1.4 A
Environmental Specifications	
Temperature	
Operating	0° to 70°C
Storage	–40° to 100°C
Humidity	
Operating	10% to 85% relative, noncondensing
Storage	5% to 95% relative, noncondensing
Operating Barometric Pressure	25 to 32 in. Hg

6.3 VECTORED INTERRUPT MODULE

The priority vector interrupt option is implemented with an expandable set of vectored interrupt modules. Each module (TI part no. 973300-0001) provides eight interrupt lines. Up to four modules may be used together to provide a maximum of 32 vectored interrupt lines. Each interrupt line has two dedicated memory locations associated with it. A vectored interrupt signal causes a CPU interrupt on priority level 2, and when processed, the interrupt causes the CPU to branch to the trap addresses associated with the interrupt line.

The programming and interface requirement information for this module are described in the *Specification-980 Vectored Interrupt Module,* TI part no. 973301-0001.

The external interface connector pin assignments are described in table 6-5.

A summary of module characteristics is presented in table 6-6.

6.4 COMMUNICATIONS MODULE

The Communications Module, TI part no. 966637-0001, supplies a serial interface for the 980 computer. Specifically, the unit provides an RS232C compatible interface for Bell data sets Models 103A or F, or equivalent, and Models 202C or D, or equivalent. It provides an optically isolated current loop interface for use with Teletype or equivalent terminals. Also, a differential line driver/receiver interface is supplied. This module requires ±15 Vdc power.

Table 6-5. Vectored Interrupt Module Signals and External Connector Pin Assignments

Connector Pin	Signal Name	Explanation
P2-10	INTRQ 0–	Interrupt Input Lines
P2-9	INTRQ 1–	
P2-8	INTRQ 2–	
P2-7	INTRQ 3–	
P2-B	INTRQ 4–	
P2-2	INTRQ 5–	
P2-3	INTRQ 6–	
P2-C	INTRQ 7–	
P2-13	INTRQ–	Signal EXPINT– buffered
P2-15	BUSY 0	Busy Lines
P2-17	BUSY 0	
P2-19	BUSY 0	
P2-16	BUSY 0	
P2-5	BUSY 0	
P2-E	BUSY 0	
P2-D	BUSY 0	
P2-4	BUSY 7	

Table 6-6. Vectored Interrupt Module Characteristics and Specifications

Characteristic	Description or Specification
Interrupts	8 lines, expandable by adding modules to 32 lines. Interrupts CPU on priority level 2.
Electrical Power Requirement	+5 volts dc at 850 mA
Environmental Specifications	(See table 6-1)

Programming and interface requirements are supplied in the *Model 980 Computer Communications Module User's Manual,* TI part no. 966643-9701. The external interface connector is shown in figure 6-1. The characteristics of the I/O Module are summarized in table 6-7.

6.5 FULL DUPLEX SYNCHRONOUS COMMUNICATION MODULE

The Synchronous Communication Module (TI part no. 966538-0001) completes the interface between the Model 980 Computer and a Bell or Bell-compatible synchronous modem. This module is on a wire-wrap board. Data rate is determined by the type of modem used. All modems must be internally clocked. The module may be installed in any one-inch I/O slot. The module requires that ±15 Vdc power be furnished.

The external edge connector pin assignments are described in table 6-8. The programming and interface requirements are described in detail in the *Model 980 Computer Full Duplex Synchronous Communication Module User's Manual,* Manual No. 943006-9701. The characteristics are summarized in table 6-9.

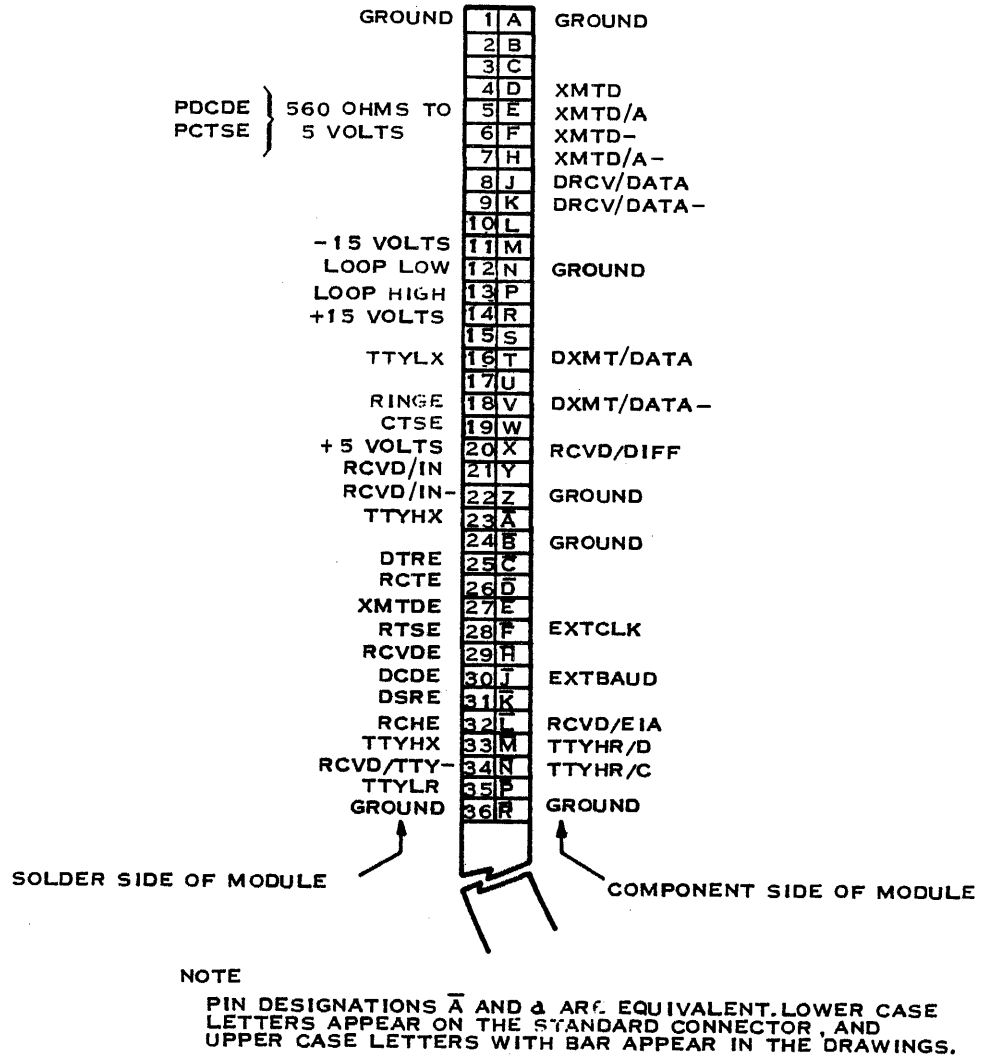


Figure 6-1. Communications Module Interface Connector Pins

6.6 REGULATOR MODULE, ±15 VOLT

The ±15-volt regulator module (TI part no. 226855-0001) must be used to supply two of the voltages required by the Communications Module and the Full Duplex Synchronous Communication Module when these modules are used in the internal CRU expansion. The module obtains power from the 35-volt ac pins of the internal expansion I/O port labeled REG. Up to 360 milliamperes of each voltage is supplied, which is adequate to power a number of modules, depending on the individual module options. Requirements for more current may be satisfied by attaching external supplies to the wiring of the CRU back panel. The regulator plugs into the internal expansion slot labeled REG.

Table 6-7. Communications Module Characteristics and Specifications

Characteristic	Description or Specification
Data Interface	Serial; selectable to EIA RS232, optically coupled isolation current loop, or differential line driver/receiver
Data Transfer Rate	Selectable to 75, 110, 150, 300, 1200, 2400, 4800 or 9600 baud
Parity	Selectable: odd, even or none
Electrical Power Requirements (maximum)	
Without Current Loop	+5 ±0.25 volts dc at 1.0 A −15 ±0.5 volts dc at 0.052 A +15 ±1.0 volts dc at 0.044 A
With 20 mA loop Using ±15-volt dc Module	+5 ±0.25 volts dc at 1.0 A −15 ±0.5 volts dc at 0.072 A +15 ±1.0 volts dc at 0.064 A
With 60 mA loop Using ±15-volt dc module	+5 ±0.25 volts dc at 1.0 A −15 ±0.5 volts dc at 0.112 A +15 ±1.0 volts dc at 0.104 A
Environmental	
Temperature	
Operational	0° to 70°C
Storage	−40° to 100°C
Humidity	
Operational	0 to 95% relative, noncondensing
Storage	0 to 95% relative, noncondensing
Operational Barometric Pressure	25 to 32 in. Hg

Normally there are no external connections to the module. The module supplies ±15 volts to existing I/O back panel wiring. The ±15 volts may be obtained from the top edge connector of the module as listed in table 6-10.

Specifications for the regulator module are listed in table 6-11.

6.7 CARD READER CONTROLLER

The Card Reader controller module (TI part no. 217556-0001) provides the interface between the 980 computer and a card reader peripheral device. This is the universal interface for several models of card readers.

Table 6-8. Synchronous Communication Module Top Edge Connector Pin Assignments

Pin	Name	Voltage Levels	Description
3	PLUS15V	–	Input for +15 volts dc
4	MINUS15V	–	Input for –15 volts dc
5	XSK-	TTL	Serial clock output for line synchronization
6	DCTB–	TTL	Dibit clock output for line synchronization
7	RCVDTRU	TTL	True output of received data
8	RCVDTRU–	TTL	False output of received data
9	XMTDTRU	TTL	True output of transmitted data
10	XMTDTRU–	TTL	False output of transmitted data
11	PENB	TTL	Parity enable
12	PODD	TTL	Parity select
13	HDENB	TTL	Hafl duplex enable
21	NEWSYNC	EIA	New sync output line to modem
22	CTSE	EIA	Clear to send input line from modem
23	DCT	EIA	Dibit clock transmit line from modem
24	RINGE	EIA	Ring indicator line from modem
25	DTRE	EIA	Data terminal ready line to modem
26	SCR	EIA	Serial clock receive line from modem
27	XMTDE	EIA	Transmitted data line to modem
28	RTSE	EIA	Request to send line to modem
29	RCVDE	EIA	Received data line from modem
30	DCDE	EIA	Data carrier detect line from modem
31	DSRE	EIA	Data set ready line from modem
32	SCT	EIA	Serial clock transmit line from modem
A,M,N,P R,S,T,U, V,W	GROUND	–	System ground
C	CPUP15V	–	Internally supplied +15 volts dc
D	CPUM15V	–	Internally supplied –15 volts dc
E,F	RTSCLK–	TTL	Line synchronization clock input
H,J	RCVD	TTL	Received data input
K,L	XMTD	TTL	Transmitted data input

Table 6-9. Synchronous Communication Module Characteristics and Specifications

Characteristic	Description or Specification
Data Interface	Serial for synchronous modem
Data Transfer Rate	Determined by modem-provided clock
Parity	Selectable: odd, even or none
±15 Vdc Voltage Supply	Supplied externally or internally
Electrical Power Requirements	+5 volts dc at 1.6 A nominal, 2.5 A maximum
	+15 volts dc at 0.040 A nominal, 0.088 A maximum
	−15 volts dc at 0.036 A nominal, 0.080 A maximum
Environmental Specifications	(See table 6-1)

Table 6-10. ±15-Volt Regulator Signals and Connector Pin Assignments

Signal	Pins
+15 V	20, 21, X, Y
GND	18, 19, 36, 1, A, V, W, $\overline{R}$
−15 V	16, 17, T, U

Table 6-11. ±15-Volt Regulator Module Specifications

Characteristic	Specification
Inputs	35 volts ac at 1 A from CPU power supply
Output	±15 volts dc at 360 mA ±0.2% total line and load

The signals provided on the top edge external connector are shown in table 6-12. The interface requirements and programming description are specified in the *Model 980 Computer Card Reader User's Manual,* 966317-9701. The module characteristics are summarized in table 6-13.

6.8 PAPER TAPE PUNCH INTERFACE MODULE

The Paper Tape Punch Interface Module (TI part no. 217564-0001) permits transfer of data from the 980 computer to paper tape through the I/O bus.

The interface and programming requirements are described in the *Model 980 Computer Paper Tape Punch User's Manual,* TI part no. 965944-9701. The external interface connector pin assignments are shown in table 6-14. The characteristics of the module are summarized in table 6-15.

Table 6-12. Card Reader Controller Signals and Card Reader Connector Pin Locations

Pin	Signal Line	To/From Controller	Pin	Signal Line	To/From Controller
1	Spares		A	Spares	
2			B		
3			C		
4			D		
5	Ground 1:Data Rows		E		
6	Ground 2:Data Rows		F	Data Row 6 (DR6)	To
7	Data Row 9 (DR9)	To	H	Data Row 5 (DR5)	To
8	Data Row 4 (DR4)	To	J	Data Row 3 (DR3)	To
9	Data Row 8 (DR8)	To	K	Data Row 12 (DR12)	To
10	Data Row 2 (DR2)	To	L	Data Row 7 (DR7)	To
11	Data Row 1 (DR1)	To	M	Ground 3:Column Index	
12	Data Row 10 (DR10)	To	N	Ground 4:Common	
13	Data Row 11 (DR11)	To	P	Ground 5: Common	
14	Cycle Complete (CYCP)	To	R	Feed Command (FEED)	From
15	Column Index (COLX)	To	S	Reader Ready (RDY)	To
16	Feed Error (FDER)	To	T	Card Presence (CP)	To
17	Power Disable (PWRD)	To	U	Data Presence (DP)	To
18	Stop Command (STOPC)	From	V	Data Error (DAER)	To
19	Reject Command (REJ)	From	W	Stacker Full (STF)	To
20	Start Command (STRTC)	From	X	Hopper Empty (HOE)	To
21	Power On (PWRN)	To	Y	Feed & Ready Invert (FRINV)	To
22	Do not connect to these pins.		Z	Do not connect to these pins.	
23			a		
24			b		
25			c		
26			d		
27			e		
28			f		
29			h		
30					

Table 6-13. Card Reader Controller Characteristics and Specifications

Characteristic	Description or Specification
Data Interface	Parallel; DTL/TTL compatible
Electrical Power Requirement	+5 volts dc ±2% at 0.31 A
Environmental Specifications	
Temperature	
Operating	0° to 50°C
Storage	−40° to 100°C
Humidity	
Operating	10% to 85% relative, noncondensing
Storage	10% to 85% relative, noncondensing
Operating Barometric Pressure	25 to 32 in. Hg

Table 6-14. Paper Tape Punch Interface Module Signals

Comment	PTP Interface Connector Pin	Signal	1075/3075 PTP Unit
	P2–$\overline{L}$	TRACK 1	P1–1
	P2–$\overline{F}$	TRACK 2	P1–2
	P2–$\overline{B}$	TRACK 3	P1–3
	P2–X	TRACK 4	P1–4
	P2–T	TRACK 5	P1–5
	P2–N	TRACK 6	P1–6
	P2–J	TRACK 7	P1–7
	P2–D	TRACK 8	P1–8
TWPR Common		SIGNAL GROUND	P1–25
	No Connection	DIRECTION	P1–10
	P2–32	PUNCH COMMAND	P1–11
	P2–13	PUNCH READY–	P1–12
Not Used on 980	P2–5		
	P2–17	SYSTEM READY–	P1–13

Table 6-15. Paper Tape Punch Interface Module Characteristics and Specifications

Characteristic	Description or Specification
Data Interface	TTL compatible
Electrical Power Requirement	+5 volts dc at 60 mA
Environmental Specifications	(See table 6-1)

6.9 PAPER TAPE READER INTERFACE MODULE

The Paper Tape Reader Interface Module (TI part no. 217570-0001) provides the I/O bus interface between the 980 computer and a paper tape reader peripheral device. Several similar paper tape reader models may be controlled with this interface.

The programming considerations and interface requirements for this controller are described in the reference manual, *Model 980 Computer Paper Tape Reader User's Manual,* TI part no. 965945-9701. External interface pin assignments are listed in table 6-16. The characteristics are summarized in table 6-17.

6.10 INTERVAL TIMER

The Interval Timer module (TI part no. 966580-0001) is an I/O bus device used to determine real-time intervals of from 10 microseconds to 40.96 seconds. These intervals are selectable in resolutions of 10 microseconds, 100 microseconds, 1 millisecond or 10 milliseconds. The programming considerations are described in the *Operation and Maintenance Instructions for Model 980 Interval Timer*, TI part no. 943001-9701. The characteristics of the module are described in table 6-18. (No external interface is provided.)

Table 6-16. Paper Tape Reader Interface Module Signals and Connector Pin Assignments

Comment	PTR Interface Connector Pin (PCB Top Edge)	Signal
	P2-$\overline{M}$	TRACK 1-
	P2-$\overline{H}$	TRACK 2-
	P2-$\overline{C}$	TRACK 3-
	P2-Y	TRACK 4-
	P2-U	TRACK 5-
	P2-P	TRACK 6-
	P2-K	TRACK 7-
	P2-E	TRACK 8-
TWPR Common		SIGNAL GROUND
	P2-$\overline{F}$	STEP- (VCC)
	P2-$\overline{L}$	DRIVE-
	P2-5	SPROCKET-
	(None)	HIGH SPEED- (Grounded at card reader)

Table 6-17. Paper Tape Reader Interface Module Characteristics and Specifications

Characteristic	Specification
Data Interface	For the following paper tape readers: Models 305, 3075, 6300 and 6375.
Electrical Power Requirements	+5 volts dc at 0.64A
Environmental Specifications	(See table 6-1)

Table 6-18. Interval Timer Characteristics and Specifications

Characteristic	Description or Specification
Oscillator	Crystal-controlled
Selectable time intervals	10 μsec, 100 μsec, 1 msec, or 10 msec
Electrical Power Requirement	+5 ± 0.01 volts dc at 1.33 A
Environmental Specifications	(See table 6-1)

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
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  Tx-yy

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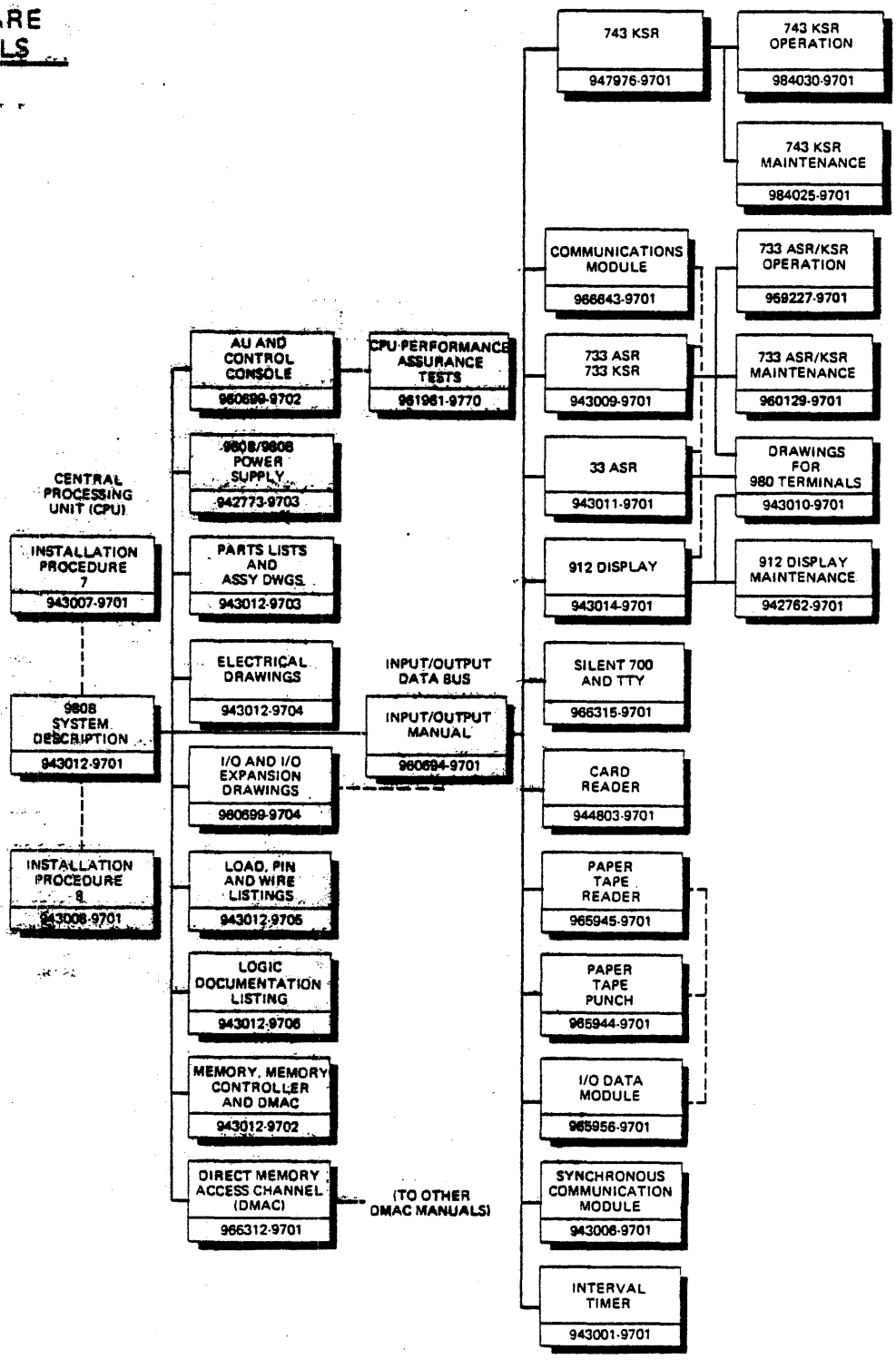

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