product of the currents in diodes whose voltages are negative with respect to that node, the constant of proportionality being the ratio of the product of the saturation currents of the former set of diodes to that of the latter set.

Acknowledgment

During the course of this work, the discussions held with L. Larson of the Advanced Instruments Group and G. Wilson of the Integrated Circuits Group proved stimulating and helpful. The experimental work of E. Traa is also gratefully acknowledged.

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A Precise Four-Quadrant Multiplier with Subnanosecond Response

BARRIE GILBERT, MEMBER, IEEE

***Abstract*—This paper describes a technique for the design of two-signal four-quadrant multipliers, linear on both inputs and useful from dc to an upper frequency very close to the f_t of the transistors comprising the circuit. The precision of the product is shown to be limited primarily by the matching of the transistors, particularly with reference to emitter-junction areas. Expressions are derived for the nonlinearities due to various causes.**

I. Introduction

AN IDEAL FOUR-quadrant multiplier would perfectly satisfy the expression

$$Z = \text{constant}, XY \tag{1}$$

for any values of X and Y, and produce an output having the correct algebraic sign. Ideally, there would be no limitation on the rate of variation of either input.

All practical multipliers suffer from one or more of the following shortcomings.

1) A nonlinear dependence on one or both of the inputs.
2) A limited rate of response.
3) A residual response to one input when the other is zero (imperfect "null-suppression").
4) A scaling constant that varies with temperature and/or supply voltages.
5) An equivalent dc offset on one or both of the inputs;
6) A dc offset on the output.

In the field of high-accuracy medium-speed multipliers, the "quarter-square" technique has gained favor [1]. This method makes use of the relationship

$$XY = \tfrac{1}{4}[(X + Y)^2 - (X - Y)^2] \tag{2}$$

and employs elements having bipolar square-law voltage–current characteristics, together with several operational amplifiers.

Much work has been put into harnessing the excellent exponential voltage–current characteristics of the junction diode for multiplier applications, either by using single diodes (or transistors) in conjunction with operational amplifiers [2], or, more recently, pairs of transistors connected as a differential amplifier [3]–[6]. In the majority of cases, the strong temperature dependence of the diode voltage proved a problem, and at least two commercially available multipliers are equipped with an oven to reduce this dependence.

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The author is with Tektronix, Inc., Beaverton, Ore.

Another problem of the "differential-amplifier" multiplier, analyzed in [7], is the nonlinear response with respect to the base-voltage input. To achieve useful linearity, the dynamic range on this input must be restricted to a very small fraction of the full capability, leading to poor noise performance and worsened temperature dependence, including poor zero stability.

The problems associated with this type of multiplier can be largely overcome, however, by using diodes as current–voltage convertors for the base inputs, thus rendering the circuit entirely current controlled, theoretically linear, and substantially free from temperature effects. This paper is concerned mainly with the determination of the magnitude of the nonlinearities in a practical realization, and the analysis draws heavily on the groundwork laid in [7]; some mathematical expressions will be quoted directly from this paper without proof here.

II. The Basic Circuit

The basic scheme is shown in Fig. 1. It is comprised of two pairs of transistors, $Q2$-$Q3$ and $Q5$-$Q6$, having their collectors cross-connected, driven on the bases by a further pair of transistors, $Q1$-$Q4$, connected as diodes. It is the addition of this pair of diodes that linearizes the circuit. The X signal input is the pair of currents xI_B and $(1-x)I_B$. The Y signal is yI_E and $(1-y)I_E$, where x and y are dimensionless indexes in the range zero to unity.

It was previously shown [7] that the *ratio* of the emitter currents in the $Q2$-$Q3$ and $Q5$-$Q6$ pairs is the same as that in the $Q1$-$Q4$ pair and independent of the magnitudes of I_B and I_E (neglecting second order effects). We can thus write

$$\begin{aligned} I_{C2} &= xyI_E \\ I_{C3} &= (1-x)yI_E \\ I_{C5} &= x(1-y)I_E \\ I_{C6} &= (1-x)(1-y)I_E. \end{aligned} \tag{3}$$

The *differential*[1] output is

$$I_{out} = I_{C2} + I_{C6} - I_{C3} - I_{C5}. \tag{4}$$

Thus, the normalized output Z is

$$\begin{aligned} Z = \frac{I_{out}}{I_E} &= xy + (1-x)(1-y) \\ &\quad - (1-x)y - (1-y)x \\ &= 1 - 2y - 2x + 4xy. \end{aligned} \tag{5}$$

It is seen that the circuit is balanced when x and y are equal to 0.5. If we apply bias currents such that *bipolar* signals X and Y can be used as the inputs, and

[1] The output may also be taken as a single-sided signal from the collectors of $Q2$ and $Q6$, in which case it is $Z = \frac{1}{2}(1 + XY)$.

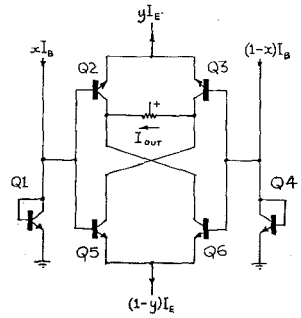

Fig. 1. The basic four-quadrant multiplier.

substitute

$$\begin{aligned} X &= 2x - 1 \\ Y &= 2y - 1 \end{aligned} \tag{6}$$

where X and Y are in the range -1 to $+1$, the output is

$$Z = XY. \tag{7}$$

This is an exact large-signal analysis, and makes no assumptions about temperature. It did, however, assume that the transistors had 1) perfectly matched emitter diodes, 2) perfect exponential characteristics (no ohmic resistance), and 3) infinite betas.

The extent to which departures from this ideal case impair the linearity will now be analyzed.

III. Distortion Due to Area Mismatches

In [7] it was found that "offset voltage"—the voltage required to balance the emitter currents of a pair of transistors in a differential amplifier—could be expressed more conveniently as a ratio of the saturation currents (or areas) of the two emitter junctions. For the four-transistor amplifier "cell" discussed in that paper, the mismatch ratio

$$\gamma = \frac{I_{S2}I_{S4}}{I_{S1}I_{S3}} \tag{8}$$

was defined. It was then shown that for $\gamma \neq 1$ (imperfect matching), the output currents were no longer simply in the same ratio x as the input currents, but had the form

$$a = \frac{\gamma}{1 + x(\gamma - 1)} \cdot x. \tag{9}$$

This can be expressed in a form that shows the nonlinearity due to area mismatches as a separate term D_A

$$a = x + D_A = x + \frac{x(1-x)(1-\gamma)}{1 + x(\gamma - 1)}. \tag{10}$$

For $\gamma \approx 1$, this simplifies to

$$D_A \approx x(1-x)(1-\gamma). \tag{11}$$

This is a parabolic function of x having a peak value $\hat{D}_A$ of $0.25(1-\gamma)$, which leads to the useful rule of thumb

$$\hat{D}_A(\text{percent}) \approx V_0(\text{mV}) \text{ at } 300^\circ\text{K} \tag{12}$$

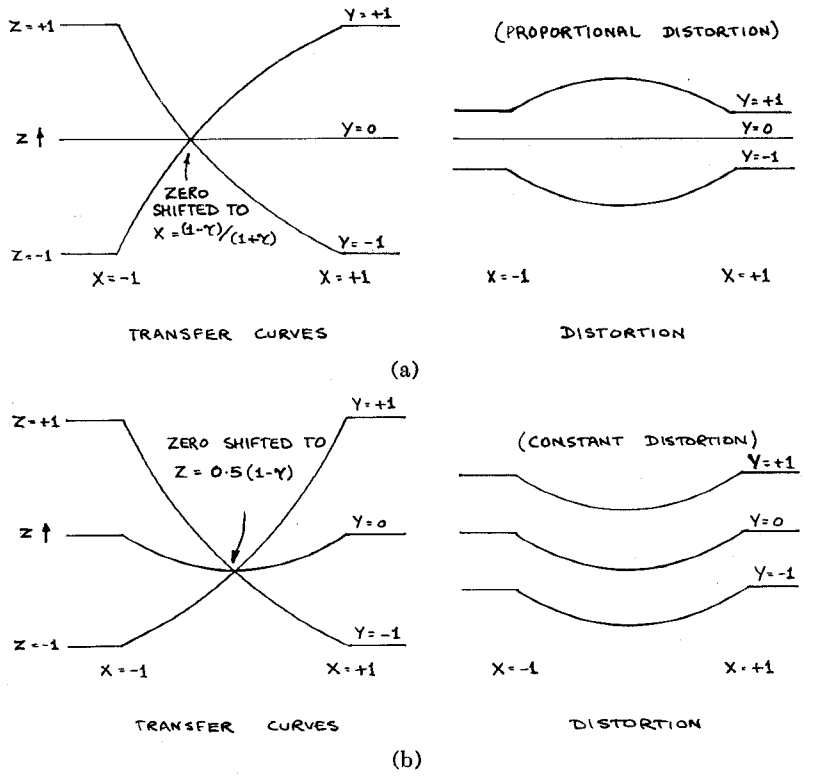

Fig. 2. Distortion introduced by area mismatches (exaggerated). (a) $\gamma_1 = \gamma_2$. (b) $\gamma_1 = 1/\gamma_2$.

where $V_0 = (kT/q) \log \gamma$, the total loop offset voltage. However, notice that $\hat{D}_A$ is not a function of temperature.

In the case of the four-quadrant multiplier, there are two such circuits working in conjunction, so we must define two area ratios

$$\gamma_1 = \frac{I_{S2}I_{S4}}{I_{S1}I_{S3}} \quad \text{and} \quad \gamma_2 = \frac{I_{S5}I_{S4}}{I_{S1}I_{S6}}. \tag{13}$$

The total distortion (with respect to the x-input) will now be a function of y. For example if $Q1$-$Q2$-$Q3$-$Q4$ match perfectly ($\gamma_1 = 1$) but $Q1$-$Q5$-$Q6$-$Q4$ do not ($\gamma_2 \neq 1$), there will be no distortion when $y = 1$, becoming maximal when $y = 0$.

The output can be expressed as

$$Z = XY + 2yD_{A1} - 2(1 - y)D_{A2} \tag{14}$$

where

$$D_{A1} \approx x(1 - x)(1 - \gamma_1)$$

and

$$D_{A2} \approx x(1 - x)(1 - \gamma_2). \tag{15}$$

It will be seen that the linearity of Z with respect to the y input is not affected by area mismatches.

For the purposes of demonstration we can consider the cases where $Q1$ and $Q4$ match perfectly, but

1) $Q2$ and $Q3$ have the same mismatch as $Q5$ and $Q6$, that is $\gamma_1 = \gamma_2$;
2) $Q2$ and $Q3$ have the opposite polarity mismatch of $Q5$ and $Q6$, but the same magnitude, that is $\gamma_1 = 1/\gamma_2$, or $\gamma_1 \approx -\gamma_2$.

In the first case,

$$Z = XY + 2x(1 - x)(1 - \gamma)(2y - 1). \tag{16}$$

When the y input is balanced, $Y = 0$, $y = \frac{1}{2}$. Thus $Z = 0$ for all values of X. Stated differently, the null suppression with respect to the X input is unaffected by this mismatch situation.

The general form of the transfer curves and distortion products for this case is shown in Fig. 2(a), which also shows that the common point of intersection P (where $dZ/dy = 0$) is shifted to $X = (1 - \gamma)/(1 + \gamma)$, $Z = 0$. Notice also that the nonlinearity is always of the same sign as the output slope, and *varies in proportion* to it.

For the second case

$$Z = XY - 2x(1 - x)(1 - \gamma) \tag{17}$$

which corresponds to a constant parabolic distortion component *added* to the signal. In this case, when the Y input is balanced, there is a *residue* on the output of peak amplitude $0.5(1-\gamma)$. The point P is thus at $X = 0$, $Z = -0.5(1-\gamma)$, as shown in Fig. 2(b).

The general co-ordinates of P are

$$P(X, Z) = \left(\frac{1 - \sqrt{\gamma_1\gamma_2}}{1 + \sqrt{\gamma_1\gamma_2}}, \frac{\gamma_2 - \sqrt{\gamma_1\gamma_2}}{\gamma_2 + \sqrt{\gamma_1\gamma_2}}\right). \tag{18}$$

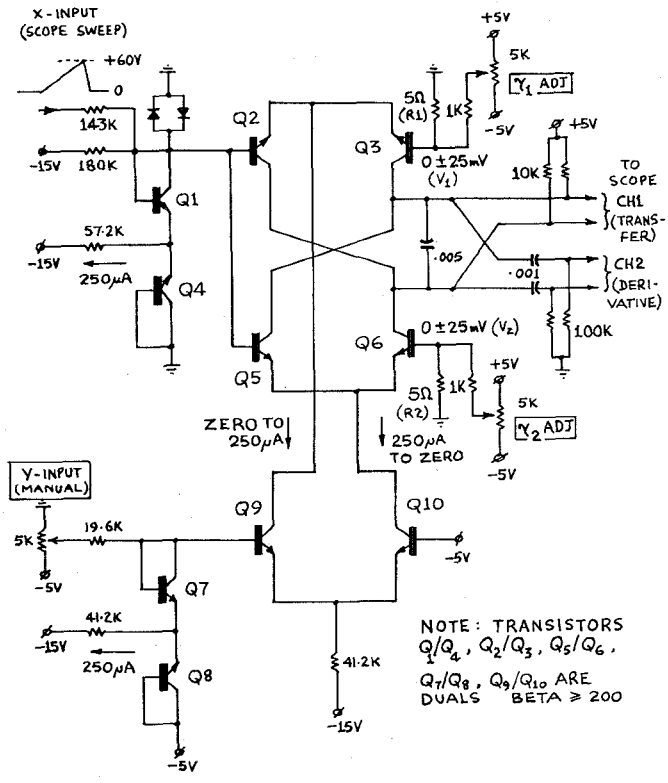

Fig. 3. Experimental circuit for investigation of nonlinear effects.

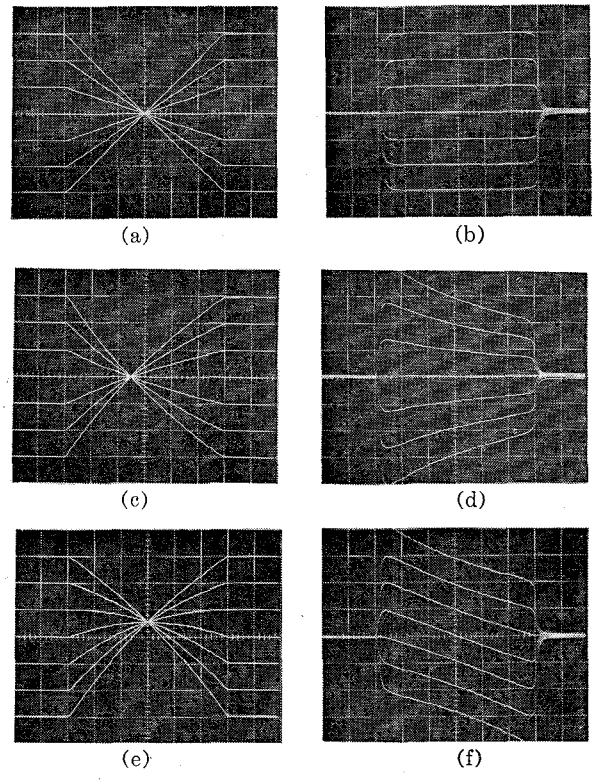

Fig. 4. Demonstration of distortion due to area mismatches. Scales are arbitrary.

Verification

To verify the above theory, and demonstrate the two cases discussed, a circuit was built as shown in Fig. 3. Use was made of the equivalence of area mismatches and offset voltage. The equivalent areas of $Q2$, $Q3$, $Q5$, and $Q6$ could be varied by the bias voltages V_1 and V_2, giving

$$\gamma_1 = e^{qV_1/kT}$$

and (19)

$$\gamma_2 = e^{qV_2/kT}.$$

The devices were operated at low powers ($I_B = I_E =$ 250 μA, $V_C = 2.5$ volts) so that the junction temperatures were close to 300 °K. The use of low operating currents also eliminated the distortion due to ohmic resistances, discussed later.

To demonstrate the nonlinearity more clearly, a linear ramp was used as the X input, and a simple R–C differentiator produced a waveform corresponding to the incremental slope of the transfer function. This technique provides a very convenient sensitive measurement of distortion, and became a valuable tool during the investigation of improved multiplier designs, without which it would have been necessary to resort to tedious point-by-point DVM measurements to reveal the nonlinearities.

Fig. 4(a) shows the transfer curves with V_1 and V_2 adjusted for minimum distortion, and Fig. 4(b) are the derivatives. Seven static values of Y, from -1 to $+1$, are shown. These demonstrate the excellent linearity that can be achieved with well-matched transistors. The departure from constant slope is within $+0$ -1 percent over 75 percent of the dynamic range. In terms of the nonlinearity term D_A (which is a measure of the deviation from the ideal line), this amounts to less than 0.3 percent at any point.

With $V_1 = V_2 = -10$ mV, ($\gamma_1 = \gamma_2 = 1.47$) the theoretical point of intersection is shifted to $X = -0.19$. The actual point is at -0.18, as shown in Fig. 4(c). Notice that the slope [Fig. 4(d)] falls as X varies from -1 to $+1$, starting 30-percent high and finishing 30-percent low. The deviation from the ideal line is now about 8 percent; of course, an offset voltage this large would be exceptional.

With $V_1 = +10$ mV, $V_2 = -10$ mV ($\gamma_1 = 1.47$, $\gamma_2 = 0.68$) the theoretical value of Z at $X = 0.0$ should be -0.197. This is close to the value of -0.185 measured from the waveforms of Fig. 4(e). An interesting feature of the derivatives shown in Fig. 4(f) is the one for $Y = 0$. Its linear form confirms the parabolic shape of the distortion term.

IV. Distortion Due to Ohmic Resistances

Fig. 5 shows the circuit with the addition of linear resistances in the emitters of all the transistors. These represent all the bulk resistances of the diffusions, particularly the base resistance, referred to the emitter circuit. In fact, these elements will be current dependent, due both to crowding effects and beta nonlinearities. However, if the device geometry is such that the cur-

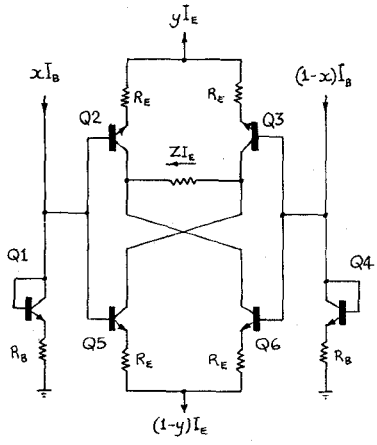

Fig. 5. Circuit having ohmic emitter resistances.

rent-density distribution is equalized in the appropriate sets of devices, the current dependence can be neglected.

Using the variables shown in Fig. 5, the loop equation for the quad $Q1$-$Q2$-$Q3$-$Q4$ under these conditions becomes

$$\frac{kT}{q}\log\left[\frac{x(1-a)}{a(1-x)}\right] = I_BR_B(1-2x) - yI_ER_E(1-2a) \quad (20)$$

which has no explicit solution for a in terms of the other variables. However, guessing that the distortion will be small, we will make the substitutions

$$a = x + D_R \quad (21)$$

and

$$\log(1-D_R) \approx -D_R$$

where D_R is the fractional distortion due to resistances. Equation (20) simplifies to

$$\frac{kT}{q}\frac{D_R}{(x+D_R)(1-x)} = yI_ER_E(1-2x-2D_R) - I_BR_B(1-2x). \quad (22)$$

Solving for the distortion term, and changing input variable from x to X,

$$D_R = \frac{q}{kT}(y\phi_E - \phi_B)\,\Delta(X) \quad (23)$$

where

$$\phi_E = I_ER_E$$

and

$$\phi_B = I_BR_B, \quad (24)$$

these representing the extra voltages in the emitter and base circuits due to resistances, and

$$\Delta(X) = \tfrac{1}{4}X(X^2-1) \quad (25)$$

which describes the form of the distortion, and has peak values of ± 0.096 at $X = \pm 0.577$, and zeros at $X \pm 1$ and 0.

Equation (23) makes the reasonable assumption that ϕ_E and ϕ_B are small compared to kT/q. For example, assume $R_E = 1$ ohm and $I_E = 2.5$ mA, giving $\phi_E = 2.5$ mV, about 10 percent of kT/q at 300°K.

Using the above approximate analysis, we can state a rule of thumb for the peak magnitude of D_R, for the quad $Q1$-$Q2$-$Q3$-$Q4$:

$$\hat{D}_{R1} \approx \pm 0.37(y\phi_E - \phi_B) \quad (26)$$

for ϕ_E, ϕ_B in millivolts, at 300°K, and $\hat{D}_{R1}$ in percent. Similarly, for the $Q1$-$Q5$-$Q6$-$Q4$ circuit, we have

$$\hat{D}_{R2} \approx \pm 0.37\,\{(1-y)\,\phi_E - \phi_B\}. \quad (27)$$

The *net* nonlinearity will come from both circuits, and vary with the y input. The outputs of each quad (and hence the distortion terms) are also weighted by y and connected out of phase. Thus

$$\begin{aligned}\hat{D}_R &= \hat{D}_{R2} - \hat{D}_{R1}\\ &= \pm 0.37[\{y\phi_E - \phi_B\}y - \{(1-y)\phi_E - \phi_B\}(1-y)]\\ &= \pm 0.37(\phi_E - \phi_B)Y \quad \text{(percent)}, \end{aligned} \quad (28)$$

with the substitution of $Y = 2y-1$. The nonlinearities introduced by *balanced* emitter resistances can be summarized as follows.

1) The distortion with respect to the X input has a symmetrical form and is a fixed percentage of the output Z.
2) There is no distortion with respect to the Y input.
3) The common point of intersection of the transfer curves is always at $X = Y = Z = 0$.
4) No distortion arises when $\phi_E = \phi_B$.

Thus, quite large ohmic resistances can be tolerated (that is, it is possible to use devices with high base resistance and/or low beta), provided that the base and emitter voltage terms are balanced. By scaling the device geometrics in the ratio I_E/I_B, the closeness with which $\phi_E = \phi_B$ is then a matter of device matching.

In practice the resistors labeled R_B in Fig. 5 will not be equal. It can be shown that under these conditions there will be a residue in the multiplier output for $Y = 0$, having the S-shaped form described by (25), and having a peak amplitude (at 300°K) of

$$\hat{D}_R \approx \pm 0.05\,I_E(R_{E2} + R_{E3} - R_{E5} - R_{E6}) \quad (29)$$

where $\hat{D}_R$ is in percent, I_E in milliamperes, R_E in ohms. Notice that this residue term is independent of ϕ_B, a fact that has been experimentally confirmed. It will be apparent that linear emitter resistances reduce the output swing capability because in the limit (when the diode voltages are small compared to the "ohmic" voltages) the circuit becomes completely cancelling for all values of X or Y. Also, the case where these resistances are unbalanced will give rise to an equivalent offset on one or both of the inputs.

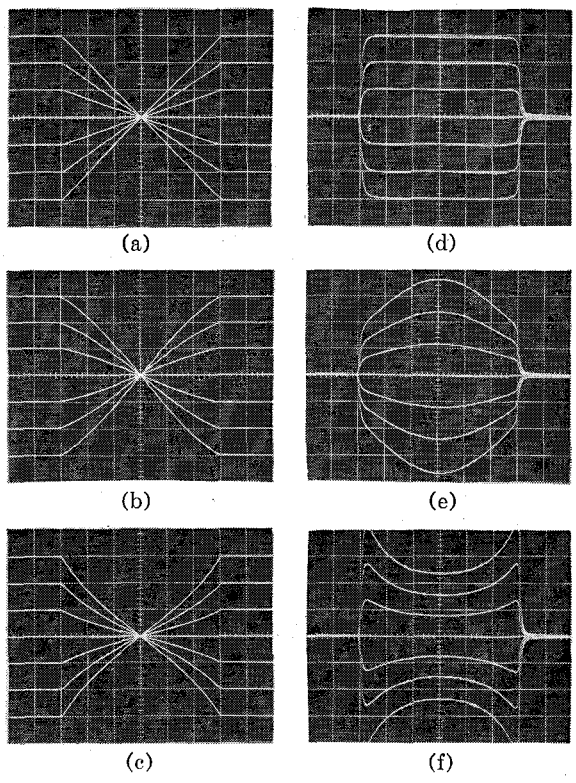

Fig. 6. Demonstration of distortion due to ohmic resistances.

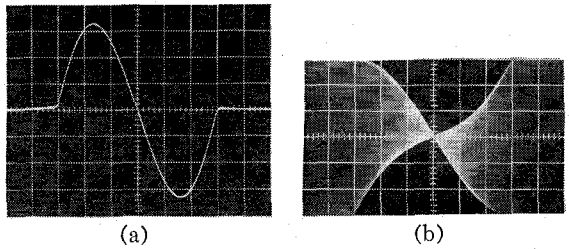

Fig. 7. Characteristic distortion due to mismatched resistances. (a) Vertical scale expanded to 0.33 percent/div. (b) 3.3 percent/div.

Verification

Using the test circuit of Fig. 3, to which emitter resistors were added, these nonlinearities were demonstrated. In Fig. 6(a), all resistors were 50 ohms and $I_B = I_E = 250$ μA; thus $\phi_E = \phi_B = 12.5$ mV. The derivative waveform, shown in Fig. 6(b), shows little degradation of linearity over the full dynamic range.

By omitting the resistors in the $Q2$-$Q3$ and $Q5$-$Q6$ emitters, a net error of $\phi_B = 12.5$ mV remains. Equation (28) predicts a nonlinear term of ± 4.5 percent at $Y = \pm 1$. The measured value is ± 3.3 percent. (Due to the approximations, (28) will err on the high side when ϕ_B or ϕ_E become comparable with kT/q). See Figs. 6(c) and (d). By omitting the resistors in the $Q1$-$Q4$ emitters, the distortion is of the opposite polarity, as Figs. 6(e) and (f) demonstrate.

The most typical distortion is due to the case where the ohmic voltages do not match, due probably to mismatches in r_b and beta. This can be demonstrated, too, by inserting the 50-ohm resistors in just the $Q2$-$Q3$ pair, when (29) predicts a peak distortion of ± 1.25 percent of full scale with the Y input balanced. The measured nonlinearity is shown in Fig. 7(a), in which the display was expanded vertically 50 times and the distortion has peak values of ± 1.1 percent. Fig. 7(b) gives the appearance of the distortion when the Y input was modulated to a depth of about 20 percent.

V. Distortion Due to Beta

The final imperfection to consider is that of finite beta. Three cases can be considered:

1) the transistors have identical, constant beta;
2) the transistors have differing, but still constant, beta;
3) the transistors have identical, current-dependent beta.

The first case was dealt with in [7] where it was shown that the only error is that the output current is reduced by the factor alpha (for I_E less than βI_B). In the version of the circuit driven by a single-sided input current (as, for example, the test configuration shown in Fig. 3), a small offset term also arises, and the dc output for $Y = 0$ is approximately

$$Z(X, 0) = (1 - \bar{\alpha}) \frac{I_E}{I_B} \tag{30}$$

where $\bar{\alpha}$ is the large-signal common-base current gain.

The second and third cases have not been completely analyzed, and it is doubtful whether explicit expressions involving all the betas and their nonlinearities would be of any value. Clearly, there is now the possibility for distortion terms to arise. However, the variations in beta from device to device, and over a small current range, are usually sufficiently small that no serious distortion should arise using typical transistors with betas in the neighborhood of 100.

VI. Thermal Distortion

The topic of thermal distortion in this category of circuits was dealt with in [7], where it was shown that theoretically no distortion arises due to the differential heating of devices if the power dissipation in the inner and outer pair are equal. This can usually be arranged, and, if necessary, the circuit can operate with I_E less than I_B.

In practice, using monolithic circuits the thermal distortion in response to a step input is very much less than 1 percent of the output amplitude, and persists for no more than a few microseconds.

VII. Transient Response

Because of the very small voltage swings at the inputs, and the cross connection of the transistors, the aberrations due to capacitances are very small, especially when properly balanced inputs are used. The main speed limitation is the f_t of the transistors.

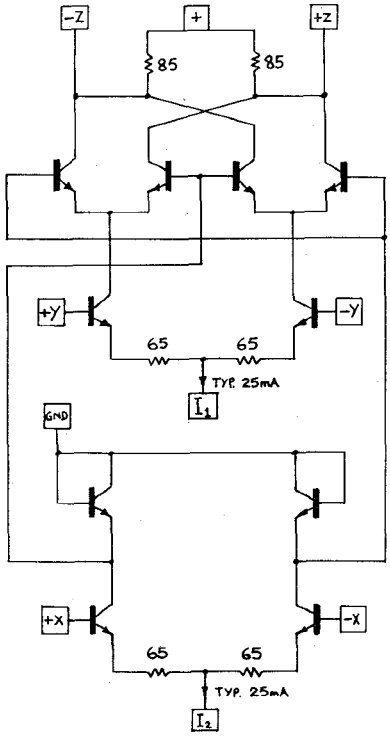

Fig. 8. Circuit used to examine high-frequency behavior.

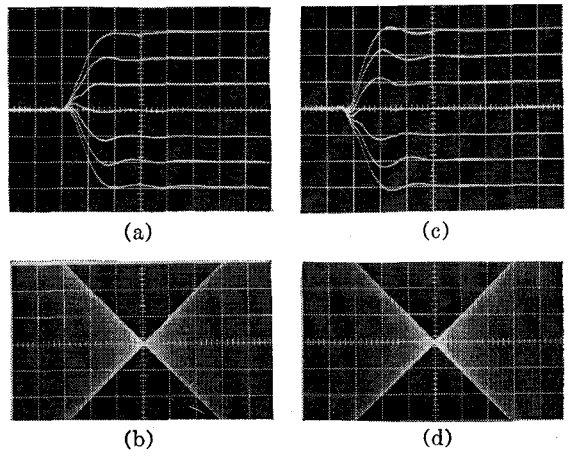

Fig. 9. Performance of integrated version of Figs. 8. (a) and (b). Transient response on X and Y inputs, respectively, at 1 ns/div. using dc control on other input. (c) and (d) 200-MHz carrier on X and Y inputs, respectively, staircase voltage on other input. Peak swing is 90 percent of full scale in all cases.

At $Y = \pm 1$, one of the transistor pairs $Q2$-$Q3$ or $Q5$-$Q6$ is producing all the output. The 3-dB bandwidth is, thus, about $f_t I_E/I_B$. At $Y = 0$, each pair receives $I_E/2$, and the bandwidth is doubled. We would, therefore, expect a risetime variation in response to a step on the X input of about two to one between these extremes. The step response to the Y input should be fairly independent of the X amplitude.

Measurements on an early integrated multiplier were made to examine the high-frequency behavior. The circuit, shown in Fig. 8, uses an "inverted" pair of input diodes [7], which are conveniently driven from pairs of emitter-degenerated stages for the X and Y inputs.

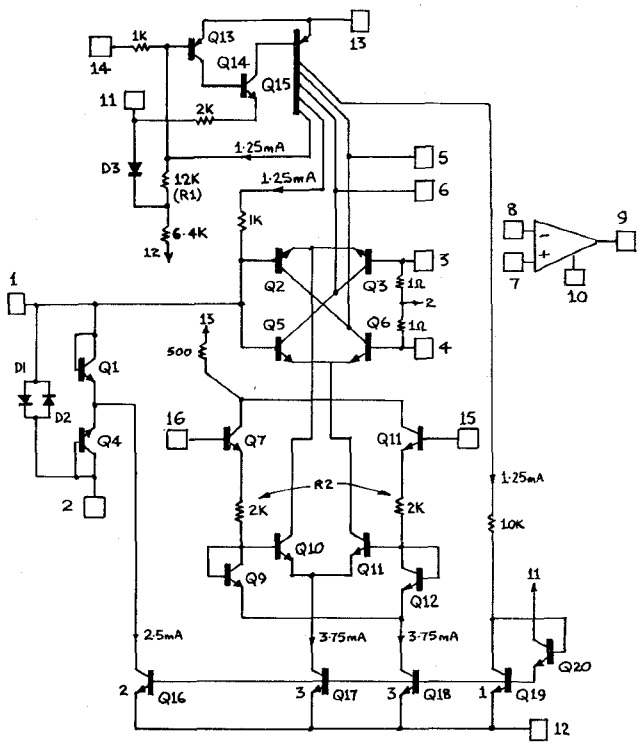

Fig. 10. Complete monolithic multiplier.

Transient response for each input is shown in Fig. 9(a) and (b). Figs. 9(c) and (d) show the CW response for a 200-MHz input, with the other input driven by the staircase output of the sampling time base in the oscilloscope used to examine the responses. The null suppression was better than 20 dB at 500 MHz.

VIII. A. Complete Monolithic Multiplier

Fig. 10 is the circuit of a complete multiplier suitable for integration. It is designed so as to be usable with a minimum of additional components to achieve medium-accuracy operation, or with extra components to perform at a higher accuracy. Wide-band operation (dc to >100 MHz) is available, or more versatility can be obtained by using the built-in operational amplifier to give division, squaring and square-rooting modes. These variations are possible by pin changes only. The X input is a single-sided current I_x into a summing point at ground potential, in the range 0 ±1 mA. The y input is a differential voltage V_Y into a high impedance (approx. 400 kΩ) in the range 0 ±5 volts. It can be shown that the output from pin 6 is

$$I_Z = \frac{I_x V_y}{5} \tag{31}$$

the scale factor being determined by the +15-volt supply and the ratio of R_1 to R_2. The diode D_3 ensures temperature stable scaling, and also makes the scaling factor proportional to the positive supply over a limited range.

Input and output current balance, and the rest of the circuit currents, are determined by the five-collector

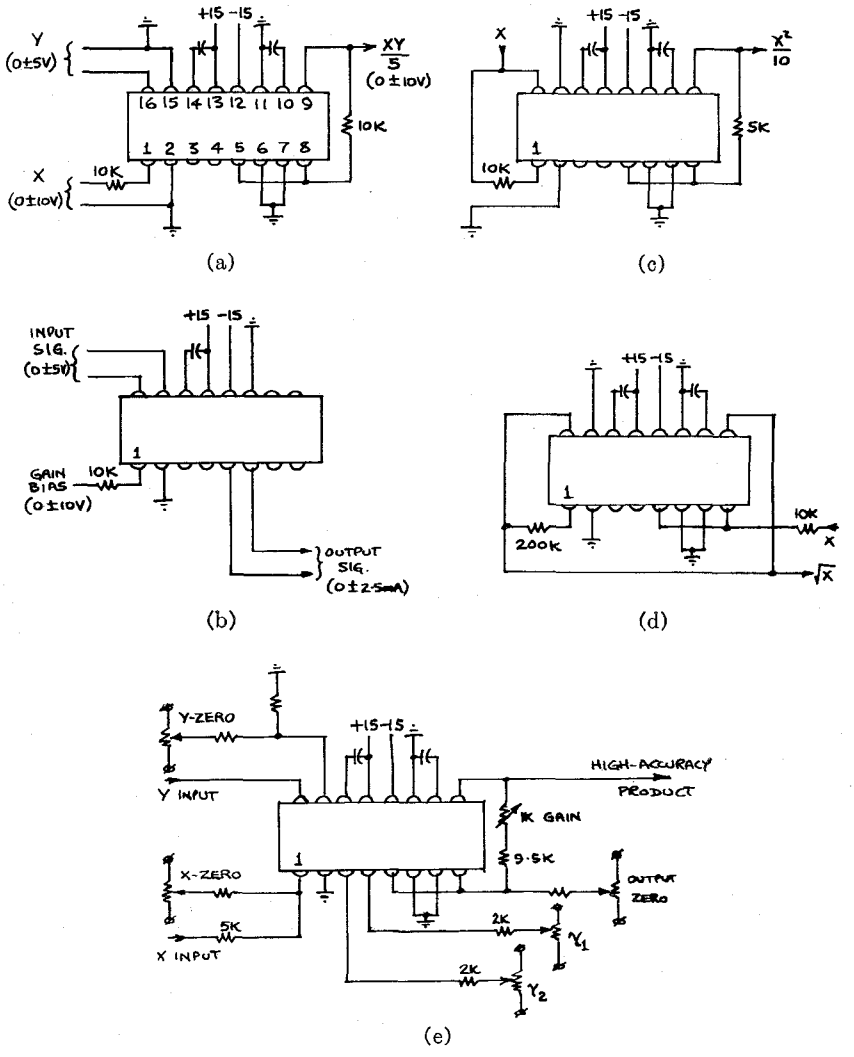

Fig. 11. Circuit of Fig. 9 connected as (a) medium-accuracy multiplier, (b) wide-band gain and polarity control, (c) squarer, (d) square-rooter, and (e) fully corrected multiplier.

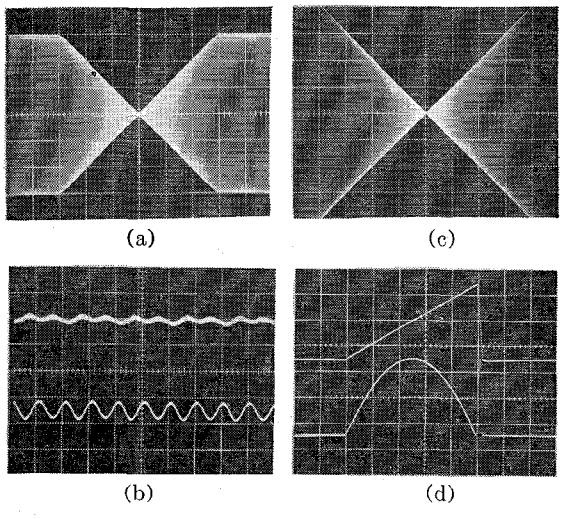

Fig. 12. Typical performance. (a) As balanced modulator, carrier frequency 5 MHz, peak output swing is 90 percent of full scale. (b) Output expanded ten times in vertical and horizontal axes—vertical now 1.67 percent of full scale/div. (c) Null suppression for full-scale 5-MHz carrier on X (upper trace) and Y (lower trace), expanded to 0.1 percent/div. (d) Offset ramp applied to both inputs produces the parabolic output, 1 μs/div.

lateral p-n-p, $Q15$. The matching of the currents to the five collectors (base diffusions) is vital to balanced operation. Measurements indicate that matching errors considerably less than ± 2 percent can be achieved. Notice that one of the collectors is connected in an operational configuration, through $Q13$ and $Q14$. This loop has to be stabilized by an external capacitor connected between pins 13 and 14. The second collector supplies a nominal 1.25 mA to balance the X input; collectors 3 and 4 supply the output balance currents; collector 5 sets up the current tails for the multiplier via $Q16$ through $Q20$.

Pins 3 and 4 give access to the bases of $Q3$ and $Q6$, allowing linearity-connection voltages to be applied. For perfect connection, these voltages should be proportional to absolute temperature. The aluminum 1-ohm resistors come close to this ideal, having a temperature coefficient of 0.38 percent per °K, slightly greater than the coefficient of kT/q at 300°K.

The operational amplifier increases the versatility of the device by permitting several modes to be imple-

mented. Pin 7 is normally grounded, and the inverted output from the multiplier, pin 5, is connected to pin 8; pin 6 is also grounded. Hence, the multiplier block $Q2$, $Q3$, $Q5$, $Q6$ works with a collector-base voltage of 0 $\pm$100 mV (the base voltage swing). The overload diodes, $D1$ and $D2$, must, therefore, be Schottky-barrier diodes having negligible conduction for most of the working voltage range at the X-input summing point, but being able to conduct heavily before the collector diodes of $Q2$ and $Q5$ under overload conditions. These may now be fabricated along with the standard silicon circuitry.

Fig. 11(a) through (e) illustrate the versatility of the circuit. The waveforms in Fig. 12 show linearity and null suppression at 5 MHz, and the output in the squaring configuration.

IX. Summary

A technique has been described that overcomes the inherent temperature dependence and nonlinearity of a transistor four-quadrant multiplier, and the feasibility of producing a complete monolithic multiplier with a worst-case linearity error of the order of 1 percent on either input has been demonstrated. Better linearity is possible by adjustment of transistor offset voltages. Bandwidths of over 500 MHz have been measured.

Acknowledgment

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Applications of a Monolithic Analog Multiplier

ALBERTO BILOTTI, SENIOR MEMBER, IEEE

***Abstract*—A fully balanced analog multiplier using differential transistor pairs is briefly described. Several circuit functions usually required in communication systems can be derived from the basic circuit. In particular, the different modes of operation leading to FM detection, suppressed carrier modulation, synchronous AM detection, and TV chroma demodulation are discussed. Experimental data obtained with a monolithic analog multiplier are also presented.**

I. Introduction

MANY CIRCUIT functions required in communication systems can be derived by way of analog multiplication. Fig. 1 shows a functional block consisting of an analog multiplier, symmetrical input limiters, and an optional output low-pass filter. When properly combined with passive networks, this block can perform FM detection, phase comparison, synchronous AM detection, amplitude modulation, and other functions based on frequency translation. This paper considers an integrated circuit that can be represented by the block diagram in Fig. 1.

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The author was with Sprague Electric Company, North Adams, Mass. He is now with the Faculty of Engineering, University of Buenos Aires, Buenos Aires, Argentina.

II. Basic Circuit

Fig. 2 shows the fully balanced arrangement of the three differential transistor pairs Q_1, Q_2, and Q_3 forming an analog multiplier block. The essential features of this circuit have been discussed elsewhere [1], [2] and the objective here is to achieve an understanding of the modes of operation possible, and through these modes, to consider a number of possible system applications [3]. Assume for a moment low-level driving at the inputs of V_1 and V_2. The current I_b established in the current source transistor is split in proportion to the applied voltage in transistor pair Q_1. This current division determines the bias and, therefore, the gain of the pairs Q_2 and Q_3. The output collector current summed in the load resistor R is proportional to the product of the two applied signals V_1 and V_2. The circuit topology is such that if $V_1 = 0$, the output currents due to a signal V_2 are of equal magnitude and opposite instantaneous polarity, giving a zero net output. The same is true for an applied