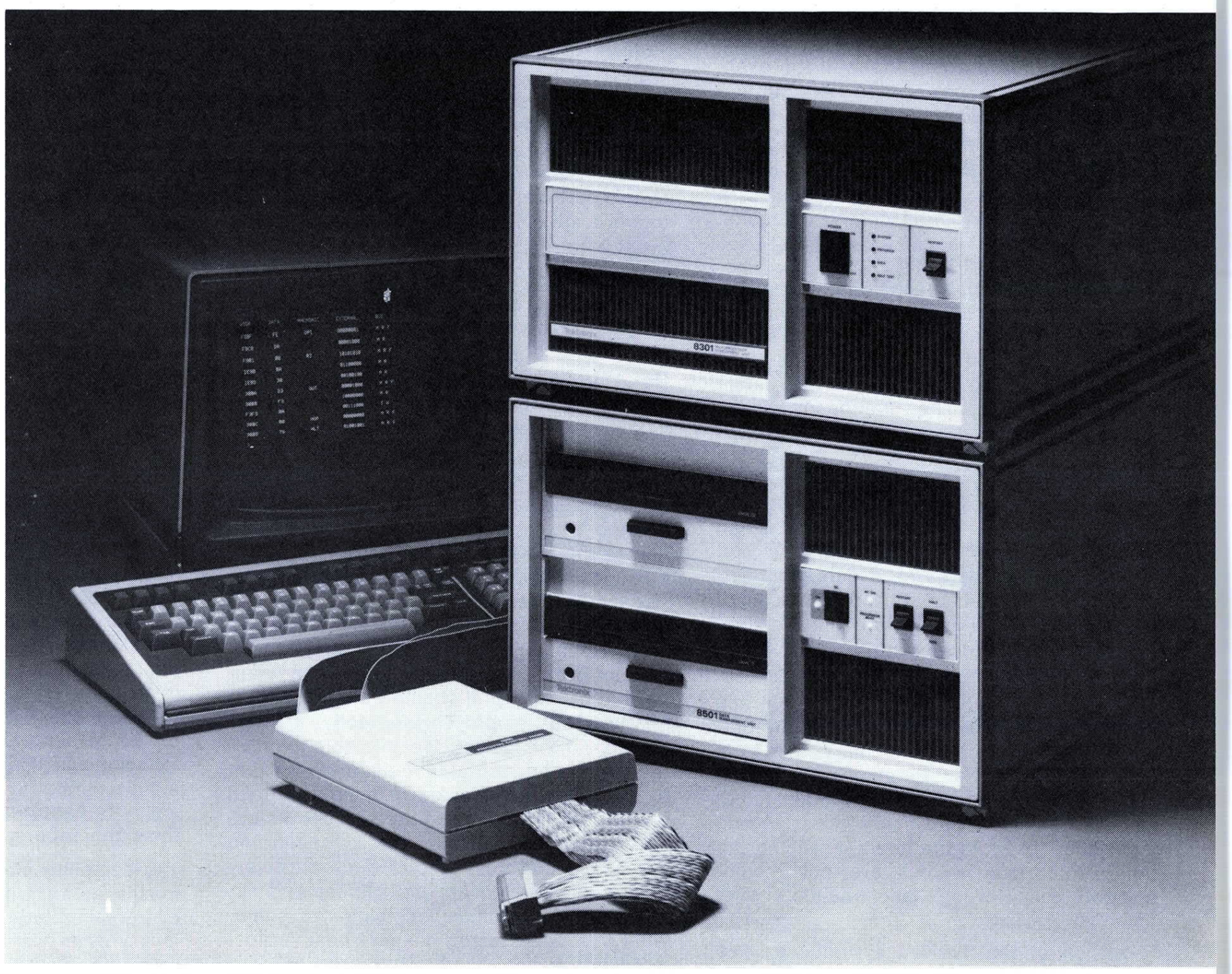
Full In-Circuit Emulation for F8, 3870, 3872, 8080A, TMS900
8800, Z80A, 1802, 8085A, 6802 Real-Time Prototype Analyze
Line Printer **Microcomputer Development Labs** Text Edito
Modular Development Language Debugging Software Lin
Display Terminal Macro Relocatable Assemblers Full In-Ci



MDL Now Supports

8088	6802
8086	6803
8085A	6808
8080A	F8
8048	3870
8049	3872
8035	3874
8039	3876
8039-6	Z-80A
8021	Z8000
8022	TMS9900
8041A	SBP9900
68000	1802
6800	6500/1
6801	

. . . with more to come

Tektronix Microcomputer Development Labs offer the broadest range of quality multiple microprocessor support available today. Tektronix won't lock you into one microprocessor family or vendor. Plus, every Tektronix MDL is backed with over 30 years of design experience. We test our Development Labs thoroughly to ensure performance and reliability. Each one provides complete development capability and the Tektronix committment that guarantees you'll keep abreast of the fast paced microprocessor technology.

Call your local specialist today to find out more about the new Tektronix 8550 MDL. Tektronix can also offer you high level language support with our Modular Development Language MDL/μ.

8001

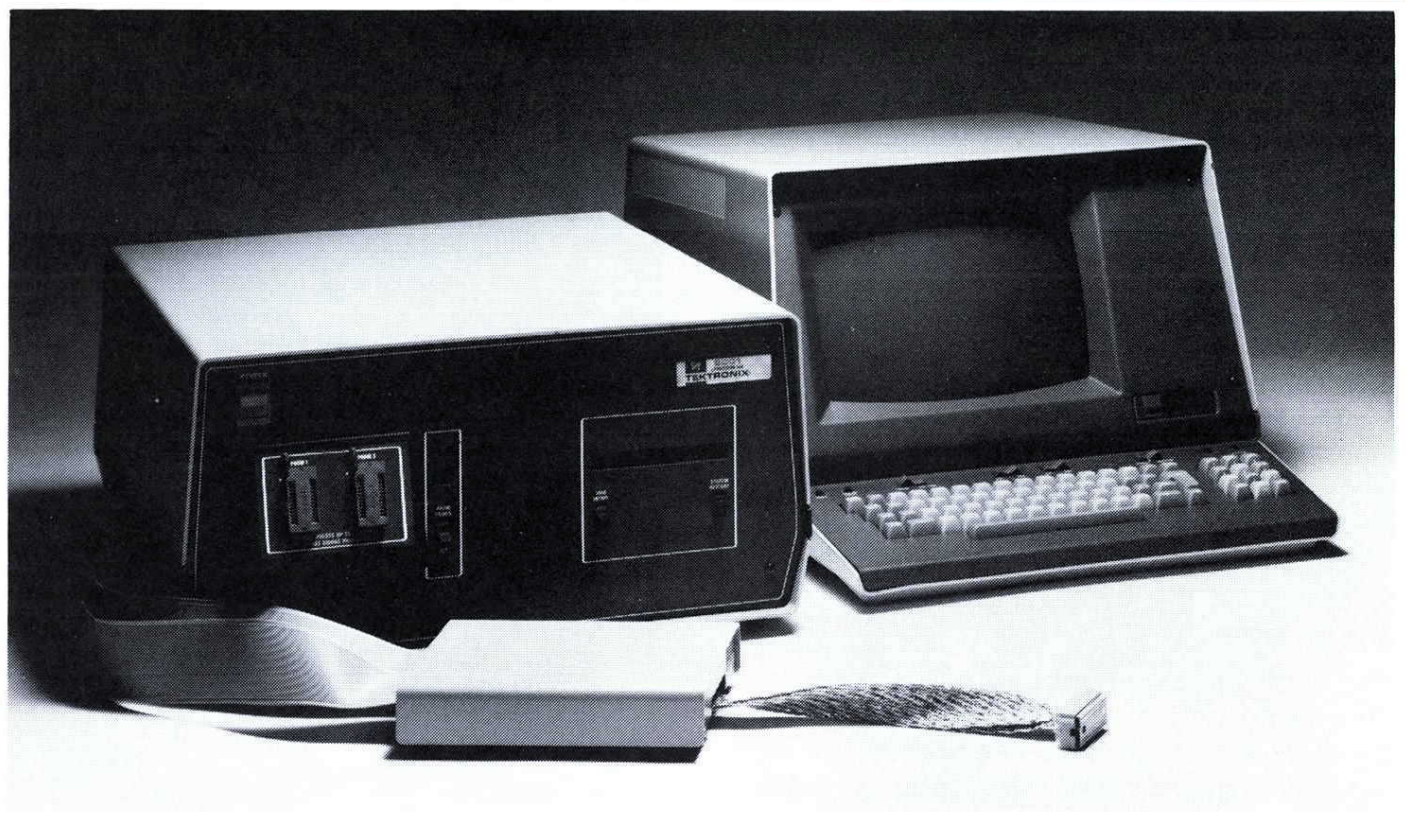
Multiple Microprocessor Support

In-Circuit Emulation

Real-Time Prototype Analysis

The 8001 Microprocessor Lab is a total hardware debugging system for the design of microprocessor-based products. A key feature is its ability to support many microprocessor chips, including the 8086, 8041A, 8022, 8085A, 8080A, 8048, 8049, 8039, 8039-6, 8035 and 8021, 6800 and 6802, TMS9900, Z-80A, and Z8000, F8, 1802 and the 3870 and 3872, 3874, 3876 and 6500/1.

In addition to multiple microprocessor support, the 8001 offers three emulation modes for software debugging, partial and full emulation, as well as a real-time prototype analyzer option offering all the capabilities of a microprocessor analyzer with eight channels of external input.



The 8001 Microprocessor Lab consists of the 8001 Mainframe with 16K of Program Memory. Microprocessor Support Packages for microprocessors are optional. A Microprocessor Support Package includes an emulator ROM, an emulator processor, and a prototype control probe. The 4024/4025 Computer Display Terminals, or the LP8200 Line Printer are recommended optional peripherals.

Three Emulation Modes

In a typical design sequence, software is first developed independently using timesharing, a minicomputer, another development system, or some other means. It is then downloaded to the 8001 using the Tektronix Hexadecimal File Format to insure accurate transfer of the program. At this point the in-prototype emulation and software/hardware integration capabilities of the 8001 come into play.

After the developed software is downloaded to the 8001, the resulting object code may be executed in system emulation mode 0 on the optional emulator processor. The emulator processor is identical to the microprocessor that will finally be installed in the user's prototype. Execution is performed under control of the debug system; during execution, program steps can be traced, software breakpoints can be set, and memory can be examined and changed as required. Should an error be discovered, that portion of the program can be corrected at the source level using the editing, assembling and linking feature of the host computer. This continues until the program is correct.

Partial emulation mode 1 lets the user release control in methodical steps from the 8001 to the prototype. The developmental software runs using 8001 memory space, and the prototype's I/O and clock. The 8001 memory mapping feature allows memory to be gradually mapped over to the prototype in address blocks as small as 128 bytes. Throughout partial emulation, the user has access to prototype circuitry via the powerful 8001 debugging system, which enables him to trace, set breakpoints, examine and change memory and register contents.

Full emulation mode 2 lets the user exercise the program on the prototype while still maintaining complete control through the Microprocessor Lab. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively free-standing, the user may still direct program activity through the prototype control probe.

PROM Programmer

The 1702 and 2704/2708 PROM Programmer, Options 47 and 48 for the 8002A and 8001 Microprocessor Labs, provide the ability to program either 1702 or 2704/2708 erasable PROM chips. When the module is installed in an 8002A or 8001 Mainframe, the PROM Programmer software enables communication between 8002A or 8001 program memory and the PROM installed in the front-panel PROM programming porch.

1702 or 2704/2708 PROM Programmer software transfers one data byte at a time, and actual addresses are assigned. Data may be written from 8002A or 8001 program memory (WPROM); read from PROM into program memory (RPROM); or compared on the system terminal (CPROM).

The RPROM command allows the programmed PROM to be read into program memory and dumped to the system console. The CPROM compare function performs an address-by-address comparison between the PROM and the program under development. When an inequality between PROM bytes and memory bytes occurs, the memory address, memory byte content, and PROM byte content are displayed on the system console. A successful comparison between designated PROM and memory bytes is indicated by an End of Job message on the console.

8001 CHARACTERISTICS

The 8001 Microprocessor Lab is a modular system whose mainframe houses up to 20 plug-in circuit boards. Emulator processor modules for the microprocessor of choice, its associated prototype control probe, and a ROM-based software module are optional. A terminal is necessary for system operation, and may be ordered as an optional peripheral.

The Real-Time Prototype Analyzer module, additional 16K byte Program Memory modules, and PROM Programmer modules for the 1702 or 2704/2708 are available as system options.

In addition to the standard system console I/O port, the 8001 provides a system communication module with three RS-232-C compatible ports for use with such peripherals as paper tape reader/punchers, line printers (LP8200), printing terminals, modems and other peripherals. One port is designated a general purpose RS-232-C compatible input/output port with independent input and output baud rate selection. Another port is an RS-232-C compatible output only port for use with line printers. The third port is a modem compatible port for use with half duplex modems. All ports have strap selectable baud rates of 110, 300, 600, 1200, or 2400.

8001 PHYSICAL CHARACTERISTICS

Dimensions	in	cm
Height	9.6	24.7
Width	18.8	48.3
Length	22.3	57.3
Weight	**lb**	**kg**
Net	66	30

8001 ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	0°C to +35°C (+32°F to 95°F).
Humidity	To 90° relative noncondensing.
Altitude	
Operating	To 15,000 feet max.

8001 ELECTRICAL CHARACTERISTICS

Ac Input Voltages	115 V ac ±10% or 230 V ac ±10%.
Frequency Range	60 Hz (50 Hz special order)

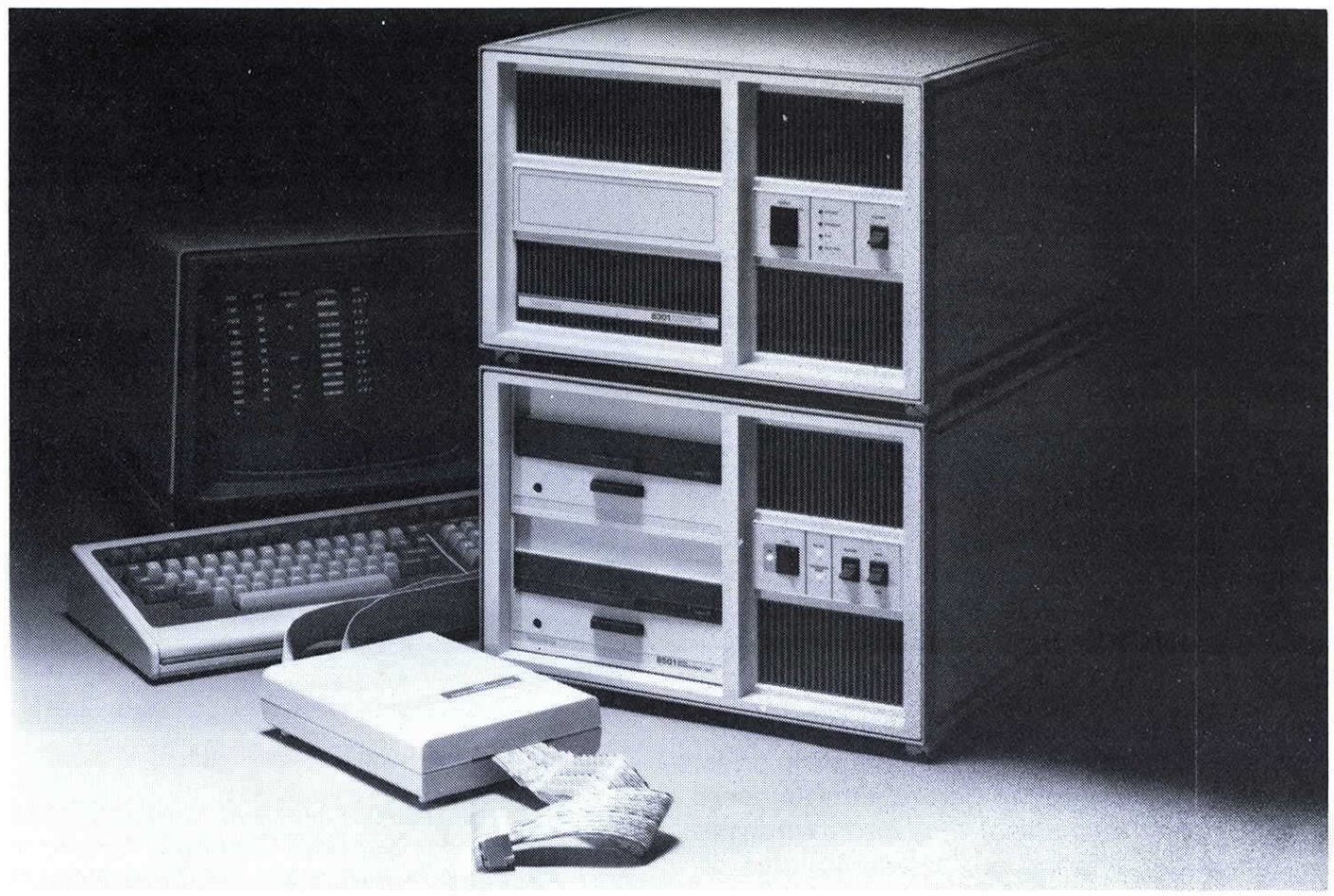
Microcomputer Development Lab System

8550

Multiple Microprocessor Support

In-Circuit Emulation

Real-Time Prototype Analysis



The Tektronix 8550 Microcomputer Development Lab is a versatile software development and hardware/software integration system for microcomputer-based product design. The system supports many 8- and 16-bit microprocessors, allowing the user to configure the 8550 for a wide variety of design types.

The 8550 Development Lab offers resources for editing facilities to support both assembly-level and high-level languages, as well as linking capabilities. The optional advanced CRT-oriented editor eases the task of program entry and editing. With the appropriate assembler and emulator options for the target microprocessor, the user can execute software in the 8550 for full program debugging.

The Lab also offers complete in-circuit emulation and hardware testing capabilities. With the appropriate prototype control probe for the target microprocessor, the user can transfer control from the 8550 to the prototype block by block, dedugging at every stage. The real-time prototype analyzer option provides an invaluable tool for verifying and correcting execution of the program in real time.

The basic 8550 system consists of two major components, the 8301 Microprocessor Development Unit and 8501 Data Management Unit. The Microprocessor Development Unit houses the operating system software, D0S/50; 32K bytes of program memory; language processor; emulator controller; and hardware options such as emulator processors and prototype control probes for selected microprocessors, an additional 32K of static RAM, the real-time prototype analyzer, and the PROM programmer. Optional system software includes assemblers for all supported microprocessors, Pascal and MDL/u compilers for several supported microprocessors, and the advanced CRT-oriented editor.

The Data Management Unit handles files and auxiliary I/O for DOS/50 and manages the movement of user files between its dual-sided, double-density flexible discs and the Microprocessor Development Unit. Disc memory capacity is 2 megabytes.

Multiple Microprocessor Support

A key feature of the 8550 is its ability to support many microprocessor chips, including the 8086, 8085A, 8080A, 8048, 8049, 8035, 8039, 8039-6, 8021, 8041A, 8022, 6800, 6802, 6808, F8, 3870, 3872, 3874, 3876, Z8000, Z80A, TMS9900, 1802 and 6500/1.

Program Development

Under the supervision of the operating system software, the Microcomputer Development Lab aids the designer in all phases of program development and debugging.

D0S/50 supervises the following tasks:

- General input and output.
- File creation and maintenance.
- Program assembly and compilation.
- Program execution, monitoring, and debugging.

Program entry and editing is accomplished via the standard line-oriented editor or the optional advanced screen-oriented editor, which allows both line-and screen-oriented editing.

Data management is simplified through a tree-like structure format, which allows the user to specify one main system directory, one root directory for each disc, and any number of sub-directories under the root directory. Data files may be created and entered directly into the root directory. As files are accumulated, the user may organize them into specific groups, each under its own specific directory. This allows the user to create directories within directories to any level of nesting needed.

The assembler processor, with the appropriate disc inserted in the flexible disc drive, performs program assembly functions for each microprocessor supported by the 8550.

The powerful macro capability allows the designer to access frequently used sets of code by referencing the macro by name. The linker, working with the relocating features of the Assembler, links and locates multiple code segments into a complete executable program. Additionally, the conditional assembler capability of the 8550 allows the designer to customize the final program by testing conditions to determine which of certain code segments are to be assembled into the final program. Code management is further enhanced by the Assembler's versatile string handling capability. Extension English language diagnostics of the 8550 provide easy to understand error messages and locate the line in which the error has occurred. When assembly is completed, the assembled object code is stored on disc in a newly created binary format file.

Three Emulation Modes

After an error-free assembly listing has been obtained, the resulting object code may be executed in system emulation mode 0 on the optional emulator processor. The emulator processor is identical to the microprocessor that will finally be installed in the user's prototype. Execution is performed under control of the debug system; during execution, program steps can be traced, software breakpoints can be set, and memory can be examined and changed as required. Should an error be discovered, that portion of the program can be corrected at the source level using the text editor. It can then be reassembled and executed again. This procedure continues until the program is correct.

After the software has been debugged, it may be exercised on the prototype circuitry in the partial emulation mode (mode 1). During partial emulation, control may be released from the 8550 to the prototype in stages. The developmental software runs using 8550 memory space and prototype I/O and clock. The 8550 memory mapping feature allows memory to be gradually mapped over to the prototype in 128-byte address blocks. Throughout partial emulation, the user has access to prototype circuitry through the debugging system, which enables him, as before, to trace, set breakpoints, examine and change memory and register contents.

In full emulation (mode 2) the program is run on the prototype, but program execution is still under the complete control of the debug system. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively free-standing, then, the user may still direct program activity from the 8550.

8550 Parts and Functions

Real-Time Prototype Analyzer

The real-time prototype analyzer option is useful for resolving timing problems in the prototype. This hardware trace function captures bus information from the program as it executes. It can store this information and display it later in trace format, or it can use the information to trigger a break in execution, time a program segment, or signal an external device usch as a logic analyzer.

8550 Parts and Functions

Refer to Figure 1 for the functional block diagram of the complete 8550 Microcomputer Development Lab system.

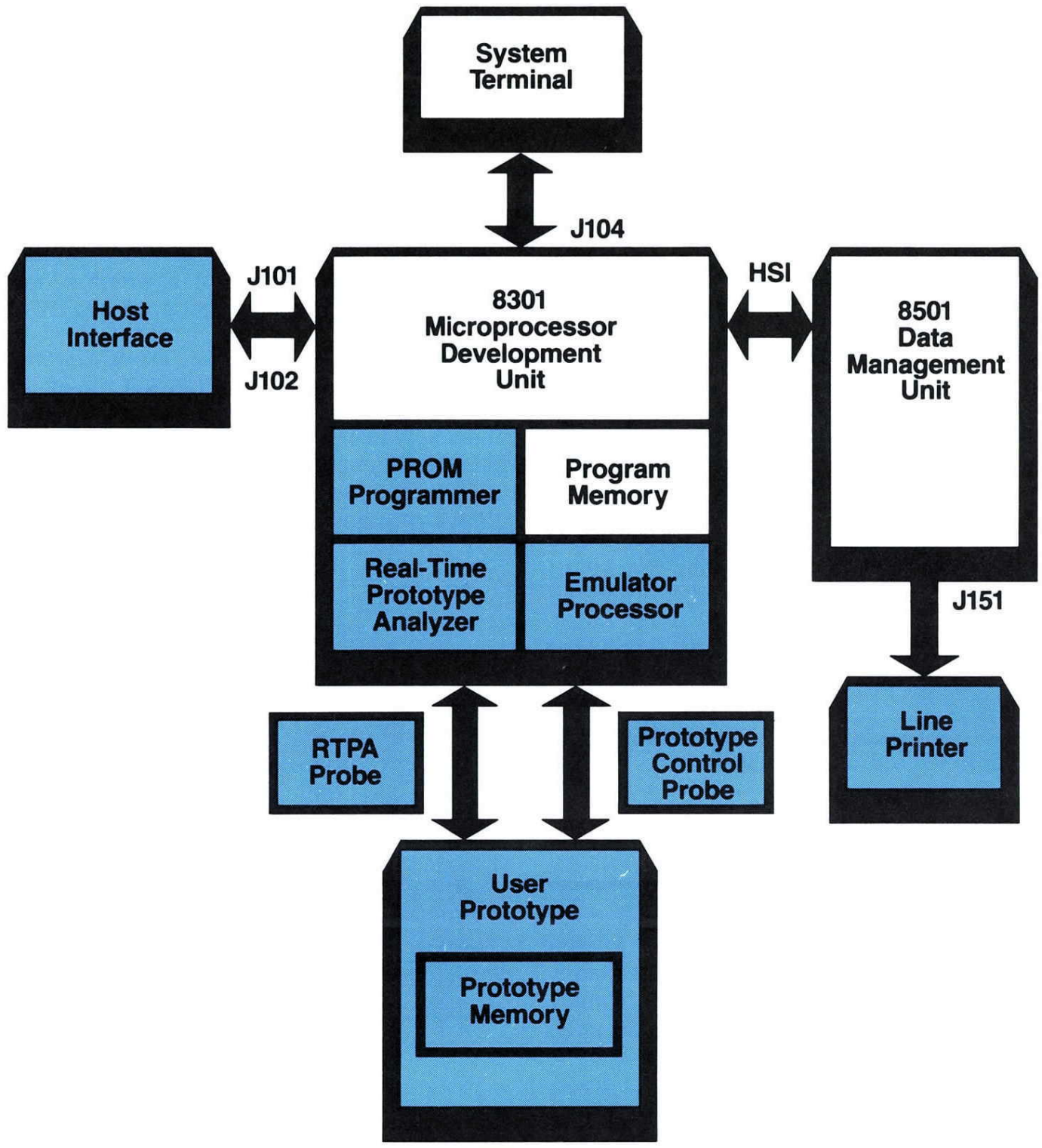


Figure 1 shows the components of a complete 8550 Microcomputer Development Lab system.

8550 CHARACTERISTICS

8301 MICROPROCESSOR DEVELOPMENT UNIT

Physical

Height	11 in	(280 mm)
Width	17 in	(430 mm)
Length	23 in	(585 mm)
Net Weight	60 lbs	(27 kg)

ENVIRONMENTAL

Operating Temperature	32°F to 122°F (0°C to 50°C)
Humidity	90% @ 86°F to 140°F (30°C to 60°C)
Altitude	
Operating	0 to 15,000 ft (4,500 m)
Storage	0 to 50,000 ft (15,000 m)

POWER REQUIREMENTS

115 V ac (90 V ac-132 V ac) @ 48 to 66 Hz.
230 V ac (180 V ac-250 V) @ 48 to 66 Hz.

Outputs

5.2 V dc +1%/-2% @ 35.0A
+12 V dc +0/-5% @ 1.7A
−12 V dc +0/-5% @ 1.7A

8501 DATA MANAGEMENT UNIT

Physical

Height	10.5 in	(267 mm)
Width	16.8 in	(424 mm)
Length	23.5 in	(597 mm)
Net Weight	55 lb	(25 kg)

ENVIRONMENTAL

Operating Temperature	50°F to 104°F (10°C to 40°C)
Humidity	20% to 80% relative noncondensing
Altitude	
Operating	0 to 8,000 ft (2500 m) Derate max operating temp. by 1°C for each 300 m above 2400 m.
Storage	0 to 50,000 ft (15,000 m)

POWER REQUIREMENTS

115 V ac (90-127 V RMS) @ 50 Hz ±1% or 60 Hz ±1%.
230 V ac (180-250 V RMS) @ 50 Hz ±1% or 60 Hz ±1%.

Outputs

24 V dc ±5% @ 2A
12 V dc ±3% @ 4A
−12 V dc ±5% @ 540 mA
5 V dc ±5% @ 20 A
15 V dc ±10% @ 20 mA

Output Ripple

24 V dc	100 mV (p-p)
±12 V dc	120 mV (p-p)
15 V dc	50 mV (p-p)
15 V dc	100 mV (p-p)

Overload Protection

Automatic current limit foldback.

FLEX DISC CHARACTERISTICS

Encoding — IBM compatible single or double density. Format must qualify as follows: MFM sectors—256 bytes. FM sectors—128 bytes.

Diskette Type — Single or double sided, soft sectored.

Capacity —

Double sided, double density 1,021,696 bytes.

Single sided, double density 509,184 bytes.

Single sided, single density 256,256 bytes.

Microprocessor Development Lab and Software Support

16-Bit Assembler and Prototype Debug Support

The 8086 and Z8000 Assemblers and 8086 Prototype Debug package are software products intended for use with the Tektronix 8550 Microcomputer Development Lab. The Assemblers support any software development effort targeted for the Intel 8086 or 8088 microprocessor or Zilog Z8002, while the Debug package will support the Intel iSBC 86/12A™.

In a typical design situation, the Assembler and Debug software is used in the following manner: First, an absolute object code file is generated by the Assembler or modules are linked to form a load file. Next, the file is downloaded to the SBC under control of the debug software, which supplies the protocol necessary for the serial transfer. This hardware link is accomplished through an RS-232 interface between the 8550's systems communication module and the SBC's serial data port. The 180 cm (6 ft) interface cable is supplied as part of the package. With the download complete, debug commands are entered through the 8550 system console and executed by interaction between two software components, one resident in the 8550 and the other on board the SBC. Both of these components are supplied as part of the debug package.

The Assembler

The Assembler supports software development by converting source code into executable object code, using a source file that has been created through the editing software. It will assemble code within an address range of 0 to 64K bytes, which allows full use of the memory space on the iSBC 86/12A.

Included with the assembler are a powerful set of macro features which allow the expansion of in-line code. Among these are the ability to call macros through easily identificable names, and the inclusion of an indefinite number of arguments. Assembly time string manipulation is allowed, including the use of variable length strings both inside and outside of macros. There is also a group of commands which allow conditional assembly based on an IF/ELSE structure. If more than one object code module is used, the linker will combine the separate files into a single load file.

Prototype Debug

The Debug package supports hardware/software integration on the iSBC 86/12A through two operations. First, it allows assembled absolute object code or a linked load file from the 8550 to be serially downloaded to the SBC memory for execution by its 8086 processor. Second, it permits a wide range of debugging operations to occur while exercising the downloaded software on the SBC.

Program execution can take place in real-time with predetermined breakpoints, or in single instruction steps. During debugging, the user can examine and modify the contents of both the SBC memory and the processor registers. In addition, blocks of data can be moved from one set of memory locations to another. The memory can also be filled with a specified hex or ASCII string, or searched for the occurrence of a specified data pattern. The results of debugging can be saved by uploading the SBC memory contents to the 8550 for file storage.

8002A

Multiple Microprocessor Support

In-Circuit Emulation

Real-Time Prototype Analysis

The 8002A Microprocessor Lab is a complete software development system for the design of microprocessor-based products. A key feature is its ability to support many microprocessor chips, including the Intel 8085A, 8080A, 8048, 8049, 8039, 8039-6, 8035 and 8021, Motorola 6800 and 6802, Texas Instruments TMS9900, Zilog Z-80A, Fairchild F8, RCA 1802, Mostek 3870/72, and the Rockwell 6500/1. The 8002A also supports the new 16-bit processors inciuding the Intel 8086/88, Zilog Z8000, and the Motorola 68000.

In addition to multiple microprocessor support, the 8002A offers a superior operating system and powerful text editor, assembler, and debugging programs; three optional levels of emulation for software debugging, partial and full emulation; and a real-time prototype analyzer option offering all the capabilities of a microprocessor analyzer with eight channels of external input.

Software Development and Debugging

In a typical design sequence, software is developed using all the resources of TEKDOS, the disc-operating system software for the 8002A Microprocessor Lab. TEKDOS performs flexible disc and file utility functions, data transfer functions, and system/peripheral device control functions. In addition to relieving the user of these housekeeping chores, TEKDOS also supervises the text editor, assembler, and linker programs and the optional emulation support, debugging system, and PROM programming routines.

Program entry and editing may be accomplished module by module. The line-oriented text editor offers several convenience features for preparing, correcting, and modifying the program quickly and easily.

The assembler processor, with the appropriate disc inserted in the flexible disc drive, performs program assembly functions for each microprocessor supported by the 8002A.

After an error-free assembly listing has been obtained, the resulting object code may be executed in system emulation mode 0 on the optional emulator processor.

Partial and Full Emulation

After the software has been debugged, it may be exercised on the prototype circuitry in the partial emulation mode (mode 1). During partial emulation, control may be released from the 8002A to the prototype in stages.

In full emulation (mode 2) the program is run on the prototype, but program execution is still under the complete control of the debug system. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor.

8002A CHARACTERISTICS

The 8002A Microprocessor Lab is a modular system whose mainframe houses up to 20 plug-in circuit boards. A terminal is necessary for system operation, and may be ordered as an optional peripheral.

The Real-Time Prototype Analyzer module, additional 16K byte Program Memory modules (Standard Program Memory consists of 32k bytes of RAM), and PROM Programmer modules for the 1702 or 2704/2708 are available as system options.

In addition to the standard system console I/O port, the 8002A provides a system communication module with three RS-232-C compatible ports for use with such peripherals as paper tape reader/punchers, line printers (LP8200), printing terminals (CT 8101) modems and other peripherals. One port is designated a general purpose RS-232-C compatible-input/output port with independent input and output baud rate selection. Another port is an RS-232-C compatable-output-only port for use with line printers. The third port is a modem-compatible port for use with half duplex modems. All ports have strap selectable baud rates of 110, 300, 600, 1200, or 2400.

Emulator Processor and Prototype Control Probe Support Packages

The 8550, 8002A, and 8001 Microcomputer Development Labs support a wide variety of different microprocessors and microcomputers.

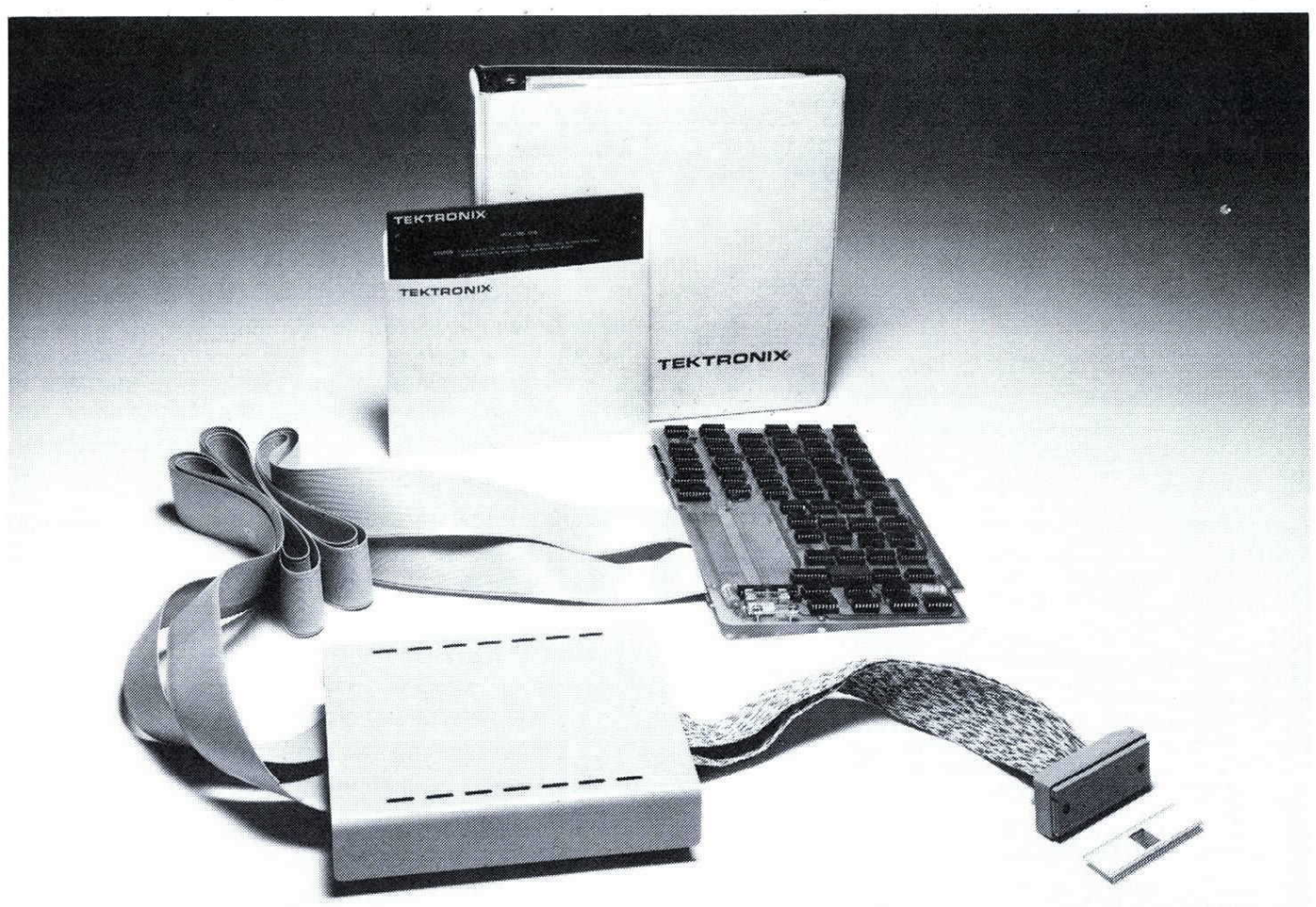
Emulators are currently available for the Intel 8080A, 8085A, 8048, 8049, 8039, 8039-6, 8035 and 8021, Motorola 6800 and 6802, Texas Instruments TMS9900, Zilog Z-80A, Fairchild F8, RCA 1802, the Mostek 3870 and 3872, and Rockwell 6500/1.

Emulator packages for the 8002A and 8001 may be ordered as system options. These options provide the capabilities necessary to fully emulate the target microprocessor in a user's prototype system.

The emulator processor, which resides on a plug-in circuit module along with controlling logic circuitry, enables the user to execute and debug the program on a microprocessor identical to the one which will be used in the prototype, while giving him access to the full 64K bytes of Microprocessor Lab program memory.

The prototype control probe, which links the emulator processor to the prototype system, allows partial and full in-circuit emulation.

All emulation operations are controlled by the powerful Microprocessor Lab system software. The user is able to monitor program execution, set software breakpoints, examine and change memory and register contents. Debug trace information is displayed in a format unique to the microprocessor, with instruction fetches disassembled into mnemonics for easy interpretation.



8049, 8035, 8039, 8039-6, 8022, 8041A, 8048/8021 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

8048, 8049, 8039, 8039-6, 8035, 8022, 8041A and 8021 are trademarks of Intel Corporation, Tektronix, Inc., does not guarantee that other vendor's versions of these microcomputers will be compatible with Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft. (1.8 m) of cable from the emulator processor to the interface assembly. 1.5 ft. (45 cm) of cable from the interface assembly to the 40-pin plug (or 28-pin plug for 8021).

Cable Configuration

6 ft. (1.8 m)

Two 40 conductor ribbon cables with alternating ground and signal paths.

1.5 ft. (45 cm)

Two laminated 40 conductor cables made up of signal-ground pairs.

(TYPICAL WORST CASE) EMULATION INTERFACE DELAYS FOR THE 8048 (8021 IF DIFFERENT)

		tPLH (ns) Typ. Worst Case	tPHL (ns) Typ. Worst Case
ALE		14,20	14,20
$\overline{PSEN}$		22,32	22,32
$\overline{RD}$,$\overline{WR}$		18,26	15,22
$\overline{PROG}$		14,20	14,20
D80-D87*** (P00-P07) User to CPU	t_1—fetch cycle t_2—execute cycle	,90 26,38	,90 26,38
D80-DB7 (P00-P07) CPU to User	t_3—Address Out t_4—Ext Data Out t_5—OUTL, ANL, ORL, data out	26,38 26,38 14,20	26,38 26,38 14,20
P10-P17 P24-P27		2,2	2,2
P20-P23			
TO**	out/in	11,15	11,15
T1			102,82
$\overline{INT}$		21,32	21,32
RST	8048 (8021)	(120,212)	69,122
SS		22,32	22,32
CLK		29,47	31,52

*INTEL 8099 chip specifications.

**for clock in to 8039 > 6 MHz and memory mapped to 8550, t0 out is divided by 2.

***tRD* = t 1.2 + t user mem access.

8041A PROTOTYPE CONTROL PROBE

(Typical, worst case) Emulation Interface Delays

	tPLH (ns) (typ. WC)	tPHL (ns) (typ. WC)
SYNC	14,20	14,20
$\overline{PROG}$	14,20	14,20
T1		27,39
P10-P17	2,2	2,2
T0	29,45	22,34

Symbol	Parameter	Min	Max	Units
tACC	$\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$	54		ns
tCAC	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	71		ns
tACD	$\overline{DACK}$ to data valid		225	ns
tCRQ	$\overline{RD}$ or $\overline{WR}$ to DRQ cleared		200	ns
tAW	$\overline{CS}$,A0 Setup to $\overline{WR}$	0		ns
tWA	$\overline{CS}$,A0 Hold after $\overline{WR}$	24		ns
tWW	$\overline{WR}$ Pulse Width	250		ns
tDW	Data Setup to $\overline{WR}$	150		ns
tWD	Data Hold after $\overline{WR}$	70		ns

8022 PROTOTYPE CONTROL PROBE

8022 Timing Characteristics With Emulation Interface Delays

	tPLH (ns) typ. worst case	tPHL (ns) typ. worst case
ALE	24,34	32,46
P00-P07	54,87	57,91
P00-P07	1.3 μs	1.3 μs
P10-P17	t1—CPU to USER t2—USER to CPU } 2,2	2,2
P20-P23	for OUTL inst: data valid before ALE after the next instruction fetch. t3—MOVD P2, A 13,18 t4—MOVD A, P2 IN A, P2 } 13,18	17,24 17,24
$\overline{PROG}$	13,18	17,24
T0	17,24	17,24
T1	102,182	102,182
AN0,AN1	336,444	336,444
XTAL1	21,33	29,45

[1]Inputs must be present until read by an input instruction (Intel Specification).

Emulator Processor and Prototype Control Probe Support Packages

8080A EMULATOR SUPPORT PACKAGE CHARACTERISTICS

8080 and 8080A refer to microprocessors manufactured by Intel Corporation. Tektronix, Inc., does not guarantee that other vendors' versions of the 8080 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processor to the interface assembly.

1.5 ft. (45.8 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with alternating ground and signal paths.

1.5 ft (45.8 cm) — 2 twisted pair 40 conductor cables.

Termination

6 ft (1.8 m) — The interface assembly contains resistive termination and receivers for data, address, and control from the emulator processor module.

1.5 ft (45.8 cm) — Not terminated.

40 pin plug—40 pin spring plate protected plug. When used with a zero insertion force socket, an included 40 pin low profile DIP socket must be used between the zero insertion force socket and the 40 pin probe plug.

TIMING CHARACTERISTICS

Emulation Interface Delays*

To 8080A from Interface Assembly	Typ	Max (in ns)
ø1	44	60
ø2	44	60
$\overline{\text{HOLD}}$	44	67
$\overline{\text{RESET}}$	44	67
RDY**	35	40
$\overline{\text{INT}}$	63	104
DATA	44	53

From 8080A to Interface Assembly	Typ	Max (in ns)
HOLDA***	39	55
SYNC	37	45
$\overline{\text{WAIT}}$	37	45
$\overline{\text{WR}}$	37	45
DBIN	37	45
INTE	39	55
ADDRESS	27	35
DATA	50	63

**Assumes 6 ft of cable at 1.5 ns/ft.*

***RDY is ignored unless user memory or I/O is accessed in control mode 2 or special mode.*

****The equation for HOLDA to tristate timing is as follows: HOLDA • DBIN = FLOAT. Tristate of data and address follows the trailing edges of DBIN or WR by approximately 20 ns.*

8085A EMULATOR SUPPORT PACKAGE CHARACTERISTICS

8085 and 8085A refer to microprocessors manufactured by Intel Corporation. Tektronix, Inc., does not guarantee that other vendor's versions of the 8085 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processor to the interface assembly.

1 ft (30 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with chassis ground plane and signal paths.

1 ft (30 cm) — 2 40-conductor twisted pair cables.

Termination

6 ft (1.8 m) — The interface assembly contains receivers for data, address, and control from the 8085 emulator processor module.

1 ft (30 cm) — Not terminated.

AC CHARACTERISTICS

Emulation Clock

Mode 1 or Mode 2 (user's clock), with 8085A Prototype Control Probe.	6.25 MHz max*; crystal, RC timing network or TTL input to X1.
Mode 0 (system clock)	6.25 MHz ±0.01%

6800/6802 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

6800 and 6802 refer to microprocessors manufactured by Motorola Corporation. Tektronix, Inc., does not guarantee that other vendors' versions of the 6800 or 6802 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processor to the interface assembly.

1 ft (30 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with alternating ground and signal paths.

1 ft (30 cm) — 2 twisted pair 40 conductor cables made up of signal/ground pairs.

6800 PROTOTYPE CONTROL PROBE
Read/Write Timing (in ns)

Characteristic	Symbol	Min	Typ	Max
Peripheral Read Access Time	^{D}TACC			506
Address Setup Time	^{D}TAD			350
R/W Setup Time	^{D}R/WSU			375
VMA Setup Time	^{D}EVMA			365
Data Setup Time (Read)	^{D}TDDR	119		
Data Delay Time (Write) (relative to 01↑)	^{T}DDW			513
Delay for DBE Rising Edge (relative to 01↑)	^{D}DBER			444
Input Data Hold Time	^{D}HRD	29		
Output Data Hold Time (after 01↑)	^{D}TDWH	40**	10	
Output Data Hold Time (after DBE↓)	^{D}TDWH	20		
Address Hold Time	^{D}ADH	65		
VMA Hold Time	^{D}VMAH	68		
R/W Hold Time	^{D}R/WH	61		

6802 PROTOTYPE CONTROL PROBE
Read/Write Timing (in ns)

Characteristic	Symbol	Min	Typ	Max
Peripheral Read Access Time	^{D}TACC			480
Address Setup Time	^{D}TAD			367
VMA Setup Time	^{D}EVMA			373
R/W Setup Time	^{D}R/WSU			392
Data Setup Time (Read)	^{D}TDDR	127		
Data Delay Time (Write)	^{T}DDW			527
Input Data Hold Time	^{D}HRD	40**	10	
Output Data Hold Time	^{D}TDWH	39		
Address Hold Time	^{D}ADH	63		
VMA Hold Time	^{D}VMAH	66		
R/W Hold Time	^{D}R/WH	70		

**Although data should remain valid at least 40 ns after Enable, typically 10 ns will be sufficient.

Z80A EMULATOR SUPPORT PACKAGE CHARACTERISTICS

Z80 and Z80A refer to microprocessors manufactured by Zilog Corporation. Tektronix, Inc., does not guarantee that other vendor's versions of the Z80 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processort to the interface assembly.

1 ft (30 cm) of cable from the interface assembly to the 40 pin plug.

Cable Configuration

6 ft. (1.8) — 2 40-conductor ribbon cables with chassis ground plane and signal paths.

1 ft (30 cm) — 2 40-conductor twisted pair cables.

Termination

6 ft (1.8 m) — The interface assembly contains receivers for data, address, and control from the Z80 Emulator Processor module.

1 ft (30 cm) — Not terminated.

TIMING CHARACTERISTICS

The Z80A Emulator Processor was designed to match the ac characteristics of the Z80A and Z80 Microprocessors.

TMS9900 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

TMS9900 refers to microprocessors manufactured by Texas Instruments Corporation. Tektronix, Inc., does not guarantee that other vendor's versions of the TMS9900 will be compatible with the TEKTRONIX Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from the emulator processor to the interface assembly.

9.5 in (24.2 cm) of cable from the interface assembly to the 64 pin plug.

Cable Configuration

6 ft (1.8 m) — 2 40-conductor ribbon cables with chassis ground plane and signal paths.

9.5 in (24.2 cm) — 2 32-conductor twisted pair cables.

Termination

6 ft (1.8 m) — The interface assembly contains receivers for data, address, and control from the TMS9900 emulator processor module.

9.5 in (24.2 m) — Not terminated.

TIMING CHARACTERISTICS

To TMS9900 from Interface Assembly	Emulation Typical	Interface Delays* Maximum (in ns)
ø1	41	59
ø2	41	59
ø3	41	59
ø4	41	59
CRUIN	12	23
INTREQ	12	18
IC0	12	23
IC1	12	23
IC2	12	23
$\overline{\text{IC3}}$	12	23
$\overline{\text{HOLD}}$	12	18
$\overline{\text{READY}}$	12	18
$\overline{\text{LOAD}}$	12	18
RESET	68	98
DATA	14	21

From TMS9900 to Interface Assembly	Typical	Maximum (in ns)
DBIN	24	41
MEMEN	12	18
WE	12	18
CRUCK	12	23
CRUOUT	12	23
HOLDA	12	23
WAIT	12	23
IAQ	12	23
ADDRESS	14	21
DATA	14	21

**Assumes 1.5 ft of cable at 1.5 ns/ft.*

Note: All inputs and outputs of the 64 pin plug at the end of the prototype control probe are buffered by 74LSXXX type devices. In all cases, data and control should not change during clock ø1.

6500/1 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

6500/1 is a trademark of Rockwell International Corporation. Tektronix, Inc. does not guarantee that other vendor's versions of these microcomputers will be compatible with Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft) of cable from the emulator processor to the interface assembly. 45 cm (1.5 ft) of cable from the interface assembly to the 40-pin plug.

Cable Configuration

1.8 m (6 ft) — Two 40 conductor ribbon cables with alternating ground and signal paths.

45 cm (1.5 ft) — Two laminated 40 conductor cables made up of signal-ground pairs.

TYP Delays in ns added to 6500/1E by Emulator with 6.8K Pull Up Resistors

		Output Driving	Input Receiving
PA0—PA7	RISING EDGE	1 CLK CYCLE +300	100
	FALLING EDGE	1 CLK CYCLE +300	100
PB0—PB7, PC0—PC7, PD0—PD7	RISING EDGE	300	*
	FALLING EDGE	30	*
CNTR	RISING EDGE	100	100
	FALLING EDGE	20	20

*Gated in only during a read instruction from 81, 82, 83.

F8, 3870, 3872 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

F8 refers to microprocessors manufactured by Fairchild's Corporation; the 3870 and 3872 refer to microcomputers manufactured by Mostek Corporation. Tektronix, Inc., does not guarantee that other vendor's versions of the F8, 3870, or 3872 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length 6 ft (1.8 m) of cable from emulator processor to the interface assembly. 1 ft (30 cm) of cable from the interface to 40 pin plug.

Cable Configuration

6 ft (1.8 m) — Two 40-conductor ribbon cables with chassis ground plane and signal paths.

1 ft (30 cm) — Two 40-conductor twisted pair cables.

Termination

6 ft (1.8 m) — The interface assembly contains receivers for data, address, and control from the F8/3870/3872 Emulator Processor module.

1 ft (30 cm)—Not terminated.

TIMING CHARACTERISTICS

3870/3872 — The 3870/3872 Prototype Control Probe was designed to meet all the ac characteristics of the 3870 and 3872 Microcomputers.

F8 (3850) — The F8 Prototype Control Probe meets all of the F8 ac characteristics with the following exceptions: (1) the worst-case delay from the falling edges of WRITE to the ROMC lines being valid is 650 ns (compared to 550 ns for the F8 CPU); (2) the worst-case skew between an external clock input is 0 to 90 ns longer than that specified for the F8.

1802 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Length — 6 ft (1.8 m) of cable from the emulator processor to the interface assembly. 1.5 ft (45 cm) of cable from the interface assembly to the 40-pin plug.

Cable Configuration

6 ft (1.8 m) — Two 40-conductor ribbon cables with alternating ground and signal paths.

1.5 ft (45 cm) — Two laminated 40-conductor cables made up of signal-ground pairs.

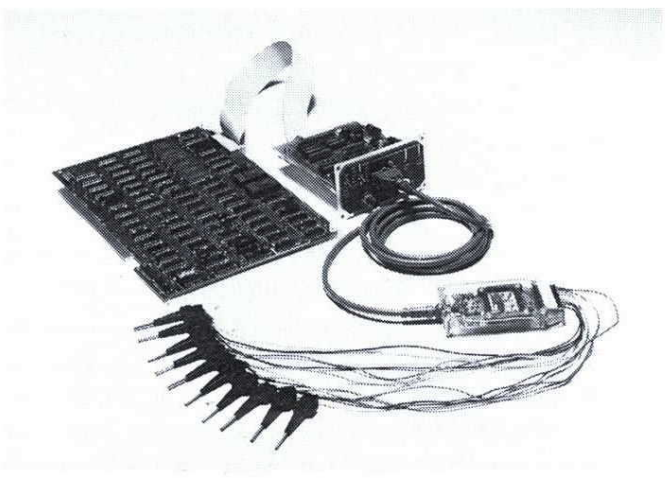
TIMING CHARACTERISTICS

The 1802 Prototype Control Probe is designed to meet all the ac characteristics of the 1802 Microprocessor —Vcc ≥4.0 V.

AC CHARACTERISTICS

Emulation Clock

Mode 1 or Mode 2 (user clock) with 1802 Prototype Control Probe.	5.0 MHz max at 10 Vcc. 25°C, this can be crystal, or external input to clock (pin 1).
Tracking power supply to monitor user voltage (Vcc) and run the probe at the same voltage (4 V to 12 V).	2.5 MHz



REAL-TIME PROTOTYPE ANALYZER

The Real-Time Prototype Analyzer, Option 46 for the 8001 and 8002A Microprocessor Labs, and Option 01 for the 8550 Microcomputer Development Lab, is comprised of a real-time trace module, a data acquisition interface, and an 8 channel general logic probe. This option provides a real-time trace of the user program executing on the emulator processor, with 43 channels of data acquired simultaneously. The prototype address bus, data bus, control bus, and any eight external locations on the prototype circuit may be monitored without slowing up the operational speed of the processor. The Real-Time Prototype Analyzer is indispensable when isolating critical timing errors and hardware/software sequence discrepancies during the final integration phases of prototype development.

The analyzer module is a separate plug-in circuit card that may be inserted into either the 8550 or 8001 system mainframe. The P6451 Probe connects to the prototype circuitry and permits data transference from the prototype to the analyzer. Data from the prototype is buffered and driven by the probe to the data acquisition interface, and then loaded into the analyzer module's real-time trace buffer.

As the user program executes on the emulator processor, 48 bit data words are sequentially acquired from the prototype and loaded into the real-time trace buffer. Each data word contains 16 bit data from the address bus; 8 bit or 16 bit data from the data bus; 8 bit data from the test probe; 3 bit data identifying cycle type (read, write, I/O, memory, or instruction fetch); and 5 bit data used internally to identify last start/stop of the emulator processor. The analyzer will continue to acquire these sequential cycles of logic input until the processor is stopped or the real-time trace buffer is frozen by a specified trigger occurrence. The real-time trace buffer can retain up to 128 data words in pre-, variable center, or post-trigger modes; thus enabling the storage of pertinent program bus transactions.

The Real-Time Prototype Analyzer offers expanded breakpoints to aid in efficient location of prototype problems. Two event comparators located within the analyzer module can be utilized to halt program execution and stop real-time trace. A trigger may be generated on any specific data occurrence in the address bus, data bus, test probe input, and instruction cycle type. Triggering may be immediate; delayed by counting the number of passes; or delayed by counting the number of clock select outputs (clock select may be by microseconds, milliseconds, emulator clocks, etc.). In addition, an output pulse may be generated, via the data acquisition interface, to trigger a logic analyzer or an oscilloscope.

The two event comparators (triggers) may be set to designate a break or halt in the program execution. These comparators may be used as independent breakpoints; or they may be used together to enable a breakpoint on a specific event combination. The program execution can be halted when two trigger events occur simultaneously; when one trigger event precedes another; or when either trigger event occurs. When a break in the program execution takes place, program transactions stored in the real-time trace buffer may be displayed or printed.

Data stored in the real-time trace buffer is displayed sequentially in the order it was acquired from the prototype. Buffer content may be displayed in whole or in part. Optional command parameters are available to limit the storing of data to any specific transaction type, such as memory reads only. If the total buffer contents are displayed, a blank line will separate the data sequence associated with each program starting point.

The Real-Time Prototype Analyzer features a convenient and easy-to-understand display format. With this format, the address location, data, probe input, and control bus data of each acquired transaction are displayed. If the transaction was an instruction fetch, the instruction is also disassembled into the appropriate mnemonic readout unique to the emulator type being used.

Prototype Analyzer, High Level Language

The Real-Time Prototype Analyzer functions in all emulation modes and operates with all commercial microprocessors supported by the 8550, 8002A and 8001 Microcomputer Labs.

REAL-TIME PROTOTYPE ANALYZER CHARACTERISTICS

OPERATIONAL SPEED CHARACTERISTICS

Processor	Maximum Processor Clock Rate*
8085A	3.125 MHz (internal clock)
8080A	2.08 MHz
6800/6802	1.00 MHz
Z80	4.00 MHz
TMS9900	3.33 MHz
3870/3872	4.00 MHz
F8	2.00 MHz
6500/1	1.00 MHz
1802	6.4 MHz

**Maximum processor clock rate for Real-Time Prototype Analyzer operation.*

INPUT/OUTPUT CHARACTERISTICS

Variable Threshold

Range	$>+10$ V dc to <-10 V dc
Preset TTL Voltage	$+1.4$ V dc ± 200 mV
Event Trigger Out	High level voltage out (when Vcc=Min, Vi=0.5, Ro=50 Ω to GND) is >2 V dc.

Adjustments—Variable Threshold may be adjusted from $>+10$ V dc to <-10 V dc with a screwdriver adjustment accessible at the rear panel of the Microcomputer Lab. This voltage must be monitored with a voltmeter having an input impedance of at least 10 MΩ.

Jumpers—With the internal jumper in position '0-3' the clock threshold is designated to be the same as channels 0-3. In position '4-7' the jumper designates the clock threshold to be the same as channels 4-7.

Cable Length — 50 cm (19.5 in).

MODULAR DEVELOPMENT LANGUAGE MDL/μ

MDL/μ is a high level language designed specifically for use in microprocessor-based design. Its parent language is ANSI Minimal BASIC, a widely used and well understood programming format. MDL/μ offers an extensive number of enhancements from BASIC that make this new language an extremely effective design tool while retaining the advantages of simplicity and easy learning found in BASIC.

One essential advantage of MDL/μ is that it uses a compiler instead of an interpreter. Each program statement is translated to machine code only once, instead of every time the statement is executed. The result is faster, and often more compact code for final program execution.

MDL/μ allows a module-oriented approach to software development. Two statements, USES and PROVIDES, allow variables, functions and procedures to be shared by programmers working on different modules of an overall program. The USES statement also allows direct access to absolute memory locations, I/O ports and interrupts—all essential for proper control of hardware/software integration.

Variable names and strings have been considerably expanded with MDL/μ. Variable names can contain up to six characters, the first alphabetic and the others alphanumeric, for easy identification during program development. Strings can vary in length from 1 to 255 characters instead of the unalterable 18 used in minimal BASIC. Substring replacement is also enhanced to assist in character manipulation.

I/O features include access to ports and absolute addressing of memory, which allows variables to be assigned a specific address. Both ASCII and general purpose binary file manipulations are possible through a series of I/O statements including OPEN, CLOSE, RESTORE, READ, WRITE, PRINT and INPUT.

Among many other MDL/μ enhancements to BASIC are logical operators (AND, OR, XOR, NOT) plus shift and rotate operations for bit manipulation, DISABLE and ENABLE to turn the interrupt off and on and a built in code optimization.

The conversion of MDL/μ source code to actual machine code is a three-step process. The first step converts MDL/μ source code into assembly language source code which is stored on a file or device. The assembly source code contains the original MDL/μ statements as comments preceding each block of assembly source code. At this stage, the assembly language can be further optimized by using the 8550's powerful editor. In the second step the assembler converts the assembly language source into object code. The third step is to link the object code with the run time support library and any other assembled object code modules.

PASCAL: HIGH-LEVEL PROGRAMMING LANGUAGE

Pascal, a high-level programming language, is receiving much attention in the electronics industry. Features such as program structure, strong data typing, and readability greatly enhance programmer efficiency, and thereby reduce software development and maintenance costs. The Tektronix Pascal 8080/8085 Compiler is designed specifically for those who are writing programs for the 8080 or 8085 microprocessors. The Tektronix Pascal 8080/8085 Compiler is a superset of the ISO draft standard Pascal. A true compiler rather than a P-code interpreter, the Pascal 8080/8085 Compiler generates object code directly. Each program statement is translated to machine code only once instead of every time the statement is executed, resulting in faster and often more compact code.

Standard Pascal Features

Pascal is a block-structured language that allows the program to be divided into subprograms called procedures and functions. This block structure encourages programmers to logically plan and construct programs, so debugging time is greatly reduced. The block structure also requires that all variable declarations occur prior to executable code.

Pascal's six control structures correspond closely with flowchart elements and make algorithm coding very natural. All control structures have a single entrance and exit unless GOTO's are used, so program modifications are unlikely to introduce errors into the program.

Pascal allows programmers to use many flexible forms of data representations and to define data types that accurately express their particular problems. Pascal also has strong data typing, which means that each variable must be defined as a single data type prior to its use and used consistently with its definitions.

Pascal programs are easy to read, and thus to maintain. Pascal differs from most line-oriented languages by allowing extra spaces, tabs, and carriage returns almost anywhere. Variable, procedure, and function names can be meaningful and easily understood because they are not restricted in length. However, identifiers used by TEKDOS must be unique in the first eight characters, other identifiers, in the first 19.

Tektronix Pascal 8080/8085 Compiler Major Extensions

Input/Output

Included with the Pascal 8080/8085 Compiler are several predefined procedures and functions used for chip-level I/O. A procedure to send data to a specified port and function to read data from a specified port are included. These procedures and functions are analogous to the standard Pascal WRITE, WRITELN, READ, READLN procedures, which are available for 8002A mode O operation when using TEKDOS I/O. All of the 8002A's I/O capability is available to a Pascal program running in emulation mode O, so the Pascal program can access the console terminal, discs, line printer, and auxilliary I/O ports. The Pascal 8080/8085 Compiler also allows an ORIGIN attribute to be associated with variables. The ORIGIN attribute assigns variables to specific memory addresses and is very useful for memory mapped I/O.

Interrupt Handling

The Pascal 8080/8085 Compiler supports full use of the 8080's and 8085's interrupts. The interrupts are supported by writing the interrupt service routine as a separate procedure having the INTERRUPT attribute. Separate routines are required to connect a specific interrupt vector to the appropriate interrupt service routine. The interrupt service routines are included as convenience routines with the compiler. Procedures are also supplied to set (SIM) and read (RIM), the 8085's interrupt mask.

Linkage to Assembly Routines

Speed-critical or timing-critical applications are likely to require some program segments to be written in assembly language. Because the code generated by the Pascal 8080/8085 Compiler is compatible with the 8002A linker, assembly code can be linked to Pascal code.

Separate Compilations

Separate compilations are supported by the Pascal 8080/8085 Compiler. The main program module's first word is the keyword "PROGRAM." Submodules to be separately compiled begin with the keyword "MODULE". Global variables, procedures, and functions can be referenced between separately compiled modules and the main program via PUBLIC and EXTERN attributes. The PUBLIC and EXTERN attributes are associated with variables, procedures, and functions and cause the compiler to generate the appropriate linker text.

Non-Decimal Integers

In many microcomputers applications, programmers want to use non-decimal integers. The Pascal 8080/8085 Compiler supports binary, octal, and hexadecimal integers for input and output.

ROM/RAM Applications

ROM/RAM applications are facilitated by control-section typing. Control-section typing means that the compiler gives the user the information he needs to allocate program variables into a linker section separate from literals, constants, and instructions, which are put into a second linker section.

Structured Constants

Standard Pascal allows only constants of type, integer, real, boolean, and text char. The Pascal 8080/8085 Compiler also provides constants which are arrays, and records. The most common application of structured constants is to initialize structured variables (arrays and records) that must reside in potentially volatile RAM.

Metacommands

Metacommands are compiler directives that cause the compiler to do such things as format the listings or generate run-time debugging code.

Tektronix offers maintenance training classes on Microcomputer Development Labs and a variety of user workshops featuring microprocessor hardware and software design concepts. For further training information, contact your local Field Office or request a copy of the Tektronix Customer Training Catalog on the return card at the back of this catalog.

4024 Computer Display Terminal

The 4024 Computer Display Terminal is an optional peripheral recommended for use with the 8001 or 8002A Microcomputer Labs.

The 4024 Computer Display Terminal is serially interfaced to either Microprocessor Development Lab through an EIA standard RS-232-C port on the systems communications module. The 12 inch (30 cm) diagonal crt displays up to 34 lines of 80 characters each, and the keyboard contains a full ASCII set of characters in upper and lower case. Option 20 (8K bytes Program Memory) is required for proper 8001 and 8002A operation.

4024 Computer Display Terminal with Option 20* **$3450**

LP 8200 Line Printer

The LP 8200 Line Printer is an optional system peripheral for the 8002A and 8001 Microprocessor Labs.

The LP 8200 is serially interfaced to either Microprocessor Lab through an EIA standard RS-232-C port on the system communications module. Baud rates of 300 to 9600 are selectable.

The printout provides space for 132 characters/line, 6 lines/vertical inch. The full ASCII set of 96 upper/lower case characters is provided.

ELECTRICAL CHARACTERISTICS

Voltage	90 to 132 V ac standard*
Frequency	60 Hz ±1 Hz.
Power	400 W max (printing); 200 W max (idle).

PHYSICAL CHARACTERISTICS

Dimensions	**in**	**cm**
Height	33.5	85.09
Width	27.5	69.85
Length	21.7	55.12
Weight	**lb**	**kg**
Net	102	46.4

LP 8200 Line Printer **$3765**

*Alternate line voltages are available for the LP 8200. Please contact a Tektronix Sales Office in your area for more information.

4025 Computer Display Terminal

The 4025 Computer Display Terminal is an optional peripheral for use with the 8001 or 8002A Microprocessor Development Labs.

The 4025 Computer Display Terminal is serially interfaced to either Microprocessor Development Lab through an EIA standard RS-232-C port on the systems communications module. The 4025 Terminal provides all the capabilities of the 4024 plus the ability to expand from basic alphanumerics, to forms ruling and then into graphics. Option 20 (8K bytes Program Memory) is required for proper 8001 and 8002A operation.

4025 Computer Display Terminal with Option 20* **$4050**

*Option 20 (8K bytes Display Memory) is required for proper 8001 and 8002A operation.

MDL WORKSHOP

Tektronix offers four Microcomputer Development Lab Workshops in a number of locations throughout the year. The courses on intensive, hands-on workshops designed to help the attendee meet the demanding challenges of the growing microcomputer development market.

Introduction to Microprocessor Software Design Workshop

The Introduction to Microprocessor Software Design Workshop is a comprehensive look at microcomputer software development, from flowcharting through hardware/software integration. It includes hands-on experience with the 8550 Microprocessor Development Lab, a self-contained microcomputer design tool. The introduction to Microprocessor Software Design Workshop is a Five-day course.

8550 Operations Workshop

The 8550 Operations Workship covers all aspects of the 8550 Microprocessor Development Lab, a design tool used for both software development and hardware/software integration. The 8550's features are explored in depth and applied to a typical microcomputer design cycle. Throughout the course, the attendee gets intensive, hands-on experience for an in-depth understanding of all 8550 operations. The 8550 Operations Workship is a Five-day course.

Microprocessor Hardware/Software Integration Techniques

The Microprocessor Hardware/Software Integration Techniques Workshop examines various aspects of the microcomputer design cycle and the role of each in the overall development scheme. Throughout the course, the participant will work with a number of design tools commonly used in developing microprocessor-based systems. Included are the 8550 MDL, logic analyzers, oscilloscopes and data communications testers. Extensive hands-on experience is provided for each tool. The Microprocessor Hardware/Software Integration Techniques Workshop is a Five-day course.

Microprocessor Software Development with Pascal Workshop

The Microprocessor Software Development With Pascal Workshop is an intensive examination of Pascal and its relationship to microcomputer software development. It emphasizes how to "think" in Pascal program structure and looks at the philosophy behind the language. In addition to defining the language in terms of the ISO Pascal standing, the course introduces Tektronix's special extensions aimed specifically at developing code at the microprocessor level. Also considered are tradeoffs between using assembly or high level language for micro software development, and the process of linking Pascal modules with assembly-written modules to form a complete program. The Microprocessor Software Development with Pascal Workshop is a Five-day course.

For detailed information on Tektronix Microcomputer Development Workshops and Workshop schedules, contact your local Tektronix Sales Engineer.

Ordering Information and Matrix

8001 Microprocessor Lab — $5350

Field Number	Emulator Support:	Factory Configuration Number	Price
8001F01	8080A Microprocessor Support Package	Option 01	$4100
8001F02	6800 Microprocessor Support Package	Option 02	$4100
8001F2A	6802 Prototype Control Probe	Option 2A	$ 990
8001F2B	6802 Microprocessor Support Package	Option 2B	$4100
8001F03	Z80A Microprocessor Support Package	Option 03	$4100
8001F04	TMS9900 Microprocessor Support Package	Option 04	$5100
8001F05	8085A Microprocessor Support Package	Option 05	$4100
8001F06	3870/3872 Microprocessor Support Package	Option 06	$4900
8001F07	F8 Microprocessor Support Package	Option 07	$4600
8001F08	1802 Microprocessor Support Package	Option 08	$4900
8001F09	8048/8021 Microprocessor Support Package	Option 09	$3710
8001F10	8048 Prototype Control Probe	Option 10	$1190
8001F11	8021 Prototype Control Probe Adapter (requires 8001F09 & 8001F10)	Option 11	$ 350
8001F12	8041A Prototype Control Probe (requires 8001F09)	Option 12	$1190
8001F13	8022 Prototype Control Probe (requires 8001F09)	Option 13	$1190
8001F14	6500/1 Microprocessor Support Package	Option 14	$4100
	System Options:		
——	32K Program Memory Modules	Option 45	$3100
8001F46	Real-Time Prototype Analyzer	Option 46	$2700
8001F48	2704/2708 PROM Programmer	Option 48	$ 650
8001F49	16K Program Memory Module	Option 49	$1550
——	220 V at 50 Hz	Option 4W	NC

8550 Microcomputer Development Lab — $12750

	Assemblers:		
8300A01	8080A/8085A Assembler	Option 1A	$ 850
8300A02	6800/6801/6802 Assembler	Option 1B	$ 850
8300A04	Z80A Assembler	Option 1C	$ 850
8300A05	TMS9900 Assembler	Option 1D	$ 950
8300O07	3870/3872/F8 Assembler	Option 1E	$ 850
8300A09	1802 Assembler	Option 1F	$ 850
8300A10	8048/8021/8041A/8022 Assembler	Option 1G	$ 850
8300A14	6500/1 Assembler	Option 1H	$ 850
8300A15	8086/8088 Assembler	Option 1J	$ 950
8300A20	Z8000 Assembler	Option 1K	$ 950
8300A26	68000 Assembler	Option 1L	$ 950
	Emulators:		
8300E01	8080A Emulator Processor and Emulator Control Software	Option 2A	$2350
8300E02	6800/6802 Emulator Processor and Emulator Control Software	Option 2B	$2350
8300E04	Z80A Emulator Processor and Emulator Control Software	Option 2C	$2350
8300E05	TMS9900 Emulator Processor and Emulator Control Software	Option 2D	$3150
8300E06	8085A Emulator Processor and Emulator Control Software	Option 2E	$2350
8300E07	3870/3872/F8 Emulator Processor and Emulator Control Software	Option 2F	$3150
8300E09	1802 Emulator Processor and Emulator Control Software	Option 2G	$3150
8300E10	8048/8021/8041A/8022 Emulator Processor and Emulator Control Software (requires 8300P10, 8300P12, or 8300P13)	Option 2H	$2950
8300E14	6500/1 Emulator Processor, Prototype Control Probe, and Emulator Control Software	Option 2J	$3340
	Probes:		
8300P01	8080A Prototype Control Probe	Option 3A	$ 990
8300P02	6800 Prototype Control Probe	Option 3B	$ 990
8300P03	6802 Prototype Control Probe	Option 3C	$ 990
8300P04	Z80A Prototype Control Probe	Option 3D	$ 990
8300P05	TMS9900 Prototype Control Probe	Option 3E	$1160
8300P06	8085A Prototype Control Probe	Option 3F	$ 990
8300P07	3870/3872 Prototype Control Probe	Option 3G	$ 990
8300P08	F8 Prototype Control Probe	Option 3H	$ 990
8300P09	1802 Prototype Control Probe	Option 3J	$ 990
8300P10	8048 Prototype Control Probe	Option 3K	$1190
8300P11	8021 Adapter (requires 8300P10)	Option 3L	$ 350
8300P12	8041A Prototype Control Probe	Option 3M	$1190
8300P13	8022 Prototype Control Probe	Option 3N	$1190
	Language Products:		
8300G01	Pascal 8080/8085	Option 1P	$1950
8300H01	Modular Development Language; 8080/8085/Z80	Option 1Q	$1000
8300H02	Modular Development Language; 6800/6802	Option 1R	$1000
	Prototype Debug Package:		
8300D15	8086 Prototype Debug Support	Option 2S	$1650
	System Options:		
8550F01	Real Time Prototype Analyzer	Option 01	$2700
8550F02	32K Static Memory Board	Option 02	$3100
8550	Universal Euro 220V/16A Power	Option A1	NC
8550	U.K. 240V/13A Power	Option A2	NC
8550	Australia 240V/10A Power	Option A3	NC
8550	North American 240V/15A Power	Option A4	NC
8550	115V at 50 Hz	Option 4X	NC
8550	230V at 50 Hz	Option 4Y	NC

	Peripherals	
LP8200	Line Printer Option 4W 220 V at 50 Hz	$3765
4024	Computer Display Terminal with Option 20*	$3450
4025	Computer Display Terminal with Option 20*	$4050
	*Option 20 (8K bytes Display Memory) is required for proper 8001/8002A operation	
	Accessories	
RS232	Interconnecting cable 012-0757-00 (10 feet — 300 cm)	$ 100
Null-Modem	Interconnecting cable 012-0820-00 (5 feet — 150 cm)	$ 80

*Order the products as 8001 or 8550 options to have the system factory configured and tested.

8002A Microprocessor Lab (includes 32K Program Memory) — $10,950

Field Number		Factory Configuration Number*	Price
8002F01	8080A Assembler Software Support	Option 01	+$ 850
8002F1A	MDL/8080A/8085A Software Support (requires 64K Program Memory & Option 01 or 05)	Option 1A	+$1000
8002F02	6800 Assembler Software Support	Option 02	+$ 850
8002F2A	MDL/6800 Software Support (requires 64K Program Memory & Option 02)	Option 2A	+$1000
8002F03	Z80A Assembler Software Support	Option 03	+$ 850
8002F3A	MDL/8080A/Z80A Software Support (requires 64K Program Memory & Option 03)	Option 3A	+$1000
8002F04	TMS9900 Assembler Software Support	Option 04	+$ 850
8002F05	8085A Assembler Software Support	Option 05	+$ 850
8002F06	F8/3870/3872 Assembler Software Support	Option 06	+$ 850
8002F07	1802 Assembler Software Support	Option 07	+$ 850
8002F08	8048/8021 Assembler Software Support	Option 08	+$ 850
8002F09	6500/1 Assembler	Option 09	+$ 850
8002F13	8086/8088 Assembler	Option 13	+$ 950
8002F14	Z8000 Assembler	Option 14	+$ 950
8002F15	68000 Assembler	Option 15	+$ 950
8002F16	8080A Emulator Support	Option 16	+$2350
8002F17	6800 Emulator Support	Option 17	+$2350
8002F18	Z80A Emulator Support	Option 18	+$2350
8002F19	TMS9900 Emulator Support	Option 19	+$2600
8002F20	8085A Emulator Support	Option 20	+$2350
8002F21	F8/3870/3872 Emulator Support	Option 21	+$2850
8002F22	1802 Emulator Support	Option 22	+$2850
8002F23	8048/8021 Emulator Support	Option 23	+$2350
8002F24	6500/1 Emulator Support (Includes Probe)	Option 24	+$3340
8002F28	8086 Prototype Debug Support	Option 28	+$1650
8002F29	Z8000 Prototype Debug Support	Option 29	+$1650
8002F30	68000 Prototype Debug Support	Option 30	+$1650
8002F31	8080A Prototype Control Probe	Option 31	+$ 990
8002F32	6800 Prototype Control Probe	Option 32	+$ 990
8002F33	Z80A Prototype Control Probe	Option 33	+$ 990
8002F34	TMS9900 Prototype Control Probe	Option 34	+$1160
8002F35	8085A Prototype Control Probe	Option 35	+$ 990
8002F36	3870/3872 Prototype Control Probe	Option 36	+$ 990
8002F37	F8 Prototype Control Probe	Option 37	+$ 990
8002F38	1802 Prototype Control Probe	Option 38	+$ 990
8002F39	6802 Prototype Control Probe	Option 39	+$ 990
8002F40	8048 Prototype Control Probe	Option 40	+$1190
8002F41	8021 Prototype Control Probe Adapter (requires Option 40)	Option 41	+$ 350
8002F42	8041A Prototype Control Probe	Option 42	+$1190
8002F43	8022 Prototype Control Probe	Option 43	+$1190
	32K Program Memory Modules	Option 45	+$3100
8002F46	Real-Time Prototype Analyzer	Option 46	+$2700
8002F48	2704/2708 PROM Programmer	Option 48	+$ 650
8002F49	16K Program Memory Module	Option 49	+$1550

ORDER MATRIX
8002A

Processor	Assembler	Emulator	Probe	HLL	Prototype Debug
8080	Option 01	Option 16	Option 31	Option 1A	
8085	Option 05	Option 20	Option 35	Option 1A	
Z80	Option 03	Option 18	Option 33	Option 3A	
6800	Option 02	Option 17	Option 32	Option 2A	
6802/08	Option 02	Option 17	Option 39	Option 2A	
TMS9900	Option 04	Option 19	Option 34		
3870/72/74/76	Option 06	Option 21	Option 36		
F8	Option 06	Option 21	Option 37		
1802	Option 07	Option 22	Option 38		
8048/8035/8039-6	Option 08	Option 23	Option 40		
8021	Option 08	Option 23	Option 41*		
8041A	Option 08	Option 23	Option 42		
8022	Option 08	Option 23	Option 43		
6500/1	Option 09	Option 24**			
8086	Option 13				Option 28
Z8000	Option 14				Option 29
68000	Option 15				Option 30

*Requires Option 40 **Includes Probe

ORDER MATRIX

To use the matrix below:

A) Identify the mainframe (8001 or 8550).
B) Select a processor (8080, 8085, Z80, 6800, etc.).
C) Select a level of support (assembler, emulator, probe, HLL, Prototype Debug).
D) Order mainframe and options for deemed level of support.*

	8001		8550			
Processor	Emulator Probe	Assembler	Emulator	Probe	HLL	Prototype Debug
8080	Option 01	Option 1A	Option 2A	Option 3A	Option 1P	
8085	Option 05	Option 1A	Option 2E	Option 3F	Option 1Q	
Z80	Option 03	Option 1C	Option 2C	Option 3D	Option 1P	
6800	Option 02	Option 1B	Option 2B	Option 3B	Option 1Q	
6802/08	Option 2B	Option 1B	Option 2B	Option 3C	Option 1P	
TMS9900	Option 04	Option 1D	Option 2D	Option 3E	Option 1Q	
3870/72/74/76	Option 06	Option 1E	Option 2F	Option 3G	Option 1R	
F8	Option 07	Option 1E	Option 2F	Option 3H	Option 1R	
1802	Option 08	Option 1F	Option 2G	Option 3J		
8048/8035/8039-6	Option 09	Option 1G	Option 2H	Option 3K		
8021	Option 11[1]	Option 1G	Option 2H	Option 3L[3]		
8041A	Option 12[2]	Option 1G	Option 2H	Option 3M		
8022	Option 13[2]	Option 1G	Option 2H	Option 3N		
6500/1	Option 14	Option 1H	Option 2J[4]			
8086	Not Available	Option 1J				Option 2S
Z8000	Not Available	Option 1K				
68000	Not Available	Option 1L				

[1]Requires Option 09 and 10 [2]Requires Option 10 [3]Requires Option 3K [4]Includes Probe

*NOTE: If this support is to be added to a previously purchased mainframe, use the equivalent product nomenclature, i.e., FIELD NUMBER (**NOT** the factory configuration option number) when placing your order.