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Tektronix®

4924

**DIGITAL CARTRIDGE
TAPE DRIVE**

SERVICE MANUAL



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4924
**DIGITAL CARTRIDGE
TAPE DRIVE**

SERVICE MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

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Fig. 1-1. 4924 Digital Cartridge Tape Drive.

Section 1

GENERAL DESCRIPTION

The 4924 Digital Cartridge Tape Drive (Fig. 1-1) is a programmable digital tape recorder, designed especially for use as an auxiliary tape unit for the Tektronix 4051 Graphic System. It may also be used as an auxiliary storage device for other systems which employ the IEEE Standard Digital Interface for Programmable Instrumentation, described in IEEE Standard 488-1975. (Such systems are characterized by the use of a standardized General Purpose Interface Bus (GPIB) for exchange of data and commands among several "talkers", "listeners", and "controllers".)

There are two basic configurations for the 4924: the standard, which receives its commands over the GPIB as "secondary addresses", and Option 37. Instruments equipped with Option 37 may also receive their commands over the GPIB in an "Alternate" format which does not use secondary addresses.

SWITCHES AND INDICATORS

On the front panel of the 4924 (Fig. 1-2) are seven switches and five LED indicators. The POWER switch is an on-off switch for the connection to the power mains. The red ON LINE switch is used to select between the options of controlling the 4924 by commands sent to it over the GPIB and of controlling the 4924 manually, by use of the other switches on the front panel. The other five switches, and the indicator lights above them, are used only when the 4924 is being controlled manually (not ON LINE); their functions are described later, under "Manual Operation".

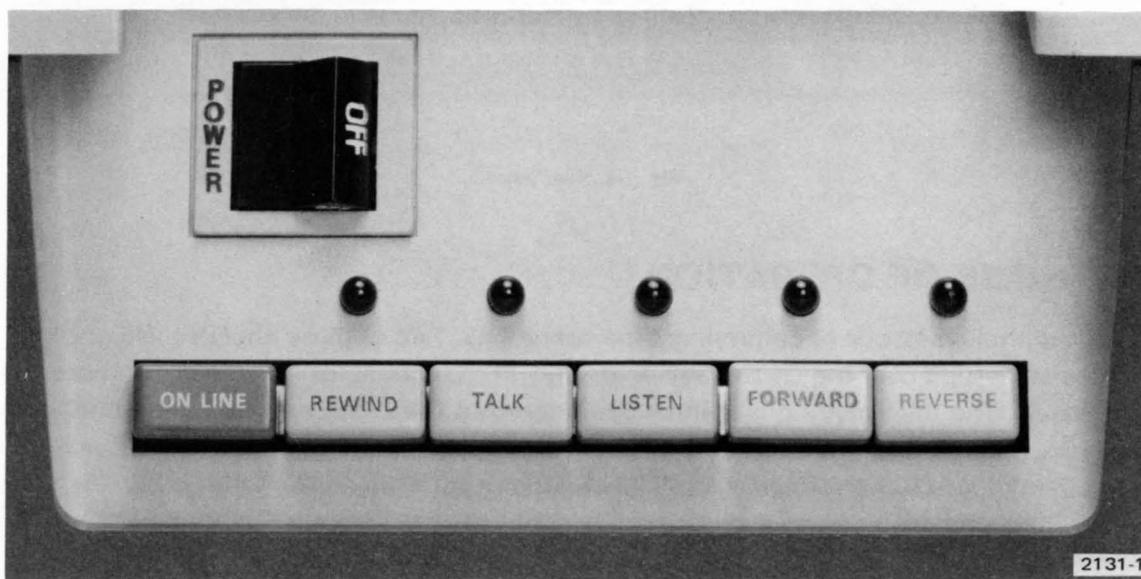


Fig. 1-2. Front Panel Switches and Indicators.

General Description

In the lower left part of the rear panel (Fig. 1-3) are eight miniature rocker switches mounted in one dual-in-line package. Of these, the top five are the GPIB ADDRESS switches; they are used to select the device address (or addresses) by which the 4924 is addressed over the GPIB. The other three switches are the ALT-4051 switch and the two MODE switches, SW1 and SW2; their function is described below, under "Manual Operation".

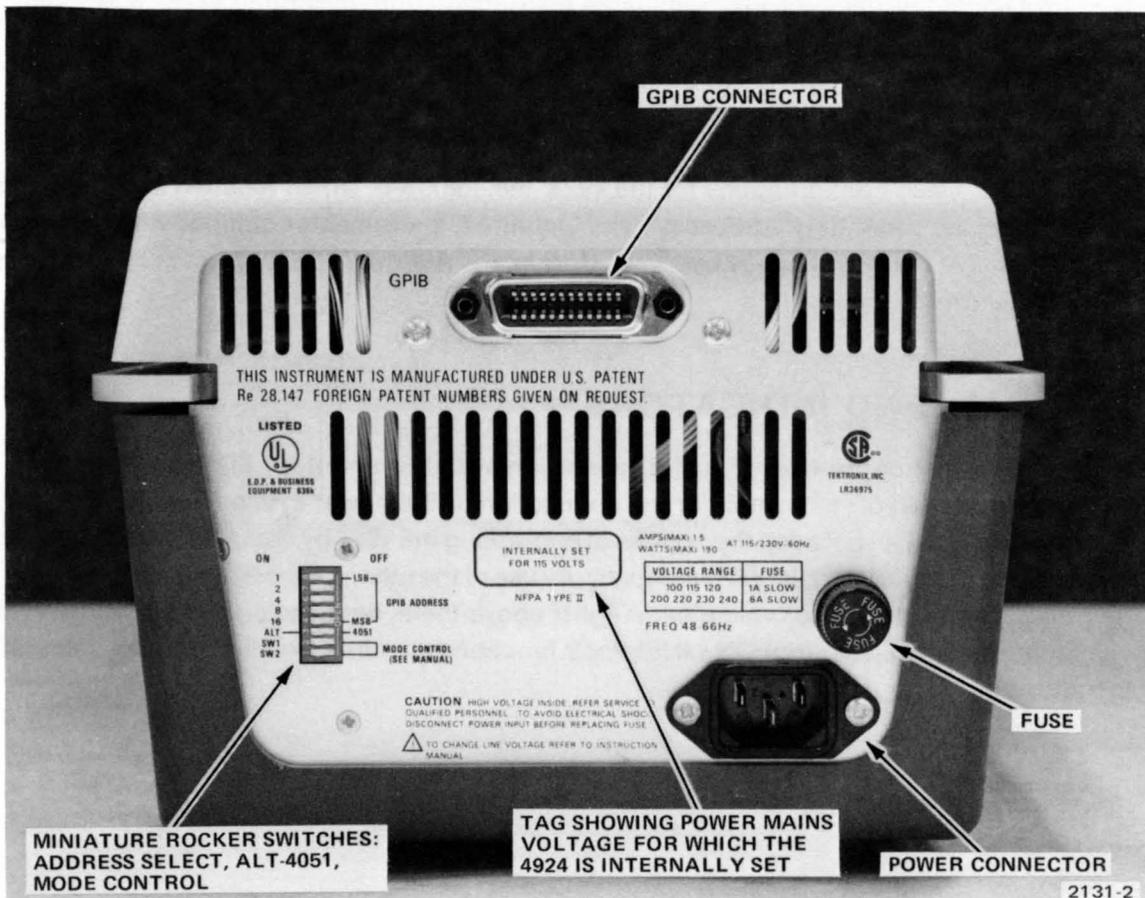


Fig. 1-3. Rear Panel.

METHODS OF OPERATION

There are three methods of controlling tape operations. Two of these are ON LINE and use commands issued over the GPIB; they differ only in the format, or "protocol", of these commands. The third method is manual operation (not ON LINE) and uses the front panel switches, rather than signals from the GPIB, to command the 4924; this permits a few basic tape operations to be performed without the need for a controller unit on the GPIB. The three control methods are:

1. Program-controlled operation using primary and secondary addresses (4051 Mode);
2. Program-controlled operation using primary addresses and command verbs (Alternate Mode, available only on Option 37); and
3. Manual operation.

NOTE

If the manual operating mode is used, it is essential that the tape cartridge be already marked off into files and records. This may be done with the cartridge inserted in another machine, such as the 4051 Graphic System, or by the 4924 while operating under program control.

Selection of the operating method is made by settings of the front panel ON LINE switch and of the rear-panel switches.

4051 MODE

When the 4924 is serving as an auxiliary tape unit for the Tektronix Model 4051 Graphic System, the 4051 mode of program-controlled operation is used. In this mode, the 4924 conforms with the 4051's way of addressing its peripheral devices using two addresses: a "primary address" specifying the particular device, and a "secondary address" which specifies the command which that device is to obey.¹

Selecting the 4051 Mode

To select the 4051 mode of program-controlled operation:

1. Depress the red ON LINE switch on the front panel.
2. If the 4924 is equipped with Option 37, set the ALT-4051 switch on the rear panel to 4051. This is the third switch from the bottom of the eight miniature rocker switches in the lower left part of the rear panel (Fig. 1-3). On standard 4924's (not equipped with Option 37) it is not necessary to set this switch.
3. Choose a "device address"¹ in the range from 1 to 30 for the 4924, and encode it as a binary number, using the GPIB ADDRESS switches. These are the five uppermost of the miniature rocker switches just mentioned (Fig. 1-3).

¹The term "address" is used in a variety of ways in this manual. When in doubt about the meaning of that word, or any word, look in the Glossary (Appendix A).

Controlling the 4924 from the 4051

When using the 4051 to control the 4924, the user need not be concerned with the details of just which bytes are sent over the GPIB to control the 4924; the 4051 will automatically take care of those details. (However, if a different GPIB controller is used, then the user must program that controller so that it sends the correct sequence of bytes over the GPIB).

To illustrate the procedure, assume that device address 2 has been set into the 4924's GPIB ADDRESS switches. To command the 4924 to find the fifteenth file on the tape and position the beginning of that file at its read/write head, enter the following BASIC statement from the 4051 keyboard:

```
FIND @2:15
```

and depress the 4051's RETURN key. The 4051 will automatically send the proper commands to the 4924 over the GPIB. The 4924 responds by moving the tape in its cartridge until the beginning of the fifteenth tape file is under its read/write head.

For details of the syntax of the 4051 Graphic System's BASIC statements, refer to the 4051 Graphic System Reference Manual, Tektronix Part Number 070-2056-01. For a description of the function of each of the commands understood by the 4924, see the 4924 Operators Manual, Tektronix Part Number 070-2128-00. In Appendix B of this manual there is a table of examples of how to command the 4924 to perform each of its various functions.

Controlling the 4924 from the GPIB

Whether the 4924 is operating under control of a 4051, or some other controller, it receives its commands over the General Purpose Interface Bus (GPIB). The GPIB is described in more detail in Section 4; but for the present discussion the most important facts about it are these:

1. Groups of eight binary bits (bytes) may be sent over the GPIB's "data bus".
2. The GPIB includes an EOI line that may be used by the "talker", when sending a string of bytes over the data bus, to mark the last byte in the string.
3. The controller may use the GPIB's ATN (attention!) line to send the ATN message to devices connected to the GPIB. The ATN message causes all the devices to pay attention to the byte which the GPIB controller is sending on the GPIB's data bus, as that byte may represent a "universal command", a "primary address" or a "secondary address".

When a device address has been set into the 4924's rear-panel GPIB ADDRESS switches, the 4924 will recognize two different "primary address" bytes sent by the controller with ATN active. These are the 4924's "primary talk address" and its "primary listen address". The primary talk address is used to address the 4924 when it is to transmit data out over the GPIB; the primary listen address is used when the 4924 will be accepting data sent to it over the GPIB.

These addresses are detailed in Table 1-1, and in a similar table in Appendix C. The table lists the addresses in their binary form, the way they would be sent over the GPIB.

Table 1-1
GPIB PRIMARY ADDRESSES

Decimal Device Address Chosen for the 4924	Position of GPIB ADDRESS Switches 16 8 4 2 1	Primary Listen Address		Primary Talk Address	
		Constant	Switch Selected	Constant	Switch Selected
0 ²	-----	0 0 1	0 0 0 0 0	0 1 0	0 0 0 0 0
1	0 0 0 0 1	0 0 1	0 0 0 0 1	0 1 0	0 0 0 0 1
2	0 0 0 1 0	0 0 1	0 0 0 1 0	0 1 0	0 0 0 1 0
3	0 0 0 1 1	0 0 1	0 0 0 1 1	0 1 0	0 0 0 1 1
.
.
.
n	b ₅ b ₄ b ₃ b ₂ b ₁	0 0 1	b ₅ b ₄ b ₃ b ₂ b ₁	0 1 0	b ₅ b ₄ b ₃ b ₂ b ₁
.
.
.
29	1 1 1 0 1	0 0 1	1 1 1 0 1	0 1 0	1 1 1 0 1
30	1 1 1 1 0	0 0 1	1 1 1 1 0	0 1 0	1 1 1 1 0
31 ²	-----	0 0 1	1 1 1 1 1	0 1 0	1 1 1 1 1

Device addresses 0 and 31 may not be used for the 4924. Device address 0 is reserved by the 4051 for future use. Device address 31 is used for the UNTALK and UNLISTEN commands.

For each device address n, its representation as a binary numeral, b₅b₄b₃b₂b₁ is included in the binary talk address, 0 1 0 b₅b₄b₃b₂b₁ and the binary listen address, 0 1 0 b₅b₄b₃b₂b₁.

To command the 4924 when it is in 4051 mode, the GPIB controller activates the GPIB's ATN line and sends two bytes over the GPIB data bus: the 4924's primary talk or listen address, and a secondary address which constitutes a command to the 4924. The secondary addresses recognized by the 4924 are listed in Table 1-2, and in a similar table in the Appendix. For a more complete description of the function of these commands, see the 4924 Operators Manual (Tektronix Part Number 070-2128-00) and the 4051 Graphic System Reference Manual (Tektronix Part Number 070-2056-01).

To illustrate the procedure, assume that the 4924 is to be commanded to find the fifteenth file on the tape, and then to transmit the contents of that file in ASCII format to another device on the GPIB (which also uses the 4051's method of receiving its commands as secondary addresses).

General Description

First, the GPIB controller activates the ATN line. With ATN active, it transmits the primary listen address corresponding to the device address selected on the 4924's GPIB ADDRESS switches. For instance, if 16 has been selected on those switches, the primary listen address is binary 00110000. (See Appendix C for tables of primary and secondary addresses, and of ASCII characters.) The controller then sends the secondary address for the FIND command, binary 01111011. After sending these two bytes, it releases ATN and sends the ASCII string for the file number (15): 00110001, 00110101. It marks the end of the string by sending the ASCII carriage return character, or, alternatively, by activating the EOI line as the last byte of the string is sent.

Table 1-2
4051 MODE SECONDARY ADDRESSES

4051 GS Secondary Address	Command	Byte Sent Over GPIB
0	"STATUS"	0 1 1 0 0 0 0 0
1	SAVE	0 1 1 0 0 0 0 1
2	CLOSE ³	0 1 1 0 0 0 1 0
4	OLD/APPEND	0 1 1 0 0 1 0 0
6	"TYPE"	0 1 1 0 0 1 1 0
7	KILL	0 1 1 0 0 1 1 1
9	"HEADER"	0 1 1 0 1 0 0 1
12	PRINT	0 1 1 0 1 1 0 0
13	INPUT	0 1 1 0 1 1 0 1
14	READ	0 1 1 0 1 1 1 0
15	WRITE	0 1 1 0 1 1 1 1
24	"READ ERRORS"	0 1 1 1 1 0 0 0
25	"LISTEN"	0 1 1 1 1 0 0 1
26	"TALK"	0 1 1 1 1 0 1 0
27	FIND	0 1 1 1 1 0 1 1
28	MARK	0 1 1 1 1 1 0 0
29	SECRET	0 1 1 1 1 1 0 1
30	"ERROR"	0 1 1 1 1 1 1 0

NOTE: Commands whose names are given within quotation marks (for instance, "STATUS") are commands for which no 4051 BASIC keyword exists.

The 4924 has now received its primary listen address, a secondary address for the FIND command, and the parameter 15; it obeys the command by searching for tape file 15 and positioning its read/write head at the beginning of that file.

Next, the controller activates the ATN line and addresses the 4924 at its primary talk address (binary 01010000), followed by the secondary address for the INPUT command (01101101).⁴It

³Not a 4924 keyword.

⁴Despite its name, the INPUT command causes the 4924 to send data out over the GPIB. This command gets its name from the 4051's BASIC keyword "INPUT" by which the 4051 may be instructed to cause external devices such as the 4924 to send ASCII character strings to it.

then addresses the other device on the GPIB (which is to receive the data string from the 4924) at its primary listen address, followed by a secondary address to command that device to receive the ASCII string which the 4924 will be sending. After sending these four bytes (4924's primary and secondary addresses, other device's primary and secondary addresses), it then releases the ATN line.

The 4924 and the "listener" device then perform the specified operation. The 4924 reads ASCII characters from the tape file and transmits them (over the GPIB data bus) to the other device. The GPIB controller may interrupt the data transfer by activating the ATN line and sending the UNTALK and UNLISTEN commands. If the operation is not interrupted before the last byte in the file is reached, the 4924 activates the EOI line as that last byte is transmitted, signalling the end of the data string to the listener and to the GPIB controller.

The following is a summary of the GPIB activity just described. In the summary, each phrase within parentheses represents a byte sent over the GPIB. An underscore below a byte indicates that ATN is active during that byte's transmission. These abbreviations are used:

MTA (my talk address) for the 4924's primary talk address;
 MLA (my listen address) for the 4924's primary listen address; and
 MSA (my secondary address) for a secondary address.

1. The controller sends: "(MLA),(MSA for the FIND command), (1),(5),(CR), (UNLISTEN);"

or, alternatively, the controller may signal the end of the string of ASCII characters by activating the EOI line: "(MLA),(MSA for the FIND command),(1),(5 sent with EOI active),(UNLISTEN)."

2. The 4924 finds file 15 on the tape.

3. The controller sends: "(MLA),(MSA for the INPUT command),(listener's primary listen address),(listener's secondary address to command it to listen)."

4. The 4924 sends: "(ASCII character),. . . , (ASCII character), (ASCII character with EOI active)."

5. The controller sends: "(UNTALK),(UNLISTEN)."

ALTERNATE MODE (For Option 37 Machines)

Those 4924's which are equipped with Option 37 have the capability of receiving their commands over the GPIB in an alternate format which does not involve the use of secondary addresses. This is described in the following paragraphs.

Selecting the Alternate Mode

To select the Alternate mode of program-controlled operation in a 4924 equipped with Option 37:

1. Depress the red ON LINE switch on the front panel.
2. Set the ALT-4051 switch (on the rear panel) to ALT. This is the third switch from the bottom of the eight miniature rocker switches in the lower left part of the rear panel.
3. Choose two "device addresses" in the range from 2 to 29 for the 4924. One device address, the DPA (data primary address), must be an even number; the other device address, the CPA (command primary address), must be the odd number just one greater than the DPA. Set the GPIB ADDRESS switches (on the rear panel) to represent either of these two device addresses. It does not matter which of the two addresses is set in the switches, as they differ only in the least significant bit (LSB) and the switch for that bit is ignored by the 4924 in Alternate mode.

Giving Alternate Mode Commands from the 4051

Although the Alternate mode is intended primarily to allow the 4924 to be used with other GPIB controllers, the 4051 can be used to command the 4924 in Alternate mode. Using the 4051 to issue commands has the advantage that the 4051 will automatically issue the correct GPIB byte sequence to control the 4924.

Although the 4051 automatically issues both primary and secondary addresses when communicating with device on the GPIB, in Alternate mode the 4924 uses only primary addresses and ignores any secondary addresses sent by the 4051.

Commands are sent to the 4924 in Alternate mode by sending its Command Primary Address (CPA) with ATN active, followed by a string of ASCII characters (the "command string"), ending with the universal UNLISTEN command (sent with ATN active). This may be accomplished from the 4051 keyboard by using the BASIC "PRINT" command. For instance, if 2 and 3 have been set as the 4924's device addresses (DPA=2, CPA=3), to command the 4924 to find the fifteenth tape file, enter

```
PRINT @3:"F=15"
```

and depress the 4051's RETURN key. The 4051 will automatically issue the correct sequence of bytes over the GPIB, and the 4924 will respond by moving its tape until the fifteenth tape file is positioned at its read/write head.

In the example, the "F=15" in the BASIC statement caused the 4051 to issue the ASCII command string "F","=","1","5","CR". Other command strings are possible. For example, the

BASIC statements

```
PRINT @3: "F?15"
```

or

```
PRINT @3: "FIND 15"
```

would have worked just as well. For details of the syntax of the command strings for the different 4924 commands, refer to the 4924 Operators Manual (Tektronix Part Number 070-2128-00); for syntax of the 4051 BASIC statements, see the 4051 Graphic System Reference Manual (Tektronix Part Number 070-2056-01). Examples of BASIC statements to cause the 4924 to perform various operations are given in Appendix B of this manual.

In the Alternate mode, commands are received by the 4924 at its CPA, but the DPA must be used for sending or receiving data. Therefore, to cause the 4924 to send or receive data, one must first send the command string to the CPA and then, at some later time, address the 4924 at its DPA. When addressed there, the 4924 executes the command.

For instance, to write "This is a test message." at the start of file number three, we might have the 4051 execute this program:

```
100 PRINT @3: "F=3"
110 PRINT @3: "P"
120 PRINT @2: "This is a test message."
```

In this case, statements 100 and 110 address the 4924 at its CPA (3); they command it to find file three and prepare to write ASCII data into that file. Statement 120 addresses the 4924 at its DPA (2); the string of ASCII characters sent to the 4924 by this statement is treated as data to be recorded on the tape.

Refer to Appendix B for other examples of 4051 BASIC statements which may be used to command the 4924 in Alternate mode.

Sending Alternate Mode Commands over the GPIB

In Alternate mode as well as in 4051 mode, the 4924 receives its commands over the GPIB. The GPIB is described in more detail in Section 4, but for this discussion it suffices to know these facts:

1. The controller or the 4924 may send groups of eight binary bits (bytes) over the GPIB's data bus.

General Description

2. The controller may activate an ATN (attention!) line in the GPIB to cause the 4924 (and other devices on the GPIB) to examine the byte being sent by the controller on the GPIB's data bus to see if it is a primary or secondary address or a "universal command".
3. A "talker" sending a string of bytes on the GPIB data bus may mark the last byte in the string by activating an EOI (End or Identify) line in the GPIB.

In Alternate mode, the 4924 recognizes as its addresses four different bytes (sent by the controller with ATN active). Two of these bytes are the "talk" and "listen" addresses corresponding to the Command Primary Address, and two are the "talk" and "listen" addresses for the Data Primary Address. Thus, the 4924 recognizes four "primary addresses": the Command Primary Listen Address (CPLA), the Command Primary Talk Address (CPTA), the Data Primary Listen Address (DPLA), and the Data Primary Talk Address (DPTA).

To command the 4924, the GPIB controller sends the 4924's Command Primary Listen Address (CPLA), and then sends a string of ASCII characters. For instance, to make the 4924 search for the fifteenth file on the tape, the controller could send the string "FIND 15" or the string "F=15". (The formats of the command strings for different commands are detailed in the 4924 Operators Manual, Tektronix Part Number 070-2128-00). The end of the command string is marked by an ASCII carriage return character or by activating EOI as the last character is sent. The controller must then send the universal command UNLISTEN; this is necessary to cause the 4924 to empty its input buffer and examine the character string it has just received.

To cause the 4924 to send or receive data, the controller sends the 4924's Command Primary Listen Address, an ASCII string constituting the command, and then the UNLISTEN command. This "sets up" the command in the 4924. Later, the controller sends the 4924's Data Primary Listen Address (to "listen") or its Data Primary Talk Address (to "talk"). This triggers the 4924 to execute the command. After the data transfer is complete, the controller must send UNLISTEN or UNTALK.

To illustrate the procedure, assume that the 4924 is to find the fifteenth tape file and transmit the contents of that file (in ASCII format) to another device on the GPIB. For simplicity, assume that the second device takes its commands as secondary addresses.

First, the GPIB controller pulls the ATN line active low and transmits the 4924's Command Primary Listen Address (CPLA). It then releases ATN and sends a string of ASCII characters, such as "F", "=", "1", "5", "CR". The string may end with the carriage return character (CR), or its end may be marked by activating EOI as the last character is sent. The controller then activates ATN and sends UNLISTEN to force the 4924 to empty its input buffer and examine the character string.

The 4924 then searches for file number 15 and positions the start of that file at its read/write head.

Next, the controller activates ATN and sends the 4924's Command Primary Listen Address (CPLA) again. It releases ATN and sends another ASCII string, such as "I", "N", "P", "U", "T", "CR". After the command string, the controller activates ATN and sends the universal command UNLISTEN.

This "sets up" the INPUT command in the 4924.

The GPIB controller then activates ATN and sends the Primary Listen Address of the device which is to "listen" to the ASCII output of the 4924. With ATN still active, the controller sends the secondary address which commands the listener to receive an ASCII character string.

With ATN still active, the controller transmits the 4924's Data Primary Talk Address (DPTA). It then releases the ATN line.

As ATN is released, the 4924 and the listener each execute their commands. The 4924 reads the ASCII characters from the tape and sends them out over the GPIB data bus. The listener accepts the string of characters sent by the 4924. At the end of the file, the 4924 activates EOI as it sends the last ASCII character; this signals the end of the string to the listener and to the controller.

This sequence of bytes is summarized below. In the summary, each phrase within parentheses represents a byte sent over the GPIB. An underscore below a byte indicates that ATN is active during transmission of that byte.

1. The controller sends: "(CPLA),(F),(=),(1),(5),(CR),(UNLISTEN)";

or, alternatively, it may mark the end of the ASCII string by asserting EOI:

"(CPLA), (F),(=),(1),(5—with EOI active),(UNLISTEN)".

2. The 4924 finds file 15 on the tape.

3. The controller sends: "(CPLA),(I),(N),(P),(U),(T),(CR),(UNLISTEN)."

4. The 4924 sets up the INPUT command for later execution.

5. The controllers sends: "(Listener's primary listen address), (Listener's secondary address to command it to receive ASCII characters),(DPTA)".

6. The 4924 reads bytes from file 15 and sends them to the listener. It sends: "(ASCII character), ..., (ASCII character), (ASCII character—with EOI active)".

7. The controller sends: "(UNTALK), (UNLISTEN)".

General Description

As commands are sent to the CPLA, and data to be written on or read from the tape is sent to the DPLA or from the DPTA, one might suppose that the CPTA (Command Primary Talk Address) is unused. However, a few commands do use this address: These are the ERROR, TYPE, HEADER, and READ STATUS commands. When one of these commands has been set up in the 4924, and it is then addressed at the CPTA, the 4924 will issue a string of ASCII characters which represent, not data from the tape, but other information—such as an error code or the status of the 4924's Programmable Option Status Byte.

Example:

1. The controller sends: "(CPLA), (E), (CR), (UNLISTEN)".
2. The 4924 sets up the ERROR command for later execution.
3. The controller sends: "(CPTA)".
4. The 4924 sends an ASCII character string representing an error code. For instance, it might send "(1),(2),(CR)".
5. The controller sends: "(UNTALK)".

MANUAL OPERATION

The Manual operating mode is intended primarily to provide some limited off-line data logging capability. It is also useful in servicing the machine, as it allows the unit to be exercised without being connected to the 4051 or another GPIB controller.

For the 4924 to operate properly in this mode, the tape cartridge inserted into it must already have files and records marked, as described in Section 2 under "Tape Format". This can be done with the cartridge inserted into another machine, such as the 4051, or may be done by the 4924 while operating under program control (ON LINE).

To select manual operation, release the red ON LINE switch on the front panel.

NOTE

Releasing this switch does not disconnect the 4924 from the GPIB. It enables the front panel switches and some of the rear panel switches. With the ON LINE switch released the GPIB is used to transfer data between the 4924 and other devices but the 4924's commands are provided by the switches.

Front Panel Switches

The REWIND switch, when pressed, causes the 4924 to rewind the tape. The LED indicator above the switch will be on until the tape is rewound. Any open file will be closed (that is, a logical end-of-file mark, hexadecimal FF, written into it). If the tape is already fully rewound, the LED will immediately go out and no tape movement will occur.

The TALK switch, when pressed, causes the unit to transmit the contents of the current file to any device listening on the GPIB. When the last byte in this file is transmitted, the EOI (End or Identify) message is sent over the GPIB and the operation is terminated. The LED indicator above the switch will remain on until the entire file is transmitted, or will go out if no listener is present on the GPIB.

The LISTEN switch, when pressed, puts the 4924 in LISTEN mode. Data sent over the GPIB is written on a file on the tape. As the last byte is reached, an EOI message from the GPIB causes the 4924 to close the file and stop recording data. The LED indicator above the switch will remain on until the file is closed, or will go out if no other devices are on the GPIB.

The FORWARD switch, when pressed, causes the 4924 to perform a "Forward Space File" function. That is, it skips forward (at 90 inches per second) until it finds the next sequential file. Each time the switch is pressed, the tape will skip forward one file, positioning the start of the next file under the tape head. While skipping forward, the unit ignores repeated depressions of the FORWARD switch until the next file is found. Once having stopped at the next file, however, the 4924 will respond to a depression of the FORWARD switch; so, by holding the FORWARD switch down, one may cause the unit to skip forward through several files.

The internal program controlling the 4924 during this "skip forward" operation depends on the detection of record and file marks on the tape. After the FORWARD button is pressed, the tape runs forward at the normal speed (30 inches per second) until the first record mark is encountered, and then shifts to high speed (90 inches per second). A tape which has not been marked into records and files, such as the calibration tape used for head alignment, will never cause the 4924 to change to the faster speed.

The REVERSE switch, when pressed, causes the 4924 to perform a "Backspace File" function. That is, it skips the tape backward (at 90 inches per second) to find the preceding sequential file. The LED above this switch stays on until the file is found. If the first file on the tape is found, further depressions of this switch will be ignored.

The REVERSE switch does not depend on the detection of record marks for its correct operation. The tape moves backward at high speed (90 inches per second) even with a blank tape or a calibration tape inserted.

MODE Switches

The MODE switches (SW1 and SW2 on the rear panel) determine the state of the "status byte" in manual mode. This byte (in the 4924's internal memory) selects several programmable options concerning the tape format. The two MODE switches provide four possible positions (Table 1-3) to select one of three options: "Programmable Status", "4051 Status", and "4923 Status". Table 1-3 lists the status options selected by the various positions of these two switches.

Table I-3

SETTINGS OF THE REAR-PANEL MODE SWITCHES

SW 1	SW 2	MEANING
OFF	OFF	PROGRAMMABLE STATUS
ON	OFF	4051 STATUS
OFF	ON	4923 STATUS
ON	ON	PROGRAMMABLE STATUS

With MODE switches SW1 and SW2 set to select "Programmable Status", the last Programmable Option Status Byte (as described in Section 2) that was set under program control will prevail in the manual mode.

With SW1 and SW2 set for "4051 Status", the manual mode status byte will be compatible with the 4051 Graphic System. This will set up 256-byte records with checksums and headers. The read-after-write option is not set.

With SW1 and SW2 set for "4923 Status", the manual mode status byte will be compatible with the Tektronix Model 4923 Digital Cartridge Tape Recorder. This will set up 128-byte records without checksums or headers or read-after-write checks.

Section 2

CHARACTERISTICS

POWER REQUIREMENTS

The 4924 can be operated from the power mains of most countries of the world, as its transformer will accept either 50 Hz or 60 Hz alternating current, and may be tapped to operate from a variety of different voltages. The procedure for selecting the particular line voltage is described in Section 3, under "Line Voltage Selection".

CAUTION

The 4924 is intended to be operated from a single-phase power source that has one of its current-carrying conductors (neutral) at ground (earth) potential. Operation from other power sources where both current-carrying conductors are live with respect to ground (such as phase-to-phase on a multiphase system, or across the legs of a 115-230 volt single-phase three-wire system) is not recommended, since only the line conductor has over-current (fuse) protection within the unit.

The power specifications are listed in Table 2-1.

Table 2-1
4924 POWER SPECIFICATIONS

Line voltage selection	Voltage selections ($\pm 10\%$)
115 V (nominal)	100 Vac
Range	115 Vac
	120 Vac
220 Vac (nominal)	200 Vac
Range	220 Vac
	230 Vac
	240 Vac
Power Consumption	62 watts at 115 Vac, 60 Hz
Line Frequency	50 to 60 Hz
Line Fuse	
115 Vac Range	1.0 A slow-blow
220 Vac Range	0.6 A slow-blow

AC POWER CORD AND GROUNDING REQUIREMENTS

This instrument has a detachable three-wire cord with a three-wire polarized plug for connection to the power source and safety earth. The Safety Earth terminal of the plug is directly connected to the instrument frame for electric-shock protection. Insert this plug only in a mating outlet with a safety earth contact or otherwise connect the frame of the unit to a safety earth system.

WARNING

To avoid electrical shock or equipment damage, be sure to replace the cord set only with another of the same polarity.

Power Cord Conductor Identification

Conductor	Color	Alternate Color
Ungrounded (Line)	Brown	Black
Grounded (Neutral)	Blue	White
Grounding (Earthing)	Green-Yellow	Green-Yellow

See Fig. 2-1 for standard power cords. Use only these cords (Tektronix Part Number 161-0066-00 for 100-120 Vac, Tektronix Part Number 161-0066-01 for 200-240 Vac). In other jurisdictions, replace the standard plug with a plug that satisfies local authorities. For power cord Options A1, A2, A3, A4 (European Power Cord), see Accessories in this manual.

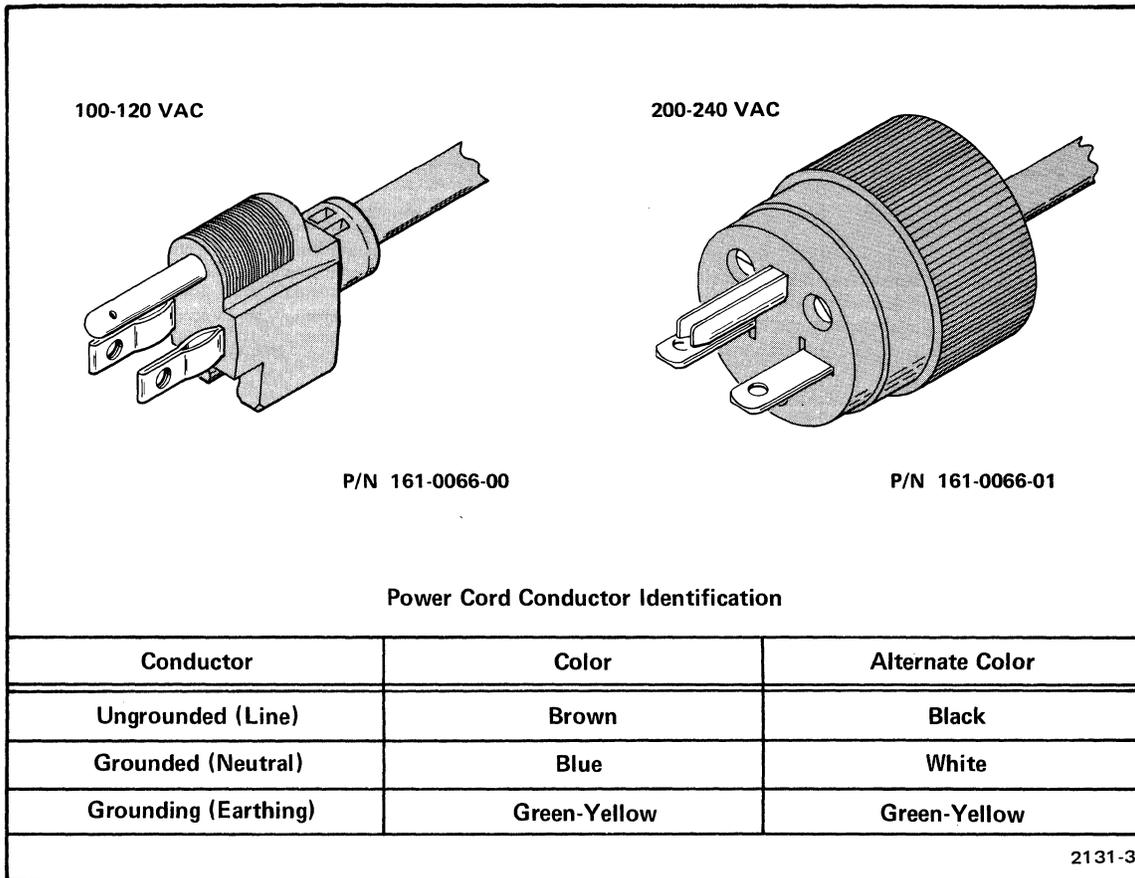


Fig. 2-1. USA Standard Power Cords.

ENVIRONMENTAL REQUIREMENTS

The 4924 will require more frequent maintenance if it is operated in an extremely dusty or dirty environment. Conditions of extreme heat or cold may damage the unit or the tape cartridge. The environmental limitations are detailed in Table 2-2.

Table 2-2
4924 Environmental Specifications

Temperature	
Operation (with tape installed)	10 to 40°C (50 to 104°F)
Storage of 4924	-40 to +65°C (-40 to +149°F)
Storage of Tape cartridge	5 to 45°C (41 to 113°F)
Transportation of tape Cartridge	-40 to +45°C (-40 to +113°F)
Altitude	
Operation	Up to 15,000 feet (4,500 m)
Storage	Up to 50,000 feet (15,000 m)
Humidity limits for tape cartridge	20% to 80%, NON-CONDENSING
Tape cartridge environmental conditioning	The cartridge must be conditioned to the operating environment for a time equal to the time away from the environment, not to exceed 8 hours, and should be rewound before use.

TAPE CARTRIDGE

The 4924 uses the 3M® type DC-300A data cartridge, illustrated in Fig. 2-2. The lower plane of the cartridge (reference plane) is heavy gauge metal; the remainder of the cartridge is high-impact plastic.

The tape in the cartridge does not touch the 4924 drive roller, eliminating the need for cleaning the drive roller. Drive is accomplished by contacting the cartridge drive roller with the rubber-covered drive roller mounted on the 4924 drive motor shaft. The cartridge drive roller causes an internal drive band to move, which, in turn, moves both reels and keeps the tape tension uniform.

Each data cartridge provides 300 feet of usable storage space. Beginning of Tape (BOT), Load Point (LP), Early Warning, and End of Tape (EOT) markers are provided by specially placed holes in the tape. These holes are sensed by a lamp-mirror-phototransistor arrangement. (See Fig. 2-3).

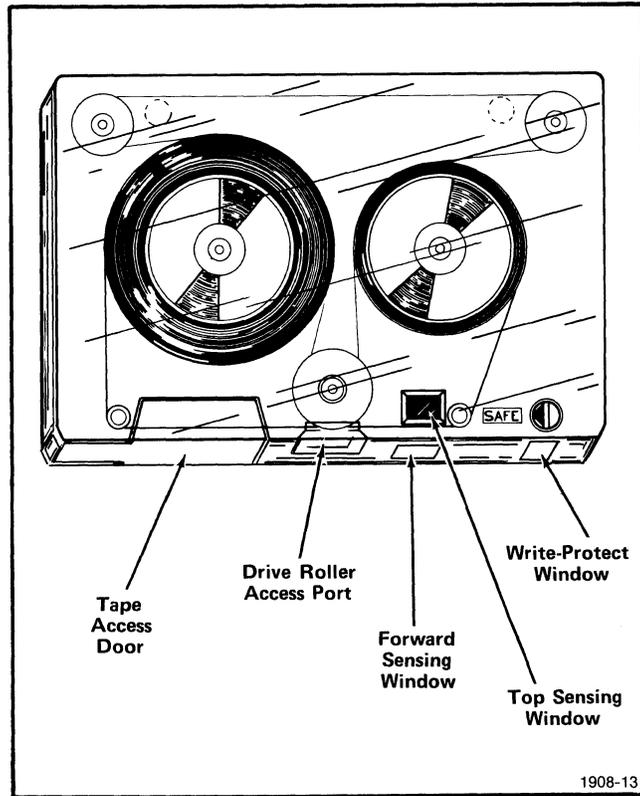


Fig. 2-2. Tape Cartridge Parts.

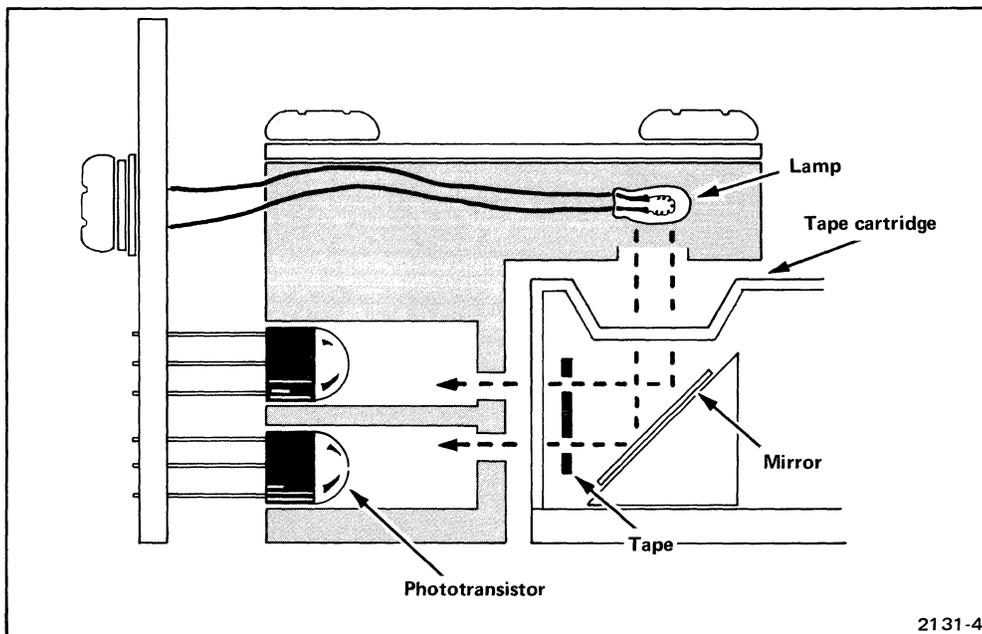


Fig. 2-3. Position Marker Sensing.

TAPE CARTRIDGE MOUNTING CHARACTERISTICS

Cartridge mounting characteristics are shown in Table 2-3. In addition, Fig. 2-4 shows a cartridge in its proper position, with the label edge (back edge) flush with the forward edge of the 4924 frame. The critical mounting positions of the tape transport components are shown on the drawing, with reference to the cartridge in this position.

Table 2-3
Cartridge Mounting Characteristics

Cartridge Mounting	4 point mounting against cartridge base. ¹
Cartridge Latching	Once past the latching point, the cartridge is pulled into position by two latching arms. Tension is maintained by a spring between the two arms.
Cartridge Insertion/Removal Force	45 to 60 ounces.
Switch Mounting	Two micro switches are mounted on the Status bracket to detect cartridge presence and Write-Protection.

¹This mounting is ensured by a cartridge hold-down roller that presses the forward edge of the cartridge down against the forward mounting points within 2 capstan revolutions. This is only necessary if the cartridge is installed at an angle. As with all precision devices, proper cartridge insertion ensures more reliable operation.

TAPE FORMAT

The 4924 records data onto the tape in two tracks (Fig. 2-5); the upper track is the 1 (one) track and the lower track is the 0 (zero) track. The head writes on the tape tracks with direct current in its internal electromagnet, producing regions on the tape which are magnetized with a given magnetic polarity (flux). Each time a reversal of this flux occurs (on either track) it is interpreted as a bit. The bit is a one or a zero, depending on the track on which the flux reversal occurs.

After each eight-bit byte (character), an Inter-Character Gap (ICG) is written (Fig. 2-5). This is a period of three clock periods during which no flux reversals occur. (Within the characters, flux reversals occur at every clock pulse; two flux reversals are omitted from the train to create the ICG.) This NFR (period of no flux reversals) serves as a reset, ensuring that a bit error in one character will affect only that character and not the entire data string.

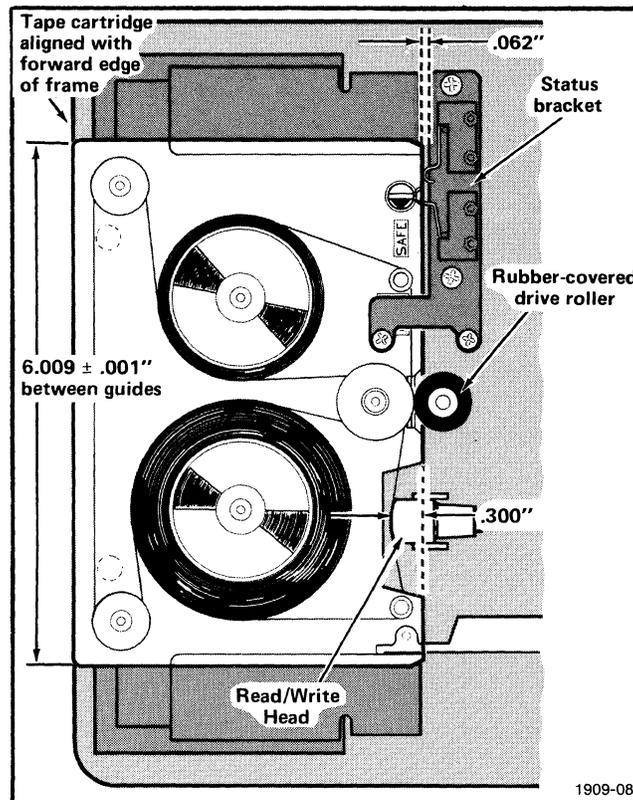
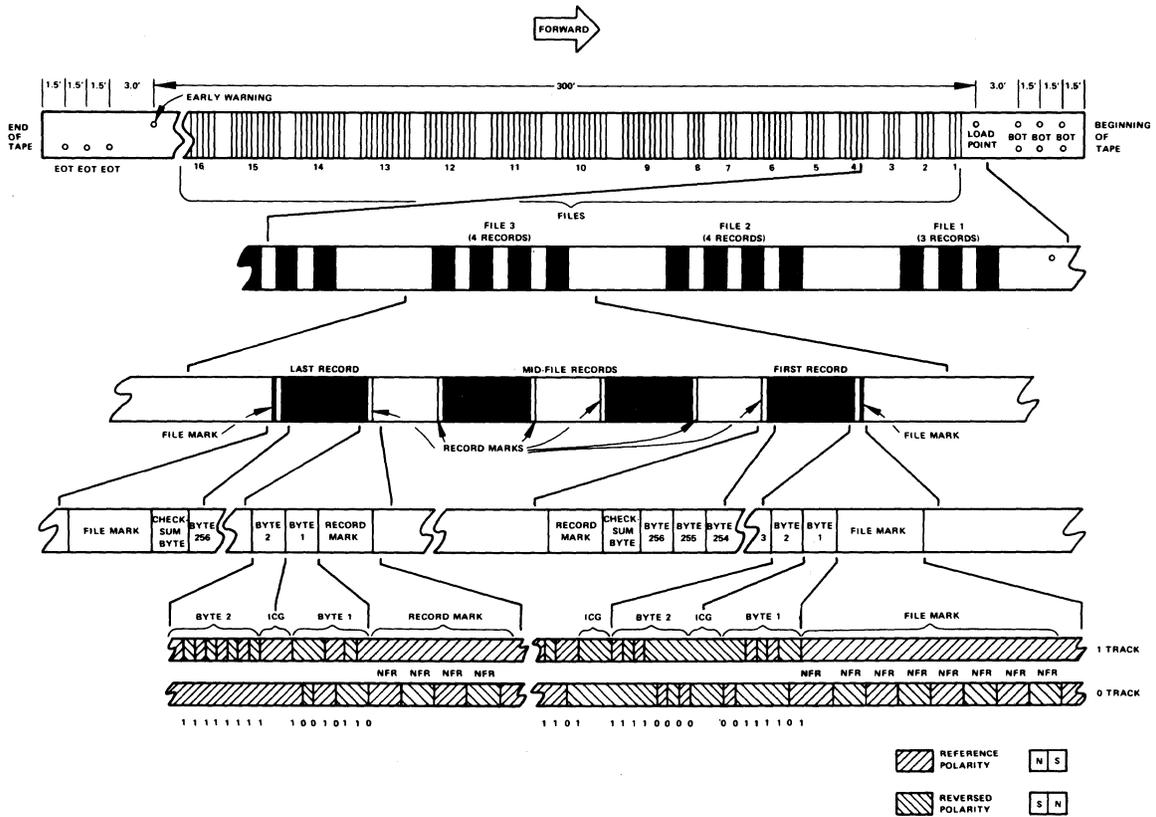


Fig. 2-4. Cartridge Position Dimensions.

Data is recorded in blocks of 128 or 256 characters, called "records". There is a programmable option to insert an extra byte (the "checksum" byte) into each record, to make a total of 129 or 257 bytes per record. The beginning and end of each record is indicated by "record marks" (comprised of four NFRs). Each two NFRs within the record mark are separated by a clock pulse. (This is simply a bit written onto one of the tracks.) Records are separated by Inter-record Gaps — spaces of about 1.2 inches of blank tape.

Records are combined into "files" of data. The length of a file is variable, and is determined by "file marks" at the beginning and end of the file. These file marks replace the record marks at the start of the first record and the end of the last record of the file (Fig. 2-5). They are composed of eight NFRs, making them equivalent to two record marks. Files are separated by Inter-File Gaps of about 3.6 inches of blank tape, equivalent to three Inter-Record Gaps.

Characteristics



2131-5

Fig. 2-5. 4924 Tape Data Format.

HEADERS

There is a programmable option to use the first record of each file as a "header" record. In this record, the first 44 bytes are a string of ASCII characters containing the file number, file type, file usage, whether the file is secret, and the number of records allocated. The remainder of the record is filled with ASCII blanks. The header format is shown in Table 2-4.

**Table 2-4
HEADER RECORD FORMAT**

BYTES	ITEM
1	Space
2-7	File Number
8	Space
9-16	File Type
17-26	File Usage
27-34	Secret
35-42	Records Allocated
43	CR
44	DC3

The "File Number" represents the sequential number of the file from the beginning of the tape. The first file is number 1.

"File Type" can be ASCII, BINARY, NEW or LAST. Refer to the 4051 Graphic System Reference Manual, Tektronix Part Number 070-2056-01, for detailed description of file types.

"File Usage" represents the last usage of the file. This is normally PROGRAM or DATA. Other usages such as LOG or TEXT are possible.

When "SECRET" is written in bytes 27 to 32, the ASCII PROGRAM stored in the file is marked as being secret. Normally, such a program would have been scrambled by the 4051. When the 4051 is to retrieve such a file from the 4924, the 4051 must be informed (by a SECRET command) that the file is secret before retrieving the SECRET program from the 4924. Details of how this is done are found in the 4924 Operators Manual (Tektronix Part Number 070-2128-00). A SECRET file may be APPENDED, but it may not be LISTed and, once retrieved from the 4924 with an APPEND operation, it may not be SAVED.

"Records allocated" is the number of physical records in the file.

NOTE

This can be the actual number of records used or the number of records reserved. It is possible to reserve extra records on the end of the last record used for future revisions or additions. These "blank" records contain ASCII blanks.

BINARY DATA HEADERS

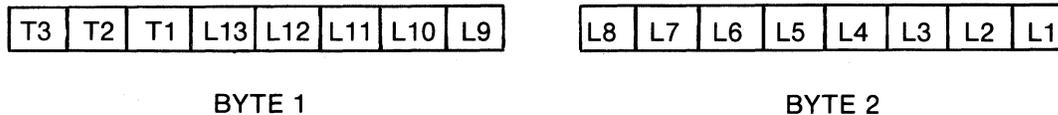
If a tape file is marked as BINARY, then the binary data stored in the following records of the file must be in a special form. Each binary item contains its own header which identifies the length

Characteristics

of the item and the type. This header, which is two bytes long, has a format detailed in Table 2-5:

**Table 2-5
BINARY DATA HEADERS**

The two bytes header is of the form:



T3, T2, T1 define the type of binary data.

L1 to L13 comprise a binary number equal to the number of bytes used to hold the binary item and its header.

T3	T2	T1	Type
0	0	0	Unassigned
0	0	1	Binary value
0	1	0	Binary string
0	1	1	Unassigned
1	0	0	"
1	0	1	"
1	1	0	"
1	1	1	"

TAPE FORMAT SPECIFICATIONS

The tape format specifications are summarized in Table 2-6.

**Table 2-6
RECORDING FORMAT**

RECORDING FORMAT	
Character Format	8-bit serial with LSB (least significant bit) first, MSB (most significant bit) last.
Characters per Record	128 or 256 8-bit bytes with optional following checksum byte. This is programmable in the on-line mode and switch selectable in the manual mode.
Number of Records per File	Variable: a minimum of 3 records per file, maximum of 65,535 records per file.

Maximum number of Files per tape	255
Maximum storage capacity	300K bytes
Tracks	Two data tracks (1's and 0's), combined into one data channel.
Head Type	Single Read/Write head

PROGRAMMABLE OPTION STATUS BYTE

One of the bytes in the 4924's internal memory is reserved for indicating the states of several programmable options. The manual setting of these options when the 4924 is in Manual mode (not ON LINE) was described in Section 1, in the description of the MODE switches, SW1 and SW2.

When the 4924 is operating under the control of the 4051, the state of this byte may be set using the "SET STATUS" command (a PRINT statement with a secondary address of 0). The Programmable Option Status Byte is read using the "READ STATUS" command (an INPUT statement with secondary address of 0.) This is described in the 4924 Operators Manual (Tektronix Part Number 070-2128-00).

The four options whose states are indicated by this byte are:

1. The number of bytes per record (exclusive of a possible checksum byte);
2. Whether a checksum byte is to be included as the last byte of each record;
3. Whether each file is to have a header as its first record; and
4. Whether the read-after-write option is to be used.

If the read-after-write option is chosen, then each time the 4924 writes a record onto the tape, it backs up and reads that record, to check that the record was correctly written. If the record was not correctly written, the 4924 backs up again and re-records that record over the same spot in the tape. If after two tries it still cannot write the record correctly, it generates an error (sets an error code for the ERROR command) and demands service (SRQ) from the GPIB controller.

On power-up, the Programmable Option Status Byte is set for compatibility with the 4051: 256-byte records with checksums and headers and no read-after-write.

ERROR CHECKING

Error checking is provided in the 4924 during Read operations. A combination of hardware and firmware checks for the proper number of bits per byte and bytes per record.

If the "checksum" option is chosen, each time the 4924 reads a physical record from the tape, it computes a "checksum" from the first 256 bytes of the record and compares this checksum with the final "checksum byte." If they do not agree, a "read error" has been detected: the 4924 backs up the tape and tries again to read the record, up to a total of nine rereads (or ten reads). If the data is correctly read, it is transferred out. If, after the maximum number of tries the data still doesn't check, an error flag is set in the serial poll status byte, an error code is set for the ERROR command, and the 4924 demands service of the GPIB controller by activating the SRQ line.

SERIAL POLL

The 4924 has provision to respond to a "serial poll" from the GPIB. The serial poll operation is normally initiated by the GPIB controller in response to a service request (SRQ) sent it by one of the devices on the GPIB.

To determine which device is requesting service, the GPIB controller pulls the ATN line active low and sends the SPE (Serial Poll Enable) universal command to all devices. With ATN still active, it sends the primary talk address of one of the devices on the line; then it lets ATN go inactive high and waits for that device to send back a "status byte" over the GPIB.

The controller sequentially requests the status of each device on the bus. This procedure continues until the device which initiated the SRQ has been found or the controller terminates the sequence.

When the controller has finished the serial poll, it signals this to the 4924 (and the other devices on the GPIB) by sending the universal command SPD (Serial Poll Disable).

The status byte returned by the 4924 in response to a serial poll is described in Table 2-7.

**Table 2-7
SERIAL POLL STATUS BYTE**

The format of the serial poll status byte is:

BIT	8	7	6	5	4	3	2	1
	X	SRQ	ERR	BUSY	ALT	LINE	EOT	EOF

BIT	NAME	FUNCTION
1	EOF	End of File has occurred.
2	EOT	End of Tape has occurred.
3	Line ¹	4924 is on line.
4	Alt ¹	Command switch is in ALT position.
5	Busy	4924 is busy.
6	ERR	An error condition has occurred.
7	SRQ	4924 is requesting service.
8		Unassigned, will not be used.

¹An SRQ will be generated when the unit goes from "on-line" operation to manual operation, or from 4051 command mode to ALT command mode.

On power-up the system is defined to be on-line, in 4051 mode, so an SRQ will be generated if the ON LINE switch is released or the ALT-4051 switch is in ALT position.

TAPE DRIVE CHARACTERISTICS

Characteristics of the 4924's tape driving mechanism are listed in Table 2-8:

Table 2-8

DRIVE CHARACTERISTICS	
Drive Type	Servo-controlled DC motor with tachometer.
Drive Method	Single capstan drive on cartridge drive roller.
Drive Speed	
Normal Read/Write	30 in/sec (76.2 cm/sec) $\pm 7\%$
Skip Forward/Reverse	90 in/sec (228.6 cm/sec) $\pm 10\%$
Fast Forward/Fast Rewind	90 in/sec (228.6 cm/sec) $\pm 10\%$
Start/Stop Time	
Normal Read/Write	25 ms ($\pm 4\%$ at 25° C)
Skip Forward/Reverse	75 ms ($\pm 4\%$ at 25° C)
Fast Forward/Rewind	75 ms ($\pm 10\%$)
Start/Stop Distance	
Normal Read/Write	≈ 0.375 in (≈ 9.5 mm)
Skip Forward/Reverse	≈ 3.375 in (≈ 85.7 mm)
Fast Forward/Rewind	≈ 3.375 in (≈ 85.7 mm)

DC VOLTAGES

Table 2-9 lists the voltages provided by the 4924's power supply.

**Table 2-9
INTERNAL POWER BUS VOLTAGES**

+22 V	Unregulated, 1 A (4 A peak), fused at 3 A fast-blow.
-22 V	Unregulated, 1 A (4 A peak), fused at 3 A fast-blow.
+5.1 V*	Regulated $\pm 1\%$, 2.2 A, fused at 3 A fast-blow.
+12 V*	Regulated, adjustable $\pm 0.5\%$, 50 mA, current limited at 550 mA.
-12 V*	Regulated $\pm 1.5\%$, 150 mA, current limited at 500 mA.
*Ripple	10 mV. (Regulated voltages only)

GPIB FUNCTION SUBSETS

Table 2-10 lists the "interface function subsets" for each of the 4924's programming modes. Refer to IEEE Standard 488-1975 for definitions of these subsets.

**Table 2-10
 GPIB FUNCTION SUBSETS SUPPORTED BY THE 4924**

Interface Function	Subsets Supported		
	4051 Mode	Alternate Mode	Manual Mode
Source Handshake	SH1	SH1	SH1
Acceptor Handshake	AH1	AH1	AH1
Talker	TE6	T6	T3
Listener	LE4	L4	L1
Service Request	SR1	SR1	SR0
Remote Local	RL0	RL0	RL0
Parallel Poll	PP0	PP0	PP0
Device Clear	DC0	DC0	DC0
Device Trigger	DT0	DT0	DT0
Controller	C0	C0	C0

PHYSICAL DIMENSIONS

The physical dimensions of the 4924 Tape Storage Unit are listed in Table 2-11.

**Table 2-11
PHYSICAL DIMENSIONS**

Width	8.75 inches	(22.2 cm)
Depth	17.25 inches	(43.8 cm)
Height	6 inches	(15.2 cm)
Weight	17 pounds	(7.7 kg)

Section 3

SERVICING

This section includes procedures for mechanical disassembly and assembly, removal and replacement of critical parts (such as the Read/Write head), and calibration and adjustment of the electronics.

ROUTINE MAINTENANCE

Occasional cleaning will preserve the appearance of the 4924. Periodic cleaning of the Read/Write head is necessary to remove accumulations of oxide and other foreign matter from the head. Such accumulations can cause read or write errors.

CLEANING THE CASE

To clean the exterior of the 4924, use the following procedure:

1. Turn the power switch off, then disconnect the power cord. Remove the cartridge (if installed).
2. Use a cloth dampened in a mild detergent solution to wash the upper and lower case. Avoid using abrasive cleaners (such as scouring powder) and harsh chemicals.
3. Remove any soap residue with a clean damp cloth and dry the case with a clean dry cloth.
4. Connect the power cord to the power source. The 4924 may again be operated normally.

CLEANING THE TAPE HEAD

The surface of the tape head (Fig. 3-1) must be kept clean to prevent read and write errors. Head life and data reliability are directly related to cartridge and tape head care. Oxide deposits, dust, and other foreign particles may be deposited on the head during operation, causing data errors. In addition, these particles act as abrasives when propelled across the head by tape motion, increasing head wear and reducing head life.

To minimize oxide and foreign matter accumulation, the tape head should be cleaned regularly. Frequency of cleaning depends on use and the cleanliness of the area in which it is used. Tape units with light to moderate use should be cleaned weekly. For heavy use or dusty environments the cleaning schedule should be increased accordingly. Cleaning may be required more frequently if data errors occur (indicated by rapid tape reversal and re-read). To clean the head, use the following procedure:

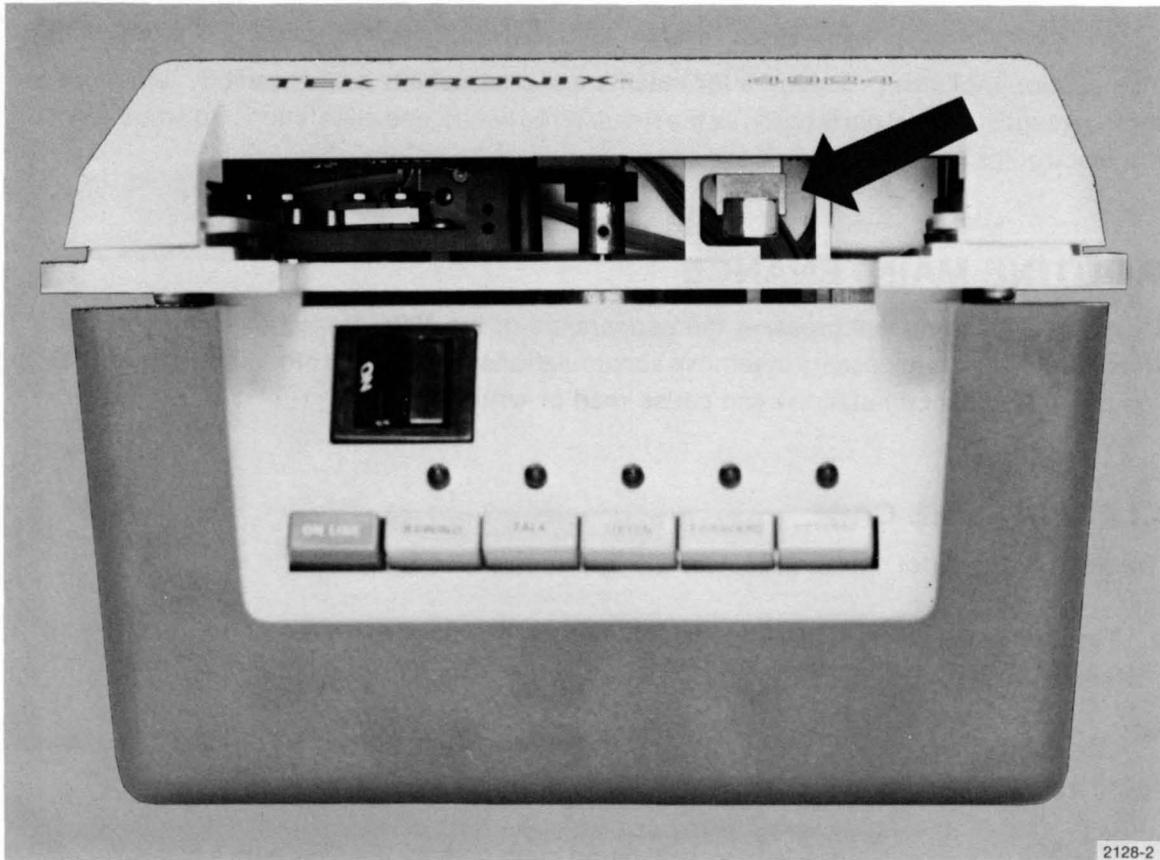


Fig. 3-1. Tape Head Location.

CAUTION

Do not use magnetic devices near the tape head. Do not touch the head with metal or other hard objects. To do so may damage the head and may result in damage to tape cartridges, causing data to be lost.

1. Inspect the head (Fig. 3-1) by shining a light, such as a penlight, across the surface of the head at an angle. This will reveal accumulations of oxide, and will also reveal damage to the head. If the head is scratched, scored, or excessively worn (Fig. 3-2), it should be replaced, as described later in this section. If the head is dirty, continue with this procedure.
2. Use a cotton swab moistened with isopropyl alcohol to rub off the accumulated matter. Light accumulations of oxide will probably be readily removable, while heavy or long-term accumulations may require more cleaning with alcohol and clean swabs. Use extreme care when cleaning the head to prevent scratching or damaging the head surface.

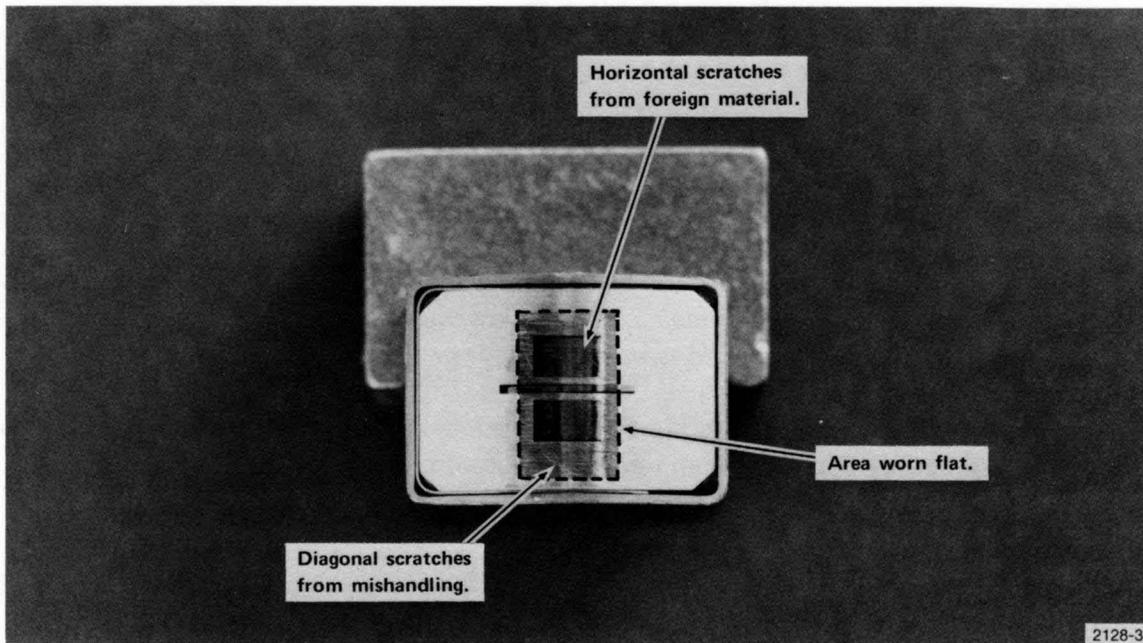


Fig. 3-2. Tape Head Damage.

3. After removing the oxides and other foreign matter, use a clean, dry cotton swab to polish the head and remove alcohol residue.

DISASSEMBLY/ASSEMBLY INFORMATION

The following paragraphs provide details on gaining access to the inside of the 4924, and on removal and replacement of circuit boards, components and assemblies. In addition, following the removal instructions sequentially provides a complete disassembly procedure. To reassemble the unit, follow the disassembly procedure in reverse order.

During disassembly/assembly or removal and replacement of parts, certain precautions are necessary to make certain that the procedure will be properly completed. Follow all instructions carefully and completely, particularly in the tape drive area. Removal of the covers is a prerequisite for any disassembly procedure.

COVER REMOVAL AND REPLACEMENT

1. Disconnect the unit from the power source prior to any disassembly.

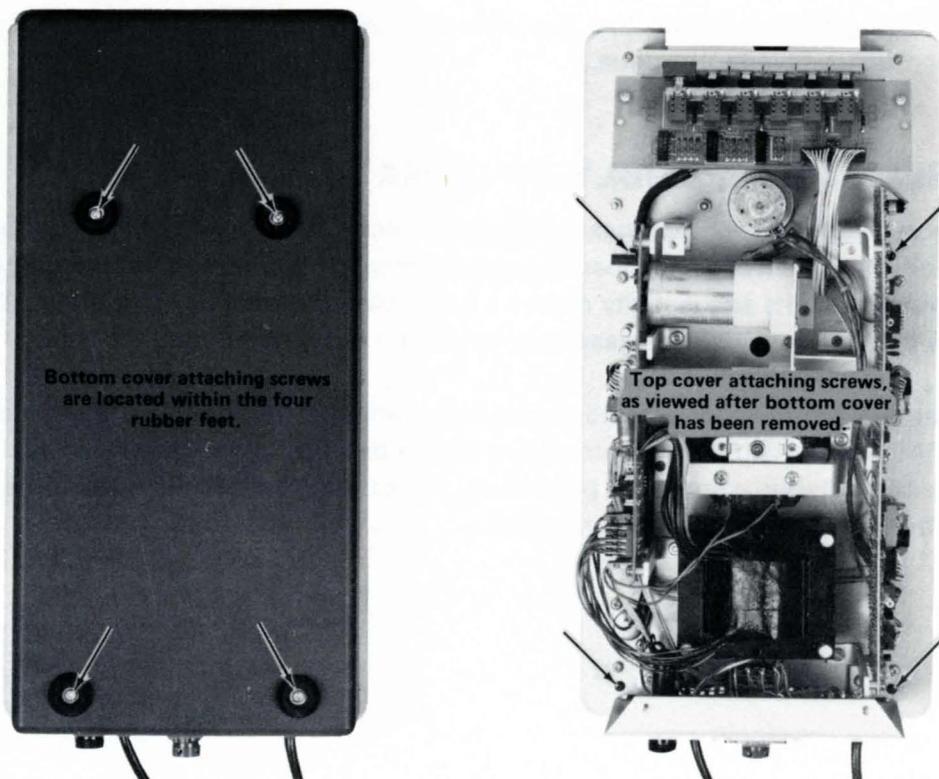
WARNING

Dangerous voltages exist at several places inside the unit, unless the power cord is disconnected from the power mains. (If the power switch is off, power may still be applied to the switch connections unless the power cord is disconnected.)

2. Turn the 4924 over, resting it on its top. Remove the four screws which attach both the unit's feet and bottom cover (Fig. 3-3), then remove the bottom cover.

NOTE

The unit should be placed on a clean surface which is free of any objects which might scratch the top cover.



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Fig. 3-3. Cover Attaching Screws.

3. Leaving the unit on its top, remove the four black internal screws which attach the top cover (Fig. 3-3), then lift the chassis out of the top cover and place it upright on the work surface.
4. To replace the covers on the unit, turn the chassis over, place it back into the top cover, then follow steps 2 and 3 in reverse order.

MOTOR/TACHOMETER REMOVAL AND REPLACEMENT

Replacing the Motor/Tachometer assembly is necessary whenever the motor does not turn when the appropriate voltage is present on the motor poles, or when excessive ripple or non-linear voltage is present in the tachometer output. To remove and replace the motor, use the following procedure:

1. Disconnect J326 on the Read/Write board, which carries all connections to and from the Motor/Tachometer assembly.
2. Remove the rubber-covered drive roller from the motor shaft by loosening the set screw securing the roller to the shaft, and lifting the roller from the shaft.
3. Remove the four screws that attach the Motor/Tachometer to the 4924 frame (Fig. 3-4). As the last screw is removed, the motor assembly is freed for removal from the chassis.

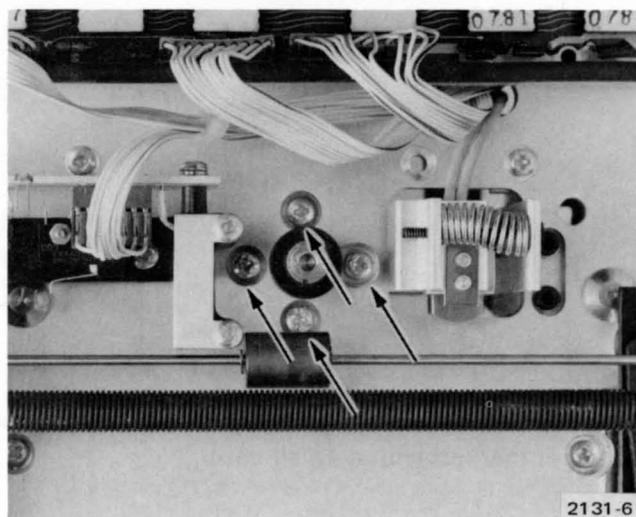


Fig. 3-4. Motor Attaching Screws.

Servicing

4. Loosen the screws that attach the motor filter assembly to the motor.
5. To install a new motor, first disconnect the leads from the motor and tachometer poles. Attach the motor and tachometer filter leads in position on the motor and tachometer.
6. Secure the filter assembly to the motor.
7. Install the new motor (with filter assembly attached) from the underside of the 4924 frame, positioning the motor pilot (Fig. 3-5) into the chassis motor opening. Rotate the motor until the screw holes are aligned, then install and tighten the four securing screws.

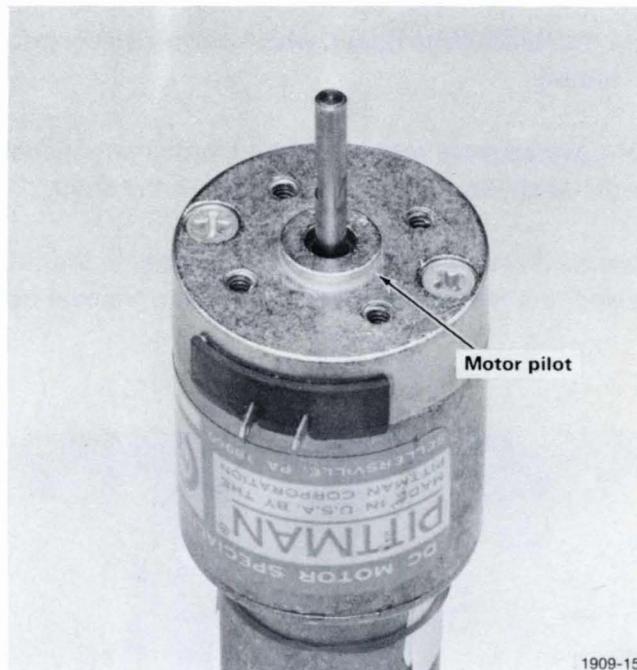


Fig. 3-5. Motor Pilot Location.

8. Connect J326 on the Read/Write board, aligning pin one of the connector with pin one on the circuit board. (Pin one is marked with a small caret.)
9. Place the rubber-covered drive roller on the motor shaft, positioning the set screw to the flat area on the motor shaft. (The rubber portion of the roller is the upper half.) Turn the set screw in until snug, but not tight.
10. Insert a cartridge into the unit and check to see that the rubber-covered roller contacts only the cartridge's internal drive roller (Fig. 3-6). After making certain that the rubber roller contacts only the cartridge drive roller, tighten the set screw against the flat area of the motor shaft.

CAUTION

The rubber roller must contact no part of the plastic cartridge case. Contact with the plastic case may damage the roller or the cartridge case. If the cartridge case is damaged, bits of plastic may be deposited within the case, damaging the tape or the Read/Write head, and causing subsequent loss of data from the tape.

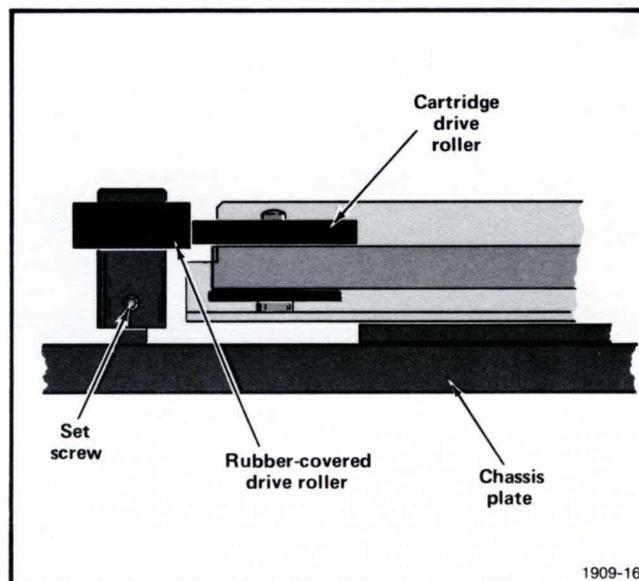


Fig. 3-6. Rubber Roller/Cartridge Roller Positioning.

DRIVE ROLLER REMOVAL AND REPLACEMENT

To remove or replace the drive roller, refer to steps 2, 9 and 10 of the Motor/Tachometer Removal/Replacement procedure.

TAPE HEAD REMOVAL AND REPLACEMENT

It is necessary to replace the Read/Write head if it becomes badly worn, scratched, or otherwise damaged. Refer to the earlier description of cleaning the Read/Write head and Fig. 3-2 for inspection procedures and damage indications.

Servicing

1. Remove the two screws that attach the head assembly to the mounting bracket (Fig. 3-7). Remove the head assembly.

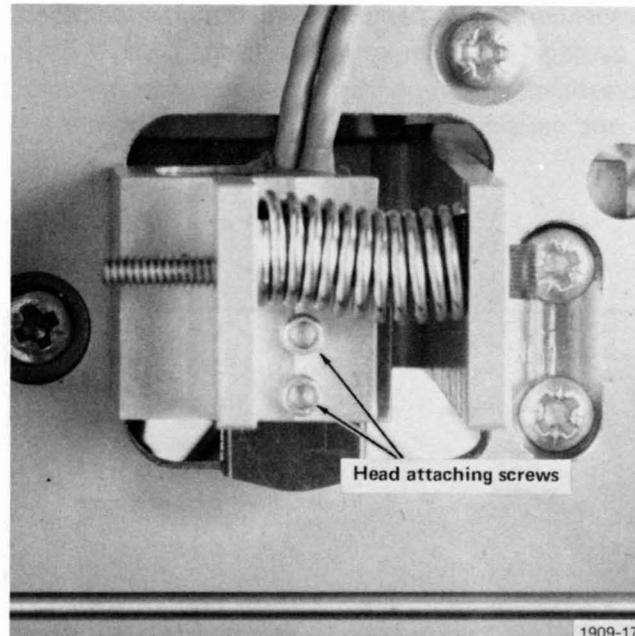


Fig. 3-7. Location of Head Attaching Screws.

2. Unplug the connector from the back of the Read/Write head, and note which side of the connector is on top, for reference during reassembly.
3. Replace the connector on the Read/Write head, paying attention to the previously marked upper side. (A small caret marks the side closest to the drive roller.)
4. Place the new head in position, and loosely install the two attaching screws. Position the forward edge parallel to the front of the mounting bracket (Fig. 3-7), and tighten the attaching screws.

NOTE

After replacing the Read/Write head, it will be necessary to adjust for height and skew compensation. Refer to "Electrical Adjustments" later in this section.

STATUS BOARD AND BRACKET REMOVAL AND REPLACEMENT

The Status board contains connections for the Load switch (which determines whether the cartridge is inserted), the Write-Protect switch (which determines whether or not the cartridge is Write-Protected), and the lamp and photo-transistors for light-sensing the position marker holes in each end of the tape. All these components are located on the Status bracket, which is secured to the Status board by screws and circuit connections. Removal and replacement of the Status board and bracket are as follows:

1. To replace the lamp in the Status bracket, it is not necessary to remove the assembly from the 4924. Remove the metal cover from the top of the bracket by removing the two attaching screws, then unsolder the two lamp connections from the Status board (Fig. 3-8).

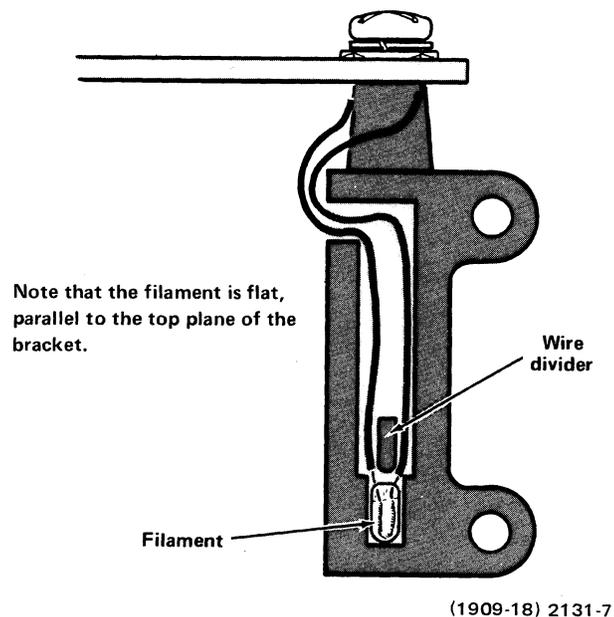


Fig. 3-8. Sensor Lamp Positioning.

2. Place new insulation tubing on the leads of a new lamp, then place the new lamp into the bracket, positioning one of the leads on each side of the bracket's internal divider. With one lamp lead on each side of the divider, the filament should be roughly parallel to the top plane of the bracket. The position of the filament is critical in its ability to be sensed by the phototransistors. Position the leads out through the back of the bracket, and solder them in position on the Status board. (Refer to Fig. 3-8).

3. If this is the only service procedure, replace the metal cover on the lamp part of the Status bracket, and secure it with two attaching screws. If the board is to be further disassembled, leave the cover off.

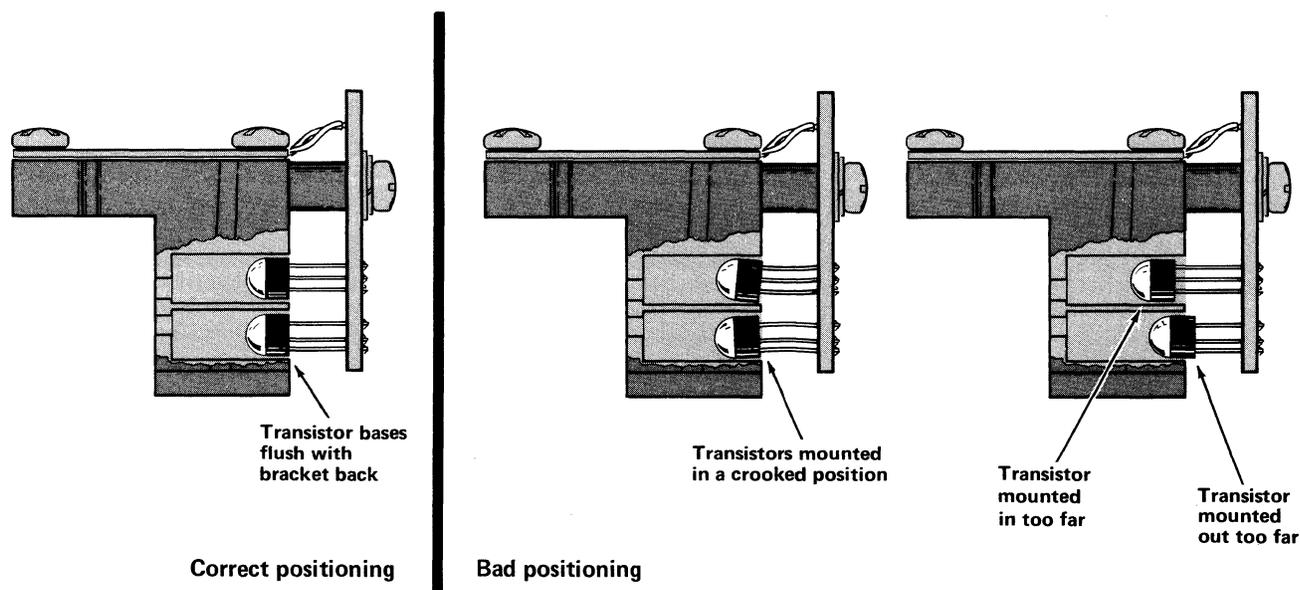
Servicing

4. Mark the position of the status bracket on the frame with a fine-point pen or pencil.
5. Remove the connector from J360, and remove the two screws and locknuts that secure the bracket to the 4924 frame. The entire assembly may then be removed.
6. To remove the Load or Write-Protect switch from the bracket, it is necessary first to unsolder the Status board wire leads from the appropriate switch connectors. (If the entire bracket is to be removed from the Status board, the leads to both switches must be unsoldered.) Once the leads have been unsoldered, the switch may be removed by removing the two screws and nuts which attach it to the bracket. To replace the switch, with no further disassembly or repair, refer to step 10.
7. To remove the bracket from the Status board, unsolder the connections from both switches, as noted above. Remove the two bracket-to-board attaching screws from the back side of the Status board; the board and bracket may now be separated. (Q1 and Q2, the phototransistors for detecting the position markers, remain connected to the Status board.)
8. To replace Q1 or Q2, first note the length of its leads, then unsolder its connections.

NOTE

The base lead of the phototransistors is not used in this application. The base lead may be left on or removed (cut off) if desired.

Position the new part onto the board, then position the bracket onto the board to check the positioning of the phototransistor. The back side of the phototransistor should be flush with and parallel to the back plane of the bracket, when the bracket is in position; the phototransistors must be positioned straight into the hole. (Refer to Fig. 3-9.) Adjust the position of the phototransistor as necessary, then solder the leads and clip off the excess. Use a clean, soft cloth to clean fingerprints from the spherical lens at the front of the phototransistor.



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Fig. 3-9. Phototransistor Mounting.

9. Position the bracket onto the Status board, and secure it with the two attaching screws.
10. Position the switches onto the bracket (if they have been removed), and install the screws and nuts which secure them to the bracket. Place the Status board wire leads back into the switch connectors, and solder them in place.
11. Position the bracket within the scribe marks (made in step 4) and secure it with two attaching screws and nuts. Check the distance between the bracket and an installed cartridge against Fig. 3-10. There should be a 0.060" space, and the bracket must be **parallel** to the cartridge. Connect the harmonica connector to J360, aligning pin one of each. (Pin one is marked with a small caret.)
12. To finish a complete reassembly (when the Status board and bracket have been separated), position the lamp into its position in the bracket as described in step 2, then replace the metal cover and secure it with the two attaching screws.
13. If switches have been replaced, insert a cartridge into the bracket and make certain that the switches close. (First use a non-write-protected cartridge to check the Load switch, then activate the Write-Protect feature and check the Write-Protect switch.) A faint "click" may be heard as the switch actuates. (If the switches do not close when the cartridge and bracket are properly installed, carefully bend the switch actuators forward until proper operation occurs.)

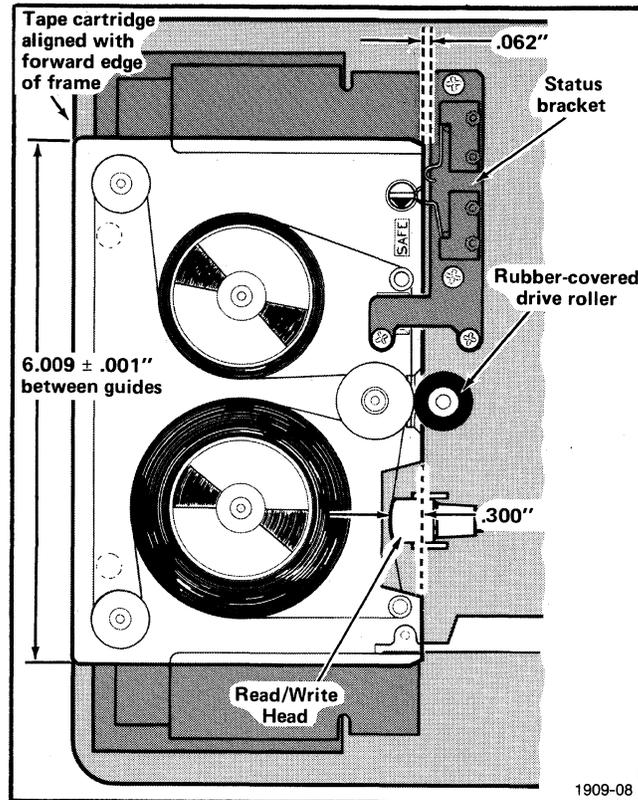


Fig. 3-10. Cartridge Position Dimensions.

CARTRIDGE GUIDE ASSEMBLY REMOVAL AND REPLACEMENT

If it becomes necessary to remove the cartridge guide assembly for any reason, use the following procedure:

1. If only the cartridge detent arms are to be removed, it is not necessary to remove the entire guide from the frame. Disconnect the tension springs (see Fig. 3-11), then remove the screws (one for each detent arm) that attach the arms to the guide. The arms may then be removed.
2. To replace the detent arm, position it back on the guide, with the pin through the slot in the guide and into the metal roller disk beneath the guide. (Refer to Fig. 3-11.) Install the aluminum bushings, then install the attaching screws. Install the spring ends into the mounting holes.
3. To remove the complete guide assembly, first carefully mark the 4924 frame around both cartridge guides with a fine-point pen or pencil. The guide assembly position is critical since it serves to lock the cartridge in position against the head, drive roller, and status switches.

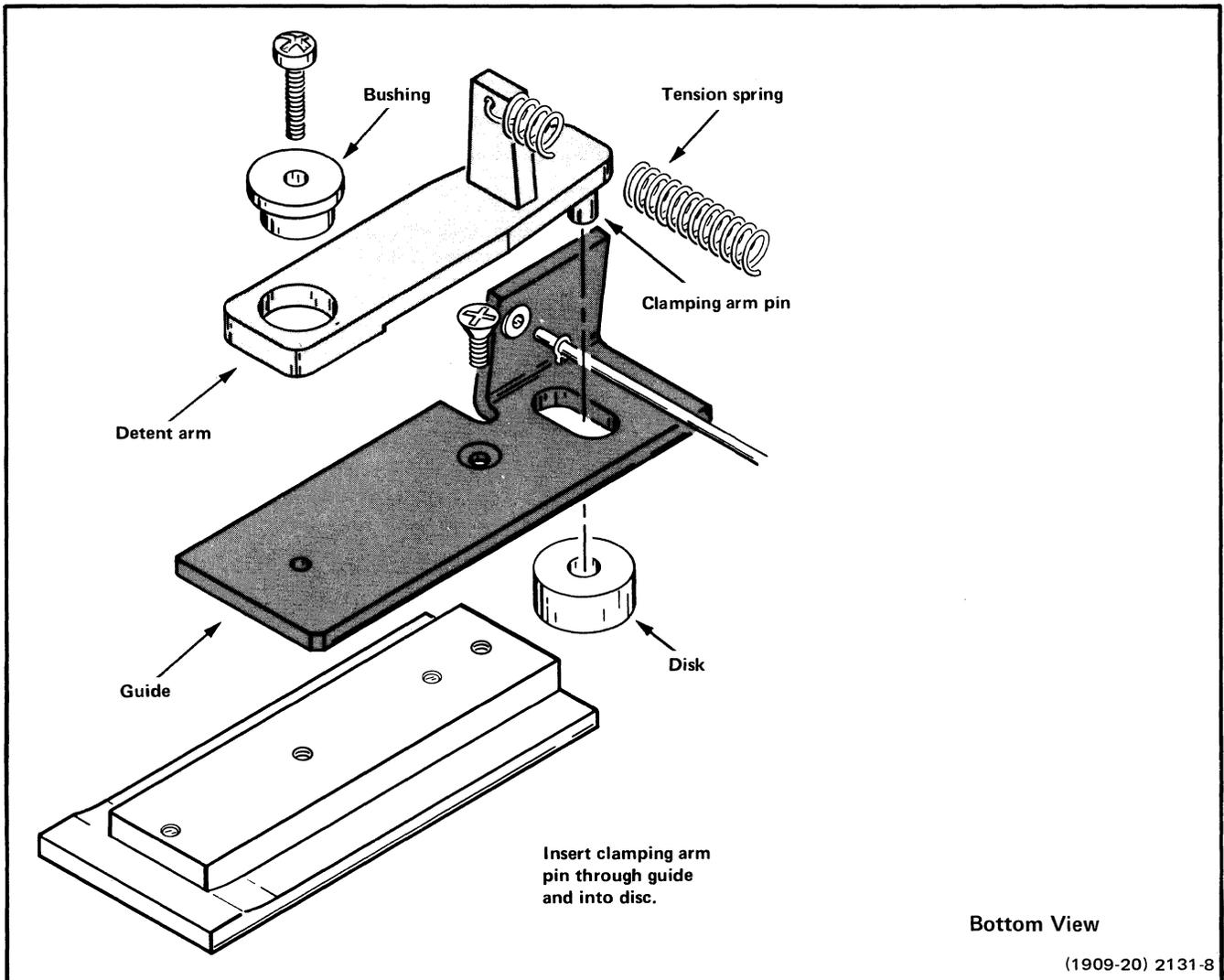


Fig. 3-11. Cartridge Guide Components.

4. From the bottom side of the frame, remove the four screws that attach the guides to the frame (Fig. 3-11). After removal, clean the areas under the moving parts with alcohol and swabs.
5. To replace the guide assembly, position each side of the guide over the mounting holes, and loosely install the attaching screws. Carefully position the guides within the previously-made marks, and tighten the attaching screws.
6. Check the cartridge fit with a number of cartridges. If any are excessively tight (or loose), readjust the guides within the scribe marks as necessary.

FAN MOTOR REMOVAL AND REPLACEMENT

If the cooling fan should fail to operate when power is applied, check to see that the fan blade rotates freely. If it does not, determine where it is binding and correct. If it turns freely by hand, but does not turn when power is applied, it will be necessary to remove and replace the motor. Use the following procedure:

1. Disconnect the fan motor leads from the Power Supply board (J345).
2. Remove the two screws and attaching nuts that secure the fan bracket to the 4924 frame. The locknuts may be held with a flat 5/16" open-end wrench (under the Control board) while the screws are removed.
3. Remove the two screws that attach the fan motor to the fan bracket. Remove the bracket. The fan and motor may then be lifted from the unit.
4. Pull the fan from the motor shaft.
5. Unsolder the motor leads from the tabs on the fan motor, and solder them in place on the new fan motor.
6. Push the fan blade assembly onto the motor shaft. Make certain that there is adequate clearance for rotation between the circular center area of the fan blades and the motor assembly. The clip should face away from the motor.
7. Install the fan assembly into the fan bracket, and install the two attaching screws loosely. Check the fan clearance by spinning it by hand.
8. Position the entire fan assembly into the 4924. Install the attaching screws through the frame, and secure them with the locknuts. (The locknuts may be held as before, by inserting a flat 5/16" open-end wrench under the Control board.)
9. Tighten the two screws that attach the fan to the fan bracket. Install the fan connector to J345 on the Power Supply.

POWER SUPPLY BOARD REMOVAL AND REPLACEMENT

The Power Supply has three electrolytic capacitors mounted in a bracket attached to the back of the board. To remove the assembly, use this procedure:

1. Disconnect all harmonica connectors from the Power Supply board.
2. Remove the two screws and locknuts that secure the capacitor bracket to the 4924 frame. The locknuts may be held while removing the screws by inserting a flat 5/16" open-end wrench under the Control board.

3. Remove the Power Supply board from its mounting brackets by removing the six attaching screws.
4. To further (completely) remove the Power Supply board for replacement, it is necessary to unsolder the transformer wire connections. Be sure to note which wire is unsoldered from each location. When the wires have been unsoldered, the assembly may then be removed.
5. Remove the capacitor bracket and "sockets" from the old assembly. To do so, first remove the six screws and attaching nuts that secure the "sockets" to the bracket, and remove the bracket. The "sockets" may then be individually pulled from the capacitors; the fit is fairly tight.
6. Install the capacitor sockets, one at a time, on the capacitors of the new Power Supply board. Position the sockets to align with the holes in the bracket, then install the screws and nuts to secure the sockets to the bracket.
7. Resolder the transformer leads to the appropriate positions on the Power Supply board, then place the board in position and loosely install the six attaching screws.
8. Install the two screws and locknuts that secure the capacitor bracket to the 4924 frame. (It may be necessary to reposition the bracket slightly on the capacitors to align with the mounting holes in the frame). Tighten the six previously installed attaching screws.
9. Reconnect all of the harmonica connectors on to the Power Supply board. Be careful to install pin 1 of the connector to pin 1 of the board.

HEAD MOUNTING BRACKET REMOVAL AND REPLACEMENT

It is normally not necessary to remove or replace the Head Mounting Bracket, except in case of breakage. Should the Head Mounting Bracket become broken or otherwise damaged, use this procedure to replace it:

1. Remove the connector from the back of the Read/Write head, noting which side is up for later reassembly.
2. Remove the six screws which attach the Read/Write board to the 4924 frame. Disconnect all connectors, and remove the Read/Write board.

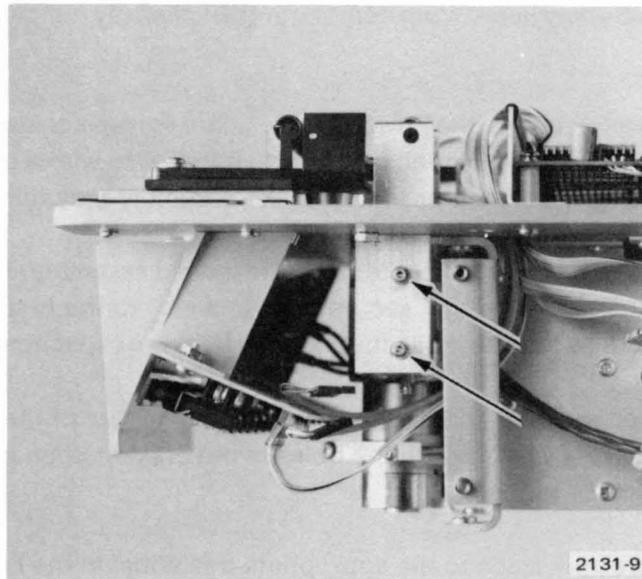


Fig. 3-12. Head Bracket Mounting Screws.

3. Remove the two screws that attach the Head Mounting Bracket to the mounting block (Fig. 3-12) and lift the bracket out from the top.

NOTE

Do not remove the mounting block from the 4924 frame.

4. Place the new bracket in position and install it by following the above steps in reverse order.

MECHANICAL COMPONENT POSITIONING

All previous disassembly procedures pertaining to the critical transport parts have recommended marking the position of the part on the frame prior to removal. This aids in positioning the replacement part in the same position as the removed part.

However, if it is suspected that the alignment of these parts is in error, or if a part should be dislodged in use, alignment may be checked using Fig. 3-10, which shows the relative position of the critical parts when the cartridge is installed in the proper position. The detent arms should pull the cartridge into this position (the back edge of the cartridge flush with and parallel to the forward edge of the 4924 frame) when the cartridge is installed.

In addition, a complete mechanical alignment may be performed using the mechanical alignment fixture (Tektronix Part Number 067-0769-01). The Head Alignment Fixture (Tektronix Part Number 067-0788-00) can be used to align the Read/Write Head after adjusting for height and skew azimuth.

AC POWER REQUIREMENTS



The 4924 is intended to be operated from a single-phase power source which has one of its current-carrying conductors (neutral) at ground (earth) potential. Operation from other power sources in which both current-carrying conductors are live with respect to ground (such as phase-to-phase on a multi-phase system, or across the legs of a 115-230 volt single-phase three-wire system) is not recommended, since only the line conductor has over-current (fuse) protection within the unit.

The 4924 is designed to operate from a 115 or 230 volt nominal line voltage source that has a frequency of 50 to 60 Hz. In addition, any of three voltage ranges for 115 Vac or four voltage ranges for 230 Vac may be selected. Voltage, current and range limitations are listed in Table 3-1.

A fuse change and a transformer jumper arrangement permit the 4924 to be modified to suit the voltage supply. A tag on the back panel identifies the internal voltage setting for which the unit is wired when shipped from the factory. If the jumper arrangement is changed for any reason (changing the internal voltage setting), cross out the old setting and attach a tag with the new setting in its place.

Table 3-1
4924 OPERATING VOLTAGES

Nominal Voltage	Tolerance	Voltage Range	Frequency	Line Fuse Value
100 Vac 115 Vac 120 Vac	±10%	90 to 110 Vac 104 to 126 Vac 108 to 132 Vac	50 to 60 Hz	1.0 A Slow-blow
200 Vac 220 Vac 230 Vac 240 Vac		180 to 220 Vac 198 to 242 Vac 207 to 253 Vac 216 to 264 Vac		0.6 A Slow-blow

AC POWER CORD AND GROUNDING REQUIREMENTS

This instrument has a detachable three-wire cord with a three-wire terminal polarized plug for connection to the power source and safety earth. The Safety Earth terminal of the plug is directly connected to the instrument frame for electric-shock protection. Insert this plug only in a mating outlet with a safety earth contact, or otherwise connect the frame of the unit to a safety earth system.

See Fig. 3-13 for standard power cords. In other jurisdictions, replace standard plugs with plugs that satisfy local authorities.

WARNING

To avoid electrical shock or equipment damage, be sure to replace the cord set only with another of the same polarity.

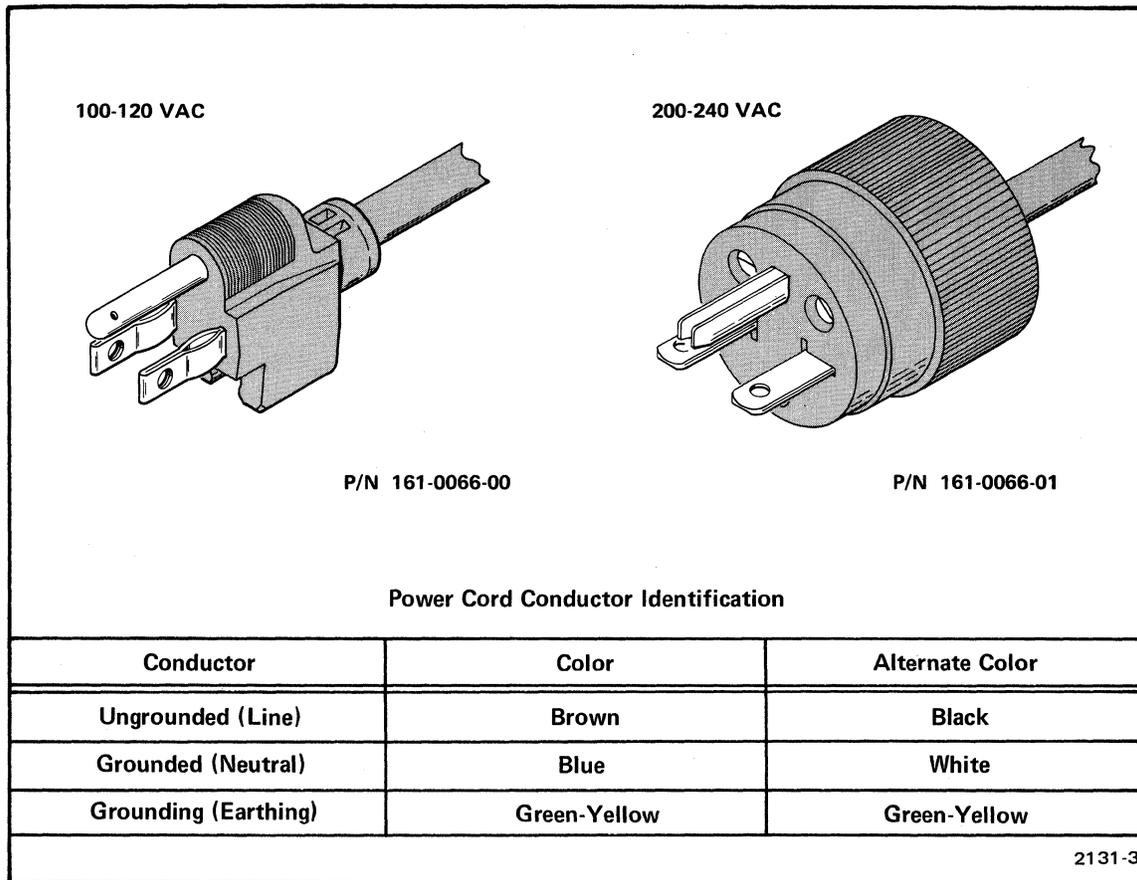


Fig. 3-13. Standard Power Cords.

LINE VOLTAGE SELECTION

To change the line voltage selection, remove the cover, as described in COVER REMOVAL AND REPLACEMENT.

The line voltage selection strap is located on the lower left side of the unit, as viewed from the front. To change the line voltage selection, position the strap to the desired location (Fig. 3-14).

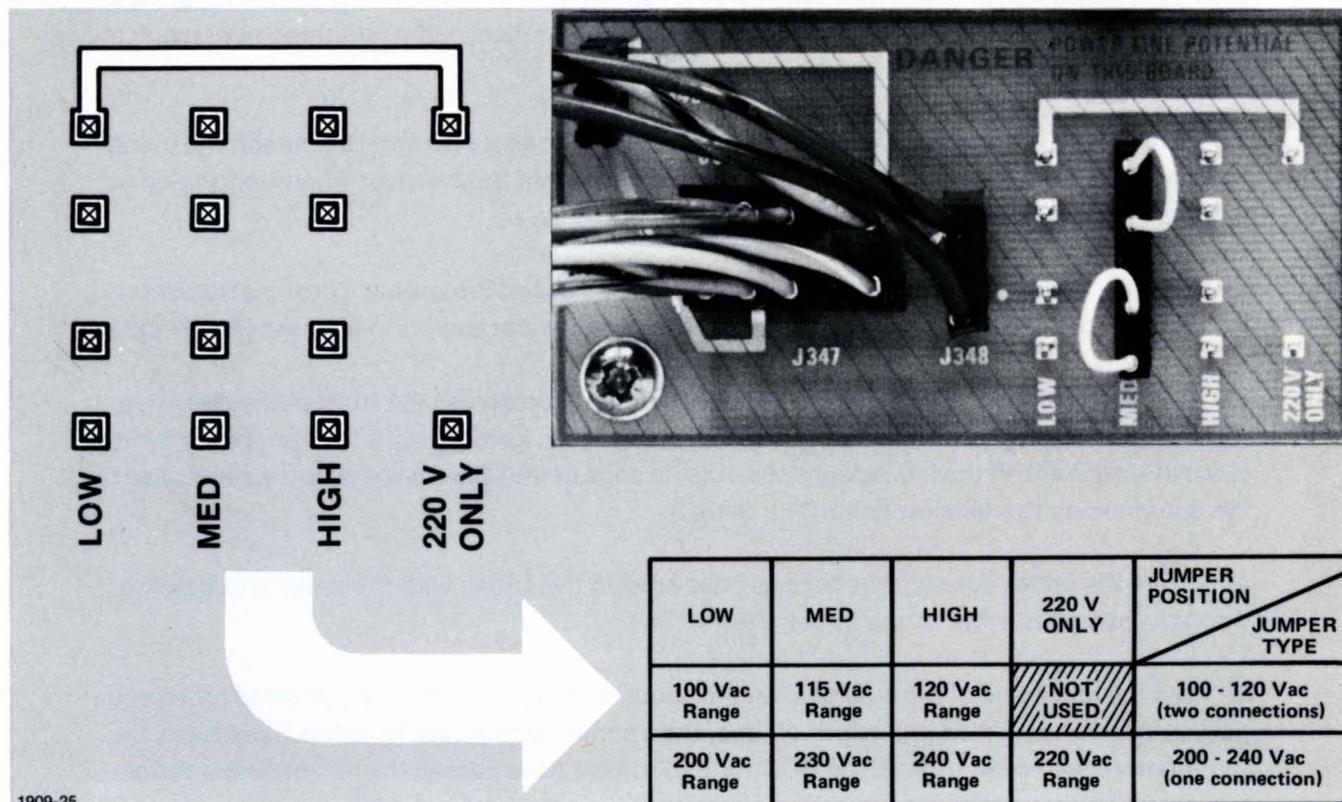


Fig. 3-14. Line Voltage Selection.

For operation in the 110, 115, and 120 Vac ranges, the line voltage jumpers are connected from pin 1 to pin 3 and from pin 6 to pin 8. For operation in the four ranges above 200 Vac, an alternate jumper is supplied. It connects only the two outside pins (pin 1 to pin 8). Note also that a single pair of pins provides a jumper position for the 220 Vac range, while the HIGH, MED, and LOW positions provide for 240 Vac, 230 Vac, and 200 Vac respectively.

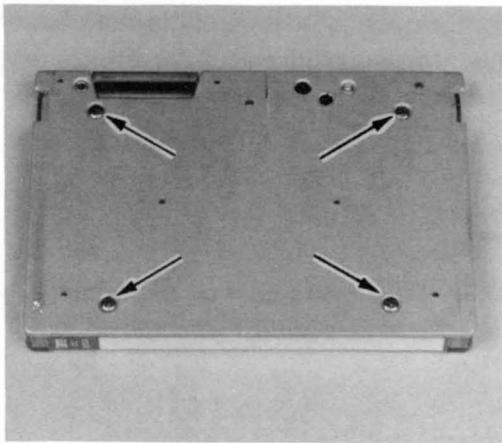
LINE FUSE

There is one power line fuse, located on the 4924 back panel. This fuse is a 1 A slow-blow fuse for operation in the 100-120 Vac range; it must be changed to a 0.6 A slow-blow fuse for operation in the 200-240 Vac range.

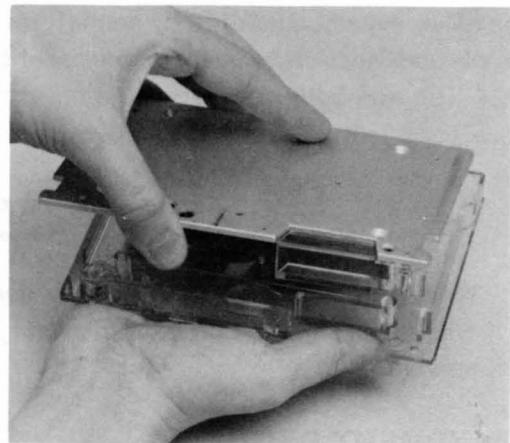
CARTRIDGE RESPOOLING

The tape cartridge used in the 4924 is open-ended; that is, the tape ends are not secured to either of the spools. The unit relies on light-sensing of small holes near each end of the tape to stop tape motion before the physical end of the tape is reached. Two conditions may cause the tape to run off one of the spools. These conditions are: a possible circuit failure, or an obstruction in the light path (such as a soiled cartridge or Lamp-Detector assembly), or a faulty cartridge, particularly if it is a new one. Use the following procedure to respool the tape. Tape positioning is critical to proper interpretation of the data. Incorrect positioning may result in loss of information.

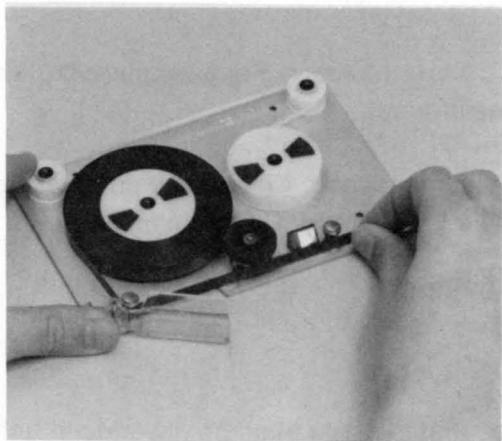
1. Turn the cartridge over (metal side up) and remove the four screws that attach the metal base to the plastic cover (Fig. 3-15A). Do not use a magnetic screwdriver when working on or around the cartridge.
2. Carefully remove the cartridge base from the plastic cover. Be careful not to lose the Write-Protect cylinder or the small metal spring between the cylinder and the metal base (Fig. 3-15B).
3. Turn the base over, and place the loose end of the tape across the front of the cartridge, threading it through in front of the two guide posts. Now, keeping light tension on the tape, place the loose end of the tape around the outside edge of the take-up spool, to the point where the spool meets the tension band (Fig. 3-15C).
4. Rotate the spool, causing the tape to pass around the spool, with the loose end passing through the inside edge of the spool (Fig. 3-15D).
5. Hold the loose end of the tape against the spool, and continue to rotate until the loose end passes under the continuing length of tape, then continue to rotate for a few more turns by turning the drive roller, until all the BOT (or EOT) holes have passed the mirror. Make certain that these first windings stay evenly within the spool edges (Fig. 3-15E).
6. Make certain that the Write-Protect cylinder is in position, with the spring washer between the cylinder and the metal cartridge base. Turn the cartridge base over, and carefully position it into the plastic case, making certain to fit the Write-Protect cylinder through the opening in the plastic case. Be careful not to catch and wrinkle the tape with the plastic case (Fig. 3-15F).
7. Holding the cartridge together, install the four screws that attach the plastic case to the metal base.



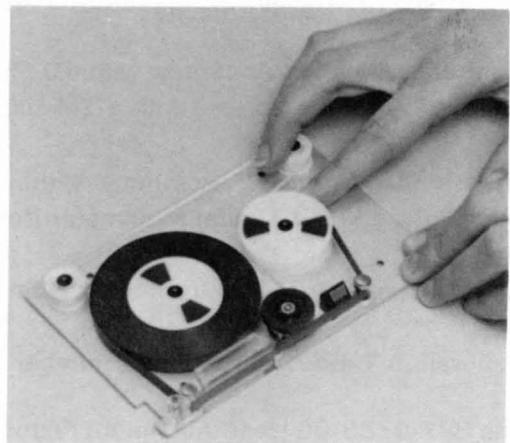
A. Cartridge attaching screws.



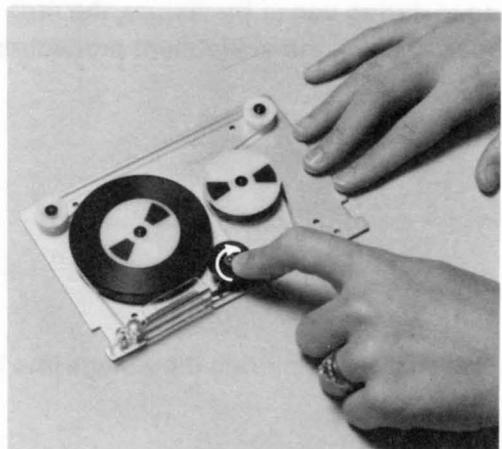
B. Disassembling the tape cartridge.



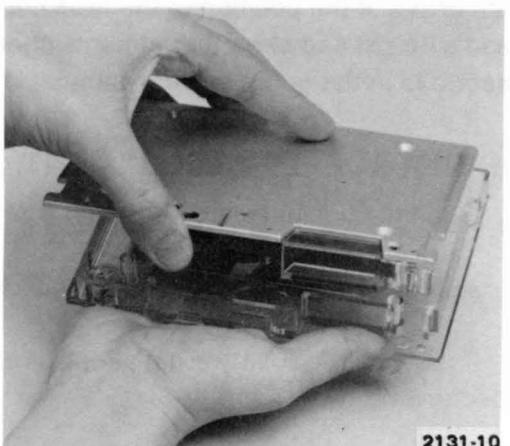
C. Tape positioning within the cartridge.



D. Beginning the tape winding.



E. Winding the tape.



F. Assembling the tape cartridge.

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Fig. 3-15. Cartridge Respooling Procedure.

ELECTRICAL ADJUSTMENTS

The following adjustments may be performed to ensure proper calibration of the 4924 Power Supply and Read/Write boards. There are no adjustments on any other circuit cards within the 4924. Top and bottom covers must be removed to perform these adjustments.

WARNING

When operating the 4924 with the bottom cover removed, use caution to contact only the designated points. Line voltage is exposed at several points when power is applied.

EQUIPMENT REQUIRED

Test Oscilloscope. Bandwidth DC to at least 30 MHz. Minimum deflection factor: 5 millivolts per division. For example, a Tektronix Model 465 Oscilloscope.

Frequency Counter. Accuracy: within 0.5%. Range: 10 kHz minimum. For example, a DC 503 Universal Counter (for use with a TM 500 series mainframe).

Precision DC Voltmeter. Accuracy: within 0.5%. Input Impedance: 1 megohm minimum. For example, a DM 501 Digital Multimeter (for use with a TM 500 series mainframe).

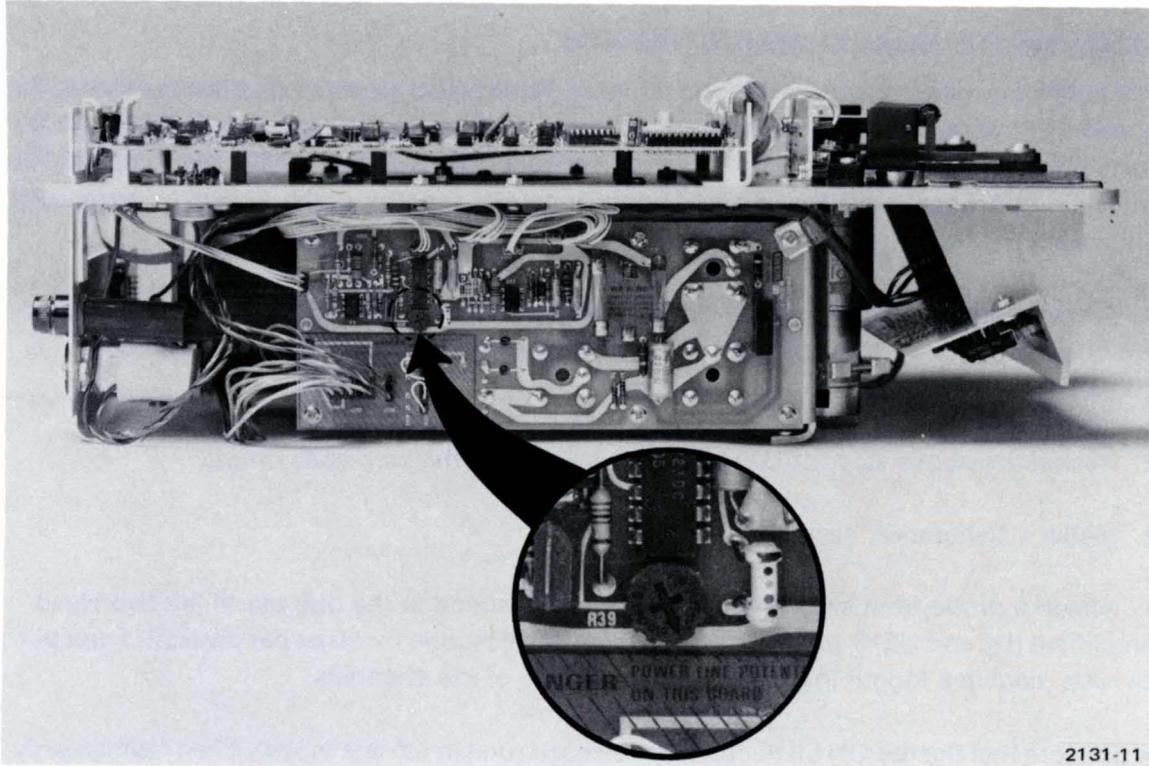
Calibration Fixture. Tektronix Part Number 067-0788-00.

Calibration Tape. Tektronix part number 067-0781-01.

The 067-0788-00 Head Alignment Fixture ensures that the tape head on digital tape units is correctly positioned with respect to other mechanical parts on the unit. Use the fixture after head replacement or mechanical disassembly, or when tape head position causes data errors. If the position of the tape head is changed during use of the fixture, the tape head's height and skew adjustments should be checked using the adjustment procedure described in the unit's service manual.

POWER SUPPLY ADJUSTMENT

1. Place the voltmeter probe on pin 2 of J342.
2. Apply power to the 4924, and check for +12 volts $\pm 0.5\%$ (60 mV).
3. If the +12 Vdc supply is not as specified, adjust R39 (Fig. 3-16) to bring the voltage into the specified range.
4. No other voltages on the Power Supply board are adjustable; all may be checked against the voltages shown in Table 3-2.



2131-11

Fig. 3-16. +12 Volt Supply Adjustment Locations.

Table 3-2
4924 INTERNAL VOLTAGES

Voltage	Tolerance	Location
+12 V	$\pm 0.5\%$ (60 mV)	J342-2
+22 V	Unregulated	J344-2
+5.1 V	$\pm 1\%$ (51 mV)	J344-5
-12 V	$\pm 1.5\%$ (180 mV)	J342-1
-22 V	Unregulated	J344-3

READ/WRITE BOARD ADJUSTMENTS

The following electrical adjustments on the Read/Write board provide adjustment of the Motor Speed Control and Data Level Offset. In addition, mechanical adjustments that provide for correct head height and skew (azimuth) alignment are measured on the Read/Write board. The adjustments are made with the unit in its normal operating configuration, except for removal of the covers.

1. Place the voltmeter probe on the output (pin 6) of Head Amplifier U5. With no tape installed, the output should be zero volts. If not, adjust R13 (Fig. 3-17) until the zero volts output is obtained.
2. Repeat the above step for U215, adjusting R213 for the zero volts output.
3. Install a Calibration Tape.
4. Attach a probe from each channel of the oscilloscope to the outputs of the two Head Amplifiers (U5 and U215, pin 6 of each). Set the oscilloscope for 50 μ s per division, 1 volt per division, negative trigger internally, and invert one of the channels.
5. Be sure that the red ON LINE button is released (unit in off-line mode). Then momentarily press the FORWARD button.

NOTE

The tape should run forward at its normal speed of 30 inches per second. If it runs forward at the faster speed of 90 inches per second, wait for it to reach the end of the tape and rewind, then press the FORWARD button again.

Observe the waveforms on the oscilloscope screen. They should resemble those in Fig. 3-18. Adjust the skew (azimuth) adjusting screw (Fig. 3-19) to align the two waveform peaks, as in Fig. 3-18A, then change to 10 μ s per division, 0.5 volts per division for further alignment, as in Fig. 3-18B.

6. Move the scope probes to pins 1 and 2 of U235, and change the time base to 1 μ s per division and change back to 1 V/division. The pulses should be aligned within 1 μ s.

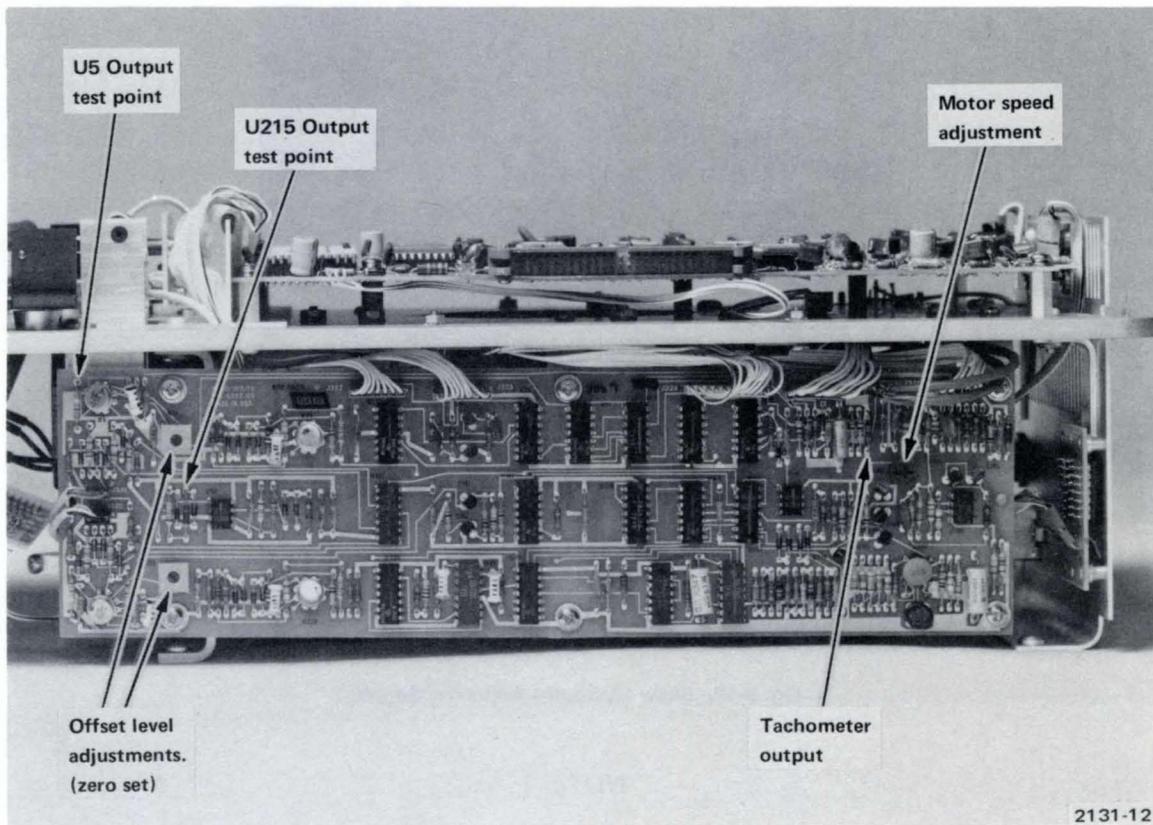


Fig. 3-17. Read/Write Board Adjustment Locations.

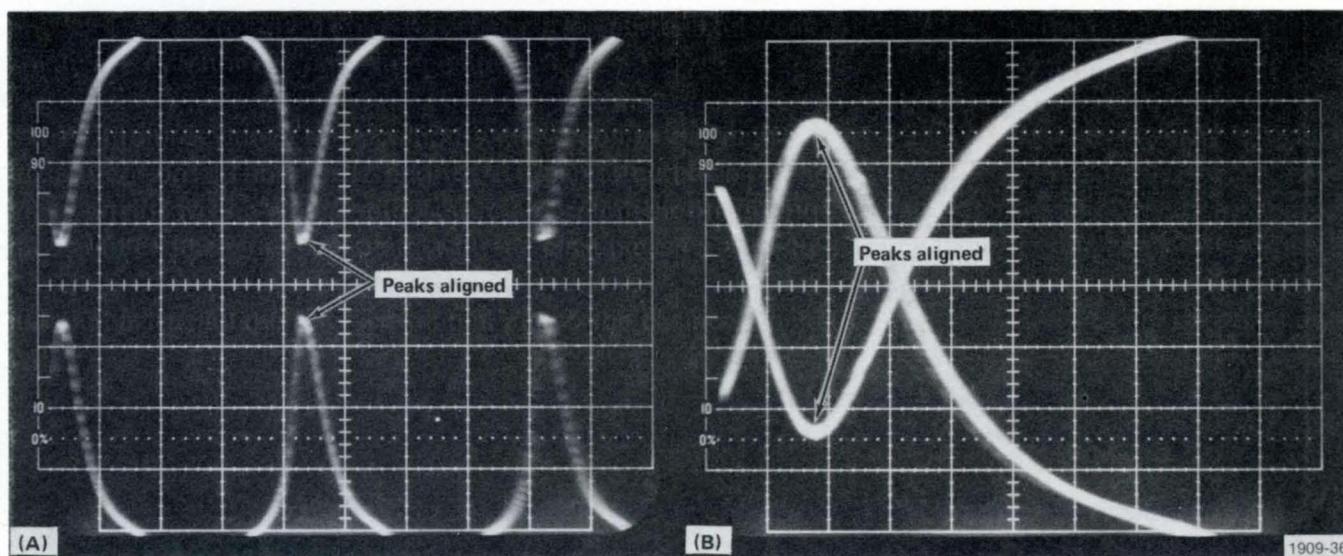


Fig. 3-18. Correct Skew Adjustment Waveforms.

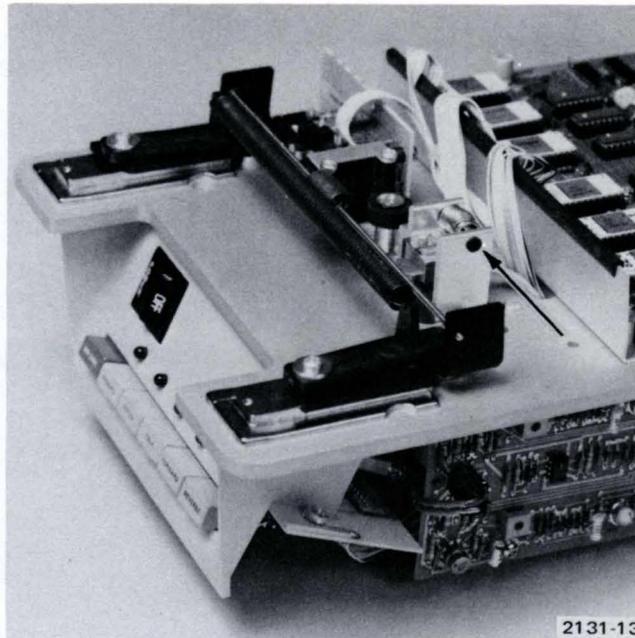


Fig. 3-19. Skew (Azimuth) Adjusting Screw.

NOTE

The calibration tape has erased portions within the first half of the tape for use in setting the correct head height. If tape motion has passed the halfway point prior to performing the height adjustment (step 7), it will be necessary to wait for the tape to reach the end and rewind to the beginning. Then press the FORWARD button again, to start the tape moving at 30 inches per second.

7. Change the oscilloscope time base to 20 ms per division, and place the probes back in their original positions (U5 and U215, pin 6 of each). The narrow portions of the oscilloscope display (Fig. 3-20) represent the edges of erased portions of the tape.

To adjust the head height, back off the height locking screw and turn the adjusting screw (Fig. 3-21) until the erased portions of the oscilloscope trace are minimized as in Fig. 3-20A, then change to 0.2 V/division for fine adjustment, as in Fig. 3-20B. Turn the locking screw in until snug. After resetting the locking screw, the height should be rechecked. Slight readjustment may be necessary.

8. After completing the height adjustment, the skew (azimuth) adjustment (steps 5 and 6) should be rechecked, followed by a recheck of the height (step 7).

9. To check the drive motor speed, attach the counter probe to pin 1 of U235 (on the Read/Write board). Access the second half of the calibration tape (which has no erased portions) and monitor the pulse period. The period should be 100 μ s (for a frequency of 10 kHz). If not, adjust R186 to reach the correct frequency (and motor speed).

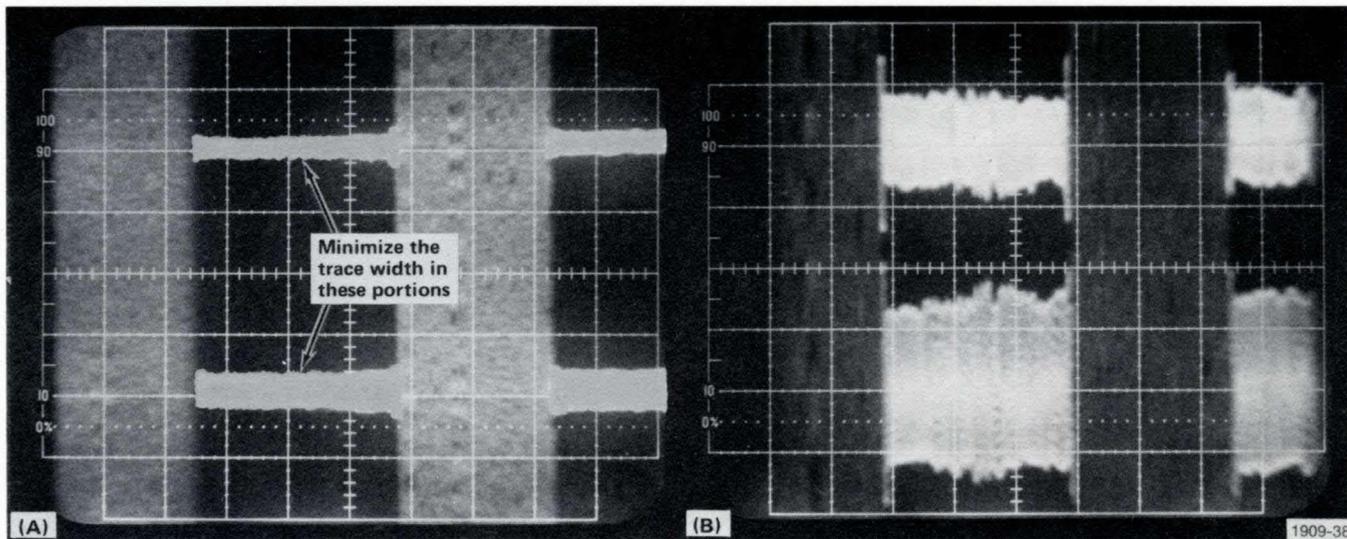


Fig. 3-20. Correct Height Adjustment Waveforms.

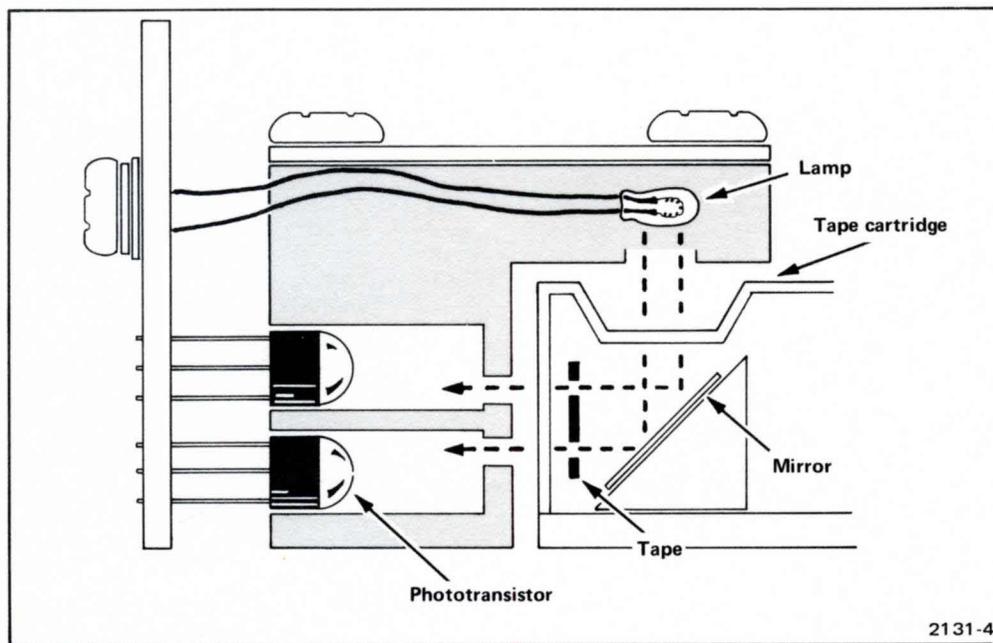


Fig. 3-21. Height Adjusting Screws.

NOTE

A frequency measurement must be averaged over a period of at least one second.

Section 4

GENERAL PURPOSE INTERFACE BUS

The 4924 communicates with the outside world by means of the General Purpose Interface Bus, whose operation is defined in IEEE Standard 488-1975. This section summarizes the pertinent parts of that standard.

The GPIB is a collection of 24 wires in a common shielded cable. Eight of the wires are grounds; the other sixteen are functionally grouped into three busses: the data, management, and transfer busses. The GPIB attaches to the 4924 at rear-panel connector J302, whose pin arrangement is shown in Fig. 4-1.

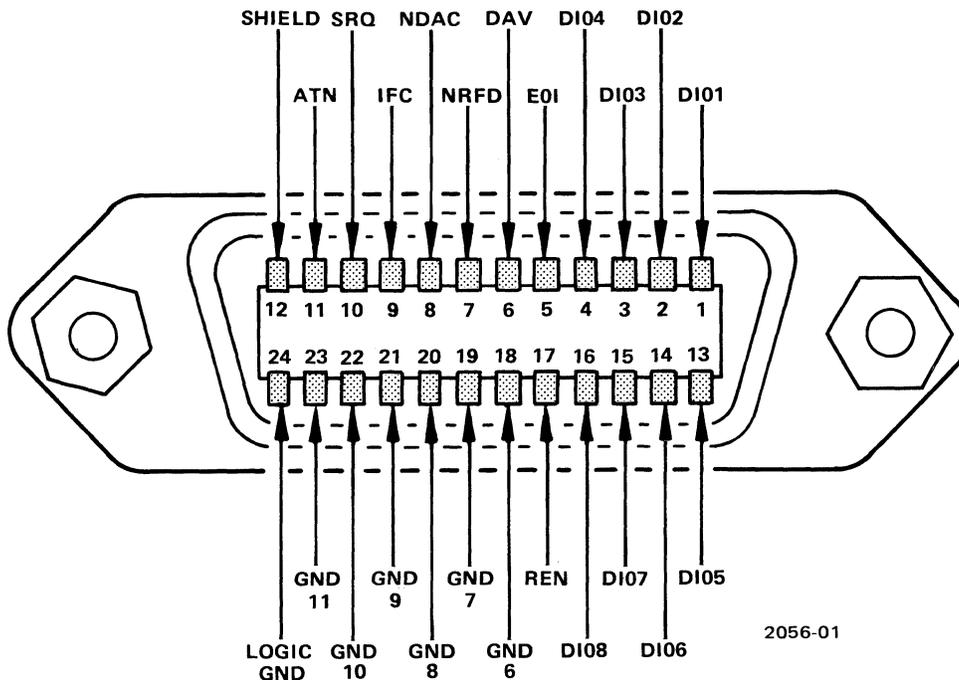


Fig. 4-1. GPIB Connector.

All devices on the GPIB are connected in parallel, and all the lines of the GPIB's three busses are active low, passive high; a line is low if any device on the GPIB pulls it low (i.e., to ground) and high only if all devices let it float to a TTL high (i.e., +3.4 V). That is, the devices are connected to the GPIB lines in a "wired-OR" configuration.

DATA BUS

The Data Bus contains eight bidirectional active-low signal lines. One byte of information (eight bits) is transferred over the bus at a time. DIO1 (Data In-Out bit 1) represents the least significant bit in the byte; DIO8 (Data In-Out 8) represents the most significant bit. Each byte represents a primary or secondary address, a universal command, or a data byte. (Primary and secondary addresses and universal commands are distinguished from data bytes by having the ATN line—in the management bus—activated while they are sent. With ATN asserted, certain bytes are reserved for universal commands and others for primary and secondary addresses.)

MANAGEMENT BUS

The Management Bus is a group of five signal lines used to control data transfers over the Data Bus. Their signal definitions are:

- | | |
|-----------------------|---|
| ATN (Attention!) | This line is activated by the controller when devices on the GPIB are being assigned as listeners and talkers. Only device addresses (primary or secondary) and control messages can be transferred over the Data Bus when ATN is active low. After ATN goes high, only the devices assigned as listeners and talkers can take part in the data transfer. |
| SRQ (Service Request) | Any device on the GPIB can request the attention of the controller by setting SRQ active low. The 4924 will generate a SRQ when an error condition occurs. For example, if the 4924 is writing data into a file on the tape and the end of the tape is reached before the end of the file, a SRQ is generated. The GPIB controller should respond to the SRQ by initiating a serial poll, to ascertain which device on the GPIB is requesting service. As the device requesting service is polled, it releases SRQ, letting it float inactive high. If the 4924 is the only possible device which might have issued the SRQ, the controller might have the 4924 perform the ERROR command rather than doing a serial poll; this, too, would cause the 4924 to release the SRQ line. |
| IFC (Interface Clear) | The IFC message may be sent by the GPIB controller to put all devices on the GPIB into a known quiescent state. If the 4924 is performing some task when the controller pulls IFC active low, it interrupts that task and goes into a quiescent state, awaiting possible commands from the controller. |
| REN (Remote Enable) | The REN message is used in some GPIB systems to transfer devices from manual operation to operation by remote control. The 4924 does not respond to the REN message. |

EOI (End or Identify) The EOI signal can be used by the talker to indicate the end of a data transfer sequence. The talker activates EOI as the last byte of data is transmitted.

TRANSFER BUS

A handshake sequence is executed by the talker and the listeners over the transfer bus each time a byte is transferred over the data bus. These are the definitions of the transfer bus signal lines:

NRFD (Not Ready For Data) An active low NRFD signal indicates that one or more assigned listeners are not ready to receive the next byte. When all of the listeners for a particular data transfer have released NRFD, the NRFD line goes inactive high. This tells the talker that it may place the next byte on the data bus.

DAV (Data Valid) The DAV line is activated by the talker shortly after placing a valid byte on the data bus. An active low DAV signal tells each listener to capture the data presented on the data bus. The talker is inhibited from activating DAV when NRFD is active low.

NDAC (Data Not Accepted) The NDAC signal is held active low by each listener until it has captured the byte currently presented on the data bus. When all listeners have captured the byte, NDAC goes inactive high. This notifies the talker that it may remove the byte from the data bus.

HANDSHAKE SEQUENCE

Fig. 4-2 illustrates the "handshake" sequence by which the Transfer Bus regulates the exchange of data bytes over the Data Bus.

Initially, the listeners are holding NDAC (Data Not Accepted) active low, and the talker leaves DAV (Data Valid) inactive high. One or more of the listeners may be holding NRFD (Not Ready For Data) low, indicating that it is not yet ready to accept a data byte.

When all listeners are ready for data, NRFD goes inactive high. The talker then places a data byte on the Data Bus, waits briefly for this data to settle, and then pulls DAV low, indicating to the listeners that valid data is available on the Data Bus.

The listeners capture the data. Before beginning to accept the data, each listener pulls NRFD active low, indicating that it is not ready for the talker to place another data byte on the Data bus; then it reads the data, and, having done so, releases NDAC. When the slowest listener has

General Purpose Interface Bus

captured the data, NDAC goes inactive high, signaling the talker that all listeners have received the byte.

The talker then releases the DAV line and changes the data byte on the Data Bus. The listeners, sensing DAV go high, pull down NDAC, preparing for the next data byte.

The process then repeats for successive data bytes.

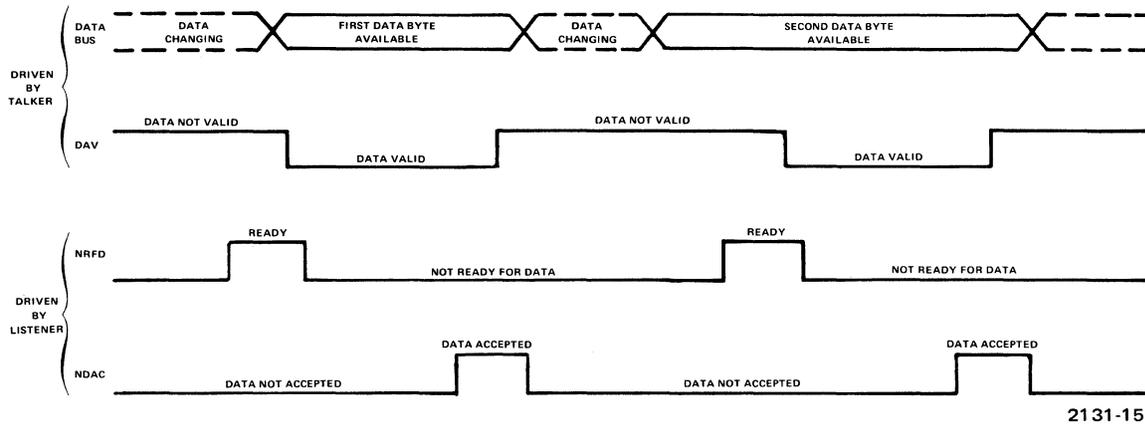


Fig. 4-2. GPIB Transfer Bus Handshake Sequence.

NOTE

According to the IEEE GPIB Standard: If several devices are connected to the GPIB bus, one more than 50% of the devices must be turned on (regardless of whether they are actually used), or the bus may be loaded down by the turned-off devices, causing a spurious SRQ signal on the bus.

Section 5

CIRCUIT DESCRIPTIONS

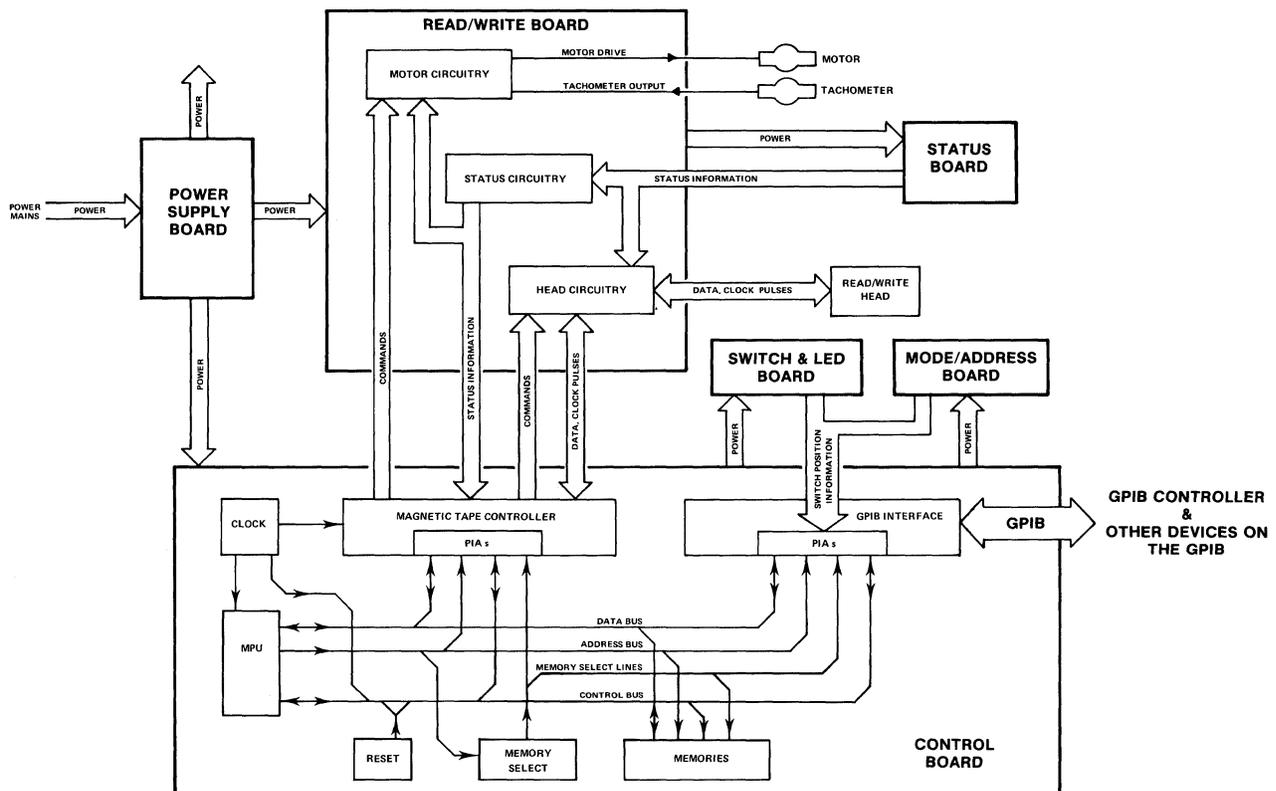
This section contains descriptions of the 4924's system architecture and of the circuitry.

SYSTEM ARCHITECTURE

The 4924's electrical components are mounted on six etched circuit boards: the Control, Switch and LED, Mode/Address, Status, Read/Write and Power Supply boards. A few components are mounted directly on the 4924 chassis.

Control Board

The Control board may be partitioned into these functional blocks: MPU, Clock, Reset, Memory Select, Memories, Magnetic Tape Controller, and GPIB Interface. (See Fig. 5-1.)



This block diagram also appears as a fold-out in Section 7, just before the schematic diagrams.

2131-16

Fig. 5-1. 4924 Block Diagram.

Circuit Descriptions

The MPU, or microprocessor unit, is a little computer which is the "brain" of the 4924. It communicates with its memories, and with the Peripheral Interface Adapters (PIAs), by means of three busses: the data, address, and control busses. They are described below, in the description of the MPU.

The Clock provides timing signals for the MPU and its memories, and for the Magnetic Tape Controller.

The Reset circuit is used to initialize the MPU and the PIAs at system power-up or power-fail. It communicates with them by the RESET line of the control bus.

The Memory Select circuitry decodes certain of the address bus lines to provide "enable" lines for the various memory packages. Its outputs, the memory select lines, could be regarded as supplementary lines for the address bus.

The Memories consist of RAMs (Random Access Memories) used for temporary storage of data, and ROMs (Read Only Memories) in which the MPU's program of instructions is stored. Individual memory packages are selected by the output lines of the Memory select circuitry; individual memory locations within each package are selected by the low-order address bus lines, which connect directly to the memory packages.

Except for the power supply, all other parts of the 4924 are regarded by the MPU as peripheral devices. Information from them, and commands to them, pass through Peripheral Interface Adapters (PIAs), whose registers are regarded by the MPU as memory cells and are addressed by it in the same way as other memory cells packaged in ROMs and RAMs.

The Magnetic Tape Controller, which includes two PIAs, interfaces between the MPU and the Read/Write Board. It relays commands from the MPU to the motor circuitry on the Read/Write board, and it relays status information from that board's status circuitry to the MPU. It tells the head circuitry whether to "read" or to "write", and in write mode it provides that circuitry with clock and data pulses. During a read operation, it receives clock and data signals from the head circuitry, sending the data on to the MPU, and monitoring the clock pulses to detect record marks and file marks. On detecting a record or file mark, it signals that fact to the MPU.

The GPIB Interface, as its name implies, is an interface between the MPU and the General Purpose Interface Bus. Under control of the MPU, it provides the "handshake" signals used in transferring bytes to and from the GPIB. Of the two PIAs in the GPIB Interface, one is used also to interface between the MPU and the switches on the 4924's front panel (Switch and LED board) and rear panel (Mode/Address board).

Switch and LED Board

The Switch and LED board holds the front panel switches (except the POWER switch) and the

front panel indicator lights. It also holds a few logical components associated with these switches and lights. It receives its power from, and communicates its information to, the Control board.

Mode/Address Board

The Mode/Address board holds only the rear-panel miniature rocker switches (mounted together in one dual-in-line package) and the pull-up resistors for these switches. It is connected by a cable to the Control board.

Status Board

The Status board contains connections for the switches that determine whether the cartridge is loaded or write-protected. Also on this board are the lamp and photo-transistors used to detect position marker holes in the tape. The status board receives its power from the Read/Write board, and communicates its information to the status circuitry on that board.

Read/Write Board

The Read/Write board may be functionally partitioned into three major blocks: Motor Circuitry, Status Circuitry, and Head Circuitry (Fig. 5-1).

The Motor Circuitry controls the motor, regulating its speed by means of feedback from the tachometer. Obeying the Control Board's Magnetic Tape Controller, it may cause the tape to Stop or to run forward or backward, at either 30 inches per second or 90 inches per second.

The Status Circuitry monitors the Status board's hole detector outputs to determine when the EOT (End of Tape), BOT (Beginning of Tape) and Load Point tape position markers have been sensed, relaying that information to the Magnetic Tape Controller on the Control Board. It also sends the BOT and EOT information to the Motor Circuitry, allowing that circuitry to shut down the motor if necessary. It monitors the Status board's cartridge position and write-protect switches, relaying their information to the Magnetic Tape Controller. It monitors voltages from the Motor Circuitry to detect tape motion and tape speed, and relays that information to the Magnetic Tape Controller.

The Head Circuitry, operating under control of the Magnetic Tape Controller, performs the actual reading and writing of data on the tape. It also monitors the Status board's Safe Switch, disabling itself from writing if the cartridge is write-protected.

Power Supply Board

The Power Supply Board provides unregulated power busses at +22 and -22 V, and regulated power supplies at +12 V, +5 V, and -12 V. It also provides connection for the 4924's cooling fan. Some of the power supply components are mounted directly on the 4924 chassis, rather than on the Power Supply board. These are: the POWER switch, the fan, the line fuse, the power transformer, and the regulator transistors.

CONTROL BOARD (For Serial Numbers B041 193 and Below)

The Control board is the largest of the 4924's etched circuit boards. It is comprised of several blocks, as shown in Fig. 5-1: Clock, Reset, MPU, Memory Select, Memories, Magnetic Tape Controller, and GPIB Interface. The Magnetic Tape Controller and the GPIB Interface are so complex as to deserve subdivision into blocks of their own; they will be discussed separately.

Clock

The Clock circuitry (Schematic 1-1) provides 819 kHz timing signals for the MPU ($\emptyset 1$ and $\emptyset 2$) and for the Memory Select circuitry, Memories and PIA's ($\emptyset 2L$). It also provides timing pulses every 20.8 μs (MAGCLK) for use by the Magnetic Tape Controller in generating the signals to be written on the tape.

The output of a crystal oscillator is fed to a divide-by-six counter to produce a 819.2 kHz square wave. This square wave is used to produce the MPU's two clocks, $\emptyset 1$ and $\emptyset 2$. However, $\emptyset 1$ and $\emptyset 2$ must be conditioned so that there is no overlap of their "high" states and so that their edges (transitions) have sufficiently fast rise and fall times.

This conditioning is done by a set-reset flip-flop comprised of two gates followed by inverting circuitry. The gates prevent $\emptyset 1$ from going high until $\emptyset 2$ has gone low, and vice versa. The inverting circuitry after each gate consists of a pull-up transistor to provide a sharp leading edge on the pulses and to give good saturation to the +5 V level, and a pair of pull-down inverters to bring each clock line low at the end of its positive pulse. Separate inverters drive the $\emptyset 1L$ and $\emptyset 2L$ lines, which provide clock signals to the external System Test Fixture connector J304 and to the memories, PIAs, and Memory Select circuitry.

The 819.2 kHz square wave from the divide-by-six counter is also fed to a divide-by-17 counter, which provides a 1.22 μs pulse once each 20.752 μs . This pulse appears on the MAGCLK lines, and is used by the Magnetic Tape Controller to time the writing of bits onto the tape.

Reset

The Reset circuit (Schematic 1-1) generates a pulse for initializing the MPU and the PIAs on

system power-up and on power failure. It comprises a differential operational amplifier functioning as a comparator, together with buffering output inverters and associated components.

During power-up the power supply voltages (+5 V, +12 V, -12 V) come up at widely varying times. A capacitor on the op amp's non-inverting (+) input delays the rise on that input until after the +5 V supply has stabilized. This delay also guarantees that a minimum number of clock pulses occur to initialize the MPU. Until then the comparator's output is negative, producing a low RESET pulse. Once the capacitor charges up, the comparator output goes positive. A dropping resistor and diode protect the output buffer inverter from excessive input voltage.

Should a power failure occur, and the +5 V supply drop below 4.75 V, the comparator will again produce a RESET pulse. Once again, the capacitor on the "+" input guarantees that enough clock cycles elapse before the RESET pulse is permitted to end.

MPU

The MPU block (Schematic 1-1) consists of the MC6800 microprocessor, together with its data bus transceivers, their steering inverters, and an inverter to drive the RWOC (Read/Write Open Collector) line.

The MC6800 microprocessor is a miniature computer which is the "brain" of the 4924. Following instructions stored in the Read Only Memories (ROMs), it acts on signals sent it from other parts of the 4924 or from the outside world on the GPIB, and issues commands to the various parts of the 4924, causing the motor to stop or to run forward or backward, the Head Circuitry to read from or write on the tape, data to be received from or sent out on the GPIB, etc.

To operate properly it requires two clock signals ($\emptyset 1$ and $\emptyset 2$) from the Clock circuitry and a RESET pulse from the Reset circuit to initialize it on power-up or power-fail.

Most of all, the MPU requires its memories: Read Only Memories (ROMs), Random Access Memories (RAMs), and Peripheral Interface Adapters (PIAs). The ROMs hold the MPU's instructions, while the RAMs serve as temporary storage areas for data. The PIAs, which appear to the MPU to be the same as other memories, serve as interfaces between the MPU and the other parts of the machine.

The MPU communicates with its memories by means of various signal lines, grouped functionally into three "busses": the data, address, and control busses.

The data bus, lines BD \emptyset to BD7, carries bytes of data between the microprocessor and its memories. As the microprocessor's data pins D \emptyset to D7 are limited in their drive capability, a pair of "data bus transceivers" interface between the MC6800 and the data bus.

Circuit Descriptions

Lines A8 to A12 of the address bus drive the Memory Select circuitry, which selectively enables the various memory packages. Lines A0 to A10 select specific memory locations within the memory packages. Lines A13 to A15 are not used.

Unlike the data and address busses, the control bus is not really a "bus" in the sense of a collection of lines together carrying the same information; it is, rather, the set of control lines by which the flow of addresses and data over the other two busses is controlled. These lines are:

- (a) RWOC (Read/Write Open Collector), which tells whether data is to be read from, or written into, a memory location (and which may be pulled low by the external System Test Fixture as well as by the MPU);
- (b) VMA (Valid Memory Address), which indicates the availability of a valid memory address on the address bus, and which is used to enable the Memory Select circuitry;
- (c) RESET, used to initialize the MPU and PIAs on power-up and power-fail;
- (d) IRQ (Interrupt Request), used by the PIAs to signal the MPU of their request for service;
- (e) NMI, used by the PIAs to request a non-maskable interrupt;
- (f) GO/HALT, used by the external System Test Fixture to stop the microprocessor for a DMA (Direct Memory Access) operation;
- (g) BA (Bus Available), used to enable the Memory Select circuitry when the System Test Fixture has stopped the MPU for DMA; and
- (h) \emptyset 2L (Phase Two Clock), used to time memory access operations.

Memory Select

The Memory Select circuitry (Schematics 1-1 and 1-4) is used to decode the high-order memory address bits A8 to A12, selectively enabling the various memory packages. This circuitry also has a gate and an inverter (Schematic 1-1) which provide an "enable" signal (E) for the external System Test Fixture, deriving this signal from the phase two clock (\emptyset 2L-0) and the VMA signals.

The circuitry uses three address decoders, which enable each other sequentially. The first of these (Schematic 1-1) is enabled by a NOR gate only when either a VMA or BA signal is available from the MPU. Its outputs S2, S3, ..., S7 select the various Read Only Memories (Schematic 1-4). Its EN output enables the second address decoder.

The second decoder (Schematic 1-4) provides an S1 output to enable the PIAs and an S0 output for enabling the third decoder.

The third decoder selects the various Random Access Memories. These RAMs must be enabled only during the "high" of the phase two clock; so the S0 output of the second decoder and the phase two clock $\phi 2L$ are ANDed together to enable this third decoder, which in turn selectively enables the RAMs.

The effect of the Memory Select circuitry is to assign to each memory package or PIA a different block of addresses in the microprocessor's memory address space. Table 5-1 summarizes these assignments.

In using the table, one should bear in mind that, since the address bits A13 to A15 are ignored by the 4924, there is a "memory wrap-around" effect: addresses which differ only in these high-order bits are considered equivalent by the 4924. Thus "2000", the next hexadecimal address after "1FFF", addresses the same memory cell as "0000"; again, "FFFF" is equivalent to "1FFF".

Table 5-1

4924 MEMORY ADDRESS ASSIGNMENTS

Hexadecimal Address	Device Selected	
0000 - 00FF	U551, U253	} Random Access Memories
0100 - 01FF	U453, U251	
0200 - 02FF	U451, U151	
0300 - 040B	Unused	
040C - 040F	U315	
040C	PIAGPA Control Register	} PIA s
040D	PIAGPA Peripheral & Data Direction Registers	
040E	PIAGPB Control Register	
040F	PIAGPB Peripheral & Data Direction Registers	
0410 - 0413	Unused	
0414 - 0417	U331	
0414	PIAMTR Control Register	
0415	PIAMTR Peripheral & Data Direction Registers	
0416	PIAMTW Control Register	
0417	PIAMTW Peripheral & Data Direction Registers	
0418 - 041B	U341	
0418	PIAMTA Control Register	} PIA s
0419	PIAMTA Peripheral & Data Direction Registers	
041A	PIAMTB Control Register	
041B	PIAMTB Peripheral & Data Direction Registers	
041C - 0427	Unused	
0428 - 042B	U321	
0428	PIAKYB Control Register	} PIA s
0429	PIAKYB Peripheral & Data Direction Registers	
042A	PIAADR Control Register	
042B	PIAADR Peripheral & Data Direction Registers	
042C - 07FF	Unused	
0800 - 0BFF	U55	} Read Only Memories
0C00 - 0FFF	U155	
1000 - 13FF	U255	
1400 - 17FF	U355	
1800 - 1BFF	U455	
1C00 - 1FFF	U555	

Memories

The memory packages (RAMs and ROMs) appear in schematic 1-4. The RAMs are each organized into 256 words of 4 bits each, but the MPU expects each memory location to hold eight bits. So, pairs of RAMs are selected together. One RAM contains the four low-order bits of a memory location; the other, the four high-order bits.

U555 is the ROM addressed by the highest addresses in the 4924's memory address space (hexadecimal 1C00 to 1FFF). Its enabling may be overridden by a high provided to test connector J304's A2 pin from the external System Test Fixture.

PIAs

The Peripheral Interface Adapters in the GPIB Interface (Schematic 1-2) and the Magnetic Tape Controller (Schematic 1-3) contain registers which are addressed by the MPU in the same way as other memory locations. These devices differ from the other memories, however, by providing a way to interface the MPU with the rest of the machine and with the outside world.

Each PIA is selected when two of its "chip select" pins (CS0, CS1) are high and one (CS2) is low. The two "register select" pins are connected to the low-order address lines A0 and A1, so that the PIA occupies four adjacent locations in the MPU's memory address space. The two lower addresses, for which RS1 is "0", refer to the "A" half of the PIA, and the two higher addresses, for which RS1 is "1", to the "B" half.

Each half of the PIA has three registers. These are the Control, Peripheral, and Data Direction registers. The Control Register is addressed at an even-numbered address (for instance, 0414). The Peripheral and Data Direction registers share the same odd-numbered address (0415). A bit set by the MPU in the Control Register (in our example, address 0414) determines which of these two registers is accessed by the MPU when it addresses the odd-numbered address (0415) for that half of the PIA.

The Peripheral Registers are the PIA registers used most in the 4924's operation, as they provide the interface for the MPU to the world beyond its memories. Each half of the PIA has eight pins (PA0 to PA7 or PB0 to PB7) through which its Peripheral Register receives data from, or sends data to, external devices. Each bit of a Peripheral Register is programmed to receive or transmit data according to the state of the corresponding bit in that register's Data Direction Register. For instance, a "0" in the low-order bit of Data Direction Register A causes the low-order bit of Peripheral Register A to receive data from the PA0 pin. Similarly, a "1" in the low-order bit of Data Direction Register A would program the low-order bit of Peripheral Register A to transmit data to the PA0 pin.

For instance, in PIA U331 (Schematic 1-3), all the bits of Peripheral Register A act as inputs; so Data Direction Register A must have all zeroes programmed into it. Peripheral Register B is used to send data out; so all the bits of Data Direction Register B must be ones.

Each half of the PIA also has two pins (CA1 and CA2, or CB1 and CB2) by which its Control Register can interact with the outside world. When these are used as inputs, the Control Register can be programmed to generate an interrupt request when the voltage at these inputs changes. This it does by pulling the IRQA or IRQB pin low. These pins are connected to the MPU's IRQ or NMI control lines, so that a low generates an interrupt request.

MAGNETIC TAPE CONTROLLER

The Magnetic Tape Controller on the Control Board includes these functional blocks (Schematic 1-3): PIA s, Write Shift Register, Read/Write Shift Register, Write Control, Read/Write Shift Register Input Gating, Clock Gating, Write Output Gating, Timer, Cartridge Removal Circuit, Debouncers, and Tape Monitor.

PIAs

PIAMTR and PIAMTW are the "A" and "B" halves of a single Peripheral Interface Adapter package. PIAMTR's Peripheral Register is used during read operations to receive into the MPU's memory the data being read from the tape. PIAMTW's Peripheral Register is used in write operations to send out from the MPU the data to be written on the tape. The control ports CA1, CB1, and CB2 are used to interrupt the MPU during certain operations, while control port CA2 is used as an output, to control the Timer.

PIAMTA and PIAMTB are the "A" and "B" halves of another PIA. Their Peripheral Registers perform a variety of input and output functions, carrying data to the MPU and commands from it. All four of their control ports are used as inputs, generating MPU interrupts upon detection of record marks or inter-file gaps.

Write Shift Register

During "write" operations, the Write Shift Register (Schematic 1-3) converts data from parallel to serial format. Each data byte from PIAMTW is loaded into it in parallel, then shifted out serially and passed through the Write Output Gating to become the WRITE DATA signal. This signal is sent to the Read/Write board's Head Circuitry to be written on the tape.

Read/Write Shift Register

The Read/Write Shift Register performs two functions. During a read operation, it is a serial-to-parallel converter. It accepts the serial READ DATA signal (after it has passed through the Read/Write Shift Register Input Gating) and converts each serial byte to eight parallel bits to be read by PIAMTR.

During a write operation, the Read/Write Shift Register becomes part of a mechanism which produces a waveform used to control the write operation. For this, refer to the description of the Write Control circuitry.

Write Control

The Write Control is used, together with the Read/Write Shift Register, to generate a waveform used to control several of the Magnetic Tape Controller's blocks during a write operation. This waveform is low except when the 4924 is writing data bytes onto the tape; then it is high for eight MAGCLK pulses, low for the next two pulses, high for eight, low for two, etc.

Refer to Fig. 5-2, which shows an extract from Schematic 1-3 and pertinent waveforms.

Shortly before a series of data bytes is written on the tape, READ-0/WRITE-1 is high and GNFR (Generate NFRs) and WENABLE (Write Enable) are low. FF2's \overline{Q} is high, the R/W Shift Register's Q_H is high, and FF1 is cleared. FF1's Q output, which makes the control waveform, is low. With FF1-Q low, the Clock Gating prevents MAGCLK pulses from reaching the Write Shift Register or the WRITECLOCK output.

To start the writing of a series of data bytes on the tape, the MPU sends high the WENABLE input to Gate 2. With both FF1- \overline{Q} and FF2- \overline{Q} high, Gates 1 and 2 present a "1" to FF2-D.

At the first MAGCLK pulse, FF2- \overline{Q} goes low, clearing the R/W Shift Register, which in turn enables FF1. Gates 1 and 2 then present a "0" at FF2-D, and a "1" at FF1-D.

At the second MAGCLK pulse, FF2- \overline{Q} goes high again, enabling the Read/Write Shift Register (which, having been cleared, has "0's" in all its stages). FF1-Q goes high, and FF1- \overline{Q} low, causing Gate 1 to send a "1" to FF1-D and "0" to FF2-D, latching high FF1-Q and FF2- \overline{Q} on successive clocks.

Now that the control waveform from FF1-Q is high, the Clock Gating will pass MAGCLK pulses to the Write Shift Register. These pulses are also passed through the Output Gating to become the WRITECLOCK.

For the third, fourth, ..., and ninth MAGCLK pulses, FF1-Q remains high. With FF1-Q high, the tenth MAGCLK pulse does pass through the Clock Gating. However, this pulse, in clocking the Read/Write Shift Register, produces a "1" at that register's Q_H output; the "0's" that were in the shift register have all been shifted out. The "1" at Q_H clears FF1, sending the control waveform low. Gate 1 and Gate 2 then present a "1" to FF2-D.

Things now are just as they were before the first MAGCLK pulse; the next pulse begins a new cycle. On the first two MAGCLK pulses of each cycle, the control waveform from FF1-Q is low, disabling the WRITECLOCK and writing an inter-character gap (ICG) of about 62 μ s. During

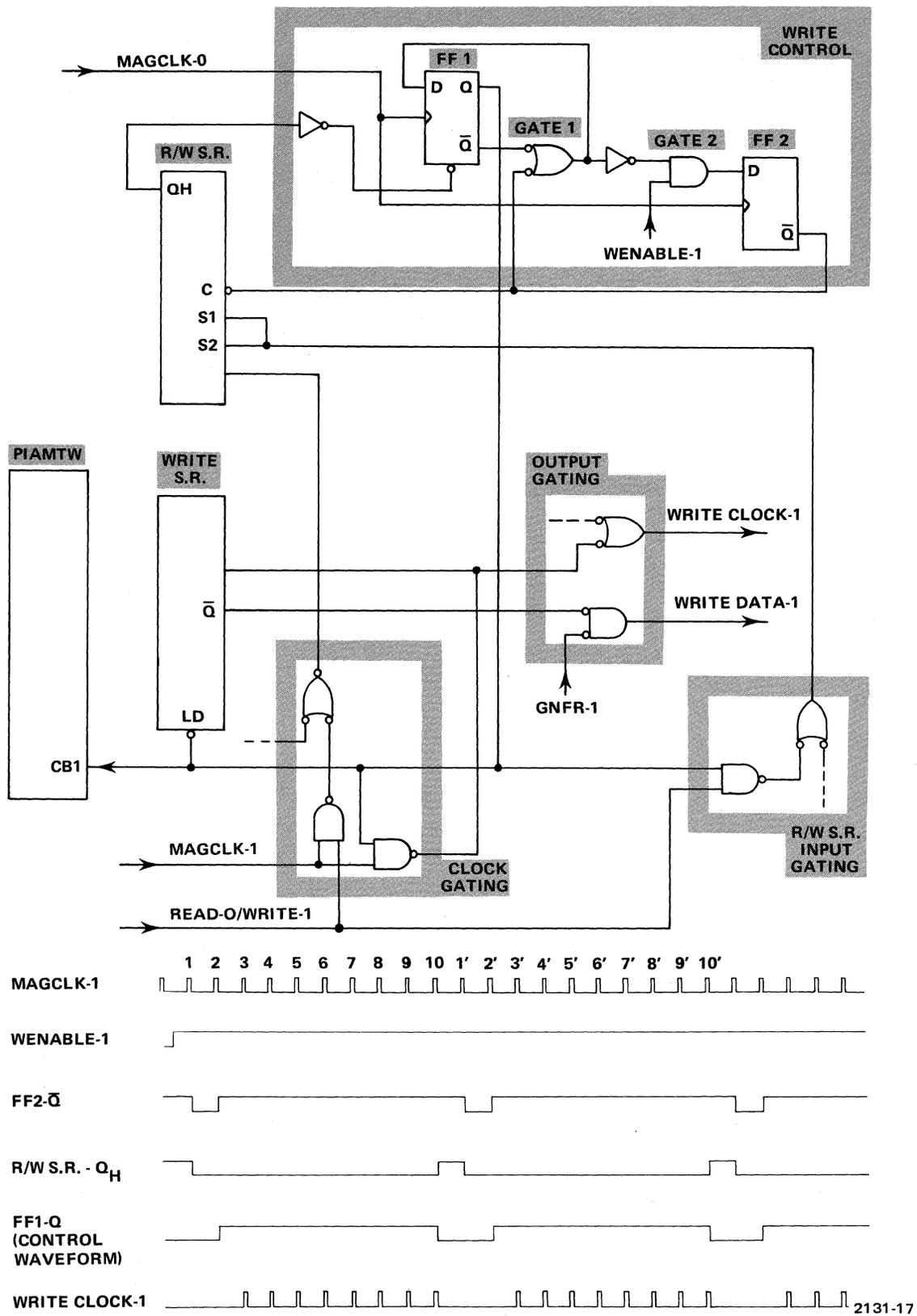


Fig. 5-2. Write Control Circuitry and Waveforms.

the remaining eight MAGCLK pulses of the cycle, FF1-Q is high, enabling the WRITE CLOCK and causing data to be serially shifted out of the Write Shift Register.

As the write control waveform from FF1-Q goes low at the end of each cycle, it disables the Write Shift Register, putting it in "load" mode. The falling edge of this waveform, fed to PIAMTW's CB1 port, causes the PIA to interrupt the microprocessor, informing it that the data has been shifted out and that it may load another data byte into the Write Shift Register.

The writing of data on the tape is terminated by the MPU's sending WENABLE-1 low. The current cycle of the Write Control circuitry is then completed, this allows the Write Shift Register to finish shifting out the last data byte. The Write Control circuitry then resumes its initial state until again enabled by a WENABLE signal.

Read/Write Shift Register Input Gating

Since the Read/Write Shift Register (Schematic 1-3) has different functions during the "read" and "write" operations, it must also have different inputs. The Read/Write Input Gating is a logic tree which accomplishes this; during "read", it feeds the READ DATA signal to the shift register, and during "write" it presents the Write Control waveform to the shift register.

Clock Gating

The Clock Gating circuitry (Schematic 1-3) provides switching of the clock pulses to the two shift registers. During "read", it steers the READ CLOCK pulses to the Read/Write Shift Register. During "write", it provides that register with MAGCLK pulses. During "write", but only during the high of the Write Control's output waveform, it feeds MAGCLK pulses to the Write Shift Register and (through the Write Output Gating) to the WRITE CLOCK line.

Write Output Gating

The Write Output Gating circuitry (Schematic 1-3) sends the WRITE CLOCK and WRITE DATA signals on to the Read/Write board during "write" operations.

The inverting-input AND gate in this circuitry passes serial data bytes from the Write Shift Register to the WRITE DATA output. When the periods of no flux reversal (NFRs) which comprise record marks and file marks are being written, the GNFR output from PIAMTB is high, and this gate holds the WRITE DATA line low. Thus, the flux reversals separating the NFRs in record and file marks are all written on the zeroes track of the tape.

The other two gates drive the WRITE CLOCK line, producing WRITE CLOCK pulses when either (a) the Write Shift Register is being clocked, sending a data byte out on the WRITE DATA line, or (b) a record mark or file mark is being written (GNFR is high) and the CA2 port of PIAMTR outputs a pulse. The NAND gate in this circuitry isolates the CA2 port's output from

the WRITE CLOCK line except when record or file marks are being written; this permits the MPU to use the Timer at other times than during the writing of record and file marks.

Timer

The Timer (Schematic 1-3) is a one-shot multivibrator which provides the MPU with a hardware timing mechanism independent of the Clock.

PIAMTR's CA2 output is normally high. To start a timing cycle, a read of PIAMTR causes a momentary low pulse from the CA2 port. This pulse, after inversion, triggers the one-shot, which sends its output high for about 40 μ s. This high is applied to PIAMTA's PA0 input.

Meanwhile, after possibly performing some other tasks, the MPU enters a loop in its program, continually checking the contents of PIAMTA's Peripheral Register. When the one-shot times out, PIAMTA's PA0 pin goes low; in reading the Peripheral Register, the MPU detects this low, thus learning that the timing cycle has been completed.

Cartridge Removal Circuit

The Cartridge Removal Circuit (Schematic 1-3) includes three gates, two of which comprise a set-reset flip-flop. When the tape cartridge is removed from its slot, a switch on the Status board grounds the LOAD SWITCH line, setting the flip-flop, which sends the NOCART line high. This high is presented to PIAKYB's PA6 input (Schematic 1-2) to inform the MPU of the cartridge's removal. The flip-flop is reset when the MPU causes PIAMTA's PA1 output (Schematic 1-3) to toggle.

The other gate in the Cartridge Removal Circuit drives the LOAD line, sending it high on a RESET pulse or when the cartridge is removed. The LOAD signal initializes the Stop Tape Control and Tape Hole Monitor logic on the Read/Write board.

Debounce

The Debouncers (Schematic 1-2) are two-sixths of an MC14490 contact bounce eliminator, the other four-sixths of which are used in the GPIB Interface (Schematic 1-2). These debouncers clean up the BOT and EOT signals from the Read/Write board, delaying them about 20 μ s, and present the clean, delayed signals to PIAMTB's CB1 and CB2 ports, where they are used to set flags in the control register of the PIA indicating detection of the BOT or EOT tape position markers.

NOTE

The BOT and EOT signals are not used to cause MPU interrupts to prevent the tape from running off its spools. Nor are they monitored by the MPU during rewind operations to see when the tape is fully rewound. Instead, the tape is kept from running off its spools by the Stop Tape Control (in the Motor Circuitry). During rewind, the MPU monitors the TNIM (Tape Not In Motion) signal to see when the Stop Tape Control has halted the tape; it is by TNIM (not by BOT) that the MPU learns that the tape has been fully rewound.

Tape Monitor

During read operations, the Tape Monitor (Schematic 1-3) watches the READCLOCK pulses, using them to detect the end of each serial byte as well as record marks and file marks. When the tape skips fast forward or fast reverse, it detects the long blank spaces between files. On detection of the end of a serial byte, or of a record mark, file mark, or inter-file gap, it signals to a PIA control port, causing the PIA to generate an MPU interrupt.

The Tape Monitor is comprised of an NFR Detector, a Record and File Mark Detector, a Bit Counter, and a File Finder.

NFR Detector. The NFR Detector, a one-shot multivibrator, detects the NFRs (periods of no flux reversal) which comprise record marks and file marks.

With the tape running at its normal speed and the FNFR (Find NFRs) line high, the first READCLOCK pulse of each data byte triggers the one-shot, and succeeding pulses within the byte re-trigger it, keeping its output high for the duration of the byte. At the end of the byte, however, an inter-character gap (ICG) of about 60 μ s elapses with no READCLOCK pulses; the one-shot times out, and the negative transition at its Q output signals the detection of an NFR. Similarly, after each of the clock pulses separating the NFRs within record or file marks, the NFR detector times out, signalling detection of an NFR.

Record and File Mark Detector. The Record and File Mark Detector is a counter clocked by the negative transitions from the NFR detector's output which signal the detection of NFRs. A record mark consists of four NFRs; so at the count of four, the counter's Q_C output drives the RMARK line high, signalling detection of a record mark. Similarly, at the count of eight, Q_D signals detection of a file mark on the FMARK line.

The Record and File Mark Detector may be reset by a pulse from the Bit Counter, or by sending FNFR low.

Circuit Descriptions

Bit Counter. Since the NFR Detector remains triggered for the duration of each data byte, its \overline{Q} output is low. This enables the Bit Counter, which counts the READCLOCK pulses within each byte. At the count of four, its Q_c output resets the Record and File Mark Detector; this prevents that circuit from counting the inter-character gaps and giving erroneous record mark or file mark indications. At the count of eight, its Q_d output sends the READIT line high; this signals to the MPU that all eight bits of the character have been clocked into the Read Shift Register, and that it may now read into PIAMTR the parallel data byte presented at that shift register's output.

Whenever the NFR Detector times out, its \overline{Q} output resets the Bit Counter.

File Finder. When the tape is skipping fast forward or fast reverse, the MPU must know when inter-file gaps occur. The File Finder is a one-shot used to detect these.

With the tape running at the faster speed, the inter-character gaps and the NFRs within record and file marks are too brief for the NFR Detector to time out; thus the Bit Counter is not reset, but keeps running. Its Q_a output is used to trigger and re-trigger the File Finder one-shot, which has a 31.5 ms period. At the faster tape speed, re-triggering occurs frequently enough to keep the File Finder's \overline{Q} output low, except during the long inter-file gaps. When these occur, the one-shot times out, sending the FILEFND line high and causing PIAMTA to generate an MPU interrupt.

The MPU may disable the File Finder by causing PIAMTB to set its PB7 output low.

GPIB INTERFACE

The GPIB Interface on the Control board (Schematic 1-2) interfaces between the General Purpose Interface Bus and the 4924's microprocessor. Its PIA package U321 (PIAADR and PIAKYB) also interfaces between the MPU and the switches on the front panel (Switch and LED Board) and the rear panel (Mode/Address board).

The GPIB Interface includes PIA's, Transfer Bus and Management Bus Transceivers, a Transfer Bus Transceiver Steering circuit, a Data Bus Interface, Listen/Talk Steering circuitry, Debouncers, a "Hello" circuit, Hand Gating, Source Handshake circuitry (SH), Acceptor Handshake circuitry (AH₁ and AH₂), and AH Enable circuitry. Refer to Schematic 1-2 to locate these circuit blocks.

Before reading the GPIB Interface circuit descriptions, be sure to read Section 4, which describes the GPIB's functions.

PIAs

PIAs PIAGPA and PIAGPB do most of the interfacing between the MPU and the GPIB Interface circuitry. PIAGPA's peripheral register transmits data between the MPU and the GPIB data

bus, while PIAGPB's peripheral register transmits a variety of signals between the MPU and the GPIB Interface circuitry. The control ports CA1, CA2, CB1, CB2 of PIAGPA and PIAGPB are used to generate MPU interrupts.

PIAADR's CB2 port relays the SHAKE signal from the MPU to the GPIB circuitry, while the rest of PIAADR and PIAKYB are really independent of the GPIB interfacing function; they interface between the MPU and the rear panel switches on the Mode/Address board and between the MPU and the front panel switches on the Switch and LED board. PIAADR's CB1 port is functionally part of the Magnetic Tape Controller, as it carries the LD POINT interrupt signal from the Read/Write board to the MPU.

Transfer Bus Transceiver

The Transfer Bus Transceiver (Schematic 1-2) provides interfacing to the three GPIB transfer bus lines DAV, NRFD and NDAC, and to one of the management bus lines, EOI. Its internal schematic is illustrated in Fig. 5-3. Each input or receive port (such as AI) at all times follows the signal presented to the corresponding GPIB port (A). An output or transmit port (such as AO) drives the GPIB line connected to its GPIB port with its open-collector driver only if the transceiver is enabled with a low at its enable input. The GPIB ports are active-low to conform with the GPIB standard, while the receive ports and transmit ports are active-high.

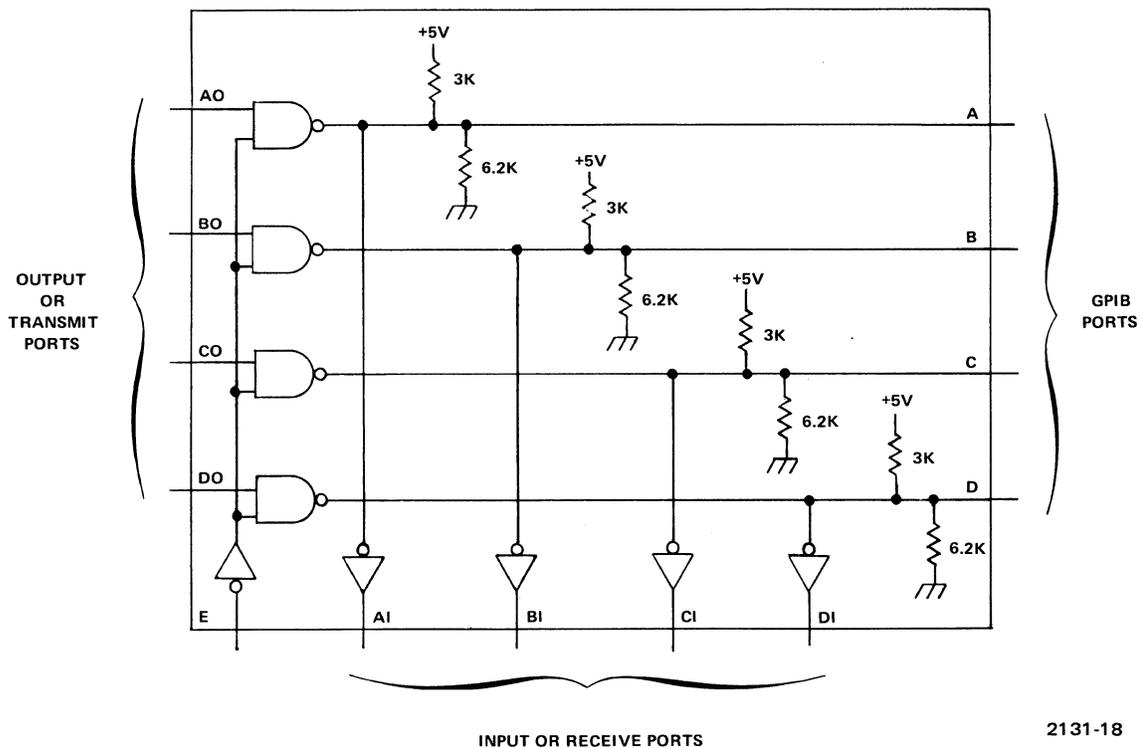


Fig. 5-3. GPIB Transceiver.

Management Bus Transceiver

The Management Bus Transceiver (Schematic 1-2), like the Transfer Bus Transceiver, is a type 3441 GPIB transceiver. Unlike the Transfer Bus Transceiver, it is always enabled to transmit (its enable input is grounded). However, since the 4924 is not permitted to send the ATN, IFC or REN signals over the GPIB, the corresponding transmit ports (CO, BO, AO) are grounded. Any time that a high is presented at its DO port, however, it will transmit the SRQ (Service Request) message on the GPIB.

Transfer Bus Transceiver Steering

The Transfer Bus Transceiver is only enabled to transmit when the 4924 is to receive or send bytes over the GPIB. This occurs when (a) the 4924 has been addressed as a "talker" or "listener", and (b) when the controller is holding ATN active, commanding all GPIB devices to "listen" to the addresses or commands on the GPIB data bus. The Transfer Bus Transceiver Steering gate (Schematic 1-2) detects these two conditions and enables the Transfer Bus Transceiver when either of them occurs.

Data Bus Interface

The Data Bus Interface (Schematic 1-2), as its name implies, is an interface between the 4924 and the GPIB's data bus. It includes two GPIB transceivers similar to the ones used as the Transfer Bus and Management Bus Transceivers. Since the "receive" ports of these transceivers are always active, the Data Bus Interface also includes a pair of "quad tri-state buffers" which effectively isolate the GPIB transceiver "receive" ports during "transmit", but connect them to PIAGPA during "receive".

Listen/Talk Steering

The PB5 output of PIAGPB is sent low by the MPU when bytes are to be transmitted out over the GPIB, and high when bytes are to be received. The Listen/Talk Steering Circuitry (Schematic 1-2) uses this signal and the ATN signal received from the GPIB as inputs, and provides outputs to steer various circuit blocks in the GPIB Interface between their "listen" and "talk" modes:

- (a) When PIAGPB-PB5 says "listen", or ATN is active, the Data Bus Interface's GPIB transceivers are disabled from transmitting. On "talk", with ATN inactive, they are enabled.
- (b) The Data Bus Interface's tri-state buffers are enabled on "listen", and disabled on "talk".
- (c) The SH (Source Handshake) circuitry's output is enabled on "talk", and disabled on "listen".

(d) The AH Enable and Hand Gating circuits are provided inputs to indicate whether "listen" or "talk" mode is active.

Debounce

The Debouncers (Schematic 1-2) comprise four-sixths of an MC14490 contact bounce eliminator. They "clean up" the ATN, IFC, NDAC and HAND signals, in order to prevent false MPU interrupts due to "ringing" on these lines. They debounce both the rising and the falling edges of the signal.

Hello

The Hello circuit (Schematic 1-2) is a gate used by the 4924 to detect, prior to transmitting data over the GPIB, whether there are any "listeners" on the GPIB to receive the data. If a listener is on the line, then it will be pulling either the NRFD (Not Ready For Data) or NDAC (Data Not Accepted) line active. If neither line is in its active state, then no listener is on the line, and the Hello circuit will signal this fact to the MPU by pulling the NOBODY line high.

If nobody is on the line to "listen", the 4924 will not attempt to "talk"; this prevents the 4924 from being "hung up" while waiting for a non-existent listener to respond to its handshake signals. (In the Manual mode, the 4924 will then turn off the command it was issued, extinguishing the LED on the front panel.)

Hand Gating

The Hand Gating circuitry (Schematic 1-2) is used during the three-wire "handshake" procedure by which the GPIB transfer bus regulates the flow of data bytes over the data bus. Its output is passed through a debouncer, becoming the HAND signal which is applied to PIAGPA's CA1 port to generate an MPU interrupt.

When data is to be transmitted, this interrupt informs the MPU that the "listeners" on the GPIB have all released the NRFD line and that the 4924 may now place a byte on the data bus. (When that byte has been placed, the MPU will send the SHAKE signal, causing the SH circuitry to transmit the DAV message.)

When data is to be received, the HAND interrupt informs the MPU that the "talker" on the GPIB has sent the DAV (Data Valid) signal, indicating that a byte has been placed on the GPIB data bus. (When the 4924 has read that byte, the MPU will send the SHAKE signal, causing the AH circuitry to transmit the "data accepted" message.)

The Hand Gating Circuitry, then, is a logic tree which sends the HAND signal when (a) the 4924 is in "listen" mode and the DAV signal is true, or (b) the 4924 is in "talk" mode and the NRFD signal is false.

Source Handshake

The SH (Source Handshake) circuitry (Schematic 1-2) is used to generate "handshake" signals on the GPIB's transfer bus during the transmission of data from the 4924.

The SH circuitry includes a flip-flop which is set when (a) the 4924 is in "listen" mode or, moreover, (b) the DAC (Data Accepted) signal is true. When the "listeners" on the GPIB indicate that they are all ready to accept data (NRFD false), the HAND signal from the Hand Gating circuitry causes the MPU to place a byte on the data bus and send the SHAKE signal. This SHAKE signal clears the flip-flop in the SH circuitry, sending its output high. This sends a "1" through an AND gate to the Transfer Bus Transceiver, which sends the DAV signal on the GPIB.

The AND gate on the output of the flip-flop disables the SH circuitry from transmitting the DAV signal whenever the 4924 is in "listen" mode.

Acceptor Handshake

The Acceptor Handshake circuitry (Schematic 1-2) is used to generate "handshake" signals for the GPIB transfer bus during reception of bytes from the GPIB data bus. It feeds its outputs to the Transfer Bus Transceiver which keys the appropriate GPIB transfer bus lines. It includes the AH₁, AH₂, and AH Enable functions. Refer to Fig. 5-4.

The AH Enable gate within this functional block enables the AH circuitry whenever the 4924 is not in "talk" mode, and also whenever the ATN signal is true. Thus, even while the 4924 has not been addressed, the AH circuitry is enabled. This does not matter, however, as the Transfer Bus Transceiver Steering gate prevents the Transfer Bus Transceiver from transmitting.

The 4924 will be ready to accept data when (a) the AH circuitry is enabled, and (b) the talker has not yet placed a new byte on the GPIB data bus (DAV false). (With DAV false, the set-reset flip-flop in the AH₁ block is set.) Under these circumstances, the logic in the AH₁ block provides a "0" to the Transfer Bus Transceiver's BO port, signaling to the GPIB that the 4924 is ready to accept data.

When all GPIB "listeners" are ready for data, the GPIB's NRFD line goes inactive high (NRFD false). The "talker" then places a byte on the data bus, and sends the DAV message.

Immediately on receipt of the DAV message, the logic in the AH₁ block causes the Transfer Bus Transceiver to send the NRFD message, inhibiting the "talker" from placing another byte on the data bus. Also the Hand Gating circuitry and its associated debouncer produce the HAND signal, which generates an MPU interrupt. The interrupt causes the MPU to read the byte available on the data bus, and then to send the SHAKE signal.

The HAND signal is also fed to the logic in the AH₂ block, which acts as a "NRFD hold" circuit. That is, it prevents the 4924 from sending the "ready for data" signal until the DAV signal has

gone away and this information has had time to clock its way through the debouncer to send the HAND signal low. This prevents the 4924 from missing a HAND interrupt when a very fast "talker" is on the line.

Until the MPU has read the data byte, the flip-flop in the AH₁ block will be set, providing a "1" to the Transfer Bus Transceiver's CO port. This causes a NDAC message to be sent on the GPIB. When, however, the MPU has read the data, it sends the SHAKE signal, which resets this flip-flop and causes the Transfer Bus Transceiver to signal that the 4924 has accepted the data by letting the NDAC line go inactive high.

When all "listeners" on the GPIB have accepted the data, the "talker" can place another byte on the data bus and start the handshake procedure again by sending the DAV message.

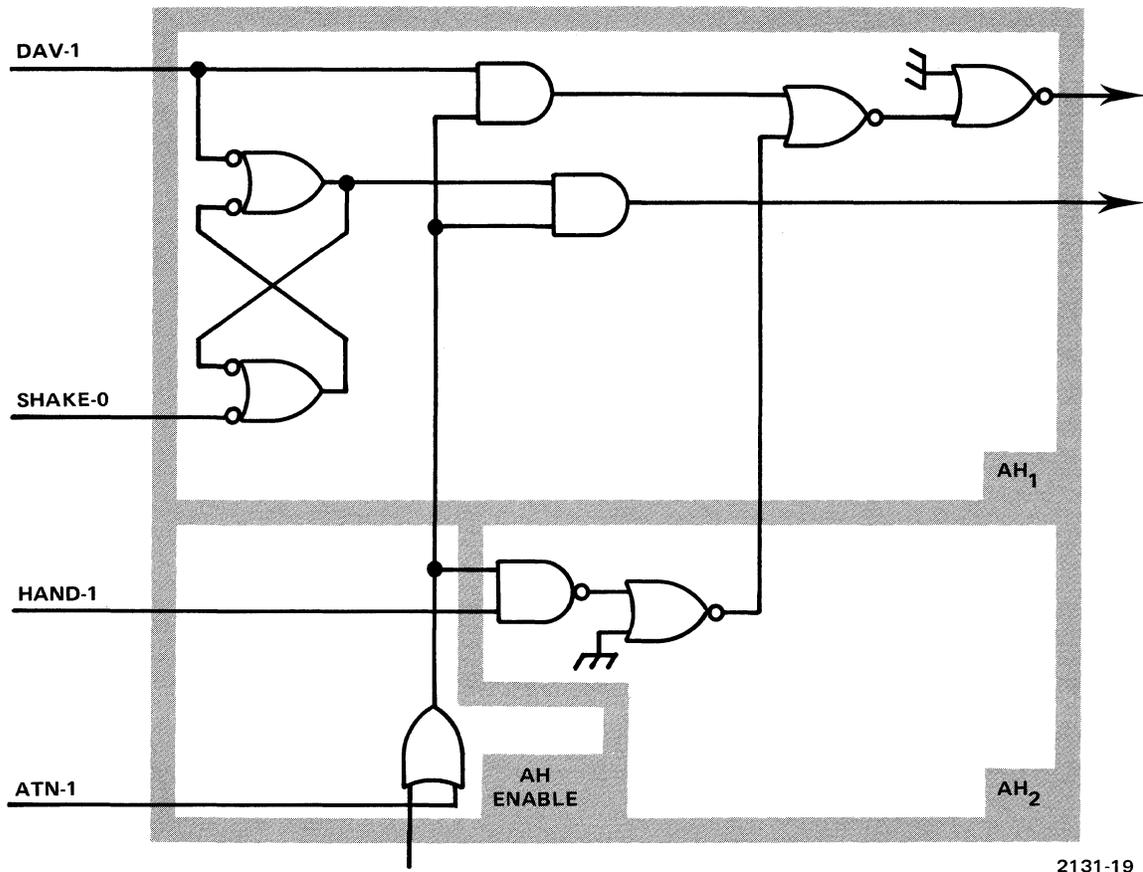


Fig. 5-4. Acceptor Handshake (AH) Block.

Interfacing The ATN Line

The ATN signal may not be sent by the 4924; hence the CO port of the Management Bus Transceiver is tied to ground.

When the ATN signal is received, it is fed from the Management Bus Transceiver's CI port to:

(a) the Debounce, which present a debounced version of it (ATNDLY) to PIAGPB, setting flags in PIAGPB's control register to tell if ATN is being asserted or if it is going away, and setting the peripheral register's PB4 bit to show the DC level of ATN;

(b) the Transfer Bus Steering, which immediately enables the Transfer Bus, so that "acceptor handshake" signals may be transmitted;

(c) the AH Enable gate, which enables the Acceptor Handshake circuitry; and

(d) the Receive/Transmit Steering, which immediately disables the Data Bus Interface from transmitting.

When the MPU responds to the interrupt, it will steer the GPIB Interface into "receive" mode (if it is not already in that mode), thus enabling the Data Bus Interface to pass the received byte to PIAGPA.

As long as ATN is held active, the 4924 will be in "receive" mode, receiving universal commands or device addresses from the GPIB controller. If the MPU, in receiving these bytes, recognizes its own talk or listen address, it will cause PIAGPB's PB6 port to send the ADDRESS signal to the Transfer Bus Transceiver Steering gate. (Then, when the ATN line is released, the Transfer Bus Transceiver will still be enabled to transmit.)

When the GPIB controller releases the ATN line, and ATNDLY signals this to the MPU via PIAGPB's IRQ line, the MPU will follow any commands just given it by the controller.

Interfacing Other GPIB Management Bus Lines

The 4924 may send, but not receive, the SRQ message. PIAGPB's PB1 port is used by the MPU to send the SRQ message (which requests service from the GPIB controller). Since the 4924 may not respond to the SRQ message, the DI port of the Management Bus Transceiver is left unconnected. (It is not even shown in Schematic 1-2.)

The 4924 may not send the IFC (Interface Clear) message, so the Management Bus Transceiver's BO is tied to ground. When an IFC message is received, it is sent from the Management Bus Transceiver's BI port through the Debouncer to PIAGPA's CA2 input, where it causes an MPU interrupt. This interrupt causes the MPU to stop whatever it is doing and await possible commands to be sent from the GPIB controller.

The 4924 may neither receive nor send the REN message; so the Management Bus Transceiver's AO is tied to ground and its AI port left unconnected.

When a series of data bytes is being sent over the GPIB, the EOI (End Or Identify) message may be used by the "talker" to mark the last byte in the data string. When acting as a "talker", the 4924 may send this signal from PIAGPB's PB0 port along the TRANSMIT EOI line and through the Transfer Bus Transceiver out onto the GPIB. When the 4924 is a "listener", any EOI signal it receives will appear at the Transfer Bus Transceiver's DI port and be sent from there to PIAGPB's PB7 input.

READ/WRITE BOARD: MOTOR CIRCUITRY

The Motor Circuitry is one of the three major blocks on the Read/Write board (Fig. 5-1). Obeying commands from the Control board's Magnetic Tape Controller, it controls the motor, regulating the motor speed by feedback from the tachometer. It is subdivided into these blocks: Stop Tape Control, Step Generator, Ramp Generator, Motor Speed Control, and Darlington Drivers.

The motor speed is determined by a "ramp voltage" which is the output of the Ramp Generator. This voltage is positive if the motor is to run forward, negative if it is to run backward, and zero if the motor is to be stopped. The Motor Speed Control compares the ramp voltage with the feedback voltage from the tachometer, and provides current (amplified by the Darlington Drivers) to cause the motor to speed up or slow down until the two voltages agree.

The Ramp Generator, in turn, is controlled by the Step Generator, which determines whether the ramp voltage is to become more positive (ramp up) or negative (ramp down), or remain the same. The Step Generator provides a positive voltage if the Ramp Generator is to ramp up, negative if it is to ramp down, and zero if it is to remain the same (which would keep the motor speed constant). To determine whether the Ramp Generator should ramp up or ramp down, the Step Generator compares what the ramp voltage **ought to be** (as determined by its input logic) with what it **is** (as determined by feedback from the Ramp Generator's output).

Stop Tape Control

The Stop Tape Control (Schematic 2-1, Fig. 5-5) provides a hardware stop of the motor to prevent the tape running off its spools.

Logic Tree 1 (Fig. 5-6) sets the Stop Flip-Flop whenever (a) the tape is running forward and an EOT marker is sensed, or (b) the tape is running backward and a BOT is sensed. That flip-flop sends the STOP signal to the Step Generator, causing it to stop the motor.

The BOT/EOT Flip-Flop stores the information of which marker was sensed. When the Control board commands the tape to be driven (DRIVE TAPE active) in the correct direction (forward if

BOT was sensed, reverse for EOT), Logic Tree 2 clocks the STOP Flip-Flop, removing the STOP signal. The Stop Tape Control may also be reset by a LOAD pulse.

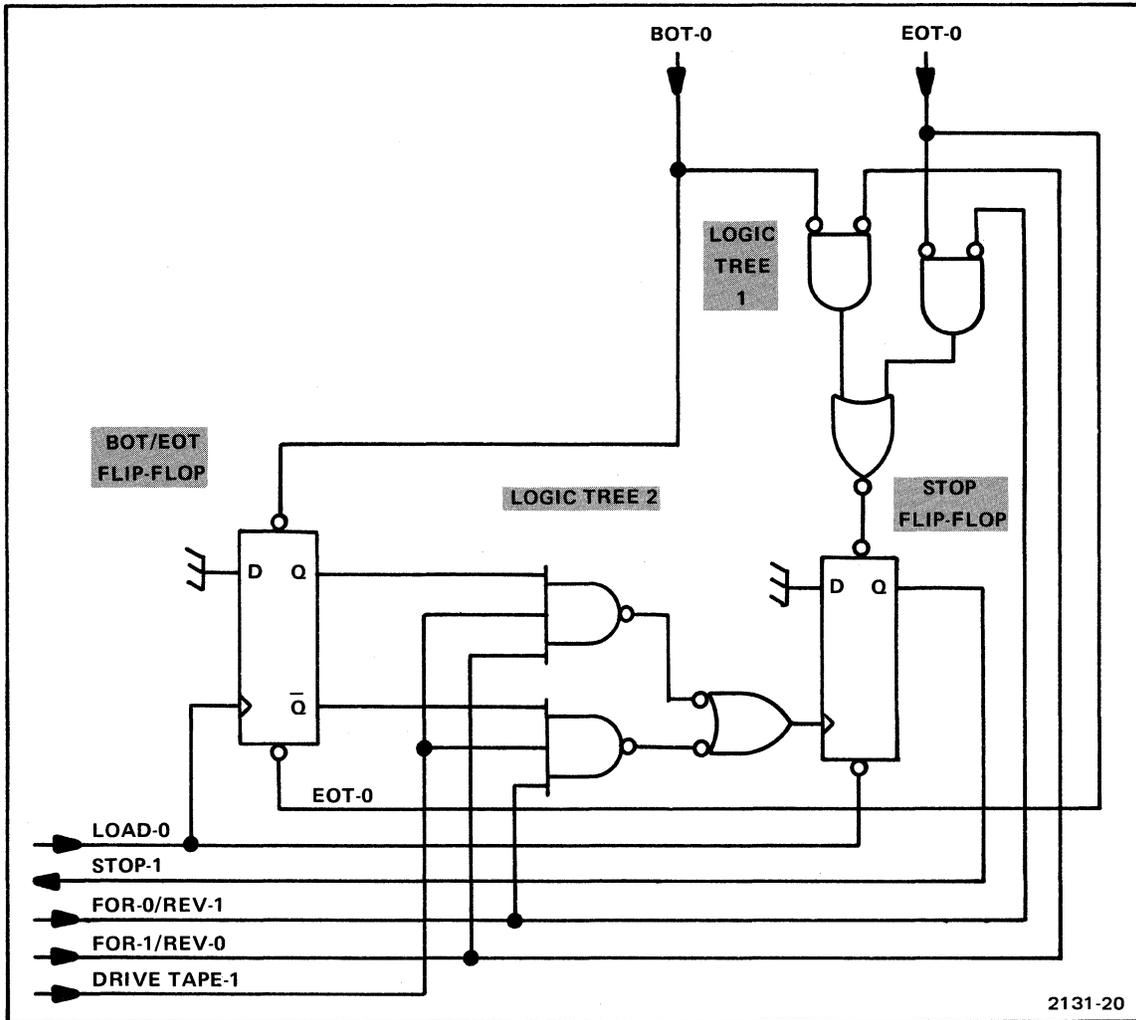


Fig. 5-5. Stop Tape Control.

Step Generator

As mentioned before, the Step Generator (Schematic 2-1) provides a "step" waveform to control the Ramp Generator: a positive voltage to ramp up, a negative voltage to ramp down, and zero if the ramp voltage (and therefore the motor speed) is to remain constant.

The Step Generator does this by means of an op amp functioning as a comparator. The voltage supplied to the inverting input divider network is a measure of whether the motor is to run

forward, or backward, or stop; while the non-inverting input gets a feedback voltage from the Ramp Generator output. If the two do not agree, the comparator provides a positive or negative "step" voltage to cause the Ramp Generator to ramp up or ramp down. (If the voltages agree, the Step Generator provides zero output.)

The divider network at the inverting input of the comparator is connected to +12 V if the motor is to be driven in reverse, -12 V if it is to run forward, and 0 V if it is to be stopped. This is accomplished by a logic network which monitors the DRIVE TAPE, FOR-0/REV-1 and STOP signal lines and keys switching transistors connected to the +12 V and -12 V power supplies.

On the FAST signal, a resistor is switched into the feedback path from the Ramp Generator's output, causing a smaller fraction of the ramp voltage to reach the comparator. Thus, to turn the comparator off, a greater ramp voltage is needed; the ramp voltage (and the motor speed) consequently ramp up to a greater value.

Ramp Generator

The Ramp Generator (Schematic 2-1) provides a "ramp" waveform which is used to determine the direction and speed of the motor's rotation. When the motor is to run forward, the ramp voltage is negative; when it runs in reverse, the ramp voltage is positive; a zero ramp voltage stops the motor.

At the input of the Ramp Generator is a diode bridge functioning as a voltage-operated current switch (Fig. 5-6). When the Step Generator's output is at zero, the current through the two halves of the bridge are equal, and the bridge's output is at ground potential. When the Step Generator's output goes positive, the "A" and "D" diodes are reverse biased; the bridge output receives current through diode "B" from the positive supply, but is isolated from the negative supply. Similarly, when the "step" voltage is negative, the bridge's output receives current from the negative supply, but is isolated from the positive supply. Thus, the output of the diode bridge is at +2 V, 0 V, or -2 V, according to whether the Step Generator's output is positive, zero, or negative.

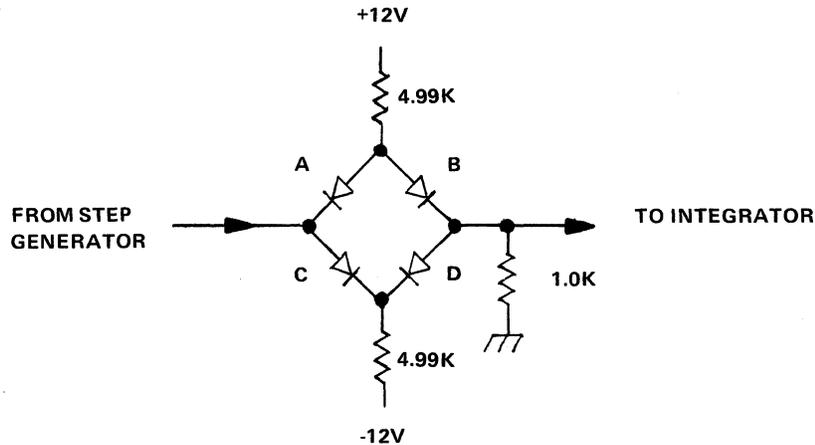
The diode bridge's output is connected to an operational amplifier which functions as an integrator. When its input is negative, its output provides a voltage which is increasing at a constant rate (it "ramps up"). When its input is zero, the output voltage remains constant. When its input is positive, the output voltage "ramps down".

Motor Speed Control and Darlington Drivers

The output of the Ramp Generator (Schematic 2-1) is amplified by an operational amplifier, push-pull transistors and push-pull Darlington driver transistors to provide the current which drives the motor. A voltage from the tachometer is fed back to the input of the operational

Circuit Descriptions

amplifier to regulate the motor speed. Potentiometer R186 in the feedback path provides a way of adjusting the motor speed.



2131-21

Fig. 5-6. Diode Bridge Functioning as a Current Switch.

READ/WRITE BOARD: STATUS CIRCUITRY

The Status Circuitry is one of the Read/Write board's major functional blocks (Fig. 5-5). This circuitry monitors outputs from the Status board and voltages from the Motor Circuitry's Ramp Generator, providing signals to the Control board's Magnetic Tape Controller. These signals indicate whether the tape cartridge is in position, whether it is write-protected, whether the tape is in motion, and if in motion, whether it is up to speed. They also notify the Control board when the tape position markers BOT, EOT and Load Point are detected. Some of these latter signals are also fed to the Motor Circuitry's Stop Tape Control to provide a hardware stop of the motor if the tape should be about to run off its spools or if it has been commanded to perform the Rewind function.

The Status Circuitry includes a Tape Hole Monitor, a Ramp Monitor, and a Write-Protect circuit.

Tape Hole Monitor

The Tape Hole Monitor (Schematic 2-1) uses the hole sensing phototransistors' outputs (UPPER and LOWER) to detect the Beginning of Tape (BOT), End of Tape (EOT) and Load Point tape position markers.

NOTE

The BOT and EOT signals are not used to cause MPU interrupts to prevent the tape from running off its spools. Nor are they monitored by the MPU during rewind operations to see when the tape is fully rewound. Instead, the tape is kept from running off its spools by the Stop Tape Control (in the Motor Circuitry). During rewind, the MPU monitors the TNIM (Tape Not In Motion) signal to see when the Stop Tape Control has halted the tape; it is by TNIM (not by BOT) that the MPU learns that the tape has been fully rewound.

The UPPER and LOWER signals from the Status board are buffered and fed through a NOR gate to a one-shot. The one-shot is disabled from firing until the low from the NOR gate "cocks" it. (When the NOR gate's output goes high once again, the one-shot will fire.) The signals are also fed to two flip-flops, one of which is set whenever a LOWER pulse appears, and the other only when both UPPER and LOWER pulses are present. The outputs of these flip-flops, and of the one-shot, are fed to three NAND gates, which detect the BOT, EOT, and LD POINT conditions. When the tape's motion has carried the tape position marking holes past the phototransistors so that neither UPPER nor LOWER pulse is present, the one-shot fires; it outputs a pulse of about 82 μ s, which enables the NAND gates. When the one-shot times out, the flip-flops are reset; they may also be reset by the LOAD pulse from the Magnetic Tape Controller, which occurs on power-up or when the tape cartridge is removed.

Ramp Monitor

The Ramp Monitor (Schematic 2-1) includes two op amps, connected as window comparators, which monitor the input and the output of the ramp generator. Each window comparator gives a positive output only when its input is very nearly zero volts; for non-zero input voltages, the comparators give negative outputs.

When both the Ramp Generator's input and its output are zero, this indicates that the tape is stopped; this condition is detected by a NAND gate and used to generate the TNIM (Tape Not In Motion) signal.

When the Ramp generator's output is non-zero (motor supposed to be running) and the input is zero (no need to continue ramping up or down), the tape is up to speed. Another gate monitors the window comparator outputs and senses this condition, triggering a one-shot. If the condition is still present when the one-shot times out, the TUTS (Tape Up To Speed) signal is sent.

Write Protect

The Write-Protect circuit (Schematic 2-2) simply buffers the output of the Status board's Safe Switch, and feeds the buffered output to the Control board's Magnetic Tape Controller.

READ/WRITE BOARD: HEAD CIRCUITRY

The Head Circuitry (Fig. 5-5), performs the actual reading and writing of data on the tape. It also monitors the Status board's Safe Switch, disabling itself if the cartridge is write-protected. The Head Circuitry is divided into these blocks (Schematic 2-2) : Write Logic, Head Control, Read Amplifiers, Peak Detectors, and the Read Data and Read Clock Generator.

Write Logic

The Write Logic consists of input gating and a pair of JK flip-flops which determine the direction of the flux to be written on the "ones" and "zeroes" tracks of the tape. The WRITE DATA signal is fed to the J and K inputs of the "ones" flip-flop, and its inverse to the inputs of the "zeroes" flip-flop. Thus, when WRITE DATA is "1" and a WRITE CLOCK pulse clocks the flip-flops, the "ones" flip-flop toggles but the "zeroes" flip-flop does not. If WRITE DATA=0, a WRITE CLOCK pulse toggles the "zeroes" flip-flop but not the "ones" flip-flop.

When the READ/WRITE line says "READ", or the DRIVE TAPE command is inactive, both flip-flops are reset.

Head Control

During "write" operations the Head Control circuits (Schematic 2-2) steer current through the windings of the read/write head to write flux of the appropriate polarity on the two tracks of the tape. Open-collector NAND gates, enabled by the outputs of the "ones" and "zeroes" flip-flops of the Write Logic and the WRITE signal, provide ground returns for the currents flowing through the head windings. The "B+" for these write currents comes through the Status board's Safe Switch and a switching transistor which is turned on by the WRITE command. If the Safe Switch is open (cartridge write-protected) or the WRITE command absent, switching diodes in the path of the write current will be reverse-biased, preventing current from flowing through the read/write head's windings to write flux on the tape.

Read Amplifiers and Peak Detectors

The Read Amplifiers and the Peak Detectors (Schematic 2-2) are used in "read" operations to amplify signals from the heads and prepare them for the Read Data and Read Clock Generator.

During a "read" operation, as the tape moves past the read/write head, any flux reversals on the tracks induce voltage pulses at the terminals of the head windings. These pulses are amplified by one pair of operational amplifiers, and then rectified by another pair connected as precision rectifiers. The resulting positive pulses are then applied to the Peak Detectors.

The Peak Detectors are differential amplifiers configured with positive and negative feedback

loops. A capacitor on the inverting input of each Peak Detector charges toward the peak voltage. After the input has reached its peak value and begins to drop, a switching action takes place. This is caused by the relative drop of the non-inverting input compared to the reference voltage on the capacitor. The result is that a low-active pulse is output within 4 to 6 μs of the input peak. This pulse drives a one-shot in the Read Data and Read Clock Generator.

Read Data and Read Clock Generator

During "read" operations, the Read Data and Read Clock Generator (Schematic 2-2) takes negative pulses from the Peak Detectors and uses them to generate the READ CLOCK and READ DATA signals for the Control Board's Magnetic Tape Controller.

Whenever a flux reversal occurs on the "ones" track, the "ones" Peak Detector sends a negative pulse to the "ones" one-shot, causing it to fire for about 700 ns. Similarly, a flux reversal on the "zeroes" track causes the "zeroes" one-shot to fire. If either one-shot fires, a gate detects this and sends a 700 ns READ CLOCK pulse.

When the "ones" one-shot fires, it sets a flip-flop comprised of two gates; firing the "zeroes" one-shot resets this flip-flop. The output of the flip-flop drives the READ DATA line. It is the falling edge of the READ CLOCK pulse which is used to clock circuitry in the Magnetic Tape Controller; the READ DATA signal will have settled by the time this falling edge occurs.

A WRITE command from the Magnetic Tape Controller clears both one-shots; this disables the Read Clock and Read Data Generator so that no READ CLOCK pulses may occur during "write" operations.

SMALLER BOARDS

Switch and LED Board

The Switch and LED Board (Schematic 3-1) holds the front-panel pushbuttons and the LED indicators. It also holds five set-reset flip-flops, which are used when the 4924 is in Manual mode (red ON LINE switch released).

When the 4924 is in Manual mode, depressing one of the five momentary-contact pushbuttons grounds an input to the corresponding flip-flop, setting it. The output of this flip-flop is buffered and used to drive the corresponding LED indicator and send the corresponding command (REWIND, TALK, LISTEN, SKIP FORWARD, SKIP REVERSE) to the Control Board.

A three-input gate is used to clear all five flip-flops whenever (a) a PROG RESET pulse from the Control board indicates that a command has just been carried out, or (b) a parity tree comprised of four EOR gates detects that more than one flip-flop has been set, or (c) the red ON LINE switch is depressed. If the three-input gate is not clearing the flip-flops, it sends a VALID signal to the Control board.

Circuit Descriptions

To remove the 4924 from Manual mode, the red ON LINE switch is depressed. In addition to causing the three-input gate to clear the five flip-flops, this sends an ON LINE signal to the Control board.

Status Board

The status board (Schematic 2-2) holds switches and sensors to detect whether the tape cartridge is present, whether it is write-protected, and whether the tape position marker holes are before the mirror in the tape cartridge.

The Load Switch grounds the LOAD SWITCH line except when a cartridge is in position. The Safe Switch senses the cartridge's write-protect window. The switch is open if the cartridge is write-protected. When the switch is closed, +12 V is applied to the Head Control circuit.

An incandescent lamp shines onto the cartridge's mirror; if a tape position marker hole is before the mirror, the light shines through the hole onto a phototransistor, which sends an UPPER or LOWER signal according to whether it was an upper or lower hole on the tape.

POWER SUPPLY BOARD

The Power Supply board (Schematic 4-1) contains circuitry to provide the necessary operating voltages for the 4924. These include +12 V, -12 V, +22 V, -22 V, and +5 V for the logic. In addition, strapping for the selectable line voltage ranges is provided on the Power Supply.

Reference Supply (+12 V)

The Reference Supply provides a regulated +12 volt supply for the 4924 electronics. In addition, the +12 volt supply serves as a reference for both the +5 volt and -12 volt supplies.

U39 is a precision voltage regulator. It receives its supply through CR173, input to pin 12. A reference voltage (+7.1 V) is output from pin 6 and fed back into pin 5, through R37. R37 is chosen to represent the same resistance that is seen at pin 4. R39 provides for adjustment of the +12 V Reference Supply.

Current limiting is provided on pin 2, which causes the base drive for pass element Q1002 to drop when the current exceeds the specified limit. R33 is selected to cause current limiting to occur at about 550 mA.

+5 V Supply

The +5 V supply provides a regulated +5.1 volts for the 4924's TTL logic. The reference supply

is input to op amp U9 through the voltage divider composed of R5 and R7. Q1004 is the Darlington pass element which provides increased current.

CR33 is an SCR which provides a crowbar circuit by turning on when the supply exceeds about 6 volts, effectively shorting the +5 V supply and blowing fuse F72.

–12 V Supply

The –12 Volt supply is referenced to the +12 Volt supply. It is regulated by U53, which outputs –12 volts to the base of Q1006. Q1006 is the pass element to provide increased current for the –12 volt supply.

CONTROL BOARD (For Serial Numbers B041194 and Up)

Memory Select

The Memory Select circuitry (Schematics 1-1 and 1-4) is used to decode the high-order memory address bits A8 to A12, selectively enabling the various memory packages. This circuitry also has a gate and an inverter (Schematic 1-1) which provide an “enable” signal (E) for the external System Test Fixture, deriving this signal from the phase two clock ($\phi 2L-0$) and the VMA signals.

The circuitry uses three address decoders, which enable each other sequentially. The first of these (Schematic 1-1) is enabled by a NOR gate only when either a VMA or BA signal is available from the MPU. Its outputs S2, S3, . . . , S7 select the various Read Only Memories (Schematic 1-4). Its EN output enables the second address decoder.

The second decoder (Schematic 1-4) provides an S1 output to enable the PIAs and an $S\emptyset$ output for enabling the third decoder.

The third decoder selects the Random Access Memories. These RAMs must be enabled only during the “high” of the phase two clock; so the $S\emptyset$ output of the second decoder and the phase two clock $\phi 2L$ are ANDed together to enable this third decoder, which in turn selectively enables the RAMs.

The effect of the Memory Select circuitry is to assign to each memory package or PIA a different block of addresses in the microprocessor’s memory address space. Table 5-2 summarizes these assignments.

In using the table, one should bear in mind that, since the address bits A13 to A15 are ignored by the 4924, there is a “memory wrap-around” effect: addresses which differ only in these high-order bits are considered equivalent by the 4924. Thus “2000”, the next hexadecimal address after “1FFF”, addresses the same memory cell as “0000”; again, “FFFF” is equivalent to “1FFF”.

Table 5-2

**MODIFIED CONTROL BOARD
4924 MEMORY ADDRESS ASSIGNMENTS**

Hexadecimal Address	Device Selected	
0000 – 03FF	U271, U275	RANDOM ACCESS MEMORIES
0400 – 040B	Unused	
040C – 040F	U621	} PIAs
040C	PIAGPA Control Register	
040D	PIAGPA Peripheral & Data Direction Registers	
040E	PIAGPB Control Register	
040F	PIAGPB Peripheral & Data Direction Registers	
0410 – 0413	Unused	
0414 – 0417	U641	
0414	PIAMTR Control Register	
0415	PIAMTR Peripheral & Data Direction Registers	
0416	PIAMTW Control Register	
0417	PIAMTW Peripheral & Data Direction Registers	
0418 – 041B	U651	
0418	PIAMTA Control Register	
0419	PIAMTA Peripheral & Data Direction Registers	
041A	PIAMTB Control Register	
041B	PIAMTB Peripheral & Data Direction Registers	
041C – 0427	Unused	
0428 – 042B	U631	
0428	PIAKYB Control Register	
0429	PIAKYB Peripheral & Data Direction Registers	
042A	PIAADR Control Register	
042B	PIAADR Peripheral & Data Direction Registers	
042C - 07FF	Unused	
0800 – 0BFF	U451	} 1K READ ONLY MEMORIES
0C00 – 0FFF	U455	
1000 – 13FF	U465	
1400 – 17FF	U475	
1800 – 1BFF	U485	
1C00 – 1FFF	U495	
042C – 0FFF	Unused	} 2K READ ONLY MEMORIES
1000 – 17FF	U451	
1800 – 1FFF	U455	
2000 – 27FF	U465	
2800 – 2FFF	U475	
3000 – 37FF	U485	
3800 – 3FFF	U495	

Memories

The memory packages (RAMs and ROMs) appear in schematic 1-4. The RAMs are each organized into 1K words of 4 bits each, but the MPU expects each memory location to hold eight bits. So, pairs of RAMs are selected together. One RAM contains the four low-order bits of a memory location; the other, the four high-order bits.

U495 is the ROM addressed by the highest addresses in the 4924's memory address space (hexadecimal 1C00 to 1FFF for 1K and 3800 to 3FFF for 2K). Its enabling may be overridden by a high provided to test connector J304's A2 pin from the external System Test Fixture.

PIAs

The Peripheral Interface Adapters in the GPIB Interface (Schematic 1-2) and the Magnetic Tape Controller (Schematic 1-3) contain registers which are addressed by the MPU in the same way as other memory locations. These devices differ from the other memories, however, by providing a way to interface the MPU with the rest of the machine and with the outside world.

Each PIA is selected when two of its "chip select" pins (CS0, CS1) are high and one (CS2) is low. The two "register select" pins are connected to the low-order address lines A0 and A1, so that the PIA occupies four adjacent locations in the MPU's memory address space. The two lower addresses, for which RS1 is "0", refer to the "A" half of the PIA, and the two higher addresses, for which RS1 is "1", to the "B" half.

Each half of the PIA has three registers. These are the Control, Peripheral, and Data Direction registers. The Control Register is addressed at an even-numbered address (for instance, 0414). The Peripheral and Data Direction registers share the same odd-numbered address (0415). A bit set by the MPU in the Control Register (in our example, address 0414) determines which of these two registers is accessed by the MPU when it addresses the odd-numbered address (0415) for that half of the PIA.

The Peripheral Registers are the PIA registers used most in the 4924's operation, as they provide the interface for the MPU to the world beyond its memories. Each half of the PIA has eight pins (PA0 to PA7 or PB0 to PB7) through which its Peripheral Register receives data from, or sends data to, external devices. Each bit of a Peripheral Register is programmed to receive or transmit data according to the state of the corresponding bit in that register's Data Direction Register. For instance, a "0" in the low-order bit of Data Direction Register A causes the low-order bit of Peripheral Register A to receive data from the PA0 pin. Similarly, a "1" in the low-order bit of Data Direction Register A would program the low-order bit of Peripheral Register A to transmit data to the PA0 pin.

Circuit Descriptions

For instance, in PIA U641 (Schematic 1-3), all the bits of Peripheral Register A act as inputs; so Data Direction Register A must have all zeroes programmed into it. Peripheral Register B is used to send data out; so all the bits of Data Direction Register B must be ones.

Each half of the PIA also has two pins (CA1 and CA2, or CB1 and CB2) by which its Control Register can interact with the outside world. When these are used as inputs, the Control Register can be programmed to generate an interrupt request when the voltage at these inputs changes. This it does by pulling the IRQA or IRQB pin low. These pins are connected to the MPU's IRQ or NMI control lines, so that a low generates an interrupt request.

MAGNETIC TAPE CONTROLLER

The Magnetic Tape Controller on the Control Board includes these functional blocks (Schematic 1-3): PIAs, Write Shift Register, Read/Write Shift Register, Write Control, Read/Write Shift Register Input Gating, Clock Gating, Write Output Gating, Timer, Cartridge Removal Circuit, Debouncers, and Tape Monitor.

PIAs

PIAMTR and PIAMTW are the "A" and "B" halves of a single Peripheral Interface Adapter package. PIAMTR's Peripheral Register is used during read operations to receive into the MPU's memory the data being read from the tape. PIAMTW's Peripheral Register is used in write operations to send out from the MPU the data to be written on the tape. The control ports CA1, CB1, and CB2 are used to interrupt the MPU during certain operations, while control port CA2 is used as an output, to control the Timer.

PIAMTA and PIAMTB are the "A" and "B" halves of another PIA. Their Peripheral Registers perform a variety of input and output functions, carrying data to the MPU and commands from it. All four of their control ports are used as inputs, generating MPU interrupts upon detection of record marks or inter-file gaps.

Write Shift Register

During "write" operations, the Write Shift Register (Schematic 1-3) converts data from parallel to serial format. Each data byte from PIAMTW is loaded into it in parallel, then shifted out serially and passed through the Write Output Gating to become the WRITE DATA signal. This signal is sent to the Read/Write board's Head Circuitry to be written on the tape.

Read/Write Shift Register

The Read/Write Shift Register performs two functions. During a read operation, it is a serial-to-parallel converter. It accepts the serial READ DATA signal (after it has passed through the Read/Write Shift Register Input Gating) and converts each serial byte to eight parallel bits to be read by PIAMTR.

During a write operation, the Read/Write Shift Register becomes part of a mechanism which produces a waveform used to control the write operation. For this, refer to the description of the Write Control circuitry.

Write Control

The Write Control is used, together with the Read/Write Shift Register, to generate a waveform used to control several of the Magnetic Tape Controller's blocks during a write operation. This waveform is low except when the 4924 is writing data bytes onto the tape; then it is high for eight MAGCLK pulses, low for the next two pulses, high for eight, low for two, etc.

Refer to Fig. 5-7, which shows an extract from Schematic 1-3 and pertinent waveforms.

Shortly before a series of data bytes is written on the tape, READ-0/WRITE-1 is high and GNFR (Generate NFRs) and WENABLE (Write Enable) are low. FF2's Q is high, the R/W Shift Register's Q_H is high, and FF1 is cleared. FF1's Q output, which makes the control waveform, is low. With FF1-Q low, the Clock Gating prevents MAGCLK pulses from reaching the Write Shift Register or the WRITECLOCK output.

To start the writing of a series of data bytes on the tape, the MPU sends high the WENABLE input to Gate 2. With FF1- \bar{Q} high, Gate 2 presents a "1" to FF2-D.

At the first MAGCLK pulse, FF2- \bar{Q} goes low, clearing the R/W Shift Register, which in turn enables FF1. Gates 1 and 2 then present a "0" at FF2-D, and a "1" at FF1-D.

At the second MAGCLK pulse, FF2- \bar{Q} goes high again, enabling the Read/Write Shift Register (which, having been cleared, has "0's" in all its stages). FF1-Q goes high, and FF1- \bar{Q} low, causing Gate 1 to send a "1" to FF1-D and "0" to FF2-D, latching high FF1- \bar{Q} and FF2-Q on successive clocks.

Now that the control waveform from FF1-Q is high, the Clock Gating will pass MAGCLK pulses to the Write Shift Register. These pulses are also passed through the Output Gating to become the WRITECLOCK.

Circuit Descriptions

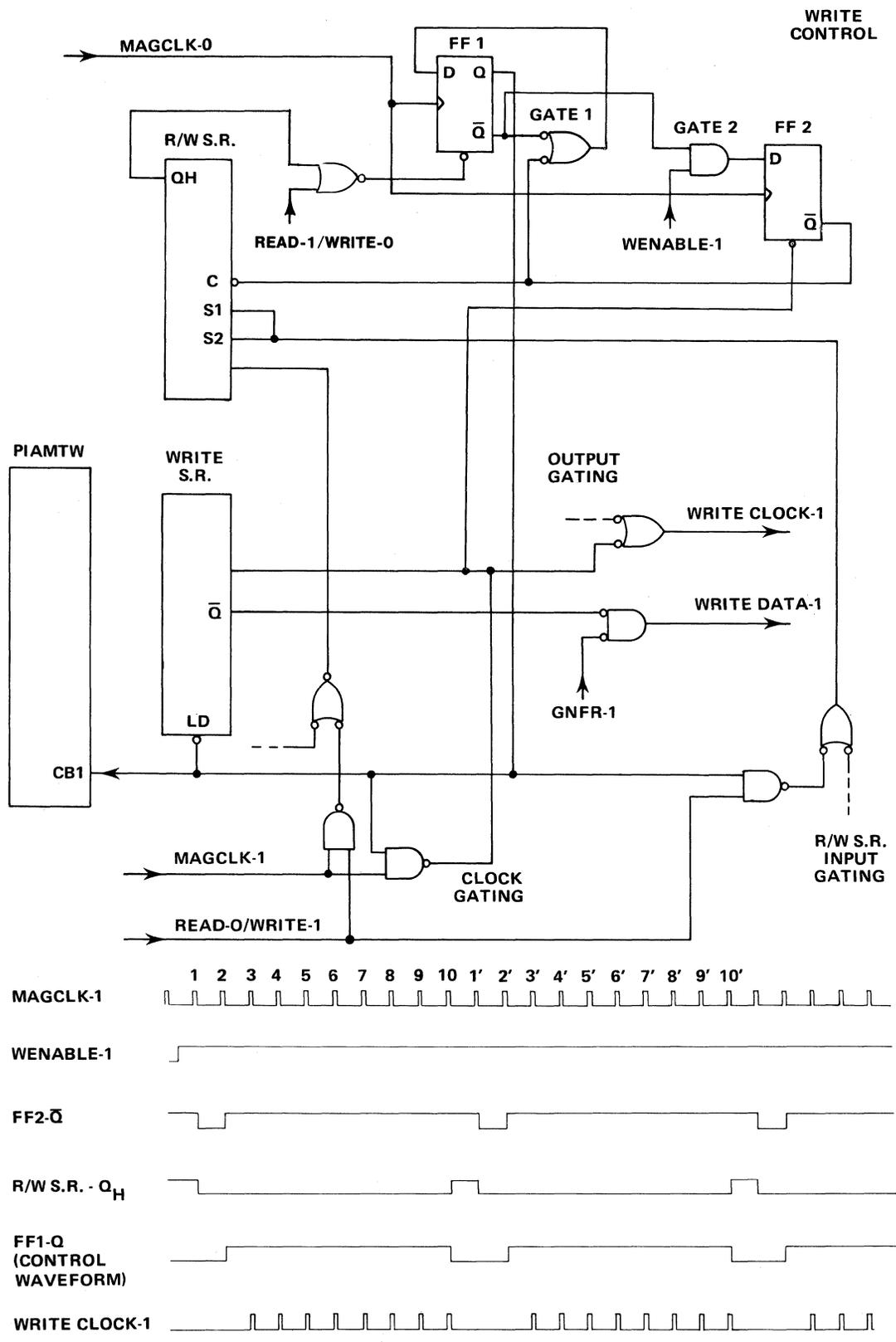


Fig. 5-7. Write Control Circuitry and Waveforms.

For the third, fourth, . . . , and ninth MAGCLK pulses, FF1-Q remains high. With FF1-Q high, the tenth MAGCLK pulse does pass through the Clock Gating. However, this pulse, in clocking the Read/Write Shift Register, produces a “1” at that register’s Q_H output; the “0’s” that were in the shift register have all been shifted out. The “1” at Q_H clears FF1, sending the control waveform low. Gate 2 then presents a “1” to FF2-D.

Things now are just as they were before the first MAGCLK pulse; the next pulse begins a new cycle. On the first two MAGCLK pulses of each cycle, the control waveform from FF1-Q is low, disabling the WRITECLOCK and writing an inter-character gap (ICG) of about 62 μ s. During the remaining eight MAGCLK pulses of the cycle, FF1-Q is high, enabling the WRITECLOCK and causing data to be serially shifted out of the Write Shift Register.

As the write control waveform from FF1-Q goes low at the end of each cycle, it disables the Write Shift Register, putting it in “load” mode. The falling edge of this waveform, fed to PIAMTW’s CB1 port, causes the PIA to interrupt the microprocessor, informing it that the data has been shifted out and that it may load another data byte into the Write Shift Register.

The writing of data on the tape is terminated by the MPU’s sending WENABLE-1 low. The current cycle of the Write Control circuitry is then completed, this allows the Write Shift Register to finish shifting out the last data byte. The Write Control circuitry then resumes its initial state until again enabled by WENABLE signal.

Read/Write Shift Register Input Gating

Since the Read/Write Shift Register (Schematic 1-3) has different functions during the “read” and “write” operations, it must also have different inputs. The Read/Write Input Gating is a logic tree which accomplishes this; during “read”, it feeds the READ DATA signal to the shift register, and during “write” it presents the Write Control waveform to the shift register.

Clock Gating

The Clock Gating circuitry (Schematic 1-3) provides switching of the clock pulses to the two shift registers. During “read”, it steers the READ CLOCK pulses to the Read/Write Shift Register. During “write”, it provides that register with MAGCLK pulses. During “write”, but only during the high of the Write Control’s output waveform, it feeds MAGCLK pulses to the Write Shift Register and (through the Write Output Gating) to the WRITE CLOCK line.

Write Output Gating

The Write Output Gating circuitry (Schematic 1-3) sends the WRITE CLOCK and WRITE DATA signals on to the Read/Write board during “write” operations.

The inverting-input AND gate in this circuitry passes serial data bytes from the Write Shift Register to the WRITE DATA output. When the periods of no flux reversal (NFRs) which comprise record marks and file marks are being written, the GNFR output from PIAMTB is high, and this gate holds the WRITE DATA line low. Thus, the flux reversals separating the NFRs in record and file marks are all written on the zeroes track of the tape.

The other two gates drive the WRITE CLOCK line, producing WRITE CLOCK pulses when either (a) the Write Shift Register is being clocked, sending a data byte out on the WRITE DATA line, or (b) a record mark or file mark is being written (GNFR is high) and the CA2 port of PIAMTR outputs a pulse. The NAND gate in this circuitry isolates the CA2 port's output from the WRITE CLOCK line except when record or file marks are being written; this permits the MPU to use the Timer at other times than during the writing of record and file marks.

Timer

The Timer (Schematic 1-3) is a one-shot multivibrator which provides the MPU with a hardware timing mechanism independent of the Clock.

PIAMTR's CA2 output is normally high. To start a timing cycle, a read of PIAMTR causes a momentary low pulse from the CA2 port. This pulse, after inversion, triggers the one-shot, which sends its output high for about 40 μ s. This high is applied to PIAMTA's PA0 input.

Meanwhile, after possibly performing some other tasks, the MPU enters a loop in its program, continually checking the contents of PIAMTA's Peripheral Register. When the one-shot times out, PIAMTA's PA0 pin goes low; in reading the Peripheral Register, the MPU detects this low, thus learning that the timing cycle has been completed.

Cartridge Removal Circuit

The Cartridge Removal Circuit (Schematic 1-3) includes three gates, two of which comprise a set-reset flip-flop. When the tape cartridge is removed from its slot, a switch on the Status board grounds the LOAD SWITCH line, setting the flip-flop, which sends the NOCART line high. This high is presented to PIAKYB's PA6 input (Schematic 1-2) to inform the MPU of the cartridge's removal. The flip-flop is reset when the MPU causes PIAMTA's PA1 output (Schematic 1-3) to toggle.

The other gate in the Cartridge Removal Circuit drives the LOAD Line, sending it high on a RESET pulse or when the cartridge is removed. The LOAD signal initializes the Stop Tape Control and Tape Hole Monitor logic on the Read/Write board.

Debounce

The Debouncers (Schematic 1-2) are two-sixths of an MC14490 contact bounce eliminator, the other four-sixths of which are used in the GPIB Interface (Schematic 1-2). These debouncers clean up the BOT and EOT signals from the Read/Write board, delaying them about 20 μ s, and present the clean, delayed signals to PIAMTB's CB1 and CB2 ports, where they are used to set flags in the control register of the PIA indicating detection of the BOT or EOT tape position markers.

NOTE

The BOT and EOT signals are not used to cause MPU interrupts to prevent the tape from running off its spools. Nor are they monitored by the MPU during rewind operations to see when the tape is fully rewound. Instead, the tape is kept from running off its spools by the Stop Tape Control (in the Motor Circuitry). During rewind, the MPU monitors the TNIM (Tape Not In Motion) signal to see when the Stop Tape Control has halted the tape; it is by TNIM (not by BOT) that the MPU learns that the tape has been fully rewound.

Tape Monitor

During read operations, the Tape Monitor (Schematic 1-3) watches the READCLOCK pulses, using them to detect the end of each serial byte as well as record marks and file marks. When the tape skips fast forward or fast reverse, it detects the long blank spaces between files. On detection of the end of a serial byte, or of a record mark, file mark, or inter-file gap, it signals to a PIA control port, causing the PIA to generate an MPU interrupt.

The Tape Monitor is comprised of an NFR Detector, a Record and File Mark Detector, a Bit Counter, and a File Finder.

NFR Detector.. The NFR Detector, a one-shot multivibrator, detects the NFRs (periods of no flux reversal) which comprise record marks and file marks.

Circuit Descriptions

With the tape running at its normal speed and the FNFR (Find NFRs) line high, the first READCLOCK pulse of each data byte triggers the one-shot, and succeeding pulses within the byte re-trigger it, keeping its output high for the duration of the byte. At the end of the byte, however, an inter-character gap (ICG) of about $60 \mu\text{s}$ elapses with no READCLOCK pulses; the one-shot times out, and the negative transition at its Q output signals the detection of an NFR. Similarly, after each of the clock pulses separating the NFRs within record or file marks, the NFR detector times out, signalling detection of an NFR.

Record and File Mark Detector. The Record and File Mark Detector is a counter clocked by the negative transitions from the NFR detector's output which signal the detection of NFRs. A record mark consists of four NFRs; so at the count of four, the counter's Q_C output drives the RMARK line high, signalling detection of a record mark. Similarly, at the count of eight, Q_D signals detection of a file mark on the FMARK line.

The Record and File Mark Detector may be reset by a pulse from the Bit Counter, or by sending FNFR low.

Bit Counter. Since the NFR Detector remains triggered for the duration of each data byte, its \bar{Q} output is low. This enables the Bit Counter, which counts the READCLOCK pulses within each byte. At the count of four, its Q_C output resets the Record and File Mark Detector; this prevents that circuit from counting the inter-character gaps and giving erroneous record mark or file mark indications. At the count of eight, its Q_D output sends the READIT line high; this signals to the MPU that all eight bits of the character have been clocked into the Read Shift Register, and that it may now read into PIAMTR the parallel data byte presented at that shift register's output.

Whenever the NFR Detector times out, its Q output resets the Bit Counter.

File Finder. When the tape is skipping fast forward or fast reverse, the MPU must know when inter-file gaps occur. The File Finder is a one-shot used to detect these.

With the tape running at the faster speed, the inter-character gaps and the NFRs within record and file marks are too brief for the NFR Detector to time out; thus the Bit Counter is not reset, but keeps running. Its Q_D output is used to trigger and re-trigger the File Finder one-shot, which has a 31.5 ms period. At the faster tape speed, re-triggering occurs frequently enough to keep the File Finder's \bar{Q} output low, except during the long inter-file gaps. When these occur, the one-shot times out, sending the FILEFND line high and causing PIAMTA to generate an MPU interrupt.

The MPU may disable the File Finder by causing PIAMTB to set its PB7 output low.

GPIB INTERFACE

The GPIB Interface on the Control board (Schematic 1-2) interfaces between the General Purpose Interface Bus and the 4924's microprocessor. Its PIA package U321 (PIADDR and PIAKYB) also interfaces between the MPU and the switches on the front panel (Switch and LED Board) and the rear panel (Mode/Address board).

The GPIB Interface includes PIA's, Transfer Bus and Management Bus Transceivers, a Transfer Bus Transceiver Steering circuit, a Data Bus Interface, Listen/Talk Steering circuitry, Debouncers, a "Hello" circuit, Hand Gating, Source Handshake circuitry (SH), Acceptor Handshake circuitry (AH₁ and AH₂), and AH Enable circuitry. Refer to Schematic 1-2 to locate these circuit blocks.

Before reading the GPIB Interface circuit descriptions, be sure to read Section 4, which describes the GPIB's functions.

PIAs

PIAs PIAGPA and PIAGPB do most of the interfacing between the MPU and the GPIB Interface circuitry. PIAGPA's peripheral register transmits data between the MPU and the GPIB data bus, while PIAGPB's peripheral register transmits a variety of signals between the MPU and the GPIB Interface circuitry. The control ports CA1, CA2, CB1, CB2 of PIAGPA and PIAGPB are used to generate MPU interrupts.

PIADDR's CB2 port relays the SHAKE signal from the MPU to the GPIB circuitry, while the rest of PIADDR and PIAKYB are really independent of the GPIB interfacing function; they interface between the MPU and the rear panel switches on the Mode/Address board and between the MPU and the front panel switches on the Switch and LED board. PIADDR's CB1 port is functionally part of the Magnetic Tape Controller, as it carries the LD POINT interrupt signal from the Read/Write board to the MPU.

Transfer Bus Transceiver

The Transfer Bus Transceiver (Schematic 1-2) provides interfacing to the three GPIB transfer bus lines DAV, NRFD and NDAC, and to one of the management bus lines, EOI. Its internal schematic is illustrated in Fig. 5-8. Each input or receive port (such as AI) at all times follows the signal presented to the corresponding GPIB port (A). An output or transmit port (such as AO) drives the GPIB line connected to its GPIB port with its open-collector driver only if the transceiver is enabled with a low at its enable input. The GPIB ports are active-low to conform with the GPIB standard, while the receive ports and transmit ports are active-high.

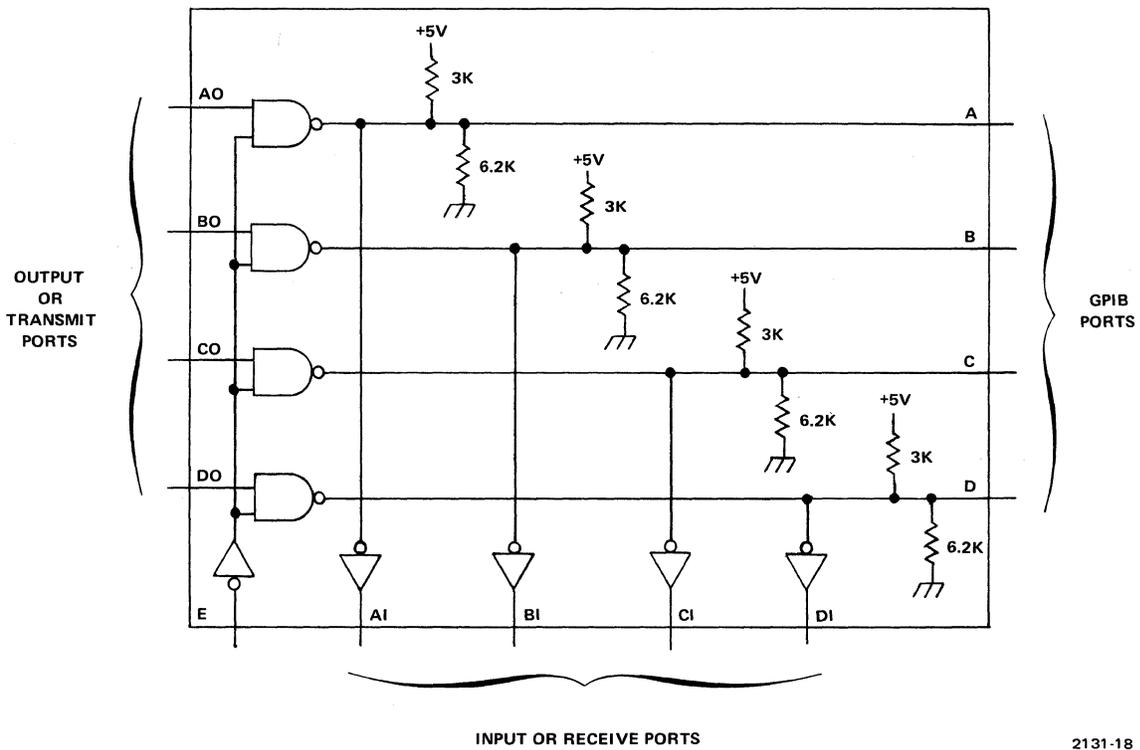


Fig. 5-8. GPIB Transceiver.

Management Bus Transceiver

The Management Bus Transceiver (Schematic 1-2), like the Transfer Bus Transceiver, is a type 3441 GPIB transceiver. Unlike the Transfer Bus Transceiver, it is always enabled to transmit (its enable input is grounded). However, since the 4924 is not permitted to send the ATN, IFC or REN signals over the GPIB, the corresponding transmit ports (CO, BO, AO) are grounded. Any time that a high is presented at its DO port, however, it will transmit the SRQ (Service Request) message on the GPIB.

Transfer Bus Transceiver Steering

The Transfer Bus Transceiver is only enabled to transmit when the 4924 is to receive or send bytes over the GPIB. This occurs when (a) the 4924 has been addressed as a "talker" or "listener", and (b) when the controller is holding ATN active, commanding all GPIB devices to "listen" to the addresses or commands on the GPIB data bus. The Transfer Bus Transceiver Steering gate (Schematic 1-2) detects these two conditions and enables the Transfer Bus Transceiver when either of them occurs.

Data Bus Interface

The Data Bus Interface (Schematic 1-2), as its name implies, is an interface between the 4924 and the GPIB's data bus. It includes two GPIB transceivers similar to the ones used as the Transfer Bus and Management Bus Transceivers. Since the "receive" ports of these transceivers are always active, the Data Bus Interface also includes a pair of "quad tri-state buffers" which effectively isolate the GPIB transceiver "receive" ports during "transmit", but connect them to PIAGPA during "receive".

Listen/Talk Steering

The PB5 output of PIAGPB is sent low by the MPU when bytes are to be transmitted out over the GPIB, and high when bytes are to be received. The Listen/Talk Steering Circuitry (Schematic 1-2) uses this signal and the ATN signal received from the GPIB as inputs, and provides outputs to steer various circuit blocks in the GPIB Interface between their "listen" and "talk" modes:

- (a) When PIAGPB-PB5 says "listen", or ATN is active, the Data Bus Interface's GPIB transceivers are disabled from transmitting. On "talk", with ATN inactive, they are enabled.
- (b) The Data Bus Interface's tri-state buffers are enabled on "listen", and disabled on "talk".
- (c) The SH (Source Handshake) circuitry's output is enabled on "talk", and disabled on "listen".
- (d) The AH Enable and Hand Gating circuits are provided inputs to indicate whether "listen" or "talk" mode is active.

Debounce

The Debouncers (Schematic 1-2) comprise four-sixths of an MC14490 contact bounce eliminator. They "clean up" the ATN, IFC, NDAC and HAND signals, in order to prevent false MPU interrupts due to "ringing" on these lines. They debounce both the rising and the falling edges of the signal. A register "traps" signals — ATN, IFC and HAND — to prevent missing interrupts.

Hello

The Hello circuit (Schematic 1-2) is a gate used by the 4924 to detect, prior to transmitting data over the GPIB, whether there are any "listeners" on the GPIB to receive the data. If a listener is on the line, then it will be pulling either the NRFD (Not Ready For Data) or NDAC (Data Not Accepted) line active. If neither line is in its active state, then no listener is on the line, and the Hello circuit will signal this fact to the MPU by pulling the NOBODY line high.

If nobody is on the line to "listen", the 4924 will not attempt to "talk"; this prevents the 4924 from being "hung up" while waiting for a non-existent listener to respond to its handshake signals. (In the Manual mode, the 4924 will then turn off the command it was issued, extinguishing the LED on the front panel.)

Hand Gating

The Hand Gating circuitry (Schematic 1-2) is used during the three-wire "handshake" procedure by which the GPIB transfer bus regulates the flow of data bytes over the data bus. Its output is passed through a debouncer, becoming the HAND signal which is applied to PIAGPA's CA1 port to generate an MPU interrupt.

When data is to be transmitted, this interrupt informs the MPU that the "listeners" on the GPIB have all released the NRFD line and that the 4924 may now place a byte on the data bus. (When that byte has been placed, the MPU will send the SHAKE signal, causing the SH circuitry to transmit the DAV message.)

When data is to be received, the HAND interrupt informs the MPU that the "talker" on the GPIB has sent the DAV (Data Valid) signal, indicating that a byte has been placed on the GPIB data bus. (When the 4924 has read that byte, the MPU will send the SHAKE signal, causing the AH circuitry to transmit the "data accepted" message.)

The Hand Gating Circuitry, then, is a logic tree which sends the HAND signal when (a) the 4924 is in "listen" mode and the DAV signal is true, or (b) the 4924 is in "talk" mode and the NRFD signal is false.

Source Handshake

The SH (Source Handshake) circuitry (Schematic 1-2) is used to generate "handshake" signals on the GPIB's transfer bus during the transmission of data from the 4924.

The SH circuitry includes a flip-flop which is set when (a) the 4924 is in “listen” mode or, moreover, (b) the DAC (Data Accepted) signal is true. When the “listeners” on the GPIB indicate that they are all ready to accept data (NRFD false), the HAND signal from the Hand Gating circuitry causes the MPU to place a byte on the data bus and send the SHAKE signal. This SHAKE signal clears the flip-flop in the SH circuitry, sending its output high. This sends a “1” through an AND gate to the Transfer Bus Transceiver, which sends the DAV signal on the GPIB.

The AND gate on the output of the flip-flop disables the SH circuitry from transmitting the DAV signal whenever the 4924 is in “listen” mode.

Acceptor Handshake

The Acceptor Handshake circuitry (Schematic 1-2) is used to generate “handshake” signals for the GPIB transfer bus during reception of bytes from the GPIB data bus. It feeds its outputs to the Transfer Bus Transceiver which keys the appropriate GPIB transfer bus lines. It includes the AH₁, AH₂, and AH Enable functions. Refer to Fig. 5-9.

The AH Enable gate within this functional block enables the AH circuitry whenever the 4924 is not in “talk” mode, and also whenever the ATN signal is true. Thus, even while the 4924 has not been addressed, the AH circuitry is enabled. This does not matter, however, as the Transfer Bus Transceiver Steering gate prevents the Transfer Bus Transceiver from transmitting.

The 4924 will be ready to accept data when (a) the AH circuitry is enabled, and (b) the talker has not yet placed a new byte on the GPIB data bus (DAV false). (With DAV false, the set-reset flip-flop in the AH₁ block is set.) Under these circumstances, the logic in the AH₁ block provides a “0” to the Transfer Bus Transceiver’s BO port, signaling to the GPIB that the 4924 is ready to accept data.

When all GPIB “listeners” are ready for data, the GPIB’s NRFD line goes inactive high (NRFD false). The “talker” then places a byte on the data bus, and sends the DAV message.

Immediately on receipt of the DAV message, the logic in the AH₁ block causes the Transfer Bus Transceiver to send the NRFD message, inhibiting the “talker” from placing another byte on the data bus. Also the Hand Gating circuitry and its associated debouncer produce the HAND signal, which generates an MPU interrupt. The interrupt causes the MPU to read the byte available on the data bus, and then to send the SHAKE signal.

Circuit Descriptions

The HAND signal is also fed to the logic in the AH₂ block, which acts as a “NRFD hold” circuit. That is, it prevents the 4924 from sending the “ready for data” signal until the DAV signal has gone away and this information has had time to clock its way through the debouncer to send the HAND signal low. This prevents the 4924 from missing a HAND interrupt when a very fast “talker” is on the line.

Until the MPU has read the data byte, the flip-flop in the AH₁ block will be set, providing a “1” to the Transfer Bus Transceiver’s CO port. This causes a NDAC message to be sent on the GPIB. When, however, the MPU has read the data, it sends the SHAKE signal, which resets this flip-flop and causes the Transfer Bus Transceiver to signal that the 4924 has accepted the data by letting the NDAC line go inactive high.

When all “listeners” on the GPIB have accepted the data, the “talker” can place another byte on the data bus and start the handshake procedure again by sending the DAV message.

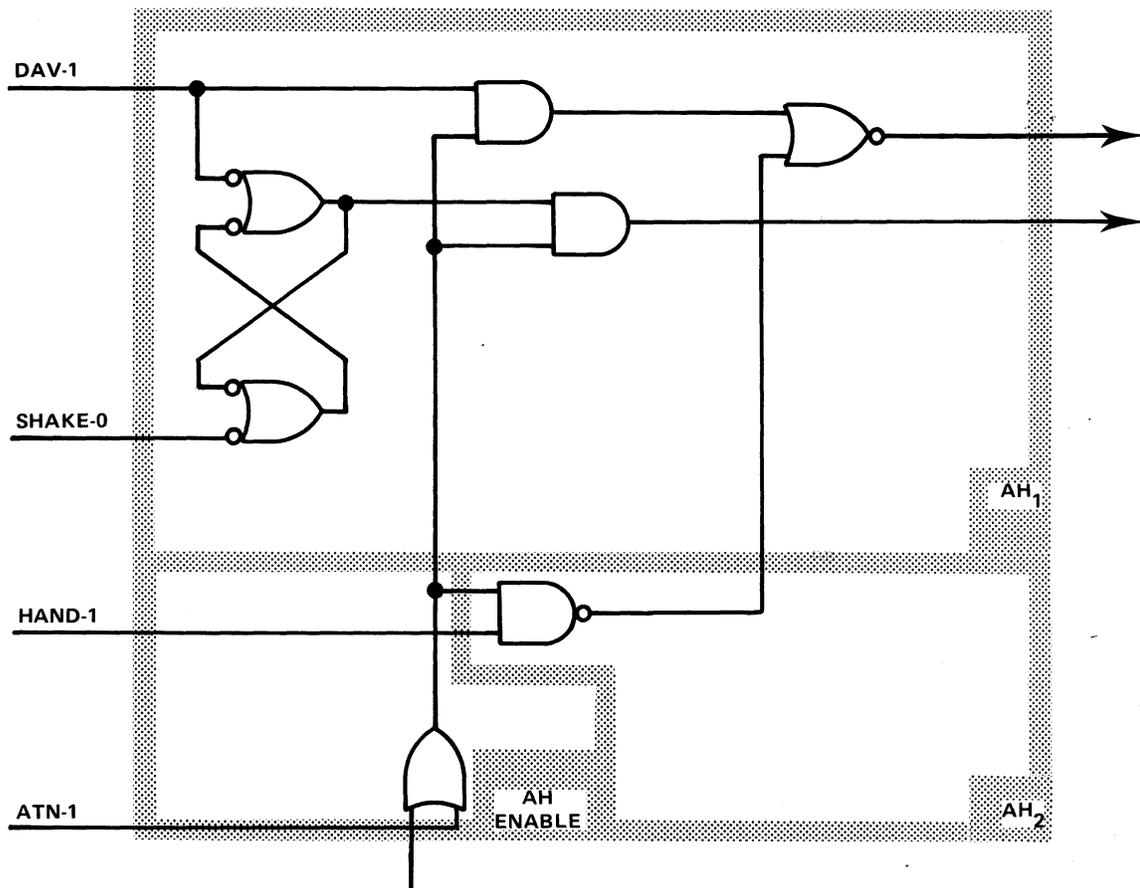


Fig. 5-9. Acceptor Handshake (AH) Block.

Interfacing the ATN Line

The TAN signal may not be sent by the 4924; hence the CO port of the Management Bus Transceiver is tied to ground.

When the ATN signal is received, it is fed from the Management Bus Transceiver's CI port to:

- (a) the Debouncers, which present a debounced version of it (ATNDLY) to PIAGPB, setting flags in PIAGPB's control register to tell if ATN is being asserted or if it is going away, and setting the peripheral register's PB4 bit to show the DC level of ATN;
- (b) the Transfer Bus Setting, which immediately enables the Transfer Bus, so that "acceptor handshake" signals may be transmitted;
- (c) The AH Enable gate, which enables the Acceptor Handshake circuitry; and
- (d) the Receive/Transmit Steering, which immediately disables the Data Bus Interface from transmitting.

When the MPU responds to the interrupt, it will steer the GPIB Interface into "receive" mode (if it is not already in that mode), thus enabling the Data Bus Interface to pass the received byte to PIAGPA.

As long as ATN is held active, the 4924 will be in "receive" mode, receiving universal commands or device addresses from the GPIB controller. If the MPU, in receiving these bytes, recognizes its own talk or listen address, it will cause PIAGPB's PB6 port to send the ADDRESS signal to the Transfer Bus Transceiver Steering gate. (Then, when the ATN line is released, the Transfer Bus Transceiver will still be enabled to transmit.)

When the GPIB controller releases the ATN line, and ATNDLY signals this to the MPU via PIAGPB's IRQ line, the MPU will follow any commands just given it by the controller.

Interfacing Other GPIB Management Bus Lines

The 4924 may send, but not receive, the SRQ message. PIAGPB's PB1 port is used by the MPU to send the SRQ message (which requests service from the GPIB controller). Since the 4924 may not respond to the SRQ message, the DI port of the Management Bus Transceiver is left unconnected. (It is not even shown in Schematic 1-2.)

Circuit Descriptions

The 4924 may not send the IFC (Interface Clear) message, so the Management Bus Transceiver's BO is tied to ground. When an IFC message is received, it is sent from the Management Bus Transceiver's BI port through the Debouncer to PIAGPA's CA2 input, where it causes an MPU interrupt. This interrupt causes the MPU to stop whatever it is doing and await possible commands to be sent from the GPIB controller.

The 4924 may neither receive nor send the REN message; so the Management Bus Transceiver's AO is tied to ground and its AI port left unconnected.

When a series of data bytes is being sent over the GPIB, the EOI (End Or Identify) message may be used by the "talker" to make the last byte in the data string. When acting as a "talker", the 4924 may send this signal from PIAGPB's PB0 port along the TRANSMIT EOI line and through the Transfer Bus Transceiver out onto the GPIB. When the 4924 is a "listener", any EOI signal it receives will appear at the Transfer Bus Transceiver's DI port and be sent from there to PIAGPB's PB7 input.

Section 6

USING THE EXTERNAL SYSTEM TEST FIXTURE

On the Control board of the 4924 is a connector (J304) for use with an external System Test Fixture (Tektronix Part Number 067-0746-00). This test fixture can be used in a variety of ways, including testing the 4924's RAMs and ROMs. This section describes how to perform these tests.

Test equipment needed:

1. A System Test Fixture, Tektronix Part Number 067-0746-00; and
2. A Test Board Buffer Adapter, Tektronix Part Number 067-0811-00.

CONNECTING THE SYSTEM TEST FIXTURE

With the 4924's cover off, and its POWER switch off, connect the Test Board Buffer Adapter to the Control board's J304 connector; then attach the System Test Fixture to the Test Board Buffer Adapter. (Refer to Fig. 6-1). Be sure to orient the connectors correctly; a caret marked on the plug should line up with a similar caret marked on the jack—reversing the connectors can seriously damage the 4924 and the test equipment. (See Fig. 6-2.) In connecting the ribbon cable from the System Test Fixture to the Test Board Buffer Adapter, the caret on the plug attached to the ribbon cable should line up with the end of the connector on the Test Board Buffer Adapter which is labelled (on the component side of the board) with the legend "A1,B1". (See Fig. 6-3.)

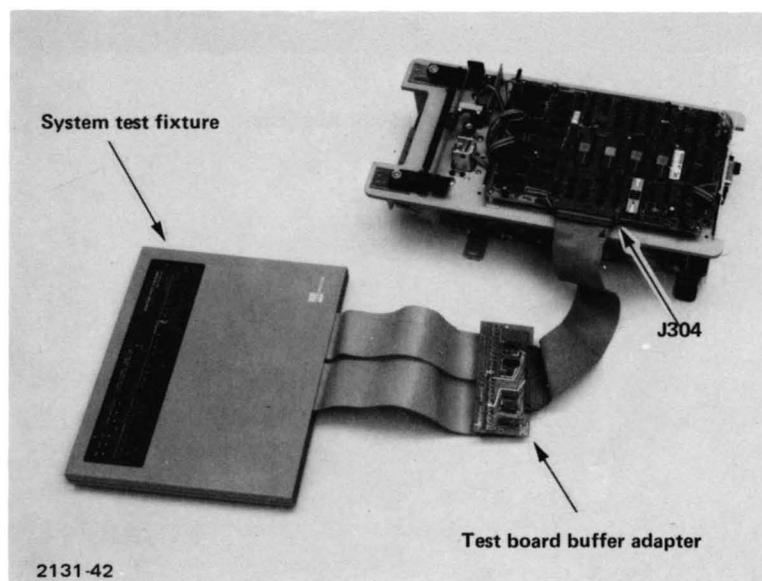


Fig. 6-1. System Test Fixture and Test Board Buffer Adapter.

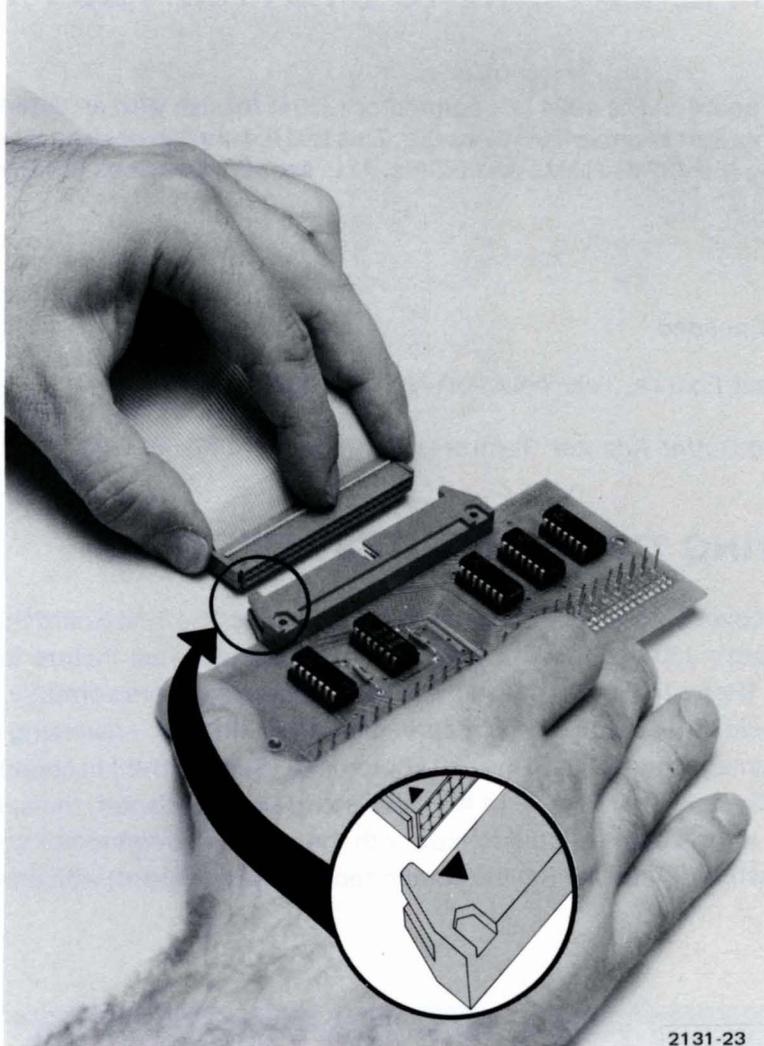
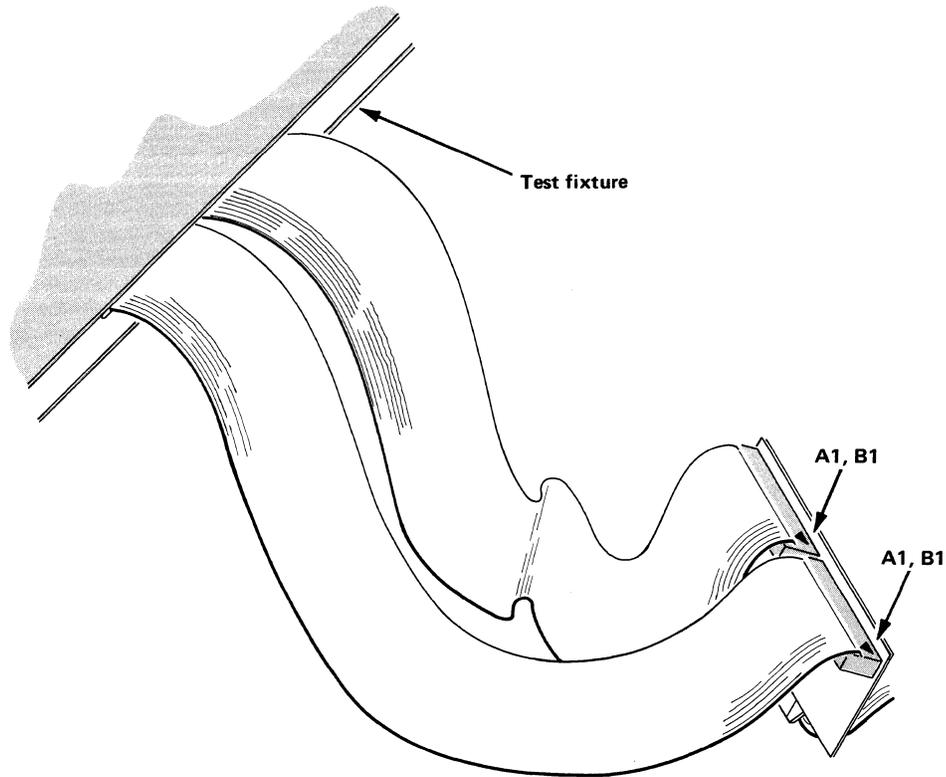


Fig. 6-2. Connector Alignment.



2131-24

Fig. 6-3. Test Board Buffer Adapter Cable Connections.

TESTING THE 4924's RAMs (For Serial Numbers B041193 and Below)

To test the 4924's Random Access Memories, the System Test Fixture should have a 156-0708-10 PROM inserted in its socket U381. The Test Fixture's ADDRESS SELECT jumper should be in its position number "9". The following procedure is then used:

1. If there is a tape cartridge inserted in the 4924, remove it.
2. Refer to the Control board component location diagram (next to Schematic 1-1 in the Schematics section of this manual), and insert a shorting strap at the "test" location indicated in the diagram.
3. Connect the System Test Fixture and the Test Board Buffer Adapter to the 4924, as described above, and turn on power. If the test fixture's ABA (Address Bus Available) LED is on, proceed to the next step. If off, then push STOP, followed by RESTART; this should light the ABA LED.

Using the External System Test Fixture

4. Turn on the System Test Fixture's RAM (internal RAM enable) switch. This switches the test fixture's internal RAM into the highest-address memory locations in the 4924's memory address space. (It also switches U555 on the Control board out of the memory.) On a RESET pulse or an MPU interrupt, the 4924's MPU will go to the System Test Fixture's RAM in order to learn the address of its next instruction.
5. Turn on the System Test Fixture's PROM (internal PROM enable) switch. This causes the System Test Fixture's PROM at its U381 socket to be switched into the 4924's memory at memory locations 9000 to 93FF. This PROM contains the program of instructions for the routine by which the 4924's MPU will test its RAMs.
6. Turn on the test fixture's DATA LATCH, ADDR LATCH, ADDR BRK (address break) and INSTR CYCLE switches; turn off the DATA BRK (data break) switch.
7. Load hexadecimal "90" into memory cell "FFFE". To do this, program hexadecimal "90" (binary "1001", "0000") into the System Test Fixture's DATA switches, and hexadecimal "FFFE" into its ADDRESS switches; then depress the test fixture's DEPOSIT switch. Check that the data has been correctly deposited by pressing the EXAMINE switch; the "data" LEDs should read hexadecimal "90". Similarly, deposit "00" into memory location "FFFF" and examine that memory location to be sure that it was correctly deposited. This loads into the highest-address two memory cells the address of the memory location at which the test program begins.
8. Set the test fixture's ADDRESS switches to "FFFD". (When the MPU has finished the first part of the test routine, it will send "FFFD" out on its address bus. Programming "FFFD" into the ADDRESS switches sets up the "address break" function of the test fixture to interrupt program execution at that point.)
9. Depress the System Test Fixture's RESTART switch, then the START switch. This starts the test routine.
10. The "RAM test" program will run for a short while, making a preliminary test of the RAM packages, starting at memory address "0000". The 4924's RAMS occupy memory addresses from "0000" to "02FF"; so when the program reaches address "0300", it will act as if it had detected a bad RAM: it will stop with "0300" displayed on the "address" LEDs.

Should the program stop with a **smaller** address than "0300" displayed, this would indicate a defective RAM package. The address of the defective RAM will be displayed on the "address" LEDs. Refer to Table 6-1, which gives the memory address for each RAM package, to determine which two RAM packages share the address displayed; one of those two packages is defective.

If the program does not stop until "0300" is displayed, then the RAMs have passed the preliminary test; go on to step 11.

11. Push the System Test Fixture's START switch twice. This restarts the test program. The program will take about two and one-half minutes to check every memory cell in every RAM package. When it is done, it should stop with the "data" LEDs all on (hexadecimal "FF"), the "address" LEDs displaying "FFFC", and the ABA LED lit.

If an error is detected, the program will stop with the ABA LED on. The "address" LEDs will show the address at which the defect was detected, and the "data" LEDs which are lit will indicate which data bits were incorrect at that address. Refer to Table 6-1 to find which RAM package has that address and those data bits; that is the defective RAM.

12. After the test, remove the "test" jumper that was inserted in step two.

Table 6-1
ADDRESSES OF RAM PACKAGES

Memory Addresses	RAM Packages	
	Bits 0-3	Bits 4-7
0000 - 00FF	U551	U253
0100 - 01FF	U453	U251
0200 - 02FF	U451	U151
0300 - 03FF	Unused	

TESTING THE 4924's ROMs

To test the 4924's Read Only Memories, the System Test Fixture should have a 067-0824-00 test PROM inserted in its socket U85. The Test Fixture's ADDRESS SELECT jumper should be in its position number "9".

Before testing the 4924's ROMs, one should first check its RAMs, as the "ROM test" program uses the RAMs. Once the RAMs have been tested, use this procedure to test the ROMs:

1. Remove any tape cartridge which may be present in the 4924.
2. Insert a shorting strap at the "test" location shown on the Control board component location diagram.
3. Connect the System Test Fixture and the Test Board Buffer Adapter, and turn on power. If the test fixture's ABA (Address Bus Available) LED is on, proceed to the next step. If off, push

Using the External System Test Fixture

STOP, followed by RESTART; this should light the ABA LED.

4. Turn on the System Test Fixture's RAM, PROM, DATA LATCH, ADDR LATCH, ADDR BRK and INSTR CYCLE switches; turn off the DATA BREAK switch.
5. Load hexadecimal "98" into memory location "FFFE", and "00" into "FFFF". This loads into the highest-address two memory cells the address ("9800") at which the test program begins.
6. Set the test fixture's ADDRESS switches to "FFFD". (When the MPU has finished the first part of the test program it will send "FFFD" out on its address bus. Setting "FFFD" in the ADDRESS switches sets up the "address break" function of the test fixture to interrupt program execution at that point.)
7. Load "00" into the DATA switches; then depress the RESTART switch, followed by the START switch. This starts a "relocating" routine, which copies the test routine from the System Test Fixture's ROM U85 into the 4924's RAM. The relocating routine will stop with the ABA LED on, the "address" LEDs showing "FFFD" and the "data" LEDs showing "00".
8. Change the ADDRESS switches to "00FD", and turn off the PROM and RAM switches. This switches the test fixture's PROMs and RAM out of the 4924's memory, and switches U555 back into memory.
9. Push START. The program will compute a checksum for one of the 4924's ROMs, and stop with that checksum displayed in the System Test Fixture's "data" LEDs and the address of the ROM in the "address" LEDs. Refer to Table 6-2, and compare this checksum to the checksum given in the table for the particular version of the ROM being tested. If the checksums do not agree, the ROM is defective.
10. To continue the test, push START again and repeat step 9. Each time START is pushed, the program will compute the checksum for another ROM. When it has checked the last ROM, it will start over again with the first ROM in the list.
11. When finished with the test, turn power off and remove the "test" jumper that was inserted in step two.

Table 6-2
ROM CHECKSUMS

Memory Address	ROM Package	Part Number	Checksum
0800	U55	156-0777-00	9B or 8C
0C00	U155	156-0778-00 -01	03 9B
1000	U255	156-0779-00 -01	E5 95
1400	U355	156-0780-00 -01	01 1E
1800	U455	156-0781-00 -01	57 95
1C00	U555	156-0782-00 -01	F9 D2

TESTING THE 4924's HARDWARE

A program in one of the System Test Fixture's PROMs can be used to exercise some of the 4924's mechanical and electrical parts, as an aid in troubleshooting. With this program, the motor can be made to run forward and backward, and a test signal can be recorded on the tape and played back, under control of the pushbuttons on the 4924's front panel.

To use this program, a type 067-0824-00 test PROM must be inserted in socket U85 of the System Test Fixture, and that test fixture's ADDRESS SELECT jumper set to its position number "9". With the PROM in place and the jumper positioned, follow this procedure:

1. If there is a tape cartridge inserted in the 4924, remove it.
2. Refer to the Control board component location diagram (next to Schematic 1-1 in the Schematics section of this manual), and insert a shorting strap at the "test" location shown on the diagram.
3. Connect the System Test Fixture and the Test Board Buffer Adapter, as described above under "Connecting the System Test Fixture", and turn on power. If the test fixture's ABA LED is on, proceed to the next step. If off, push STOP, followed by RESTART; this should light the ABA LED.
4. Turn on the System Test Fixture's RAM, PROM, DATA LATCH, ADDR LATCH, ADDR BRK, and INSTR CYCLE switches; turn off the DATA BRK switch.

Using the External System Test Fixture

5. Load Hexadecimal "98" into memory location "FFFE", and "88" into "FFFF". This loads into the highest address two memory locations the memory address ("9888") at which the test program begins.
6. Depress the red ON LINE switch on the 4924's front panel.
7. Press RESTART, then START. This passes control of the 4924 to the test program.

While the test program is running, each of the 4924's front-panel switches has a different function from its normal one; these functions are described below:

ON LINE. The red ON LINE switch is used to terminate execution of commands given with the other switches. When it is released, and one of the other front-panel switches is pressed, the 4924 will perform the function commanded by that other front-panel switch, until a different switch is pressed. Depressing the ON LINE switch causes the 4924 to cease executing any command given it by another front-panel switch.

When the ON LINE switch is depressed, and another front-panel switch is pressed, the 4924 will perform the function commanded by that other switch, but only so long as that switch is pressed; as soon as the switch is released, the 4924 will cease performing that function.

FORWARD. If the FORWARD switch is pressed while a tape cartridge is in the 4924, the motor will run the tape forward at its normal speed of 30 inches per second. This will continue until the end of the tape, when the Stop Tape Control on the Read/Write board will stop the motor.

To stop the tape, depress the red ON LINE button. With ON LINE depressed, it is possible to move the tape forward, but only so long as FORWARD is held depressed; once FORWARD is released, the tape will stop.

REVERSE. The REVERSE switch functions similarly to the FORWARD switch, except that it moves the tape backward.

REWIND. The REWIND switch, when pressed, causes the tape to move backward at its faster speed of 90 inches per second. When the beginning of the tape is reached, the motor will stop.

TALK. If the TALK switch is pressed while a tape cartridge is in the 4924, the motor will run the tape forward at its normal speed (30 inches per second), and the 4924 will record on the tape a test pattern (the binary byte "10101010", or hexadecimal "AA", repeated again and again.) This will continue until the end of the tape is reached or the red ON LINE button is depressed.

If no cartridge is present when TALK is depressed, the motor will still drive, and the DRIVE TAPE signal (a low at J324-7 on the Read/Write board) and the FORWARD signal (a low at J324-6 on the same board) will still be present.

In any case, when TALK is pressed the WRITE CLOCK and WRITE DATA waveforms can be observed at TP21 and TP545 on the Control board. Put your oscilloscope on TP21 or TP545, taking a synchronizing signal from TP45. (Trigger from TP45 on a low level at negative slope). The waveforms are illustrated in Fig. 6-4.

To stop writing test data, depress the red ON LINE button. With ON LINE depressed, it is possible to write on the tape, but only so long as TALK is held depressed; once TALK is released, the writing of data will stop.

LISTEN. When LISTEN is pressed, if a cartridge is present, the tape will run forward and the 4924 will read from the tape. Normally, one would first record test data on the tape using the TALK switch, and then read it from the tape using the LISTEN switch. With the 4924 reading the test data from the tape, the READ CLOCK and READ DATA lines may be monitored on an oscilloscope; the waveforms should resemble those in Fig. 6-4. (In this case, do not trigger the scope from TP41, but from the READIT line, U15 pin 9.)

When finished using this test program to exercise the 4924, turn power off, disconnect the test fixture, and remove the "test" strap from the 4924 Control board.

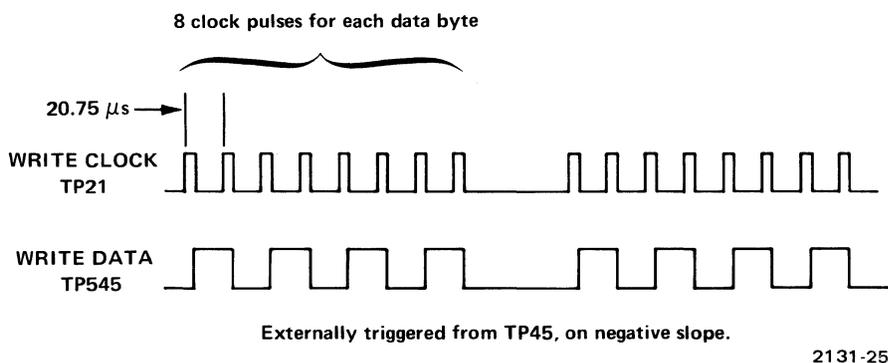


Fig. 6-4. Write waveforms.

TESTING THE 4924'S RAMS (For Serial Numbers B041194 and Up)

To test the 4924's Random Access Memories, the System Test Fixture should have a 156-0708-10 PROM inserted in its socket U381. The Test Fixture's ADDRESS SELECT jumper should be in its position number "9". The following procedure is then used:

1. If there is a tape cartridge inserted in the 4924, remove it.

Using the External System Test Fixture

2. Refer to the Control board component location diagram (next to Schematic 1-1 in the Schematics section of this manual), and insert a shorting strap at the "test" location indicated in the diagram.
3. Connect the System Test Fixture and the Test Board buffer Adapter to the 4924, as described above, and turn on power. If the test fixture's ABA (Address Bus Available) LED is on, proceed to the next step. If off, then push STOP, followed by RESTART; this should light the ABA LED.
4. Turn on the System Test Fixture's RAM (internal RAM enable) switch. This switches the test fixture's internal RAM into the highest-address memory locations in the 4924's memory address space. (It also switches U555 on the Control board out of the memory.) On a RESET pulse or an MPU interrupt, the 4924's MPU will go to the System Test Fixture's RAM in order to learn the address of its next instruction.
5. Turn on the System Test Fixture's PROM (internal PROM enable) switch. This causes the System Test Fixture's PROM at its U381 socket to be switched into the 4924's memory at memory locations 9000 to 93FF. This PROM contains the program of instructions for the routine by which the 4924's MPU will test its RAMs.
6. Turn on the test fixture's DATA LATCH, ADDR LATCH, ADDR BRK (address break) and INSTR CYCLE switches; turn off the DATA BRK (data break) switch.
7. Load hexadecimal "90" into memory cell "FFFF". To do this, program hexadecimal "90" (binary "1001", "0000") into the System Test Fixture's DATA switches, and hexadecimal "FFFE" into its ADDRESS switches; then depress the test fixture's DEPOSIT switch. Check that the data has been correctly deposited by pressing the EXAMINE switch; the "data" LEDs should read hexadecimal "90". Similarly, deposit "00" into memory location "FFFF" and examine that memory location to be sure that it was correctly deposited. This loads into the highest-address two memory cells the address of the memory location at which the test program begins.
8. Set the test fixture's ADDRESS switches to "FFFD". (When the MPU has finished the first part of the test routine, it will send "FFFD" out on its address bus. Programming "FFFD" into the ADDRESS switches sets up the "address break" function of the test fixture to interrupt program execution at that point.)
9. Depress the System Test Fixture's RESTART switch, then the START switch. This starts the test routine.

10. The "RAM test" program will run for a short while, making a preliminary test of the RAM packages, starting at memory address "0000". The 4924's RAMs occupy memory addresses from "0000" to "03FF"; so when the program reaches address "0400", it will act as if it had detected a bad RAM: it will stop with all data LEDs lit and "0400" displayed on the "address" LEDs.

Should the program stop with a **smaller** address than "0400" displayed, this would indicate a defective RAM package. The address of the defective RAM will be displayed on the "address" LEDs. Refer to Table 6-3, which gives the memory address for each RAM package, to determine which two RAM packages share the address displayed; one of those two packages is defective.

If the program does not stop until "0400" is displayed, then the RAMs have passed the preliminary test; go on to step 11.

11. Push the System Test Fixture's START switch twice. This restarts the test program. The program will take about two and one-half minutes to check every memory cell in every RAM package. When it is done, it should stop with the "data" LEDs all on (hexadecimal "FF"), the "address" LEDs displaying "FFFC", and the ABA LED lit.

If an error is detected, the program will stop with the ABA LED on. The "address" LEDs will show the address at which the defect was detected, and the "data" LEDs which are lit will indicate which data bits were incorrect at that address. Refer to Table 6-3 to find which RAM package has that address and those data bits; that is the defective RAM.

12. After the test, remove the "test" jumper that was inserted in step two.

Table 6-3

ADDRESSES OF RAM PACKAGES

Memory Addresses	RAM Packages	
	Bits 0-3	Bits 4-7
0000 - 03FF	U271	U275

TESTING THE 4924'S ROMS

To test the 4924's Read Only Memories, the System Test Fixture should have a 067-0824-00 test PROM inserted in its socket U85. The Test Fixture's ADDRESS SELECT jumper should be in its position number "9".

Before testing the 4924's ROMs, one should first check its RAMs, as the "ROM test" program uses the RAMs. Once the RAMs have been tested, use this procedure to test the ROMs:

1. Remove any tape cartridge which may be present in the 4924.
2. Insert a shorting strap at the "test" location shown on the Control board component location diagram.
3. Connect the System Test Fixture and the Test Board Buffer Adapter, and turn on power. If the test fixture's ABA (Address Bus Available) LED is on, proceed to the next step. If off, push STOP, followed by RESTART; this should light the ABA LED.
4. Turn on the System Test Fixture's RAM, PROM, DATA LATCH, ADDR LATCH, ADDR BRK and INSTR CYCLE switches; turn off the DATA BREAK switch.
5. Load hexadecimal "98" into memory location "FFFE", and "00" into "FFFF". This loads into the highest-address two memory cells the address ("9800") at which the test program begins.
6. Set the test fixture's ADDRESS switches to "FFFD". (When the MPU has finished the first part of the test program it will send "FFFD" out on its address bus. Setting "FFFD" in the ADDRESS switches sets up the "address break" function of the test fixture to interrupt program execution at that point.)
7. Load "00" into the DATA switches; then depress the RESTART switch, followed by the START switch. This starts a "relocating" routine, which copies the test routine from the System Test Fixture's ROM U85 into the 4924's RAM. The relocating routine will stop with the ABA LED on, the "address" LEDs showing "FFFD" and the "data" LEDs showing "00".
8. Change the ADDRESS switches to "00FD", and turn off the PROM and RAM switches. This switches the test fixture's PROMs and RAM out of the 4924's memory, and switches U555 back into memory.

9. Push START. The program will compute a checksum for one of the 4924's ROMs, and stop with that checksum displayed in the System Test Fixture's "data" LEDs and the address of the ROM in the "address" LEDs. Refer to Table 6-4, and compare this checksum to the checksum given in the table for the particular version of the ROM being tested. If the checksums do not agree, the ROM is defective.

10. To continue the test, push START again and repeat step 9. Each time START is pushed, the program will compute the checksum for another ROM. When it has checked the last ROM, it will start over again with the first ROM in the list.

11. When finished with the test, turn power off and remove the "test" jumper that was inserted in step two.

Table 6-4

ROM CHECKSUMS

Memory Address	ROM Package	Part Number	Checksum	Firmware Level
0800	U451	156-0777-00	9B or 8C	1, 2
		-01	7D	3
		02	A4	4
0C00	U455	156-0778-00	03	1
		-01	9B	2
		-02	AE	3, 4
1000	U465	156-0779-00	E5	1
		-01	95	2, 3, 4
1400	U475	156-0780-00	01	1
		-01	1E	2
		-02	BD	3, 4
1800	U485	156-0781-00	57	1
		-01	95	2, 3, 4
1C00	U495	156-0782-00	F9	1
		-01	D2	2
		-2	1B	3, 4

TESTING THE 4924'S HARDWARE

A program in one of the System Test Fixture's PROMs can be used to exercise some of the 4924's mechanical and electrical parts, as an aid in troubleshooting. With this program, the motor can be made to run forward and backward, and a test signal can be recorded on the tape and played back, under control of the pushbuttons on the 4924's front panel.

To use this program, a type 067-0824-00 test PROM must be inserted in socket U85 of the System Test Fixture, and that test fixture's ADDRESS SELECT jumper set to its position number "9". With the PROM in place and the jumper positioned, follow this procedure:

1. If there is a tape cartridge inserted in the 4924, remove it.
2. Refer to the Control board component location diagram (next to Schematic 1-1 in the Schematics section of this manual), and insert a shorting strap at the "test" location shown on the diagram.
3. Connect the System Test Fixture and the Test Board Buffer Adapter, as described above under "Connecting the System Test Fixture", and turn on power. If the test fixture's ABA LED is on, proceed to the next step. If off, push STOP, followed by RESTART; this should light the ABA LED.
4. Turn on the System Test Fixture's RAM, PROM, DATA LATCH, ADDR LATCH, ADDR BRK, and INSTR CYCLE switches; turn off the DATA BRK switch.
5. Load Hexadecimal "98" into memory location "FFFE", and "88" into "FFFF". This loads into the highest address two memory locations the memory address ("9888") at which the test program begins.
6. Depress the red ON LINE switch on the 4924's front panel.
7. Press RESTART, then START. This passes control of the 4924 to the test program.

ON LINE. The red ON LINE switch is used to terminate execution of commands given with the other switches. When it is released, and one of the other front-panel switches is pressed, the 4924 will perform the function commanded by that other front-panel switch, until a different switch is pressed. Depressing the ON LINE switch causes the 4924 to cease executing any command given it by another front-panel switch.

When the ON LINE switch is depressed, and another front-panel switch is pressed, the 4924 will perform the function commanded by that other switch, but only so long as that switch is pressed; as soon as the switch is released, the 4924 will cease performing that function.

FORWARD. If the FORWARD switch is pressed while a tape cartridge is in the 4924, the motor will run the tape forward at its normal speed of 30 inches per second. This will continue until the end of the tape, when the Stop Tape Control on the Read/Write board will stop the motor.

To stop the tape, depress the red ON LINE button. With ON LINE depressed, it is possible to move the tape forward, but only so long as FORWARD is held depressed; once FORWARD is released, the tape will stop.

REVERSE. The REVERSE switch functions similarly to the FORWARD switch, except that it moves the tape backward.

REWIND. The REWIND switch, when pressed, causes the tape to move backward at its faster speed of 90 inches per second. When the beginning of the tape is reached, the motor will stop.

TALK. If the TALK switch is pressed while a tape cartridge is in the 4924, the motor will run the tape forward at its normal speed (30 inches per second), and the 4924 will record on the tape a test pattern (the binary byte "10101010", or hexadecimal "AA", repeated again and again.) This will continue until the end of the tape is reached or the red ON LINE button is depressed.

If no cartridge is present when TALK is depressed, the motor will still drive, and the DRIVE TAPE signal (a low at J324-7 on the Read/Write board) and the FORWARD signal (a low at J324-6 on the same board) will still be present.

In any case, when TALK is pressed the WRITE CLOCK and WRITE DATA waveforms can be observed at TP21 and TP545 on the Control board. Put your oscilloscope on TP21 or TP545, taking a synchronizing signal from TP45. (Trigger from TP45 on a low level at negative slope.) The waveforms are illustrated in Fig. 6-6.

To stop writing test data, depress the red ON LINE button. With ON LINE depressed, it is possible to write on the tape, but only so long as TALK is held depressed; once TALK is released, the writing of data will stop.

Using the External System Test Fixture

LISTEN. When LISTEN is pressed, if a cartridge is present, the tape will run forward and the 4924 will read from the tape. Normally, one would first record test data on the tape using the TALK switch, and then read it from the tape using the LISTEN switch. With the 4924 reading the test data from the tape, the READ CLOCK and READ DATA lines may be monitored on an oscilloscope; the waveforms should resemble those in Fig. 6-6. (In this case, do not trigger the scope from TP41; but from the READIT line, U15 pin 9.)

When finished using this test program to exercise the 4924, turn power off, disconnect the test fixture, and remove the "test" strap from the 4924 Control board.

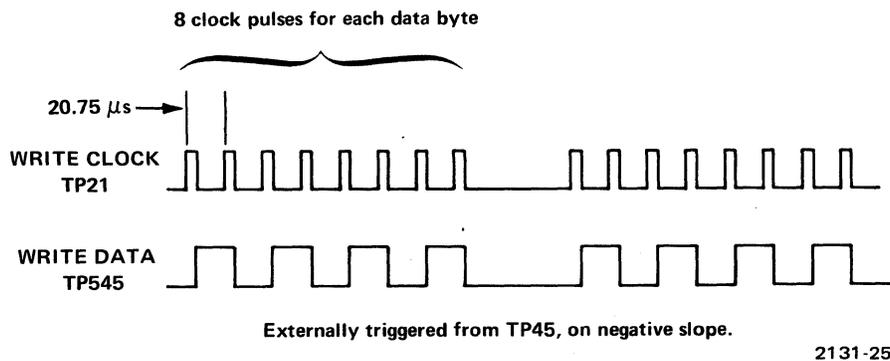


Fig. 6-6. Write waveforms.

Section 7

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000 Part first added at this serial number
00X Part removed after this serial number

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

REPLACEABLE ELECTRICAL PARTS

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01963	CHERRY ELECTRICAL PRODUCTS CORPORATION	3600 SUNSET AVENUE	WAUKEGAN, IL 60085
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
04009	ARROW-HART, INC.	103 HAWTHORNE STREET	HARTFORD, CT 06106
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD, PO BOX 20923	PHOENIX, AZ 85036
05624	BARBER-COLMAN COMPANY	1300 ROCK STREET	ROCKFORD, IL 61101
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
10389	CHICAGO SWITCH, INC.	2035 WABANSIA AVE.	CHICAGO, IL 60647
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
31718	FAIRCHILD MICROWAVE AND OPTOELECTRONICS, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	4001 MIRANDA AVE.	PALO ALTO, CA 94304
32159	WEST-CAP ARIZONA	2201 E. ELVIRA ROAD	TUCSON, AZ 85706
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
33096	COLORADO CRYSTAL CORPORATION	2303 W 8TH STREET	LOVELAND, CO 80537
34371	HARRIS SEMICONDUCTOR, DIV. OF HARRIS CORPORATION	P. O. BOX 883	MELBOURNE, FL 32901
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
50558	ELECTRONIC CONCEPTS, INC.	526 INDUSTRIAL WAY WEST	EATONTOWN, NJ 07724
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
58361	GENERAL INSTRUMENT CORP. OPTO ELECTRONICS DIV.	3400 HILLVIEW AVE	PALO ALTO, CA 94304
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
71590	CENTRALAB ELECTRONICS, DIV. OF GLOBE-UNION, INC.	P O BOX 858	FORT DODGE, IA 50501
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
76854	OAK INDUSTRIES, INC., SWITCH DIV.	S. MAIN ST.	CRYSTAL LAKE, IL 60014
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91418	RADIO MATERIALS COMPANY, DIV. OF P.R. MALLORY AND COMPANY, INC.	4242 W BRYN MAWR	CHICAGO, IL 60646
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
98938	PITTMAN CORPORATION, A SUBSIDIARY OF PENN ENGINEERING AND MFG. CORPORATION	P O BOX 150 W PARK AVE.	SELLERSVILLE, PA 18960

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
CIRCUIT BOARD ASSEMBLIES						
A1	670-3853-03			CKT BOARD ASSY:POWER SUPPLY	80009	670-3853-03
A2	670-4526-00			CKT BOARD ASSY:SWITCH & LED	80009	670-4526-00
A3	672-0573-01			CKT BOARD ASSY:STATUS	80009	672-0573-01
A4	670-3925-04	B010100	B040804	CKT BOARD ASSY:READ/WRITE	80009	670-3925-04
A4	670-3925-05	B040805	B041117	CKT BOARD ASSY:READ/WRITE	80009	670-3925-05
A4	670-3925-06	B041118		CKT BOARD ASSY:READ/WRITE	80009	670-3925-06
A5	670-4524-00			CKT BOARD ASSY:MODE/ADDRESS SELECT	80009	670-4524-00
A5	670-4524-01	B010100	B029999	CKT BOARD ASSY:MODE/ADDRESS SELECT	80009	670-4524-01
A5	670-4524-02	B030000		CKT BOARD ASSY:MODE/ADDRESS SELECT	80009	670-4524-02
A5	670-4888-00			CKT BOARD ASSY:MODE/ADDRESS SELECT (OPTION 37 ONLY)	80009	670-4888-00
A5	670-4888-01	B010100	B029999X	CKT BOARD ASSY:MODE/ADDRESS SELECT (OPTION 37 ONLY)	80009	670-4888-01
A6	670-4525-00	B010100	B019999	CKT BOARD ASSY:CONTROL	80009	670-4525-00
A6	670-4525-01	B020000	B039999	CKT BOARD ASSY:CONTROL	80009	670-4525-01
A6	670-4525-02	B040000	B040692	CKT BOARD ASSY:CONTROL	80009	670-4525-02
A6	670-4525-03	B040693	B041173	CKT BOARD ASSY:CONTROL	80009	670-4525-03
A6	670-4525-04	B041174	B041375	CKT BOARD ASSY:CONTROL	80009	670-4525-04
A6	670-4525-05	B041376		CKT BOARD ASSY:CONTROL	80009	670-4525-05
A6	670-4887-00	B010100	B019999X	CKT BOARD ASSY:CONTROL (OPTION 37 ONLY. REPLACED BY 670-4525-01)	80009	670-4887-00
A7	670-4513-00	B010100	B041117	CKT BOARD ASSY:MOTOR FILTER	80009	670-4513-00
A7	670-4513-01	B041118		CKT BOARD ASSY:MOTOR FILTER	80009	670-4513-01
A1	670-3853-03			CKT BOARD ASSY:POWER SUPPLY	80009	670-3853-03
C11	281-0771-00			CAP.,FXD,CER DI:0.0022UF,20%,200V	56289	292C Z5U222M200B
C19	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C41	290-0301-00			CAP.,FXD,ELCTLT:10UF,10%,20V	56289	150D106X9020B2
C42	281-0580-00			CAP.,FXD,CER DI:470PF,10%,500V	04222	7001-1374
C43	290-0297-00			CAP.,FXD,ELCTLT:39UF,10%,10V	56289	150D396X9010B2
C49	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
C50	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100COG101J
C65	290-0187-00			CAP.,FXD,ELCTLT:4.7UF,20%,35V	56289	150D475X0035B2
C69	290-0301-00			CAP.,FXD,ELCTLT:10UF,10%,20V	56289	150D106X9020B2
C82	290-0506-00			CAP.,FXD,ELCTLT:9600UF,+100-10%,25V	56289	68D10471
C168	290-0508-00			CAP.,FXD,ELCTLT:18,000UF,+100-10%,15V	56289	68D10444
C176	290-0255-00			CAP.,FXD,ELCTLT:20UF,50V	56289	30D206G050CC9
C182	290-0506-00			CAP.,FXD,ELCTLT:9600UF,+100-10%,25V	56289	68D10471
CR33	151-0506-00			SCR:SILICON	03508	C106B2X283
CR44	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
CR58	152-0107-00			SEMICOND DEVICE:SILICON,400V,400MA	01295	G727
CR61	152-0107-00			SEMICOND DEVICE:SILICON,400V,400MA	01295	G727
CR88	152-0462-00			SEMICOND DEVICE:RECT,SI,200V,2.5A	04713	SDA10228
CR153	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
CR154	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
CR173	152-0107-00			SEMICOND DEVICE:SILICON,400V,400MA	01295	G727
CR174	152-0107-00			SEMICOND DEVICE:SILICON,400V,400MA	01295	G727
F72	159-0015-00			FUSE,CARTRIDGE:3AG,3A,250V,0.65 SEC	71400	AGC 3
F74	159-0015-00			FUSE,CARTRIDGE:3AG,3A,250V,0.65 SEC	71400	AGC 3
F76	159-0015-00			FUSE,CARTRIDGE:3AG,3A,250V,0.65 SEC	71400	AGC 3
R5	321-0630-00			RES.,FXD,FILM:6.81K OHM,0.5%,0.125W	91637	MFF1816G68100D
R7	321-0613-01			RES.,FXD,FILM:5.03K OHM,0.5%,0.125W	91637	MFF1816G50300D

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
R8	321-0238-00		RES.,FXD,FILM:2.94K OHM,1%,0.125W	91637	MFF1816G29400F
R9	321-0239-00		RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
R15	315-0471-00		RES.,FXD,CMPNS:470 OHM,5%,0.25W	01121	CB4715
R17	315-0470-00		RES.,FXD,CMPNS:47 OHM,5%,0.25W	01121	CB4705
R19	315-0102-00		RES.,FXD,CMPNS:1K OHM,5%,0.25W	01121	CB1025
R33	321-0222-00		RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
R35	308-0767-00		RES.,FXD,WW:1.1 OHM,5%,1W	75042	BW20-1R100J
R37	321-0210-00		RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
R39	311-1563-00		RES.,VAR,NONWIR:1K OHM,20%,0.50W	73138	91-85-0
R45	321-0268-00		RES.,FXD,FILM:6.04K OHM,1%,0.125W	91637	MFF1816G60400F
R47	321-0297-00		RES.,FXD,FILM:12.1K OHM,1%,0.125W	91637	MFF1816G12101F
R49	321-0297-00		RES.,FXD,FILM:12.1K OHM,1%,0.125W	91637	MFF1816G12101F
R57	315-0101-00		RES.,FXD,CMPNS:100 OHM,5%,0.25W	01121	CB1015
R63	315-0100-00		RES.,FXD,CMPNS:10 OHM,5%,0.25W	01121	CB1005
R67	308-0685-00		RES.,FXD,WW:1.5 OHM,5%,1W	75042	BW20-1R500J
R88	302-0272-00		RES.,FXD,CMPNS:2.7K OHM,10%,0.50W	01121	EB2721
R175	302-0272-00		RES.,FXD,CMPNS:2.7K OHM,10%,0.50W	01121	EB2721
U9	156-0067-00		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
U39	156-0071-00		MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC1723CL
U53	156-0067-00		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
VR13	152-0175-00		SEMICONV DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008
A2	670-4526-00		CKT BOARD ASSY:SWITCH & LED	80009	670-4526-00
C135	283-0010-00		CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C151	283-0010-00		CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C165	281-0536-00		CAP.,FXD,CER DI:1000PF,10%,500V	72982	301000 X 5P0102K
DS35	150-1014-00		LAMP,LED:RED,50MA	58361	Q6444/MV5054-1
DS45	150-1014-00		LAMP,LED:RED,50MA	58361	Q6444/MV5054-1
DS61	150-1014-00		LAMP,LED:RED,50MA	58361	Q6444/MV5054-1
DS75	150-1014-00		LAMP,LED:RED,50MA	58361	Q6444/MV5054-1
DS85	150-1014-00		LAMP,LED:RED,50MA	58361	Q6444/MV5054-1
R15	315-0472-00		RES.,FXD,CMPNS:4.7K OHM,5%,0.25W	01121	CB4725
R25	315-0511-00		RES.,FXD,CMPNS:510 OHM,5%,0.25W	01121	CB5115
R39	315-0511-00		RES.,FXD,CMPNS:510 OHM,5%,0.25W	01121	CB5115
R51	315-0511-00		RES.,FXD,CMPNS:510 OHM,5%,0.25W	01121	CB5115
R81	315-0511-00		RES.,FXD,CMPNS:510 OHM,5%,0.25W	01121	CB5115
R95	315-0511-00		RES.,FXD,CMPNS:510 OHM,5%,0.25W	01121	CB5115
R165	315-0220-00		RES.,FXD,CMPNS:22 OHM,5%,0.25W	01121	CB2205
S15	260-1769-00		SWITCH,PUSH:6 BTN,2 POLE,MOMENTARY	71590	2KDM060000-801
S35					
S45					
S61					
S75					
S85					
U105	156-0508-00		MICROCIRCUIT,DI:QUAD R-S LATCH,TTL	01295	SN74279N
U135	156-0381-00		MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATES	80009	156-0381-00
U151	156-0030-00		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7400(N OR J)
U165	156-0047-00		MICROCIRCUIT,DI:TPL 3-INPUT POS NAND GATE	80009	156-0047-00
U181	156-0058-00		MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3	672-0573-01			CKT BOARD ASSY:STATUS	80009	672-0573-01
DS1	150-0057-01			LAMP, INCAND:5V,0.115A,WIRE LD,SEL	76854	17AS15
Q1	151-0648-00			XSTR, PHOTO:SILICON,NPN	31718	FPT 120A
Q2	151-0648-00			XSTR, PHOTO:SILICON,NPN	31718	FPT 120A
Q3	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
Q4	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
R1	315-0102-00			RES., FXD, CMPSN:1K OHM,5%,0.25W	01121	CB1025
R2	315-0102-00			RES., FXD, CMPSN:1K OHM,5%,0.25W	01121	CB1025
R3	315-0475-00			RES., FXD, CMPSN:4.7M OHM,5%,0.25W	01121	CB4755
R4	315-0475-00			RES., FXD, CMPSN:4.7M OHM,5%,0.25W	01121	CB4755
R5	315-0202-00			RES., FXD, CMPSN:2K OHM,5%,0.25W	01121	CB2025
R6	315-0202-00			RES., FXD, CMPSN:2K OHM,5%,0.25W	01121	CB2025
R7	315-0201-00			RES., FXD, CMPSN:200 OHM,5%,0.25W	01121	CB2015
R8	307-0111-00			RES., FXD, CMPSN:3.6 OHM,5%,0.25W	01121	CB36G5
S1	260-1748-00			SWITCH,PUSH:SPDT,0.1A,125VAC,LVR ACTR	01963	E63-02HB
S2	260-1748-00			SWITCH,PUSH:SPDT,0.1A,125VAC,LVR ACTR	01963	E63-02HB
A4	670-3925-04	B010100	B040804	CKT BOARD ASSY:READ/WRITE	80009	670-3925-04
A4	670-3925-05	B040805	B041117	CKT BOARD ASSY:READ/WRITE	80009	670-3925-05
A4	670-3935-06	B041118		CKT BOARD ASSY:READ/WRITE	80009	670-3935-06
C8	281-0510-00			CAP., FXD, CER DI:22PF,+/-4.4PF,500V	59660	301-000C0G0220M
C9	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C10	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C11	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C24	281-0605-00			CAP., FXD, CER DI:200PF,10%,500V	04222	7001-1375
C29	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C38	283-0065-00			CAP., FXD, CER DI:0.001UF,5%,100V	72982	805-518-Z5D0102J
C45	283-0065-00			CAP., FXD, CER DI:0.001UF,5%,100V	72982	805-518-Z5D0102J
C72	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C75	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C78	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C80	290-0297-00			CAP., FXD, ELCTLT:39UF,10%,10V	56289	150D396X9010B2
C85	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C86	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C90	283-0177-00			CAP., FXD, CER DI:1UF,+80-20%,25V	56289	273C5
C98	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C111	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C121	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C126	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C127	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C137	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C151	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C166	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C177	281-0775-00			CAP., FXD, CER DI:0.1UF,20%,50V	04222	SA205E104MAA
C186	283-0119-00			CAP., FXD, CER DI:220PF,5%,200V	59660	855-536Y5E0222J
C202	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C209	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C210	281-0510-00			CAP., FXD, CER DI:22PF,+/-4.4PF,500V	59660	301-000C0G0220M
C215	281-0773-00			CAP., FXD, CER DI:0.01UF,10%,100V	04222	GC70-1C103K
C224	281-0605-00			CAP., FXD, CER DI:200PF,10%,500V	04222	7001-1375
C239	281-0523-00			CAP., FXD, CER DI:100PF,+/-20PF,500V	72982	301-000U2M0101M
C244	281-0523-00			CAP., FXD, CER DI:100PF,+/-20PF,500V	72982	301-000U2M0101M

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
C251	281-0775-00		CAP., FXD, CER DI:0.1UF, 20%, 50V	04222	SA205E104MAA
C252	281-0770-00		CAP., FXD, CER DI:0.001UF, 20%, 100V	72982	8035D9AADX5R102M
C264	285-1130-00		CAP., FXD, PLSTC:0.22UF, 1%, 100V	50558	MH12D224F
C269	281-0772-00		CAP., FXD, CER DI:0.0047UF, 10%, 100V	04222	GC701C472K
C280	281-0773-00		CAP., FXD, CER DI:0.01UF, 10%, 100V	04222	GC70-1C103K
C288	283-0080-00		CAP., FXD, CER DI:0.022UF, +80-20%, 25V	91418	MX223Z2504R0
C295	285-1130-00		CAP., FXD, PLSTC:0.22UF, 1%, 100V	50558	MH12D224F
CR3	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR5	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR6	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR8	152-0141-00		SEMICON D DEVICE:SILICON, 30V, 150MA	80009	152-0141-00
CR19	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR20	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR21	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR22	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR72	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR77	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR88	152-0107-00		SEMICON D DEVICE:SILICON, 400V, 400MA	01295	G727
CR99	152-0107-00		SEMICON D DEVICE:SILICON, 400V, 400MA	01295	G727
CR102	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR104	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR105	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR107	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR113	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR115	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR124	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR125	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR172	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR173	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR174	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR175	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR219	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR220	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR221	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR222	152-0141-02		SEMICON D DEVICE:SILICON, 30V, 150MA	01295	1N4152R
CR288	152-0585-00		SEMICON D DEVICE:SILICON, BRIDGE, 200V, 1A	80009	152-0585-00
Q41	151-0192-00		TRANSISTOR:SILICON, NPN, SEL FROM MPS6521	04713	SPS8801
Q42	151-0192-00		TRANSISTOR:SILICON, NPN, SEL FROM MPS6521	04713	SPS8801
Q141	151-0188-00		TRANSISTOR:SILICON, PNP	04713	SPS6868K
Q142	151-0190-00		TRANSISTOR:SILICON, NPN	07263	S032677
Q183	151-0188-00		TRANSISTOR:SILICON, PNP	04713	SPS6868K
Q184	151-0190-00		TRANSISTOR:SILICON, NPN	07263	S032677
Q185	151-0188-00		TRANSISTOR:SILICON, PNP	04713	SPS6868K
Q191	151-0190-00		TRANSISTOR:SILICON, NPN	07263	S032677
Q195	151-0188-00		TRANSISTOR:SILICON, PNP	04713	SPS6868K
Q279	151-1066-00		TRANSISTOR:SILICON, FE, P-CHANNEL	80009	151-1066-00
R1	315-0473-00		RES., FXD, CMPSN:47K OHM, 5%, 0.25W	01121	CB4735
R2	321-0466-00		RES., FXD, FILM:698K OHM, 1%, 0.125W	91637	MFF1816G69802F
R4	321-0236-00		RES., FXD, FILM:2.8K OHM, 1%, 0.125W	91637	MFF1816G28000F
R7	321-0236-00		RES., FXD, FILM:2.8K OHM, 1%, 0.125W	91637	MFF1816G28000F
R9	321-0466-00		RES., FXD, FILM:698K OHM, 1%, 0.125W	91637	MFF1816G69802F
R10	315-0473-00		RES., FXD, CMPSN:47K OHM, 5%, 0.25W	01121	CB4735
R13	311-1235-00		RES., VAR, NONWIR:100K OHM, 20%, 0.50W	32997	3386F-T04-104
R17	315-0102-00		RES., FXD, CMPSN:1K OHM, 5%, 0.25W	01121	CB1025
R18	315-0912-00		RES., FXD, CMPSN:9.1K OHM, 5%, 0.25W	01121	CB9125
R23	315-0394-00		RES., FXD, CMPSN:390K OHM, 5%, 0.25W	01121	CB3945

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R24	321-0260-00			RES., FXD, FILM: 4.99K OHM, 1%, 0.125W	91637	MFF1816G49900F
R27	315-0104-00			RES., FXD, CMPSN: 100K OHM, 5%, 0.25W	01121	CB1045
R28	321-0371-00			RES., FXD, FILM: 71.5K OHM, 1%, 0.125W	91637	MFF1816G71501F
R37	315-0473-00			RES., FXD, CMPSN: 47K OHM, 5%, 0.25W	01121	CB4735
R39	315-0472-00			RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R44	315-0473-00			RES., FXD, CMPSN: 47K OHM, 5%, 0.25W	01121	CB4735
R71	315-0202-00			RES., FXD, CMPSN: 2K OHM, 5%, 0.25W	01121	CB2025
R73	315-0100-00			RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R76	315-0100-00			RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R81	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R82	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R83	315-0102-00			RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R87	307-0093-00			RES., FXD, CMPSN: 1.2 OHM, 5%, 0.50W	01121	EB12G5
R89	315-0564-00			RES., FXD, CMPSN: 560K OHM, 5%, 0.25W	01121	CB5645
R91	315-0621-00			RES., FXD, CMPSN: 620 OHM, 5%, 0.25W	01121	CB6215
R92	315-0202-00			RES., FXD, CMPSN: 2K OHM, 5%, 0.25W	01121	CB2025
R93	315-0681-00			RES., FXD, CMPSN: 680 OHM, 5%, 0.25W	01121	CB6815
R94	315-0102-00			RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R95	315-0681-00			RES., FXD, CMPSN: 680 OHM, 5%, 0.25W	01121	CB6815
R96	315-0102-00			RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R97	315-0104-00			RES., FXD, CMPSN: 100K OHM, 5%, 0.25W	01121	CB1045
R101	315-0473-00			RES., FXD, CMPSN: 47K OHM, 5%, 0.25W	01121	CB4735
R103	321-0236-00			RES., FXD, FILM: 2.8K OHM, 1%, 0.125W	91637	MFF1816G28000F
R106	321-0236-00			RES., FXD, FILM: 2.8K OHM, 1%, 0.125W	91637	MFF1816G28000F
R109	315-0473-00			RES., FXD, CMPSN: 47K OHM, 5%, 0.25W	01121	CB4735
R110	315-0473-00			RES., FXD, CMPSN: 47K OHM, 5%, 0.25W	01121	CB4735
R112	321-0354-00			RES., FXD, FILM: 47.5K OHM, 1%, 0.125W	91637	MFF1816G47501F
R114	321-0354-00			RES., FXD, FILM: 47.5K OHM, 1%, 0.125W	91637	MFF1816G47501F
R122	321-0354-00			RES., FXD, FILM: 47.5K OHM, 1%, 0.125W	91637	MFF1816G47501F
R123	321-0354-00			RES., FXD, FILM: 47.5K OHM, 1%, 0.125W	91637	MFF1816G47501F
R125	315-0153-00			RES., FXD, CMPSN: 15K OHM, 5%, 0.25W	01121	CB1535
R139	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R143	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R144	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R145	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R148	315-0472-00			RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R178	315-0202-00			RES., FXD, CMPSN: 2K OHM, 5%, 0.25W	01121	CB2025
R179	315-0472-00			RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R180	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R181	315-0472-00			RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R182	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R183	315-0103-00			RES., FXD, CMPSN: 10K OHM, 5%, 0.25W	01121	CB1035
R186	311-1560-00	B010100	B040804	RES., VAR, NONWIR: 5K OHM, 20%, 0.50W	73138	91-82-0
R186	311-1896-00	B040805		RES., VAR, NONWIR: 5K OHM, 10%, 0.50W	32997	3299W-1-502
R187	315-0474-00			RES., FXD, CMPSN: 470K OHM, 5%, 0.25W	01121	CB4745
R188	321-0254-00			RES., FXD, FILM: 4.32K OHM, 1%, 0.125W	91637	MFF1816G43200F
R189	321-0285-00			RES., FXD, FILM: 9.09K OHM, 1%, 0.125W	91637	MFF1816G90900F
R190	315-0392-00			RES., FXD, CMPSN: 3.9K OHM, 5%, 0.25W	01121	CB3925
R197	315-0102-00			RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R201	321-0466-00			RES., FXD, FILM: 698K OHM, 1%, 0.125W	91637	MFF1816G69802F
R208	321-0466-00			RES., FXD, FILM: 698K OHM, 1%, 0.125W	91637	MFF1816G69802F
R213	311-1235-00			RES., VAR, NONWIR: 100K OHM, 20%, 0.50W	32997	3386F-T04-104
R216	315-0153-00			RES., FXD, CMPSN: 15K OHM, 5%, 0.25W	01121	CB1535
R217	315-0102-00			RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R218	315-0912-00			RES., FXD, CMPSN: 9.1K OHM, 5%, 0.25W	01121	CB9125
R223	315-0394-00			RES., FXD, CMPSN: 390K OHM, 5%, 0.25W	01121	CB3945
R224	321-0260-00			RES., FXD, FILM: 4.99K OHM, 1%, 0.125W	91637	MFF1816G49900F

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R227	315-0104-00			RES., FXD, CMPSN:100K OHM, 5%, 0.25W	01121	CB1045
R228	321-0371-00			RES., FXD, FILM:71.5K OHM, 1%, 0.125W	91637	MFF1816G71501F
R229	315-0622-00			RES., FXD, CMPSN:6.2K OHM, 5%, 0.25W	01121	CB6225
R230	315-0512-00			RES., FXD, CMPSN:5.1K OHM, 5%, 0.25W	01121	CB5125
R236	315-0622-00			RES., FXD, CMPSN:6.2K OHM, 5%, 0.25W	01121	CB6225
R237	315-0512-00			RES., FXD, CMPSN:5.1K OHM, 5%, 0.25W	01121	CB5125
R239	315-0203-00			RES., FXD, CMPSN:20K OHM, 5%, 0.25W	01121	CB2035
R245	315-0203-00			RES., FXD, CMPSN:20K OHM, 5%, 0.25W	01121	CB2035
R258	315-0101-00			RES., FXD, CMPSN:100 OHM, 5%, 0.25W	01121	CB1015
R263	321-0415-00			RES., FXD, FILM:205K OHM, 1%, 0.125W	91637	MFF1816G20502F
R270	315-0513-00			RES., FXD, CMPSN:51K OHM, 5%, 0.25W	01121	CB5135
R271	315-0102-00			RES., FXD, CMPSN:1K OHM, 5%, 0.25W	01121	CB1025
R272	315-0106-00			RES., FXD, CMPSN:10M OHM, 5%, 0.25W	01121	CB1065
R273	315-0473-00			RES., FXD, CMPSN:47K OHM, 5%, 0.25W	01121	CB4735
R274	315-0473-00			RES., FXD, CMPSN:47K OHM, 5%, 0.25W	01121	CB4735
R275	315-0473-00			RES., FXD, CMPSN:47K OHM, 5%, 0.25W	01121	CB4735
R276	315-0106-00			RES., FXD, CMPSN:10M OHM, 5%, 0.25W	01121	CB1065
R277	315-0473-00			RES., FXD, CMPSN:47K OHM, 5%, 0.25W	01121	CB4735
R278	315-0223-00			RES., FXD, CMPSN:22K OHM, 5%, 0.25W	01121	CB2235
R281	321-0272-00			RES., FXD, FILM:6.65K OHM, 1%, 0.125W	91637	MFF1816G66500F
R282	321-0318-00			RES., FXD, FILM:20K OHM, 1%, 0.125W	91637	MFF1816G20001F
R283	321-0230-00			RES., FXD, FILM:2.43K OHM, 1%, 0.125W	91637	MFF1816G24300F
R284	321-0230-00			RES., FXD, FILM:2.43K OHM, 1%, 0.125W	91637	MFF1816G24300F
R285	321-0132-00			RES., FXD, FILM:232 OHM, 1%, 0.125W	91637	MFF1816G232R0F
R286	315-0104-00			RES., FXD, CMPSN:100K OHM, 5%, 0.25W	01121	CB1045
R290	321-0347-00			RES., FXD, FILM:40.2K OHM, 1%, 0.125W	91637	MFF1816G40201F
R291	321-0260-00			RES., FXD, FILM:4.99K OHM, 1%, 0.125W	91637	MFF1816G49900F
R293	321-0369-00			RES., FXD, FILM:68.1K OHM, 1%, 0.125W	91637	MFF1816G68101F
R298	321-0260-00			RES., FXD, FILM:4.99K OHM, 1%, 0.125W	91637	MFF1816G49900F
R299	321-0193-00			RES., FXD, FILM:1K OHM, 1%, 0.125W	91637	MFF1816G10000F
U5	156-0317-00			MICROCIRCUIT, LI: OPERATIONAL AMPLIFIER	34371	HA2-2625-5
U25	156-0096-00			MICROCIRCUIT, LI: VOLTAGE COMPARATOR	27014	LM311H
U35	156-0039-00			MICROCIRCUIT, DI: DUAL J-K FLIP FLOP	80009	156-0039-00
U47	156-0058-00			MICROCIRCUIT, DI: HEX. INVERTER	80009	156-0058-00
U51	156-0388-00			MICROCIRCUIT, DI: DUAL D-TYPE FLIP-FLOP	80009	156-0388-00
U59	156-0047-00			MICROCIRCUIT, DI: TPL 3-INPUT POS NAND GATE	80009	156-0047-00
U63	156-0058-00			MICROCIRCUIT, DI: HEX. INVERTER	80009	156-0058-00
U69	156-0371-00			MICROCIRCUIT, DI: QUAD 2-INPUT NAND ST	80009	156-0371-00
U117	156-0158-00			MICROCIRCUIT, LI: DUAL OPERATIONAL AMPLIFIER	18324	MC1458N
U135	156-0112-00			MICROCIRCUIT, DI: QUAD 2-INPUT POS NAND GATE	80009	156-0112-00
U147	156-0371-00			MICROCIRCUIT, DI: QUAD 2-INPUT NAND ST	80009	156-0371-00
U159	156-0041-00			MICROCIRCUIT, DI: DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U163	156-0043-00			MICROCIRCUIT, DI: QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U169	156-0112-00			MICROCIRCUIT, DI: QUAD 2-INPUT POS NAND GATE	80009	156-0112-00
U174	156-0158-00			MICROCIRCUIT, LI: DUAL OPERATIONAL AMPLIFIER	18324	MC1458N
U195	156-0067-00			MICROCIRCUIT, LI: OPERATIONAL AMPLIFIER	01295	MICROA741CP
U215	156-0317-00			MICROCIRCUIT, LI: OPERATIONAL AMPLIFIER	34371	HA2-2625-5
U225	156-0096-00			MICROCIRCUIT, LI: VOLTAGE COMPARATOR	27014	LM311H
U235	156-0030-00			MICROCIRCUIT, DI: QUAD 2-INPUT NAND GATE	01295	SN7400(N OR J)
U241	156-0487-00			MICROCIRCUIT, DI: DUAL RETRIG, ONE SHOT	80009	156-0487-00
U247	156-0043-00			MICROCIRCUIT, DI: QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U261	156-0047-00			MICROCIRCUIT, DI: TPL 3-INPUT POS NAND GATE	80009	156-0047-00
U267	156-0487-00			MICROCIRCUIT, DI: DUAL RETRIG, ONE SHOT	80009	156-0487-00
U288	156-0158-00			MICROCIRCUIT, LI: DUAL OPERATIONAL AMPLIFIER	18324	MC1458N

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5	670-4524-00			CKT BOARD ASSY:MODE/ADDRESS SELECT	80009	670-4524-00
A5	670-4524-01	B010100	B029999	CKT BOARD ASSY:MODE/ADDRESS SELECT	80009	670-4524-01
A5	670-4524-02	B030000		CKT BOARD ASSY:MODE/ADDRESS SELECT	80009	670-4524-02
A5	670-4888-00			CKT BOARD ASSY:MODE/ADDRESS SELECT	80009	670-4888-00
	-----			(OPTION 37 ONLY)		
A5	670-4888-01	B010100	B029999X	CKT BOARD ASSY:MODE/ADDRESS SELECT	80009	670-4888-01
	-----			(OPTION 37 ONLY)		
C1	283-0178-00			CAP., FXD, CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
R101	307-0383-00			RES., FXD, FILM:4.7K OHM,2%,1.5W	73138	899-1-R4.7K
R102	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
S101	260-1721-00			SWITCH,ROCKER:8,SPST,125MA,30VDC	00779	435166-5

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6	670-4525-00	B010100	B019999	CKT BOARD ASSY:CONTROL	80009	670-4525-00
A6	670-4525-01	B020000	B039999	CKT BOARD ASSY:CONTROL	80009	670-4525-01
A6	670-4525-02	B040000	B040692	CKT BOARD ASSY:CONTROL	80009	670-4525-02
A6	670-4525-03	B040693	B041173	CKT BOARD ASSY:CONTROL	80009	670-4525-03
A6	670-4525-04	B041174	B041375	CKT BOARD ASSY:CONTROL	80009	670-4525-04
A6	670-4525-05	B041376		CKT BOARD ASSY:CONTROL	80009	670-4525-05
A6	670-4887-00 -----	B010100	B019999X	CKT BOARD ASSY:CONTROL (OPTION 37 ONLY. REPLACED BY 670-4525-01)	80009	670-4887-00
C1	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C2	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C3	290-0745-00	B010100	B041173X	CAP., FXD, ELCTLT:22UF,+50-10%,25V	56289	502D225
C4	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C5	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C12	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C15	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C21	283-0083-00	B010100	B041173X	CAP., FXD, CER DI:0.0047UF,20%,500V	72982	811-565C471J
C23	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C25	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C26	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C31	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C35	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C45	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C50	290-0745-00	B010100	B041173X	CAP., FXD, ELCTLT:22UF,+50-10%,25V	56289	502D225
C51	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C55	283-0010-00 -----	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V (C55 AND U155 INSTALLED AS A PAIR)	56289	273C20
C101	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C107	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C109	290-0245-00	XB041174		CAP., FXD, ELCTLT:1.5UF,10%,10V	56289	150D155X9010A2
C112	283-0647-00	XB041174		CAP., FXD, MICA D:70PF,1%,100V	00853	D151E700F0
C115	281-0592-00	B010100	B041173X	CAP., FXD, CER DI:4.7PF,+/-0.5PF,500V	59660	301-000-C0H0479D
C116	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C117	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C125	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C131	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C133	283-0114-00	XB041174		CAP., FXD, CER DI:0.0015UF,5%,200V	72982	805-509B152J
C135	283-0114-00	XB041174		CAP., FXD, CER DI:0.0015UF,5%,200V	72982	805-509B152J
C141	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C142	283-0083-00	B010100	B041173X	CAP., FXD, CER DI:0.0047UF,20%,500V	72982	811-565C471J
C143	285-1067-00	B010100	B041173X	CAP., FXD, PLSTC:0.5UF,1%,200V	14752	230B1C504F
C151	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C155	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C156	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C201	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C205	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C211	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C215	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C221	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C231	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C251	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C253	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C255	283-0010-00	B010100	B041173	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C255	283-0422-00	B041174		CAP., FXD, CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C257	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C258	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF,+100-20%,50V	56289	273C20
C261	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C265	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C271	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C275	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C281	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C301	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C302	283-0647-00	B010100	B041173X	CAP., FXD, MICA D:70PF, 1%, 100V	00853	D151E700FO
C305	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C311	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C315	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C321	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C325	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C331	283-0010-00	B010100	B041173	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C331	283-0422-00	B041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C341	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C351	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C376	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C405	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C411	283-0010-00	B010100	B041173	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C411	283-0422-00	B041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C412	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C413	283-0114-00	B010100	B041173X	CAP., FXD, CER DI:0.0015UF, 5%, 200V	72982	805-509B152J
C415	283-0010-00	B010100	B041173	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C415	283-0422-00	B041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C416	290-0745-00	B010100	B041173X	CAP., FXD, ELCTLT: 22UF, +50-10%, 25V	56289	502D225
C417	283-0114-00	B010100	B041173X	CAP., FXD, CER DI:0.0015UF, 5%, 200V	72982	805-509B152J
C421	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C425	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C431	283-0010-00	B010100	B041173	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C431	283-0422-00	B041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C432	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C445	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C451	283-0010-00	B010100	B041173	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C451	283-0422-00	B041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C453	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C455	283-0010-00	B010100	B041173	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C455	283-0422-00	B041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C456	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C465	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C475	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C485	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C495	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C501	283-0010-00	B010100	B041173	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C501	283-0422-00	B041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C511	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C515	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C523	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C535	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C541	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C551	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C555	283-0010-00	B010100	B041173X	CAP., FXD, CER DI:0.05UF, +100-20%, 50V	56289	273C20
C556	290-0745-00	B010100	B041173X	CAP., FXD, ELCTLT: 22UF, +50-10%, 25V	56289	502D225
C563	283-0775-00	XB041174		CAP., FXD, MICA D:1764 PF, 1%, 500V	00853	D19-5F17640FO
C565	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C575	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C581	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C585	283-0422-00	XB041174		CAP., FXD, CER DI:0.047UF, +80-20%, 50V	04222	DG015E473Z
C601	290-0245-00	XB041174		CAP., FXD, ELCTLT: 1.5UF, 10%, 10V	56289	150D155X9010A2

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C602	283-0010-00	B010100	B041173	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C602	290-0245-00	B041174		CAP.,FXD,ELCTLT:1.5UF,10%,10V	56289	150D155X9010A2
C603	283-0010-00	B010100	B041173	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C603	290-0245-00	B041174		CAP.,FXD,ELCTLT:1.5UF,10%,10V	56289	150D155X9010A2
C605	290-0245-00	B010100	B041173X	CAP.,FXD,ELCTLT:1.5UF,10%,10V	56289	150D155X9010A2
C607	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C611	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C612	281-0592-00	XB041174		CAP.,FXD,CER DI:4.7PF,+/-0.5PF,500V	59660	301-000-C0H0479D
C621	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C631	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C641	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C651	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C655	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C663	283-0775-00	XB041174		CAP.,FXD,MICA D:1764 PF,1%,500V	00853	D19-5F17640F0
C665	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C667	285-1067-00	XB041174		CAP.,FXD,PLSTC:0.5UF,1%,200V	14752	230B1C504F
C675	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
C685	283-0422-00	XB041174		CAP.,FXD,CER DI:0.047UF,+80-20%,50V	04222	DG015E473Z
CR213	152-0141-02	XB041174		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
CR523	152-0141-02	B010100	B041173X	SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
J302	-----			(FURNISHED AS A UNIT WITH 386-3370-01)		
J304	131-1780-00	B010100	B041173X	CONNECTOR,RECP,:RT-ANGLE HDR,2/25 MALE	22526	65483-005
L114	108-0317-00	XB041174		COIL,RF:FIXED,15UH	32159	71501M
L302	108-0317-00	B010100	B041173X	COIL,RF:FIXED,15UH	32159	71501M
Q125	151-0188-00	XB041174		TRANSISTOR:SILICON,PNP	04713	SPS6868K
Q135	151-0188-00	XB041174		TRANSISTOR:SILICON,PNP	04713	SPS6868K
Q511	151-0188-00	B010100	B041173X	TRANSISTOR:SILICON,PNP	04713	SPS6868K
Q515	151-0188-00	B010100	B041173X	TRANSISTOR:SILICON,PNP	04713	SPS6868K
R12	315-0472-00	B010100	B041173X	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R21	315-0220-00	B010100	B041173X	RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R23	321-0329-00	B010100	B041173X	RES.,FXD,FILM:26.1K OHM,1%,0.125W	91637	MFF1816G26101F
R25	315-0102-00	B010100	B041173X	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R26	315-0470-00	B010100	B041173X	RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
R27	315-0472-00	B010100	B041173X	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R41	315-0102-00	B010100	B041173X	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R55	315-0242-00	B010100	B041173X	RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
R101	321-0225-00	XB041174		RES.,FXD,FILM:2.15K OHM,1%,0.125W	91637	MFF1816G21500F
R102	321-0231-00	XB041174		RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
R103	321-0199-00	XB041174		RES.,FXD,FILM:1.15K OHM,1%,0.125W	91637	MFF1816G11500F
R105	321-0228-00	XB041174		RES.,FXD,FILM:2.32K OHM,1%,0.125W	91637	MFF1816G23200F
R106	321-0228-00	XB041174		RES.,FXD,FILM:2.32K OHM,1%,0.125W	91637	MFF1816G23200F
R108	315-0101-00	XB041174		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R110	315-0334-00	XB041174		RES.,FXD,CMPSN:330K OHM,5%,0.25W	01121	CB3345
R111	315-0472-00	B010100	B041173	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R111	315-0332-00	B041174		RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
R112	315-0821-00	XB041174		RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R113	315-0821-00	XB041174		RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R124	315-0100-00	XB041174		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
R125	315-0220-00	XB041174		RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R126	315-0681-00	XB041174		RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
R131	315-0102-00	XB041174		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R132	315-0221-00	XB041174		RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R134	315-0102-00	XB041174		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R135	315-0242-00	XB041174		RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
R136	315-0221-00	XB041174		RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R137	315-0100-00	XB041174		RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R138	315-0220-00	XB041174		RES., FXD, CMPSN: 22 OHM, 5%, 0.25W	01121	CB2205
R139	315-0100-00	XB041174		RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R141	321-0329-00	B010100	B041173	RES., FXD, FILM: 26.1K OHM, 1%, 0.125W	91637	MFF1816G26101F
R141	315-0302-00	B041174		RES., FXD, CMPSN: 3K OHM, 5%, 0.25W	01121	CB3025
R143	321-0412-00	B010100	B041173	RES., FXD, FILM: 191K OHM, 1%, 0.125W	91637	MFF1816G19102F
R143	315-0302-00	B041174		RES., FXD, CMPSN: 3K OHM, 5%, 0.25W	01121	CB3025
R154	315-0472-00	B010100	B041173X	RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R155	315-0242-00	B010100	B041173X	RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R211	315-0101-00	XB041174		RES., FXD, CMPSN: 100 OHM, 5%, 0.25W	01121	CB1015
R220	315-0100-00	XB041174		RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R235	315-0102-00	XB041174		RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R239	315-0102-00	XB041174		RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R255	315-0242-00	B010100	B041173X	RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R302	315-0821-00	B010100	B041173X	RES., FXD, CMPSN: 820 OHM, 5%, 0.25W	01121	CB8215
R305	315-0100-00	B010100	B041173X	RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R306	315-0821-00	B010100	B041173X	RES., FXD, CMPSN: 820 OHM, 5%, 0.25W	01121	CB8215
R329	315-0102-00	XB041174		RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R341	307-0383-00	XB041174		RES., FXD, FILM: 4.7K OHM, 2%, 1.5W	73138	899-1-R4.7K
R355	315-0242-00	B010100	B041173	RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R355	315-0472-00	B041174		RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R356	315-0472-00	XB041174		RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R357	315-0472-00	XB041174		RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R358	315-0242-00	XB041174		RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R367	315-0242-00	XB041174		RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R369	315-0242-00	XB041174		RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R370	315-0242-00	XB041174		RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R371	315-0242-00	XB041174		RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R372	315-0242-00	XB041174		RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R373	315-0242-00	XB041174		RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R374	315-0472-00	XB041174		RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R386	315-0681-00	XB041174		RES., FXD, CMPSN: 680 OHM, 5%, 0.25W	01121	CB6815
R405	315-0102-00	B010100	B041173X	RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R406	315-0100-00	B010100	B041173X	RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R411	315-0681-00	B010100	B041173X	RES., FXD, CMPSN: 680 OHM, 5%, 0.25W	01121	CB6815
R412	315-0221-00	B010100	B041173X	RES., FXD, CMPSN: 220 OHM, 5%, 0.25W	01121	CB2215
R413	315-0102-00	B010100	B041173X	RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R415	315-0302-00	B010100	B041173X	RES., FXD, CMPSN: 3K OHM, 5%, 0.25W	01121	CB3025
R416	315-0302-00	B010100	B041173X	RES., FXD, CMPSN: 3K OHM, 5%, 0.25W	01121	CB3025
R424	315-0472-00	B010100	B041173X	RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R425	307-0383-00	B010100	B041173X	RES., FXD, FILM: 4.7K OHM, 2%, 1.5W	73138	899-1-R4.7K
R426	315-0472-00	B010100	B041173X	RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R427	315-0472-00	B010100	B041173X	RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R429	315-0102-00	XB041174		RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R441	315-0472-00	B010100	B041173X	RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R455	315-0242-00	B010100	B041173X	RES., FXD, CMPSN: 2.4K OHM, 5%, 0.25W	01121	CB2425
R511	315-0100-00	B010100	B041173X	RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R512	315-0100-00	B010100	B041173X	RES., FXD, CMPSN: 10 OHM, 5%, 0.25W	01121	CB1005
R513	315-0332-00	B010100	B041173	RES., FXD, CMPSN: 3.3K OHM, 5%, 0.25W	01121	CB3325
R513	315-0472-00	B041174		RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R514	321-0225-00	B010100	B041173X	RES., FXD, FILM: 2.15K OHM, 1%, 0.125W	91637	MFF1816G21500F
R516	315-0221-00	B010100	B041173	RES., FXD, CMPSN: 220 OHM, 5%, 0.25W	01121	CB2215
R516	315-0472-00	B041174		RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R517	315-0102-00	B010100	B041173	RES., FXD, CMPSN: 1K OHM, 5%, 0.25W	01121	CB1025
R517	315-0472-00	B041174		RES., FXD, CMPSN: 4.7K OHM, 5%, 0.25W	01121	CB4725
R518	315-0220-00	B010100	B041173X	RES., FXD, CMPSN: 22 OHM, 5%, 0.25W	01121	CB2205
R519	315-0220-00	B010100	B041173X	RES., FXD, CMPSN: 22 OHM, 5%, 0.25W	01121	CB2205

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R521	315-0242-00	B010100	B041173X	RES.,FXD,CMPSPN:2.4K OHM,5%,0.25W	01121	CB2425
R535	315-0472-00	B010100	B041173X	RES.,FXD,CMPSPN:4.7K OHM,5%,0.25W	01121	CB4725
R545	315-0220-00	B010100	B041173X	RES.,FXD,CMPSPN:22 OHM,5%,0.25W	01121	CB2205
R555	315-0242-00	B010100	B041173X	RES.,FXD,CMPSPN:2.4K OHM,5%,0.25W	01121	CB2425
R556	315-0221-00	B010100	B041173X	RES.,FXD,CMPSPN:220 OHM,5%,0.25W	01121	CB2215
R557	315-0471-00	B010100	B041173X	RES.,FXD,CMPSPN:470 OHM,5%,0.25W	01121	CB4715
R558	301-0331-00	B010100	B041173X	RES.,FXD,CMPSPN:330 OHM,5%,0.50W	01121	EB3315
R563	321-0338-00	XB041174		RES.,FXD,FILM:32.4K OHM,1%,0.125W	91637	MFF1816G32401F
R584	315-0220-00	XB041174		RES.,FXD,CMPSPN:22 OHM,5%,0.25W	01121	CB2205
R601	321-0199-00	B010100	B041173X	RES.,FXD,FILM:1.15K OHM,1%,0.125W	91637	MFF1816G11500F
R602	315-0101-00	B010100	B041173X	RES.,FXD,CMPSPN:100 OHM,5%,0.25W	01121	CB1015
R603	315-0101-00	B010100	B041173X	RES.,FXD,CMPSPN:100 OHM,5%,0.25W	01121	CB1015
R604	315-0334-00	B010100	B041173X	RES.,FXD,CMPSPN:330K OHM,5%,0.25W	01121	CB3345
R605	321-0231-00	B010100	B041173X	RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
R607	321-0228-00	B010100	B041173X	RES.,FXD,FILM:2.32K OHM,1%,0.125W	91637	MFF1816G23200F
R608	321-0228-00	B010100	B041173X	RES.,FXD,FILM:2.32K OHM,1%,0.125W	91637	MFF1816G23200F
R619	315-0472-00	XB041174		RES.,FXD,CMPSPN:4.7K OHM,5%,0.25W	01121	CB4725
R663	315-0102-00	XB041174		RES.,FXD,CMPSPN:1K OHM,5%,0.25W	01121	CB1025
R669	321-0406-00	XB041174		RES.,FXD,FILM:165K OHM,1%,0.125W	91637	MFF1816G16502F
R677	315-0220-00	XB041174		RES.,FXD,CMPSPN:22 OHM,5%,0.25W	01121	CB2205
R684	315-0470-00	XB041174		RES.,FXD,CMPSPN:47 OHM,5%,0.25W	01121	CB4705
R685	315-0472-00	XB041174		RES.,FXD,CMPSPN:4.7K OHM,5%,0.25W	01121	CB4725
R686	315-0472-00	XB041174		RES.,FXD,CMPSPN:4.7K OHM,5%,0.25W	01121	CB4725
U1	156-0600-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U5	156-0382-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U11	156-0385-00	B010100	B041173X	MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
U15	156-0626-00	B010100	B041173X	MICROCIRCUIT,DI:DUAL DECADE CNTR	01295	SN74390N
U16	156-0391-00	XB040693		MICROCIRCUIT,DI:HEX LATCH WITH CLEAR	04713	74LS174(N OR J)
U21	156-0487-00	B010100	B041173X	MICROCIRCUIT,DI:DUAL RETRIG,ONE SHOT	80009	156-0487-00
U25	156-0382-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U31	156-0382-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U35	156-0383-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-00
U41	156-0385-00	B010100	B041173X	MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
U45	156-0388-00	B010100	B041173X	MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	80009	156-0388-00
U55	156-0777-00	B010100	B039999	MICROCIRCUIT,DI:ROM 1K X 8 STATIC MASK	80009	156-0777-00
U55	156-0777-01	B040000	B040692	MICROCIRCUIT,DI:ROM CUSTOM MASK	80009	156-0777-01
U55	156-0777-02	B040693	B041173X	MICROCIRCUIT,DI:1024 X 8 PROM,PROGRAMMED	80009	156-0777-02
U101	156-0600-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U105	156-0480-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
U111	156-0383-00	B010100	B041173	MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-00
U111	156-0067-00	B041174		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
U115	156-0763-00	B010100	B041173X	MICROCIRCUIT,DI:HEX CONT BOUNCE ELIMINATOR	80009	156-0763-00
U121	156-0480-00	B010100	B041173	MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
U121	156-0323-00	B041174		MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U125	156-0651-00	B010100	B041173	MICROCIRCUIT,DI:8-BIT PRL-OUT,SER SHF RGTR	01295	SN74LS164N
U125	156-0171-00	B041174		MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	80009	156-0171-00
U126	156-0480-00	XB040693	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
U131	156-0146-00	B010100	B041173	MICROCIRCUIT,DI:8-BIT SHIFT REGISTER	01295	SN74165N
U131	156-0403-00	B041174		MICROCIRCUIT,DI:HEX. INV W/OPEN COLL OUTPS	80009	156-0403-00
U135	156-0382-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U141	156-0487-00	B010100	B041173X	MICROCIRCUIT,DI:DUAL RETRIG,ONE SHOT	80009	156-0487-00
U151	156-0695-00	B010100	B041173X	MICROCIRCUIT,DI:ROM,256 X 4 STATIC	18324	2606-1B
U155	156-0778-00	B010100	B019999	MICROCIRCUIT,DI:ROM,1K X 8 STATIC MASK	80009	156-0778-00
U155	156-0778-01	B020000	B039999	MICROCIRCUIT,DI:ROM,1024 X 8 CUSTOM MASK	80009	156-0778-01
U155	156-0778-02	B040000	B041173X	MICROCIRCUIT,DI:ROM CUSTOM MASK (U155 AND C55 INSTALLED AS A PAIR)	80009	156-0778-02
U201	156-0600-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U205	156-0852-00	B010100	B041173	MICROCIRCUIT,DI:HEX BUS DRIVER W/3-STATE	01295	SN74LS367 N OR J
U205	156-0382-00	B041174		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U211	156-0479-00	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N
U215	156-0480-00	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
U221	156-0385-00	XB041174		MICROCIRCUIT,DI:HEX. INVERTER	80009	156-0385-00
U225	156-0382-00	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U231	156-0387-00	XB041174		MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG	80009	156-0387-00
U235	156-0617-00	XB041174		MICROCIRCUIT,DI:DUAL 4 BIT BIN COUNTER	01295	SN74393N
U251	156-0695-00	B010100	B041173X	MICROCIRCUIT,DI:ROM,256 X 4 STATIC	18324	2606-1B
U253	156-0695-00	B010100	B041173X	MICROCIRCUIT,DI:ROM,256 X 4 STATIC	18324	2606-1B
U255	156-0779-00	B010100	B019999	MICROCIRCUIT,DI:ROM,1K X 8 STATIC	80009	156-0779-00
U255	156-0779-01	B020000	B041173	MICROCIRCUIT,DI:ROM,1024 X 8 CUSTOM MASK	80009	156-0779-01
U255	156-0426-00	B041174		MICROCIRCUIT,DI:MICROPROCESSOR	04713	MC6800S
U261	156-0531-00	XB041174		MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR	27014	DM8833N
U265	156-0531-00	XB041174		MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR	27014	DM8833N
U271	156-1028-00	XB041174		MICROCIRCUIT,DI:1024 X 4 STATIC RAM	34649	2114
U275	156-1028-00	XB041174		MICROCIRCUIT,DI:1024 X 4 STATIC RAM	34649	2114
U285	156-0480-00	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
U301	156-0600-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U305	156-0852-00	B010100	B041173X	MICROCIRCUIT,DI:HEX BUS DRIVER W/3-STATE	01295	SN74LS367 N OR J
U311	156-0600-00	XB041174		MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U315	156-0427-00	B010100	B041173	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U315	156-0600-00	B041174		MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U321	156-0427-00	B010100	B041173	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U321	156-0852-00	B041174		MICROCIRCUIT,DI:HEX BUS DRIVER W/3-STATE	01295	SN74LS367 N OR J
U325	156-0383-00	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-00
U331	156-0427-00	B010100	B041173	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U331	156-0480-00	B041174		MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
U335	156-0058-01	XB041174		MICROCIRCUIT,DI:HEX INVERTER	80009	156-0058-01
U341	156-0427-00	B010100	B041173X	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U355	156-0780-00	B010100	B019999	MICROCIRCUIT,DI:ROM,1K X 8 CUSTOM MASK	80009	156-0780-00
U355	156-0780-01	B020000	B039999	MICROCIRCUIT,DI:ROM,1024 X 8 CUSTOM MASK	80009	156-0780-01
U355	156-0780-02	B040000	B041173X	MICROCIRCUIT,DI:ROM CUSTOM MASK	80009	156-0780-02
U365	156-0469-00	XB041174		MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U375	156-0383-00	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-00
U385	156-0479-00	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N
U405	156-0323-00	B010100	B041173X	MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U411	156-0171-00	B010100	B041173	MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	80009	156-0171-00
U411	156-0600-00	B041174		MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U415	156-0403-00	B010100	B041173	MICROCIRCUIT,DI:HEX. INV W/OPEN COLL OUTPS	80009	156-0403-00
U415	156-0600-00	B041174		MICROCIRCUIT,DI:QUAD BUS XCVR	80009	156-0600-00
U421	156-0852-00	XB041174		MICROCIRCUIT,DI:HEX BUS DRIVER W/3-STATE	01295	SN74LS367 N OR J
U425	156-0651-00	XB041174		MICROCIRCUIT,DI:8-BIT PRL-OUT,SER SHF RGTR	01295	SN74LS164N
U431	156-0469-00	B010100	B041173	MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U431	156-0146-01	B041174		MICROCIRCUIT,DI:8-BIT PAR-IN SER OUT SR	80009	156-0146-01
U441	156-0385-00	B010100	B041173X	MICROCIRCUIT,DI:HEX. INVERTER	80009	156-0385-00
U445	156-0382-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U451	156-0695-00	B010100	B041173	MICROCIRCUIT,DI:ROM,256 X 4 STATIC	18324	2606-1B
U451	156-0777-02	B041174		MICROCIRCUIT,DI:1024 X 8 PROM,PROGRAMMED	80009	156-0777-02
U453	156-0695-00	B010100	B041173X	MICROCIRCUIT,DI:ROM,256 X 4 STATIC	18324	2606-1B
U455	156-0781-00	B010100	B019999	MICROCIRCUIT,DI:ROM,1K X 8 CUSTOM MASK	80009	156-0781-00
U455	156-0781-01	B020000	B041173	MICROCIRCUIT,DI:ROM,1024 X 8 CUSTOM MASK	80009	156-0781-01
U455	156-0778-02	B041174		MICROCIRCUIT,DI:ROM CUSTOM MASK	80009	156-0778-02
U465	156-0779-00	XB041174		MICROCIRCUIT,DI:ROM,1K X 8 STATIC	80009	156-0779-00
U475	156-0780-02	XB041174		MICROCIRCUIT,DI:ROM CUSTOM MASK	80009	156-0780-02
U485	156-0781-00	XB041174		MICROCIRCUIT,DI:ROM,1K X 8 CUSTOM MASK	80009	156-0781-00
U495	156-0782-02	XB041174		MICROCIRCUIT,DI:ROM CUSTOM MASK	80009	156-0782-02

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U501	156-0617-00	B010100	B041173X	MICROCIRCUIT,DI:DUAL 4 BIT BIN COUNTER	01295	SN74393N
U505	156-0387-00	B010100	B041173	MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG	80009	156-0387-00
U505	156-0383-01	B041174		MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-01
U511	156-0067-00	B010100	B041173	MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
U515	156-0383-01	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-01
U521	156-0426-00	B010100	B041173	MICROCIRCUIT,DI:MICROPROCESSOR	04713	MC6800S
U525	156-0058-00	B010100	B041173X	MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U531	156-0531-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR	27014	DM8833N
U535	156-0531-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR	27014	DM8833N
U541	156-0383-00	B010100	B041173X	MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-00
R545	156-0541-00	B010100	B041173X	MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	27014	DM74LS139N
R551	156-0695-00	B010100	B041173X	MICROCIRCUIT,DI:ROM,256 X 4 STATIC	18324	2606-1B
U555	156-0782-00	B010100	B019999	MICROCIRCUIT,DI:ROM,1K X 8 CUSTOM MASK	80009	156-0782-00
U555	156-0782-01	B020000	B039999	MICROCIRCUIT,DI:ROM,1024 X 8 CUSTOM MASK	80009	156-0782-01
U555	156-0782-02	B040000	B041173	MICROCIRCUIT,DI:ROM CUSTOM MASK	80009	156-0782-02
U555	156-0385-01	B041174		MICROCIRCUIT,DI:HEX. INVERTER	80009	156-0385-01
U555	156-0708-06	B010100	B041173X	MICROCIRCUIT,DI:PROM,PROGRAMMED (OPTION 37, 670-4887-00 ONLY)	80009	156-0708-06
U561	156-0706-01	XB041174		MICROCIRCUIT,DI:DUAL MONOSTABLE MV,CHK	80009	156-0706-01
U565	156-0480-01	XB041174		MICROCIRCUIT,DI:QUAD 2-INP AND GATE,CHK	80009	156-0480-01
U575	156-0382-01	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	80009	156-0382-01
U581	156-0383-01	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-01
U611	156-0763-01	XB041174		MICROCIRCUIT,DI:HEX CONT BOUNCE ELIM,CHK	80009	156-0763-01
U615	156-0391-01	XB041174		MICROCIRCUIT,DI:HEX. LATCH WITH CLEAR	80009	156-0391-01
U621	156-0427-01	XB041174		MICROCIRCUIT,DI:PERIPHERAL INTFC ADPTR,CHK	80009	156-0427-01
U631	156-0427-00	XB041174		MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U641	156-0427-00	XB041174		MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U651	156-0427-00	XB041174		MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U655	156-0382-01	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	80009	156-0382-01
U661	156-0388-01	XB041174		MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	80009	156-0388-01
U665	156-0487-00	XB041174		MICROCIRCUIT,DI:DUAL RETRIG,ONE SHOT	80009	156-0487-00
U675	156-0382-01	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	80009	156-0382-01
U681	156-0626-00	XB041174		MICROCIRCUIT,DI:DUAL DECADE CNTR	01295	SN74390N
U685	156-0382-01	XB041174		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	80009	156-0382-01
VR104	152-0662-00	XB041174		SEMICONV DEVICE:ZENER,0.4W,5V,1%	04713	SZG195
VR557	152-0175-00	B010100	B041173X	SEMICONV DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008
VR601	152-0662-00	B010100	B041173X	SEMICONV DEVICE:ZENER,0.4W,5V,1%	04713	SZG195
Y302	158-0072-00			XTAL UNIT,QTZ:4.9152 MHZ,0.05%	33096	OBD
A7	670-4513-00	B010100	B041117	CKT BOARD ASSY:MOTOR FILTER	80009	670-4513-00
A7	670-4513-01	B041118		CKT BOARD ASSY:MOTOR FILTER	80009	670-4513-01
C21	283-0022-00			CAP.,FXD,CER DI:0.02UF,1400VDCAC	91418	AU203-2142-1R0
C50	283-0059-00			CAP.,FXD,CER DI:1UF,+80-20%,50V	72982	8131N031Z5U0105Z
C51	283-0059-00	B010100	B041117X	CAP.,FXD,CER DI:1UF,+80-20%,50V	72982	8131N031Z5U0105Z
C91	283-0059-00	B010100	B041117	CAP.,FXD,CER DI:1UF,+80-20%,50V	72982	8131N031Z5U0105Z
C91	283-0110-00	B041118		CAP.,FXD,CER DI:0.005UF,+80-20%,150V	56289	19C242B
L35	120-1050-00			TRANSFORMER,RF:TOROID,2 WINDINGS	80009	120-1050-00
L75	120-1050-00			TRANSFORMER,RF:TOROID,2 WINDINGS	80009	120-1050-00

REPLACEABLE ELECTRICAL PARTS

Ckt No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
CHASSIS PARTS					
B1001	147-0008-00	B010100 B041451	MOTOR, AC: SHADED P, 3200RMM, 115V, 60HZ	05624	AYAA-13080
B1001	147-0008-02	B041452	MOTOR, AC: W/LEADS, CONNECTORS & HOUSING	80009	147-0008-02
F1001	159-0019-00		FUSE, CARTRIDGE: 3AG, 1A, 250V, SLOW BLOW (FOR 110-120VAC OPERATION)	71400	MDL1
F1001	159-0043-00		FUSE, CARTRIDGE: 3AG, 0.6A, 250V, SLOW-BLOW (OPTION A1, A2, A3, A4)	71400	MDL 6/10
M1015	147-0044-00		MOTOR, DC: 2V/1000 RPM, 12V, W/TACH OUT	98938	MT9413B
Q1002	151-0464-00		TRANSISTOR: SILICON, NPN	04713	SJE412
Q1004	151-0491-00		TRANSISTOR: SILICON, NPN	80009	151-0491-00
Q1006	151-0462-00		TRANSISTOR: SILICON, PNP	04713	TIP30C
Q1010	151-0465-00		TRANSISTOR: SILICON, PNP	80009	151-0465-00
Q1011	151-0606-00		TRANSISTOR: SILICON, NPN	04713	SJE375
Q1013	151-0607-00		TRANSISTOR: SILICON, PNP	04713	SJE376
S1000	260-1583-00	B010100 B041603	SWITCH, PUSH: DPST, 6A, 125VAC	10389	27-900-078
S1000	260-1842-00	B041604	SWITCH, ROCKER: DPST, 16A, 250VAC	04009	2600-11E 718
T1001	120-1017-00		XFMR, PWR, STPDN:	80009	120-1017-00
T1017	120-1017-00		XFMR, PWR, STPDN:	80009	120-1017-00

BLOCK AND INTERCONNECTION DIAGRAMS

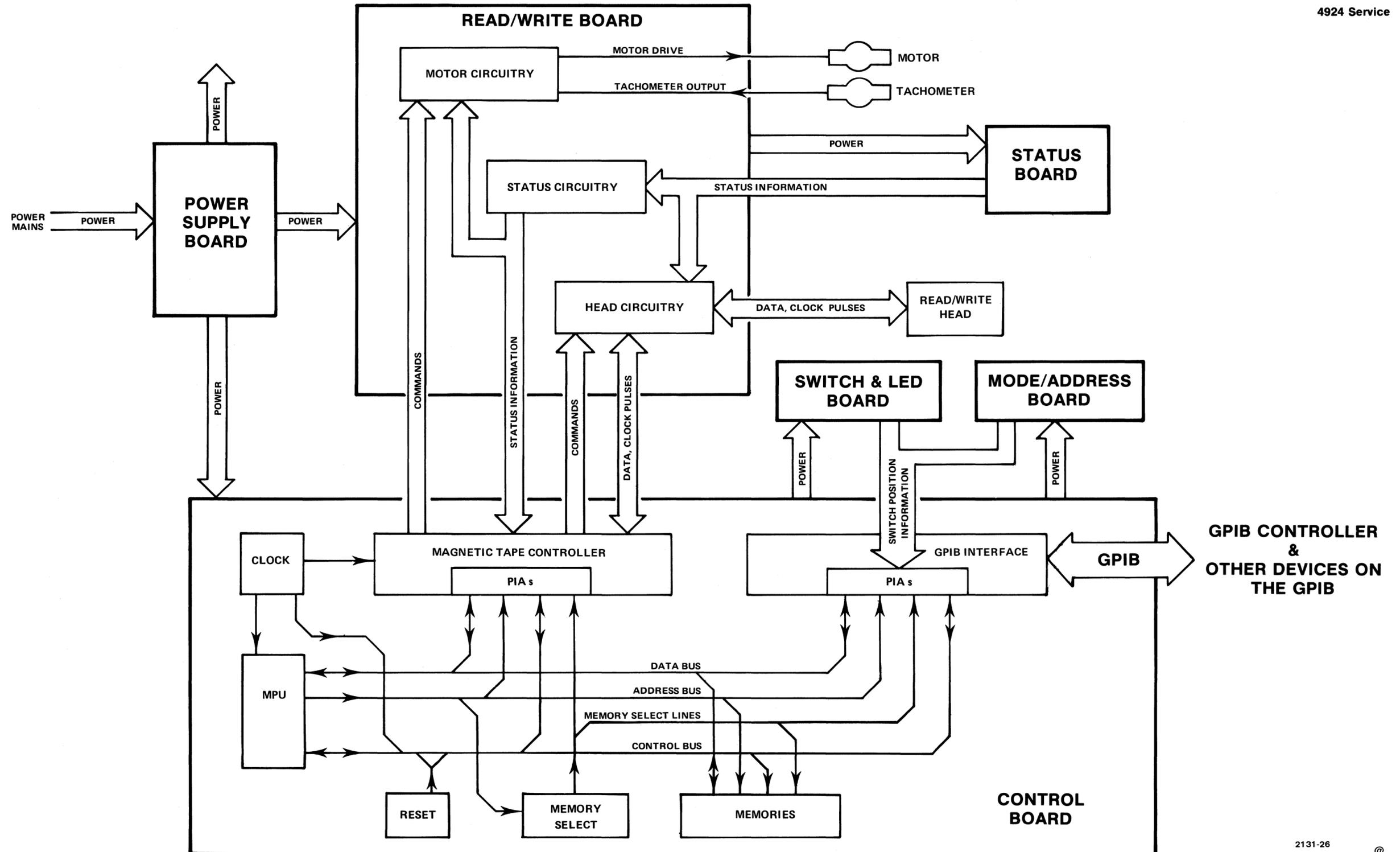


Fig. 8-1. 4924 Block Diagram.

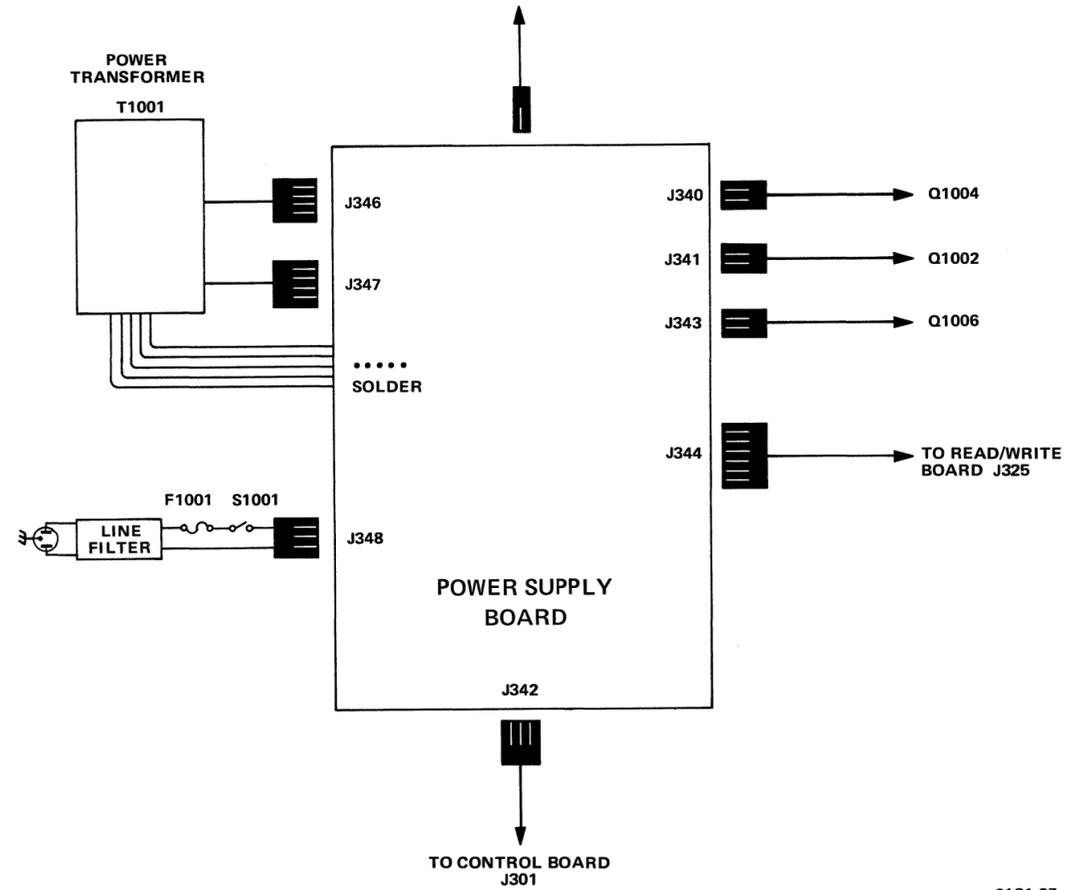


Fig. 8-2. Power Supply Board Interconnection Diagram.

2131-27

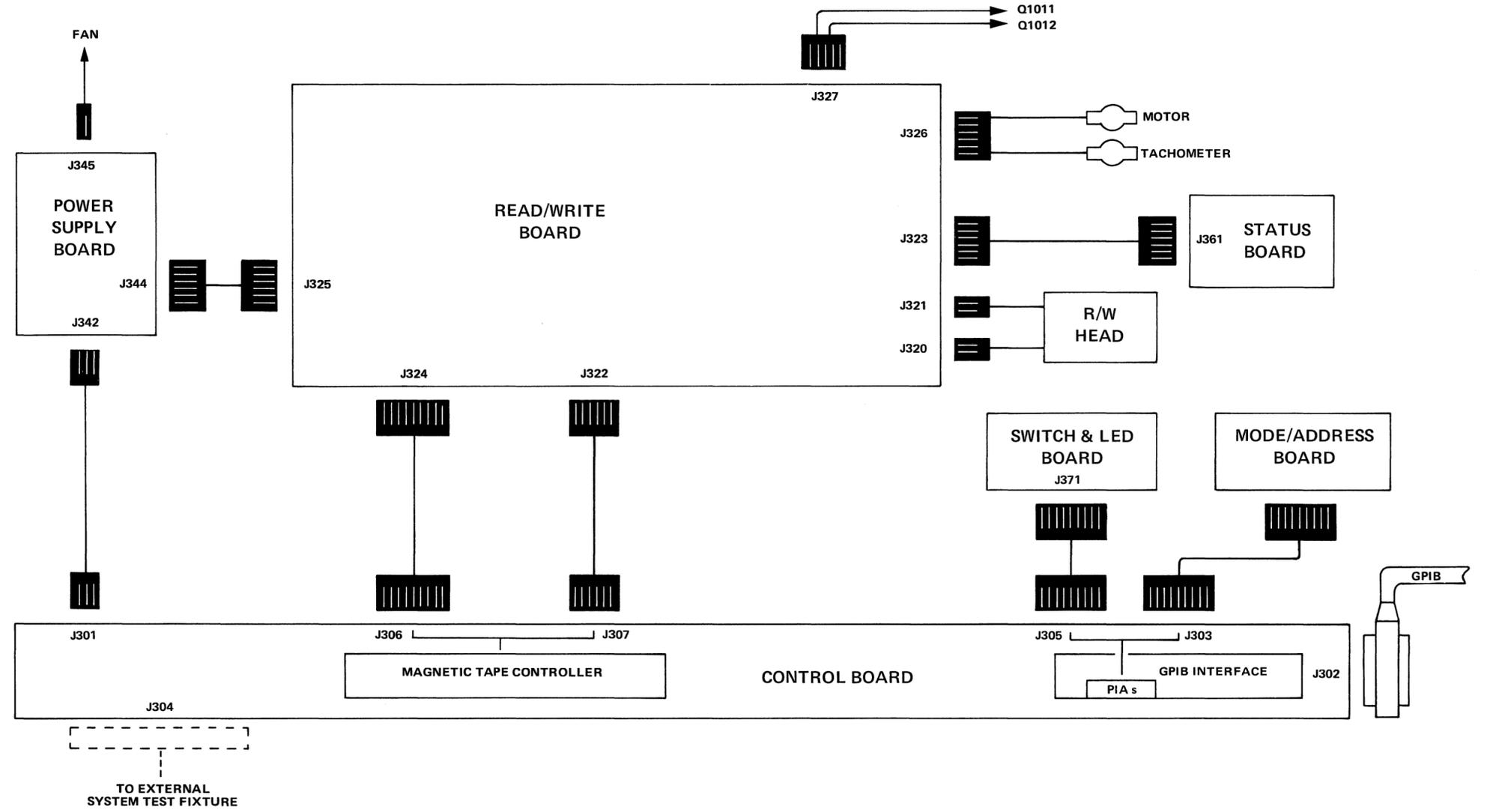


Fig. 8-3. 4924 Interconnection Diagram.

2131-28

DIAGRAMS

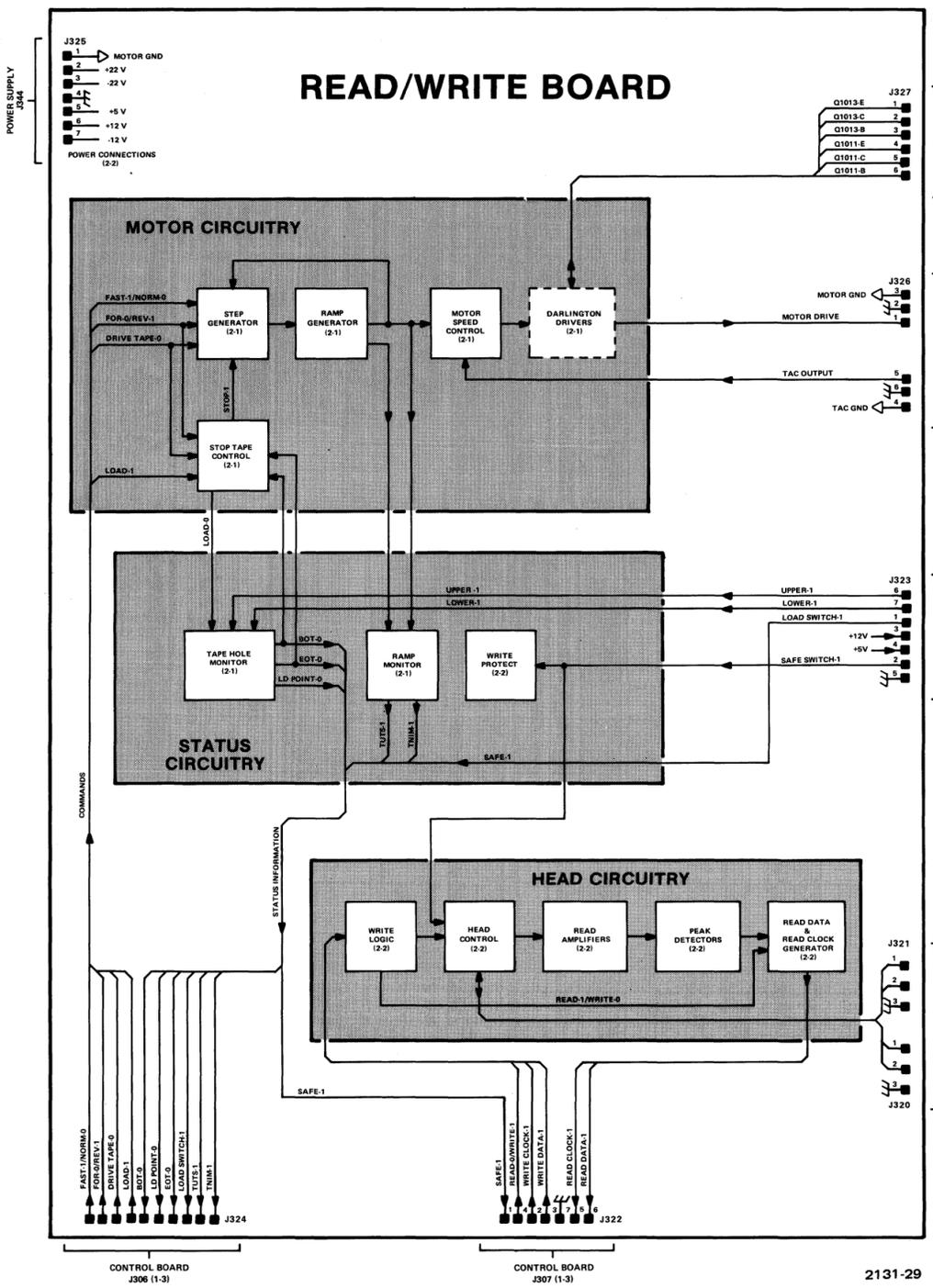
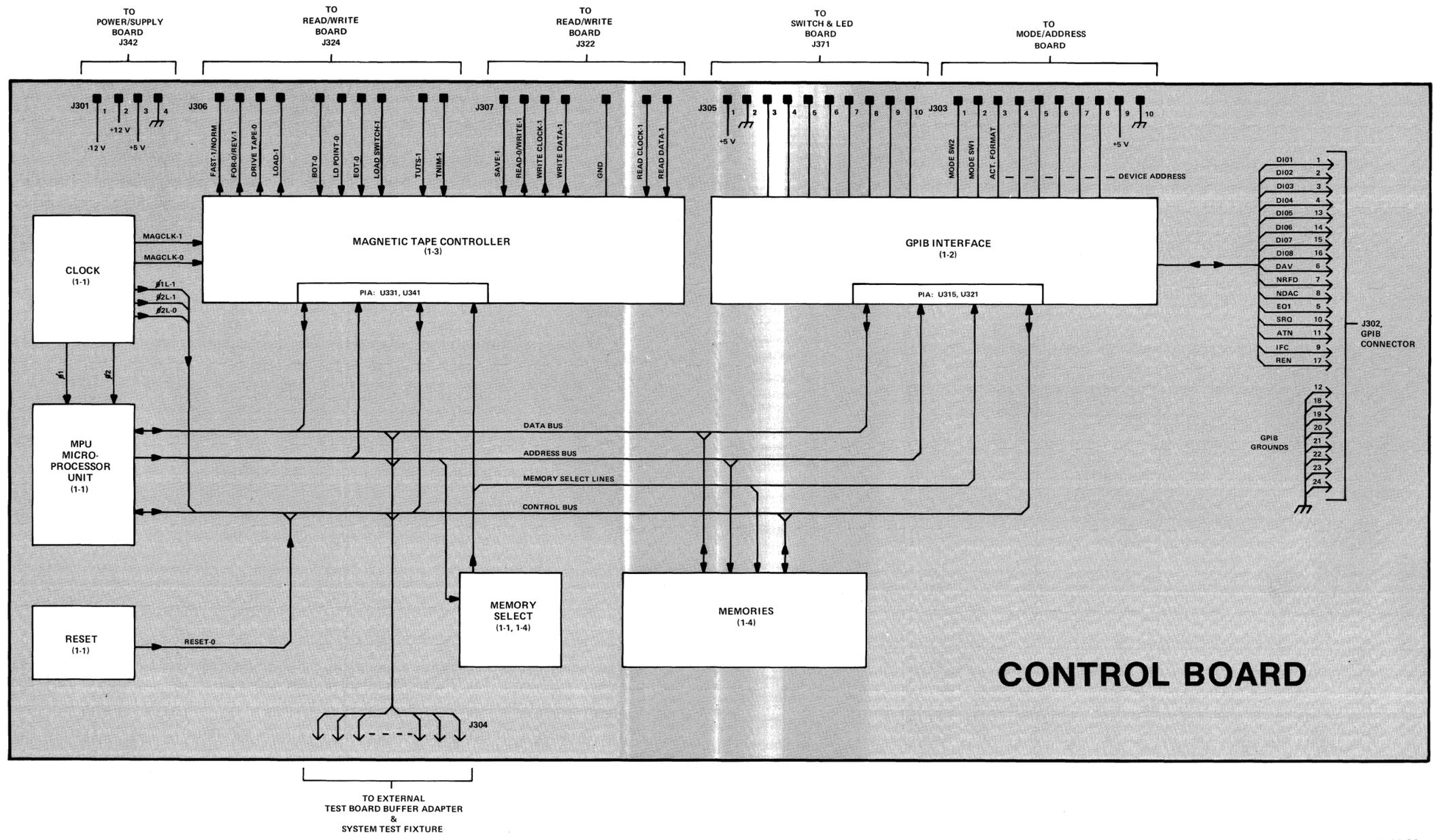


Fig. 8-4. Read/Write Board Block and Interconnection Diagram.



NOTE: Numbers in parentheses, such as "(2-2)" denote the schematic pages on which the particular circuit blocks are shown.

Fig. 8-5. Control Board Block and Interconnection Diagram.

BLOCK DIAGRAMS

Section 9 DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

4924 Service

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

- Capacitors = Values one or greater are in picofarads (pF).
 Values less than one are in microfarads (μ F).
 Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

Abbreviations are based on ANSI Y1.1-1972.

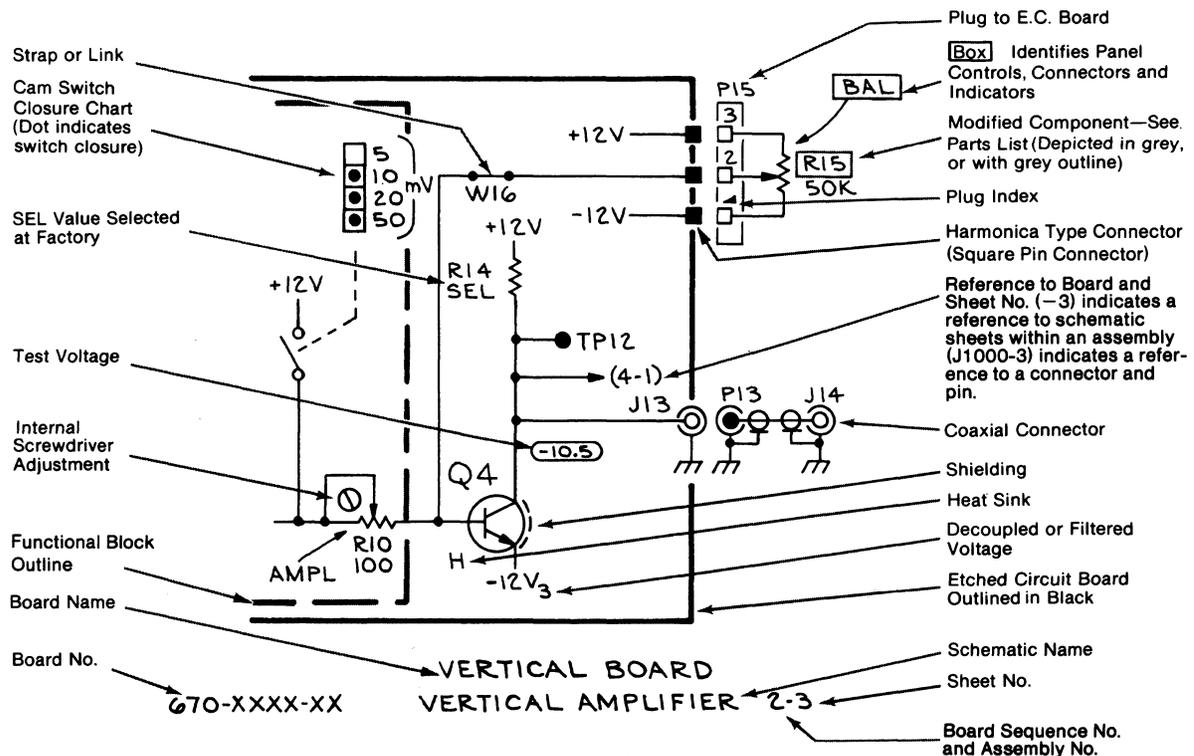
Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

- Y14.15, 1966 Drafting Practices.
- Y14.2, 1973 Line Conventions and Lettering.
- Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc)	H	Heat dissipating device (heat sink, heat radiator, etc)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:



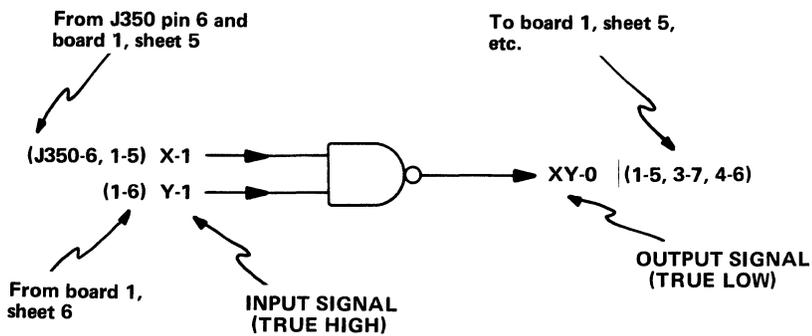
1. TRUE HIGH and TRUE LOW Signals

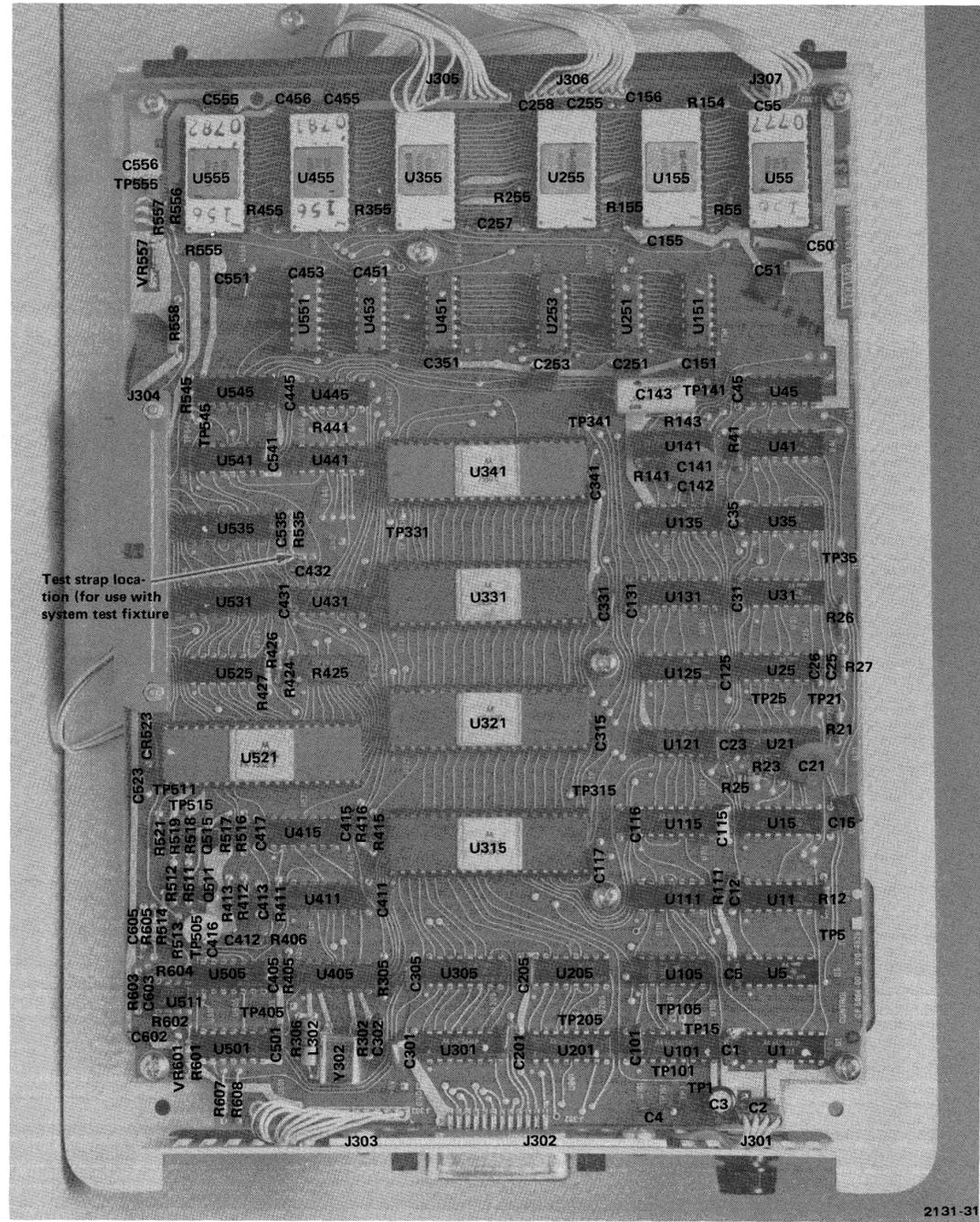
Signal names on the schematics are followed by -1 or -0. A TRUE HIGH signal is indicated by -1, and a TRUE LOW signal is indicated by -0.

SIGNAL-1 = TRUE HIGH
 SIGNAL-0 = TRUE LOW

2. Cross-References

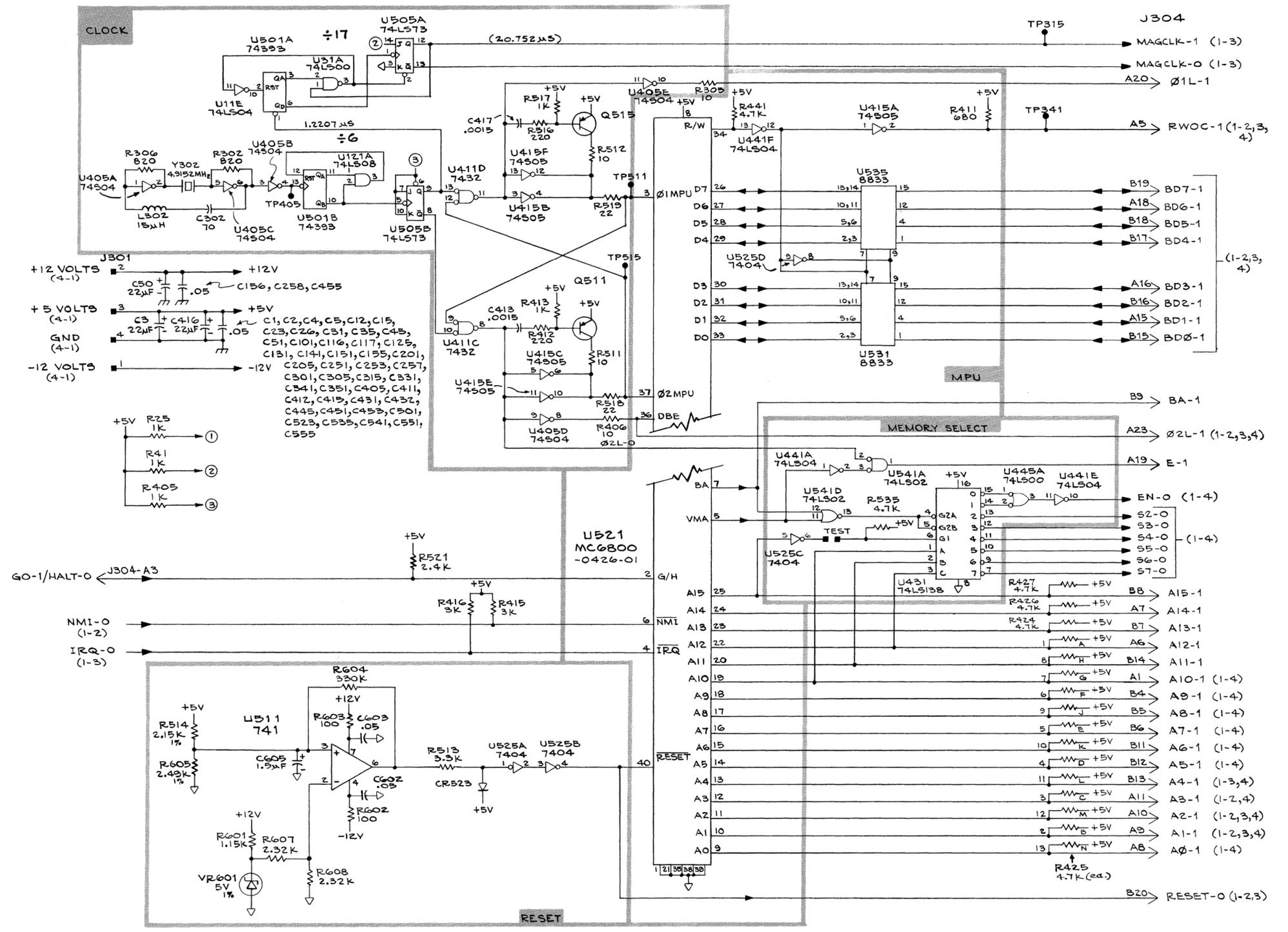
Schematic cross-references (from/to information) are included on the schematics. The "from" reference only indicates the signal "source," and the "to" reference lists all loads where the signal is used. All from/to information will be enclosed in parentheses.

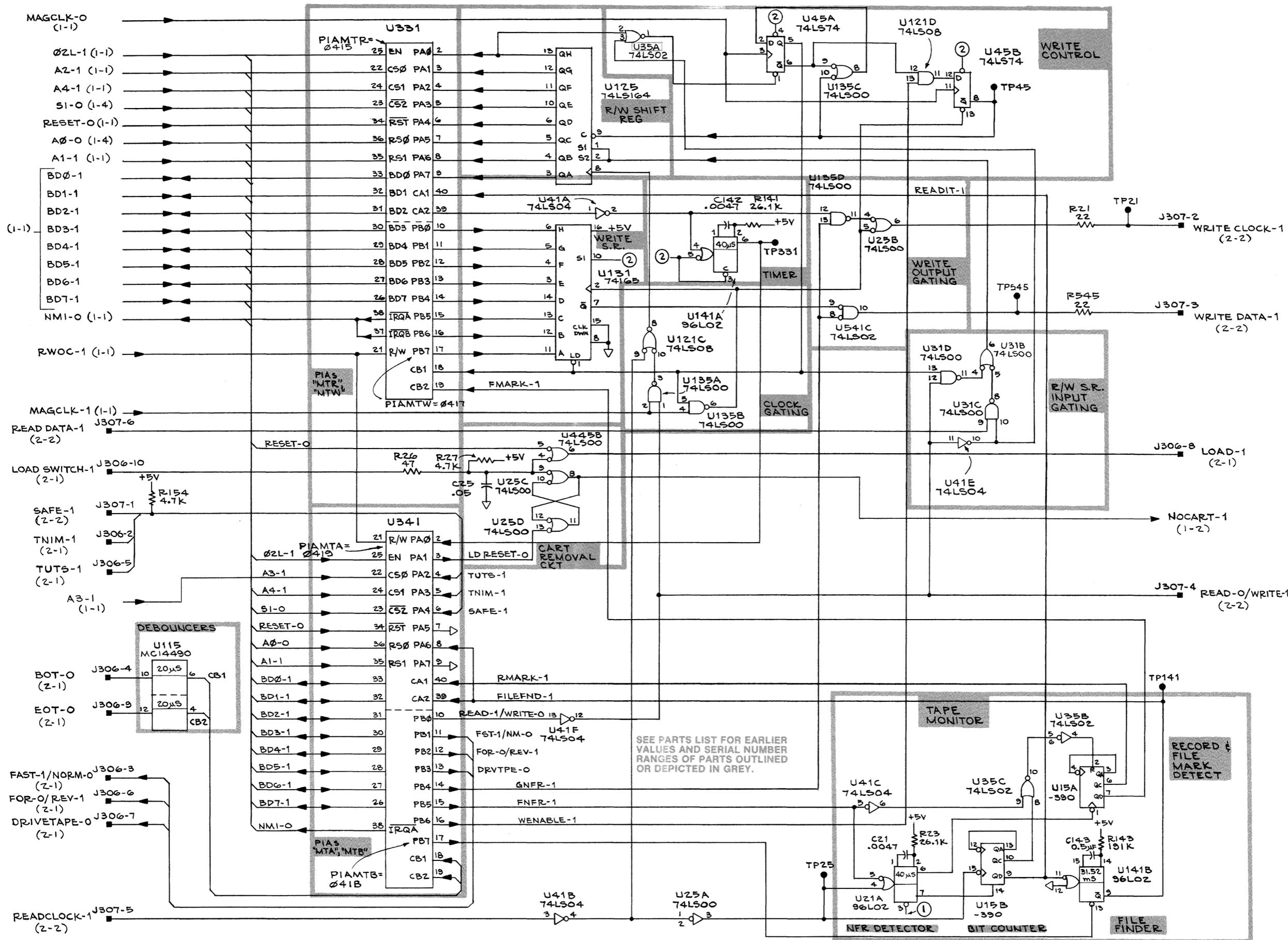


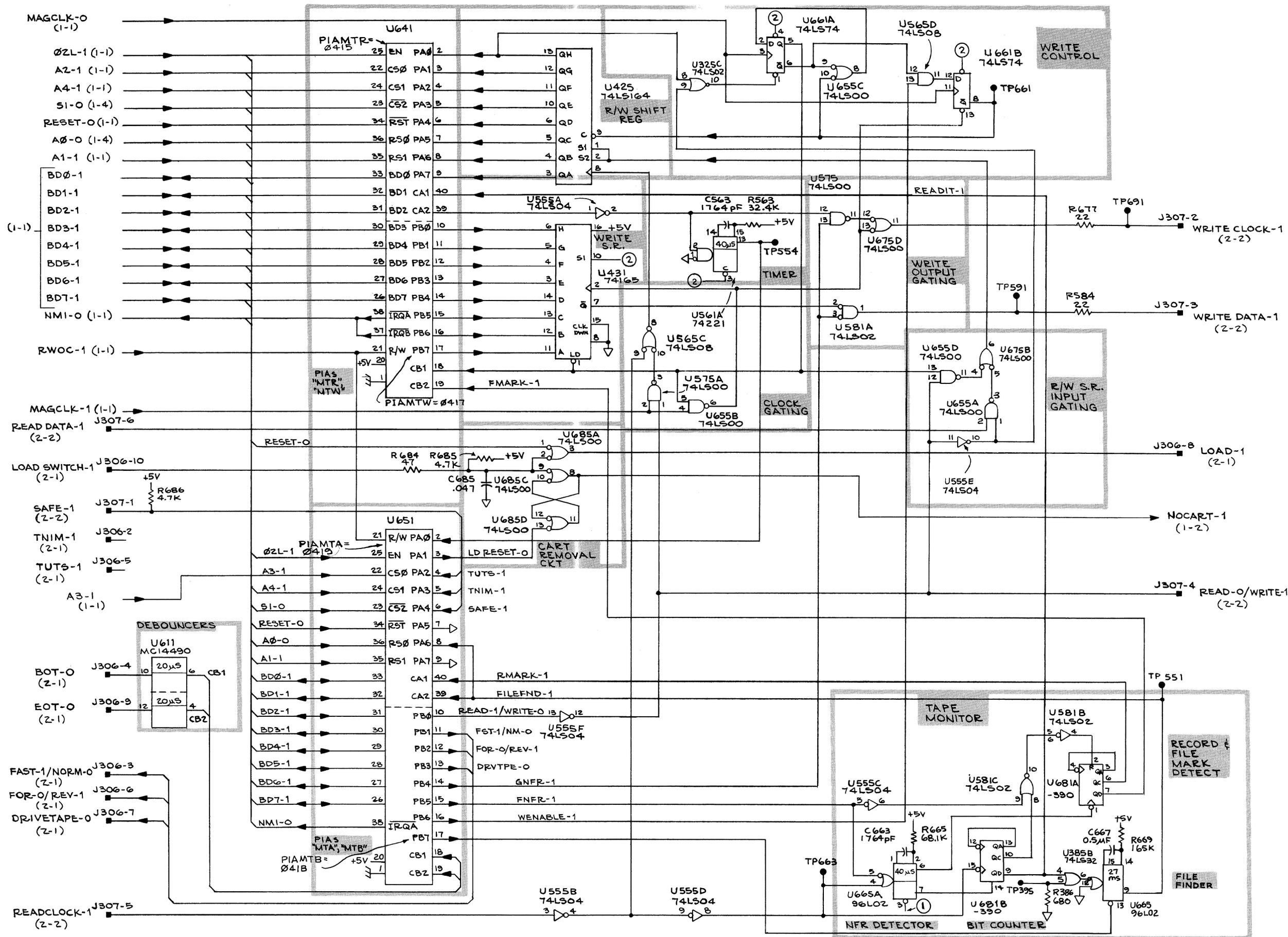


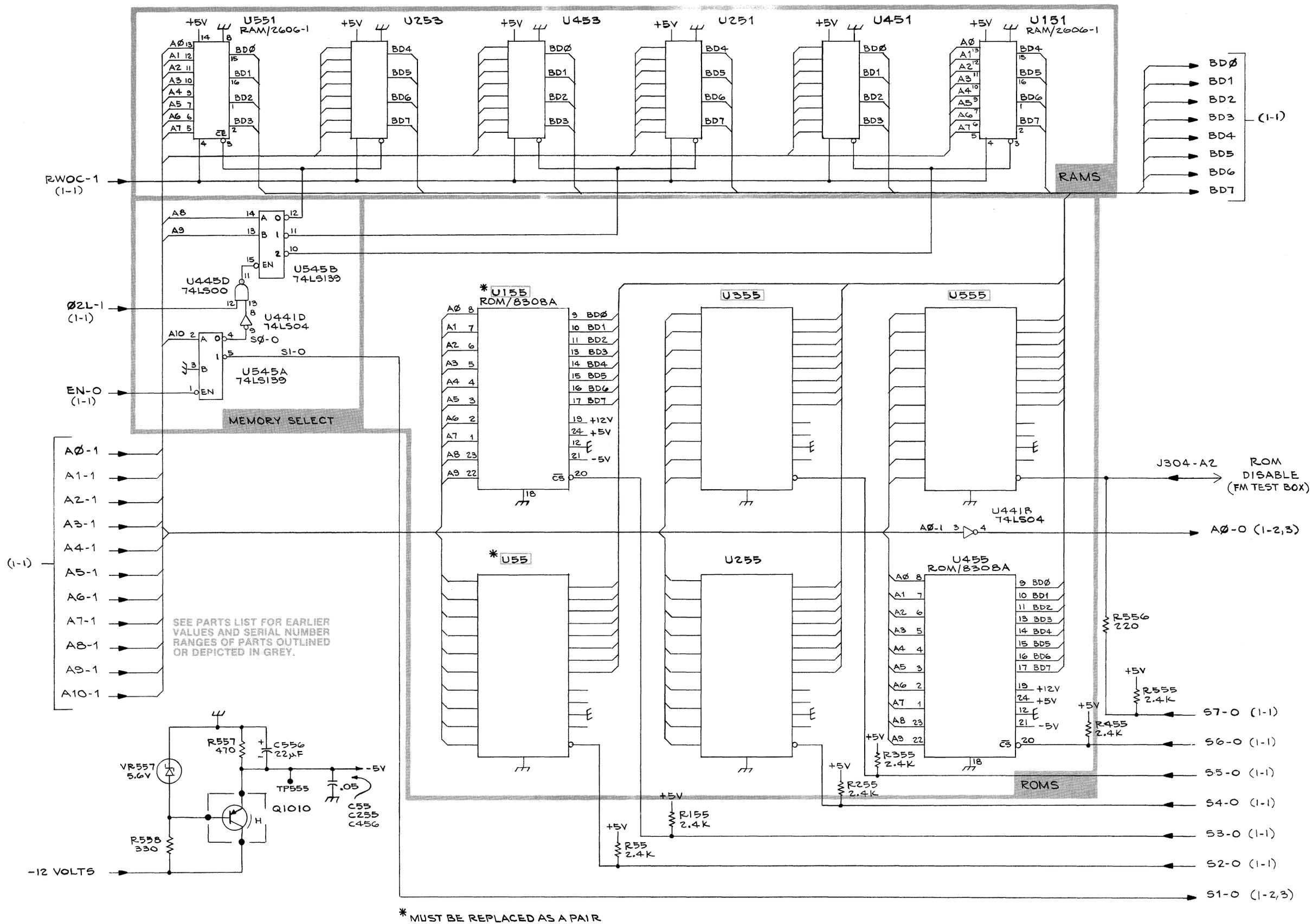
Control Board component locations

2131-31

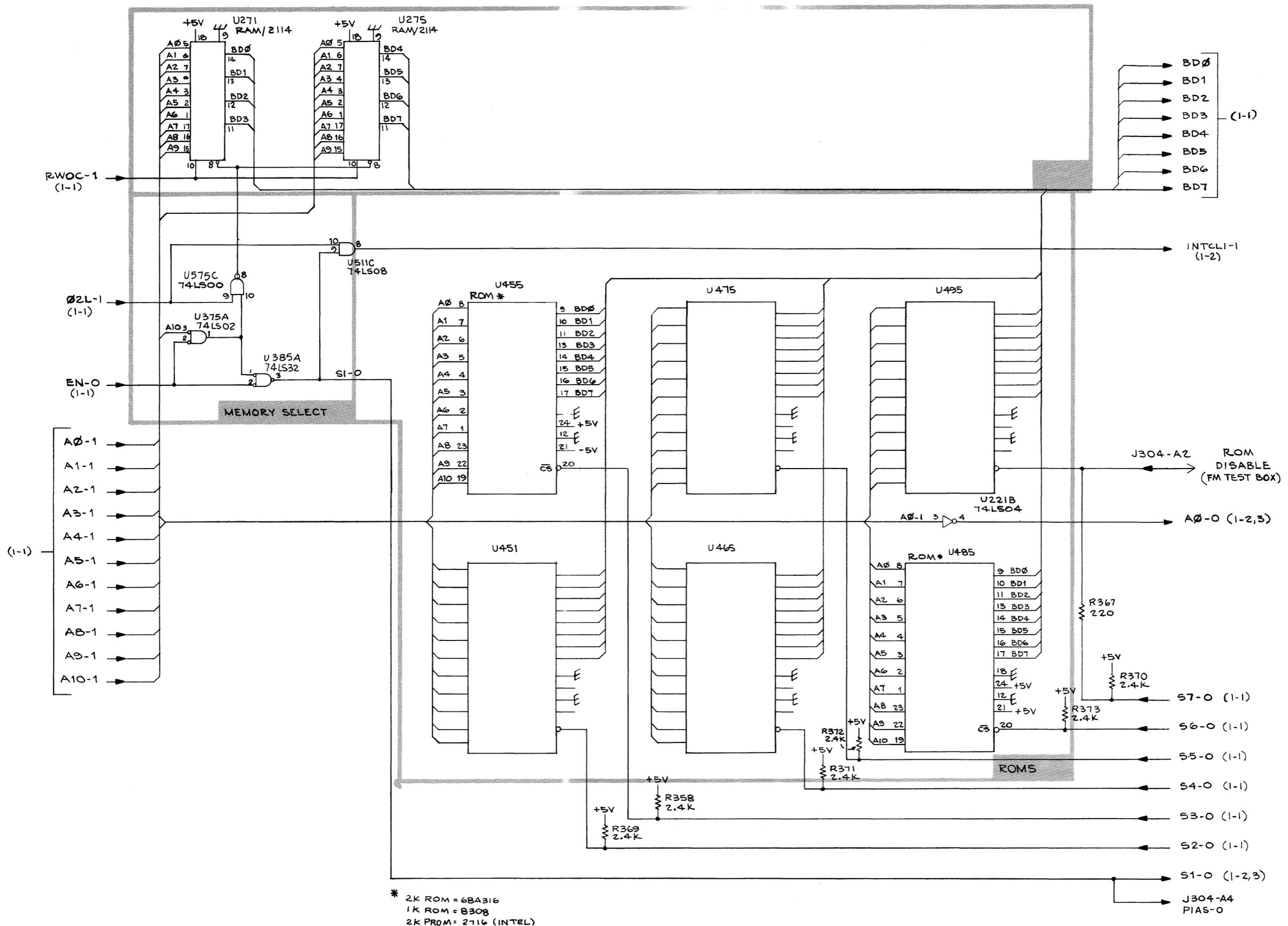


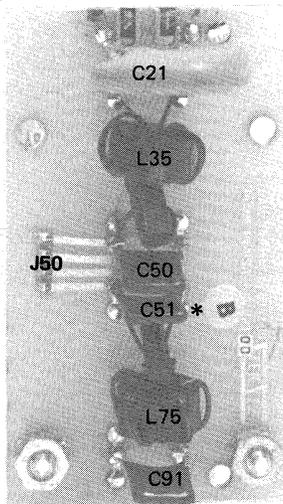






* MUST BE REPLACED AS A PAIR





***See Parts List for
serial number ranges.**

1909-79A

Fig. 7-3. Motor Filter board component locations.

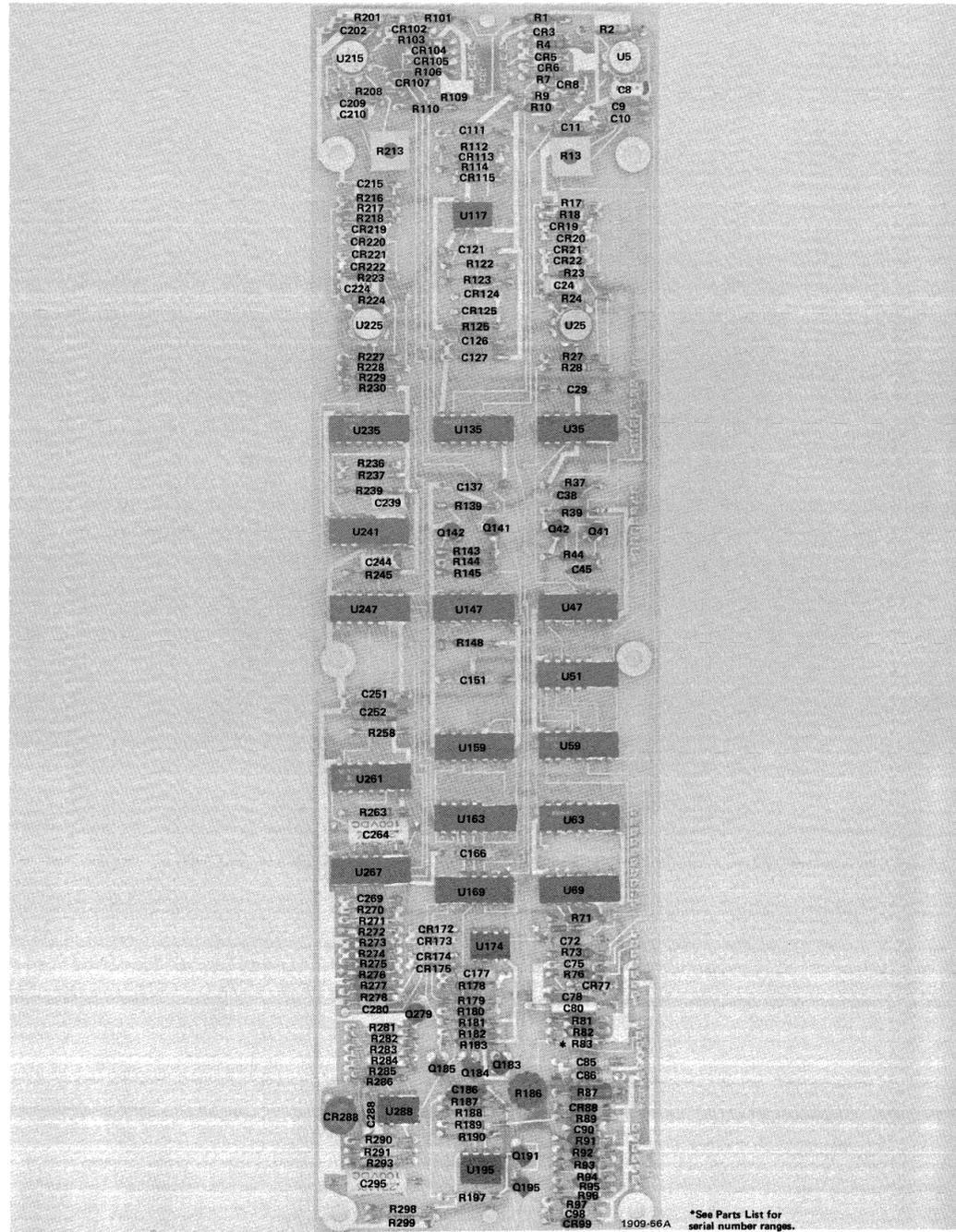
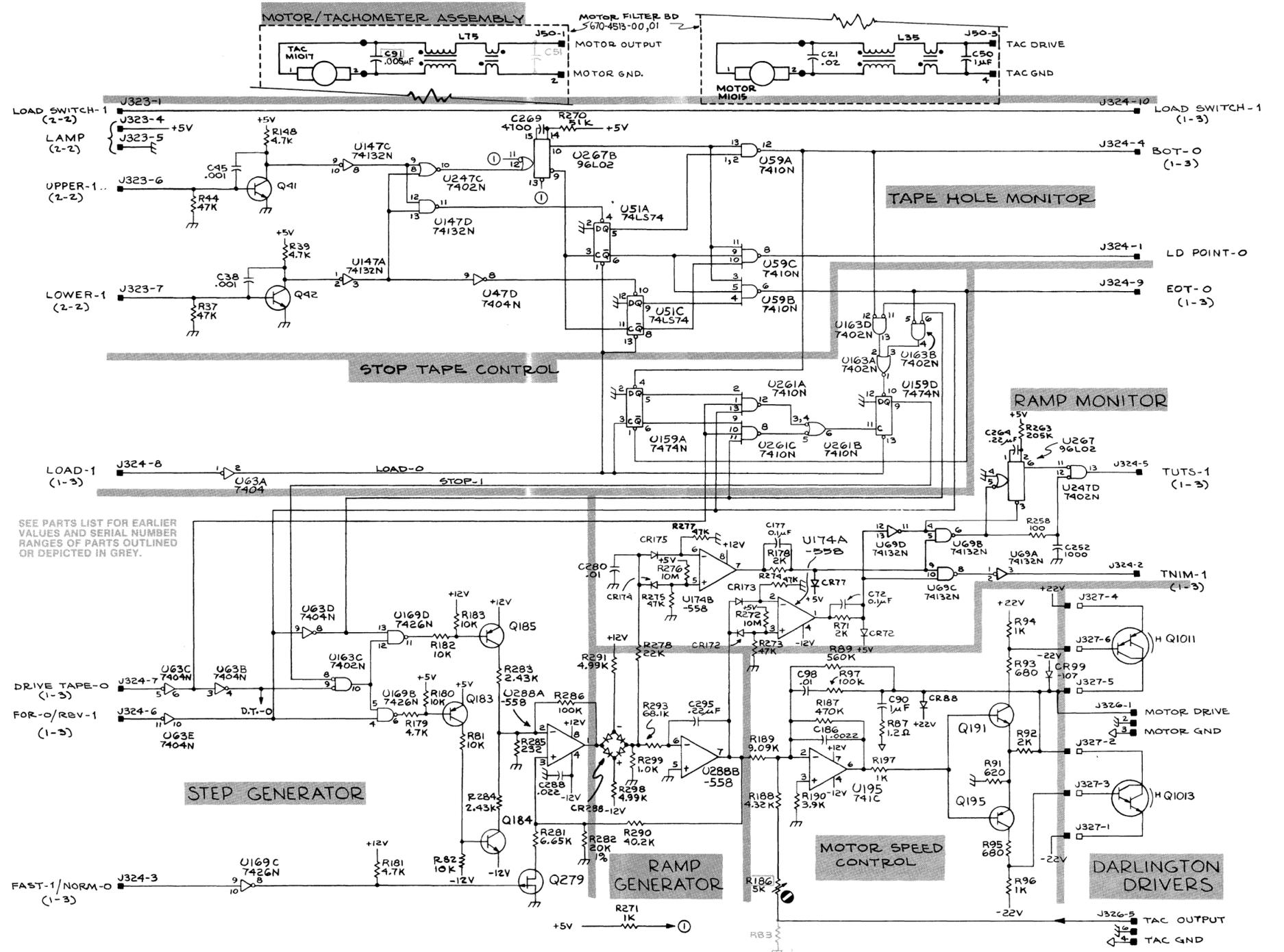


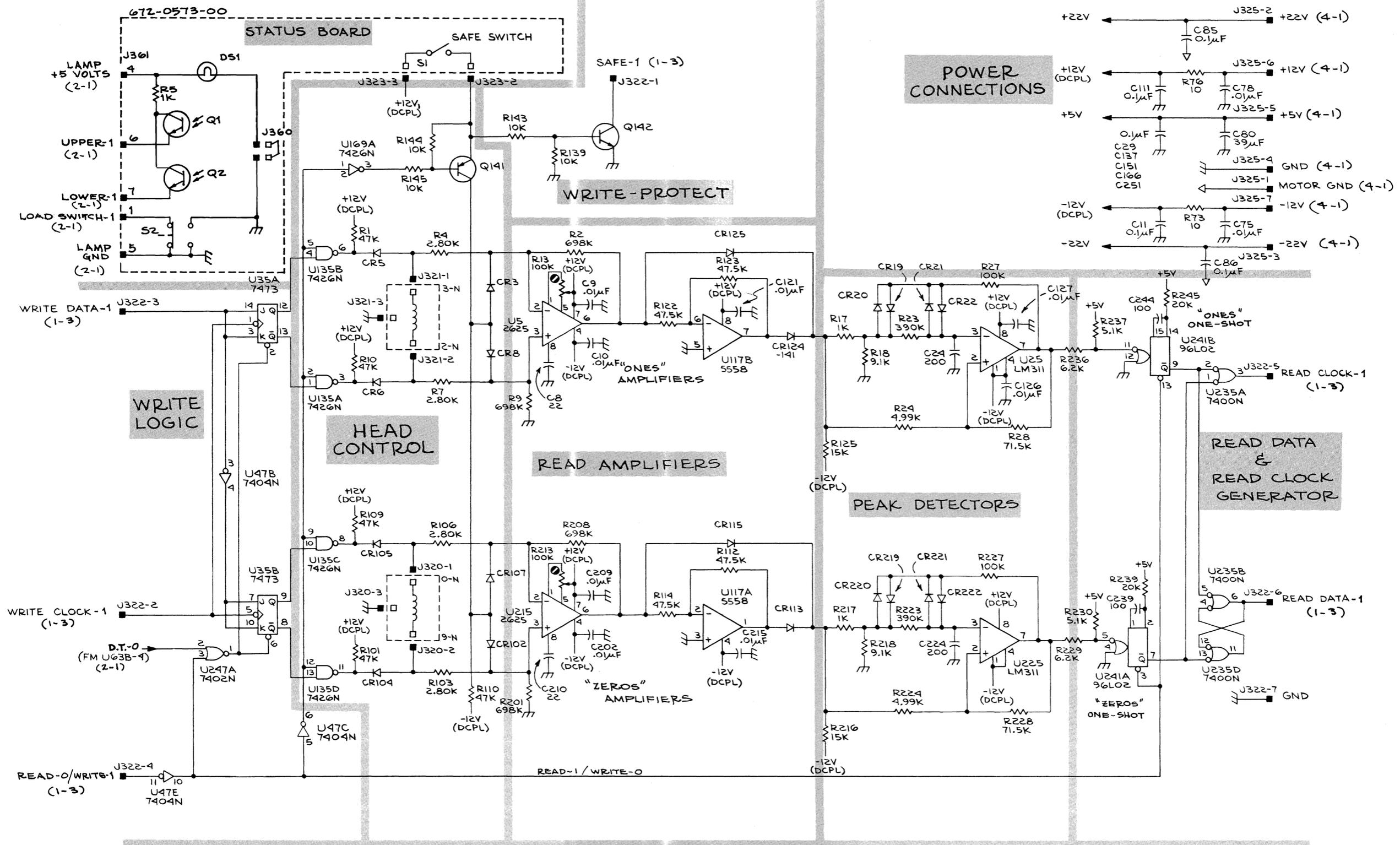
Fig. 7-3. Read/Write board component locations.

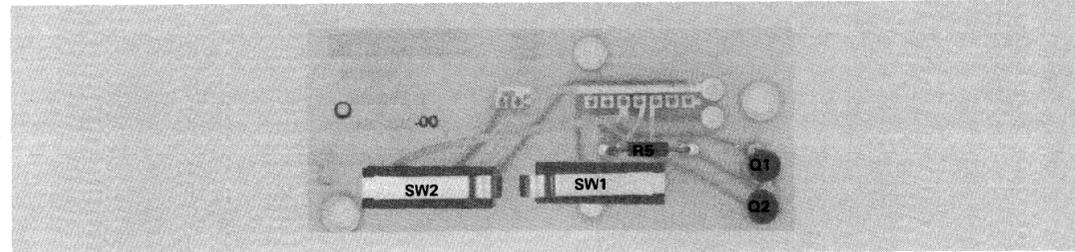


4924

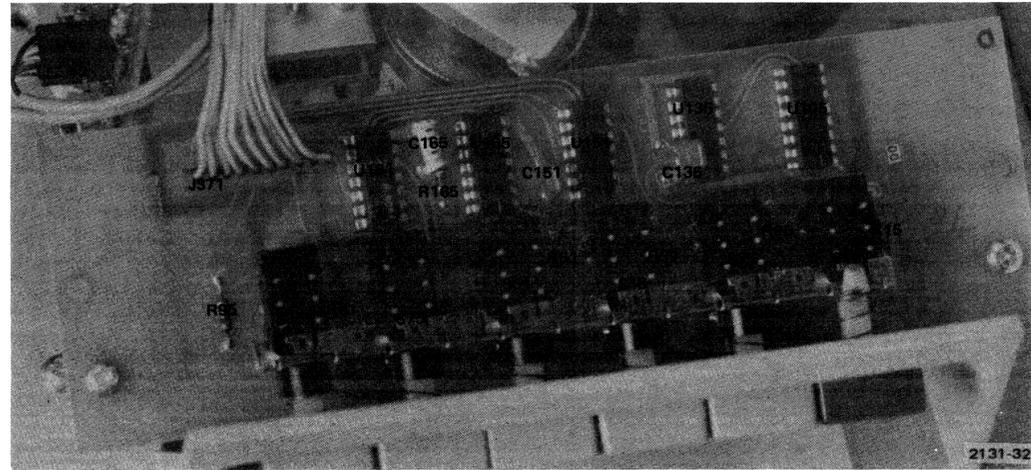
2131-39
REV. FEB 1982

(MOTOR CONTROL)
READ/WRITE BOARD 2-1
670-3925-04,05,06

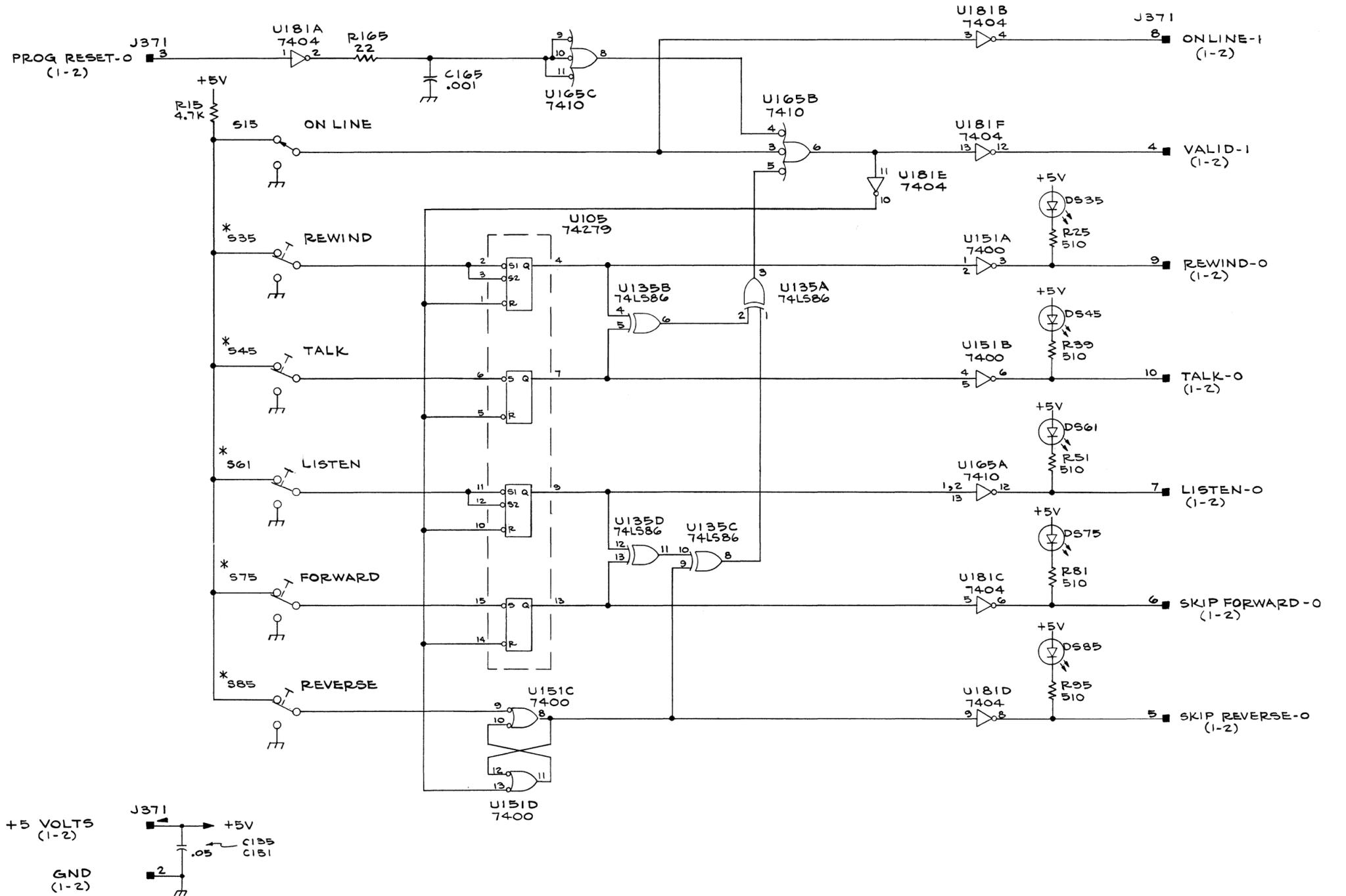




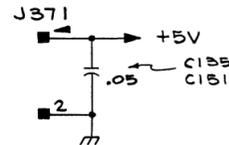
Status board component locations.



Switch & LED Board component locations



+5 VOLTS (1-2)
GND (1-2)

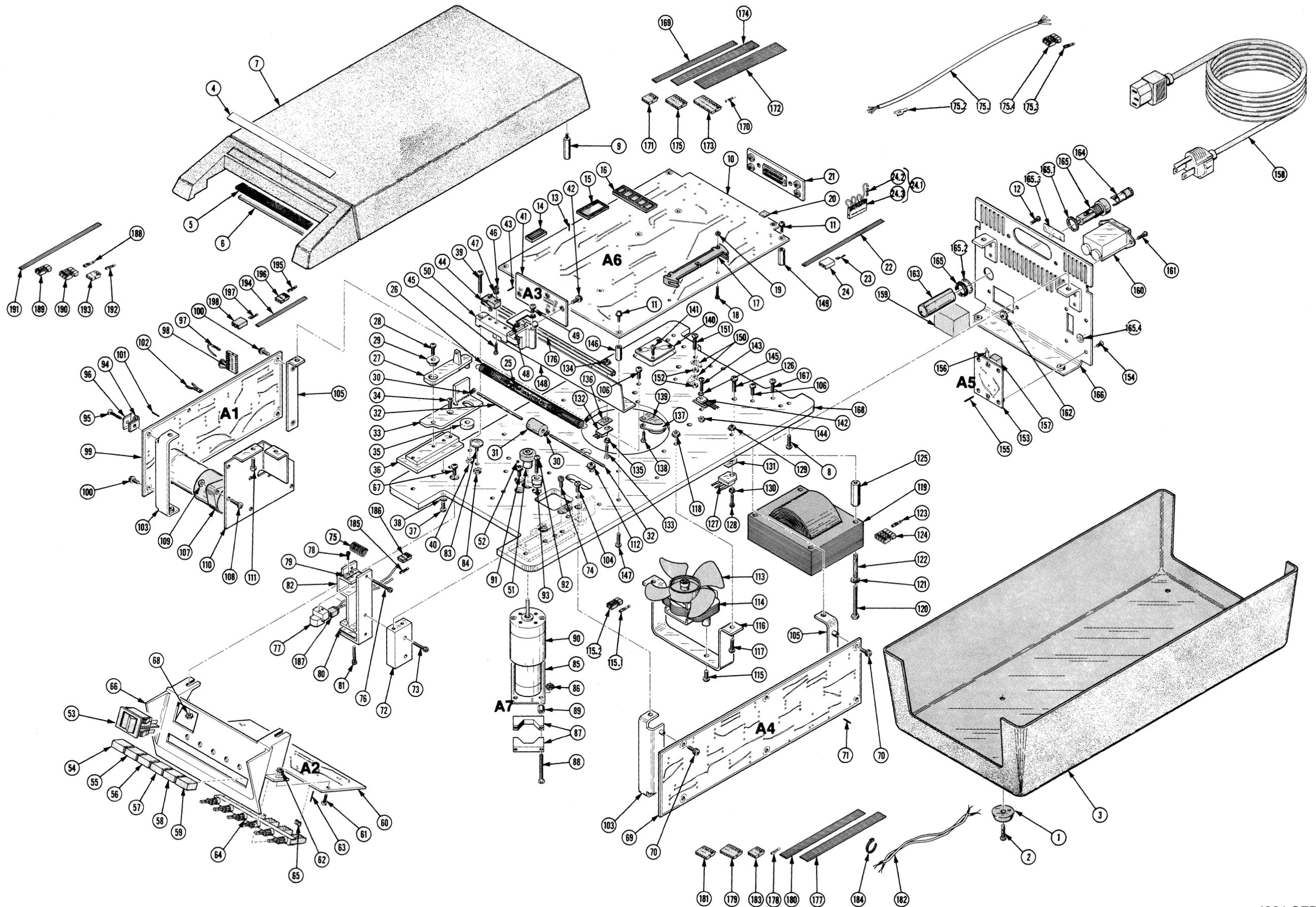


* NOTE: MOMENTARY CONTACT

4924

SWITCH & LED BOARD 3-1
670-4526-00

@



REV JAN 1982

4924 SERVICE

Section 10 REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000 Part first added at this serial number
00X Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```

1 2 3 4 5           Name & Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
    --- * ---
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
    --- * ---
Parts of Detail Part
Attaching parts for Parts of Detail Part
    --- * ---
    
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol --- * --- indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH	ELCTRN	ELECTRON	IN	INCH	SE	SINGLE END
#	NUMBER SIZE	ELEC	ELECTRICAL	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ACTUATOR	ELCTLT	ELECTROLYTIC	INSUL	INSULATOR	SEMICOND	SEMICONDUCTOR
ADPTR	ADAPTER	ELEM	ELEMENT	INTL	INTERNAL	SHLD	SHIELD
ALIGN	ALIGNMENT	EPL	ELECTRICAL PARTS LIST	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	ALUMINUM	EQPT	EQUIPMENT	MACH	MACHINE	SKT	SOCKET
ASSEM	ASSEMBLED	EXT	EXTERNAL	MECH	MECHANICAL	SL	SLIDE
ASSY	ASSEMBLY	FIL	FILLISTER HEAD	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	ATTENUATOR	FLEX	FLEXIBLE	NIP	NIPPLE	SLVG	SLEEVING
AWG	AMERICAN WIRE GAGE	FLH	FLAT HEAD	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	BOARD	FLTR	FILTER	OBD	ORDER BY DESCRIPTION	SQ	SQUARE
BRKT	BRACKET	FR	FRAME or FRONT	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRZ	BRASS	FSTNR	FASTENER	OVH	OVAL HEAD	STL	STEEL
BRZ	BRONZE	FT	FOOT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	BUSHING	FXD	FIXED	PL	PLAIN or PLATE	T	TUBE
CAB	CABINET	GSKT	GASKET	PLSTC	PLASTIC	TERM	TERMINAL
CAP	CAPACITOR	HDL	HANDLE	PN	PART NUMBER	THD	THREAD
CER	CERAMIC	HEX	HEXAGON	PNH	PAN HEAD	THK	THICK
CHAS	CHASSIS	HEX HD	HEXAGONAL HEAD	PWR	POWER	TNSN	TENSION
CKT	CIRCUIT	HEX SOC	HEXAGONAL SOCKET	RCPT	RECEPTACLE	TPG	TAPPING
COMP	COMPOSITION	HLCPS	HELICAL COMPRESSION	RES	RESISTOR	TRH	TRUSS HEAD
CONN	CONNECTOR	HLEXT	HELICAL EXTENSION	RGD	RIGID	V	VOLTAGE
COV	COVER	HV	HIGH VOLTAGE	RLF	RELIEF	VAR	VARIABLE
CPLG	COUPLING	IC	INTEGRATED CIRCUIT	RTNR	RETAINER	W/	WITH
CRT	CATHODE RAY TUBE	ID	INSIDE DIAMETER	SCH	SOCKET HEAD	WSHR	WASHER
DEG	DEGREE	IDNT	IDENTIFICATION	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	DRAWER	IMPLR	IMPELLER	SCR	SCREW	XSTR	TRANSISTOR

REPLACEABLE MECHANICAL PARTS

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
S3109	FELLER ASA ADOLF AG., C/O PANEL COMPONENTS CORP.	355 TESCONI CIRCLE	SANTA ROSA, CA 95401
S3629	PANEL COMPONENTS CORP.	2015 SECOND ST.	BERKELEY, CA 94170
000AE	GARDNER SPRING COMPANY	1115 N UTICA	TULSA, OK 74110
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
02777	HOPKINS ENGINEERING COMPANY	12900 FOOTHILL BLVD.	SAN FERNANDO, CA 91342
03614	BUSSMAN MFG., DIV. OF MCGRAW EDISON CO.	502 EARTH CITY PLAZA	EARTH CITY, MO 63045
07111	PNEUMO DYNAMICS CORPORATION	4800 PRUDENTIAL TOWER	BOSTON, MA 02199
08261	SPECTRA-STRIP CORP.	7100 LAMPSON AVE.	GARDEN GROVE, CA 92642
11983	NORTRONICS COMPANY, INC.	8101 10TH AVENUE NORTH	MINNEAPOLIS, MN 55427
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
16428	BELDEN CORP.	P. O. BOX 1331	RICHMOND, IN 47374
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
24931	SPECIALITY CONNECTOR CO., INC.	2620 ENDRESS PLACE	GREENWOOD, IN 46142
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
49671	RCA CORPORATION	30 ROCKEFELLER PLAZA	NEW YORK, NY 10020
52792	THORNGREN TOOL AND MOLDING CO., INC.	1100 EVANS AVENUE	VALPARAISO, IN 46383
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
59730	THOMAS AND BETTS COMPANY	36 BUTLER ST.	ELIZABETH, NJ 07207
70485	ATLANTIC INDIA RUBBER WORKS, INC.	571 W. POLK ST.	CHICAGO, IL 60607
70903	BELDEN CORP.	2000 S BATAVIA AVENUE	GENEVA, IL 60134
71218	BUD RADIO, INC.	4605 E. 355TH ST.	WILLOUGHBY, OH 44094
71400	BUSSMAN MFG., DIVISION OF MCGRAW- EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
74445	HOLO-KROME CO.	31 BROOK ST. WEST	HARTFORD, CT 06110
74868	BUNKER-RAMO CORP., THE AMPHENOL RF DIV.	33 E. FRANKLIN ST.	DANBURY, CT 06810
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
79136	WALDES, KOHINOOR, INC.	47-16 AUSTEL PLACE	LONG ISLAND CITY, NY 11101
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80126	PACIFIC ELECTRICORD CO.	747 W. REDONDO BEACH, P O BOX 10	GARDENA, CA 90247
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
85471	BOYD, A. B., CO.	2527 GRANT AVENUE	SAN LEANDRO, CA 94579
86445	PENN FIBRE AND SPECIALTY CO., INC.	2032 E. WESTMORELAND ST.	PHILADELPHIA, PA 19134
95987	WECKESSER CO., INC.	4444 WEST IRVING PARK RD.	CHICAGO, IL 60641
97913	INDUSTRIAL ELECTRONIC HARDWARE CORP.	109 PRINCE STREET	NEW YORK, NY 10012

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	348-0001-00		4		MOUNT, RESILIENT: 0.19 ID X 0.940 OD, RUBBER (ATTACHING PARTS)	71218	F7264A
-2	211-0651-00		4		SCREW, MACHINE: 6-32 X 0.5 PNH, STL BK OXD - - - * - - -	07111	OBD
-3	200-1812-00		1		COVER, BOTTOM: TAPE READER	80009	200-1812-00
-4	334-2854-00		1		PLATE, IDENT: MARKED 4924	80009	334-2854-00
-5	348-0382-00		1		GASKET: LIGHT SEAL, TOP AND BOTTOM	80009	348-0382-00
-6	-----		AR		PLASTIC STRIP: PRESS, SENS, ADH CTD BS		
-7	200-1813-01		1		COVER, TOP: W/6.32 INSERTS, TAN (ATTACHING PARTS)	80009	200-1813-01
-8	211-0651-00		4		SCREW, MACHINE: 6-32 X 0.5 PNH, STL BK OXD	07111	OBD
-9	129-0565-00		4		POST, ELEC-MECH: 1.281 L, W/6-32 THD, AL - - - * - - -	80009	129-0565-00
-10	-----		1		CKT BOARD ASSY: CONTROL (SEE A6 REPL) (ATTACHING PARTS)		
-11	211-0601-00		7		SCR, ASSEM WSHR: 6-32 X 0.312, DOUBLE SEMS	83385	OBD
-12	211-0507-00		2		SCREW, MACHINE: 6-32 X 0.312 INCH, PNH STL - - - * - - -	83385	OBD
-13	131-0608-00	B010100 B041173	64		CKT BOARD ASSY INCLUDES: . TERMINAL, PIN: 0.365 L X 0.025 PH BRZ GOLD	22526	47357
	131-0608-00	B041174	73		. TERMINAL, PIN: 0.365 L X 0.025 PH BRZ GOLD	22526	47357
-14	136-0260-02	B010100 B041173	6		. SKT, PL-IN ELEK: MICROCIRCUIT, 16 DIP, LOW CLE	71785	133-51-92-008
	136-0670-00	B041174	2		. SKT, PL-IN ELEK: MICROCKT, 18 PIN, LOW PROFILE	73803	CS9002-18
-15	136-0578-00		6		. SKT, PL-IN ELEK: MICROCKT, 24 PIN, LOW PROFILE	73803	C S9002-24
-16	136-0623-00		5		. SOCKET, PLUG-IN: 40 DIP, LOW PROFILE	73803	CS9002-40
-17	131-1780-00		1		. CONNECTOR, REC, : RT-ANGLE HDR, 2/25 MALE (ATTACHING PARTS)	22526	65483-005
-18	211-0185-00		2		. SCREW, MACHINE: 2-56 X 0.438", PNH, STL	07111	OBD
-19	210-0405-00		2		. NUT, PLAIN, HEX. : 2-56 X 0.188 INCH, BRZ - - - * - - -	73743	12157-50
-20	-----		AR		. PLASTIC STRIP: PRESS, SENS, ADH CTD BS		
-21	386-3370-01		1		. PLATE, CONN MTG: REAR, W/HARDWARE	80009	386-3370-01
	198-3166-00	B010100 B041173X	1		. WIRE SET, ELEC: - . . (CABLE ASSY: A6/Q1010)	80009	198-3166-00
-22	175-0826-00	B010100 B041173X	AR		. . WIRE, ELECTRICAL: 3 WIRE RIBBON	80009	175-0826-00
-23	131-1815-00	B010100 B041173	3		. . CONTACT, ELEC: 22-30 AWG, FEMALE, BRASS	27264	08-56-0110
	131-0707-00	B041174	8		. . CONNECTOR, TERM: 22-26 AWG, BRZ& CU BE GOLD	22526	47439
-24	204-0678-00	B010100 B041173	1		. . CONN BODY, PL, EL: FOR 3 FEMALE CONTACTS	27264	10-17-2032
	352-0167-08	B041174	1		. . CONN BODY, PL, EL: 9 WIRE GRAY	80009	352-0167-08
24.1	175-2903-00		1		. LEAD ASSY, ELEC: 4, 26 AWG, 1.5 L, 9-N - . . (A6, J308)	80009	175-2903-00
24.2	131-0707-00		8		. . CONNECTOR, TERM: 22-26 AWG, BRZ& CU BE GOLD	22526	47439
24.3	352-0167-08		1		. . CONN BODY, PL, EL: 9 WIRE GRAY	80009	352-0167-08
-25	124-0326-00		1		STRIP, CUSHION: SPRING SILENCER	80009	124-0326-00
-26	214-2261-00		1		SPRING, HLCP: 0.035 DIA, 5.5 L MUSIC WIRE	80009	214-2261-00
-27	214-2264-00		2		ARM, DETENT: TAPE POSITIONING (ATTACHING PARTS)	80009	214-2264-00
-28	211-0511-00		2		SCREW, MACHINE: 6-32 X 0.500, PNH, STL, CD PL - - - * - - -	83385	OBD
-29	343-0551-00		2		RTRN, DETENT ARM: 0.14 ID X 0.373 OD, AL	80009	343-0551-00
-30	354-0554-00		4		RING, RETAINING: EXT LUG GRIPPING, 0.094 D	79136	G5555-9
-31	401-0349-00		1		ROLLER, HOLDDOWN: 0.50 DIA X 0.75 L, NYLON	80009	401-0349-00
-32	384-1383-00		1		SHAFT, HOLDDOWN: 0.093 DIA X 7.66 L, STL	80009	384-1383-00
-33	351-0451-00		1		GUIDE, TAPE CRTG: TOP LEFT	80009	351-0451-00
	351-0462-00		1		GUIDE, TAPE CRTG: TOP RIGHT (ATTACHING PARTS)	80009	351-0462-00
-34	211-0538-00		2		SCREW, MACHINE: 6-32 X 0.312"100 DEG, FLH STL - - - * - - -	83385	OBD
-35	214-2263-00		2		WHEEL, DETENT: 0.187 ID X 0.6 OD, SST	80009	214-2263-00
-36	351-0445-01		2		GUIDE, TAPE CRTG: 1.250 W X 2.820 INCH LONG (ATTACHING PARTS)	80009	351-0445-01
-37	211-0511-00		2		SCREW, MACHINE: 6-32 X 0.500, PNH, STL, CD PL	83385	OBD
-38	210-0006-00		4		WASHER, LOCK: #6 INTL, 0.018THK, STL CD PL - - - * - - -	78189	1206-00-00-0541C

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
1-	343-0549-00			1						STRAP, TIEDOWN: 0.091 W X 3.62 INCH LONG	59730	TY100
	-----			1						CKT BOARD ASSY: STATUS, W/MICRO SW (SEE A3 REPL) (ATTACHING PARTS)		
-39	211-0516-00			2						SCREW, MACHINE: 6-32 X 0.875 INCH, PNH STL	83385	OBD
-40	210-0457-00			2						NUT, PL, ASSEM WA: 6-32 X 0.312, STL CD PL	83385	OBD
	-----									- - - - * - - - -		
				-						CKT BOARD ASSY INCLUDES:		
-41	-----			-						. CKT BOARD ASSY: STATUS, NOT AVAILABLE, SEE A3 (ATTACHING PARTS)		
-42	211-0601-00			2						. SCR, ASSEM WSHR: 6-32 X 0.312, DOUBLE SEMS	83385	OBD
	-----									- - - - * - - - -		
				-						. CKT BOARD ASSY INCLUDES:		
-43	131-0608-00			9						. . TERMINAL, PIN: 0.365 L X 0.025 PH BRZ GOLD	22526	47357
-44	-----			2						. SWITCH, SENS: (SEE S1, S2 REPL) (ATTACHING PARTS)		
-45	211-0034-00			4						. SCREW, MACHINE: 2-56 X 0.50 INCH, PNH	83385	OBD
-46	210-0405-00			4						. NUT, PLAIN, HEX.: 2-56 X 0.188 INCH, BRS	73743	12157-50
-47	210-0001-00			4						. WASHER, LOCK: INTL, 0.092 ID X 0.18"OD, STL	78189	1202-00-00-0541C
	-----									- - - - * - - - -		
-48	200-1886-00			1						. COVER, LIGHT: 1.191 INCH LONG, AL (ATTACHING PARTS)	80009	200-1886-00
-49	211-0503-00			2						. SCREW, MACHINE: 6-32 X 0.188 INCH, PNH STL	83385	OBD
	-----									- - - - * - - - -		
-50	-----			1						. BRKT, SENSOR MTG: NOT AVAILABLE, SEE A3		
-51	401-0333-01			1						HUB, TAPE DRIVE: W/WHEEL (ATTACHING PARTS)	80009	401-0333-01
-52	213-0048-00			1						SETSCREW: 4-40 X 0.125 INCH, HEX SOC STL	74445	OBD
	-----									- - - - * - - - -		
-53	-----			1						SWITCH, ROCKER: POWER (SEE S1000 REPL)		
-54	366-1415-02			1						PUSH BUTTON: RED, ON LINE	80009	366-1415-02
-55	366-1416-09			1						PUSH BUTTON: LT GRAY, REWIND	80009	366-1416-09
-56	366-1416-07			1						PUSH BUTTON: LT GRAY, LISTEN	80009	366-1416-07
-57	366-1416-08			1						PUSH BUTTON: LT GRAY, TALK	80009	366-1416-08
-58	366-1416-01			1						PUSH BUTTON: LT GRAY, FORWARD	80009	366-1416-01
-59	366-1416-05			1						PUSH BUTTON: LT GRAY, REVERSE	80009	366-1416-05
-60	-----			1						CKT BOARD ASSY: SWITCH, (SEE A2 REPL) (ATTACHING PARTS)		
-61	211-0510-00			2						SCREW, MACHINE: 6-32 X 0.375, PNH, STL, CD PL	83385	OBD
-62	210-0457-00			2						NUT, PL, ASSEM WA: 6-32 X 0.312, STL CD PL	83385	OBD
	-----									- - - - * - - - -		
				-						CKT BOARD ASSY INCLUDES:		
-63	131-0608-00			10						. TERMINAL, PIN: 0.365 L X 0.025 PH BRZ GOLD	22526	47357
-64	-----			1						. SWITCH, PUSH: (SEE S15, S35, S45, S61, S75, S85 REPL)		
-65	361-0383-00			6						. SPACER, PB SW: CHARCOAL, 0.33 INCH LONG	80009	361-0383-00
-66	386-3298-00			1						PANEL, FRONT: TAPE READER (ATTACHING PARTS)	80009	386-3298-00
-67	211-0511-00			2						SCREW, MACHINE: 6-32 X 0.500, PNH, STL, CD PL	83385	OBD
-68	210-0457-00			2						NUT, PL, ASSEM WA: 6-32 X 0.312, STL CD PL	83385	OBD
	-----									- - - - * - - - -		
-69	-----			1						CKT BOARD ASSY: READ/WRITE (SEE A4 REPL) (ATTACHING PARTS)		
-70	211-0601-00			6						SCR, ASSEM WSHR: 6-32 X 0.312, DOUBLE SEMS	83385	OBD
	-----									- - - - * - - - -		
				-						CKT BOARD ASSY INCLUDES:		
-71	131-0608-00			49						. TERMINAL, PIN: 0.365 L X 0.025 PH BRZ GOLD	22526	47357
-72	391-0144-00	B010100	B040639	1						BLOCK, SUPPORT: HEAD ALIGNMENT	80009	391-0144-00
	391-0144-01	B040640		1						BLOCK, SUPPORT: HEAD ALIGNMENT (ATTACHING PARTS)	80009	391-0144-01
-73	211-0093-00	B010100	B040639	2						SCR, CAP, SOC HD: 4-40 X 0.75 INCH L, STL	000BK	OBD
	211-0588-00	B040640		2						SCREW, MACHINE: 6-32 X 0.75 INCH, HEX. HD STL	83385	OBD
	210-0004-00	B010100	B040639	2						WASHER, LOCK: #4 INTL, 0.015THK, STL CD PL	000BK	OBD
	210-0803-00	B040640		2						WASHER, FLAT: 0.15 ID X 0.032 THK, STL CD PL	12327	OBD
-74	211-0564-00			2						SCREW, CAP, SCH: 6-32 X 0.375" L HEX	80009	211-0564-00
	-----									- - - - * - - - -		

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
1-75	214-2430-00		1						SPRING,HLCPS:0.375 OD X 1.5 L,OPEN ENDS (ATTACHING PARTS)	000AE	C36C
-76	211-0248-00		1						SCREW,CAP,SCH:4-40 X 1.25 FLH,82 DEG,STL - - - * - - -	000AH	OBD
-77	119-0421-00		1						HEAD,SRR: (ATTACHING PARTS)	11983	G717888-DC21P078
-78	211-0206-00		2						SCR,CAP,SOC HD:2-56 X 0.312 INCH,STL - - - * - - -	000AH	OBD
-79	386-2823-00		1						PL,MTG,TAPE HD:	80009	386-2823-00
-80	386-3554-00		1						PLATE,PROT:HEAD ALIGNMENT (ATTACHING PARTS)	80009	386-3554-00
-81	211-0164-00		1						SCREW,CAP,SCH:4-40 X 0.625 INCH,L STL	83385	OBD
	211-0093-00		1						SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL - - - * - - -	000BK	OBD
-82	352-0450-00	B010100 B040639	1						HLDR,HEAD ALIGN:ALUMINUM	80009	352-0450-00
	352-0450-01	B040640	1						HLDR,HEAD ALIGN:ALUMINUM	80009	352-0450-01
-83	361-0781-00		2						SPACER,PAD:W/4-40 THD (ATTACHING PARTS)	80009	361-0781-00
-84	210-0457-00		1						NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL - - - * - - -	83385	OBD
-85	-----		1						CKT BOARD ASSY:MOTOR FILTER(SEE A7 REPL) (ATTACHING PARTS)		
-86	210-0457-00		2						NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL - - - * - - -	83385	OBD
	-----		-						CKT BOARD ASSY INCLUDES:		
	131-0589-00		4						. TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
-87	407-1823-00		2						BRACKET,CKT BD:ALUMINUM (ATTACHING PARTS)	80009	407-1823-00
-88	211-0552-00		2						SCREW,MACHINE:6-32 X 2 INCH,PNH STL	83385	OBD
-89	361-0060-00		2						NUT,PLAIN,HEX.:6-32 X 0.175 INCH LONG - - - * - - -	80009	361-0060-00
-90	-----		1						MOTOR,DC:(SEE M1015/T1017 REPL) (ATTACHING PARTS)		
-91	211-0534-00		3						SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	OBD
-92	211-0513-00		1						SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-93	105-0729-00		1						STOP,TAPE CRTG:0.171 ID X 0.41 OD X 0.312" - - - * - - -	80009	105-0729-00
-94	343-0004-00		1						CLAMP,LOOP:0.312 INCH DIAMETER,PLSTC (ATTACHING PARTS)	95987	5-16-6B
-95	211-0510-00		1						SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
-96	210-0863-00		1						WSHR,LOOP CLAMP:0.187 ID U/W 0.5 W CLP,STL - - - * - - -	95987	C191
	131-1776-00		1						LINK,TERM.CONNE:BLACK,26 AWG,600V	80009	131-1776-00
-97	131-0707-00		4						. CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-98	352-0166-00		1						. CONN BODY,PL,EL:8 WIRE BLACK	80009	352-0166-00
-99	-----		1						CKT BOARD ASSY:POWER SUPPLY(SEE A1 REPL) (ATTACHING PARTS)		
-100	211-0601-00		3						SCR,ASSEM WSHR:6-32 X 0.312,DOUBLE SEMS - - - * - - -	83385	OBD
	-----		-						CKT BOARD ASSY INCLUDES:		
-101	131-0589-00		46						. TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
-102	344-0154-00		6						. CLIP,ELECTRICAL:FUSE,CKT BD MT	80009	344-0154-00
-103	407-1683-01		2						BRACKET,COVER:ALUMINUM (ATTACHING PARTS)	80009	407-1683-01
-104	211-0511-00		2						SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL - - - * - - -	83385	OBD
-105	407-1668-00		4						BRACKET,ANGLE:CIRCUIT BOARD,ALUMINUM (ATTACHING PARTS)	80009	407-1668-00
-106	211-0511-00		4						SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL - - - * - - -	83385	OBD
-107	432-0048-00		3						BASE,CAP.MTG:GENERAL (ATTACHING PARTS)	80009	432-0048-00
-108	211-0513-00		6						SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-109	210-0407-00		6						NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS - - - * - - -	73743	3038-0228-402

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
1-110	407-1728-00		1						BRACKET,CAP.:ALUMINUM (ATTACHING PARTS)	80009	407-1728-00
-111	211-0511-00		2						SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
-112	210-0457-00		2						NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL - - - * - - -	83385	OBD
-113	369-0037-01		1						IMPLR,FAN,AXIAL:3.5 DIA BL,CW,0.125 ID	52792	3500-CW125W
-114	-----		1						MOTOR,DC:(SEE B1001 REPL) (ATTACHING PARTS)		
-115	212-0518-00		2						SCREW,MACHINE:10-32 X 0.312,PNH,STL,CD PL - - - * - - -	83385	OBD
	-----		-						MOTOR INCLUDES:		
115.1	352-0198-00		1						. HLDR,TERM CONN:2 WIRE BLACK	80009	352-0198-00
115.2	131-0792-00		2						. CONNECTOR,TERM:18-20 AWG,CU BE GOLD PL	22526	46221
-116	407-1679-00		1						BRKT,FAN MOTOR:ALUMINUM (ATTACHING PARTS)	80009	407-1679-00
-117	211-0513-00		2						SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-118	210-0457-00		2						NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL - - - * - - -	83385	OBD
-119	-----		1						XFMR,PWR,STPDN:(SEE T1001 REPL) (ATTACHING PARTS)		
-120	212-0517-00		4						SCREW,MACHINE:10-32 X 1.750INCH,HEX HD STL	83385	OBD
-121	210-0812-00		4						WASHER,NONMETAL:#10,FIBER	86445	OBD
-122	166-0226-00		4						INS SLV,ELEC:1.125 INCHES LONG - - - * - - -	80009	166-0226-00
	-----		-						XFMR ASSY INCLUDES:		
-123	131-0621-00		8						. CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	46231
-124	352-0201-00		2						. CONN BODY,PL,EL:5 WIRE BLACK	80009	352-0201-00
-125	384-0632-00		4						POST,ELEC-MECH:0.375 X 1.109" LONG,10-32 (ATTACHING PARTS)	80009	384-0632-00
-126	212-0509-00		4						SCREW,MACHINE:10-32 X 0.625INCH,PNH STL - - - * - - -	83385	OBD
-127	-----		2						TRANSISTORS:(SEE Q1011,Q1013 REPL) (ATTACHING PARTS)		
-128	211-0014-00		2						SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	OBD
-129	210-0586-00		2						NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	OBD
-130	210-1178-00		2						WASHER,SHLDR:U/W T0-220 TRANSISTOR - - - * - - -	49671	DF137A
-131	342-0311-00		2						INSULATOR,PLATE:TRANSISTOR,MICA	01295	64-21-023-212
-132	-----		2						TRANSISTOR:(SEE Q1002,Q1006 REPL) (ATTACHING PARTS)		
-133	211-0014-00		2						SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	OBD
-134	210-0586-00		2						NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	OBD
-135	210-1178-00		2						WASHER,SHLDR:U/W T0-220 TRANSISTOR - - - * - - -	49671	DF137A
-136	342-0202-00		2						INSULATOR,PLATE:TRANSISTOR	01295	10-21-023-106
-137	-----		1						TRANSISTOR:(SEE Q1004 REPL) (ATTACHING PARTS)		
-138	213-0183-00		2						SCR,TPG,THD FOR:6-20 X 0.5 TYPE B,PNH,STL - - - * - - -	83385	OBD
-139	386-0978-00		1						INSULATOR,PLATE:TRANSISTOR,MICA	80009	386-0978-00
-140	136-0280-00		1						SOCKET,PLUG-IN:TRANSISTOR,3 CONTACT (ATTACHING PARTS)	97913	LST 2202-2
-141	213-0088-00		2						SCR,TPG,THD CTG:4-24 X 0.25 INCH,PNH STL - - - * - - -	83385	OBD
-142	-----		1						TRANSISTOR:(SEE Q1010 REPL) (ATTACHING PARTS)		
-143	211-0014-00		1						SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	OBD
-144	210-0586-00		1						NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	OBD
-145	210-0071-00		1						WASHER,SPR TNSN:0.146 ID X 0.323" OD,STL - - - * - - -	78189	4706-05-01-0531
-146	385-0070-00		2						SPACER,POST:0.5 L W/6-32 THD THRU,AL (ATTACHING PARTS)	80009	385-0070-00
-147	211-0511-00		2						SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL - - - * - - -	83385	OBD

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-148	378-0062-00			1		BAFFLE,AIR:TAPE CARTRIDGE	80009	378-0062-00
-149	384-0519-00			5		SPACER,POST:0.562 L,W/6-32 THD THRU (ATTACHING PARTS)	80009	384-0519-00
	211-0511-00			5		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL - - - * - - -	83385	OBD
-150	210-0202-00			2		TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED (ATTACHING PARTS)	78189	2104-06-00-2520N
-151	211-0513-00			1		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-152	210-0407-00	B010100	B041009	2		NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
	210-0407-00	B041010		3		NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS - - - * - - -	73743	3038-0228-402
-153	-----			1		CKT BOARD ASSY:MODE/ADDRESS SELECT(SEE A5 REPL) (ATTACHING PARTS)		
-154	211-0101-00			4		SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL - - - * - - -	83385	OBD
	-----					CKT BOARD ASSY INCLUDES:		
-155	131-0589-00			10		. TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
-156	131-0566-00			1		. BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
-157	-----			1		. SWITCH,ROCKER:(SEE S101 REPL)		
-158	-----					(SEE ACCESSORIES PAGE)		
-159	200-1788-00	B010100	B015339	1		COV,PROT,LINE:1.20 X 1.20 X 0.842",PLSTC	80009	200-1788-00
	200-1788-01	B015340		1		COV,PROT,LINE:	80009	200-1788-01
-160	119-0389-00			1		FILTER,RAD INTE:115/230V,3A (ATTACHING PARTS)	02777	F11935-3
-161	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
-162	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL - - - * - - -	83385	OBD
-163	200-0237-03	B010100	B041023	1		COVER,FUSE HLDR:	80009	200-0237-03
	200-0237-04	B041024		1		COVER,FUSE HLDR:PLASTIC,SAFETY CONTROLLED	80009	200-0237-04
-164	200-0582-00	B010100	B041999	1		CAP,ELECTRICAL:FUSE HOLDER	71400	9435 1/2
	200-2264-00	B042000		1		CAP.,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
-165	352-0010-00	B010100	B041999	1		FUSEHOLDER:WITH HARDWARE	03614	HKP-L
	204-0832-00	B042100		1		BODY,FUSEHOLDER:3AG,5 X 20MM FUSES	S3629	031.1673(MDLFEU)
165.1	210-0873-00	XB042000		1		WASHER,NONMETAL:0.5 ID X 0.688 INCH OD,NPRN	70485	OBD
165.2	210-1039-00	XB042000		1		WASHER,LOCK:INT,0.521 ID X 0.625 INCH OD	24931	OBD
165.3	334-2560-00	B010100	B040936	1		MARKER,IDENT:MARKED 230V	80009	334-2560-00
	334-2560-01	B040937		1		MARKER,IDENT:MARKED 110V,50HZ	80009	334-2560-01
165.4	334-3379-02	XB042000		1		MARKER,IDENT:MARKED GROUND SYMBOL	80009	334-3379-02
-166	333-2185-01	B010100	B041408	1		PANEL,REAR:	80009	333-2185-01
	333-2185-02	B041409		1		PANEL,REAR: (ATTACHING PARTS)	80009	333-2185-02
-167	211-0511-00			2		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL - - - * - - -	83385	OBD
-168	441-1277-00			1		CHAS,TAPE RDR:MAIN	80009	441-1277-00
	198-3132-00	B010100	B041603	1		WIRE SET,ELEC:	80009	198-3132-00
	198-3132-01	B041604		1		WIRE SET,ELEC: - CABLE ASSY:J301/J342	80009	198-3132-01
-169	175-0861-00			AR		. . WIRE,ELECTRICAL:4 WIRE RIBBON	08261	SS-0422-7(1061)
-170	131-0707-00			8		. . CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-171	352-0162-01			1		. . CONN BODY,PL,EL:4 WIRE BROWN	80009	352-0162-01
	352-0162-02			1		. . CONN BODY,PL,EL:4 WIRE RED - . CABLE ASSY:J303/J381	80009	352-0162-02
-172	175-0833-00			AR		. . WIRE,ELECTRICAL:10 WIRE RIBBON	08261	SS-1026-7
	131-0707-00			20		. . CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-173	352-0168-03			1		. . CONN BODY,PL,EL:10 WIRE ORANGE	80009	352-0168-03
	352-0168-01			1		. . HLDR,TERM CONN:10 WIRE,BROWN - . CABLE ASSY:J305/J371	80009	352-0168-01
	175-0833-00			AR		. . WIRE,ELECTRICAL:10 WIRE RIBBON	08261	SS-1026-7
	131-0707-00			20		. . CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
	352-0168-05			1		. . CONN BODY,PL,EL:10 WIRE GREEN	80009	352-0168-05
	352-0168-01			1		. . HLDR,TERM CONN:10 WIRE,BROWN - . CABLE ASSY:J306/J324	80009	352-0168-01
	175-0833-00			AR		. . WIRE,ELECTRICAL:10 WIRE RIBBON	08261	SS-1026-7
	131-0707-00			20		. . CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
	352-0168-06			1		. . CONN BODY,PL,EL:10 WIRE BLUE	80009	352-0168-06

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
1-	352-0168-04		1	CONN BODY,PL,EL:10 WIRE YELLOW	80009	352-0168-04
	-----		-	CABLE ASSY:J307/J322		
-174	175-0830-00		AR	WIRE,ELECTRICAL:7 WIRE RIBBON	08261	SS-0726-710610C
	131-0707-00		14	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-175	352-0165-07		1	CONN BODY,PL,EL:7 WIRE VIOLET	80009	352-0165-07
	352-0165-02		1	CONN BODY,PL,EL:7 WIRE RED	80009	352-0165-02
175.1	175-1577-00		AR	CABLE,SP,ELEC:4,18 AWG,TWISTED	80009	175-1577-00
175.2	131-0861-00	B010100 B041603	4	TERM,QIK DISC:16-20 AWG,0.22 W X 0.02 THK	00779	42617-2
	131-2435-00	B041604	4	TERM,QIK DISC:FEMALE,18-22 AWG	00779	2-520183-2
175.3	131-0792-00		2	CONNECTOR,TERM:18-20 AWG,CU BE GOLD PL	22526	46221
175.4	352-0199-00		1	CONN BODY,PL,EL:3 WIRE BLACK	80009	352-0199-00
	198-2304-00		1	WIRE SET,ELEC:	80009	198-2304-00
-176	252-0571-00		AR	NEOPRENE EXTR:CHAN,0.234 X 0.156	85471	DIE#1353
	-----		-	CABLE ASSY:J323/J351		
-177	175-0830-00		AR	WIRE,ELECTRICAL:7 WIRE RIBBON	08261	SS-0726-710610C
-178	131-0707-00		14	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-179	352-0165-03		1	CONN BODY,PL,EL:7 WIRE ORANGE	80009	352-0165-03
	352-0165-01		1	CONN BODY,PL,EL:7 WIRE BROWN	80009	352-0165-01
	-----		-	CABLE ASSY:J325/J344		
	175-0858-00		AR	WIRE,ELECTRICAL:7 WIRE RIBBON	08261	SS-0722-7(1061)
	131-0707-00		14	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
	352-0165-05		1	CONN BODY,PL,EL:7 WIRE GREEN	80009	352-0165-05
	352-0165-04		1	CONN BODY,PL,EL:7 WIRE YELLOW	80009	352-0165-04
	-----		-	CABLE ASSY:J327/Q1011,Q1013		
-180	175-0829-00		FT	WIRE,ELECTRICAL:6 WIRE RIBBON	08261	SS-0626-710610C
	131-0707-00		6	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-181	352-0164-07		1	HLDR,TERM CONN:6 WIRE VIOLET	80009	352-0164-07
	-----		-	CABLE ASSY:J326/J50		
-182	175-0072-00		FT	CABLE,RF:2 CONDUCTOR	80009	175-0072-00
	175-0072-00		FT	CABLE,RF:2 CONDUCTOR	80009	175-0072-00
	131-0707-00		10	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
	352-0164-06		1	CONN BODY,PL,EL:6 WIRE BLUE	80009	352-0164-06
-183	352-0162-00		1	HLDR,TERM CONN:4 WIRE BLACK	80009	352-0162-00
-184	343-0549-00		3	STRAP,TIEDOWN:0.091 W X 3.62 INCH LONG	59730	TY100
-185	131-0707-00		6	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-186	352-0161-00		1	HLDR,TERM CONN:3 WIRE,BLACK	80009	352-0161-00
	352-0161-01		1	CONN BODY,PL,EL:3 WIRE BROWN	80009	352-0161-01
-187	119-0421-01		1	HEAD,SRR CABLE:	11983	139077
	-----		-	CABLE ASSY:J345/B1001		
-188	131-0621-00		2	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	46231
-189	352-0198-00		1	HLDR,TERM CONN:2 WIRE BLACK	80009	352-0198-00
	-----		-	CABLE ASSY:J348/S1000		
	131-0621-00		3	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	46231
-190	352-0199-00		1	CONN BODY,PL,EL:3 WIRE BLACK	80009	352-0199-00
	-----		-	CABLE ASSY:J340/Q1004		
-191	175-0862-00		FT	WIRE,ELECTRICAL:3 WIRE RIBBON	08261	SS-0322-1910610C
-192	131-0707-00		3	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-193	352-0161-00		1	HLDR,TERM CONN:3 WIRE,BLACK	80009	352-0161-00
	-----		-	CABLE ASSY:J343/Q1002		
-194	175-0826-00		FT	WIRE,ELECTRICAL:3 WIRE RIBBON	80009	175-0826-00
-195	131-0707-00		3	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
-196	352-0361-03		1	CONN BODY,PL,EL:3 WIRE ORANGE	80009	352-0161-03
-197	131-1815-00		3	CONTACT,ELEC:22-30 AWG,FEMALE,BRASS	27264	08-56-0110
-198	204-0678-00		1	CONN BODY,PL,EL:FOR 3 FEMALE CONTACTS	27264	10-17-2032
	-----		-	CABLE ASSY:J341/Q1006		
	175-0826-00		FT	WIRE,ELECTRICAL:3 WIRE RIBBON	80009	175-0826-00
	131-0707-00		3	CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	47439
	352-0161-01		1	CONN BODY,PL,EL:3 WIRE BROWN	80009	352-0161-01
	131-1815-00		3	CONTACT,ELEC:22-30 AWG,FEMALE,BRASS	27264	08-56-0110
	204-0678-00		1	CONN BODY,PL,EL:FOR 3 FEMALE CONTACTS	27264	10-17-2032

Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
ACCESSORIES						
-----				- CARTRIDGE, TAPE: MAGNETIC		
012-0630-01	B010100 B040940	1		CABLE, INTCON: 2 METERS LONG	74868	AC30111102 REVC
012-0630-03	B040941	1		CABLE, INTCON: 2 METERS L	74868	AC30147-102
070-2128-00		1		MANUAL, TECH: USERS	80009	070-2128-00
161-0066-00		1		CABLE ASSY, PWR: 3, 18 AWG, 115V, 98.0 L	16428	KH8481
-----				- (100-120VAC OPERATION)		
161-0066-09	XB041298	1		CABLE ASSY, PWR: 3, 0.75MM SQ, 220V, 96.0 L	80126	OBD
-----				- (OPTION A1, UNIVERISAL EUROPEAN)		
161-0066-10	XB041298	1		CABLE ASSY, PWR: 3, 0.75MM SQ, 240V, 96.0 L	80126	OBD
-----				- (OPTION A2, UNITED KINGDOM)		
161-0066-11	XB041298	1		CABLE ASSY, PWR: 3, 0.75MM, 240V, 96.0L	S3109	OBD
-----				- (OPTION A3, AUSTRALIAN)		
161-0066-12	XB041298	1		CABLE ASSY, PWR: 3, 18 AWG, 240V, 96.0 L	80126	OBD
-----				- (OPTION A4, NORTH AMERICAN)		
OPTIONAL ACCESSORIES						
119-0680-01		1		CARTRIDGE, TAPE: MAGNETIC	80009	119-0680-01
161-0066-01		1		CABLE ASSY, PWR: 3, 18 AWG, 230V, 98.0 L	80009	161-0066-01
-----				- (200-240VAC OPERATION)		
070-2131-00		1		MANUAL, TECH: SERVICE	80009	070-2131-00

OPTIONS

OPTION	ORDER NO.	DESCRIPTION
A1		220V EUROPEAN PLUG
A2		240V UNITED KINGDOM PLUG
A3		240V AUSTRALIAN PLUG
A4		240V NORTH AMERICAN PLUG

APPENDIX A

GLOSSARY

APPENDIX A

GLOSSARY

address: *noun*—See **device address, primary address, secondary address, memory address;** also **primary listen address, primary talk address, Command Primary Address, Command Primary Listen Address, Command Primary Talk Address, Data Primary Address, Data Primary Listen Address, Data Primary Talk Address.**

address: *verb*—The GPIB controller addresses a device on the GPIB by activating the GPIB's ATN line and sending that device's primary talk address or primary listen address, followed, if necessary, by a secondary address. When the primary talk address is used, the device is "addressed to talk"; when ATN is released it will be the talker in a data transfer. If the primary listen address is used, the device is "addressed to listen"; it will be a listener in any data transfer.

address bus: A group of sixteen lines over which the 4924's MPU sends the address of the memory location into which or from which it is writing or reading data. The address bus lines are A0, A1, ..., A15. A0 carries the least significant bit of the memory address; A15, the most significant bit.

ASCII (American Standard Code for Information Interchange): A standardized code of alphanumeric characters, symbols, and special control characters. Each character is represented by eight binary bits (a byte) in which seven of the bits distinguish one character from another and the eighth bit is reserved for parity checking purposes. The 4924 ignores the parity bit in any ASCII characters it receives, and does not transmit a parity bit. (That is, it always transmits a 0 for the eighth bit.)

ATN (attention!): One of the GPIB management bus lines, activated by the controller to signal that the byte on the data bus is a universal command, primary listen address, primary talk address or secondary address.

BA (bus available): A control bus line by which the MPU may signal that it has effectively disconnected itself from the address and data busses, so that these busses are available for a Direct Memory Access (DMA) operation by an external device (such as the System Test Fixture).

BASIC: An acronym derived from "Beginners All-purpose Symbolic Instruction Code". BASIC is the high-level programming language used to command the Tektronix Model 4051 Graphic System.

bit: A binary digit; a 1 or a 0.

byte: A group of eight binary bits.

checksum: A number computed from the number of binary 1's written in the first 128 or 256 bytes of a physical record, and written into the last byte of the record, the "checksum byte".

close: When the 4924 closes a file, it adds the logical end-of-file mark to the end of the series of data bytes in its write buffer and dumps the contents of the buffer onto the tape, writing one physical record onto the tape. The logical end-of-file mark (hexadecimal FF) marks the logical end of the file; bytes in the physical record beyond the end-of-file mark are filled with ASCII blanks and are not considered part of the logical file.

closed file: A file which has been closed.

Command Primary Address (CPA): When a 4924 (Option 37) is operating in Alternate mode, the settings of the GPIB ADDRESS switches determine not one, but two device addresses. The Command Primary Address is the device address by which the controller addresses the 4924 in order to send it command strings. The CPA is an odd number in the range from 3 to 29; it is always one more than the Data Primary Address. See also, **Command Primary Listen Address**, **Command Primary Talk Address**.

Command Primary Listen Address (CPLA): The primary listen address corresponding to the 4924's Command Primary Address. It is to this address that the controller sends command strings for the 4924.

Command Primary Talk Address (CPTA): The primary talk address corresponding to the 4924's Command Primary Address. After the controller bus set up the 4924 (Option 37, operating in Alternate mode) to execute an ERROR, TYPE, HEADER, or READ STATUS command (by sending a command string to the 4924 at its CPLA), the controller may trigger the 4924 to execute the command by sending the CPTA.

control bus: A group of signal lines by which the 4924's MPU is controlled and by which it controls the transfer of data to and from its memories. The control bus includes the BA, GO/HALT, IRQ, NMI, RESET, RWOC, VMA and ϕ 2L lines.

controller: See **GPIB controller**.

CPA: See **Command Primary Address**.

CPLA: See **Command Primary Listen Address**.

CPTA: See **Command Primary Talk Address**.

data bus: (1) Eight of the wires in the GPIB, used for transferring bytes over the GPIB. The data bus lines are DIO1, DIO2, ..., DIO8; DIO1 carries the least significant bit of each byte, and DIO8 the most significant bit. (2) A bus of eight lines by which the 4924's MPU sends bytes to its memories, and receives bytes from them. The data bus lines are BD0, BD1, ..., BD7; BD0 carries the least significant bit of each byte, and BD7 the most significant bit.

Data Primary Address (DPA): When a 4924 (Option 37) is operating in Alternate mode, the settings of the GPIB ADDRESS switches determine not one, but two device addresses. The Data Primary Address is the device address by which the controller addresses the 4924 in order to send to it data to be recorded on the tape or to receive from it data which has been read from the tape. The DPA is an even number in the range from 2 to 28; it is always one less than the Command Primary Address. See also, **Data Primary Listen Address, Data Primary Talk Address.**

Data Primary Listen Address (DPLA): The primary listen address corresponding to the 4924's Data Primary Address. After the controller has set up the 4924 (Option 37, operating in Alternate mode) to execute a LISTEN, PRINT, SAVE or WRITE command (by sending a command string to the 4924 at its CPLA), the controller may trigger the 4924 to execute the command by sending the DPLA.

Data Primary Talk Address (DPTA): The primary talk address corresponding to the 4924's Data Primary Address. When a 4924 (Option 37, operating in Alternate mode) has been set up to execute a READ, TALK, INPUT or OLD command (by a command string sent to the CPLA), the GPIB controller may trigger the 4924 to execute the command by sending the 4924's DPTA.

device address: A number in the range from 0 to 30 by which a particular device on the GPIB is distinguished from other GPIB devices. The 4924's device address is determined by the settings of the GPIB ADDRESS switches; it is used as the primary address in 4051 BASIC statements used for controlling the 4924.

DPA: See **Data Primary Address.**

DPLA: See **Data Primary Listen Address.**

DPTA: See **Data Primary Talk Address.**

end-of-file mark: The byte (hexadecimal FF) written onto a tape to mark the logical end of a file.

EOI (End Or Identify): One of the GPIB management bus lines. EOI may be activated by the talker to mark the last data byte being sent in a data transfer.

file (logical file): That part of a physical file which is actually used for the storage of data or of a program. The logical file begins with the first byte after the header record; its end is marked with a logical end-of-file mark (hexadecimal FF) written on the tape.

file (physical file): A group of physical records on the tape, marked at its beginning and end with file marks. See the discussion of "Tape Format" in Section 2.

file mark: A mark (comprised of eight NFRs) used to denote the beginning and end of a physical file. See the discussion of "Tape Format" in Section 2.

General Purpose Interface Bus: See **GPIB**.

GO/HALT: A control bus line used to halt the MPU for Direct Memory Access.

GPIB (General Purpose Interface Bus): A 24-wire shielded cable over which the 4924 receives its commands and sends and receives data. The GPIB, and all devices connected to it, must conform to IEEE Standard 488-1975. See also **GPIB controller, data bus, management bus, transfer bus**.

GPIB controller: The device on the GPIB used to control the other devices on the GPIB.

header: The first 44 bytes of the header record of a file, containing information about the file. See the discussion of "Headers" in Section 2.

header record: The first physical record of a file, which holds the header in its first 44 bytes. See the discussion of "Headers" in Section 2.

IFC (Interface Clear): One of the GPIB management bus lines, activated by the controller to unaddress all devices on the bus and put them in a known quiescent state.

IRQ (Interrupt Request): A control bus line by which an interrupt may be requested of the MPU.

listener: A device on the GPIB which receives bytes sent by a talker.

logical end of file: The end of that part of a physical file which has been used for the storage of data or of a program. The logical end of a file is marked by an end-of-file mark written as a byte on the tape.

management bus: Five of the lines in the GPIB, used to control data transfers over the GPIB's data bus. The management bus lines are ATN, SRQ, IFC, EOI and REN.

memory address: A sixteen-bit binary number denoting the location of a particular byte in the 4924's memory.

MLA: *abbrev.* The 4924's primary listen address. (From the term "my listen address", used in IEEE Standard 488-1975.)

MPU (microprocessor unit): The MC6800 microprocessor which is the "brain" of the 4924.

MTA: *abbrev.* The 4924's primary talk address. (From the term "my talk address", used in IEEE Standard 488-1975.)

MSA: *abbrev.* The 4924's secondary address (the byte sent over the GPIB). (From the term "my secondary address", used in IEEE Standard 488-1975.) "MSA 7" refers to the secondary address byte corresponding to secondary address number 7. "7" would be the secondary address appearing in a 4051 BASIC statement, "MSA 7" the byte sent out over the GPIB.

NFR: A period of no flux reversals recorded on the tape. To be deemed an NFR, an interval of blank tape must last longer than about 40 microseconds at 30 inches per second.

NMI (non-maskable interrupt): A control bus line by which a non-maskable interrupt may be demanded of the MPU.

open file: A file which is being written into, and for which the writing of data into it has not yet been terminated by dumping the write buffer onto the tape and writing a logical end-of-file mark after the last meaningful data byte.

PIA (Peripheral Interface Adapter): An integrated circuit device used as an interface between the MPU and the rest of the 4924.

primary address: (1) In 4051 BASIC statements, the first of two numbers comprising the I/O Address part of the BASIC statement. If the BASIC statement is to cause commands to be sent to the 4924, the primary address will be the device address programmed into the 4924's GPIB ADDRESS switches. For Option 37 4924s operating in Alternate mode the primary address may be either the CPA or the DPA. **(2)** A byte sent by the GPIB controller (with ATN active) by which a particular device on the GPIB is selected to receive a command or participate in a data transfer to occur after ATN is released. After ATN is released, only those devices which have been addressed with ATN active will send or receive data on the GPIB data bus. Primary addresses are ASCII characters whose decimal equivalents are in the range from 32 to 62 or from 64 to 94. See **primary listen address, primary talk address.**

primary listen address: The primary address byte by which the GPIB controller may address a device on the GPIB to set it up as a listener for a coming data transfer. Primary listen addresses are ASCII characters whose decimal equivalents are in the range from 32 to 62. For each possible device address there is a corresponding primary listen address.

primary talk address: The primary address byte by which the GPIB controller may address a device on the GPIB to set it up as a talker for a coming data transfer. Primary talk addresses are ASCII characters whose decimal equivalents are in the range from 64 to 94. For each possible device address there is a corresponding primary talk address.

record (logical record): A string of ASCII characters written onto the tape, marked at its end by a logical record separator. Any ASCII character may serve as the logical record separator, but usually the carriage return character (CR) is used.

record (physical record): A block of 128 or 256 bytes (with a possible additional checksum byte for a total of 129 or 257 bytes) written onto the tape and marked at its beginning and end with record marks. See the discussion of "Tape Format" in Section 2.

record mark: A mark (comprised of four NFRs) used to denote the beginning and end of a physical record. See the discussion of "Tape Format" in Section 2.

REN (remote enable): A GPIB management bus line which may be used by the controller to send the "remote enable" signal. The 4924 does not have the capability to respond to this signal.

RESET: One of the control bus lines, driven by the Reset circuit, by which the MPU and PIAs may be initialized. On receipt of a RESET pulse, the MPU transfers control to the instruction whose address is stored in the highest-address two bytes of memory.

RWOC (Read/Write Open Collector): A control bus line, used by the MPU to steer the transfer of data between the MPU and its memories.

secondary address: (1) In 4051 BASIC statements, the second of two numbers comprising the I/O Address part of the BASIC statement. If no secondary address is explicitly named in the BASIC statement, the BASIC interpreter will supply a "default" secondary address appropriate to the BASIC keyword. The 4051 ordinarily uses secondary addresses to pass commands to its peripherals. **(2)** A byte sent by the GPIB controller (with ATN active), immediately after a primary address byte, to provide supplementary information to the device addressed by the preceding primary address byte. Secondary addresses are ASCII characters whose decimal equivalents are in the range from 96 to 127. For each secondary address (as in definition 1) in a 4051 BASIC statement, there is a corresponding secondary address byte (as in this definition) sent by the 4051 when addressing its peripherals on the GPIB. In 4051 mode, the 4924 interprets its secondary addresses as commands. In Alternate mode, the 4924 ignores any secondary addresses sent it.

serial poll: A procedure by which the GPIB controller may ascertain which device on the GPIB has activated the SRQ line. See the discussion of "Serial Poll" in Section 2.

SPD (Serial Poll Disable): The universal command by which the GPIB controller terminates a serial poll.

SPE (Serial Poll Enable): The universal command by which the GPIB controller initiates a serial poll.

SRQ (service request): (1) One of the GPIB management bus lines, activated by any device (except the controller) to request service of the controller. **(2)** A signal sent on the SRQ line.

string: A series of bytes sent over the GPIB's data bus.

talker: A device on the GPIB which transmits bytes over the GPIB's data bus to other GPIB devices.

transfer bus: Three of the lines in the GPIB, used in a "handshake" procedure during the transfer of each byte over the GPIB's data bus. The transfer bus lines are DAV, NRFD, and NDAC.

unaddress: *verb*—To unaddress a device on the GPIB is to cause it to "get off the bus" and ignore any transfer of bytes over the GPIB data bus until ATN is next activated. If a device has been addressed to talk, when it is unaddressed it ceases to function as a talker. If a device has been addressed to listen, when it is unaddressed it ceases to listen to bytes sent over the data bus. The universal commands UNTALK and UNLISTEN are used to unaddress any devices previously addressed as talkers or as listeners.

universal command: A byte sent by the GPIB controller (with ATN active) by which a command is passed to all devices on the GPIB. Universal commands are ASCII characters whose decimal equivalents are in the range from 0 to 31 or 63 or 95. The 4924 recognizes the universal commands UNTALK, UNLISTEN, SPE and SPD.

UNLISTEN: A universal command by which the GPIB controller may cause any devices on the GPIB which may have been addressed as listeners to unaddress themselves and go into a quiescent state. UNLISTEN is an ASCII character whose decimal equivalent is 63. After receiving a string of data bytes from the GPIB, the 4924 requires an UNLISTEN command to cause it to empty its input buffer and examine the bytes just received.

UNTALK: A universal command by which the GPIB controller may cause any device on the GPIB which may have been addressed as a talker to unaddress itself and go into a quiescent state. UNTALK is an ASCII character whose decimal equivalent is 95.

VMA (Valid Memory Address): One of the control bus lines. When this line is activated by the MPU, it indicates that the MPU's address bus holds a valid memory address and that a data transfer will take place on the current MPU cycle.

APPENDIX B

COMMAND SUMMARIES

The READ ERRORS Command	B-1
4051 BASIC Command Summary	B-2
4051 Mode GPIB Sequences	B-5
Alternate Mode GPIB Sequences	B-10

APPENDIX B

COMMAND SUMMARIES

THE "READ ERRORS" COMMAND

The 4924's command set includes one command, the READ ERRORS command, which is not documented in the 4924 Operators Manual. This command was intended primarily for use in checking prototypes for reliability; however, a description of it is included here, as it may be of use to the service technician.

Each time the 4924 reads a physical record from the tape, it computes a "checksum" from the first 256 bytes of the record and compares this checksum with the final "checksum byte". If they do not agree, a "read error" has been detected: the 4924 backs up the tape and tries again to read the record. If within ten tries it does not successfully read the record, a service request (SRQ) is generated. However, read errors causing only one or two re-reads may occur and not manifest themselves to the user.

Each time a read error is detected, the 4924 increments a counter in its memory. When it receives a READ ERRORS command, it sends out over the GPIB (in ASCII code) the number of read errors it has counted, and resets the counter to zero. Thus, the READ ERRORS command may be used to check for reliable operation: it can inform the service technician of read errors that occur, even when the 4924 eventually (within ten tries) succeeds in reading the record.

The READ ERRORS command may be sent from the 4051 Graphic System by means of an INPUT statement with secondary address of 24, thus:

```
INPUT @2,24:E
```

(In this example, the number of read errors that have occurred—since power-up or the last READ ERRORS command—is returned in the variable E.)

4051 "BASIC" COMMAND SUMMARY

The following are examples of how to command the 4924, when it is operating in "4051" mode, from the keyboard of a 4051 Graphic System. In all of these commands, it has been assumed that "2" is programmed into the 4924's GPIB ADDRESS switches.

<p>APPEND @2: 250 or, APPEND @2,4: 250</p>	<p>The APPEND command. This causes the BASIC program at the present tape location to be transferred over the GPIB to the 4051 Graphic System. As far as the 4924 is concerned, this command is identical to the OLD command, and so it has the same secondary address ("4") as that command. The 4051's BASIC interpreter, however, treats this command differently from the OLD command, inserting the program coming from the 4924 into the program currently in its Random Access Memory.</p>
<p>PRINT @2,2:</p>	<p>The CLOSE command. This closes the current file in the 4924 (that is, writes a "logical end-of-file mark" into that file). 2 is the secondary address for the CLOSE command.</p>
<p>INPUT @2,30: A</p>	<p>The ERROR command. This causes the 4924 to return, as a string of ASCII characters representing a valid numeric constant, the error code of the last error condition, if any. The 4051 stores this code in the numeric variable A. The ERROR command clears the error condition and any SRQ. 30 is the secondary address for the ERROR command.</p>
<p>FIND @2: 5 or, FIND @2,27: 5</p>	<p>The FIND command. This positions the 4924 tape to the beginning of the fifth file on the tape. 27 is the secondary address for the FIND command.</p>
<p>INPUT @2,9: A\$</p>	<p>The HEADER command. This causes the 4924 to return the ASCII character string that reflects the header of the current file. The 4051 stores that character string in the string variable A\$. 9 is the secondary address for the HEADER command.</p>
<p>INPUT @2: A\$ or, INPUT @2,13: A\$</p>	<p>The INPUT command. This causes the 4924 to transfer the contents of its current file to the 4051 as a string of ASCII characters. The 4051 stores the first "logical record" (the characters up to the first CR character in the string) in the string variable A\$, which must be dimensioned large enough to accept it.</p>
<p>INPUT @2: A\$,B\$</p>	<p>In this example of the INPUT command, the first logical record is stored in A\$, the second in B\$.</p>
<p>INPUT @2: N</p>	<p>In this example, the first valid numeric constant occurring in the ASCII string sent from the 4924 is stored in the variable N.</p>

<p>KILL @2: 5 or, KILL @2,7: 5</p>	<p>The KILL command. This causes the 4924 to execute a high-speed search for file 5. When that file is found, its header is marked NEW, and the information in the file cannot be recovered. This makes file 5 available for reassignment. The secondary address for the KILL command is 7.</p>
<p>WBYTE @34,121:</p>	<p>The LISTEN command. This causes the 4924 to write data that appears on the GPIB into the current tape file. In the WBYTE statement, "34" is the decimal equivalent of the binary byte representing device number 2's primary listen address; "121" is the decimal equivalent of the binary byte for secondary address 25. (25 is the secondary address for the LISTEN command.) After sending the LISTEN command to the 4924, a data string must be sent to the 4924 by the controller or by some other device on the GPIB. When the data string is concluded, the controller must send UNLISTEN (WBYTE @63:) to cause the 4924 to stop executing the LISTEN command.</p>
<p>MARK @2: 1,2000 or, MARK @2,28: 1,2000</p>	<p>The MARK command. This causes the 4924 to mark one file large enough to hold 2000 bytes, beginning at the present tape location. 28 is the secondary address for the MARK command.</p>
<p>OLD @2: or, OLD @2,4:</p>	<p>The OLD command. This causes the BASIC program at the present tape location to be transferred to the 4051. The 4051 stores it in its Random Access Memory, replacing the program currently stored there. The secondary address for the OLD command is 4.</p>
<p>PRINT @2: N or, PRINT @2,12: N</p>	<p>The PRINT command. The 4051 takes the data stored in numeric variable N and sends it over the GPIB to the 4924 as a string of ASCII characters. The 4924 records that string on the tape, starting at the present tape position.</p>
<p>PRINT @2: A\$</p>	<p>In this example of the PRINT command, the 4051 sends the contents of string variable A\$ to the 4924 as a string of ASCII characters. The 4924 records that string on the tape, starting at the present tape position.</p>
<p>READ @2: A\$ or, READ @2,14: A\$</p>	<p>The READ command. This causes the 4924 to transfer the contents of the current tape file to the 4051, which stores it in the space allocated to A\$. A\$ must be dimensioned large enough to accept the amount in the file (8192 bytes maximum) and the data must be in machine dependent binary code. 14 is the secondary address for the READ command.</p>

INPUT @2,24: A	The READ ERRORS command. This causes the 4924 to return the number of times (since the last READ ERRORS command or since power-up) that the 4924 has had to re-read a physical tape record in an attempt to get the checksum byte to agree. The 4051 stores this number in numeric variable A.
INPUT @2,0: A,B,C,D	The READ STATUS command. This causes the 4924 to return four numbers (each either 0 or 1) to the 4051, which stores them in the specified variables. These represent the programmable option status parameters currently in effect. 0 is the secondary address for the READ STATUS command.
SAVE @2: or, SAVE @2,1:	The SAVE command. A copy of the BASIC program currently in the 4051's memory is transferred to the 4924. The program is recorded beginning at the current tape position. 1 is the secondary address for the SAVE command.
SECRET @2: or, SECRET @2,29:	The SECRET command. This causes the 4924 to mark the header of the current file "secret". 29 is the secondary address for the SECRET command.
PRINT @2,0: 0,0,0,0	The SET STATUS command. The four zeroes separated by commas set the status parameters: in this case, 256-byte records with checksums and headers and no read-after-write. 0 is the secondary address for the SET STATUS command.
WBYTE @66,122:	The TALK command. This command causes the 4924 to transfer the contents of the current file out over the GPIB to whoever is listening, until it reaches the end of the file (marked by the byte "FF ₁₆ ") or is interrupted by the controller's sending UNTALK. The controller or some other device must be set up to listen to the data string sent by the 4924, and at the conclusion of the "talk" operation the controller must send the UNTALK message to the 4924. (This may be done with another WBYTE statement: "WBYTE @95:".) In this example of the TALK command, the 4924's primary talk address is represented by its decimal equivalent ("66" in the WBYTE statement) and the secondary address of 26 for the TALK command by its decimal equivalent ("122" in the WBYTE statement).
INPUT @2,6: A	The TYPE command. This causes the 4924 to return an integer from 0 through 4, indicating whether the next item in a binary data file is numeric data, character string data, or an end-of-file mark. 6 is the secondary address for the TYPE command.
WRITE @2: N or, WRITE @2,15: N	The WRITE command. This transfers the value assigned to N to the 4924 in binary format. The data is recorded on the tape starting at the present tape position. 15 is the secondary address for the WRITE command.

4051 MODE GPIB SEQUENCES

This table gives examples of the sequences of bytes sent over the GPIB when a 4051 is being used to control a 4924 (operating in 4051 Mode). Bytes sent over the GPIB are represented by expressions within parentheses. A mark in the "ATN" or "EOI" column indicates that the GPIB's ATN or EOI line is active.

(4924 MTA) = (4924's "my talk address") = (4924's primary talk address)

(4924 MLA) = (4924's "my listen address") = (4924's primary listen address)

(MSA 15) = ("my secondary address" 15) = (secondary address 15 in table of GPIB secondary addresses)

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
APPEND	APPEND @2: 250	█	(4924 MTA) (MSA 4)		(ASCII character) . . . (ASCII character) (ASCII "CR")	
		█	(UNTALK) (UNLISTEN)*			
CLOSE	PRINT @2,2:	█	(4924 MLA) (MSA 2) (ASCII "CR")	█		
		█	(UNTALK)* (UNLISTEN)			
ERROR	INPUT @2,30: A	█	(4924 MTA) (MSA 30)		(ASCII "1") (ASCII "2") (ASCII "CR")	
		█	(UNTALK) (UNLISTEN)*			
FIND	FIND @2: 5	█	(4924 MLA) (MSA 27) (ASCII "5") (ASCII "CR")	█		
		█	(UNTALK)* (UNLISTEN)			

*Automatically sent by the 4051 Graphic System, although not needed in this case.

Appendix B

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
HEADER	INPUT @2,9: A\$		(4924 MTA) (MSA 9)		(ASCII character) . . (ASCII character) (ASCII "CR")	
INPUT	INPUT @2: A\$		(4924 MTA) (MSA 13)		(ASCII character) (ASCII character) . . (ASCII character) (ASCII "CR")	
KILL	KILL @2: 5	 	(4924 MLA) (MSA 7) (ASCII "5") (ASCII "CR") (UNTALK)* (UNLISTEN)			
LISTEN	WBYTE @34,121:		(4924 MLA) (MSA 25)			
MARK	MARK @2: 1,200	 	(4924 MLA) (MSA 28) (ASCII "1") (ASCII ",") (ASCII "2") (ASCII "0") (ASCII "0") (ASCII "CR") (UNTALK)* (UNLISTEN)			
OLD	OLD @2:		(Same byte sequence as for the previous "APPEND @2:250" statement.)			

*Automatically sent by the 4051 Graphic System, although not needed in this case.

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
PRINT	PRINT @2: A\$	⋮	(4924 MLA) (MSA 12) (ASCII character) . . . (ASCII character) (ASCII "CR")	⋮		
		⋮	(UNTALK)* (UNLISTEN)			
READ	READ @2: A\$	⋮	(4924 MTA) (MSA 14)		(data byte) . . (data byte)	
		⋮	(UNTALK) (UNLISTEN)*			
READ ERRORS	INPUT @2,24: A	⋮	(4924 MTA) (MSA 24)		(ASCII "1") (ASCII "2") (ASCII "CR")	
		⋮	(UNTALK) (UNLISTEN)*			
READ STATUS	INPUT @2,0: A,B,C,D	⋮	(4924 MTA) (MSA 0)		(ASCII "0") (ASCII ",") (ASCII "0") (ASCII ",") (ASCII "0") (ASCII ",") (ASCII "0") (ASCII "CR")	
		⋮	(UNTALK) (UNLISTEN)*			

*Automatically sent by the 4051 Graphic System, although not needed in this case.

Appendix B

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
SAVE	SAVE @2:	⋮	(4924 MLA) (MSA 1) (ASCII character) (ASCII character) . . (ASCII character) (ASCII "CR")	⋮		
		⋮	(UNTALK)* (UNLISTEN)			
SECRET	SECRET @2:	⋮	(4924 MLA) (MSA 29) (ASCII "CR")			
		⋮	(UNTALK)* (UNLISTEN)			
SET STATUS	PRINT @,2,0: "0,0,0,0"	⋮	(4924 MLA) (MSA 0) (ASCII "0") (ASCII ",") (ASCII "0") (ASCII ",") (ASCII "0") (ASCII ",") (ASCII "0") (ASCII "CR")	⋮		
		⋮	(UNTALK)* (UNLISTEN)			
TALK	WBYTE @66,122: (The 4051 here may use RBYTE statements to read the data from the 4924; or another device on the GPIB may be the listener.) WBYTE @95:	⋮	(4924 MTA) (MSA 26)		(data byte) . . (data byte) (end-of-file mark)	⋮
		⋮	(UNTALK)			

*Automatically sent by the 4051 Graphic System, although not needed in this case.

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
TYPE	INPUT @2,6: A	 	(4924 MTA) (MSA 6) (UNTALK) (UNLISTEN)*		(ASCII "Ø") (ASCII "CR")	
WRITE	WRITE @2: N	 	(4924 MLA) (MSA 15) (data byte) (date byte) . . . (data byte) (data byte) (UNTALK)* (UNLISTEN)			

* Automatically sent by the 4051 Graphic System, although not needed in this case.

"ALTERNATE" MODE GPIB SEQUENCES

This table gives examples of the sequences of bytes sent over the GPIB when a 4051 is being used to control a 4924 (Option 37, operating in Alternate Mode). In these examples, it is assumed that the GPIB ADDRESS switches have been set to "2" or "3", giving a DPA of 2 and a CPA of 3.

(CPLA) = (4924's Command Primary Listen Address)

(CPTA) = (4924's Command Primary Talk Address)

(DPLA) = (4924's Data Primary Listen Address)

(DPTA) = (4924's Data Primary Talk Address)

NOTE: Secondary addresses are automatically sent by the 4051, but are ignored by the 4924 when in "Alternate" programming mode. When using another controller than the 4051, there is no need to have that controller send secondary addresses.

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
CLOSE	PRINT @3: "C"	⊠	(CPLA) (MSA)* (ASCII "C") (ASCII "CR") (UNTALK)* (UNLISTEN)	⊠		
ERROR	PRINT @3: "E" INPUT @2: A	⊠	(CPLA) (MSA)* (ASCII "E") (ASCII "CR") (UNTALK)* (UNLISTEN) (DPTA) (MSA)* (UNTALK) (UNLISTEN)*	⊠	(ASCII "1") (ASCII "2") (ASCII "CR")	
FIND	PRINT @3: "F,5"	⊠	(CPLA) (MSA)* (ASCII "F") (ASCII ",") (ASCII "5") (ASCII "CR") (UNTALK)* (UNLISTEN)	⊠		

*Automatically sent by the 4051 Graphic System, although not needed in this case.

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
HEADER	PRINT @3: "H" INPUT @3: A\$	  	(CPLA) (MSA)* (ASCII "H") (ASCII "CR") (UNTALK)* (UNLISTEN) (CPTA) (MSA)* (UNTALK) (UNLISTEN)*		(ASCII character) (ASCII character) . . (ASCII character) (ASCII "CR")	
INPUT	PRINT @3: "I" INPUT @2: A\$	  	(CPLA) (MSA)* (ASCII "I") (ASCII "CR") (UNTALK)* (UNLISTEN) (DPTA) (MSA)* (UNTALK) (UNLISTEN)*		(ASCII character) . . (ASCII character) (ASCII "CR")	
KILL	PRINT @3: "K,5"	 	(CPLA) (MSA)* (ASCII "K") (ASCII ",") (ASCII "5") (ASCII "CR") (UNTALK)* (UNLISTEN)			

*Automatically sent by the 4051 Graphic System, although not needed in this case.

Appendix B

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
LISTEN	PRINT @3: "L"		(CPLA) (MSA)* (ASCII "L") (ASCII "CR")			
	PRINT @2: A\$	 	(UNTALK)* (UNLISTEN) (DPLA) (MSA)* (ASCII character) (ASCII character) (ASCII "CR")			
MARK	PRINT @3: "M;1,200"	 	(CPLA) (MSA)* (ASCII "M") (ASCII ";") (ASCII "1") (ASCII ",") (ASCII "2") (ASCII "0") (ASCII "0") (ASCII "CR")			
OLD	PRINT @3: "O"	 	(CPLA) (MSA)* (ASCII "O") (ASCII "CR")			

*Automatically sent by the 4051 Graphic System, although not needed in this case.

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
	OLD @2:	⋮	(DPLA) (MSA)*		(ASCII character) . . . (ASCII character) (ASCII "CR") (ASCII "CR")	
PRINT	PRINT @3: "P" PRINT @2: A\$	⋮ ⋮ ⋮ ⋮	(CPLA) (MSA)* (ASCII "P") (ASCII "CR") (UNTALK)* (UNLISTEN) (DPLA) (MSA)* (ASCII character) . . (ASCII character) (ASCII "CR") (UNTALK)* (UNLISTEN)	⋮ ⋮		
READ	PRINT @3: "R" READ @2: A,B\$,C	⋮ ⋮ ⋮ ⋮	(CPLA) (MSA)* (ASCII "R") (ASCII "CR") (UNTALK) (UNLISTEN) (DPTA) (MSA)*	⋮ ⋮	(binary data byte) . . . (binary data byte)	
		⋮	(UNTALK) (UNLISTEN)*			

* Automatically sent by the 4051 Graphic System, although not needed in this case.

Appendix B

4924 Commands	4051 Graphic System BASIC Statements	ATN	4051 Sends: Data Bus	EOI	4924 Sends: Data Bus	EOI
READ STATUS	PRINT @3: "Y" INPUT @3: A,B,C,D	  	(CPLA) (MSA)* (ASCII "Y") (ASCII "CR") (UNTALK)* (UNLISTEN) (CPTA) (MSA)* (UNTALK) (UNLISTEN)*		(ASCII "Ø") (ASCII ",") (ASCII "Ø") (ASCII ",") (ASCII "Ø") (ASCII ",") (ASCII "Ø") (ASCII "CR")	
SAVE	PRINT @3: "S" SAVE @2:	  	(CPLA) (MSA)* (ASCII "S") (ASCII "CR") (UNTALK) (UNLISTEN) (DPLA) (MSA)* (ASCII character) (ASCII character) (ASCII character) (ASCII "CR") (UNTALK)* (UNLISTEN)			

*Automatically sent by the 4051 Graphic System, although not needed in this case.

4924 Commands	4051 Graphic System BASIC Statements	4051 Sends:			4924 Sends:	
		ATN	Data Bus	EOI	Data Bus	EOI
SECRET	PRINT @3: "X"	⋮	(CPLA) (MSA) * (ASCII "X") (ASCII "CR") (UNTALK) * (UNLISTEN)	⋮		
SET STATUS	PRINT @3: "Q,0,0,0,0"	⋮	(CPLA) (MSA) * (ASCII "Q") (ASCII ",") (ASCII "0") (ASCII ",") (ASCII "0") (ASCII ",") (ASCII "0") (ASCII ",") (ASCII "0") (ASCII "CR") (UNTALK) * (UNLISTEN)	⋮		
TALK	PRINT @3: "Z" INPUT @2: A\$	⋮ ⋮ ⋮	(CPLA) (MSA) * (ASCII "Z") (ASCII "CR") (UNTALK) * (UNLISTEN) (DPTA) (MSA) *	⋮	(ASCII character) . . . (ASCII character) (ASCII "CR")	
		⋮	(UNTALK) (UNLISTEN) *			

*Automatically sent by the 4051 Graphic System, although not needed in this case.

Appendix B

4924 Commands	4051 Graphic System BASIC Statements	ATN	4051 Sends: Data Bus	EOI	4924 Sends: Data Bus	EOI
TYPE	PRINT @3: "T" INPUT @3: A	   	(CPLA) (MSA)* (ASCII "T") (ASCII "CR") (UNTALK)* (UNLISTEN) (CPTA) (MSA)* (UNTALK) (UNLISTEN)*		(ASCII "2") (ASCII "CR")	
WRITE	PRINT @3: "W" WRITE @2: N	   	(CPLA) (MSA)* (ASCII "W") (ASCII "CR") (UNTALK)* (UNLISTEN) (DPLA) (MSA)* (binary data byte) (binary data byte) (UNTALK)* (UNLISTEN)	 		

*Automatically sent by the 4051 Graphic System, although not needed in this case.

APPENDIX C

TABLES

4924 Error Codes	C-1
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APPENDIX C

TABLES

4924 ERROR CODES

When the 4924 encounters an error condition and generates a service request (SRQ) to the GPIB controller, the ERROR command may be used to obtain from the 4924 a numeric code indicating the type of error that has occurred. (The ERROR command also clears the SRQ.) The error codes returned by the ERROR command are:

Error Code	Error Message
1	Domain Error or Invalid Argument
2	File Not Found
3	Mag Tape Format Error
4	Illegal Access
5	File Not Open
6	Read Error (10 re-reads)
7	No Cartridge Inserted
8	Over-Read (more than 256 bytes in the buffer)
9	Write-Protected
10	Read-After-Write Error
11	End of Medium
12	End of File

SERIAL POLL STATUS BYTE

The status byte which is sent in response to a serial poll has the form:

BIT	8	7	6	5	4	3	2	1
	X	SRQ	ERR	BUSY	ALT	LINE	EOT	EOF

BIT	NAME	FUNCTION
1	EOF	End of File has occurred.
2	EOT	End of Tape has occurred.
3	Line*	4924 is on line.
4	Alt*	Command switch is in ALT position.
5	Busy	4924 is busy.
6	ERR	An error condition has occurred.
7	SRQ	4924 is requesting service.
8		Unassigned, will not be used.

*An SRQ will be generated when the unit goes from "on-line" operation to manual operation, or from "4051" command mode to "ALT" command mode.

On power-up the system is defined to be on-line, in "4051" mode, so an SRQ will be generated if the ON LINE switch is released or the ALT—4051 switch is in "ALT" position.

MEMORY ADDRESS ASSIGNMENTS

Hexadecimal Address	Device Selected	
0000—00FF	U551, U253	} Random Access Memories
0100—01FF	U453, U251	
0200—02FF	U451, U151	
0300—040B	Unused	
040C—040F	U315	
040C	PIAGPA Control Register	} PIA s
040D	PIAGPA Peripheral & Data Direction Registers	
040E	PIAGPB Control Register	
040F	PIAGPB Peripheral & Data Direction Registers	
0410—0413	Unused	
0414—0417	U331	
0414	PIAMTR Control Register	} PIA s
0415	PIAMTR Peripheral & Data Direction Registers	
0416	PIAMTW Control Register	
0417	PIAMTW Peripheral & Data Direction Registers	
0418—041B	U341	
0418	PIAMTA Control Register	} PIA s
0419	PIAMTA Peripheral & Data Direction Registers	
041A	PIAMTB Control Register	
041B	PIAMTB Peripheral & Data Direction Registers	
041C—0427	Unused	
0428—042B	U321	
0428	PIAKYB Control Register	} PIA s
0429	PIAKYB Peripheral & Data Direction Registers	
042A	PIAADR Control Register	
042B	PIAADR Peripheral & Data Direction Registers	
042C—07FF	Unused	
0800—0BFF	U55	} Read Only Memories
0C00—0FFF	U155	
1000—13FF	U255	
1400—17FF	U355	
1800—1BFF	U455	
1C00—1FFF	U555	

GPIB PRIMARY ADDRESSES

PERIPHERAL DEVICE NUMBER	PRIMARY LISTEN ADDRESS								PRIMARY TALK ADDRESS									
	DECIMAL VALUE	DIO BUS								DECIMAL VALUE	DIO BUS							
		8	7	6	5	4	3	2	1		8	7	6	5	4	3	2	1
Device 0	32	0	0	1	0	0	0	0	0	64	0	1	0	0	0	0	0	0
Device 1	33	0	0	1	0	0	0	0	1	65	0	1	0	0	0	0	0	1
Device 2	34	0	0	1	0	0	0	1	0	66	0	1	0	0	0	0	1	0
Device 3	35	0	0	1	0	0	0	1	1	67	0	1	0	0	0	0	1	1
Device 4	36	0	0	1	0	0	1	0	0	68	0	1	0	0	0	1	0	0
Device 5	37	0	0	1	0	0	1	0	1	69	0	1	0	0	0	1	0	1
Device 6	38	0	0	1	0	0	1	1	0	70	0	1	0	0	0	1	1	0
Device 7	39	0	0	1	0	0	1	1	1	71	0	1	0	0	0	1	1	1
Device 8	40	0	0	1	0	1	0	0	0	72	0	1	0	0	1	0	0	0
Device 9	41	0	0	1	0	1	0	0	1	73	0	1	0	0	1	0	0	1
Device 10	42	0	0	1	0	1	0	1	0	74	0	1	0	0	1	0	1	0
Device 11	43	0	0	1	0	1	0	1	1	75	0	1	0	0	1	0	1	1
Device 12	44	0	0	1	0	1	1	0	0	76	0	1	0	0	1	1	0	0
Device 13	45	0	0	1	0	1	1	0	1	77	0	1	0	0	1	1	0	1
Device 14	46	0	0	1	0	1	1	1	0	78	0	1	0	0	1	1	1	0
Device 15	47	0	0	1	0	1	1	1	1	79	0	1	0	0	1	1	1	1
Device 16	48	0	0	1	1	0	0	0	0	80	0	1	0	1	0	0	0	0
Device 17	49	0	0	1	1	0	0	0	1	81	0	1	0	1	0	0	0	1
Device 18	50	0	0	1	1	0	0	1	0	82	0	1	0	1	0	0	1	0
Device 19	51	0	0	1	1	0	0	1	1	83	0	1	0	1	0	0	1	1
Device 20	52	0	0	1	1	0	1	0	0	84	0	1	0	1	0	1	0	0
Device 21	53	0	0	1	1	0	1	0	1	85	0	1	0	1	0	1	0	1
Device 22	54	0	0	1	1	0	1	1	0	86	0	1	0	1	0	1	1	0
Device 23	55	0	0	1	1	0	1	1	1	87	0	1	0	1	0	1	1	1
Device 24	56	0	0	1	1	1	0	0	0	88	0	1	0	1	1	0	0	0
Device 25	57	0	0	1	1	1	0	0	1	89	0	1	0	1	1	0	0	1
Device 26	58	0	0	1	1	1	0	1	0	90	0	1	0	1	1	0	1	0
Device 27	59	0	0	1	1	1	0	1	1	91	0	1	0	1	1	0	1	1
Device 28	60	0	0	1	1	1	1	0	0	92	0	1	0	1	1	1	0	0
Device 29	61	0	0	1	1	1	1	0	1	93	0	1	0	1	1	1	0	1
Device 30	62	0	0	1	1	1	1	1	0	94	0	1	0	1	1	1	1	0
UNLISTEN/UNTALK	63	0	0	1	1	1	1	1	1	95	0	1	0	1	1	1	1	1

GPIB SECONDARY ADDRESSES

SECONDARY ADDRESS	COMMAND	DECIMAL VALUE	DATA BUS								
			8	7	6	5	4	3	2	1	
0	"STATUS"	96	0	1	1	0	0	0	0	0	0
1	SAVE	97	0	1	1	0	0	0	0	0	1
2	CLOSE	98	0	1	1	0	0	0	1	0	0
3	*	99	0	1	1	0	0	0	1	1	1
4	OLD/APPEND	100	0	1	1	0	0	1	0	0	0
5	*	101	0	1	1	0	0	1	0	1	1
6	TYPE	102	0	1	1	0	0	1	1	0	0
7	KILL	103	0	1	1	0	0	1	1	1	1
8	*	104	0	1	1	0	1	0	0	0	0
9	"HEADER"	105	0	1	1	0	1	0	0	0	1
10	*	106	0	1	1	0	1	0	1	0	1
11	*	107	0	1	1	0	1	0	1	1	1
12	PRINT	108	0	1	1	0	1	1	0	0	0
13	INPUT	109	0	1	1	0	1	1	0	1	1
14	READ	110	0	1	1	0	1	1	1	0	0
15	WRITE	111	0	1	1	0	1	1	1	1	1
16	*	112	0	1	1	1	0	0	0	0	0
17	*	113	0	1	1	1	0	0	0	0	1
18	*	114	0	1	1	1	0	0	1	0	0
19	*	115	0	1	1	1	0	0	1	1	1
20	*	116	0	1	1	1	0	1	0	0	0
21	*	117	0	1	1	1	0	1	0	1	1
22	*	118	0	1	1	1	0	1	1	0	0
23	*	119	0	1	1	1	0	1	1	1	1
24	"READ ERRORS"	120	0	1	1	1	1	0	0	0	0
25	"LISTEN"	121	0	1	1	1	1	0	0	0	1
26	"TALK"	122	0	1	1	1	1	0	1	0	0
27	FIND	123	0	1	1	1	1	0	1	1	1
28	MARK	124	0	1	1	1	1	1	0	0	0
29	SECRET	125	0	1	1	1	1	1	0	1	1
30	"ERROR"	126	0	1	1	1	1	1	1	0	0
31	*	127	0	1	1	1	1	1	1	1	1

*undefined

ASCII CODE CHART

BITS				CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y	
B7	B6	B5	B4	B3	B2	B1					
0	0	0	0	NUL	DLE	SP	0	@	P	\	p
0	0	0	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	STX	DC2	"	2	B	R	b	r
0	0	1	1	ETX	DC3	#	3	C	S	c	s
0	1	0	0	EOT	DC4	\$	4	D	T	d	t
0	1	0	1	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	ACK	SYN	&	6	F	V	f	v
0	1	1	1	BEL BELL	ETB	/	7	G	W	g	w
1	0	0	0	BS BACK SPACE	CAN	(8	H	X	h	x
1	0	0	1	HT	EM)	9	I	Y	i	y
1	0	1	0	LF LINE FEED	SUB	*	:	J	Z	j	z
1	0	1	1	VT	ESC	+	;	K	[k	{
1	1	0	0	FF	FS	,	<	L	\	l	:
1	1	0	1	CR RETURN	GS	-	=	M]	m	}
1	1	1	0	SO	RS	.	>	N	^	n	~
1	1	1	1	SI	US	/	? UNLISTEN	O	_	o	RUBOUT (DEL) UNTALK
				UNIVERSAL COMMAND		LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES	