



Removable Cartridge Disk Drive

SparQ

Internal EIDE
Technical Reference

Part Number 113277-001

Revision A

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The SparQ and SyJet removable disk cartridges are covered by one or more of the following U.S. patents: 4,503,474; 4,717,981; 4,864,452; 4,965,691; 5,218,503; 5,280,403; 5,422,775; 5,400,201; 5,523,902; DES367,579; DES342,062.

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- Reorient the antenna.
- Relocate the equipment with respect to the receiver.
- Move the equipment away from the receiver.
- Plug the equipment into a different outlet so that equipment and receiver are on different branch circuits.

If necessary, consult your dealer or an experienced radio/television technician for additional suggestions. The booklet entitled *How to Identify and Resolve Radio-TV Interference Problems*, prepared by the Federal Communications Commission, may be helpful. This booklet, Stock No. 004-000-003454, is available from the U.S. Government Printing Office, Washington, DC 20402.

Safety Standards

This product meets the following national and international regulations:

- UL 1950 Standard for Safety of Information Processing and Business Equipment
- UL Standard for Safety of Information Technology
- CSA C22.2 No. 154 Data Processing Equipment
- CSA C22 No. 220 Information Processing Equipment
- IEC 435 Safety Requirements for Data Processing Equipment
- IEC 380 Safety of Electrical Energized Office Equipment
- IEC 950 Safety of Information Technology Equipment in Electrical Business Equipment
- VDE 0871/1984
- VFG 243/1991

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1

About This Manual

This manual provides reference information for SyQuest's SparQ EIDE disk drive and SparQ cartridge.

This manual also provides instructions for installing the internally mounted SparQ in PC-compatible systems.

Audience

We intend this manual for original-equipment manufacturers and integrators of SyQuest removable cartridge disk drives.

Organization of This Manual

Chapter 1 (this chapter) describes this manual's audience and organization.

Chapter 2 gives an overview of the SparQ, describing its advantages of availability, reliability, and maintainability. This chapter also describes basic product features, including SyQuest-provided utilities and allegiance controls for the drive and cartridge, and contamination-management functions.

Chapter 3 provides specifications for the SparQ EIDE disk drive and SparQ cartridge. Specifications range from physical and operational characteristics to performance measurements; environmental characteristics; and data on availability, reliability, and maintainability.

Chapter 4 gives instructions for installing the internally mounted SparQ in PC-compatible systems.

Chapter 5 describes the EIDE interface protocol between PC host systems and the SparQ: the standard used; physical, electrical, and signal characteristics; general operational requirements; self-test routines; interface register descriptions; and timing measurements.

Chapter 6 gives EIDE command descriptions for the SparQ.

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Features

This chapter gives an overview of the SparQ—its advantages and basic product features.

About the Product

The SparQ incorporates the finest developments of Winchester technology. Tolerances designed into the drive and cartridge, plus the use of intelligent runout cancellation algorithms, optimize the reliability of drive and cartridge functions in the harsh operating environments of interchangeable media.

The drive's breakthrough read/write performance, reliability, and interchangeability are the results of a proprietary mechanical design. This design creates the most contaminant-free operating environment available in a removable cartridge disk drive. Also, the drive's rugged servo-tracking and load/unload systems provide robust operation and extensive recovery capabilities.

Special advantages of the SparQ EIDE drive and SparQ cartridge include:

- Cartridge data availability
- Drive and cartridge reliability
- Drive and cartridge maintainability

Availability

A fixed hard drive is dependent on the disk drive assembly or PCBA for data availability. Unlike a fixed hard drive, a SyQuest disk drive houses all data on a removable cartridge. This feature ensures the accessibility and usability of stored data.

When a fixed hard drive fails, you face an uncertain and time-consuming data recovery process that includes all the risks of electro-mechanical repairs by the vendor. If a SparQ drive fails, data recovery is usually as simple as moving the cartridge to another SparQ drive. In the rare event that the SparQ cartridge is damaged, SyQuest can usually transfer your data to another cartridge by using special firmware.

Fixed hard drives are very susceptible to head crashes, primarily due to excessive shock, stiction, or accumulated debris from constant head/disk contact. When a fixed drive is powered down, the heads are parked in the *loading zone* in contact with media surfaces. Even moderate shocks during transit can cause the heads to ding the media. During periods of inactivity, another danger is the molecular bond (or *stiction*) that readily forms between the media and parked heads. This usually results in damage to both heads and media. Finally, when a fixed drive is powered up but does not access data for long periods of time, the heads continue to *track-follow* and collect debris and lube material.

In contrast, SyQuest disk drives park the heads on a ramp away from the media during times of inactivity and when powered down. Also, once you remove the SparQ cartridge from the drive, you remove the possibility of any contact between heads and media. Since SyQuest disk drives never park heads on the media, the possibility of stiction does not exist. SyQuest quality design ensures the availability of your data on a removable cartridge when you need it.

Reliability

Mean Time Between Failure (MTBF) is a term that has been used throughout the disk drive industry as a measure of how reliable a drive is expected to be. This term is often used as a basic measure of reliability for repairable items such as a CPU board or disk drive. However, in order to calculate MTBF, a system must fail, then be repaired, returned to service, and fail again. Disk drives are most often replaced, not repaired, once they fail. Therefore, MTBF is not the correct measure of reliability. SyQuest uses MTBF to mean *Mean Time to First Failure* (MTTFF) or, as it is sometimes called, *Mean Time to Failure* (MTTF).

To say that a drive has a predicted or theoretical MTBF of 250,000 hours means that, in a given large population of drives, the average time in which a drive may fail will be 250,000 hours. MTBF (or MTTF) is not a means of predicting the life of an individual drive or a small group of drives. To achieve this number, a drive would run until it reaches its end-of-life period, or fail and then be replaced by a new drive of similar reliability, and so on. In this case, it is theoretically possible that 250,000 hours would elapse before a failure would occur in a large population.

For a specific product, MTBF is calculated based on a budgeting technique where the printed circuit board assembly (PCBA) is modeled using Bellcore's Prediction Procedure for unique parts, part stress, and part count data from SyQuest's database. The head/disk assembly (HDA) mechanics are calculated with Bellcore, and then historical data containing the failure analysis of field-returned drives of similar technology is factored in. The cartridge mechanics are also calculated with Bellcore, and then historical data containing the failure analysis of field-returned cartridges of similar technology is factored in. The data from these models are combined with an analysis of the PCBA, HDA, and cartridge assembly processes to create a complete MTBF estimate.

Maintainability

SyQuest drives and cartridges are designed for heavy use and long life. The drive enclosure, an advanced air filtration system, few moving parts, and intelligent firmware cleansing algorithms support an internal drive environment that is very clean. These features ensure the maintainability of the SparQ drive and cartridge.

Proper care of the drive and cartridge can further minimize the threat of contamination:

- Never operate the drive with its door open.
- Do not open the cartridge door.
- Always completely remove a cartridge once it is ejected.
- Put the cartridge in its protective case during times of inactivity and when moving the drive. Otherwise, you may damage the drive or cartridge and void your warranty.

These additional precautions promote long life for the SparQ cartridge:

- Keep the cartridge away from strong magnetic forces.
- Store the cartridge within a nonoperating temperature range of -40°C to 60°C.

Basic Features

The SparQ product includes these features:

- Utilities that support drive-maintenance functions
- Drive-allegiance controls for the SparQ drive
- Cartridge-allegiance controls that are saved on the SparQ cartridge
- Stand-alone utilities
- Contamination-management functions

Drive-Maintenance Utilities

This special utility helps maintain the SparQ:

Clean Heads: Runs special proprietary diagnostics that remove any debris that may have settled near the heads. Use this routine only if the standard data-recovery actions of running Scandisk under Windows 95 or 3.1x fail.

Drive-Allegiance Controls

Settings for *drive-allegiance controls* affect any SparQ cartridge that you use in a particular SparQ drive. The Lock or Unlock control is saved in the drive's RAM for the current power-on session only.

Lock or Unlock: Governs the eject-button function. When the eject button is locked (disabled), you must send a software Unlock command *and* depress the eject button on the SparQ drive to remove a cartridge. (SyQuest provides this utility for Windows 3.1x only—this function is not required for Windows 95 or Windows NT.)

Cartridge-Allegiance Controls

Settings for *cartridge-allegiance controls* affect only a particular SparQ cartridge, and remain valid for any SparQ drive with which you use that cartridge.

These controls only need to be set once and are thereafter saved on the cartridge until changed by the user.

Write-Protect Enable/Disable: Specifies whether data on the cartridge can be altered or erased. SparQ cartridges are shipped ready to record data, with write protection disabled by default.

Write-Verify Enable/Disable: Specifies whether data just written to the cartridge is read and compared for correctness with the original data transferred. SparQ cartridges are shipped with this data reliability feature enabled by default. To maximize performance or when operating in audio/video mode, disable this feature.

Stand-Alone Utilities

SyQuest provides a suite of stand-alone utilities under multiple operating systems. Here are a few examples of what these utilities do:

- Copy files, partitions, and cartridges
- Backup
- Restore
- Format cartridges
- Scan cartridges for defects
- Assign defects

Contamination Management

Contamination in a removable cartridge disk drive can result in poor performance, interchangeability problems, and other malfunctions. The SparQ drive includes a proprietary labyrinth sealing door on the outside of the drive that uses system airflow to prevent contaminants from entering the drive.

Airflow within the drive works to tightly seal the drive door while it circulates through a microparticle filter located in the active, critical airflow conduits. During purge cycles and throughout continuous cleaning operations, this filter captures any particles swept off disk surfaces or introduced into airflow cavities while the cartridge is in the drive.

The SparQ cartridge includes an anti-rattle mechanism that prevents the disk from banging against the inside of the cartridge casing if the cartridge sustains a physical shock. This feature minimizes the introduction of contaminants from the cartridge.

The Microparticle Filter

The SparQ drive filter is test-proven to meet stringent criteria for managing contamination within the drive. Table 2-1 provides filter data.

Table 2-1 Microparticle Filter

Filter area	0.25 sq. in
Filter materials	5-layer electrostatic, activated carbon 3.41 mm thick at 0.5 psi
Filter performance	Activated carbon for organic vapor absorption. Impregnated K CO for acid gas absorption. Absorbs Trimethylpentone and H ₂ S. Minimum efficiency 94.24% on .2 micron parts at 5.3 cm/sec.
Volume to purge	11.92 cu. in
Continuous purge activity when cartridge is in drive (even during Sleep mode)	Heavy-particulate insertion shows 90% clean-up in 95 seconds with 0.09 to 0.2 micron particles

Firmware Cleansing Algorithms

Fewer mechanical parts and linkages to rub during drive operation, coupled with no requirement for drive adjustments during manufacturing, promote an internal drive environment that is very clean. Intelligent firmware cleansing algorithms reduce internal contaminants as well. These are the algorithms:

Sweep: This algorithm is applied at head load and other times during operation to move large particulates off disk surfaces and into the airflow for filtration. This algorithm also maintains consistent media lube over the entire surfaces of the disk.

Park: This algorithm lifts drive heads from disk surfaces after a period of no access, thus eliminating unnecessary working of disk surfaces, the depletion of lube on disk surfaces, and the vacuum-cleaner effect of gathering debris on drive heads.

Clean: This algorithm provides special maintenance for drive heads, actually burnishing and cleaning drive heads at slow speed to remove debris.

Butterfly: This is a seek algorithm that dynamically manages the media and actuator-bearing lube.

Load/Unload: This algorithm includes a special sequence of servo, actuator arm, and disk-speed controls, accompanied by Sweep and registration functions.

3

Specifications

This chapter provides specifications for the SparQ EIDE disk drive and SparQ cartridge.

The SparQ Drive

Drive specifications include:

- Physical and operational characteristics
- Performance measurements
- Environmental characteristics
- Data on reliability and maintainability

Physical and Operational Characteristics

Table 3-1 Capacity

Per Cartridge	Potential
1.0 Gigabyte minimum ¹	<i>Unlimited</i> in increments of 1.0 Gigabyte
Note: ¹ 1 Gigabyte = 1 billion bytes	

Table 3-2 Configuration

Cartridge—removable	1
Data heads	2
Data surfaces	2
Servo	Embedded sector

Table 3-3 Physical Characteristics (internal drive)

Height	1.0 inch (25.4 mm)
Length	5.75 inches (146.05 mm)
Width	4.0 inches (101.6 mm)
Weight	15 oz. (425.24 g)
Mounting	6 side holes, #6-32 UNC-2B x 0.22 inch deep

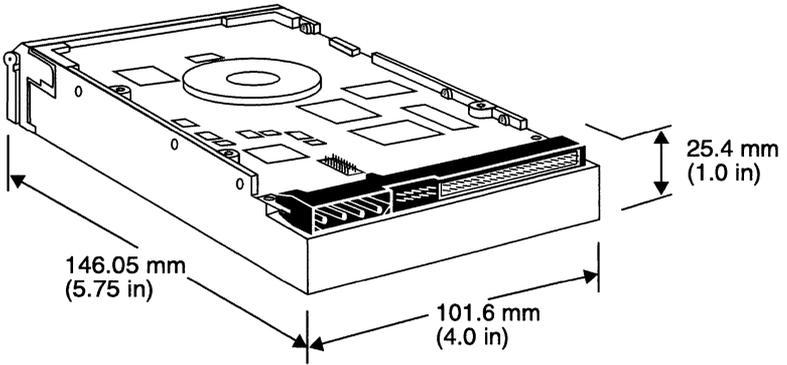


Figure 3-1 Physical Dimensions of the SparQ EIDE Drive (bottom, rear view)

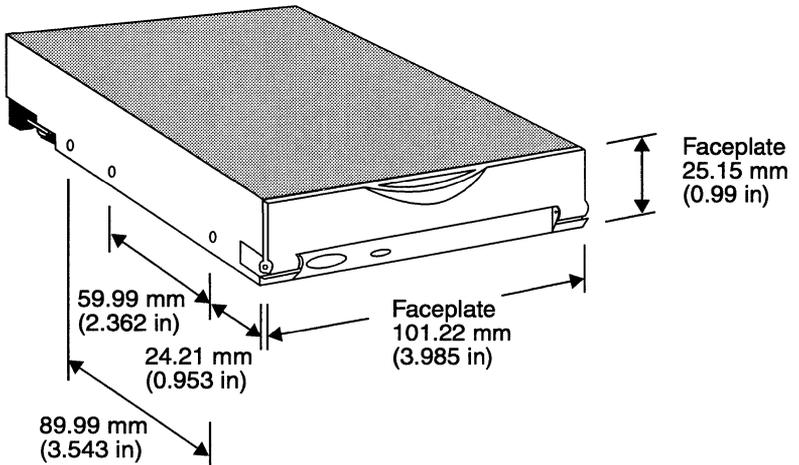


Figure 3-2 Side Mounting Screw Hole Positions and Front Faceplate Dimensions of the SparQ EIDE Drive (top, front view)

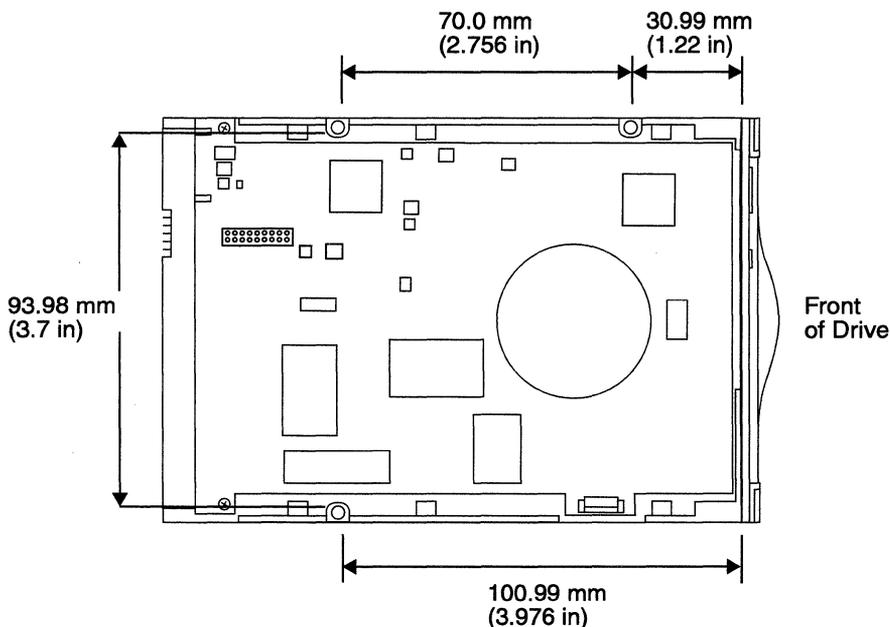


Figure 3-3 Bottom Screw Hole Positions on the SparQ EIDE Drive for Mounting Boot (provided if you use a 5.25-inch mounting bay)

Table 3-4 Power Consumption

Mode	+5V $\pm 5\%$ (avg/max) in Watts	+12V $\pm 5\%$ (avg/max) in Watts
Spin-up	2.5 / 3.5	7.5 / 9.0
Seeking	2.5 / 3.5	8.0 / 9.5
Read/Write	3.0 / 4.0	2.5 / 3.0
Standby park	2.7 / 3.5	2.5 / 3.0
Ripple	100 mv peak to peak	100 mv peak to peak

Performance

Table 3-5 Buffer

Buffer size	512K bytes
-------------	------------

Table 3-6 Seek Times (typical, including settling time)

Track to track	2 msec
Average	12 msec
Maximum	24 msec
Average latency	5.55 msec
Rotational speed ($\pm 0.1\%$)	5400 RPM

Table 3-7 EIDE Data Transfer Rates (from buffer to host)

Mode 4 PIO	16.6 MB/sec
------------	-------------

Table 3-8 Sustained Read/Write Data Transfer Rates (Write-Verify Off)

Maximum	7.0 MB/sec	Extreme OD Read large blocks
Minimum	3.7 MB/sec	Extreme ID Read large blocks
Average	5.8 MB/sec	Calculated average

Table 3-9 Sustained Write Data Transfer Rates (Write-Verify On)

Maximum	2.8 MB/sec	Extreme OD Read large blocks
Minimum	1.3 MB/sec	Extreme ID Read large blocks
Average	2.2 MB/sec	Calculated average

Table 3-10 Spin-Up and Spin-Down

Start time—Spin-up—Ready (including purge and head-loading cycle)	17 sec maximum to Ready 7 sec minimum 14 sec average
Stop time—Spin-down	6 sec typical (30 sec if no power)
Recovery from Sleep mode	3 sec typical

Environmental Characteristics

Table 3-11 Temperature (both internal and external)

Operating	10°C to 45°C
Nonoperating	-40°C to 60°C, humidity non-condensing

Table 3-12 Thermal Gradient

Operating	20°C/hr maximum
Nonoperating	To below condensation

Table 3-13 Relative Humidity

Maximum	32° C (89° F) (max) wet bulb
Operating	8% to 90% noncondensing
Nonoperating	5% to 90% noncondensing

Table 3-14 Altitude (relative to sea level)

Operating	-1,000 to 10,000 ft (-305 to 3,048 m)
Nonoperating	-1,000 to 40,000 ft (-305 to 12,192 m)

Table 3-15 Acoustical Noise (in an anechoic chamber)

Seeking	45 dB maximum at 1 m
Idle	40 dBA maximum at 1 m
No cartridge present	0 dBA

Table 3-16 Electromagnetic Field Immunity

ESD	EN50082-1 IEC801-2 8KV discharge (1000-4-2)
Radiated electric	IEC801-3 3V/m 27-500 GHz (1000-4-3)
Fast transients	IECV801-4 1kV mains, 500V other (1000-4-4)

Table 3-17 Emissions

FCC radiated	Class B CFR47 Part 15 @ 3 m
CISPR radiated	Class B @ 10 m EN55081-1
FCC conducted	Class B 0.45-30 MHz/250mV
CISPR conducted	Class B EN55022

Table 3-18 Magnetic Field (1997 requirement)

Radiated susceptibility	MIL STD 461D RS 101 Limits
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Reliability and Maintainability

Table 3-19 Reliability and Maintainability

MTBF	250,000 hours (POH)
Preventive maintenance	Keep drive door closed.
Data reliability	<1 nonrecoverable error maximum in 10 ¹² bits read
Drive mechanism	20,000 cycles minimum (cartridge insertion and removal)

Table 3-20 Shock (1/2 sine wave pulse at 11 msec)

Operating (without nonrecoverable errors)	3 g, 11 msec, half sine wave pulse (reading or writing)
Nonoperating	80 g, 11 msec, half sine wave pulse (with cartridge removed)

Table 3-21 Vibration

Operating (without nonrecoverable errors)	5 - 10 Hz: 0.048 inch (double amplitude) 10 - 300 Hz: 0.5 g's (peak-to-peak) Sweep time: 1 octave/minute
Nonoperating	2 - 10 Hz: 0.4 inch (peak-to-peak) 10 - 500 Hz: 4 g's (peak-to-peak) Sweep time: 1 octave/minute

The SparQ Cartridge

Cartridge specifications include:

- Physical characteristics
- Environmental characteristics
- Data on reliability

Physical Characteristics

Table 3-22 Capacity

Capacity	Minimum: 1 Gigabyte Formatted: 512-byte sectors
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Table 3-23 Configuration

Number of disks	1
Data surfaces	2
Servo	Embedded Sector
Track density	6,000 tracks per inch
Zones per surface	16
Bytes per block	512
Defects allowed	1000

Table 3-24 Physical Characteristics (cartridge)

Height	0.39 inch (9.9 mm)
Width	3.89 inch (98.8 mm)
Length	3.97 inch (100.84 mm)
Weight	2.5 oz. (70.87 g)

Table 3-25 Physical Characteristics (cartridge case)

Height	0.70 inch (17.78 mm)
Width	5.16 inch (131.06 mm)
Length	4.95 inch (125.73 mm)
Weight	2.3 oz. (65.2 g)

Environmental Characteristics

Table 3-26 Shelf Storage

Nonoperating	-40°C to 60°C, humidity non-condensing
Shelf life	20 years

Table 3-27 Shock

Shock	20-inch (51.28 cm) drop to a linoleum floor (without physical damage or nonrecoverable data errors)
-------	--

Reliability

Table 3-28 Reliability

Cartridge insertion/Removal	10,000 cycles minimum
Preventive maintenance	Keep cartridge in storage case when out of drive, and do not open cartridge door.

4

Installation

This chapter gives instructions for installing the internally mounted SparQ in PC-compatible systems.

Overview

SparQ EIDE drives follow the Enhanced Intelligent Drive Electronics (EIDE) standard. This standard defines an electrical interface used to attach hard drives, CD-ROMs, DVDs, or tape drives to your computer.

You can attach devices to either the primary or secondary EIDE port. Each port provides a 40-pin electrical interface. A flat two-inch (five centimeter) ribbon cable connects an EIDE device (for example, a SparQ 1.0 GB drive) to the EIDE port. You can attach up to two EIDE devices to an EIDE port. Most Pentium class computers have the primary and secondary EIDE ports built into the motherboard. However, some computers use EIDE add-on cards.

NOTE: Non-Pentium class machines typically support the earlier IDE standard. This standard defines a single IDE port that supports the attachment of up to two IDE devices. Although you can attach the SparQ to an IDE controller, this may result in degraded capacity or performance. SyQuest recommends that you attach the SparQ EIDE drive to a non-caching EIDE controller.

Required Hardware

You need the following hardware to install the SparQ:

- A 386™, 486™, or Pentium™ class desktop or tower computer
- An EIDE or IDE controller (on the motherboard or as an add-on card)
- A 40-pin cable that has a maximum length of 18 inches and a free connector for the SparQ EIDE drive
- An empty 3.5-inch or 5.25-inch mounting bay

NOTE: If you wish to use an empty 5.25-inch mounting bay, you need to use the SparQ mounting boot from SyQuest. You may also need accessory mounting rails from your PC manufacturer. The SparQ mounts directly into any 3.5-inch mounting bay.

Required Software

SyQuest supports these operating systems with the SparQ:

- Windows 95 (all versions)
- Windows NT 4.0 or later
- Windows 3.1x

Install the Drive

Use this procedure to install your SparQ and the SyQuest device driver and utilities.

- 1. Run the ADDIDE95 program if you use Windows 95.**
Run SyQuest's ADDIDE95 program to help set up your Windows environment. Insert the *Installation Diskette* into your PC's floppy disk drive. From the Start menu, select Run. Then type A:\ADDIDE95 (or B:\ADDIDE95 if your floppy disk drive is device B) and press the OK button.
- 2. Shut down, unplug, and open your PC.**
- 3. Check your PC's EIDE/IDE configuration.**
Assess the locations of your EIDE/IDE controller port(s) and existing EIDE devices. It is important to identify which are the master and slave devices on each port.
- 4. Decide how to configure your SparQ.**
Typical configurations include installing your SparQ as:
 - Master device on the secondary EIDE port
 - Slave device to your hard drive on the primary EIDE port
 - Slave device to a master device on the secondary EIDE port

Determine the best configuration for your SparQ. In some cases, you may need to relocate or remove an existing EIDE device.

Find a case in this table that matches your existing EIDE configuration. Read the corresponding recommendation.

Case	Primary EIDE Port		Secondary EIDE Port		Recommended Configuration	
	Master Device	Slave Device	Master Device	Slave Device	Controller Port	Jumper Setting
1	Boot Drive	Empty	Empty	Empty	Secondary ¹	Master
2	Boot Drive	CD-ROM or DVD	Empty	Empty	Secondary ¹	Master
3	Boot Drive	Empty	CD-ROM or DVD	Empty	Primary	Slave ²
4	Boot Drive	EIDE Device	CD-ROM or DVD	Empty	Secondary ¹	Slave ^{2,3}
5	Boot Drive	Empty	EIDE Device	EIDE Device	Primary	Slave
6	Boot Drive	EIDE Device	EIDE Device	EIDE Device	Any Position That You Can Free Up ¹	
	Single IDE Port		(Not Applicable)			
7	Boot Drive	Empty			Primary	Slave
8	Boot Drive	EIDE Device			Primary	Slave

¹ If you are using Windows 3.1x, please note that 32-bit access may only be available on the primary EIDE port.

² Alternatively, your SparQ will perform better as master device to a CD-ROM or DVD that is set to slave on the secondary port.

³ If you have a computer built before 1996, your computer may *require* that you change your CD-ROM or DVD to a slave device and install your SparQ as master device on the secondary port.

- 5. Set the Master/Slave jumper on your SparQ.**
Find the jumper pins on the back of your SparQ between the 40-pin EIDE connector and the 4-pin DC power connector.

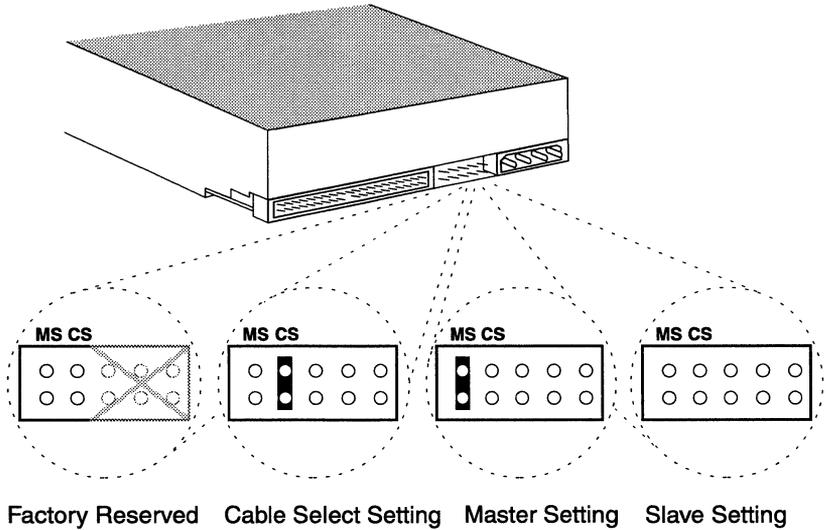


Figure 4-1. Jumper Settings on the SparQ EIDE Drive

Figure 4-1 shows the allowed jumper settings:

- A jumper installed as shown on the master/slave pins, labeled “MS,” sets your SparQ to *master*—your SparQ was packaged in this configuration.
- Remove the master/slave jumper entirely if you wish to set your SparQ to *slave*.

Alternatively, if your PC supports the cable-select function, you may install a jumper on the cable-select pins, labeled “CS.” This overrides the master/slave pins and sets the SparQ to *master* or *slave*, depending on whether the drive is attached to the first or second EIDE cable connector relative to the EIDE controller. Check your EIDE cable type to determine the correct cable connector for master or slave.

CAUTION: Do not use jumper pins identified as *factory reserved* in Figure 4-1. This might cause erratic drive behavior, including loss of data.

6. Reset jumpers on your existing EIDE devices.

If you install your SparQ as the only device on an EIDE cable, then you can skip this step. Other configurations may require that you reset jumpers on your existing EIDE devices:

- If you install your SparQ as the master device to a CD-ROM or DVD drive that was previously set as master, then reset the CD-ROM or DVD drive to *slave*. See the manufacturer’s documentation.
- If you install your SparQ as the slave device to a hard drive built prior to 1996, you may need to change a special jumper called “SP” (for *slave present*) on the hard drive. Hard-drive manufacturers such as Seagate™, Maxtor™, Conner™, Quantum™, Western Digital™, and others, used the SP jumper to acknowledge a slave device on the same EIDE cable. See the manufacturer’s documentation.

7. Prepare a mounting bay and the required cabling.

Remove the cover from the unused 3.5-inch or 5.25-inch mounting bay that you have selected.

Install an 18-inch, three-connector EIDE ribbon cable if you need extra cable length, if you need an extra connector, or if you will be using the secondary EIDE port and it currently has no cable.

NOTE: If you wish to use an empty 5.25-inch mounting bay, attach the SparQ mounting boot and, if necessary, the accessory mounting rails from your PC manufacturer.

8. Mount your SparQ in the mounting bay.

Slide your SparQ through the front opening of the 3.5-inch or 5.25-inch mounting bay and verify that the selected cable connector reaches. Then secure your SparQ (or mounting boot) to the bay while aligning the front of the drive with your other devices:

- To secure your SparQ to a 3.5-inch mounting bay, use three of the machine screws provided. Use two screws on one side of the drive, and one screw on the other.
- To secure your SparQ mounting boot to a 5.25-inch mounting bay, use four of the pointy, self-threading screws provided. Use two screws on each side.

9. Connect the EIDE ribbon cable and DC power cable to your SparQ.

Be sure that you attach the striped edge of the EIDE ribbon cable to pin 1 of your SparQ. Check that all cables are firmly attached.

10. Close, plug in, and turn on your PC.

11. Insert the SparQ cartridge into your SparQ drive.

Slide the cartridge all the way into your SparQ while firmly pressing down on the cartridge tab (the ridge along the edge) until the cartridge snaps into place.

Your SparQ's activity light will flicker green while the cartridge is spinning up. Then the activity light will glow solid green within 30 seconds, indicating that your SparQ is ready.

Problem? If your SparQ's activity light does not glow solid green within 30 seconds; or if your PC hangs, or the system BIOS reports a disk-drive error after a long delay, see "Troubleshooting" on page 4-9.

12. Insert the *Installation Diskette* into your PC's floppy disk drive.

The installation of SyQuest software requires both the cartridge and *Installation Diskette*.

13. Start the installation program as described below and follow the online instructions to install the SyQuest software.

Windows 95 and Window NT 4.0 (or later) Users: Click Start and select Settings, Control Panel, and Add/Remove Programs. Click Install, click Next, then click Finish. Follow the instructions in the Installation Wizard window.

Windows 3.1x Users: Exit Windows and enter DOS. At the DOS prompt, type A:\INSTALL (or B:\INSTALL if your floppy disk drive is device B) and press Enter. Follow the installation program prompts.

Troubleshooting

This section provides solutions for three problem situations.

Problem 1

Your SparQ's activity light does not glow solid green within 30 seconds after you insert a cartridge with the power on.

Solution

- 1. Press your SparQ's eject button to eject the cartridge.**

NOTE: If your SparQ cartridge does not eject, use the eject procedure described under "Problem 3" on page 4-13.

Make sure that you are using a SparQ cartridge, and not a SyJet or other SyQuest cartridge.

- 2. Shut down your PC and fully reinsert the cartridge until it snaps into place. Then turn on your PC.**

Your SparQ's activity light should flicker green while the cartridge is spinning up. Then the activity light should glow solid green within 30 seconds, indicating that your SparQ is ready.

- If the activity light glows solid green within 30 seconds, return to step 12 of the installation procedure.
- If the activity light does not glow solid green within 30 seconds, continue to the next step.

- 3. Shut down, unplug, and open your PC.**

4. Disconnect the EIDE ribbon cable from your SparQ and turn on your PC.

- ***If the activity light does not flicker green*** while the cartridge is spinning up, then either the cartridge has not seated in the drive properly, or your SparQ's DC power connector is not firmly attached. Eject and reinsert the cartridge, and also check your SparQ's power connection.
- ***If the activity light glows solid green*** within 30 seconds, then the EIDE ribbon cable was not firmly attached.
- ***If the activity light continues to flicker green***, but does not glow solid green within 30 seconds, then your SparQ drive or cartridge is probably defective. Call SyQuest Technology's OEM/VAR Technical Support for assistance.

5. Shut down your PC and reconnect the EIDE ribbon cable to your SparQ.

6. After you have corrected the problem, return to step 10 of the installation procedure.

Problem 2

Your PC hangs, or the system BIOS reports a disk-drive error after a long delay.

NOTE: You must correct this problem before you can use your SparQ.

Solution

1. Press your SparQ's eject button to eject the cartridge.

NOTE: If your SparQ cartridge does not eject, use the eject procedure described under "Problem 3" on page 4-13.

2. Shut down, unplug, and open your PC.

3. Check that all EIDE cable connections are secure.

4. Check the Master/Slave settings of your SparQ and other EIDE devices.

- Only one master device and one slave device may be attached to a given primary or secondary EIDE controller port.
- A single device on an EIDE controller port must be set to *master* or *single*, depending on the device. A SparQ set to *master* configures itself as a single device in this case.
- Disk drives, whether fixed or removable, are best configured as master devices to CD-ROMs, tape drives, and so on.
- Review steps 4 through 6 of the installation procedure.

5. Close, plug in, and turn on your PC.
6. Start your PC's CMOS Setup (during system boot) and check that the parameters for your SparQ are correct. Most CMOS Setup programs automatically detect and update the values for CMOS parameters when you add a new drive.

These are the correct values for your SparQ.	
CMOS Parameter	Value
Logical Block Addressing (LBA) mode	Yes
Multiple Sector Read/Write	<i>Highest number allowed</i>
Fast Programmed I/O mode	<i>Highest number allowed</i>
Cylinders	1945
Heads	16
Sectors	63
Write Precomp / Landing Zone	<i>Any valid number</i>

7. After you have corrected the problem, return to step 11 of the installation procedure.

Problem 3

You need to remove the cartridge from your SparQ because the eject button does not work or you have no power to your computer.

Solution

WARNING: *Never* manually remove a cartridge as described here while the activity light is solid green or flickering. Damage may result to both drive and cartridge, and you will void your warranty.

Use this eject procedure—*wait 45 seconds* after the last drive access. It is safest to power off your computer first. Then open the drive door, gently lift the cartridge tab, and pull the cartridge out of your SparQ.

5

EIDE Interface Protocol

This chapter describes the EIDE interface protocol between PC host systems and the SparQ:

- The standard used
- Physical and electrical characteristics
- Signal characteristics
- General operational requirements
- Self-Test routines
- Interface register descriptions
- Timing measurements

See Chapter 6 for SparQ EIDE command descriptions.

The Standard

The EIDE interface protocol maintains a high degree of compatibility with the *AT Attachment-4 Interface standard (ATA-4)*.

Physical/Electrical Characteristics

This section describes the following:

- The 40-pin interface connector and 4-pin DC power connector
- Jumper configurations
- Cable configuration
- EIDE I/O cable requirements
- DC and AC characteristics of the interface signals

The 40-Pin and 4-Pin Connectors

Table 5-1 identifies the interface signal for each pin of the 40-pin interface connector:

Table 5-1 40-Pin Connector Interface Signals

Connector Pin	Signal Name	Connector Pin	Signal Name
1	RESET-	2	Ground
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	Ground	20	(keypin)
21	DMARQ (unused)	22	Ground

Table 5-1 40-Pin Connector Interface Signals (Continued)

Connector Pin	Signal Name	Connector Pin	Signal Name
23	DIOW-	24	Ground
25	DIOR-	26	Ground
27	IORDY	28	CSEL
29	DMACK- (unused)	30	Ground
31	INTRQ	32	Reserved
33	DA1	34	PDIAG-
35	DA0	36	DA2
37	CS0-	38	CS1-
39	DASP-	40	Ground

When the SparQ is connected to the 40-pin interface cable, the drive receives DC power through the 4-pin DC power connector. Table 5-2 identifies the power-line voltage for each pin of the 4-pin connector:

Table 5-2 DC Interface Using 4-Pin Power Connector

Power-Line Designation	Pin Number
+12 Volts	1
+12 Volt return	2
+5 Volt return	3
+5 Volts	4

Figure 5-1 shows the drive-side connector pin numbering:

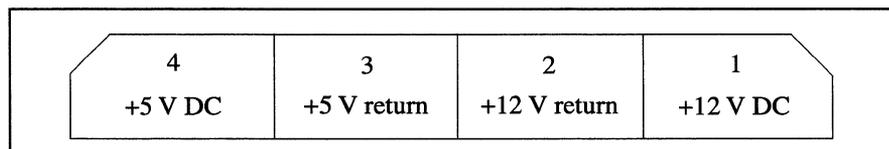


Figure 5-1 Drive-side Connector Pin Numbering

Jumper Configurations

The jumper pins (a total of 10) on the SparQ are located on the back edge of the PCBA between the 40-pin EIDE connector and the 4-pin DC power connector, as shown in Figure 4-1 on page 4-5.

The SparQ supports two jumper positions for users:

- The master/slave position, labeled “MS.”
- The cable-select position, labeled “CS.”

CAUTION: Do not use jumper pins identified as *factory reserved* in Figure 4-1. This might cause erratic drive behavior, including loss of data.

The Master/Slave Position

Install a jumper in the master/slave position (connecting the pins labeled “MS”) to configure the SparQ as a *single* or *master* disk drive. The SparQ will search for a slave device (disk drive or CD ROM) at power on. If the SparQ finds a slave device, it will perform the master function. If no slave device is found, the SparQ configures itself as a single (the only) device on the EIDE port.

Remove the jumper from the master/slave position (or leave it on only one of the two pins) to configure the SparQ as *slave*.

NOTE: A master drive, slave drive, and EIDE controller (or motherboard) may be attached in any order to any of the three connectors of an EIDE cable, but *only* if the cable-select function is not used.

The Cable Select Position

Install a jumper at the cable-select position (connecting the pins labeled “CS”) to configure the SparQ as *master* or *slave*, depending on whether it is attached to the first or second EIDE cable connector relative to the EIDE controller (or motherboard). The EIDE cable type determines the correct cable connector for master or slave. For this function to operate properly, the host PC must support the cable-select function.

NOTE: When a jumper is installed at the cable-select position, the presence or absence of a jumper at the master/slave position is ignored, as shown in Table 5-3. Cable type and the connector you use determine master or slave identity.

Table 5-3 Jumper Settings on the SparQ EIDE Drive

SparQ Configuration	MS Jumper	CS Jumper
Single or Master	On	Off
Slave	Off	Off
Master or Slave	On (ignored)	On
Master or Slave	Off (ignored)	On

Cable Configuration

The ATA-4 specification defines an interface with a single interface cable and one or two attached disk drives. If two disk drives are connected to the interface, they are connected in a daisy-chained configuration. This configures one drive as *master* and the other drive as *slave*. The same is true for a second interface (EIDE) cable if used.

EIDE I/O Cable Requirements

The cable specification affects system-data integrity:

- The cable's total length must not exceed 0.46 m (18 in).
- The cable's capacitance must not exceed 35 pf.

DC and AC Characteristics

Table 5-4 defines DC characteristics of the interface signals:

Table 5-4 DC Characteristics

Description		Min	Max
I_{oL}	Driver sink current ¹	4 mA	
I_{oH}	Driver source current ²	400 μ A	
V_{iH}	Voltage input high	2.0 V DC	
V_{iL}	Voltage input low		0.8 V DC
V_{oH}	Voltage output high ($I_{oH} = -400 \mu$ A)	2.4 V DC	
V_{oL}	Voltage output low ($I_{oL} = 12$ mA)		0.5 V DC
Notes:			
¹ I_{oL} for DASP must be 12 mA min to meet legacy timing and signal integrity.			

Table 5-5 defines AC characteristics of the interface signals:

Table 5-5 AC Characteristics

Description		Min	Max
tRISE	Rise time for any signal on AT interface ¹	5 ns	
tFALL	Fall time for any signal on AT interface ¹	5 ns	
Cin	Host input capacitance		25 pf
Cout	Host output capacitance		25 pf
Cin	SparQ input capacitance		20 pf
Cout	SparQ output capacitance		20 pf
Note: ¹ tRISE and tFALL are measured from 10 - 90% of full signal amplitude with a total capacitive load of 40 pf.			

Signal Characteristics

The physical interface consists of receivers and drivers communicating through conductors using an asynchronous interface protocol. Table 5-6 defines the signal names:

Table 5-6 Interface Signal-Name Assignments

Description	Host	Dir	Dev	Acronym
Cable select		1		CSEL
Chip select 0		→		CS0-
Chip select 1		→		CS1-
Data bus bit 0		↔		DD0
Data bus bit 1		↔		DD1
Data bus bit 2		↔		DD2
Data bus bit 3		↔		DD3

Table 5-6 Interface Signal-Name Assignments (Continued)

Description	Host	Dir	Dev	Acronym
Data bus bit 4		↔		DD4
Data bus bit 5		↔		DD5
Data bus bit 6		↔		DD6
Data bus bit 7		↔		DD7
Data bus bit 8		↔		DD8
Data bus bit 9		↔		DD9
Data bus bit 10		↔		DD10
Data bus bit 11		↔		DD11
Data bus bit 12		↔		DD12
Data bus bit 13		↔		DD13
Data bus bit 14		↔		DD14
Data bus bit 15		↔		DD15
Device active or slave (device 1) present		1		DASP-
Device address bit 0		→		DA0
Device address bit 1		→		DA1
Device address bit 2		→		DA2
Interrupt request		→		INTRQ
I/O read		→		DIOR-
I/O ready		→		IORDY
I/O write		→		DIOW-
Passed diagnostics		1		PDIAG-
Reset		→		RESET-
Note:				
¹ See Table 5-7 for information on the source of these signals.				

Table 5-7 provides descriptions for the signals summarized in the previous table:

Table 5-7 Signal Descriptions

Acronym	Description
CS0- (chip select 0)	Chip select signal from the host used to select the Command Block registers
CS1- (chip select 1)	Chip select signal from the host used to select the Control Block registers
DA2, DA1, DA0 (device address)	Three-bit binary coded address asserted by the host to access a register or data port in the device
DASP- (device active, device 1 present)	Time-multiplexed signal that indicates a device is active, or that Device 1 is present
DD(15:0) (device data)	Eight or 16-bit bidirectional-directional data interface between the host and the device. The lower eight bits are used for eight-bit register transfers.
DIOR- (device I/O read)	Strobe signal asserted by the host to read device registers or the data port
DIOW- (device I/O write)	Strobe signal asserted by the host to write device registers or the data port
INTRQ (device interrupt)	Signal used by the selected SparQ to interrupt the host system
IORDY (I/O channel ready)	Signal that is negated to extend the host transfer cycle of any host register access (Read or Write) when the SparQ is not ready to respond to a data transfer request
PDIAG- (passed diagnostics)	Signal that must be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics
RESET- (device reset)	Signal, referred to as the hardware reset, that must be used by the host system to reset the SparQ
CSEL ¹ (cable select)	Value that designates the SparQ as either Device 0 or Device 1. If CSEL is negated, then the SparQ address is 0; if CSEL is asserted, then the SparQ address is 1.
<p>Note: ¹ Special cabling can be used by the system manufacturer to selectively ground CSEL.</p>	

General Operational Requirements

This section describes the following:

- Command delivery
- Sector addressing for register delivered data-transfer commands
- Reset responses
- The power-management feature set
- The removable media feature set

Command Delivery

All commands and command parameters are delivered by writing the SparQ Command Block registers.

Sector Addressing

For register delivered data-transfer commands, all addressing of data sectors recorded on the SparQ media uses a logical sector address. There is no implied relationship between logical sector addresses and the actual physical location of the data sector on the media.

You can address the SparQ in two ways:

- Cylinder, Head, Sector (CHS) addressing mode
- Logical Block Addressing (LBA) mode

The SparQ uses the addressing method specified in the Command Block. The drive will return status information that utilizes the addressing method specified for the command.

CHS Addressing Mode

A CHS address is made up of three fields:

- The cylinder number
- The head number
- The sector address

The default CHS configuration of the SparQ is 1,945 cylinders, 16 heads, and 63 sectors per track.

When the host selects CHS translation using the command Initialize Device Parameters, it requests the number of sectors per logical track and the number of heads per logical cylinder. The SparQ then computes the number of logical cylinders available in the requested translation.

LBA Mode

The LBA mode addresses sectors with a sector-unique number. The SparQ will access a number of sectors equal to the current CHS configuration. The default number is 1,961,069.

LBA mode is supported as follows:

- The host may use either the currently selected CHS translation addressing, or LBA addressing on a command-by-command basis by using the LBA bit in the Device/Head register
- The LBA bit of the Device/Head register is ignored for commands that do not access the media

- Logical sectors on the SparQ are linearly mapped such that the first LBA-addressed sector (sector 0) is the same as the first logical CHS-addressed sector (cylinder 0, head 0, sector 1). The LBA address of a given logical sector does not change, irrespective of which logical CHS translation is active.

The following is always true:

$$\text{LBA} = ((\text{cylinder} * \text{heads_per_cylinder} + \text{heads}) * \text{sectors_per_track}) + \text{sector} - 1$$

where *heads_per_cylinder* and *sectors_per_track* are the current translation values.

Reset Responses

The interface supports three types of reset responses:

Power-On Reset. Executed at power on, the SparQ runs a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parameters, and sets default values.

Hardware Reset. Executed in response to the assertion of RESET-, the SparQ runs a series of electrical circuitry diagnostics and resets to default values.

Software Reset. Executed in response to the setting of the SRST bit in the Device Control register, the SparQ resets the interface circuitry.

Power-Management Feature Set

The SparQ uses power-management features.

The power-management feature set permits a host to modify the SparQ's behavior to reduce the power required to operate. The feature set includes commands and a timer that enable the drive to use low power-consumption modes. You can disable these features as well.

The SparQ uses this set of functions to manage power:

- The commands Check Power Mode, Idle, Idle Immediate, Sleep, Standby, and Standby Immediate
- A Standby Timer that you can set and enable or disable with the Idle or Standby command

Power Modes

Four power modes provide these drive-response and power-consumption characteristics:

Active mode. The SparQ is capable of responding to commands. During the execution of a media-access command, the drive is in Active mode. Power consumption is greatest in this mode.

Idle mode. The SparQ is capable of responding to commands, but may take slightly longer (typically, about 200 msec) to complete commands than when in the Active mode. Power consumption may be less than that of Active mode.

Standby mode. The SparQ is capable of responding to commands, but may take longer to complete commands than when in the Idle mode. Response time is typically about three seconds, but may be up to 15 seconds. Power consumption may be less than that of Idle mode.

Sleep mode. The SparQ automatically enters Sleep mode after 30 minutes of inactivity, and then returns to Active mode upon any drive access. Recovery from Sleep mode is typically about three seconds, but may be up to 15 seconds. Power consumption is least in Sleep mode.

NOTE: In Sleep Mode, the drive's interface is not active. The content of the Status register is invalid in this mode.

Standby Timer

The Standby Timer allows the SparQ to automatically enter Standby mode from either Active or Idle mode. This change of mode occurs after a host-programmed period of inactivity.

If the Standby Timer is enabled and the drive is in Active or Idle mode, the drive automatically enters Standby mode if no command is received during the specified time period.

If the Standby Timer is disabled, the drive cannot automatically enter Standby mode.

Power-Management Commands

You may use these commands to determine and change the current power mode of the SparQ:

Check Power Mode. This command allows a host to determine if the SparQ is currently in, going to, or leaving Idle or Standby mode.

Idle and Idle Immediate. These commands immediately move a SparQ from the Active or Standby mode to Idle mode. The Idle command also enables or disables the Standby Timer and sets the Standby-Timer count.

Sleep. This command moves a SparQ to Sleep mode. The drive's interface becomes inactive at the completion of the Sleep command. A reset is required to move the drive out of Sleep mode.

Standby and Standby Immediate. These commands immediately move a SparQ from the Active or Idle mode to Standby mode. The Standby command also enables or disables the Standby Timer and sets the Standby-Timer count.

Power-Mode Transitions

Figure 5-2 shows the drive's power-transition paths:

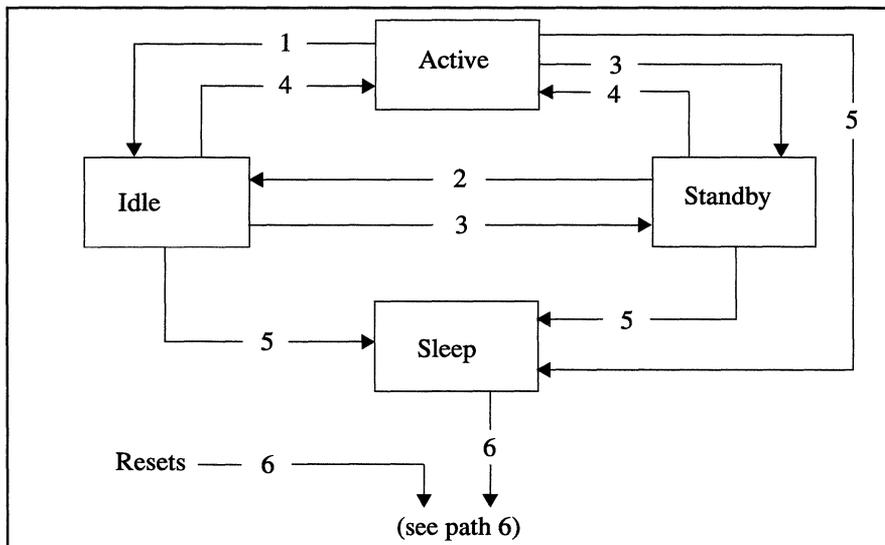


Figure 5-2 Power-transition Paths

Path 1: The command Idle or Idle Immediate, or a vendor-specific implementation, moves the drive to Idle mode.

Path 2: The command Idle or Idle Immediate moves the drive to Idle mode.

Path 3: The command Standby or Standby Immediate, a vendor-specific implementation, or Standby-Timer expiration, moves the drive to Standby mode.

Path 4: A media-access command moves the drive to Active mode.

Path 5: The Sleep command moves the drive to Sleep mode.

Path 6: A hardware or software Reset moves the drive to Active, Idle, or Standby mode, as specified by the vendor.

Removable Media Feature Set

The SparQ uses removable media features.

The removable media feature set includes these commands to support the insertion and removal of media:

- Door Lock
- Door Unlock
- Media Eject
- Media Status
- Set Features (subcommand 95h, Enable media status notification)
- Set Features (subcommand 31h, Disable media status notification)

This command set works with a variety of host PC systems. Host systems vary in level of acknowledgment for the existence of removable media disk drives such as the SparQ.

The SparQ supports two modes of media operation: Default mode and Media-Status Notification mode.

Default Mode

In Default mode, the SyQuest device driver prevents the user from inadvertently ejecting the media during media access operations. The driver locks and unlocks the front-panel eject button when the host PC is using the media. The host operating system has no knowledge of the removable nature of SparQ media, and the device driver facilitates orderly media interchange.

Media-Status Notification Mode

When Media-Status Notification (MSN) mode is enabled with the Set Features command, the host operating system assumes complete control of the media interchange.

When MSN mode is enabled, the front-panel eject button and the commands Door Lock and Door Unlock are disabled. The SparQ will respond to these commands with a *good* status, but no action is taken.

The operating system monitors media status and takes action as required in response to the Media Status command. If the user pushes the eject button, this request is passed to the operating system via the Media Status command. Then the operating system initiates an orderly eject sequence by flushing its data buffers and issuing a Media Eject command to the drive.

Refer to the command descriptions in Chapter 6 for more details.

Self-test Routines

The SparQ firmware resides in the Flash ROM mounted on the main logic board. The firmware contains all the routines necessary to execute the supported EIDE commands, run the microcontroller, and perform the self-test routines. The EIDE commands are described in Chapter 6 of this manual. The self-test power-up routines are described in this section.

Power-up Test

When power is applied to the drive, the start-up routines in the SparQ Flash ROM execute a series of tests on the drive's electronic components to establish the readiness of the drive.

The first test is a checksum operation on the SparQ Flash ROM. If this test passes, a series of reads and writes test the microcontroller registers, internal RAM, and scratch pad RAM. When these tests are completed and passed by the microcontroller, a read/write test is performed on the buffer RAM. After completion of this test, the drive performs a series of self-calibration routines and then becomes ready.

Self-Test Routine Error Reporting

The SparQ provides failure error information for its power-up sequence through an LED on the drive's front panel. The error codes are displayed as a sequence of red flashes. The flashing sequence will repeat continuously with a wait period of two seconds between each sequence. Table 5-8 shows the binary flash code and number of red LED flashes corresponding to each type of error.

Table 5-8 *Flash Codes for Power-Up Sequence*

Flash Code	Number of Red Flashes	Type of Firmware-Detected Error
01	1	Flash Check Sum Error
02	2	External RAM Error
03	3	Buffer Test Error
04	4	Sequencer Error

Call SyQuest Technology's OEM/VAR Technical Support if you observe an error. You may need to replace the SparQ.

Interface Register Descriptions

This section describes the addressing characteristics and I/O registers of the SparQ.

Addressing Characteristics

Data transfers occur in parallel between host memory and the SparQ buffer under the direction of commands from the host. The drive performs all operations required to properly read data from, or write data to, the media. Data read from the media is stored in the drive's buffer pending transfer to host memory. Conversely, the host memory transfers data to the drive buffer to be written to the media.

The host computer programs the SparQ to perform commands, and then returns status to the host at command completion. When two SparQs are daisy-chained on the interface, the host writes commands in parallel to both drives. However, with exception to the command Execute Device Diagnostics, only the selected drive executes a command. When the command Execute Device Diagnostics addresses Device 0, both SparQs execute the command, and Device 1 posts its status to Device 0 by using the passed diagnostics (PDIAG-) signal.

The DEV bit (bit 4) of the Device/Head register selects the SparQ:

- When the DEV bit is set to zero, Device 0 is selected.
- When the DEV bit is set to one, Device 1 is selected.
- When SparQs are daisy-chained, one is set as Device 0, and the other is set as Device 1.

See "Device/Head Register" on page 5-27 for further details.

I/O Registers

I/O registers for the SparQ include:

- Command-block registers, used for sending commands to the SparQ, or for posting status from the drive
- Control-block registers, used to control the SparQ and to post alternate status

All communication to or from the SparQ is through an I/O register. The I/O register routes input or output data to or from registers addressed by signals from the host. These signals include CS0-, CS1-, DA(2:0), DIOR-, and DIOW- (described in Table 5-7 on page 5-9).

Host signals result in valid or invalid addresses as follows:

- When both CS0- and CS1- are asserted or negated, this results in an *invalid* (not used) address.
- When CS0- is negated and CS1- is asserted, the only *valid* address is DA(2:0) with a value of 6h.

In this case, the SparQ holds DD(15:0) in the high-impedance state and ignores DIOR- and DIOW-.

Valid addresses for each I/O register are given in the sections that follow.

Format for Register Descriptions

Each register description that follows uses this format:

Address. Gives the valid CS and DA address of the register

Direction. Indicates if the register is read/write, read only, or write only from the host

Access Restrictions. Indicates when the register may be accessed

Effect. Indicates the effect of accessing the register

Function. Describes the function of the register

Content. Provides a Field/Bit description of the register, when applicable

Alternate Status Register

Address. CS(1:0)=1h, DA(2:0)=6h

Direction. This is a read-only register. If the host tries to write to this address, the Device Control register is written to instead.

Access Restrictions. When the BSY bit is set to zero, the other bits in this register are valid. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. Reading this register does not perform an interrupt-acknowledge function, or clear a pending interrupt.

Function. This register contains the same information as the Status register in the command block.

Content. See “Status Register” on page 5-30 for definitions of the bits in this register.

Command Register

Address. CS(1:0)=2h, DA(2:0)=7h

Direction. This is a write-only register. If the host tries to read this address, the Status register is read instead.

Access Restrictions. The host writes to this register only when both BSY and DRQ are set to zero. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. Command processing begins when this register is written. The content of the command-block registers become parameters of the command when this register is written. Writing this register clears any pending interrupt condition.

Function. This register contains the command code being sent to the SparQ. Command execution begins immediately after this register is written. See Chapter 6 for the executable commands, command codes, and required parameters for each command.

Content. A Field/Bit description follows:

7	6	5	4	3	2	1	0
Command Code							

Cylinder High Register

Address. CS(1:0)=2h, DA(2:0)=5h

Direction. This is a read/write register.

Access Restrictions. The host writes to this register only when both BSY and DRQ are set to zero. If the host writes to this register when BSY or DRQ is set to one, the result is indeterminate. Register contents are valid only when both BSY and DRQ are set to zero. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

Function. This register has command-dependent content. See Chapter 6.

Cylinder Low Register

Address. CS(1:0)=2h, DA(2:0)=4h

Direction. This is a read/write register.

Access Restrictions. The host writes to this register only when both BSY and DRQ are set to zero. If the host writes to this register when BSY or DRQ is set to one, the result is indeterminate. Register contents are valid only when both BSY and DRQ are set to zero. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

Function. This register has command-dependent content. See Chapter 6.

Data Register

Address. CS(1:0)=2h, DA(2:0)=0h

Direction. This is a read/write register.

Access Restrictions. The host writes to this register, and the register contents are valid when read, only if DRQ is asserted. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. PIO data-out transfers are processed by a series of reads to this register, each read transferring the data that follows the previous read. PIO data-in transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write.

The results of a read during a PIO-in, or a write during a PIO-out, are indeterminate.

Function. This register is 16-bits wide.

Content. A Field/Bit description follows:

15	14	13	12	11	10	9	8
Data (15:8)							

7	6	5	4	3	2	1	0
Data (7:0)							

Device Control Register

Address. CS(1:0)=1h, DA(2:0)=6h

Direction. This is a write-only register. If the host tries to read this address, the Alternate Status register is read instead.

Access Restrictions. None.

Effect. The content of this register takes effect when written.

Function. This register allows a host to software-reset attached SparQs, and to enable/disable interrupts.

Content. A Field/Bit description follows:

7	6	5	4	3	2	1	0
r	r	r	r	r	SRST	nIEN	0

- Bits 7 through 3 are reserved.
- Bit 2, SRST, is the host software-reset bit.
- Bit 1, nIEN, is the Enable bit for the SparQ interrupt to the host.

When the nIEN bit is set to zero and the SparQ is selected, INTRQ is enabled through a tri-state buffer. When the nIEN bit is set to one, or the SparQ is not selected, INTRQ is in a high-impedance state.

- Bit 0 is written with zero.

Device/Head Register

Address. CS(1:0)=2h, DA(2:0)=6h

Direction. This is a read/write register.

Access Restrictions. The host writes to this register only when both BSY and DRQ are set to zero. If the host writes to this register when BSY or DRQ is set to one, the result is indeterminate. Register contents are valid only when both BSY and DRQ are set to zero. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. The DRV bit becomes effective when this register is written. All other bits in this register become a command parameter when subsequent commands are written to the Command register.

Function. The DEV bit (bit 4) of this register selects the SparQ. A value of zero selects device 0. A value of 1 selects Device 1. Other bits in this register are command-dependent bits. See Chapter 6.

Error Register

Address. CS(1:0)=2h, DA(2:0)=1h

Direction. This is a read-only register. If the host tries to write to this address, the Features register is written to instead.

Access Restrictions. The contents of this register are valid when BSY and DRQ are set to zero and ERR is set to one, upon completing power on or reset, and upon completing the Execute Device Diagnostics command. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. None.

Function. This register contains status for the current command. Following power on, reset, or completion of an Execute Device Diagnostics command, this register contains a diagnostic code. At the completion of any command except Execute Device Diagnostics, the contents of this register are valid when the ERR bit is set to one in the Status register.

Content. A Field/Bit description follows:

7	6	5	4	3	2	1	0
r		MC		MCR	ABRT		

- Bit 7 is reserved.
- Bit 5, MC (media changed), is used by removable media SparQs to indicate that new media is available to the operating system.
- Bit 3, MCR (media change requested), is used by removable media SparQs to indicate that a request for media removal has been detected.
- Bit 2, ABRT (aborted command), indicates a requested command has been aborted because the command code or a command parameter is invalid, or because some other error has occurred.
- Other bits in this register are command-dependent bits. See Chapter 6.

Features Register

Address. CS(1:0)=2h, DA(2:0)=1h

Direction. This is a write-only register. If the host tries to read this address, the Error register is read instead.

Access Restrictions. The host writes to this register only when both BSY and DRQ are set to zero. If the host writes to this register when BSY or DRQ is set to one, the result is indeterminate.

Effect. Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

Function. This register has command-dependent content. See Chapter 6.

Sector Count Register

Address. CS(1:0)=2h, DA(2:0)=2h

Direction. This is a read/write register.

Access Restrictions. The host writes to this register only when both BSY and DRQ are set to zero. If the host writes to this register when BSY or DRQ is set to one, the result is indeterminate. Register contents are valid only when both BSY and DRQ are set to zero. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

Function. This register has command-dependent content. See Chapter 6.

Sector Number Register

Address. CS(1:0)=2h, DA(2:0)=3h

Direction. This is a read/write register.

Access Restrictions. The host writes to this register only when both BSY and DRQ are set to zero. If the host writes to this register when BSY or DRQ is set to one, the result is indeterminate. Register contents are valid only when both BSY and DRQ are set to zero. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

Function. This register has command-dependent content. See Chapter 6.

Status Register

Address. CS(1:0)=2h, DA(2:0)=7h

Direction. This register is read only. If the host tries to write to this address, the Command register is written to instead.

Access Restrictions. The contents of this register, except for BSY, are ignored when BSY is set to one. BSY is valid at all times. The contents of this register and all other command-block registers are invalid while the SparQ is in Sleep mode.

Effect. Reading this register when an interrupt is pending causes the interrupt to be cleared.

Function. This register contains the SparQ-drive status. The contents of this register are updated to reflect the current state of the drive, and the progress of any command being executed by the drive. When the BSY bit is set to zero, other bits in this register are valid. When the BSY bit is set to one, other bits in this register are invalid.

Content. A Field/Bit description follows:

7	6	5	4	3	2	1	0
BSY	DRDY			DRQ	CORR		ERR

- Bit 7, BSY (busy), is set to one when the SparQ has control of the command-block registers. When the BSY bit is set to one, the drive ignores any write from the host to a command-block register, except for the Device Reset command.

The drive does not change the state of the DRQ bit unless the BSY bit is set to one. The only exception is when the last block of a register-delivered, PIO data-in command has been transferred by the host. Then the DRQ bit is cleared to zero without the BSY bit being set to one.

When the BSY bit is set to zero, the drive may only change the IDX, DRDY, DF, and CORR bits in the Status and Data registers. The drive cannot change the other command-block registers, or other bits within the Status register.

After the host has written to the Command register, either the BSY bit is set to one, or, if the BSY bit is cleared to zero, the DRQ bit is set to one. This remains true until command completion.

NOTE: The BSY bit is set to one and then cleared to zero so quickly, that host detection of the BSY bit being set to one is uncertain.

The BSY bit is set to one by the SparQ in these circumstances:

- After either the negation of RESET-, or the setting of the SRST bit to one in the Device Control register
- After writing to the Command register, if the DRQ bit is not set to one
- Between blocks of a data transfer during PIO data-in commands, if the DRQ bit is not set to one
- After the transfer of a data block during PIO data-out commands, if the DRQ bit is not set to one

The drive does not set the BSY bit to one at any other time.

- Bit 6, DRDY (device ready), is set to one to indicate that the SparQ is capable of accepting all command codes. This bit is cleared to zero at power on.

When the DRDY bit is set to zero, the drive responds as follows:

- The drive accepts and attempts to execute the commands Execute Device Diagnostics and Initialize Device Parameters
- DRDY is set to one before the host issues any command to the device, except for the commands Execute Device Diagnostics and Initialize Device Parameters.

- Bit 5 has command-dependent content. See Chapter 6.
- Bit 4 has command-dependent content. See Chapter 6.
- Bit 3, DRQ (data request), indicates that the drive is ready to transfer a word or byte of data with the host. When the drive is ready to transfer data, DRQ is set to one and BSY is cleared to zero. DRQ is cleared to zero when the last word of the data transfer occurs. For some data-transfer protocols, BSY may be set to one before clearing DRQ to zero.
- Bit 2, CORR, is obsolete.
- Bit 1 has command-dependent content. See Chapter 6.
- Bit 0, ERR (error), indicates that an error occurred during execution of the previous command. The bits in the Error register have more information about the cause of the error.

Once the drive has set the error bit to one, it cannot change the contents of the following items until a new command has been accepted, the SRST bit is set to one, or RESET- is asserted:

- Cylinder High register
- Cylinder Low register
- Device/Head register
- Error register
- Sector Count register
- Sector Number register
- The ERR bit in the Status register

Timing

This section describes the cable deskewing requirement and presents a timing diagram for register and PIO data transfers between the SparQ and the host computer.

Cable Deskewing

The SparQ provides cable deskewing for all signals originating at the host. Conversely, the host must provide cable deskewing for all signals originating from the drive.

The timing diagram and depicted values that follow are measured at the SparQ interface connector. No values are given for measurement at the host interface.

Transfer Timing

The minimum cycle time supported by the SparQ is 120 ns, PIO Mode 4.

Figure 5-3 shows the timing relationships between interface signals for register and PIO data transfers. The footnotes for this figure are on the next page:

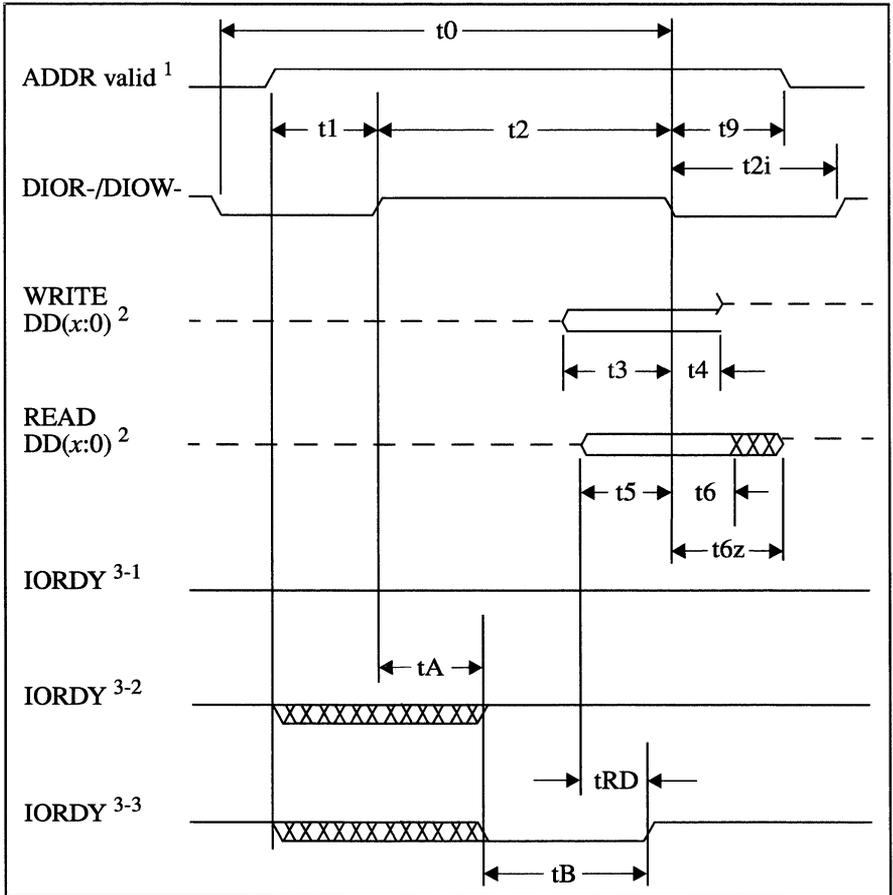


Figure 5-3 Timing Measurements

Notes:

- ¹ The device address consists of signals CS0-, CS1-, and DA(2:0).
- ² Data consists of DD(x :0), where $x = 15$ for PIO data transfers, and $x = 7$ for register transfers.
- ³ The negation of IORDY by the device is used to extend the PIO cycle. The host determines whether to extend the cycle after tA from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
 - ³⁻¹ The device never negates IORDY. No wait is generated.
 - ³⁻² The device negates IORDY before tA , but causes IORDY to be asserted before tA . No wait is generated.
 - ³⁻³ The device negates IORDY before tA . A wait is generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device places read data for tRD on DD(x :0) before asserting IORDY (where $x = 15$ for PIO data transfers, and $x = 7$ for register transfers).

6

EIDE Command Reference

The host issues commands to SparQ EIDE disk drives by loading pertinent registers with needed parameters into the command block, and then writing the command code to the Command register.

This chapter begins with a summary that lists all commands and command codes for the SparQ. Following this is a detailed description for each command.

Command Summary

Table 6-1 lists all command codes with page references for finding command descriptions:

Table 6-1 Command Summary

Code	Command	Description
E5h	Check Power Mode	See page 6-4
DEh	Door Lock	See page 6-6
DFh	Door Unlock	See page 6-9
92h	Download Microcode	See page 6-11

Table 6-1 Command Summary (Continued)

Code	Command	Description
90h	Execute Device Diagnostics	See page 6-13
ECh	Identify Device	See page 6-15
E3h	Idle	See page 6-21
E1h	Idle Immediate	See page 6-24
91h	Initialize Device Parameters	See page 6-26
EDh	Media Eject	See page 6-28
DAh	Media Status	See page 6-30
00h	NOP	See page 6-32
C4h	Read Multiple	See page 6-34
20h or 21h	Read Sector(s)	See page 6-39
40h or 41h	Read Verify Sector(s)	See page 6-42
F8h, FBh, or FCh	Reassign Sector	See page 6-45
70h	Seek	See page 6-47
EFh	Set Features	See page 6-50
C6h	Set Multiple Mode	See page 6-54
E6h	Sleep	See page 6-57
E2h	Standby	See page 6-59
E0h	Standby Immediate	See page 6-62
F0h	SyQuest Set Features	See page 6-64
C5h	Write Multiple	See page 6-68
C0h	Write Protect Enable/Disable	See page 6-72
30h or 31h	Write Sector(s)	See page 6-74

Command Descriptions

Each command description in this section includes the following information:

Command Code. The code (in parentheses next to each command). Table 6-1 lists all command codes and provides page references.

Inputs. The command-block register data supplied by the host

Normal Outputs. The command-block register data returned by the SparQ at command completion. The Status register is always valid.

Error Outputs. The command-block register data returned by the SparQ when a command completes with an unrecoverable error

Prerequisites. Any required commands or conditions that must be met before the host can issue the command

Description. An account of the command's functions

NOTE: The occurrence of *na* in this chapter's tables indicates that the content of a particular bit or field is not applicable to the command.

Check Power Mode (E5h)

Inputs

Table 6-2 Check Power Mode—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	E5h							

Normal Outputs

The Sector Count register is written with a value of 0 (00h) if the drive is in Standby mode. This register may be written with a value of 255 (FFh) if the drive is in Idle mode.

Table 6-3 Check Power Mode—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	Result value							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Sector Count result value:

- 00h - The drive is in Standby mode.
- FFh - The drive is in Idle mode.

Error Outputs

Table 6-4 Check Power Mode—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	Result value							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command allows the host to determine the current power mode of the drive.

Door Lock (DEh)

Inputs

Table 6-5 Door Lock—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	DEh							

Normal Outputs

Table 6-6 Door Lock—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

If the drive is already locked and the media-change request button is active, then a Media Change Requested status is returned. It is returned by setting the MCR bit to one in the Error register and the ERR bit to one in the Status register.

Table 6-7 Door Lock—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	MCR	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- MCR indicates that the drive is already locked and the media-change request button is active.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if the Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command either locks the drive or media, or provides the status of the media-change request button.

If the drive is not locked, the drive is set to the locked state and no error is set to one.

If the drive is locked, the status returned is for the media change request button. No error is set to one while the media change-request button is inactive. The MCR bit in the Error register and the ERR bit in the Status register are set to one when the media-change request button is active.

When the drive is in a door-locked state, the drive does not respond to the media-change request button, except by setting the MCR bit to one. The command Door Unlock or Media Eject clears the door-locked condition. So does a hardware reset.

This command takes no action and returns *good* status when MSN mode is enabled.

Door Unlock (DFh)

Inputs

Table 6-8 Door Unlock—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	DFh							

Normal Outputs

Table 6-9 Door Unlock—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-10 Door Unlock—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command unlocks the drive and allows it to respond to the media-change request button.

This command takes no action and returns *good* status when MSN mode is enabled.

Download Microcode (92h)

Inputs

The head bits of the Device/Head register are always cleared to zero. The Cylinder High and Cylinder Low registers are cleared to zero. The Sector Number and Sector Count registers are used together as a 16-bit, sector-count value: 200h (512 sectors).

Table 6-11 Download Microcode—Inputs

Register	7	6	5	4	3	2	1	0
Features	00h							
Sect Count	00h							
Sect Num	02h							
Cyl Low	00h							
Cyl High	00h							
Dev/Head	1	na	1	DEV	0	0	0	0
Command	92h							

Normal Outputs

Table 6-12 Download Microcode—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-13 Download Microcode—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

For the command to execute, the Sector Number register must be set to 02h, and the Sector Count register must be set to 00h.

Description

This command allows the host to alter the drive's microcode (firmware). The data is programmed into the drive's flash ROM. The drive expects a transfer of 512 sectors.

Upon receiving and verifying the microcode, the drive spins down, programs the flash memory, spins up, and comes ready. You can view the revision number of the new microcode by using the Identify Drive command.

Execute Device Diagnostics (90h)

Inputs

There are no inputs. The device selection bit in the Device/Head register is ignored.

Table 6-14 Execute Device Diagnostics—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	na	na	na	na	na
Command	90h							

Normal Outputs

Table 6-15 Execute Device Diagnostics—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	Diagnostic code							
Sect Count	01h							
Sect Num	01h							
Cyl Low	00h							
Cyl High	00h							
Dev/Head	00h							
Status	BSY	na	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- ERR is cleared to zero.

The diagnostic code written into the Error register is an 8-bit code. The following table defines these codes:

Table 6-16 Execute Device Diagnostics—Diagnostic Codes

Code		Description
In Device 0 Error Register	In Device 1 Error Register	
01h		Device 0 passed; device 1 passed or not present
00h, 02h - 7Fh		Device 0 failed; device 1 passed or not present
81h		Device 0 passed; device 1 failed
80h, 82h - FFh		Device 0 failed; device 1 failed
	01h	Device 1 passed
	00h, 02h - 7Fh	Device 1 failed

Error Outputs

Error information is returned as a diagnostic code in the Error register.

Prerequisites

None.

This command is accepted when DRDY is cleared to zero.

Description

This command performs vendor-unique diagnostics.

Identify Device (ECh)

Inputs

Table 6-17 Identify Device—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	ECh							

Normal Outputs

Table 6-18 Identify Device—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

The drive does not report an error.

Prerequisites

DRDY must be set to one.

Description

This command allows the host to get parameter information from the drive.

When the host issues the Identify Device command, the drive does the following:

- Sets the BSY bit to one
- Prepares to transfer 256 words of SparQ-identification data to the host
- Sets the DRQ bit to one
- Clears the BSY bit to zero
- Generates an interrupt

Then the host can transfer the data by reading the Data register. All reserved bits or words are zero.

Parameters are defined in these ways:

- As a *set* of bits. Such parameters are transmitted with indicated bits on the respective data-bus bit (e.g., bit 15 appears on DD15).
- As a 16-bit value. Such parameters place the most significant bit of the value on bit DD15, and the least significant bit of the value on bit DD0.
- As a 32-bit value (e.g., words 57 and 58). Such parameters use two-word transfers. First the drive transfers the least significant bits, bits 15 through 0 of the value, on bits DD(15:0). Then the drive transfers the most significant bits, bits 31 through 16 of the value, on bits DD(15:0).

The SparQ is fully compliant with the bit definitions of the *AT Attachment-4 Interface standard (ATA-4)*. Refer to that document for more details on bit definitions for data retrieved with the Identify Device command.

Words 0 through 61 of the SparQ-identification data are defined as follows:

Word 0: general configuration. An indication that the drive contains removable media and conforms to the ATA-4 standard

Word 1: default number of cylinders. The number of logical cylinders (2906) that the user can address in the default translation mode

Word 2. Reserved

Word 3: default number of logical heads. The number of logical heads per logical cylinder (16) that the user can address in the default translation mode

Words 4 - 5. Reserved

Word 6: default number of logical sectors per logical track. The number of logical sectors per logical track (63) that the user can address in the default translation mode

Words 7 - 9. Reserved

Words 10 - 19: serial number. The serial number of the cartridge currently in the drive

Words 20 - 22. Reserved

Words 23 - 26: microcode revision. The revision number of the drive's microcode (firmware), given as an ASCII character string of eight bytes

Words 27-46: model number. The model number of the drive, given as an ASCII character string of 40 bytes

Word 47: read/write Multiple support. The maximum number of sectors per block (16) that the drive supports for Read Multiple and Write Multiple commands

Word 48. Reserved

Word 49: capabilities for Standby Timer and IORDY support. Bit 13 indicates drive support for a Standby Timer. Bit 11 indicates drive support for IORDY operation. Bit 10 indicates drive support for disabling IORDY.

Words 50 - 53. Reserved

Word 54: current number of logical cylinders. The number of logical cylinders in the current translation mode that the user can address

Word 55: current number of logical heads. The number of logical heads per logical cylinder in the current translation mode that the user can address

Word 56: current number of logical sectors per logical track. The number of logical sectors per logical track in the current translation mode that the user can address

Words 57 - 58: current capacity in sectors. The product of words 54, 55, and 56. The current capacity in sectors excludes all sectors used for purposes that are specific to the SparQ.

Word 59: multiple sector setting. If bit 8 is set to one, bits 7 - 0 reflect the number of sectors currently set to transfer on a Read Multiple or Write Multiple command.

Words 60 - 61: total number of sectors the user can address. These words reflect the total number of sectors that the user can address in LBA translation. This value equals 1,961,069, and it does not depend on the current SparQ-drive geometry.

Word 67: minimum PIO transfer cycle time without flow control. 120 nanoseconds

Word 68: minimum PIO transfer cycle time with IORDY. 120 nanoseconds

Word 127: Removable Media Status Notification feature set support. If bit 0 is set to one and bit 1 is cleared to zero, then the device supports the Removable Media Status Notification feature set. Bits 15 through 2 are cleared to zero.

Idle (E3h)

Inputs

Table 6-19 Idle—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Time period value							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	E3h							

When the host issues the Idle command, a value other than zero in the Sector Count register determines the time period that is programmed into the Standby Timer. The following table defines these values:

Table 6-20 Idle—Automatic Standby Timer Periods

Sector Count Register Contents	Corresponding Time-Out Period ¹
0 (00h)	Time-out disabled
1 - 240 (01h - F0h)	(value * 5) seconds
241 - 251 (F1h - FBh)	((value - 240) * 30) minutes
252 (FCh)	21 minutes
253 (FDh)	8 hours
254 (FEh)	Reserved
255 (FFh)	21 minutes and 15 seconds
Note:	
¹ All times are approximate.	

Normal Outputs

Table 6-21 Idle—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-22 Idle—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command allows the host to put the drive into Idle mode while concurrently programming the Standby Timer. INTRQ is asserted, though the drive may not have fully moved to Idle Mode.

If the Sector Count register is not set to zero, then the Standby Timer is enabled. The value in the Sector Count register determines the time programmed into the Standby Timer.

If the Sector Count register is zero, then the Standby Timer is disabled.

Idle Immediate (E1h)

Inputs

Table 6-23 Idle Immediate—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	E1h							

Normal Outputs

Table 6-24 Idle Immediate—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-25 Idle Immediate—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command allows the host to put the drive into Idle mode without altering the current setting of the Standby Timer. INTRQ is asserted, though the drive may not have fully moved to Idle Mode.

Initialize Device Parameters (91h)

Inputs

The Sector Count register specifies the number of logical sectors per logical track. The Device/Head register specifies the maximum head number.

Table 6-26 Initialize Device Parameters—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Logical sectors per logical track							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	Max head			
Command	91h							

Normal Outputs

Table 6-27 Initialize Device Parameters—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- ERR is cleared to zero.

Error Outputs

Table 6-28 Initialize Device Parameters—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

None.

Description

This command allows the host to set for each logical cylinder the number of logical sectors per track and the number of logical heads minus 1. This is for the current CHS translation mode.

If a requested CHS translation is not supported, the drive fails all media-access commands with the error ID **Not Found** until a valid CHS translation is established.

Media Eject (EDh)

Inputs

Table 6-29 Media Eject—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	EDh							

Normal Outputs

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Table 6-30 Media Eject—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Error Outputs

Table 6-31 Media Eject—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command completes any pending operations, spins down the drive if needed, unlocks the drive door or media if locked, and ejects the media if needed.

Media Status (DAh)

Inputs

Table 6-32 Media Status—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	DAh							

Normal Outputs

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Table 6-33 Media Status—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Error Outputs

Table 6-34 Media Status—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	WP	MC	na	MCR	na	NM	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- WP indicates that the media is write protected.
- MC indicates that new media has been inserted since the last Media Status command.
- MCR indicates that the eject has been pushed since the last Media Status command.
- NM indicates that no media is currently inserted in the drive.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command reports the current media status of the drive.

NOP (00h)

Inputs

Table 6-35 NOP—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	00h							

Normal Outputs

This command always fails with an error.

Error Outputs

The command-block registers, other than the Error and Status registers, are not changed by this command. This command always fails with an Aborted Command error.

Table 6-36 NOP—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	Initial value ¹							
Sect Num	Initial value ¹							
Cyl Low	Initial value ¹							
Cyl High	Initial value ¹							
Dev/Head	Initial value ¹							
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR
Note: ¹ The value set by the host is not changed.								

Error register:

- ABRT indicates this command is not supported.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command allows a host that can perform only 16-bit register access to check the drive status. The drive responds as it does to an unrecognized command:

- Setting Aborted Command to one in the Error register
- Setting the Error bit in the Status register
- Clearing Busy to zero in the Status register
- Asserting INTRQ

Read Multiple (C4h)

Inputs

Table 6-37 Read Multiple—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Sector count							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	LBA	1	DEV	Head number or LBA			
Command	C4h							

The Sector Count register specifies the number of sectors to transfer. A value of 00h indicates a transfer of 256 sectors.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the starting address to read:

- The Sector Number register specifies the starting sector number or LBA address bits (7:0).
- The Cylinder Low register specifies the starting cylinder number bits (7:0) or LBA address bits (15:8).
- The Cylinder High register specifies the starting cylinder number bits (15:8) or LBA address bits (23:16).
- The Device/Head register specifies the starting head number. Bit 6 is set to one for an LBA address. Bit 6 is cleared to zero for CHS address bits (3:0) or LBA address bits (27:24).

Normal Outputs

Table 6-38 Read Multiple—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

An unrecoverable error during command execution results in terminating the command. The command-block registers contain the sector address where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 6-39 Read Multiple—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	AMNF
Sect Count	na							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	CORR	na	ERR

Error register:

- UNC indicates data is uncorrectable.
- IDNF indicates the sector's ID field could not be found.
- ABRT indicates this command is not supported.
- AMNF indicates the data address mark could not be found after finding the correct ID field.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the address of the first unrecoverable error.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- CORR indicates a correctable data error was found.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

If bit 8 of Word 59 of a response to the Identify Device command is cleared to zero, a successful Set Multiple Mode command precedes a Read Multiple command.

Description

The Read Multiple command performs similarly to the Read Sector(s) command.

Interrupts are not generated on every sector. Interrupts are generated on the transfer of a block that contains the number of sectors defined by a Set Multiple Mode command, or on the default number of sectors if no intervening Set Multiple Mode command has been issued.

Command operation is identical to the Read Sector(s) command, except that the number of sectors defined by a Set Multiple Mode command are transferred without intervening interrupts. The DRQ bit qualification for the transfer is required only at the start of the data block, not on each sector.

The block count of sectors for transfer without intervening interrupts is programmed by the Set Multiple Mode command. The Set Multiple Mode command is executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count register contains the number of requested sectors (not the number of blocks or the block count).

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred. This is followed by a final partial-block transfer that includes the remaining sectors.

If a Read Multiple command is received after it has been disabled, the operation is rejected with an **Aborted Command** error. Drive errors during the execution of Read Multiple are posted at the beginning of the block or partial-block transfer. However, the DRQ bit is still set to one and the data transfer takes place. This includes the transfer of corrupted data, if any.

Command-block registers that follow the transfer of a data block with a sector in error have undefined contents. The host retries the transfer as individual requests to obtain valid error information. Subsequent blocks or partial blocks are transferred only if the error is a data error that can be corrected. All other errors cause the command to stop after transfer of the block that contained the error.

Read Sector(s) (20h or 21h)

Inputs

Table 6-40 Read Sector(s)—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Sector count							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	LBA	1	DEV	Head number or LBA			
Command	20h or 21h							

The Sector Count register specifies the number of sectors to transfer. A value of 00h indicates a transfer of 256 sectors.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the starting address to read:

- The Sector Number register specifies the starting sector number or LBA address bits (7:0).
- The Cylinder Low register specifies the starting cylinder number bits (7:0) or LBA address bits (15:8).
- The Cylinder High register specifies the starting cylinder number bits (15:8) or LBA address bits (23:16).
- The Device/Head register specifies the starting head number. Bit 6 is set to one for an LBA address. Bit 6 is cleared to zero for CHS address bits (3:0) or LBA address bits (27:24).

Normal Outputs

Table 6-41 Read Sector(s)—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

An unrecoverable error during command execution results in terminating the command. The command-block registers contain the sector address where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 6-42 Read Sector(s)—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	AMNF
Sect Count	na							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	CORR	na	ERR

Error register:

- UNC indicates data is uncorrectable.
- IDNF indicates the sector's ID field could not be found.
- ABRT indicates this command is not supported.
- AMNF indicates the data address mark could not be found after finding the correct ID field.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the address of the first unrecoverable error.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- CORR indicates a correctable data error was found.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command reads from 1 to 256 sectors, as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

The DRQ bit is *always* set to one prior to data transfer regardless of the presence or absence of an error condition.

Read Verify Sector(s) (40h or 41h)

Inputs

Table 6-43 Read Verify Sector(s)—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Sector count							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	LBA	1	DEV	Head number or LBA			
Command	40h or 41h							

The Sector Count register specifies the number of sectors to transfer. A value of 00h indicates a transfer of 256 sectors.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the starting address to read:

- The Sector Number register specifies the starting sector number or LBA address bits (7:0).
- The Cylinder Low register specifies the starting cylinder number bits (7:0) or LBA address bits (15:8).
- The Cylinder High register specifies the starting cylinder number bits (15:8) or LBA address bits (23:16).
- The Device/Head register specifies the starting head number. Bit 6 is set to one for an LBA address. Bit 6 is cleared to zero for CHS address bits (3:0) or LBA address bits (27:24).

Normal Outputs

Table 6-44 Read Verify Sector(s)—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

An unrecoverable error during command execution results in terminating the command. The command-block registers contain the sector address where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 6-45 Read Verify Sector(s)—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	AMNF
Sect Count	na							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	CORR	na	ERR

Error register:

- UNC indicates data is uncorrectable.
- IDNF indicates the sector's ID field could not be found.
- ABRT indicates this command is not supported.
- AMNF indicates the data address mark could not be found after finding the correct ID field.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the address of the first unrecoverable error.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- CORR indicates a correctable data error was found.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command is identical to the Read Sector(s) command, except that the DRQ bit is *never* set to one, and no data is transferred to the host.

Reassign Sector (F8h, FBh, or FCh)

Inputs

Four commands are necessary to support this function:

- Enter super-user mode.

Features register: ignored

Sector count, sector: ignored

Cylinder registers: 0ffh, 0ffh

Head: drive select

Command: 0fbh

The drive aborts this command. The host ignores the aborted command and sends the next command.

- Confirm super-user mode.

Features register: ignored

Sector count, sector: ignored

Cylinder registers: 0fh, 0f0h

Head: drive select

Command: 0fbh

- Reassign block (only accepted if in super-user mode).

Features register: ignored

Sector count: 1

Sector/Cylinder/Head: address

Command: 0f8h

- Exit super-user mode (only accepted if in super-user mode).

Features register: ignored

Sector count, sector, cylinder: ignored

Head: drive select

Command: 0fch

Normal Outputs

Table 6-46 Reassign Sector—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-47 Reassign Sector—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- ABRT indicates an aborted command if the reassignment fails. The error **Aborted Command** is posted.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command reassigns a user sector to an alternate location on the media for all future commands.

Seek (70h)

Inputs

Table 6-48 Seek—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	LBA	1	DEV	Head number or LBA			
Command	70h							

The Sector Number, Cylinder Low, Cylinder High, and Device/Head (head portion only) registers contain a sector address that the host may request in a subsequent command:

- The Sector Number register specifies the starting sector number or LBA address bits (7:0).
- The Cylinder Low register specifies the starting cylinder number bits (7:0) or LBA address bits (15:8).
- The Cylinder High register specifies the starting cylinder number bits (15:8) or LBA address bits (23:16).
- The Device/Head register specifies the starting head number. Bit 6 is set to one for an LBA address. Bit 6 is cleared to zero for CHS address bits (3:0) or LBA address bits (27:24).

Normal Outputs

Table 6-49 Seek—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-50 Seek—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- IDNF indicates no ID is found.
- ABRT indicates this command is not supported.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command allows the host to notify the drive in advance that particular data may be requested in a subsequent command.

DSC is set to one concurrently or after DRDY is set to one while updating the Status register for this command.

Set Features (EFh)

Inputs

Table 6-51 Set Features—Inputs

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sect Count	Subcommand specific							
Sect Num	Subcommand specific							
Cyl Low	Subcommand specific							
Cyl High	Subcommand specific							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	EFh							

Table 6-53 defines the values of subcommands in the Features register. Some subcommands use other registers such as the Sector Count register to pass additional information to the drive.

Normal Outputs

See the subcommand information under “Description” on page 6-52.

Error Outputs

Table 6-52 Set Features—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- ABRT indicates this command is not supported or its value is invalid.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command is used by the host to establish parameters that affect the execution of some drive features. The following table defines these features:

Table 6-53 Set Features—Register Definitions

Value ¹	Subcommand/Definition
02h	Enable Write Cache
03h	Set Transfer Mode based on Sector Count register value. See Table 6-54.
31h	Disable Media Status Notification protocol
55h	Disable Read Look-Ahead
82h	Disable Write Cache
95h	Enable Media Status Notification protocol
AAh	Enable Read Look-Ahead
Note: ¹ All values (codes) not shown are reserved for future definition.	

At power on, or after a hardware reset, the default settings of the functions specified by the subcommands are vendor-specific settings.

Enable/Disable Write Cache: Subcommand codes 02h and 82h allow the host to enable and disable write cache. When the host issues the subcommand Disable Write Cache, the drive flushes cache to nonvolatile memory before posting that the command is complete.

Set Transfer Mode: Subcommand code 03h and a specified value in the Sector Count register allow the host to choose the data-transfer mechanism. The upper five bits define the type of transfer, and the lower three bits encode the mode value.

Enable Media Status Notification: Subcommand code 95h allows the host to enable the Media Status Notification mode.

This subcommand returns the following status in the Cylinder Low and Cylinder High registers:

- In the Cylinder Low register, the current revision number of MSN implementation
- In the Cylinder High register, the following values:

7	6	5	4	3	2	1	0
na	na	na	na	na	PEJ	LOCK	PEN

- PEJ is set to indicate that the drive has a power-eject mechanism.
- LOCK is set to indicate that the drive is able to inhibit the front-panel eject button.
- PEN is set to indicate that MSN mode is already active (otherwise negated).

Disable Media Status Notification: Subcommand code 31h allows the host to disable the Media Status Notification mode.

Enable/Disable Read Look-Ahead: Subcommand codes AAh and 55h allow the host to request that the SparQ enable or disable read look-ahead.

The following table shows the transfer-mode values:

Table 6-54 Set Features—Transfer-mode values

Mode ¹	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode
Reserved	10000b	na
Note:		
¹ Mode = transfer-mode number		

Set Multiple Mode (C6h)

Inputs

The Sector Count register contains the number of sectors per block to use on all Read Multiple and Write Multiple commands that follow the Set Multiple Mode command. The host sets sector-count values of 2, 4, 8, or 16.

Table 6-55 Set Multiple Mode—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Sector count							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	C6h							

Normal Outputs

Table 6-56 Set Multiple Mode—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

If a block count is not supported, an Aborted Command error is posted.

Table 6-57 Set Multiple Mode—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- ABRT indicates the block count is not supported.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command establishes the block count for Read Multiple and Write Multiple commands.

When the SparQ receives this command, it checks the Sector Count register. If the Sector Count register contains a valid value and the block count is supported:

- The execution of Read Multiple and Write Multiple commands is allowed.
- The valid value is used for all subsequent Read Multiple and Write Multiple commands.

Sleep (E6h)

Inputs

Table 6-58 Sleep—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	E6h							

Normal Outputs

Table 6-59 Sleep—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-60 Sleep—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command is the only way to cause the drive to enter Sleep mode. When the drive receives this command, it sets the BSY bit to one, prepares to enter Sleep mode, clears the BSY bit to zero, and asserts INTRQ. The host reads the Status register in order to clear the interrupt and allow the drive to enter Sleep mode.

In Sleep mode, the drive interface becomes inactive without affecting the operation of the interface. The host does not attempt to access the command-block registers while the drive is in Sleep mode.

The only way for the drive to recover from Sleep Mode is with a software reset or a hardware reset. The drive does not power on in Sleep Mode, and it does not remain in Sleep Mode following a reset sequence.

Standby (E2h)

Inputs

Table 6-61 Standby—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Time period value							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	E2h							

When the host issues the Standby command, a value other than zero in the Sector Count register determines the time period that is programmed into the Standby Timer.

The following table defines these values:

Table 6-62 Standby—Automatic Standby Timer Periods

Sector Count Register Contents		Corresponding Time-Out Period ¹
0	(00h)	Time-out disabled
1 - 240	(01h - F0h)	(value * 5) seconds
241 - 251	(F1h - FBh)	((value - 240) * 30) minutes
252	(FCh)	21 minutes
253	(FDh)	8 hours
254	(FEh)	Reserved
255	(FFh)	21 minutes and 15 seconds
Note:		
¹ All times are approximate.		

Normal Outputs

Table 6-63 Standby—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-64 Standby—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command causes the drive to enter Standby mode.

If the Sector Count register is set to a non-zero value, the Standby Timer is enabled. The value in the Sector Count register is used to determine the time programmed into the Standby Timer.

If the register is set to zero, the Standby Timer is disabled.

Standby Immediate (E0h)

Inputs

Table 6-65 Standby Immediate—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	E0h							

Normal Outputs

Table 6-66 Standby Immediate—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-67 Standby Immediate—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command causes the drive to enter Standby mode without modifying the Standby Timer.

SyQuest Set Features (F0h)

Inputs

Table 6-68 SyQuest Set Features—Inputs

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sect Count	Subcommand specific							
Sect Num	Subcommand specific							
Cyl Low	Subcommand specific							
Cyl High	Subcommand specific							
Dev/Head	1	na	1	DEV	na	na	na	na
Command	F0h							

Table 6-70 defines the values of subcommands in the Features register.

Normal Outputs

See the subcommand information under “Description” on page 6-66.

Error Outputs

Table 6-69 SyQuest Set Features—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- ABRT indicates this command is not supported or its value is invalid.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command is used by the host to establish parameters that affect the execution of some drive features. The following table defines these features:

Table 6-70 SyQuest Set Features—Register Definitions

Value ¹	Subcommand/Definition
01h	Disable cartridge allegiant write verify
02h	Enable cartridge allegiant write verify
09h	Perform head clean function
0Ah	Disable cartridge allegiant read auto-relocation
0Bh	Enable cartridge allegiant read auto-relocation
0Ch	Disable cartridge allegiant software ECC correction
0Dh	Enable cartridge allegiant software ECC correction
0Eh	Disable cartridge allegiant write auto-relocation
0Fh	Enable cartridge allegiant write auto-relocation
14h	Disable drive allegiant read auto-relocation
15h	Enable drive allegiant read auto-relocation
16h	Disable drive allegiant write auto-relocation
17h	Enable drive allegiant write auto-relocation
Note: ¹ All values (codes) not shown are reserved for future definition.	

At power on, or after a hardware reset, the default settings of functions specified by subcommands are vendor-specific settings.

Enable/disable cartridge allegiant write verify: Subcommand codes 01h and 02h allow the host to enable or disable drive allegiant write verify.

Perform head clean function: Subcommand code 09h allows the host to invoke the head cleaning function.

Enable/disable cartridge allegiant read auto-relocation:

Subcommand codes 0Ah and 0Bh allow the host to enable and disable cartridge allegiant read auto-relocation.

Enable/disable cartridge allegiant software ECC correction:

Subcommand codes 0Ch and 0Dh allow the host to enable and disable cartridge allegiant software ECC correction.

Enable/disable cartridge allegiant write auto-relocation:

Subcommand codes 0Eh and 0Fh allow the host to enable and disable cartridge allegiant write auto-relocation.

Enable/disable drive allegiant read auto-relocation:

Subcommand codes 14h and 15h allow the host to enable or disable drive allegiant read auto-relocation.

Enable/disable drive allegiant write auto-relocation:

Subcommand codes 16h and 17h allow the host to enable and disable drive allegiant write auto-relocation.

Write Multiple (C5h)

Inputs

Table 6-71 Write Multiple—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Sector count							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	LBA	1	DEV	Head number or LBA			
Command	C5h							

The Sector Count register specifies the number of sectors to transfer. A value of 00h indicates a transfer of 256 sectors.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the starting address to be written:

- The Sector Number register specifies the starting sector number or LBA address bits (7:0).
- The Cylinder Low register specifies the starting cylinder number bits (7:0) or LBA address bits (15:8).
- The Cylinder High register specifies the starting cylinder number bits (15:8) or LBA address bits (23:16).
- The Device/Head register specifies the starting head number. Bit 6 is set to one for an LBA address. Bit 6 is cleared to zero for CHS address bits (3:0) or LBA address bits (27:24).

Normal Outputs

Table 6-72 Write Multiple—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

An unrecoverable error during command execution results in terminating the command. The command-block registers contain the sector address where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 6-73 Write Multiple—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sect Count	na							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- IDNF indicates the sector's ID field could not be found.
- ABRT indicates this command is not supported.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the address of the first unrecoverable error.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

The Write Multiple command performs similarly to the Write Sector(s) command.

Interrupts are not generated on every sector. Interrupts are generated on the transfer of a block that contains the number of sectors defined by a Set Multiple Mode command, or on the default number of sectors if no intervening Set Multiple Mode command has been issued.

Command operation is identical to the Write Sector(s) command, except that the number of sectors defined by a Set Multiple Mode command are transferred without intervening interrupts. The DRQ bit qualification for the transfer is required only at the start of the data block, not on each sector.

The block count of sectors for transfer without intervening interrupts is programmed by the Set Multiple Mode command. The Set Multiple Mode command is executed prior to the Write Multiple command. When the Write Multiple command is issued, the Sector Count register contains the number of requested sectors (not the number of blocks or the block count).

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred. This is followed by a final partial-block transfer that includes the remaining sectors.

If a Write Multiple command is received after it has been disabled, the operation is rejected with an **Aborted Command** error. Drive errors during the execution of Write Multiple are posted after the attempted write of the block or partial-block transfer. The command ends with the sector in error, even if that sector is in the middle of a block. Any subsequent blocks are not transferred.

Command-block registers that follow the transfer of a partial data block with a sector in error have undefined contents. The host retries the transfer as individual requests to obtain valid error information. Interrupts are generated when the DRQ bit is set to one at the beginning of each block or partial block.

Write Protect Enable/Disable (C0h)

Inputs

Table 6-74 Write Protect Enable/Disable—Inputs

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	LBA	1	DEV	na	na	na	na
Command	C0h							

Features register:

- Subcommand code P enables write protection.
- Subcommand code E disables write protection.

Normal Outputs

Table 6-75 Write Protect Enable/Disable—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

Table 6-76 Write Protect Enable/Disable—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- ABRT indicates this command is not supported.

Prerequisites

None.

Description

This command allows the user to enable and disable write protection. When write protection is enabled, attempting to write to the media returns a error.

Write Sector(s) (30h or 31h)

Inputs

Table 6-77 Write Sector(s)—Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sect Count	Sector count							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	LBA	1	DEV	Head number or LBA			
Command	30h or 31h							

The Sector Count register specifies the number of sectors to transfer. A value of 00h indicates a transfer of 256 sectors.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the starting address to be written:

- The Sector Number register specifies the starting sector number or LBA address bits (7:0).
- The Cylinder Low register specifies the starting cylinder number bits (7:0) or LBA address bits (15:8).
- The Cylinder High register specifies the starting cylinder number bits (15:8) or LBA address bits (23:16).
- The Device/Head register specifies the starting head number. Bit 6 is set to one for an LBA address. Bit 6 is cleared to zero for CHS address bits (3:0) or LBA address bits (27:24).

Normal Outputs

Table 6-78 Write Sector(s)—Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sect Count	na							
Sect Num	na							
Cyl Low	na							
Cyl High	na							
Dev/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- ERR is cleared to zero.

Error Outputs

An unrecoverable error during command execution results in terminating the command. The command-block registers contain the sector address where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 6-79 Write Sector(s)—Error Outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sect Count	na							
Sect Num	Sector number or LBA							
Cyl Low	Cylinder low or LBA							
Cyl High	Cylinder high or LBA							
Dev/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register:

- IDNF indicates the sector's ID field could not be found.
- ABRT indicates this command is not supported.

The Sector Number, Cylinder Low, Cylinder High, and Device/Head registers specify the address of the first unrecoverable error.

Status register:

- BSY is cleared to zero, indicating command completion.
- DRDY is set to one.
- DF is set to one if a drive fault has occurred.
- DRQ is cleared to zero.
- ERR is set to one if an Error register bit is set to one.

Prerequisites

DRDY must be set to one.

Description

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors.