## MB8A 1K TO 16K EPROM BOARD



FEATURES:

## SYSTEM COMPATIBILITY

. S-100 bus computer systems.

## MEMORY

. Up to 16 K bytes of 2708 EPROMs (not included)
. Any unused EPROM socket will automatically disable the board for that lk increment. For example, with 8 EPROMs it acts as an 8 K board, taking up only 8 K of memory address space.

## ADDRESSING

. DIP switch selection of memory address assignment in 16 K byte increments.

- Magic Mapping TM allows any byte within ROM to be mixed with any similarly addressed RAM board equipped with Phantom Disable.


## VECTOR JUMP

. Power-on/reset vector jump to any 256 byte increment; DIP switch addressable.

- Vector jump can be disabled.
. Vector jump requires other memory boards to be equipped with Phantom Disable.


## OTHER FEATURES

. DIP switch selection of 0 to 8 wait state clock cycles, so fast or slow EPROMs can be used.

- All lines buffered, Reverse voltage protection.
- High grade glass epoxy PC board with gold plated edge connector contacts.
- Low profile sockets provided for all ICs.

Power requirements (less EPROMs) -- +8 V @ $160 \mathrm{~mA},+16 \mathrm{~V} @ 10 \mathrm{~mA},-16 \mathrm{~V} @ 10 \mathrm{~mA}$ typical.

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Schematic

2116 Walsh Ave. Santa Clara, California

> MB8-A - 8K/16K EPROM BOARD
1.0 ASSEMBLY INSTRUCTIONS (refer to figure 1)

Check kit contents against parts list.
$\square$ Check PC board for possible warpage and straighten if required.
Insert 16 24-pin, 916 -pin, 514 -pin, and 18 -pin socket into the component side of the board with the "pin 1" index toward the top of the board. (The component side is the side on which "Solid State Music" is printed.)

Place a flat piece of stiff cardboard of appropriate size on top of the sockets to hold them in place.

Holding the cardboard in place against the sockets, turn the board over and lay it on a flat surface. (Be sure that all of the socket pins are through the holes.)

Note: Keep soldering iron tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth or steel wool .

On each socket, solder two of the corner pins, choosing two that are diagonally opposite of each other.

Once the sockets are secured, lift the board and check to see if they are flat against the board. If not, seat the sockets by pressing on the top while reheating each soldered pin.

$\square$
Complete soldering the remaining pins of each socket. Touch pin and pad with iron tip, allowing enough solder to flow to form a filet between pin and pad. Keep the tip against the pin and pad just long enough to produce the filet. Too much heat can cause separation of pad and trace from the board. A 600 degree iron is recommended.

Insert and solder 62.7 K SIPs and 1 10K resistor.
Insert and solder 5 diodes (observing polarity).
Insert and solder 40.1 uF ceramic capacitors.
Observing polarity, insert and solder 4 dipped \& 3 tubular tantalum capacitors.

Insert 2 DIP switches with the word "OPEN" toward the left of the board.
Place regulators on the board so the mounting hole in the regulator is in line with the hole in the board. Mark leads for proper bending to match the board holes - allow for a bend radius. -

Bend regulator leads to match holes in board.
If available, apply thermal compound to the back side of each regulator case (the side that will contact the heat sink). Use just a little thermal compound. Too much is worse than none at all.

On the front (component side) of the board, position 2 heatsink insulators on the U12 and U24 regulator locations $\%$. Next position heatsink and insert regulator for each of the 5 regulators. Finally, position nut and lockwasher on top of regulator and secure from behind with screw in each case. Be sure regulators and heatsinks fit flat on board and then solder all regulator leads.

### 2.0 FUNCTIONAL CHECK

WARNING! DO NOT INSTALL OR REMOVE BOARD WITH POWER ON. DAMAGE TO THIS AND OTHER BOARDS COULD OCCUR.

Apply power ( +8 volts approx.) to board by plugging into computer or by connection to a suitable power supply. Measure the output of U25. If less than 4.8 volts is measured (allowing for meter accuracy) check for shorts or wiring errors. CAUTION: WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGULATORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES OR HANDS. BETTER SAFE THAN SORRY - KEEP FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THIS AND SUBSEQUENT TESTS!

Apply power ( +16 volts) to the board by plugging into computer or by connection to a suitable power supply. Verify that the outputs of Ul \& U13 are between +11. 5 \& +12.5 Vdc.

Apply power ( -16 volts) to the board by plugging into computer or by connection to a suitable power supply. Verify that the outputs of U12 \& U24 are between $-4.8 \&-5.4 \mathrm{Vdc}$.

Finally, insert the ICs into their sockets, observing polarity.
Now, look the board over carefully. Check for poor solder joints or bridges. Using the component layout drawing, look for improper part location or polarity. A few minutes of careful inspection may save a few hours of troubleshooting.

[^0]
### 3.1 Address Selection

The $M B-8$ card can be set to one of four possible address locations in 16 K increments. HIGH ORDER BITS
Starting Address
$\varnothing \varnothing \varnothing \varnothing(\quad \varnothing)$
$4 \emptyset \emptyset \emptyset(16,384)$.
A15 $\quad$ Al4
SETTING OF S2 A15

A14

| $\emptyset$ | $\varnothing$ | OPEN | OPEN |
| :--- | :--- | :--- | :--- |
| $\emptyset$ | 1 | OPEN | CLOSED |
| 1 | $\emptyset$ | CLOSED | OPEN |
| 1 | 1 | CLOSED | CLOSED |

Сøø (49,148)
1

```
note: open = off
closed = on
```

Even though the MB-8A card can support 16K of PROM, it can be disabled down to as small as one byte of PROM. No jumpers necessary for disable selection!

### 3.2 PROM Area Enable/Disable

A. 1 K Increments

Where ever PROM is inserted into the MB-8A card, the board can enable at that address location, and the empty ROM sockets will be addresses that the card will disable itself. This will allow the user to have only 1 K or 2 K of active PROM area. This means you can place a RAM card at an address within the MB-8A's area if there is no PROM in the socket at that address.
B. Less than 1 K increments.

If the user wants PROM areas on the MB-8A in fractions of 1 K , it is possible.

Example.
Problem: Only a 512 byte program is needed for system operation, the user then wants the rest of his 16 K bytes filled with RAM.

Solution: Address the MB-8A card so that it will overlap the wanted 512 byte program's address. Find the socket on the MB-8A card which is the IK block that overlays the 512 bytes. Program a 2708 PROM for this socket with the 512 byte program, and any bytes that are not used shall be programmed with FF Hex. Now insert the MB-8A card with the one PROM into the computer and insert RAM at all addresses except where 512 bytes of ROM is located.

As you can see, any byte in ROM set to FF Hex will disable the MB-8A card.

This is the most interesting mode of the $\mathrm{MB}-8 \mathrm{~A}$ card, but requires more software and care in implementing. The idea of magic mapping is the ability of having scratch RAM within the 1024 bytes of a 2708 ROM or have a couple of bytes (or more) of ROM right in the middle of a RAM card. If that sounds like what you have been looking for, then here is how to do it.
A. The RAM card that will be mixed with PROM must be equipped with Phantom disable. (Pin 67 on the bus going low will disable memory,)
B. Any area of a 2708 PROM you wanted to be changed into RAM must be programmed with FF Hex.
C. The area of RAM that a 2708 overlaps must be initialized to FF before the user program can be run. This initialization program can not have any FF bytes in its machine code, if it also overlaps RAM memory.

A simple initialization routine is listed below:
;THIS PROGRAM WILL FILL JUST ONE BLOCK OF ; MEMORY WITH FF HEX. WRITTEN BY MALCOLA URIGHT. 31-10-1978.
$3^{\text {"LOC" IS THE STARTING ADDRESS OF }}$ ; THE PROGRAM.



3 THIS PROGRAM WILL FILL AREAS OF GEMORY WITH 3FF HEX AS SPECIFIED IN A ADDRESS TABLE SUPPLIED ; BY THE USER. WRITTEN BY MALCOLM WRIGAT, 1-1@-1978.

FCOD
F621
FCOD

FCDD $212 A F C$ FCD3 4E FCO4 23
FCES 46

## FCO6 23

FC07 5E
FCO8 2.3.
FCOS 56
FCDA 23
FCOB 78
FCDC BI
FCDD C218FC
FC10 B3
FC11 C218FC
FC14 B2
FC15 CA21FD

FC18 DB
FC19 83
FClA AF
FC13 $2 F$
FCIC 2
FC1D 78
FCIE BA
FCIF DA19FC
FC22 79
FC23 BB
FC24 DA19FC FC27 C303FG

FC2A

:THE ENTRY POINT OF THIS PROGRAM BEGINS UITH ;LXI H INSTRUCTION. THE TWO BYTES THAT ARE GOING ; INTO H\&L CAN NOT BE FF HEX.
:IF EITHER BYTE IS FF, THEN TRY THIS:



| START: NEXT: | DCX | B |  |
| :---: | :---: | :---: | :---: |
|  | INX | B |  |
|  | XRA | A | :Clear reg.a to zero |
|  | CMA |  |  |
|  | STAX | B | :STORE "FF" |
|  | MOV | A, B |  |
|  | CMP | D |  |
|  | JC | NEXT | ; * WARNING! |
|  | MOV | A, C |  |
|  | CMP | E |  |
|  | JC | NEXT | 3* WARNING! |
|  | JMP | GET | ; NEXT AREA PLEASE. |
| TABLE: | DS | 12 | ; WARNING! |
|  |  |  | ;SET WITH ADDRESS VALUES |

;*....THIS BYTE OR INSTRUCTION CAN NOT BE FF HEX. END
3.3 (continued)
(3) If individual IK blocks need to be initialized to FF Hex, then the routine on the previous page will help.

The lower part of the program labeled "Table" is where the starting E ending addresses of each block is stored. The format is:

Table:
Starting Address 1; Two Bytes (low half first)
Ending Address 1; Two Bytes
Starting Address 2; Two Bytes
Ending Address 2; Two Bytes

| 1 | 1 |
| :--- | :--- |
| 1 | 1 |
| 1 | 1 |

Starting Address Last Ending Address Last

| NOP | ; | Four zero Bytes |
| :--- | :--- | :--- |
| NOP | Indicate end of table. |  |
| NOP |  |  |
| NOP. |  |  |

### 3.4 Wait State Selection

The MB-8A can be set for zero to eight wait states.

| $\begin{array}{r} \text { Prom Acce } \\ \text { (n s } \\ \hline \end{array}$ | Time* <br> c) |  |  | WD |  | ettings W2 | Wait Cycles | DIP Switch Notation |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Less than | 550 |  | 1 | $\emptyset$ | $\emptyset$ | $\emptyset$ | $\emptyset$ | $\emptyset=$ switch closed |
|  | 1050 |  | $\emptyset$ | 1 | 1 | 1 | 1 | l=switch open |
|  | 1550 |  | $\emptyset$ | $\emptyset$ | 1 | 1 | 2 |  |
|  | 2050 |  | $\emptyset$ | 1 | $\emptyset$ | 1 | 3 |  |
|  | 2550 |  | $\emptyset$ | $\emptyset$ | $\emptyset$ | 1 | 4 |  |
|  | 3050 |  | $\emptyset$ | 1 | 1 | $\emptyset$ | 5 |  |
|  | 3550 |  | $\emptyset$ | $\emptyset$ | 1 | $\emptyset$ | 6 |  |
|  | 4050 |  | $\emptyset$ | 1 | $\emptyset$ | $\emptyset$ | 7 |  |
| Less: than | 455ø |  | $\emptyset$ | $\emptyset$ | $\emptyset$ | $\emptyset$ | 8 |  |

*--. Prime 2708's normally do not require wait cycles.

### 3.5 Jump Address Selection

The MB-8A is equipped with a Power-On Clear or Reset Vector Jump Circuit. To activate this function, switch S2-JE must be switched to the closed (on) position. The Jump Select Connection has already been connected for Power-On Jump, but this small PC Jumper can be cut to allow for a Jumper Wire Selecting the Reset option.

The Jump circuit generates four Bytes onto the bus which are:

$$
\begin{aligned}
& \text { F3------Disable Interrupts } \\
& \text { C3------Jump Instruction, lst Byte } \\
& \text { mo-------Low Address, 2nd Byte } \\
& \text { YY--...--High Address, 3rd Byte }
\end{aligned}
$$

The last Byte (YY) can be set by switch $S 1$ which controls the high address (A8 thru A15). A switch position set to open (off) is a logic $\emptyset$ state and set to closed (on) as a logic 1 . Sl can be set for any address from $\emptyset \emptyset \emptyset \emptyset H$ to $F F \emptyset \emptyset H$ in 256 Byte increments.

Jump Address
$\emptyset \emptyset \emptyset \emptyset$ Hex $\emptyset 1 \varnothing \emptyset$ Hex $\emptyset 2 \emptyset \emptyset$ Hex
1
1
FFØD Hex

Setting of Sl
Al5 Al4 Al3 Al2 All Alø A9 A8

All Open (off)
All Open, Except $A 8=$ closed
All Open, Except $A 9=c$ losed

All Closed (On)

### 4.0 Trouble Shooting Hints

a. Check for proper settings of DIP switches.
b. Verify that all ICs are in the correct sockets.
c. Visually inspect all iCs to be sure that leads are in the sockets and not bent under.
d. Verify that the output voltage of each regulator is correct.
e. Inspect back side of board for solder bridges, running a small shar! knife blade between traces that appear suspicious. A magnifying glass is a must for this.
f. If you have an addressing problem:

1) Check U35 (7465136) for addresses Al4 \& Al5.
2) Check U28 (74367) for address A13.
3) Check U30 \& U34 (74L138) for addresses Al0 thru A12.
4) Check U27 \& U28 (7465367) for addresses Aø thru A9.
g. If you have a problem with data output (consistent missing bits):
5) Check outputs of buffers U32 \& U33 (74L5367) for shorts as well as proper operation.
6) Check signals on U23 (74L\$øø).
h. If you have a wait cycle problem:
7) Check signals on U23 (74L\$197)
8) Check signals on U31 (74L\$04)
9) Check signals on U36 (75453)
i. If you have a vector jump problem:
10) Check U26, U2 \& U14 if the jump code is wrong.
11) Check $U 26$ \& $U 29$ if no code sequence is sent out. Also check switch Sl-JE for proper operation.
j. If the "Magic Maping" feature doesn't work, then check out Ull $\varepsilon$ U29 for proper operation.

### 5.0 Theory of Operation

### 5.1 Us'eage

1) Ull (8-Input Nand, 74LS3 ( is a detector for "FF" Hex Bytes.
2) U23 (Presettable Binary Counter, 74197) is used to count Phase 2 cycles to give a number of different Wait State cycles depending on the settings of S 2 .
3) U26 (Hex D Flip-Flops, 74LS174) is used as a shift register to sequence the Jump code on to the bus for Power-On Jump.
4) U27, U28 (Hex Tri-State Buffers, 74LS367) are to buffer (isolate) the lower address lines (Aø thru A9, A13) onto the card.
5) U29 (Quad 2-Input Nand, 74 LSøø) is used as control logic for address enable, PDBIN strobe and PRDY functions on the card.
6) U3Ø, U34 ( 3 to 8 Decoder, 74 LS138) are used for decoding the addr ress for driving the appropriate chip select pin of the bank of 2708's.
7) U31 (Hex Inverter, 74LS@4) is used to buffer signal lines onto the card (Psync, Phase 2, Alø, All \& Al2).
8) U32, U33 (Hex Tri-State Buffers, 74LS367) are used for buffering the eight output data lines. These buffers are turn-on by PDBIN.

## 5.1 (continued)

9) U35 (Quad Exclusive-0r gates with open collectors, 74LS136) is used to compare the Dip Switch address selected with Al4 \& Als. This IC is also used as a phantom line driver and a enable gate for SMEMR status to the card.
10) 436 (Dual 2-Input or with open collectors, 75453 ) is used to drive the PRDY and PS bus lines.
11) Ui, U13 (340T-12) positive 12 volt regulators for the PROMS
12) U12, U24 (320T-5) negative 5 volt regulators for the PROMS.
13) U25 (340T-5) positive 5 volt regulator for logic power.

### 5.2 Operation

The MB-8 card uses U30 \& U34 for chip selection of the 2708's. U30 \& $U 34$ decode the address bits Alø, All, Al2 \& Al3 for address steps in $1 K$ increments. U30 \& U34 are only disabled during the Vector Jump operation of the card. $U 35$ is used to decode the address selection from S 2 against Al5 \& Al4 for a SMEMR state. If the address is valid, then a enable signal (logic 1) is sent to U29, pin 12, for a possible output data enable signal. U29 receives a address enable signal and a signal from Ull which is a "FF" code detector. The 'FF" detector will output a logic zero to U29, pin 13 if all ones are detected. U29 will provide an enable signal (U29, 'pin $3=\emptyset$ ) for output data to U32 \& U33, if the address is valid (U29, pin 13=1), and PDBIN signal is valid (U29, pin $2=1$ ).

The Wait State circuit uses a counter $U 23$ to count out the number of wait cycles. PSYNC drives the load enable of U 23 , pin 1 through a inverter U31. PSYNC loads U23 with a binary number from S2 which activates the PRDY signal to U36 pin 7. (logic $\emptyset$ ) Phase 2 pulses the clock of U23 which counts up from the binary number until U23, pin 5 goes high to turnon the PRDY signal.

The Vector Jump circuit is activated by a logic zero on pin 1 (clear) of U26. The logic zero signal can be PRESET or POC depending on the user selected Jumper wire. Switch S2, position JE, must be closed for the Vector Jump to operate.

U26 is connected up as a shift register to sequence (five cycles) out the Jump instruction onto the Computer's Bus. $U 26$ controls the Input Select, chip enable and some on the Input lines of the 74LS258 IC's (U2, U14). U26 is clocked through its sequence by a pulse form U29, pin 3 (PDBIN).

U2, 414 receive logic patterns on the A-select Inputs (pins 2, 5, 11, 4) for the Hex codes F3, C3, \& $\emptyset \emptyset$ from U26. These Hex codes give the computer a Disable Interrupt and $2 / 3$ of a Jump Command. The Final Byte (high address) of the Vector Jump is received from Switch Sl (8 bits) to the B-Select Inputs of U2 \& U14. After the four machine instruction Bytes,

## 5.2 (continued)

a fifth cycle is sequenced which turns off U2 \& U14.
During the whole Vector Jump operation U3Ø \& U34 are disable so that all the PROM's outputs are disable, and U2 \& U14 are enable so their TriState Outputs are turned-on.
6.0 Warranty

Parts guaranteed to original purchaser for 90 days, unless failure is due to misuse or failure of purchaser to excercise caution in addembly and operation. Registration card must be returned at time of purchase to validate warranty.

Assembled boards may be returned for service. A service charge will be made unless, in our judgement, the problem is due to a defective board or parts.



NOTE:
Place two plastic insulators sideways, as shown and underneath the regulator heat sink of the two negative voltage regulators ul2 6 u2t.


MB8A Parts List

Chip Pack
2 - U2,14
1 - U11
1 - U23
1 - U26
1 - U29
2-U30,34
1 - U31
1 - U36
4 - U27,28,32,33
1 - U35
Capacitor Pack

$$
\begin{aligned}
& 3-\mathrm{C} 3,8,11 \\
& 4-\mathrm{C}, 6,9,10 \\
& 4-\mathrm{C} 1,2,4,7
\end{aligned}
$$

Resistor Pack
5 - D1-5
6-R1-6
1 - R7
Hardware Pack

```
2 - U1,13
2 - U12,24
1 - U25
5
4
5
```


## Socket Pack

## 1

5
1
2
Misc.

74L\$258
74L\$30
74L\$197/8291
74L\$174
$74 \mathrm{~L} \$ 00$
74L\$138
74 L 04
75453
74367/8097
74L\$136

> 10uf, 20v
$0.1 u f$ disc
4.7uf 20v drop tant

1N4001 to 1N4006
$2.7 \mathrm{~K} \times 7$ SIP pack
$10 \mathrm{~K} \frac{1}{4} \mathrm{~W} 5 \%$

7812/340T-12
7905/320T-5
7805/340T-5
Heatsinks
Insulators
Sets \#6 hardware

24 pin socket
14 pin sockets
8 pin socket
8 position DIP switch

24 pin sockets
16 pin sockets
PC board
Warranty card Instruction manual

## Magic Mapping vs. Wait States

The magic mapping function will disable the outputting of data and wait states from the MB8A, if there is no ROM in the socket or the ROM's code is FF (Hex). Another way a ROM can generate an FF code is to be slow in responding to a chip select on pin 20. A slow ROM can disable its own wait state signal back to the computer.

In most computer systems today, the ROM's speed is better than 550 nanoseconds for chip select and the main system clock is 2 mhz , so no read problems occur. If the ROM is very slow or the computer is running at 4 mhz , then do the following:

1. Wait States wanted, but no Magic Mapping!
a. Remove Ull from the board to defeat Magic Mapping.
b. The MB8A is now a full 16 K ROM with/or without the ROMs in their sockets.
2. Wait States wanted and Magic Mapping!
a. Cut the very short trace going to U29, pin 9.

B. Jumper U29, pin 9 to U29, pin 10.


[^0]:    * See lllustration on page 12.

