OMTI 8640 Technical Reference Manual

Scientific Micro Systems, Inc.

OMTI 8640
AT - ESDI Controller
Technical Reference Manual
June, 1989

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OMTI 8640 AT - ESDI CONTROLLER TECHNICAL MANUAL

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1.1 PRODUCT DESCRIPTION

The OMTI 8640 controller is a combination ESDI disk drive and floppy disk controller for IBM AT Bus compatible computers (16 bit data path). The controller is contained on a single PCB that plugs into an empty slot of the computer's motherboard.

The OMTI 8640 controller uses SMS's sophisticated VLSI circuitry to provide many advanced features. These include:

- **Support for two ESDI disk drives. Drives may have different capacities or come from different manufacturers.**
- **Support for high capacity (up to 1.44 Megabytes) floppies.**
- **High performance (1:1 interleave on disk).**
- **32 Kbyte buffer minimum.**
- **Full Track Cache Option.**
- **56 bit Error Correction Code.**
- **Concurrent data operations on winchester and floppy disks.**
- **Support for Hard or Soft Sectored ESDI disk drives.**
- **Supports ESDI disks which run at a data rate of 10 Mbit/sec or the newer drives which run at 15 Mbit/sec.**
- **On-board BIOS which gives the user the following features:**

  Low level format utility.
  Ability to read the ESDI drive parameters.
  Automatic support for non-standard drive types.
  Ability to automatically read the ESDI defect map.
  Cylinder and Head skewing options.
  Surface Analysis to insure data reliability.

- **Sector level defect mapping.**
  Sector sparing and sector flagging options provided.
- **Variable sectors per track support.**
- **Conversion Mode. Based on 62 sectors per track and 16 heads. This mode automatically provides support for drives with greater than 1024 cylinders.**
- **8640 is XT height.**

1.2 SPECIFICATION

1.2.1 Features

WINCHESTER DISKS

- Operates up to two hard or soft sectored ESDI compatible Winchester disks.
- Support for ESDI Drive transfer rates of 10 Mbit/sec or 15 Mbit/sec.
- Supports programmable sector size.
- Supports programmable sector interleave including one to one interleave.
- Addresses up to 2048 tracks (cylinders) and 16 heads.
- Word (16 bits) width data transfer on AT bus.

FLOPPY DISKS

- Operates up to four floppy disk drives.
- Supports 48 and 96 TPI drives plus the high density AT compatible drives.
- Supports 250, 300, or 500 K bits/sec transfer rate including dual rotational speed floppies.
- Host has direct access to floppy disk controller chip (NEC 765 or equivalent).

1.2.2 Physical Specifications of the OMTI 8640 controller

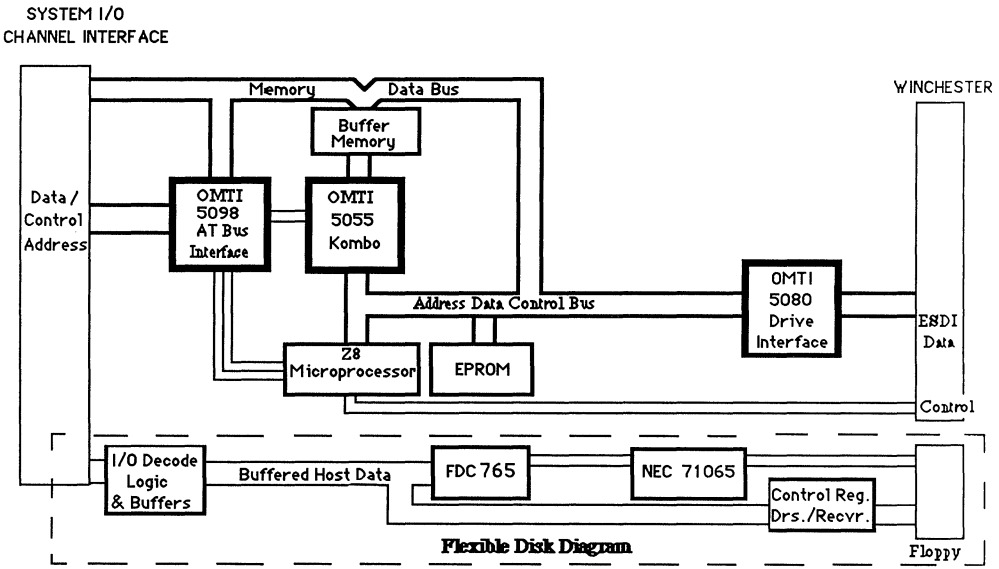
	8640
Length	13.25 inches
Height	3.9 inches
Width	.75 inches

1.2.3 Environmental Specifications

	Operating	Storage
Temperature	0 to 50 ° C	40 to 75 ° C
Relative Humidity	10 to 95% N.C.	10 to 95% Noncondensing
Maximum Wet Bulb	30 deg C	Noncondensing
Altitude	0 to 10,000 ft.	0 to 15,000 ft.

1.2.4 Power Requirements of the OMTI 8640 controller

Voltage	4.75 to 5.25 VDC
Maximum ripple and noise	100 mv
Maximum current drawn	1.0 Amp max



CONTROLLER BLOCK DIAGRAM

Figure 1.1 Functional Organization (Block Diagram)

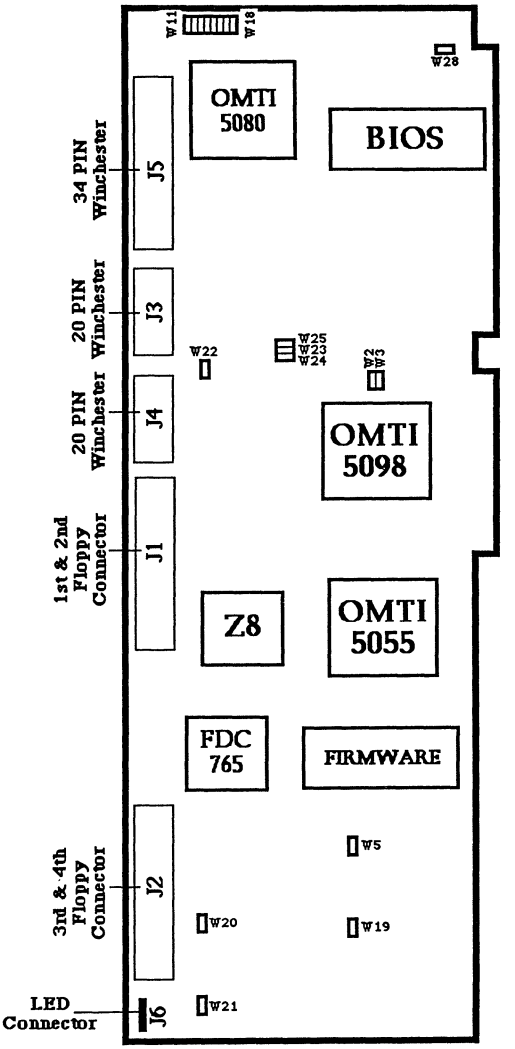


Figure 1.2 OMTI 8640 Bcard Layout

2.1. INTRODUCTION

The OMTI 8640 Data Controller is electrically and mechanically compatible with the bus or Input/Output channel used in the IBM AT computer. Physically this Input/Output channel is contained on two card edge connectors.

The Input/Output channel provides the necessary hardware interface to the host CPU to allow it to communicate with the controller.

2.2 INPUT/OUTPUT CHANNEL PIN ASSIGNMENTS

The following figures summarize pin assignments for the Input/Output channel connectors.

INPUT/OUTPUT CHANNEL (COMPONENT SIDE of 62 pin EDGE CONNECTOR)

I/O	Signal Name	Input/Output
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

Input/Output Channel (SOLDER SIDE of 62 pin EDGE CONNECTOR)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	O
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	-OWS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	O
B16	DRQ3	I
B17	-DACK1	O
B18	DRQ1	I
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	-DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5 Vdc	Power
B30	OSC	O
B31	GND	Ground

Input/Output Channel (COMPONENT SIDE of 36 pin EDGE CONNECTOR)

I/O Pin	Signal Name	I/O
C1	-SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SDO8	I/O
C12	SDO9	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

Input/Output Channel (SOLDER SIDE of 36 pin EDGE CONNECTOR)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS 16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ13	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5 Vdc	Power
D17	-MASTER	I
D18	GND	GND

2.3 INPUT/OUTPUT CHANNEL SIGNAL DESCRIPTION

The following is a description of the system boards INPUT/OUTPUT channel signals. All signal lines are TTL-compatible. Input/Output adapters should be designed with a maximum of two low-power Shottky (LS) loads per line. Signals preceded by a hyphen (-) indicate that the signal is in an active low state.

SA0 through SA19 (Input/Output)

Address bits 0 through 19 are used to address memory and Input/Output devices within the system. These 20 address lines, in addition to LA17 through LA23, allow access of up to 16Mb of memory. SA0 through SA19 are gated on the system bus when "BALE" is high and are latched on the falling edge of "BALE." These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the Input/Output channel.

LA17 through LA23 (Input/Output)

These signals (unlatched) are used to address memory and Input/Output devices within the system. They give the system up to 16Mb of addressability. These signals are valid when "BALE" is high. LA17 through LA23 are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by Input/Output adapters on the falling edge of "BALE." These signals also may be driven by other microprocessors or DMA controllers that reside on the Input/Output channel. Note that it is these signals that are decoded by the Input/Output adapter to generate "MEM CS16" for 16 bit, 1 wait -state memory cycles.

CLK (Output)

This is the 6-MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

RESET DRV (Output)

"Reset drive" is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SD0 through SD15 (Input/Output)

These signals provide bus bits 0 through 15 for the microprocessor, memory, and Input/Output devices. DO is the least-significant bit and D15 is the most significant bit. All 8-bit devices on the Input/Output channel should use DO through D7 for communications to the microprocessor. The 16-bit devices will use DO through D15. To support 8-bit devices, the data on D8 through D15 will be gated to D0 through D7 during 8-bit transfers to these devices; 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

BALE (Output)(buffered)

"Address latch enable" is provided by the 82288 Bus Controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the Input/Output channel as an indicator of a valid microprocessor or DMA address (when used with "AEN"). Microprocessor addresses SA0 through SA19 are latched with the falling edge of "BALE." "BALE" is forced high during DMA cycles. Note:"BALE" is usually used by the IO adapter only to latch the LA17-LA23 address lines (or the decode of LA17-LA23 that indicates an address match for the IO adapter). "BALE" may not occur on all 8-bit Input/Output cycles (which use only address lines SA0-SA9 for device decoding) or on some 8-bit memory transfers.

Input/Output CH RDY (Input)

"Input/Output channel ready" is pulled low (not ready) by a memory or Input/Output device to lengthen Input/Output memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles (167 nanoseconds). This signal should be held low for no more than 2.5 microseconds.

IRQ3-IRQ7, IRQ9-IRQ12 and IRQ 14 through 15 (Input)

Interrupt Requests 3 through 7, 9 through 12, and 14 are used to signal the microprocessor that an Input/Output device needs attention. These interrupt requests are prioritized, with IRQ9 through IRQ 12 and IRQ 14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine). Interrupt 13 is used on the system board and is not available on the Input/Output channel. Interrupt 8 is used for the real-time clock.

-IOR (Input/Output)

'Input/Output Read' instructs an Input/Output device to drive its data onto the databus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the Input/Output channel. This signal is active low.

-IOW (Input/Output)

"-Input/Output Write" instructs an Input/Output device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

-SMEMR (Output) -MEMR (Input/Output)

These signals instruct the memory devices to drive data onto the data bus. "-SMEMR" is active only when the memory decode is within the low 1Mb of memory space. "-MEMR" is active on all memory read cycles. "-MEMR" may be driven by any microprocessor or DMA controller in the system. -SMEMR" is derived from "-MEMR" and the decode of the low 1 Mb of memory. When a microprocessor on the Input/Output channel wishes to drive "-MEMR", it must have the address lines valid on the bus for one system clock period before driving "-MEMR active. Both signals are active LOW.

-SMEMW (Output) -MEMW (Input/Output)

These signals instruct the memory devices to store the data present on the data bus. "-SMEMW" is active only when the memory decode is within the low 1Mb of the memory space. "-MEMW" is active on all memory read cycles. "-MEMW" may be driven by any microprocessor or DMA controller in the system. "-SMEMW" is derived from "-MEMW" and the decode of the low 1Mb of memory. When a microprocessor on the Input/Output channel wishes to drive "MEMW", it must have the address lines valid on the bus for one system clock period before driving "-MEMW" active. Both signals are active low.

DRQ0-DRQ3 and DRQ5-DRQ7 (Input)

DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the Input/Output channel microprocessors to gain DMA service (or control of the system). They are prioritized, with "DRQ0" having the highest priority and "DRQ7" having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding "DMA Request Acknowledge" (DACK) line goes active. "DRQ0" through "DRQ3" will perform 8-bit DMA transfers; "DRQ5" through "DRQ7" will perform 16-bit transfers. "DRQ4" is used on the system board and is not available on the Input/Output channel.

-DACK to -DACK3 and -DACK5 to -DACK7 (Output)

-DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQ) through DRQ7). They are active low.

AEN (Output)

"Address Enable" is used to degate the microprocessor and other devices from the Input/Output channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus READ command lines (memory and Input/Output, and the Write command lines (memory and Input/Output).

-REFRESH (Input/Output)

This signal is used to indicate a refresh cycle and can be driven by a microprocessor on the Input/Output channel.

T/C (Output)

"Terminal Count" provides a pulse when the terminal count for any DMA channel is reached.

-SBHE (Input/Output)

"Bus High Enable" indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. Sixteen-bit devices use "-SBHE" to condition data bus buffers tied to SD8 through SD15.

-SBHE AND SAO ENCODINGS:

-SBHE	SAO	FUNCTION
0	0	WORD TRANSFER
0	1	BYTE TRANSFER ON SD8-SD15
1	0	BYTE TRANSFER ON SD0-SD7
1	1	RESERVED

-MASTER (Input)

This signal is used with DRQ line to gain control of the system. A processor or DMA controller on the Input/Output channel may issue a DRQ to a DMA channel in cascade mode and receive a "-DACK". Upon receiving the "-DACK", an Input/Output microprocessor may pull "-MASTER" low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After -MASTER" is low, the Input/Output microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

-MEM CS16 (Input)

"-MEM16 Chip Select" signals the system board if the present data transfer is a 1 wait-state, 16-bit memory cycle. It must be derived from the decode of LA17 through LA23. Note that this requires that all 16-bit memory devices must occupy at least 128 kbytes of address space on the Bus and must not decode the SA address lines as a condition to driving "-MEM CS16" as the SA lines are not valid in time to meet the "-MEM CS16" timing requirements. "-MEM CS16" should be driven with an open-collector or tri-state driver capable of sinking 20 mA.

-Input/Output CS16 (Input)

"-Input/Output 16 bit Chip Select" signals the system board that the present data transfer is a 16-bit, 1 wait-state, Input/Output cycle. It is derived from an address decode. "Input/Output CS16" is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

OSC (Output)

"Oscillator" (OSC) is a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

-OWS (Input)

The "Zero Wait State" (-OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, "-OWS" is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, "-OWS" should be driven active one system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. Note that "-OWS" must be synchronous to the system clock (CLK) and meet specific set-up and hold timing requirements to prevent undesirable system malfunction . "-OWS" is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

2.4 WINCHESTER TRACK AND SECTOR FORMAT (Soft Sectored ESDI Drives)

The standard track format for Winchester Disk drives is organized into numbered data segments, or sectors.

FORMAT TRACK FUNCTION START/RESTART STATE = 21h LOOP END STATE = 0Eh

FIELD	POST INDEX GAP	AM ENABL TIME	ID PRE-AMBLE	ID PRE-AMBLE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA ECC FIELD	DATA POST AMBLE	INTER SECTOR GAP	PRE INDEX GAP
SEQ-CNT	*PRM	03	*PRM	01	01	04	02	04	01	*PRM	01	N	06	04	*prm	01(H)

Standard ESDI Winchester Disk Sector Format

OMTI 8640: The number of sectors per track on most ESDI drives varies by vendor.

2.5 PIN ASSIGNMENTS

The following tables define the various Floppy Disk Drive's pin assignments .

2.5.1. FLOPPY DRIVE CONTROL AND DATA CONNECTOR (J1) PIN DESCRIPTION

SIG GND	SIG	SIGNAL PIN	SIGNAL MNEMONIC	I/O NAME
1	2	WCCNTRL-	WRITE CURRENT-CONTROL-	O
1 5	4	NC		
	6	NC		
7	8	INDEX-	INDEX-	I
9	10	MOTEN1-	MOTOR-ENABLE1-	O
15	16	MOTEN2-	MOTOR-ENABLE2-	O
11	12	DS2-	DRIVE-SELECT2-	O
13	14	DS1	DRIVE-SELECT1-	O
17	18	DIR	DIRCTION	O
19	20	STEP-	STEP-PULSE-	O
21	22	WRT DATA-	WRITE DATA-	O
23	24	WRT EN-	WRITE-DATA-	O
25	26	TRK0	TRACK0	I
27	28	WRT PROT	WRITE PROTECT	I
29	30	READ DATA	READ DATA	I
31	32	HS1	HEAD SELECT1	O
33	34	DISKETTE CHG	DISKETTE CHANGE	I

Pin One is designated by a square backing on the solder side of the board.

2.5.2. ESDI Winchester Disk Drive Interface

ESDI COMPATIBLE DISK DATA SIGNAL CONNECTOR (J3 &J4) RADIAL

PINS	FIXED DISKS
1	DRIVE SELECTED
2	SECTOR-ADDRESS MARK NOT FOUND
3	COMMAND COMPLETE
4	ADDRESS MARK ENABLE
5	RESERVED
6	GROUND
7	+WRITE REF CLOCK
8	-READ REF CLOCK
9	RESERVED
10	RESERVED
11	+READ REF CLOCK
12	-READ REF CLOCK
13	+NRZ WRITE DATA
14	-NRZ WRITE DATA
15	GROUND
16	GROUND
17	+NRZ READ DATA
18	-NRZ READ DATA
19	GROUND
20	INDEX

ESDI COMPATIBLE DISK CONTROL SIGNAL CONNECTOR (J5) CHAINED

	PINS	FIXED DISKS
GND	1 2	HEAD SELECT 3
	3 4	HEAD SELECT 2
	5 6	WRITE GATE
	7 8	CONFIG/-STATUS DATA
	9 10	TRANSFER ACK
	11 12	ATTENTION
	13 14	HEAD SELECT 0
	15 16	SECTOR/-ADDRESS MARK NOT FOUND
	17 18	HEAD SELECT 1
	19 20	INDEX
	21 22	READY
	23 24	TRANSFER REQ
	25 26	DRIVE SELECT 1
	27 28	DRIVE SELECT 2
	29 30	DRIVE SELECT 3
	31 32	READ GATE
GND	33 34	COMMAND/DATA

Pin One is designated by a square backing on the solder side of the board.

3.1 Handling (Caution)

It is recommended that you handle the controller by the edges of the card as some of the components are static sensitive and can be damaged by static.

3.2 Installation

The OMTI 8640 AT Compatible Data Controller is designed to plug directly into any unused 16 bit location on the system motherboard. The floppy and winchester disk drives are connected to the controller by ribbon cables. It is recommended that these cables do not exceed 20 feet in length.

3.3 Jumper Settings

W2 Floppy Primary/Secondary Address Setting

* 0 Primary Address
1 Secondary Address

W3 Winchester Primary/Secondary Address Setting

*0 Primary Address
1 Secondary Address

W5 Floppy Disable

*0 Floppy is enabled
1 Floppy is disabled

W16 Sectors per track

*0 Read from drive
1 Calculate and set

W17 Cache Option

*0 Cache disabled
1 Cache enabled

W18

*0 Disable Track Offset Command and disable Data Strobe Offset
1 Enable Track Offset Command and enable Data Strobe Offset

W19 Dual Speed Floppy

*0 Single Speed
1 Dual Speed

W20 J1 Floppy Connector Polarity

*1-2 Jumpered	Active High
2-3 Jumpered	Active Low

W21 J2 Floppy Connector Polarity

*1-2 Jumpered	Active High
2-3 Jumpered	Active Low

W23	W24	BIOS Base Address
*1	1	C8000
1	0	CA000
0	1	CC000
0	0	CE000

W25 BIOS Enable

0	BIOS Disabled
1	BIOS Enabled

W28 Chassis Ground

*0	Chassis not grounded.
1	Chassis grounded

*Designates how jumper is set when board is shipped.

****

3.4 Installation of Controller in system with one winchester drive.

1. Connect the floppy drive cable to position J1 on the 8640 Controller. Pin 1 on all connectors is specified by a square solder pad, visible on the soldered side of the board.

2. Winchester drive cabling requirements.
   - One (1) 34-pin straight through cable.
   - One (1) 20-pin straight through cable.

3. On winchester drive:
   - Install drive select jumper to lowest Drive Select (DSO or DS1).

4. Install the 34-pin winchester drive interface cable to the J5 connector.
   - Install the 20-pin data cable to either the J3 or J4 connector.

5. Attach the winchester activity LED connector to J6.

6. Install the controller in any available slot on the PC/AT motherboard. **CAUTION**: Power must be off!

7. Insert system Diagnostic Diskette (or execute internal diagnostics/setup program).

8. Turn on the power.

9. Enter setup routine.

10. Setup system options.

11. A) Select proper Drive Type. Consult your Technical Reference Manual for further information on the drive type table parameters. If your system BIOS does not contain an ESDI drive type, the BIOS on the 8640 will allow you to overide the drive table in the system BIOS. In this case you should setup the system for one Winchester disk drive, type 1.

    B) For highest performance using a 1:1 interleave, it is recommended you format your drive using the BIOS on the 8640 controller. You may access the BIOS by rebooting the system with DOS and inserting a diskette with the DEBUG program on it. Once you have done this type DEBUG and press <return>.
    If you have entered debug you will get the following prompt:
    -

12. Enter G=C800:6 and press <return>.
    The following screen will appear.

Screen 1

```
                    ***** OMTI 8640 Formatter Utility *****

Drive:0          # Cyls              # Heads          # Secs/Trk

This utility will destroy ALL DATA on your disk!!!

Press <RET> to proceed, <ESC> to cancel....
```

The utility will automatically display your drive characteristics (number of cylinders, heads and sectors per track). This utility will allow you to format your drive which will destroy all previous data on the disk.

Press <return> to continue to the next screen.

Screen 2

```
                    *****OMTI 8640 Formatter Utility*****

DRIVE PARAMETERS MODE

1)   Standard Table (# cylinders truncated to 1024)
2)   Translated Table
3)   Non-Standard Table (no cylinder truncation)

Enter choice: 1
```

This screen will only appear if your drive has more than 1024 cylinders. This screen allows you to choose the way in which the drive's parameters appear if your drive has more than 1024 cylinders. Option 1 will show the drive with its true head and sectors per track values but only 1024 cylinders will appear. Option 2 will show you a translation based on 16 heads and 62 sectors per track. Option 3 will show the true parameters of your drive. Remember that DOS cannot recognize a device which has more than 1024 cylinders. If your drive has more than 1024 cylinders you will require a device driver under DOS. Other operating systems such as XENIX and OS/2 also will not recognize a device with more than 1024 cylinders. When you have entered your choice, press <return> and continue.

Screen 3

```
***** OMTI 8640 Formatter Utility *****

DRIVE PARAMETERS MODE

1)    Standard Table (# cylinders truncated to 1024)
2)    Translated Table
3)    Non-Standard Table (no cylinder truncation)

Interleave (1-15) . . . . :
```

You should enter the interleave value you want to use. A value of one is recommmended for highest performance.

After you have entered your value, press <return> to continue.

Screen 4

```
***** OMTI 8640 Formatter Utility *****

DRIVE PARAMETERS MODE

1)    Standard Table (# cylinders truncated to 1024)
2)    Translated Table
3)    Non-Standard Table (no cylinder truncation)

Interleave (1-15) . . . . : 1
Head Skew (0-15) . . . :
```

You may obtain the correct Head Skew value from your drive manufacturer representative or drive reference manual. If you cannot obtain this value we recommend that you enter a value of 2, then press <return>.

Screen 5

```
***** OMTI 8640 Formatter Utility *****

DRIVE PARAMETERS MODE

1)      Standard Table (# cylinders truncated to 1024)
2)      Translated Table
3)      Non-Standard Table (no cylinder truncation)

Interleave (1-15) . . . . : 1
Head Skew (0-15) . . . : 2
Cylinder Skew (0-10) . . . :
```

Cylinder Skew, like Head Skew, is a value you may obtain from your drive manufacturer. These options allow you to maximize the performance of your ESDI Disk Drive, and will vary for every drive. Please do not call OMTI Technical Support for these values, you must get them from your drive manufacturer. If you are unsure of what value to enter, we recommend that you enter a value of 4. After you have entered your Cylinder Skew value, press <return> to continue.

Screen 6

```
***** OMTI 8640 Formatter Utility *****

DRIVE PARAMETERS MODE

1)      Standard Table (# cylinders truncated to 1024)
2)      Translated Table
3)      Non-Standard Table (no cylinder truncation)

Interleave (1-15) . . . . . : 1
Head Skew (0-15) . . . . . : 2
Cylinder Skew (0-10) . . : 4

DEFECT MANAGEMENT MENU

1)      Auto Defect Management
2)      Manual Defect Management
3)      No Defect Management

Enter choice: 1
```

Most ESDI disk drives have a defect map stored on the drive which the 8640 can read. You enable this feature when you choose the Auto Defect Management option. If you want to enter your own defect map you should choose the Manual Defect Management Option which begins at screen 11. If you want No Defect Management you may choose that option and then proceed to screen 15.

Screen 7

```
***** OMTI 8640 Formatter Utility *****

DRIVE PARAMETERS MODE

1)    Standard Table (# cylinders truncated to 1024)
2)    Translated Table
3)    Non-Standard Table (no cylinder truncation)

Interleave (1-15) . . . . : 1
Head Skew (0-15) . . . : 2
Cylinder Skew (0-10) . . : 4

DEFECT MANAGEMENT MENU

1)    Auto Defect Management
2)    Manual Defect Management
3)    No Defect Management

Enter choice: 1

1)    Sector flagging
2)    Sector sparing

Enter Choice: 1
```

The OMTI 8640 does its defect management on the sector level versus track level. This enables you to get the maximum capacity from your drive. The sector flagging option flags each bad sector the 8640 encounters.

Sector sparing saves one sector per track for defect management. This allows the track containing a defect to appear defect free. However it decreases total available storage space and can affect data transfer rates.

Screen 8 shows what appears if you enter the Auto Defect Management option with either sector flagging or sector mapping.

Screen 8

```
***** OMTI 8640 Formatter Utility *****

Building Defect List for head # 0 . . .

(Cyl, BFI) :        Cyl #      # Bytes from Index

Building defect list for head # 1

(Cyl, BFI) :        Cyl #      # Bytes from Index

Do you wish to see entire defect list (Y/N)? y
```

The above screen shows you the defect list for all heads on your drive. If you wish to see the entire defect list answer yes and press <return>.

Screen 9

```
***** OMTI 8640 Formatter Utility *****

     Cylinder      Head`      BFI

1.   Cyl. #        Head #     # of Bytes from Index

Press any key to continue . . .
```

After you have reviewed the complete defect list the last screen will look like the following:

Screen 10

```
***** OMTI 8640 Formatter Utility *****

Drive:0          # Cyls              # Heads          # Secs/Trk

Are you SURE you want to format (Y/N) ? y
```

If you wish to format enter a "Y" and press <return>. The format will destroy all previous data. Go to Screen 16 to continue this procedure.

****

If at screen 5 you chose the Manual Defect Management you should continue here:

Screen 11

```
***** OMTI 8640 Formatter Utility ******

Interleave (1-15) . . . . . : 1
Head Skew (0-15) . . . : 2
Cylinder Skew (0-10) . . : 4

DEFECT MANAGEMENT MENU

1)      Auto Defect Management
2)      Manual Defect Management
3)      No Defect Management

Enter Choice: 2

1)      Sector flagging
2)      Sector sparing

Enter Choice: 1
```

The OMTI 8640 does its defect management on the sector level versus track level. This enables you to get the maximum capacity from your drive. The sector flagging option flags each bad sector the 8640 encounters.

Sector sparing saves one sector per track for defect management. This allows the track containing a defect to appear defect free. However it decreases total available storage space and can affect data transfer rates

Screen 12

```
***** OMTI 8640 Formatter Utility *****

                                Defect Entry List
                              Cylinder    Head      BFI
(Press <RET> to end defect list)

CYLINDER. . . . . :
```

The BIOS will ask you your cylinder number for your first defect. Enter that number.

Screen 13

```
***** OMTI 8640 Formatter Utility *****

                                        Defect Entry List
                                    Cylinder    Head    BFI

(Press <RET> to end defect list)

CYLINDER. . . . . : 100                 100
HEAD . . . . . .: .: .: .:
```

In the example we entered a defective cylinder number of 100 and now we will enter a defective head number of 5.

Screen 14

```
***** OMTI 8640 Formatter Utility *****

                                        Defect Entry List
                                    Cylinder    Head    BFI

(Press <RET> to end defect list)

Cylinder . . . .:       100         100         5       1030
Head . . . . . :          5
Bytes from Index:       1030
```

A defect at cylinder 100, head 5, and 1030 bytes from index has now been entered. For this example we will press <return> to leave the defect management option.

Screen 15

```
***** OMTI 8640 Formatter Utility *****

Drive 0:            # Cyls           # Heads           #Secs/Trk

Are you SURE you wish to format (Y/N) ? y
```

To format, a "y" is entered. To leave this program and go back to DOS, enter an "n". The next screen will show the cylinder and head that is being formatted during the procedure:

Screen 16

```
***** OMTI 8640 Formatter Utility *****

Drive 0:          # Cyls          # Heads          # Secs/Trk

Are you SURE you want to format (Y/N//) ? y

Formatting Cylinder #            Head #
```

As soon as the last Cylinder and Head are formatted the following Screen will appear:

Screen 17

```
***** OMTI 8640 Formattter Utility *****

Drive 0:          # Cyls          # Heads          # Secs/Trk

Are you SURE you want to format (Y/N)? y

Formatting Cylinder #            Head #

Format Complete

Do you wish to perform a surface analysis (Y/N)? y
```

If you want to perform the surface analysis enter "y" then press <return>. If you do not want a surface analysis enter "n" then press <return> and you are finished.

Screen 18

```
***** OMTI 8640 Formatter Utility *****

Drive 0:          # Cyls          # Heads          # Secs/Trk

Are you SURE you want to format (Y/N) ? y

Formatting Cylinder #            Head #

Format Complete

Do you wish to perfrom a surface analysis (Y/N)? y

Verifying Cylinder 5  Head 9          <--- defect processed
Verifying Cylinder #  Head #
```

The utility will process all defects it encounters during the verify. Once the verify is done the screen will ask you to press any key to reboot, once you do this you will return to DOS and go on to FDisk.

Screen 19

```
                    ***** OMTI 8640 Formatter Utility *****

Drive 0:          # Cyls          # Heads          # Secs/Trk

Are you SURE you want to format (Y/N)? y

Formatting Cylinder #            Head #

Format Complete

Do you wish to perform a surface analysis (Y/N)? y

Verifying Cylinder 5  Head 9     <--- defect processed

Verify complete
Press any key to reboot . . .
```

13. Create a DOS partition by executing the FDISK utility.

14. Initialize the drive by executing the command: FORMAT C:/S

15. Your winchester should now be bootable drive C.

3.5 Installation of Two Drive System

1. On Winchester Drive

   - Set Drive Select to DS2 (or DS1) for drive D:
   - Install termination resistor on drive at end of daisy chain cable. Remove termination resistor on first drive on daisy chain cable.

2. Connect second drive to controller using 34-pin daisy chain straight through cable and one 20-pin straight through cable.

3. Follow steps 5 to 15 as defined in installing one drive system.

The OMTI 8640 contains 10 registers by which the host can communicate with the controller. This section describes the registers and command set that are supported by the Winchester disk portion of the 8640 controller.

The 8640 Register Addresses

Table 4.1

		I/O Address	
Primary	**Secondary**	**Read**	**Write**
1F0	170	Data Register	Data Register
1F1	171	Error Register	
1F2	172	Sector Count	Sector Count
1F3	173	Sector Number	Sector Number
1F4	174	Cylinder Number (LSB)	Cylinder Number (LSB)
1F5	175	Cylinder Number (MSB)	Cylinder Number (MSB)
1F6	176	SDH Select	SDH Select
1F7	177	Status	Command

Control and Status Registers

		I/O Address	
Primary	**Secondary**	**Read**	**Write**
3F2	372		Floppy Select/Control
3F4	374	Main floppy status	Main Floppy Status
3F5	375	Floppy Data	Floppy Data
3F6	376	Secondary status	Fixed Disk
3F7	377	Head/Select status	Rate Select

4.1 Read Register Definitions

4.1.1 Data Register 1F0 (170)

This register transfers controller data between the Host and the 8640. In Word Mode, 16 bits of data are transferred requiring I/O_CS_16 to be asserted and possibly deasserting I/O_CH_RDY. In Byte Mode, 8 bits of data are transferred leaving I/O_CS_16 deasserted and I/O_CH_RDY

4.1.2 Error Register 1F1 (171)

This register contains the error status of the last command executed by the controller. It can only be accessed while the controller is in the NOT BUSY state. This register is not affected by a reset. The data returned is only valid when the error bit is set.

Bit 7 - Bad Block Found — This indicates that the specified sector has previously been formatted with the Bad Track flag set in the ID field. It is not possible to access data on this sector.

Bit 6 - ECC Error — This indicates that a non-zero syndrome was detected in a specified data field. If the data error was corrected by ECC, Bit 2 of the Status Register will also be set and the command will continue if more sectors are specified. If the data error was not corrected by ECC, bit 0 of the Status Register will be set and the command terminated.

Bit 5 - Not used — Set to zero.

Bit 4 - ID not found — This indicates that the controller was able to locate the correct cylinder and head number but was unable to locate the correct sector. An ID CRC error can also generate this error condition.

Bit 3 - Not used — Set to zero.

Bit 2 - Aborted Command — The current command issued by the Host has been aborted due to an undefined Command, or a Write Fault/Not Ready condition exists on the selected drive.

Bit 1 - No Cylinder Zero — This indicates that during a recalibration command or if retries are enabled no Cylinder 000 was detected. This error occurs after the controller issues 2048 step pulses towards cylinder 000 and the selected drive does not respond with the Track 000 signal.

Bit 0 - No Data Mark Found — This indicates that the controller was able to locate the sector but was unable to locate the data mark associated with it.

4.1.3 Sector Count Register 1F2 (172)

The number of sectors transferred during a read, write, verify or format track command is determined by this register. A 0 in the sector count register specifies a 256 sector transfer. The initialize drive characteristics command must be performed before a multiple sector transfer. During a format command the number of sectors per track must be loaded into this register before each format track.

4.1.4 Sector Number Register 1F3 (173)

This register contains the current sector number being processed by the controller. It can only be accessed while the controller is in the Not Busy state. If an error condition exists, this register contains the sector number in error. It is set to 1 after a Reset.

4.1.5 Cylinder Number Register (LSB) 1F4 (174)

This register contains the least significant byte of the current cylinder number. It can only be accessed while the controller is in the Not Busy state. If an error condition exists, this register contains the least significant byte of the cylinder number in error. This register is set to 0 after a Reset.

4.1.6 Cylinder Number Register (MSB) 1F5 (175)

This register contains the most significant byte of the current cylinder number. It can only be accessed while the controller is in the Not Busy state. If an error condition exists, this register contains the most significant byte of the cylinder number in error. This register is set to 0 after a Reset.

4.1.7 SDH Register 1F6 (176)

This register contains the controller Error Code/Sector Size parameters along with the current Drive/Head select. It can only be accessed when the controller is Not Busy. This register is set to 0 after a reset.

Bit	Definition
7	Set to 1 the data field will be appended with an ECC field. Set to 0 the data field will be appended with a CRC field.
6 and 5	These bits indicate the sector size selected. Their definitions are:

6	5	
0	0	256 Bytes per Sector
0	1	512 Bytes per Sector
1	0	1024 Bytes per Sector
1	1	128 Bytes per Sector

4	Drive Select 0 is Drive 0 1 is Drive 1
3-0	Head Select. Bit 3 is the MSB with Bit 0 being the LSB.

4.1.8 Status Register 1F7 (177)

The status of the command is reported in this register after its execution. A read of this register clears interrupt request. Bit Definition:

7	**Busy**	This bit indicates the state of the controller. If set, the controller is busy executing the specified command and is not in a data transfer state. Any write to the Host Read/Write registers while this bit is set will be ignored. If cleared the controller is either in a Not Busy or a Data Transfer state. The DRQ bit will be set if the controller is in the Data Transfer state.
6	**Ready.**	This bit is an inverted copy of the Ready signal of the selected drive.
5	**Write Fault.**	This bit is an inverted copy of the Write Fault signal of the selected drive.
4	**Seek Complete**	This bit is an inverted copy of the Seek Complete signal of the selected drive.
3	**Data Request.**	This bit indicates that the controller is in a Data Transfer mode. While this bit is set, the Busy bit will be cleared and the controller will wait for data to be transferred to or from the host.
2	**Corrected**	When this bit is set it indicates the data read from the disk was properly corrected with the use of ECC. If CRC is selected, this bit has no meaning and is set to zero.
1	**Index.**	This bit is set on each revolution of the disk.
0	**Error.**	When set to 1 this indicates the previous command ended in an error and that the error register has been set. The next command clears this bit.

4.1.9 Secondary Status Register 3F6 (376)

This register contains the Controller/Drive status. It is identical to the Status Register at 1F7 (177).

4.1.10 Head\Select Status Register 3F7 (377)

This register contains the Head/Drive Select status. The bit definitions are:

Bit 7 - Diskette Change	This bit indicates the state of the floppy Disk Change signal If set, no diskette, door open or Drive Not Ready condition.
Bit 6 - Write Gate	This bit indicates the state of the Winchester 'Write Gate signal'.

Bit 5 - Head Select 3/RWC	This bit indicates the state of Head Select 3.
Bit 4 - Head Select 2	This bit indicates the state of Head Select 2.
Bit 3 - Head Select 1	This bit indicates the state of Head Select 1.
Bit 2 - Head Select 0	This bit indicates the state of Head Select 0.
Bit 1 - Drive Select 1	This bit indicates the state of Drive Select 1. If set to 0, Drive 1 is selected.
Bit 0 - Drive Select 0	This bit indicates the state of Drive Select 0. If set to 0 Drive 0 is selected.

4.2 8640 Write Register Definitions

4.2.1 Data Register 1F0 (170)

This register transfers controller data between the 8640 and the HOST. In WORD MODE, 16 bits of data are transferred requiring I/O_CS_16 to be asserted and possibly de-asserting I/O_CH_RDY. In BYTE MODE, 8 bits of data are transferred leaving I/0_CS_16 deasserted and I/O_CH_RDY asserted.

4.2.2 Sector Count Register 1F2 (172)

The number of sectors transferred during a read, write, verify or format track command is determined by this register. A 0 in the sector count register specifies a 256 sector transfer. The initialize drive characteristics command must be performed before a sector transfer. During a format command the number of sectors per track must be loaded into this register before each format track.

4.2.3 Sector Number Register 1F3 (173)

This register specifies the starting sector number. It should be written prior to the Command Register being written. This register is set to 1 after a reset.

4.2.4 Cylinder Number Register (LSB) 1F4 (174)

This register specifies the least significant byte of the starting cylinder number. It should be written prior to the Command register being written. This register is set to 0 after a Reset.

4.2.5 Cylinder Number Register (MSB) 1F5 (175)

This register specifies the most significant byte of the starting cylinder number. It should be written prior to the Command Register being written. This register is set to 0 after a Reset.

4.2.6 SDH Register 1F6 (176)

This register specifies the controller Error Code/Sector Size parameters along with the Drive/Head select. This register should be written prior to the Command Register being written. This register is set to 0 after a Reset. The bit definitions are:

Bit **Definition**

7 This bit specifies the error code to be selected. If this bit is set the data field will be appended with an ECC field. If cleared the data field will be appended with a CRC field.

6 and 5 These bits indicate the sector size selected. Their definitions are:

6	5
0	0 - 256 Bytes per Sector
0	1 - 512 Bytes per Sector
1	0 - 1024 Bytes per Sector
1	1 - 128 Bytes per Sector

4 Drive Select
0 is Drive 0
1 is Drive 1

3-0 Head Select. Bit 3 is the MSB with Bit 0 being the LSB.

4.2.7 Command Register 1F7 (177)

This register accepts commands for Winchester operations. Table 4.2 lists the commands supported.

Table 4.2

Command	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Recalibrate	0	0	0	1	0	0	0	0
Seek	0	1	1	1	0	0	0	0
Read Sector	0	0	1	0	0	0	L	R
Write Sector	0	0	1	1	0	0	L	R
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	R
Diagnostic	1	0	0	1	0	0	0	0

Table 4.2 (continued)

	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
Set Parameters	1	0	0	1	0	0	0	1
Initiate ESDI	1	1	1	0	0	0	0	0
Start/Stop Motor	1	1	1	0	0	0	0	1
Read Data Buffer	1	1	1	0	0	1	0	0
Write Data Buffer	1	1	1	0	1	0	0	0
Read Parameters	1	1	1	0	1	1	0	0
Read ESDI Defect List	0	0	1	0	0	1	0	0
Cache Control	1	1	1	0	1	1	1	1

L = When set to 1 a Read or Write Long has occurred and 4 (of 7) ECC bytes will be transferred.
R = When set to 1 Retries are disabled.

4.2.8 Recalibrate (10H)

The drive specified is stepped toward the outside cylinder until either Track Zero signal is detected or more steps have been issued than available cylinders for the device type. The controller issues one step pulse, waits for seek complete, and tests the Track 000 signal.

4.2.9 Seek (70H)

This command causes the read/write heads to be physically positioned to the cylinder specified in the cylinder high and low registers. If executed in the buffered mode step pulses and command complete will be issued before the seek is complete, allowing an overlapped seek.

4.2.10 Read Sector (20H)

This command specifies the number of sectors (1-256) to be read from the Winchester Disk with or without the ECC field appended (ECC field is appended if Read Long bit is set). The sector count register determines the number of sectors to be transferred. If a read is issued prior to initialization of a step rate the default value will be used. If the retries bit is set to 0, up to ten retries will be performed before an error is reported. If the retries bit is set to 1 only two retries will be executed. Interrupts occur as each sector is ready to be read, there is no interrupt at the end of a command.

4.2.11 Write Sector (30H)

This command specifies the number of sectors (1-256) to be written to the Winchester Disk with or without the ECC Bytes appended by the Host (ECC field is appended if Write Long bit is set). The sector count register is used to determine the number of sectors to be transferred. If a write is issued prior to initialization of a step rate the default value is used. If the retries bit is set to 0 up to ten retries will be performed before an error is reported. If the retries bit is set to 1 only two retries will be executed. Interrupts are generated as each sector is transferred into the Sector Buffer (except the first sector) and at the end of the command.

4.2.12 Format Track (50H)

The track specified in the task file is formatted with ID and data fields according to the interleave table that is transferred to the buffer. The sector count register must be loaded with the number of sectors per track before each Format Track command. An interrupt is generated at the end of this command. There are no valid errors for this command.

4.2.13 Read Verify (40H)

This command is similiar to a read sector with the difference being that no data is transferred during a read verify. If this command is issued prior to initialization of a step rate the default value of 7.5 msec is used and a recalibrate is performed first. Any number of sectors may be transferred up to 256, the ECC bytes generated are compared with those that were recorded to verify data integrity. An interrupt is generated at the end of this command or when an error is encountered.

4.2.14 Diagnostic (90H)

This command causes the Controller to perform an on-board diagnostic and report the result in the Error Register. This command tests the Interface, Buffer, RAM, Sequencer and ROM. The error codes that can be reported in the error register are:

01	NO ERROR
02	CONTROLLER INTERFACE FAILURE
03	CONTROLLER BUFFER RAM FAILURE
04	SEQUENCER FAILURE
05	CONTROLLER ROM FAILURE

4.2.15 Set Parameters (91H)

This command sets up the drive parameters specifying the maximum number of heads and sectors per track. This command must be issued before any multiple sector operations are begun. The drive/head select register should be used to specify the drive which is having its parameters set. This allows drives to have different parameters.

4.2.16 Read ESDI Defect List (24H)

This command causes the specified drive to return 512 bytes of drive manufacturer recorded defect list during the data-in phase of the command execution. Only the list for the specified head will be returned. The head is specified in the 1F6 register. The data is returned in the following manner:

Defect List Data Format
Header

Byte	
0	MONTH
1	DAY
2	YEAR
3	HEAD NUMBER
4	Zero Value
5	Zero Value

Bytes 0-2 return the date at which the list was recorded.

DEFECT Descriptor Format

Byte	
6	Cylinder (MSB)
7	Cylinder (LSB)
8	Byte Count from Index (MSB)
9	Byte Count from Index (LSB)
10	Error Length (In Bits)

Each defect is listed with a 5 byte field as described above.

End of List Format

xx-4	FF
xx-3	FF
xx-2	FF
xx-1	FF
xx	FF

Five ff bytes indicate the end of the defect list.

4.2.17 Start/Stop Motor (E1H)

To start the motor bit 1 of register (1F1) must be set. To stop the motor this bit must be set to 0.

4.2.18 Read Data Buffer (E4H)

This command causes data to be written from the host to the controller's buffer.

4.2.19 Write Data Buffer (E8H)

Data from the controller's buffer is returned to the host when this command is executed.

4.2.20 Read Parameters (ECH)

This command retrieves the drive configuration from the ESDI Drive.

4.2.21 Cache Control (EFH)

This command controls the read ahead buffer which is used on the 8640. To enable or disable the cache the user must write the correct code to the Precomp Register (1F1).

AA= Cache enabled
55= Cache disabled

4.2.22 Initiate ESDI (E0H)

This command enables the system processor to send instructions directly to the selected drive by loading the cylinder register (high and low) and executing the Initiate command. the host fills the cylinder registers with the command it wants to execute prior to issuing the Initiate ESDI command. The controller then processes the data and sends it to the drive. After the drive completes the command it sends completion status back to the controller.

ESDI Commands

Command Function Bit				Command Function Definition	Command Modifier Applicable	Command Parameter Applicable	Status returned to controller
15	14	13	12	Bits 11-8	Bits 11-0		
0	0	0	0	Seek	No	Yes	No
0	0	0	1	Recalibrate	No	No	No
0	0	1	0	Request Status	Yes	No	Yes
0	0	1	1	Request Configuration	Yes	No	Yes
0	1	0	0	Select Head Group	No	Yes	No
0	1	0	1	Control	Yes	No	No
0	1	1	0	Data strobe Offset	Yes	No	No
0	1	1	1	Track Offset	Yes	No	No
1	0	0	0	Initiate Diagnostics	No	Yes	No
1	0	0	1	Set Bytes per Sector	No	Yes	No
1	0	1	0	Reserved			
1	0	1	1	Reserved			
1	1	0	0	Reserved			
1	1	0	1	Reserved			
1	1	1	0	Set Configuration	No	Yes	No
1	1	1	1	Reserved			

ESDI Request Configuration

Command Modifier Bits				Function
11	10	9	8	
0	0	0	0	General Configuration Response Bits
0	0	0	1	Number of Cylinders - Fixed
0	0	1	0	Number of Cylinders - Removeable
0	0	1	1	Number of Heads
0	1	0	0	Unformatted Bytes per Track
0	1	0	1	Unformatted Bytes per Sector
0	1	1	0	Number of Sectors per Track
0	1	1	1	Bytes in ISG Field
1	0	0	0	Bytes per PLO Sync Field
1	0	0	1	Number of Vendor uniques status words available
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Vendor Identification

ESDI General Configuration Response Word

Bit Position	Function
15	0 is magnetic disk drive, 1 is non-magnetic disk drive.
14	1 is format speed tolerance gap required.
13	1 is track offset option available.
12	1 is data strobe offset option available.
11	1 is rotational speed tolerance >0.5%.
10	1 is transfer rate > 10MHz.
9	1 is transfer rate > 5MHz.
8	1 is transfer rate of 5MHz.
7	1 is a removeable cartridge drive.
6	1 is a fixed drive.
5	1 is spindle motor control option implemented.
4	1 is head swithch time > 15 seconds.
3	1 is not MFM.
2	1 is controller soft sectored.
1	1 is hard sectored.
0	Reserved.

ESDI Status Response Bits

Bit	Function
15	Reserved
14	1 is removeable media not present.
13	1 is write protected removeable media, 0 is non removable media.
12	1 is write protected fixed media.
11	Reserved.
10	Reserved.
9	1 is spindle motor stopped by stop command.
8	1 is power on reset condition exists.
7	1 is command data parity fault.
6	1 is interface fault.
5	1 is invalid or unimplemented command fault.
4	1 is seek fault.
3	1 is write gate with track offset fault.
2	Vendor unique status available.
1	1 is a write fault.
0	1 is removable media changed since last request.

ESDI Configuration Data

Number of Cylinders
Number of Removeable Cylinders
Number of Heads
Unformatted bytes/track
Unformatted bytes/sector
Sectors/track
Minimum number of bytes in ISG
Minimum number of bytes in PLO
Number of words of vendor unique status

Controller Information

8640 X.A MM/DD/YY

This information signifies the revision level of firmware and date of revision.

X= revision level in an alpha character.
A= revision level in numeric character.
M= month of revision.
D= Date of revision.
Y= year of revision.

4.2.23 Fixed Disk Register 3F6 (376)

Bit 4 - 7	0
Bit 3 HS3EN	When set to 0 this enables reduced write cylinder
Bit 2 Reset	This bit must be enabled for a minumum of 5 µ seconds the bit must be turned off to complete the reset function.
Bit 1 EN	Interrupt Enable enables or disables IRQ 14. A system reset clears the interrupt while leaving the interrupt enabled.
Bit 0	0

5.1. FLOPPY DISK REGISTERS

There are five I/O registers (eight bits) which the host accesses to communicate with the floppy disk portions of the OMTI 8640 controller. The address of these registers is selectable (See Section 3) to be either at the primary or secondary location as shown in table 4-1.

Table 5-1

I/O Address			
Primary	**Secondary**	**Read**	**Write**
3F2h	**372h**		**Floppy Select/ Control**
3F4h	**372h**	**Main Floppy Status**	**Main Floppy Status**
3F5h	**375h**	**Floppy Data**	**Floppy Datga**
3F6h	**376h**	**Secondary Status**	**Fixed Disk**
3F7h	**377h**	**Head/Select Status**	**Rate Select**

The host uses the Main Floppy Status and Data Register to issue commands to and receive status from the controller. The Digital Input, Digital Output and Diskette Control Register and Additional Control Registers are used to control the specific drive functions as shown:

Read Register		Definition
Main Floppy Status (3F4/374)		This is a read only register used in conjuntion with the Data register to transfer commands to the controller.
	Bit 7	Request for Master (RQM). Indicates that the data register is ready to send or receive data. This bit must be used by the host to perform handshaking functions between the host and controller. This bit is cleared by reading or writing the Data Register.
	Bit 6	Data In/Out (DIO) indicates direction of data transfer. If DIO = 1, then transfer is from the Data Register to the host. If DIO = 0, then it is from the host to the Data Register.

Read Register (Continued)		Definition
	Bit 5	Non-DMA mode when 1. This can occur only during execution phase.
	Bit 4	When 1, the controller is busy executing a command.
	Bit 3, 2	Reserved
	Bit 1	Drive B is in the Seek mode when 1.
	Bit 0	Drive A is in the Seek mode when 1.

Write Register		Definition
Floppy Select/Control (3F2/372)		This is an output only register used to control drive motors, drive selection, interrupts/DMA and reset. All bits are cleared when a channel reset occurs.
	Bit 7	Drive D Motor Enable when 1.
	Bit 6	Drive C Motor Enable when 1.
	Bit 5	Drive B Motor Enable when 1.
	Bit 4	Drive A Motor Enable when 1.
	Bit 3	Interrupts and DMA enable when 1.
	Bit 2	Reset floppy disk function when 0. The floppy disk function comes out of reset when this bit is set to 1.
	Bit 1	Select Drive-C/D. 0 selects drive C. 1 selects drive D.
	Bit 0	Select Drive-A/B. 0 selects drive A. 1 selects drive B.
Floppy Rate Select (3F7/377)		This is an output only register which gives the controller data rate information. All bits are cleared when a channel reset occurs.
	Bits 2-7	Reserved
	Bits	**1 0 Data Rate** 0 0 500 Kbits/sec 0 1 300 Kbits/sec 1 0 250 Kbits/sec 1 1 Reserved

Read/Write Register	Definition
Floppy Data (3F5/375)	This register is used to transfer information to/from the host. This register can be logically viewed as several registers in a stack with only one presented at any time. Data bytes are read out of or written into the Data register in order to program a command or obtain the results after the execution of a command.

5.2 FLOPPY DISK PROTOCOL

The host sends commands to the controller by sending several bytes of information to the controller (via the Data register) synchronized with bits 6 and 7 in the Status register. The sending of command data is called the command phase. The controller then goes "Busy" and executes the command (the command phase). Upon completion of the command the controller becomes "not busy" and results may be obtained from the Data register again synchronized with bit 6 and 7 in the Status register. Floppy commands, parameters and results are listed in section 4.5.

FLOPPY DISK FUNCTIONS

5.3 FLOPPY DISK COMMAND SUMMARY

The following is a list of commands that may be issued to the Floppy section of the combination disk controller.

- READ DATA
- FORMAT TRACK
- SCAN EQUAL
- SCAN LOW OR EQUAL
- SCAN HIGH OR EQUAL
- RECALIBRATE
- SENSE INTERRUPT STATUS
- SPECIFY
- SENSE DRIVE STATUS
- SEEK
- INVALID

5.4 DESCRIPTION OF SYMBOLS

The following are descriptions of the symbols used in the "Command Definitions" later in this section.

AO Address Line 0 - A0 selects the main status register, and a 1 selects the data register.

C Cylinder Number - Contains the current or selected cylinder number in binary notation.

D Data - Contains the data pattern to be written to a sector.

D7-D0 Data Bus - An 8-bit data bus in which D7 is the most significant bit and D0 is the least-significant.

DTL Data Length - When N is 00, DTL is the data length to be read from or written to a sector.

EOT End of Track- The final sector number on a cylinder.

GPL Gap Length - The length of gap 3 (spacing between sectors excluding the VCO synchronous field).

H Head Address - The head number, either 0 or 1, as specified in the ID field.

HD Head - The selected head number, either 0 or 1. (H=HD in all command words).

HLT Head Load Time - The head load time in the selected drive (2 to 256 millisecond increments for the 1.2Mbyte drive and 4 to 512 milliseconds in 4 millisecond increments for the 320K-byte drive).

HUT Head Unload Time - The head unload time after a read or write operation (0 to 240 milliseconds in 16 millisecond increments for the 1.2M-byte drive and 0 to 480 milliseconds in 32 millisecond increments for the 320K-byte drive.

MF FM or MFM Mode - A0 selects FM mode and a 1 selects MFM. (MFM is selected only if it is implemented).

MT Multitrack - A1 selects multitrack operation. (Both HD0 and HD1 will be read or written).

N Number - The number of data bytes written in a sector.

NCN New Cylinder - The new cylinder number for a seek operation.

ND Non-Data Mode - This indicates an operation in the non-data mode.

PCN Present Cylinder Number - The cylinder number at the completion of a Sense interrupt status command (present position of the head).

R Record - The sector number to be read or written.

R/W Read/Write - This stands for either a 'read' or 'write' signal.

SC Sector - The number of sectors per cylinder.

SK Skip - This stands for skip deleted-data address mark.

SRT This 4 bit byte indicates the stepping rate for the diskette drive as follows:

1.2MByte Diskette Drive

1111 1 millisecond
1110 2 milliseconds
1101 3 milliseconds

320KByte Diskette Drive

1111 2 milliseconds
1110 4 milliseconds
1101 6 milliseconds

ST0-ST1 Status 0-Status 3 - One of the four registers that stores status information after a command is completed.

STP Scan Test - If STP is 1, the data in contiguous sectors is compared with the data sent by the processor during a scan operation. If STP is 2, then alternate sectors are read and compared.

US0-US1 Unit Select - The selected driver number encoded the same as bits 0 and 1 of the digital output register (DOR).

5.5. FLOPPY COMMANDS

The following are commands that may be issued to the floppy section of controller.
NOTE: An X is used to indicate a don't care condition.

5.5.1. READ DATA command

Command Phase : The following bytes are issued by the processor in the command phase:

MT	MF	SK	0	0	1	1	0
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
DTL							

Result Phase : The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

5.5.2 FORMAT A TRACK Command

Command Phase: The following bytes are issued by the processor in the command phase :

0	MF	0	0	1	1	0	0
X	X	X	X	X	HD	US1	US0
N							
SC							
GPL							
D							

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

5.5.3 SCAN EQUAL Command

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	0	0	0	1
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
STP							

Result Phase: The following bytes are issued by the controller in the result phase:
ST0
ST1
ST2
C
H
R
N

5.5.4. SCAN LOW OR EQUAL Command

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	1	0	0	1
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
STP							

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

5.5.5. SCAN HIGH OR EQUAL Command

Command Phase: The following bytes are issued by the processor in the command phase:

MT	MF	SK	1	1	1	0	1
X	X	X	X	X	HD	US1	US0
C							
H							
R							
N							
EOT							
GPL							
STP							

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

5.5.6. RECALIBRATE Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	0	1	1	1
X	X	X	X	X	0	US1	US0

Result Phase: This command has no result phase.

5.5.7. SENSE INTERRUPT STATUS Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	1	0	0	0

Result Phase: The following bytes are issued by the controller in the result phase:

STO
PCN

5.5.8. SPECIFY Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	0	0	1	1
(SRT)		(HUT)					
(HLT)		ND					

Result Phase: This command has no result phase.

5.5.9. SENSE DRIVER STATUS Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	0	0	1	0
X	X	X	X	X	HD	US1	US0

Result Phase: The following bytes are issued by the controller in the result phase:
ST3

5.5.10. SEEK Command

Command Phase: The following bytes are issued by the processor in the command phase:

0	0	0	0	1	1	1	1
X	X	X	X	X	HD	US1	US0
NCN							

Result Phase: This command has no result phase.

5.5.11. INVALID Command

Command Phase: The following bytes are issued by the processor in the command phase:

Invalid Codes

X X X X X HD US1 US0

Result Phase: The following bytes are issued by the controller in the result phase:
ST0

5.6. COMMAND STATUS REGISTERS

The following is information about the command status registers ST0 through ST3.

5.6.1. Command Status Register 0 (ST0)

The following are bit definitions for command status register 0.

Bit 7-Bit 6 Interrupt Code (IC)

- 00 Normal Termination of Command (NT) - The command was completed and properly executed.
- 01 Abrupt Termination of Command (AT) - The execution of the command was started but not successfully completed.
- 10 Invalid Command Issue (IC) - The issued command was never started.
- 11 Abnormal termination because, during the execution of a command, the 'ready' signal from the diskette drive changed state.

Bit 5 Seek End (SE) - Set to 1 when the controller completes the Seek command.

Bit 4 Equipment Check (EC)- Set if a 'fault' signal is received from the diskette drive, or if the 'track-0' signal fails to occur after 77 step pulses (Recalibrate Command).

Bit 3 and 2 Not Used - Always zero

Bit 1-Bit 0 Unit select 1 and 2 (US 1 and 2) - Indicate a drive's unit number at interrupt.

5.6.2. Command Status Register 1 (ST1)

The following are bit definitions for command status registers 1.

Bit 7 End of Cylinder (EC) - Set when the controller tries to gain access to a sector of a cylinder.

Bit 6 Not Used-Always 0.

Bit 5 Data Error (DE) - Set when the controller detects a CRC error in either the ID field or the data field.

Bit 4 Overrun (OR) - Set if the controller is not serviced by the main system within a certain time limit during data transfers.

Bit 3 Not Used - This bit is always set to 0.

Bit 2 No Data (ND) - Set if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or Scan Command. This flag is also set if the controller cannot read the ID field without an error during the execution of a Read ID command or if the starting sector cannot be found during the execution of a Read Cylinder command.

Bit 1 Not Writeable (NW) - Set if the controller detects a 'write-protect' signal from the diskette drive during execution of a Write Data, Write Deleted Data, or Format Cylinder command.

Bit 0 Missing Address Mark (MA) - Set if the controller cannot detect the ID address mark. At the same time, the MD of status register 2 is set.

5.6.3. Command Status Register 2 (ST2)

Bit 7 Not Used - Always zero.

Bit 6 ****Control Mark (CM) - This flag is set if the controller encounters a sector that has a deleted data-address mark during execution of a Read Data or Scan command.

Bit 5 Data Error in Data Field (DD) - Set if the controller detects an error in the data.

Bit 4 Wrong Cylinder (WC) - This flag is related to ND (no data) and when the contents of C on the medium are different from that stored in the ID register, this flag is set.

Bit 3 Scan Equal Hit (SH) - Set if the contiguous sector data equals the processor data during the execution of a Scan command.

Bit 2 Scan Not Satisfied (SN) - Set if the controller cannot find a sector on the cylinder that meets the condition during a Scan command.

Bit 1 Bad Cylinder (BC) - Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, this flag is set.

Bit 0 Missing Address Mark in Data Field (MD) Set if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

5.6.4. Command Status Register 3 (ST3)

The following are bit definitions for command status register 3.

Bit 7 Not used - always zero.

Bit 6 Write Protect (WP) - Status of the 'write-protect' signal from the diskette drive.

Bit 5 Not used - always zero.

Bit 4 Track 0 (T0) - Status of the 'ready' signal from the diskette drive.

Bit 3 Not used - always zero.

Bit 2 Head Address (HD) - Status of the 'side-select' sig: al to the diskette drive.

Bit 1 Not used - always zero.

Bit 0 Not used - always 1.