SDC-RLV12
Winchester Controller
Manual

Sigma

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Section 1 - General Information

1.1 INTRODUCTION

This manual provides the necessary information to install and operate the SDC-RLV12 winchester disk controller manufactured by Sigma Information Systems, Anaheim, California.

The material is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a brief general description of the SDC-RLV12 and the specifications for the controller module.

Section 2 - INSTALLATION AND DIAGNOSTICS. This section explains the procedures for equipment installation and diagnostic testing.

Section 3 - PROGRAMMING CONSIDERATIONS. This section contains register data bit functions and provides programming examples using register bit definitions.

1.2 GENERAL DESCRIPTION

The SDC-RLV12 is a dual-wide single module 5 1/4" winchester controller that interfaces with the Xebec S1410 or Adaptec ACB4000 formatter and/or Iomega ALPHA 10.5 removable media drive with onboard SASI formatter. The drive subsystem emulates the DEC* RL01/RL02 disk subsystem.

The compact controller is pin-to-pin, signal, and power compatible with Q bus* backplanes that support LSI-11 CPUs and associated modules. It plugs directly into any Q bus slot.

The SDC-RLV12 is software compatible with DEC operating systems and diagnostics designed for the RL01/RL02.

1.3 FEATURES

- Controller contained on one dual-wide module
- 22-bit addressing capability
- Error Correction (ECC)
- Multi-level interrupt priorities
- Drive configuration PROM allows selection of up to four different drive types
- Drives can be configured as either RL01 or RL02
- Mixed capacity drives support
- Transparent firmware boot
- Selectable device/vector addresses
- REMAKE Z-TRACK function for Iomega disk drives

*DEC is a registered trademark of Digital Equipment Corporation.

1.4 SPECIFICATIONS

Power Requirements:	5VDC at 2.5A typical.
Priority Level:	Selectable. Compatible with LSI-11/23
Device Address:	774400 standard. Selectable fixed alternate.
Interrupt Vector:	160 (octal) standard. Selectable fixed alternate.
Bus Load:	1
Interface:	SASI bus
Media:	Fixed
Recording Method:	Modified frequency modulation (MFM)
Drives/controller:	2 (up to 4 logical units)
Error Detection:	Cyclic redundancy check (CRC) on data and headers. 11-bit ECC
Cable:	Requires 50-conductor ribbon cable to Xebec/ Adaptec formatter or Alpha 10.5 drive (not included).
Dimensions:	Standard dual-wide module. 10.45" (26.6cm)H x 8.94" (22.7cm)L.
Installation:	Plugs directly into any Q bus slot.
Temperature	
Operating:	0°C to 50°C
Storage:	-16°C to 60°C
Humidity:	10% to 95% noncondensing

Section 2 - Installation and Diagnostics

2.1 INTRODUCTION

This section provides the information necessary to configure and install the SDC-RLV12. Information concerning selectable device addressing, interrupt vectors, and drive configuration PROM is included.

The SDC-RLV12 is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

Unpack the SDC-RLV12 and visually inspect for physical damage. If any damage has occurred, contact the factory immediately.

Refer to Figure 2-1 for component location during installation and configuration.

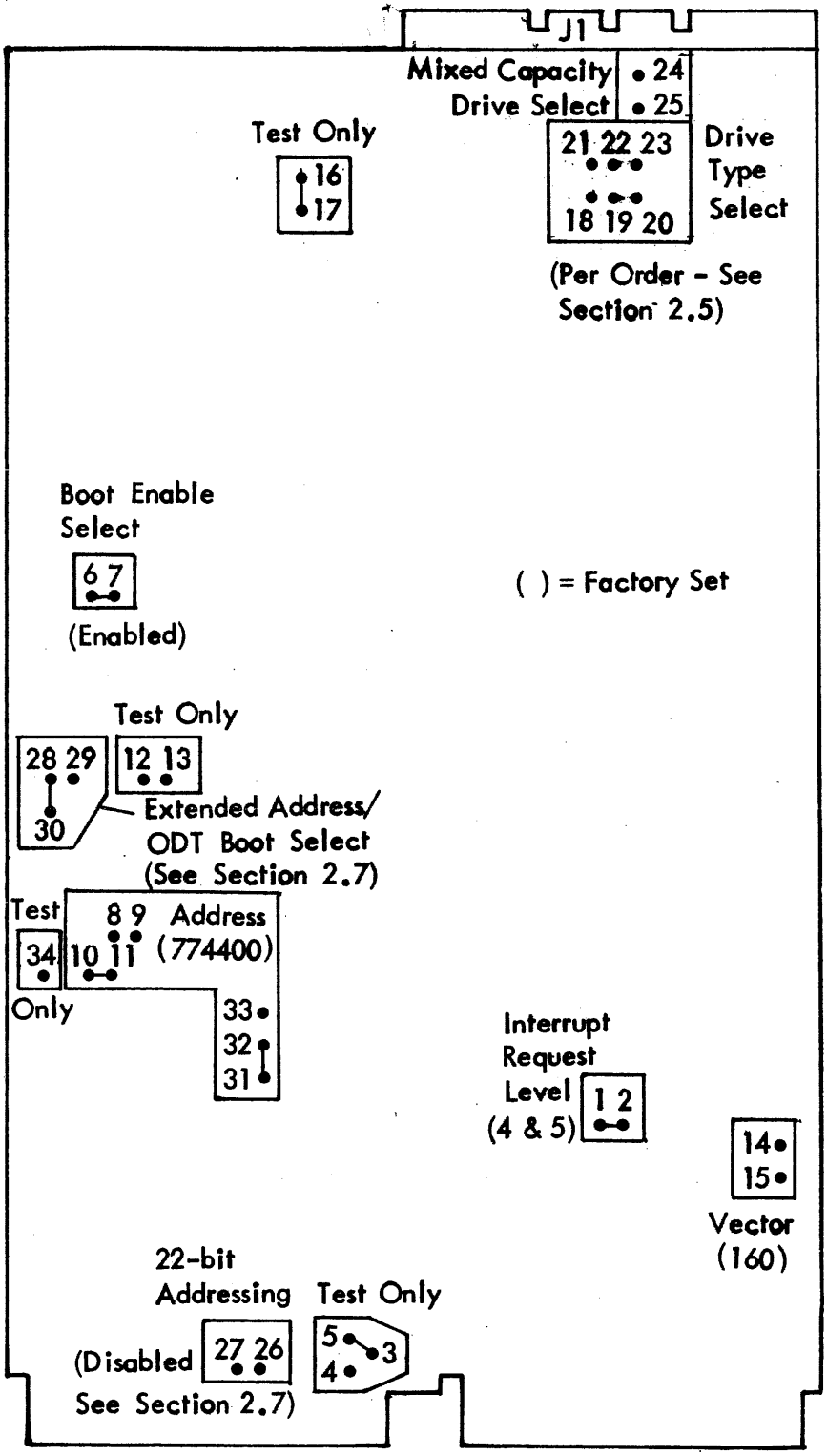


FIGURE 2-1: SDC-RLV12 FACTORY-SET JUMPERS

2.2 DEVICE ADDRESS SELECTION

Software control of the SDC-RLV12 is via five device registers with the following factory configured addresses:

CSR	Control Status Register	774400
BAR	Bus Address Register	774402
DAR	Drive Address Register	774404
MPR	Multipurpose Register	774406
BAE	Bus Address Extension Register	774410

The first four registers are used for 16- or 18-bit addressing. The bus address extension register (BAE) is included for upper address bit selection for 22-bit addressing. Three additional device registers are assigned by DEC at 774412, 774414, and 774416. These registers are unused by DEC; however, the SDC-RLV12 uses 774414 to store error information from the S1410, and register 774416 to bootstrap from ODT. These functions are explained in more detail in later sections. The ususal device starting address is listed in Table 2-1.

The first register (CSR) is assigned the starting address, and the other registers are assigned the next sequential addresses as shown in Table 2-1.

DEVICE ADDRESS	16-BIT ADDRESSING	18-BIT ADDRESSING	22-BIT ADDRESSING
Starting Address Range	160000-177760	760000-777760	17760000-17777760
Starting Address	174400	774400	17774400
Registers Used	CSR (174400) BAR (174402) DAR (174404) MPR (174406)	CSR (774400) BAR (774402) DAR (774404) MPR (774406)	CSR (17774400) BAR (17774402) DAR (17774404) MPR (17774406) BAE (17774410)

TABLE 2-1: ADDRESS SELECTION

The SDC-RLV12 controller is shipped configured with DEC standard operating parameters as defined in Table 2-2.

PARAMETER	SELECTION
Control Address	774400
Vector Address	160
Interrupt Vector	4 and 5
Firmware Boot	Enabled
22-bit Addressing	Disabled

TABLE 2-2: FACTORY SET PARAMETERS

Most options are etched to the most often used operations. Etches must be cut before alternate jumpers are installed. Several of the options are selectable by using AMP 530153-2 pin jumpers or, alternately, No. 30 wire wrap. Refer to Figure 2-1 for jumper locations.

NOTE

Certain jumpers are dedicated for factory test only. They must not be altered.

2.3 DEVICE AND VECTOR ADDRESS SELECTION

The controller is shipped with DEC standard device and vector addresses preset to 774400 and 160, respectively. Any change in these addresses requires a change in system software.

The alternate device and vector addresses are selectable at 776400 and 150, respectively. These alternate addresses are typically used for systems with more than two drives where two controllers are required. To configure the second controller for address/vector assignments, cut the etch between W10 and W11; then jumper W8-W9 and W14-W15 as shown in Table 2-3.

OPTION	JUMPERS		
	W10-11	W8-9	W14-15
Standard Device (774400)	IN	OUT	OUT
Standard Vector (160)	IN	OUT	OUT
Alternate Device (776400)	OUT	IN	IN
Alternate Vector (150)	OUT	IN	IN

TABLE 2-3: DEVICE/VECTOR ADDRESS JUMPERS

2.4 INTERRUPT REQUEST LEVEL

The SDC-RLV12 interrupts are priority level 4 or 5 as shown in Table 2-4. Refer to Figure 2-1 for component locations.

W1-W2	INTERRUPT REQUEST LEVEL
OUT	4
IN	4 AND 5

TABLE 2-4: INTERRUPT REQUEST LEVEL SELECTION

2.5 DRIVE CONFIGURATION

Refer to PROM configuration Table 2-5 to determine how to program the configuration PROM for specific drive manufacturer types. The letters in the CONFIGURATION LABEL (right column in Table 2-5) defines the configuration. For example, a PROM labelled

D F A B

implies that the configuration PROM contents are:

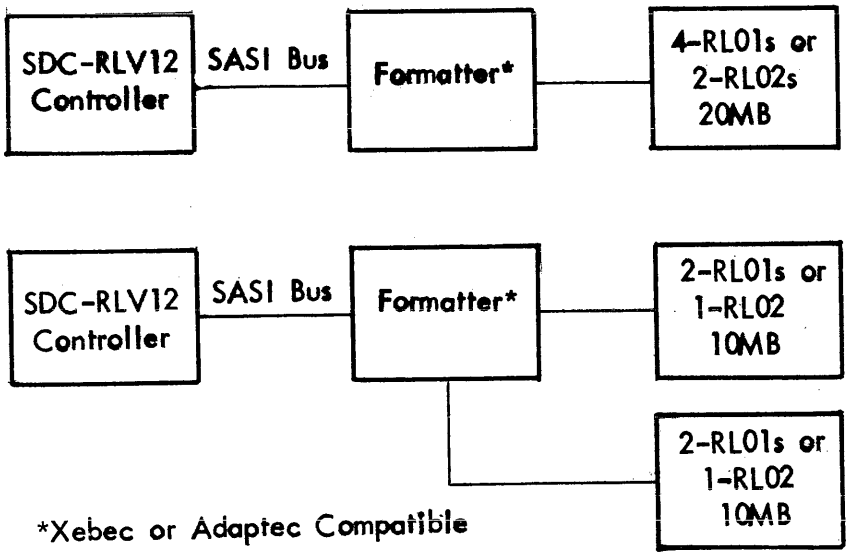
00 50 08 00 84 00 00 84 (1ST 8 BYTES)
90 A0 08 00 84 00 00 84 (2ND 8 BYTES)
C1 41 02 00 84 00 00 84 (3RD 8 BYTES)
80 A0 04 00 84 00 00 84 (4TH 8 BYTES).

The SDC-RLV12 supports 5MB RL01 or 10MB RL02 configured drive types with 40MBs or four logical units maximum capacity. For example, a 5 1/4" winchester drive, depending on capacity, can be configured as one or more RL01s or RL02s. When Iomega an ALPHA-10.5 drive is used, it should be configured as an RL02 disk drive. Drive configuration is determined by W24-W25 jumper; when removed, two like-capacity drives can be used and, when installed, two mixed capacity drives can be used. In the latter case, the drive type (RL01 or RL02) may be different. Example configurations are shown in Figure 2-2.

MANUFACTURER	MODEL	NUMBER OF CYLINDERS	HEADS	DRIVE CAPACITY	START REDUCED WRITE CURRENT CYLINDERS	START WRITE PRECOMP	LOGICAL UNITS	EMULATION	CONFIGURATION PROM CONTENTS	CONFIGURATION LABEL
RODIME	R201	320	2	5.25MB	132(84)	0 (0)	1	RL01	C1, 41, 02, 00, 84, 00, 00, 84	A
RODIME	R202	320	4	10MB	132(84)	0 (0)	2	RL01	80, A0, 04, 00, 84, 00, 00, 84	B
RODIME	R203	320	2	15.7MB	132(84)	0 (0)	3	RL01	40, 68, 06, 00, 84, 00, 00, 84	C
RODIME	R204	320	8	21MG	132(84)	0 (0)	4	RL01	00, 50, 08, 00, 84, 00, 00, 84	D
RODIME	R202	320	4	10.5MB	132(84)	0 (0)	1	RL02	D1, 41, 04, 00, 84, 00, 00, 84	E
RODIME	R204	320	8	21MB	320(84)	0 (0)	2	RL02	90, A0, 08, 00, 84, 00, 00, 84	F
COMPTER MEM	CM5410	256	4	8.38MB	256(100)	256(100)	1	RL01	C1, 00, 04, 01, 00, 01, 00, 84	G
COMPTER MEM	CM5616	146	6	12.5MB	256(100)	256(100)	1	RL02	C1, 00, 06, 01, 00, 01, 00, 84	H
COMPTER MEM	CM5412	306	4	10.0MB	256(100)	256(100)	1	RL02	D1, 32, 04, 01, 00, 01, 00, 84	I
COMPTER MEM	CM5619	306	6	15.0MB	256(100)	256(100)	3	RL01	40, 68, 06, 01, 00, 01, 00, 84	J
ROTATING MEM	RMS513	216	6	10.6MB	128(80)	128(80)	1	RL02	D0, D8, 06, 00, 80, 00, 80, 84	K
ROTATING MEM	RMS512	216	6	10.6MB	128(80)	128(80)	2	RL01	80, 6C 06, 00, 80, 00, 80, 84	L
ROTATING MEM	RMS518	216	8	14.1MB	128(80)	128(80)	3	RL01	40, 50, 08, 00, 80, 00, 80, 84	M
ROTATING MEM	RMS519	306	6	15.04MB	128(80)	128(80)	3	RL01	40, 68, 06, 00, 80, 00, 80, 84	N
TANDON	TM603S	153	6	7.52MB	128(80)	153(99)	1	RL01	C0, 99, 06, 00, 80, 00, 80, 84	O
TANDON	TM602E	230	4	7.53MB	128(80)	128(80)	1	RL01	C0, E6, 04, 00, 80, 00, 80, 84	P
TANDON	TM603E	230	4	7.53MB	128(80)	128(80)	1	RL02	D0, E6, 06 00, 80, 00, 80, 84	Q
SEAGATE	ST506	153	4	5.01MB	128(80)	64(40)	1	RL01	C0, 99, 04, 00, 80, 00, 40, 84	R
(typo)	ST419	306	6	15 MB	128	128	3	RL01	40, 68, 06, 00, 80, 00, 80, 84	N
SEAGATE	ST412	306	4	10.0MB	128(80)	64(40)	1	RL02	D1, 32, 04, 00, 80, 00, 40, 84	S
MINISCRIBE	MSI006	306	2	5MB	153(99)	0	1	RL01	C1, 32, 02, 00, 99, 00, 00, 84	T
MINISCRIBE	MSI012	306	4	10MB	153(99)	0	1	RL02	D1, 32, 04, 00, 99, 00, 00, 84	U
OLIVETTI	HD571/2	180	4	5.8MB	128(80)	64(40)	1	RL01	C0, 84, 04, 00, 80, 00, 40, 84	V
SHUGART	604	160	4	5,242,880	128(80)	128(80)	1	RL01	C0, A0, 04, 00, 80, 00, 80, 84	W
SHUGART	606	160	6	7.8MB	128(80)	128(80)	1	RL01	C0, A0, 06, 00, 80, 00, 80, 84	X
SHUGART	612	306	4	10.0MB	128	128	1	RL02	D1, 32, 04, 00, 80, 00, 80, 84	Y
RMS	512	153	8	10.24MB	48	48	2	RL01	80, 50. 08. 00. 48. 00. 48. 84	Z
RMS	512	153	8	10.24MB	48	48	1	RL02	C0, 99, 08, 00, 48, 00, 48, 84	A1
IDC	9415-5	697	5	36.3MB UNF	0	0	3	RL02	(92, 89, 05, 00, 00, 00, 00, 84	

TABLE 2-5: DRIVE CONFIGURATION PROM CONTENTS

TYPE I - SIMILAR CAPACITY DRIVE (W24-W25 REMOVED)



TYPE II - MIXED CAPACITY DRIVES (W24-W25 INSTALLED)

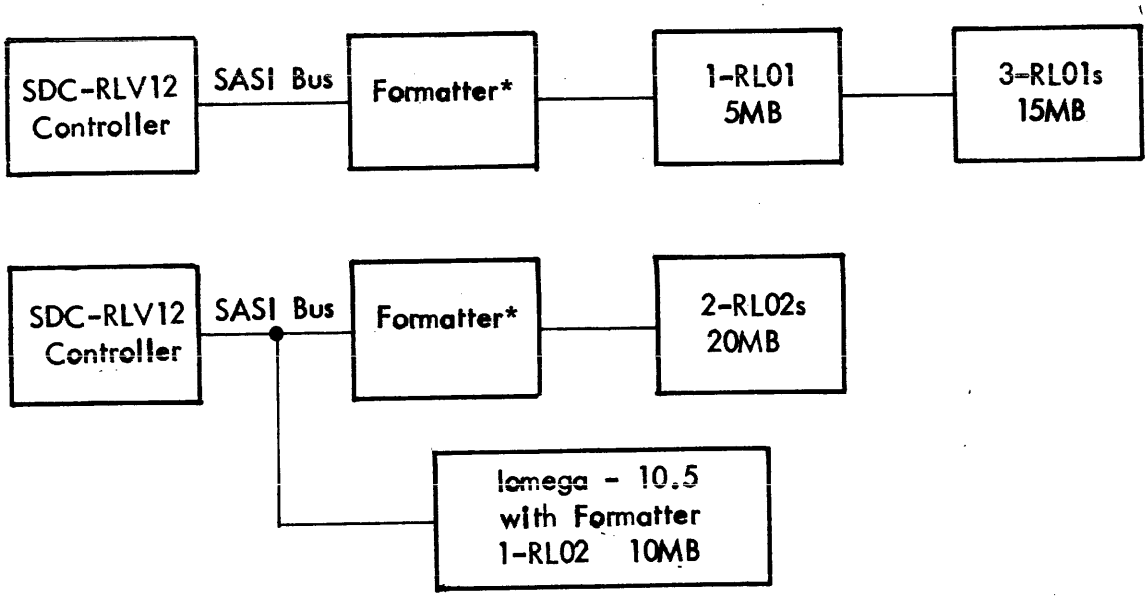


FIGURE 2-2: EXAMPLE DRIVE CONFIGURATIONS

Type I configurations (like-capacity drives with W24-W25 removed) enable selection of up to four different drive/capacity combinations as stored in the configuration PROM U64. Selection is determined by jumpers W18 through W23 as listed in Table 2-6.

JUMPER	CONNECTIONS	BYTE DEFINITION
W18-W19	W21-W22	1st 8 bytes
W18-W19	W22-W23	2nd 8 bytes
W19-W20	W21-W22	3rd 8 bytes
W19-W20	W22-W23	4th 8 bytes

TABLE 2-6: LIKE-CAPACITY DRIVE CONFIGURATIONS JUMPERS

Type II configurations (mixed capacity drives with W24-W25 installed) enables selection of two drive/capacity combinations as stored in the configuration PROM U56. Selection is determined by jumpers W18 through W20 as listed in Table 2-7.

NOTE

For mixed capacity drive configurations, jumpers W21, W22 and W23 must be removed.

JUMPER CONNECTIONS	BYTE DEFINITION
W18-W19	1st 8 bytes and 2nd 8 bytes
W19-W20	3rd 8 bytes and 4th 8 bytes

TABLE 2-7: MIXED CAPACITY DRIVE CONFIGURATION JUMPERS

Each separate drive configuration requires 8 bytes of data stored in PROM in order to specify configuration parameters to the S1410 formatter. The controller reads PROM and uses the 8 bytes of data stored to initialize the S1410 and to load the particular winchester drive configuration paramaters. The byte format of the PROM is shown in Figure 2-3.

XEBEC-COMPATIBLE WORD FORMAT

	BIT NUMBER 7	6	5	4	3	2	1	0
BYTE 0	NLU		0	DT	HI CYLINDER ADDRESS			
BYTE 1	LOW CYLINDER ADDRESS							
BYTE 2	MAXIMUM NUMBER OF HEADS							
BYTE 3	HIGH WRITE CURRENT ADDRESS							
BYTE 4	LOW WRITE CURRENT ADDRESS							
BYTE 5	HIGH PRECOMPENSATION ADDRESS							
BYTE 6	LOW PRECOMPENSATION ADDRESS							
BYTE 7	CONTROL BYTE*							

Where NLU = Number of Logical Units:

Bit 7	Bit 6	LUN
0	0	4
0	1	3
1	0	2
1	1	1

DT = Drive Type:: Bit 4 = 0 = RLO1
1 = RLO2

**See Xebec manual for control byte bit assignments

IOMEGA-COMPATIBLE WORD FORMAT

	BIT NUMBER 7	6	5	4	3	2	1	0
BYTE 0	NLU		1	1	0	0	0	0
BYTES 1-6	MUST BE ZEROS							
BYTE 7	DWELL TIME							

Where NLU = Number of Logical Units as defined above
Bit 4 = Drive Type (must be configured as RLO2 = 1)
Bits 3 through 0 are not used (must be 0s).

*See Iomega Manual for dwell time requirements.

FIGURE 2-3: CONFIGURATION WORD FORMATS

The PROM type is 74S288, a 32 x 8 bipolar PROM. An example for programming the PROM for the RODIME RO204 for (A) 4 RL01s, and (B) 2 RL02s follows:

DRIVE CONFIGURATION PROM EXAMPLES

(A) PROGRAMMING EXAMPLE: RODIME AS 4 RL01s

Byte 0 00 High Cylinder address

The RO204 has 321 cylinders (decimal). Mapping the unit to 4 RL01s results in 321/4 or 80 cylinders/drive. 80 decimal = 50 hex. This is a single byte number; therefore the high byte is 0.

Note that 50 hex cyclinders results in formatted capacity of 80 tracks of 32 sectors/track of 256 bytes/sector and 8 tracks/cylinder. 80 x 32 x 256 x 8 = 5.24288 Mbytes. This is the exact capacity of the DEC RL01.

A and B for 4 logical units = 0
C for RL01 = 0.

Byte 1	50	Low cylinder address in hex
Byte 2	08	Maximum number of heads for RO204
Byte 3	00	Address (high byte) for reduced write current
Byte 4	84	Address (low byte) for reduced write current
Byte 5	00	Write precomp cylinder address (high byte)
Byte 6	00	Write precomp cylinder address (low byte)
Byte 7	04	Control byte, 200us pulse/step option.

(B) PROGRAMMING EXAMPLE: RODIME AS 2 RL02s

Byte 0	90	2 RL02s, high cylinder address = 0
Byte 1	A0	Low cylinder address=321/2=160 decimal=A0 hex
Byte 2	08	Maximum number of heads for RO204
Byte 3	00	Address (high byte) for reduced write current
Byte 4	84	Address (low byte) for reduced write current
Byte 5	00	Write precomp cylinder address (high byte)
Byte 6	00	Write precomp cylinder address (low byte)
Byte 7	04	Control byte, 200us pulse/step option

2.6 MODULE INSTALLATION

The SDC-RLV12 can be installed in any dual LSI-11 bus slot. The priority level is based on the electrical distance from the processor module. With Figure 2-4 as a guide, use the following procedure to install the module. When cabling, ensure that pin 1 (illustrated as o) is in the proper position.

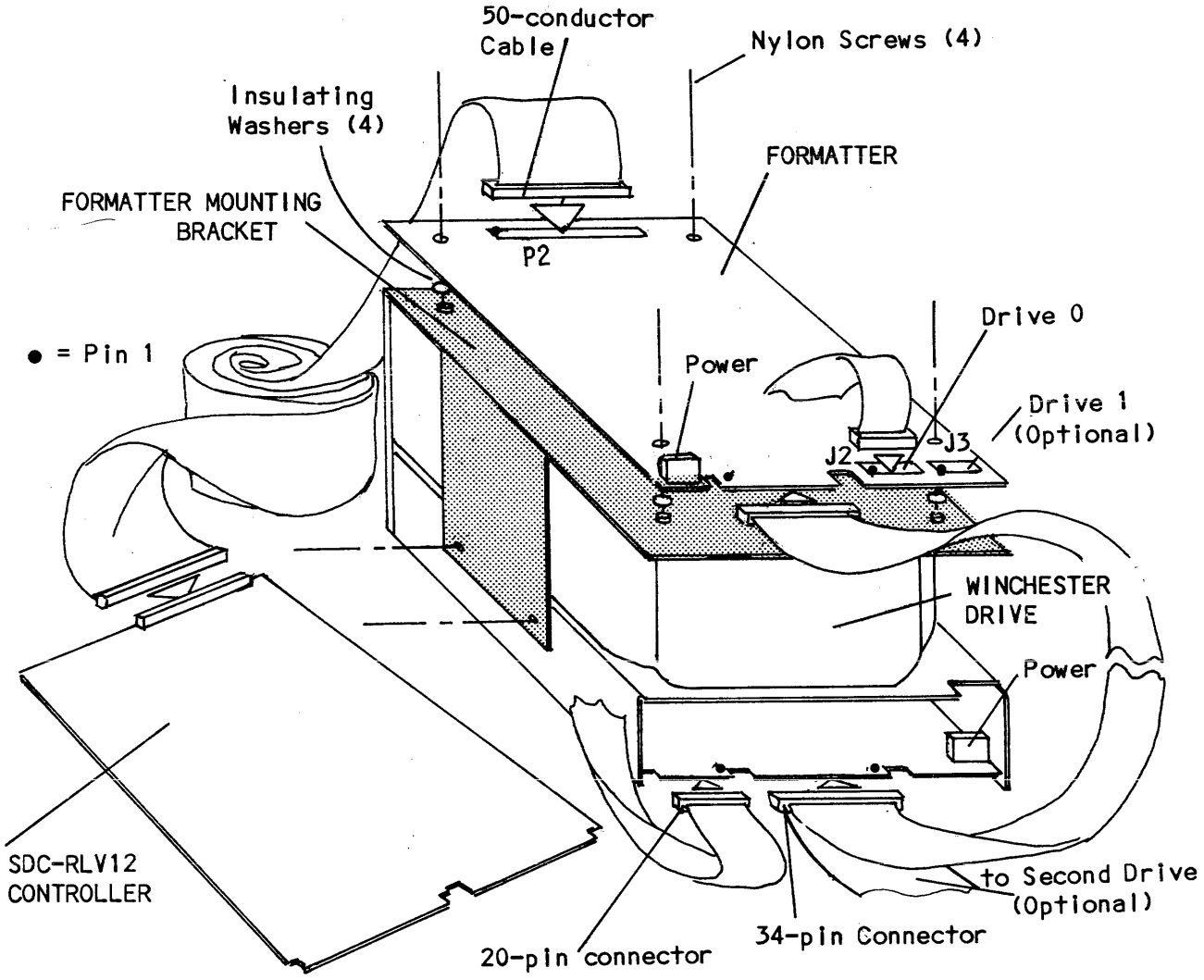


FIGURE 2-4: WINCHESTER CONTROLLER/DRIVE CABLING

WINCHESTER DRIVES WITH SEPARATE FORMATTER

1. Mount Xebec or Adaptec formatter onto drive using Sigma drive mounting kit (PN 500xxx-100) or equivalent. Be sure to isolate formatter from mounting bracket with nylon mounting hardware and mylar insulators.

2. Secure bracket to both sides of winchester drive assembly.

3. Connect data cables from Xebec/Adaptec formatter to drive(s). The 20-pin cable plugs into J2 (J0) of Xebec(Adaptec) formatter for physical drive 1, and J3 (J1) for physical drive 2. Ensure pin 1 cable orientation is maintained.

4. Connect 34-pin cable from formatter edge connector to winchester drive (physical drive 1), and daisy chain to second drive (drive 2). Ensure correct pin 1 connections.

5. Connect power cables from power supply to Xebec or Adaptec formatter and to drive module(s).

4. Connect 50-conductor ribbon cable from SDC-RlV12 to format ter (P2 of Xebec/J4 of Adaptec). Ensure pin 1 connections.

5. Install the SDC-RLV12 module into the LSI-11 backplane.

NOTE

When two physical drives are installed, each drive must be jumpered as unit 0 for physical drive 0 and unit 1 for physical drive 1. Also, only one drive should be terminated. Remove the drive terminator from the drive physically closest to the formatter.

WINCHESTER DRIVES WITH ON-BOARD FORMATTER

If Iomega drives are installed refer to Iomega manual for cable connections and switch settings. Use the following procedure:

1. Connect the 50-conductor ribbon cable from the SDC-RLV12 to the Iomega host interface.

2. Set the Iomega SASI address to respond to address bit 1.

3. Disable SASI bus parity on Iomega formatter module.

2.7 BOOTSTRAPPING AND 22-BIT ADDRESSING

The SDC-RLV12 has an on-board transparent firmware bootstrap which is initiated when program execution starts at location 773000. It reads two sectors of unit 0, starting from cylinder 0. Sectors 0 and 1 are loaded into memory starting at location 0. Program execution is then transferred to location 0. Jumper W6-W7 must be installed to enable on-board boot (factory set) and can be disabled by removing W6-W7 if another device has bootstrap precedence.

If booting the controller from an external bootstrap, or if 773000 is responded by another device in the system, remove W6-W7. The SDC-RLV12 can then be booted via ODT as follows:

1. Set the processor to ODT on power-up.

2. Refer to DEC processor manual and ensure proper jumper configuration on the processor module and SDC-RLV12 module for 18-bit or 22-bit addressing.

CPU MODULE		MODE 1
W5	W6	
IN	OUT	LSI-11/2
OUT	IN	LSI-11/23

SDC-RLV12 MODULE				BOOT	
W26-27	W28-29	W28-30	ADD	ODT	PWR-UP
IN	OUT	IN	22-BIT	YES	YES
OUT	OUT	IN	18-BIT	YES	YES
OUT	IN	OUT	18-BIT	NO	YES

3. While in ODT, enter 774416G.

4. The controller will boot from DL0.

2.8 OFF-LINE CONTROLLER FUNCTION

The SDC-RLV12 microprocessor provides several important off-line functions, which include drive formatting, self-test diagnostics, drive diagnostics, and writing a bad sector file. Table 2-8 shows the command codes assigned for each off-line function.

1.	FORMATTING	264
*2.	XEBEC DIAGNOSTICS	300
*3.	XEBEC RAM DIAGNOSTICS	320
*4.	DRIVE DIAGNOSTICS	340
5.	WRITE BAD SECTOR FILE	360

*Not supported in Iomega or Adaptec microcode.

TABLE 2-8: OFF-LINE COMMAND CODES

2.8.1 Drive Formatting

The SDC-RLV12 provides a firmware routine to format attached drive(s). When executed, the format routine formats to 32 sectors/track, each cylinder as defined by the SDC-RLV12 configuration PROM. To format the drive(s), use the following procedure:
NOTE: (CR) denotes carriage return

1. While in ODT, access the SDC-RLV12 disk address register (DAR) at location 774404 by entering 774404/ at the console. The processor will respond with the contents of 774404, displaying 774404/000000 (not necessarily all zeroes).

2. Enter 264 (CR).

3. Access the SDC-RLV12 control status register (CSR) by entering 774400/. The response will normally be 774400/ 000201.

4. Enter the appropriate LUN (see Table 2-9).

5. The drive will then be accessed and will format completely.

6. If formatting is unsuccessful, be sure to verify that the configuration PROM is correct for the installed drive. See Section 2.5 for PROM configurations.

IOMEGA FORMATTER

CAUTION

REMAKE Z-TRACK may destroy customer data on the cartridge. The user should REMAKE Z-TRACK on all Iomega disk cartridges before using in the subsystem; otherwise performance will be degraded.

For IOMEGA disk drives a firmware routine is provided to perform an IOMEGA command "REMAKE Z-TRACK" to allow the user to change disk cartridge characteristics. The procedure for "REMAKE Z-TRACK" is the same as the formatting pack procedure with the exception of step 2. Enter the appropriate "REMAKE Z-TRACK" code (octal) as follows:

220 - ECC Mode
224 - CRC Mode with Post CRC Check
234 - CRC Mode with No Post CRC Check

The sector interleave factor is set to 4 for the above codes.

2.8.2 Writing Bad Sector File

The SDC-RLV12 includes a firmware program designed to write a bad sector file at the end of each logical drive. The format of the bad sector file is per DEC STD-144, and is compatible with the bad sector file found on the DEC RL01/RL02 disk cartridge.

DEC diagnostic CZRLM can also be used to generate or check the bad sector file information. To write a bad sector file on each logical unit, while in ODT, deposit 360 into the DAR(774404) and then deposit the appropriate logical unit number (see Table 2-3 in Section 2.8.3) into the CSR (774400). The controller will access the drive and perform the function.

2.8.3 Self-Test

The SDC-RLV12 has an extensive set of diagnostic software built into the controller. Each time a power-up or BINIT routine is completed, the SDC-RLV12 executes a complete set of self-test diagnostics that test the SDC-RLV12.

Upon successful completion of the self-test diagnostics, LED CR2 is latched in the ON state. If the LED remains OFF after a power-up cycle, part of the subsystem is not functioning properly and the fault should be remedied before trying to use the disk.

The diagnostics executed on power-up are:

- SDC-RLV12 DIAGNOSTICS. These tests check the SDC-RLV12 microprocessor and buffer memory and all related data paths.

If using a new drive, the disk drive must be formatted before any drive tests are attempted. Be sure the controller configuration PROM is correct and configured properly before attempting any drive operations. See Section 2.5 for PROM configurations.

In order to execute a function from ODT, open the drive address register (DAR at 774404) and deposit the appropriate command. Then open the control/status register (CSR at 774400) and deposit 4(CR).

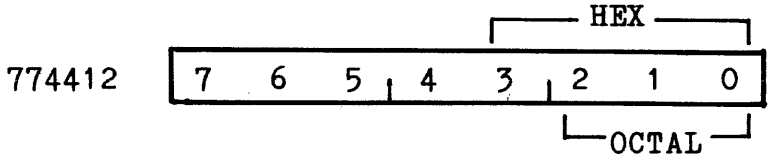
If the operation is to be performed on a drive whose logical unit number (LUN) is other than 0, the drive number must be specified as shown in Table 2-9.

LUN	CSR COMMAND CODE
0	4
1	404
2	1004
3	1404

TABLE 2-9: LOGICAL DRIVE NUMBER (LUN)

ERRORS

After an error occurs, the SDC-RLV12 stores the error code in 774414. The error information is an hexadecimal number, whereas the ODT read of the register is octal. Therefore, an octal-to-hexadecimal conversion must be made to obtain the correct error code. The error bit assignments are as follows:



Where,
Bits 0-3 Hexadecimal Error Code
Bits 4,5 Error Class (0-4)
Bits 6,7 Ignore

ERROR CODES

If an error occurs during these tests, the SDC-RLV12 will store the reported error information in location 774414. Errors are of four classes and are defined in Table 2-10.

TYPE 0 DISK DRIVE ERRORS
TYPE 1 S1410 FORMATTER ERRORS
TYPE 2 COMMAND ERRORS
TYPE 3 MISCELLANEOUS

TABLE 2-10: ERROR CODE DEFINITIONS

HEX	DEFINITION
	TYPE 0 ERROR CODES - DISK DRIVE
0	Controller detected no error during execution of previous operation.
1	Controller did not detect an index signal from the drive.
2	Controller did not get a Seek Complete signal from the drive after a seek operation.
3	Controller detected a Write Fault from drive during last operation.
4	After controller selected drive, the drive did not respond with Ready signal.
5	Not used.
6	After stepping maximum number of cylinders, controller did not receive Track 00 signal from the drive.
9	Media not loaded.
A	Insufficient Capacity
	TYPE 1 ERROR CODES - CONTROLLER
0	ID Read Error: Controller detected an ECC error in the target ID field on the disk.
1	Data Error: Controller detected an uncorrectable ECC error in the target sector during a Read operation.
2	Address Mark: Controller did not detect the target address mark (AM) on the disk.
3	Not used.
4	Sector Not Found: Controller found the correct cylinder and track, but not the target sector.
5	Seek Error: Controller detected an incorrect cylinder or track, or both.
6	Not used.
7	Not used.
8	Correctable Data Error: Controller detected a correctable ECC error in the target data field.
9	Bad Track: Controller detected the bad track flag during the last operation.
A	Interleave Error
B	Data Transfer not complete.

TYPE 2 AND 3 ERROR - COMMAND AND MISCELLANEOUS		
HEX	TYPE	DEFINITION
0	2	Invalid Command: Controller has received an invalid command from the host.
1	2	Illegal Disk Address: Controller detected an address that is beyond the maximum range.
0	3	RAM Error: Controller detected a data error during the RAM sector buffer diagnostic.
1	3	Program Memory Checksum Error: During its internal diagnostic, the controller detected a program-memory checksum error.
2	3	ECC Polynominal Error: During the controller internal diagnostic the hardware ECC generator failed its test. For the Iomega formatter, this error code indicates parity error on the SASI bus.

Table 2-11 is a summary of the error codes returned as the result of Request Sense Status command. NOTE: Address valid bit (bit 7) may or may not be set and is not included here for clarity.

TABLE 2-11: ERROR CODE SUMMARY

HEX	DEFINITION
00	No error detected (command completed OK).
01	No index detected from disk drive.
02	No seek complete from disk drive.
03	Write fault from disk drive.
04	Drive not ready after it was selected.
05	Not used.
06	Track 00 not found.
07-0F	Not used.
10	ID field read error.
11	Uncorrectable data error.
12	Address mark not found.
13	Not used.
14	Target sector not found
15	Seek error
16-17	Not used.
18	Correctable data error.
19	Bad track flag detected
1A	Format error
1B-1F	Not used.
20	Invalid command
21	Illegal disk address
22-2F	Not used
30	RAM diagnostic failure
31	Program memory checksum error.
32	ECC diagnostic failure
33-3F	Not used.

2.9 DIAGNOSTIC COMPATIBILITY

The SDC-RLV12 is compatible with the following DEC diagnostic programs:

CZRLG	Controller Test Part 1
CZRLH	Controller Test Part 2
CZRLK	Performance Exercizer
DZRLM	Bad Sector File Utility

Sigma recommends that the SDC-RLV12 subsystem be excersized using the Performance Exerciser diagnostic as a means of verifying system integrity. If problems with the controller or subsystem are suspected, running DZRLG and CZRLH will serve as valuable aids.

These diagnostic program are available and may be purhcased from Digitial Equipment Corporation.

Section 3 - Programming Considerations

3.1 INTRODUCTION

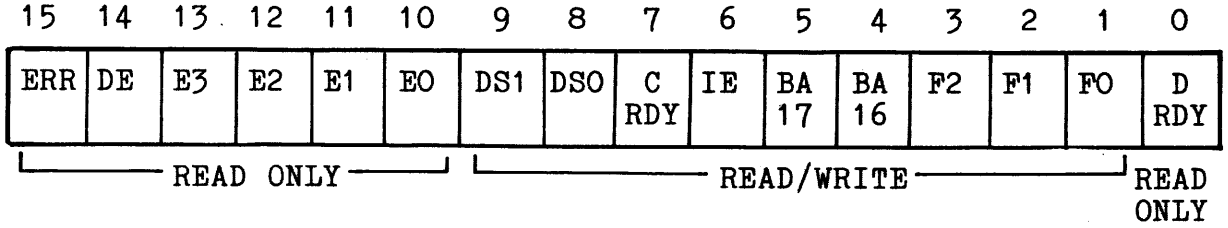
This section describes the function of the bits in each of the five programmable registers, and the commands sent to the CSR for specific disk functions.

NOTE

To prevent accidental writing on a disk, the SDC-RLV12 synchronizes on controller ready (CRDY). If the CRDY bit in the CSR changes from clear to set while the processor is in ODT mode, the next read access of any SDC-RLV12 register produces all 0s.

3.2 CONTROL/STATUS REGISTER (CSR)

The control/status register is a 16-bit word-addressable register with standard address of 774400 for 18-bit addressing, an 17774400 for 22-bit addressing. Bits 1 through 9 can be read or written; the other bits can only be read. The it functions are described below.



where,

DRDY DRIVE READY. When set, this bit indicates that the selected drive is ready to receive a command or supply valid read data. Cleared when a Seek or head select operation is started; set when the Seek operation is completed.

F2-FO FUNCTION CODE. These bits are the function code set by software to indicate the command to be executed.

FUNCTION F2	F1	FO	COMMAND	OCTAL CODE
0	0	0	Maintenance mode (NOP)	0
0	0	1	Write Check	1
0	1	0	Get Status	2
0	1	1	Seek	3
1	0	0	Read Header	4
1	0	1	Write Data	5
1	1	0	Read Data	6
1	1	1	Read Data without Header Check	7

Command execution starts when CRDY (bit 7) is cleared by software. The commands are described in detail in Section 3-7. The function code is cleared by initializing the bus (BINIT L).

BA17, BA16 EXTENDED ADDRESS BITS. These two bits are the upper-order bus address bits for 18-bit buses. They are read and written as bits 4 and 5 of the CSR and function as address bits 16 and 17 of the BAR. Writing bits 4 and 5 of the CSR also writes bits 0 and 1 of the BAE.

IE INTERRUPT ENABLE. When CRDY is asserted, bit 6 allows the controller to interrupt the processor. This interrupt occurs at the termination of a command. Once an interrupt request is placed on the LSI-11 bus, it is not removed until acknowledged by the LSI-11 processor even if IE (bit 6) is cleared. Cleared by initializing the bus.

CRDY CONTROLLER READY. When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. Set by the controller at completion of a command, at detection of an error, or by initializing the bus. Software cannot set this bit because no registers are accessible while CRDY is 0.

DS0, DS1 DRIVE SELECT. These bits determine which drive will communication with the controller via the drive bus. Cleared by initializing the bus.

E3-E0 CONTROLLER STATUS ERRORS. These bits are the error code set by the controller to indicate on of the following errors:

ERROR CODE				ERROR	OCTAL
E3	E2	E1	E0		CODE*
0	0	0	1	Operation incomplete (OPI)	1
0	0	1	0	Data CRC (DCRC)	2
0	0	1	1	Header CRC (HCRC)	3
0	1	0	0	Data late (DLT)	4
0	1	0	1	Header not found (HNF)	5
1	0	0	0	Nonexistent memory (NXM)	10
1	0	0	1	Parity error abort (PAR ERR)	11

*See Section 3-7.

Operation incomplete indicates that the current command was not completed within the OPI timeout period of 550ms.

A data CRC error indicates that, while ready the data field from the disk, an error was found.

A header CRC error indicates that, while reading the header from the disk, an error was found. The CRC check is performed on the first and second header words, although the second header word is always 0.

Data late indicates that the FIFO RAM was more than half full and the controller was not able to read the next sequential sector. This error may occur during a Read without Header Check command.

Header not found indicates that OPI timeout occurred while the controller was searching for the correct sector to read or write. A header compare did not occur.

A nonexistent memory error indicates that, during a DMA transfer, the memory location addressed did not respond with RPLY within 10us.

A memory parity error abort indicates that a parity error was detected while reading the system optional memory that has parity error checking. If an error was detected, the current command to the SDC-RLV12 is aborted.

DE DRIVE ERROR. This bit is buffered from the drive error interface line. When set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a Get Status command. DE will not set ERR or CRDY until the usual occurrence of CRDY.

ERR COMPOSITE ERROR. When set, this bit indicates that one or more of the error bits (bits 10-14) are set. When an error occurs, the current operation terminates and an interrupt routine is started if the interrupt enable bit (bit 6 of the CSR) is set.

All error bits are cleared by initializing the bus by starting a new command, with the exception of DE an ERR if they were caused by a drive error.

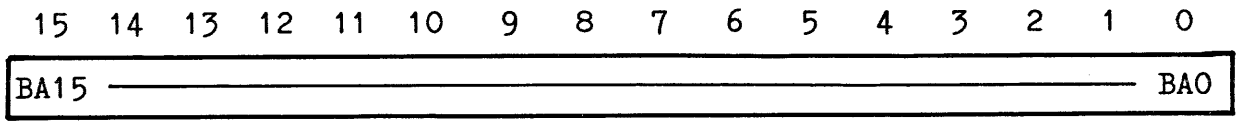
When the LSI-11 bus is initialized with BINIT L, bits 1-6 and 8-13 are cleared, and bit 7 (CRDY) is set. Bit 0 (DRDY) is set when the selected drive is ready to accept a command; otherwise, this bit is cleared. Bit 14(DE) is clear as long as there is no drive error. Otherwise, this bit is set and stays set until the drive error is corrected; or if bit 3 (drive reset) is set in the DAR and the controller is sent a Get Status command, the DE bit is cleared.

Bit 15 (ERR) is set when there is a drive or controller error in bits 10-14.

At the beginning of each controller command, error bits 10-13 are automatically cleared. At the completion of each controller command, it 7 is automatically set. Bit 7 is also set if an error is detected during command execution.

3.3 BUS ADDRESS REGISTER (BAR)

The bus address register is a 16-bit, word addressable register with a standard address of 774402 for 18-bit addressing, an 17774400 for 22-bit addressing. Bits 9 through 15 can be read or written; bit 0 is usually written as 0. The bus address register indicates the memory location for the DMA data transfer during a read or write operation. The register contents are automatically incremented by 2 as each word is transferred between system memory and controller. BAR is cleared by initializing the bus (BINIT L).



The bus address can be expanded for an 18-bit LSI-11 bus by using bits 4 and 5 (BA16 and BA17) of the CSR, or by using bits 0 and 1 of the BAE register. The bus address can be expanded for a 22-bit LSI-11 bus by using the BAE register (BAE16-BAE21).

NOTE

When using 22-bit mode, writing CSR bits 4 and 5 modifies BAE bits 0 and 1-and vice versa.

3.4 DISK ADDRESS REGISTER (DAR)

The disk address register is a 16-bit, read/write, word addressable register with a standard address of 774404 for 18-bit addressing, and 17774404 for 22-bit addressing. Its contents has one of three meanings, depending on the command being performed. DAR is cleared by initializing the bus (BINIT L).

COMMAND	DAR FUNCTION
Seek	Head selected, number of cylinder to move, direction
Read Data or Write Data	Head selected, cylinder address, sector address
Get Status	Send drive status to MPR; reset error registers

DAR DURING A SEEK COMMAND

To perform a Seek command, the program must provide the head selected (HS), direction to move (DIR), and the cylinder address difference (DF).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0	0	0	HS	0	DIR	0	MRKR

Where,

MRKR MARKER. Must be 1.

BIT 1 Must be 1, indicating to the drive that a Seek command is being issued and that the other bits in the register hold the Seek specifications.

DIR DIRECTION. This bit indicates the direction in which the Seek is to take place. When set, the heads move toward the spindle (to a higher cylinder address). When cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-15).

BIT 3 Must be 0.

HS HEAD SELECT. Indicates which head (disk surface) is to be selected: 1 = lower, 0 = upper.

BITS 5,6 Reserved

DF CYLINDER ADDRESS DIFFERENCE. Indicates the number of cylinders the heads are to move on a Seek.

DAR DURING A READ, WRITE, OR WRITE CHECK COMMAND

For a Read, Write, or Write Check command, the DAR provides the head selected (HS) and the address of the first sector to be transferred (SA). As each sector is transferred, the DAR sector address increments by 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

Where,

SA SECTOR ADDRESS. Address of one of the 40 sectors on a track (Octal range is 0 to 47.

HS HEAD SELECT. Indicates which head (disk surface) is to be selected: 1 = lower, 0 = upper.

CA CYLINDER ADDRESS. Address of one of the 256 cylinders for RL01 or 512 cylinders for RL02. Octal range is 0 to 777.

DAR DURING A GET STATUS COMMAND

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	RST	0	GS	MRKR

Where,

MRKR MARKER. Must be 1.

GS GET STATUS. Must be 1, indicating to the drive to send its status word. At the completion of the Get Status command, the drive status word is read into the controller multipurpose register (MPR). With this bit set, bits 8-15 are ignored by the drive.

BIT 2 Must be 0.

RST RESET. When set, the disk drive clears its error register of soft errors before sending a status word to the controller.

BITS 4-7 Must be 0s.

BITS 8-15 Not used.

3.5 MULTIPURPOSE REGISTER (MPR)

The multipurpose register is a 16-bit, read/write, word-addressable register. It is accessed using the standard address of 774406 for 18-bit addressing, and 17774404 for 22-bit addressing. Following a Read Header command or a Get Status command, reading the MPR obtains sector header or drive status information.

Writing to the MPR is used to set the word count. The word count is cleared by initializing the bus (BINIT L).

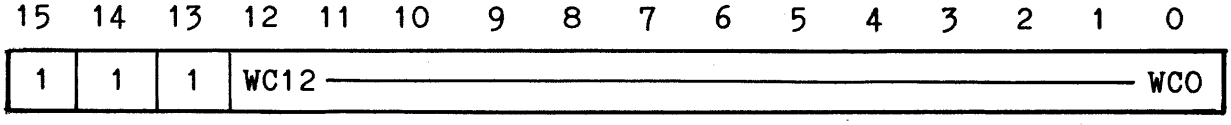
WRITING THE MPR TO SET THE WORD COUNT

Before starting a DMA transfer, the MPR is loaded with the word count. The program must load the MPR with the 2's complement of the number of words to be transferred. The MPR is written in the format shown and described below. As each word is transferred, the MPR is automatically incremented by 1. The reading or writing operation continues until a word count overflow occurs, indicating that all words have been transferred.

The word count can range from 1 to 2120 data words. The maximum word count is limited by the maximum number of sectors available (40) and the maximum words per sector (128).

NOTE

Once written, the word count cannot be read back. Reading the MPR does not change the word count.

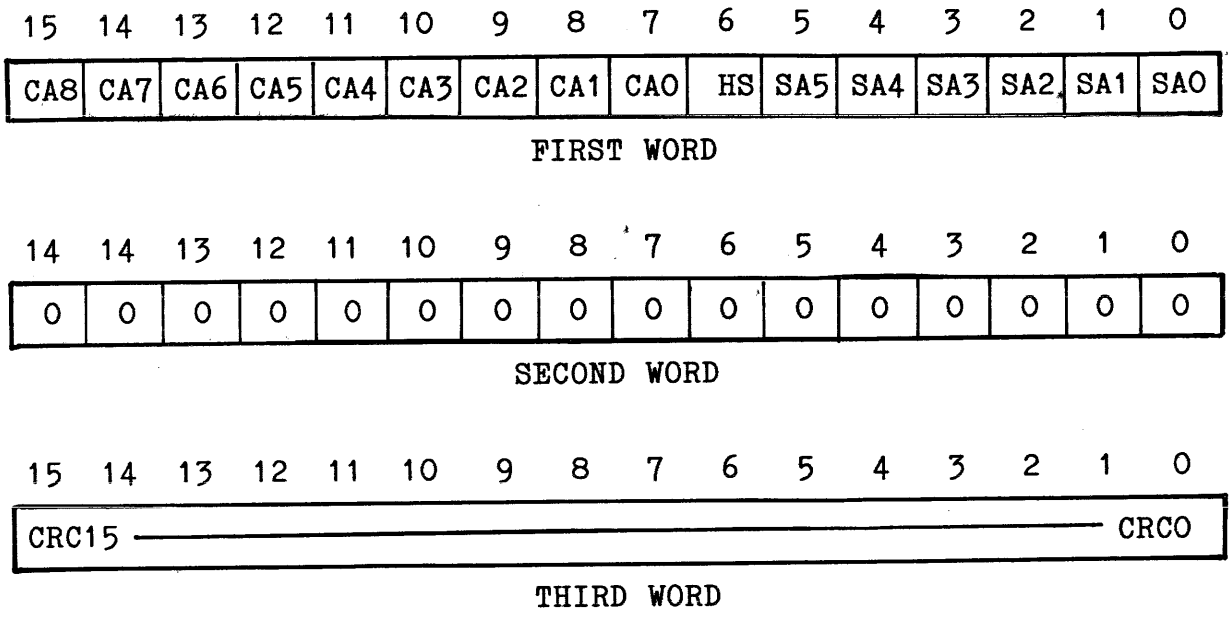


Where,

WC WORD COUNT. This is the 2's complement of the total number of words to be transferred.

BITS 13-15 Must be all 1s for word count to be in correct range.

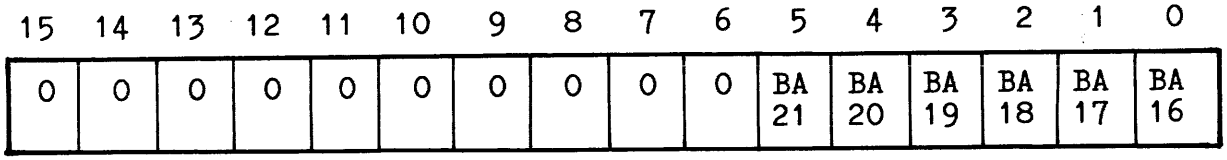
READING THE MPR AFTER A READ HEADER COMMAND



3.6 BUS ADDRESS EXTENSION REGISTER (BAE)

The bus address extension register is a 6-bit read/write register used to drive address bits 16-21 for a 22-bit LSI-11 bus. The BAE has a standard address of 17774410 for 22-bit addresssing. A write to the BAE loads TS DAL 0-5 into BAE 0-5, shown below. Reading the BAE enables bank select 7 (BBS7 L) to the LSI-11 bus. When address bits 13-21 are all 1s, the SDC-RLV12 drives BBS7 L to direct data to the I/O page.

The two least significant bits of the BAE (bus address lines 16 and 17) are mirrowed in bits 4 and 5 of the CSR. The same bits can be read or written as CSR bits 4 and 5, or BAE bits 0 and 1.



3.7 CSR COMMANDS

This section describes the commands sent to the control/status register (CSR), bit F0, F1, and F2, to perform a specific disk function. A prerequisite to issuing any command is that CRDY (controller ready) is set in the CSR. Software cannot set this bit and cannot access any register if bit 7 = 0.

At the start of each new command, the error bits in the CSR (bits 10-13) are automatically cleared. At the completion of each command, the CRDY bit is automatically set. CRDY is also set if an error is detected during command execution. The commands are define in detail below where the number in parentheses after each command is the octal code for the command.

WRITE CHECK (1)

PREREQUISITE: The disk heads must be placed at the correct track by issuing a Seek command if necessary. BAR must be loaded with the address of the first location of the data block in system memory. The word count of the data block length must be loaded in the MPR and the DAR must be loaded with the starting disk address location.

The Write Check command is used to verify that data was written on the disk correctly. It is used after writing a block of data on the disk by the Write Data command.

The Write Check command reads this same block of data and compares it with the data in the computer's system memory. This comparison is performed in the controller, thus the source data must be transferred out of memory into the controller FIFO buffer. A bit-by-bit comparison of the header on the disk and the contents of the disk address register checks for a header match.

Once a header match is found and the header CRC validates the match, the 128 words of data are read from the disk. This data is then compared with the serial data coming out of the FIFO serializer (SER DATA OUT). A compare error or a data CRC error sets bit 11 in the CSR.

NOTE

When writing only a partial sector (less than 128 words), words with all 0s are used to fill the remaining portion of the sector.

GET STATUS (2)

PREREQUISITE: The software must first verify that the controller ready bit is set. (The drive does not have to be ready.) Then a status request word must be loaded into the DAR where bits 0 and 1 must be set; bit 3 (reset) can be either 0 or 1, and all other bits must be 0s. (See Paragraph 3.4.)

A Get Status command in the CSR asks the selected disk drive to return information about its current operation and error status. If DAR reset bit (bit 3) is set, the disk drive first clears its error register of all soft errors before sending back the drive status. When the drive sends back its status word, it is stored in the FIFO buffer and can be accessed by reading the MPR.

DRDY (drive ready) does not have to be set to issue a Get Status command. For example, a Get Status command can be issued during a seek operation or when the drive is in its load state.

SEEK (3)

PREREQUISITE: The present location of the disk head must be known. This can be determined with a Read Header command. Then the software must compute the cylinder address difference (DF) needed by the drive to move the heads to the new location. Then the DAR must be loaded with the head positioning information. The DAR must include the number of cylinders to move (bits 7-15), the head select bit (bit 4), and the direction to move (bit 2). Bits 6, 5, and 1 must be set to 0; bit 0 must be set to 1.

The Seek command shifts the contents of the DAR to the disk drive. The DAR contains the head selected for the next data transaction, the cylinder difference address, and the direction of movem,ent. Once the drive receives this head positioning information, it moves the head to the new track location.

READ HEADER (4)

PREREQUISITE: A Get Status command must be issued and DRDY must be set in the CSR.

The Read Header command reads the first header found on the selected drive and stores the three header words in the FIFO RAM. The first word, WD1, includes the cylinder address, the head selected, and the sector address. The second word, WD2, is all zeros. The third word, WD3, has the header CRC information. These words can be read from the FIFO RAM buffer by consecutive read MPR instructions. Three read MPR instructions are needed to read three FIFO words. Reading the first header word provides enough head positioning information to permit softweare computation of the cylinder difference for another Seek command to a new track address.

WRITE DATA (5)

PREREQUISITE: The head must be loaded at the correct track by issuing a Seek command if necessary. The 2's complement of the words to be written (word count) must be loaded into the MPR.

The Write Data command enables the controller DMA circuitry. The SDC-RLV12 becomes LSI-11 bus master, and data words are loaded into the FIFO buffer. When the drive is ready, header information is read from the disk and compared with the first sector address stored in the DAR. Once a header match is found, the FIFO data is written on the disk in sequential sectors until the word count is complete. The BAR and word count are incremented for each word transferred. If only part of a sector is filled by the new data, the rest of the sector area is filled with Os. At the end of the sector, the sector part of the DAR is incremented. At the end of a transfer, CRDY is set and an interrupt is made if IE is set.

READ DATA (6)

PREREQUISITE: The head must be loaded at the correct track by issuing a Seek command if necessary. The 2's complement of the words to be read (word count) must be loaded into the MPR.

The Read Data command causes headers to be read from the disk and compared to the sector address stored in the DAR. When a header match is found, disk data words are transferred into the FIFO memory. Both the BAR and word count are incremented for each word transferred. After four words are read from the disk, the microsequencer starts a DMA transfer on the LSI-11 bus. The data transfer ends when the word counter overflows. If the word count is not complete, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

READ WITHOUT HEADER CHECK (7)

PREREQUISITE: The location of the sector with the bad header must be known. The BAR must be loaded with the starting memory location to place the words to be read. The MPR must be loaded with the word count in 2's complement form.

The Read without Header Check allows the recovery of data if the headers cannot be read. If header not found (HNF) or header CRC (HCRC) errors are found on a sector, then data cannot be recovered by the usual Read Data command.

A Seek command must be issued to position the head on the sector with the bad header. Then the sector preceding the bad sector must be found by performing consecutive Read Header commands. Finally, a Read without Header Check command must be issued within 300us to recover the data in the bad sector. The BAR and word count are incremented for each word transferred. Data CRC is checked at the end of a sector. If the word count is not complete, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

NOTE

The DAR is automatically incremented after each sector is transferred.

3.8 PROGRAMMING EXAMPLES

The following example show the use of SDC-RLV12 commands in software programs.

SEEK OPERATION

1. Issue a Read Header command to the desired disk drive and wait for an interrupt request or wait for CRDY.
2. Check error flag in CSR.
3. Read the header word from MPR.
4. Computer the difference address and the direction for the seek.
5. Write the difference word into DAR.
6. Issue the Seek command to the drive and wait for seek to be completed as indicated by DRDY.
7. Check error flag in CSR.

Steps 1, 2 and 3 above are not needed for the next Seek commands if the software program keeps the current cylinder address and head selected in memory.

Reading sequential headers gives head position and present direction so the program can optimize the shortest distance to the new location.

DATA TRANSFER OPERATION

1. Perform the steps of the seek operation described above.

2. Write the extended bus address in BAE if using 22-bit addressing.

4. Write DAR with the cylinder address, head selection, and sector address of the first disk location to be transferred.

5. Load MPR with the word count (2's complement of words to be transferred).

6. Issue a Read Data, Write Data, or Write Check command in CSR.

7. Wait for interrupt or test for CRDY.

8. Check CSR for error flag.

Seek commands or data transfer commands may be given to other drives between issuing a Seek to the first drive and issuing a data transfer command.

As soon as a Seek command is issued to the first drive, it returns an interrupt and sets CRDY. A Seek command may be given to another drive while the first drive is seeking. No interrupts occur when all the seeks are complete, so as soon as all Seek commands are issued, data transfer commands may be issued. Starting with the drive that was given the shortest seek distance makes it possible for the drive that completes its seek first to immediately perform its data transfer and interrupts when done.