SBC-100S Slave Processor

Technical Description Manual

Version 1.0

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I. Description

The Sierra Data Sciences SBC-100S is the first "true" single board slave computer designed to operate as a peripheral to the IEEE 696 S-100 Buss. It does not, however, require a buss structure to operate in other environments.

To assist in the implementation of multi-processor implementations, Sierra Data Sciences has designed the SBC-100S Satellite (or "Slave") Processor PC Board. The SBC-100S is a implementation that can operate in tandom with the SBC-100 or other S100 based host processor PCB. Only four I/O mapped ports on the S100 buss are recognized by the SBC-100S processor board, hence, up to sixty-four separately addressed SBC-100S processors can simultaneously be operating on a single motherboard. This design flexibility makes it possible to build multi-processor based systems utilizing other host processors, such as the Alpha Micro, 8086, Z8000, MC68000, etc.

The SBC-100S has an additional buss available for extended processing (The X-Buss). Located at the top of the card, this 39 pin buss provides all the pin-out signals of the Z80 processor chip in addition to a number of selected support signals. The X-Buss provides a natural interface for computer controlled peripheral processors. The major features of the SBC-100S are as follows:

Z80A Processor (4 Mhz)

Zilog Dart (SIO optional) Serial I/O chip. This part provides two (2) RS-232 ports.

Two (2) ZPIO Parallel I/O chips. Four full parallel ports are provided with these chips. Two ports are available through a connector located at the top of the board. The remaining two ports operate on the S100 Buss as a high-speed data channel, and are used for I/O transfer operations during multi-processor communications.

64K Dynamic Random Access Memory. 64K of RAM is provided with the board. The SBC-100S is designed to permit the on-board RAM to execute with no wait states.

Four (4) 2732A EPROMs are supported by the board. The EPROMs provide up to 16K of user PROM space. The PROM address space may be "phantomed" on or off by a simple output command to a special on-board global control port.

EPROM Programmer (Optional). This option allows the user to program his or her own 2732A EPROMs. EPROM

programming software is provided with the purchase of this option.

Software Controlled Reset Inhibit. This feature permits any hardware reset (i.e. front-panel reset key) to be ignored or recognized via a software controlled global control port. This control port may also be programmed to generate an on-board hardware reset.

Intelligent Winchester Interface. (Optional) An interface is available for the Micropolis 122x series intelligent 8" winchester drives. A special interface card is provided to interface these winchester drives to the parallel ports on the SBC-100S. Driver and formatter software is also provided with the purchase of this option.

Adherence to the IEEE-696 proposed standards. The SBC-100 was designed to meet the proposed IEEE-696 standard for the lines that it accesses.

Standalone option. This option allows the SBC-100S to be run without an S-100 buss structure. With this option, the on-board power regulators are replaced with a connector to allow using an external regulated power supply.

MP/M and CP/Net can be configured on the SBC-100 and SBC-100S processors. SDS does not directly support MP/M as we find the TurboDOS operating system far superior. However, the SBC-100S has been used successfully under both MP/M and CP/Net.

In addition, the powerful TurboDOS multi-user operating system can be configured to operate with Sierra Data products either as a single user system or as a full multi-processor system using dedicated satellite processors such as the Sierra Data Sciences SBC-100S Satellite processor in conjunction with a single SBC-100 master processor.

Sierra Data has developed extensive communications software designed to run in the SBC-100S. These packages are sold separately and allow any S100 system to communicate with a variety of large mainframe computers such as an IBM or Univac system. Contact SDS for further information on our communications products.

For those users with special requirements, the SBC-100 and SBC-100S are ideal candidates for the nucleus of a powerful computer system for business, scientific, educational, or any computing requirements.

II. Interfacing - Slave

A. S-100 Buss to SBC-100S Interface

This section describes how the SBC-100S interfaces with the 696 (S-100) Buss. The SBC-100S internal port assignments and description can be found in this section under "B. SBC-100S Internal Port Assignments".

The SBC-100S occupies a total of four I/O mapped ports on the S100 buss. Address bits A7 through A3 are decoded and used to set the board base address. A jumper inserted in shorting block #4 (SB4) represents a binary one setting for that bit, and conversely, a removed jumper represents a binary zero setting for that bit. For example, if the area is configured with address bit jumpers A7 and A6 inserted, then the base address would be C0H and the SBC-100S would occupy ports C0H, C1H, C2H, and C3H. SDS releases most slave boards addressed at 40 hex. The only exceptions are when multiple slaves are ordered with a TurboDOS system, in which case the port addresses are configured for TurboDOS usage during final testing.

The SBC-100S can be used in two modes of operation, both of which are determined by the jumpers in SB3. In the following example, the six bit base address will be represented as XXXXXX.

In both modes of operation, output to any of the four ports in the block will write data from the S100 buss to the SBC-100S.

OUTPUT In Mode 1 and 2

XXXXXX00	Port used to transfer data and commands from the S100 to the SBC-100S
XXXXXX01	SAME function
XXXXXX10	SAME function
XXXXXX11	SAME function

INPUT From SBC-100S In Mode 1: Interrupt Vector Mode

XXXXXX00 Input data and commands from the SBC-100S to the S100 buss

XXXXXX10 Same as XXXXXX00

XXXXXX01 Disabled in this mode of operation. The SBC-100S will not respond to an input from this port unless ECN #005 is applied to the board.

XXXXXX11 Same as XXXXXX01

In this mode of operation, an interrupt vector (which can be modified by the SBC-100S) is placed onto the data buss for interrupt processing. This vector is designed to be used with the Z80 Mode 2 interrupt processing, The vector can be also be used as an indirect displacement into an interrupt processing routine on a system that does not support the Z80's Mode 2 interrupt system. When using more than one SBC-100S in the same motherboard, the daisy chain jumpers must be inserted such that only one board places its vector onto the buss during INTA. The daisy chain area is adjacent to S-100 pins 4 through 11. Also see sheet 3 of slave schematic.

The value of the vector that is placed onto the buss is determined by SB5 and the six bits that the SBC-100S can modify under software control. This is illustrated as follows:

INTERRUPT ACKNOWLEDGE VECTOR

BITS 7 through 3: Programmed by SBC-100S

BIT 2: (Shorting Block #5)

If a jumper is inserted, this bit gives the status of the BRDY bit. If on, data is ready to be transferred from the SBC-100S to the S100 buss. If off, data from the SBC-100S is not ready to be sent to the S100 buss.

This jumper is prewired on the SBC-100S PC card.

BIT 1: (Shorting Block #5)

If a jumper is inserted here, bit 1 gives the status of the ARDY line. If on, data can be written to the SBC-100S from the S100 buss. If off, data cannot be written to the SBC-100S from the S-100 buss.

This jumper is also prewired on the SBC-100S PC card.

INPUT FROM SBC-100S IN MODE 2: Status Port Mode

In this mode of operation, the SBC-100S will not respond to interrupt acknowledge. The INTA byte described above can be accessed by reading a status port. It should be noted that though the SBC-100S will not place a vector onto the buss during INTA, it can still be programmed to generate an interrupt whenever it has data or commands to send or receive from the S100 buss. The status port can then be interrogated to determine the cause of the interrupt. The input ports in this mode of operation are:

XXXXXX00 Data and command input

XXXXXX10 Same as XXXXXX00

XXXXXX01 Input from this port presents SBC-100S status to the S100 buss

XXXXXX11 Same as port XXXXXX01

II. Interfacing - Slave

B. SBC-100S Internal Port Assignments

This section describes the internal port assignments and functions of the SBC-100S.

Port Address	Port Identification
80H	Serial Channel A data input and output.
81H	Serial Channel A status and commands.
82H	Serial Channel B data input and output.
83H	Serial Channel B status and commands
84H	Parallel Channel A data (External Access)
85H	Parallel Channel A command (External Access)
86H	Parallel Channel B data (External Access)
87H	Parallel Channel B command (External Access)
88H	CTC Channel 0 - baud rate generator for serial channel A
89H	CTC Channel 1 - baud rate generator for serial channel B
8AH	CTC Channel 2 - output connected to CTC 3 input
8BH	CTC Channel 3 - available for RTC
9CH	Parallel Channel C input data (S-100 to Slave Data Port)
9DH	Parallel Channel C command (Program for Input)
9EH	Parallel Channel D output data (Slave to S-100 Data Port)
9FH	Parallel Channel D command (Program for Output)

B. SBC-100S Internal Port Assignemnts (Continued)

Port Address	Port Identification
90H	Auxiliary Control Port A (Output Only)
91H	Same as Port 90
92H	Auxiliary Control Port B (Output Only)
93H	Same as Port 92

The remaining ports on the SBC-100S are not used, although the port 94H through 9FH are reserved for future expansion boards. Expansion boards are attached via two X-Buss connectors located at the top of the SBC-100S. (Consult factory if expansion boards other than those manufacterd by Sierra Data Sciences are to be used).

Details on programming the Zilog SIO, PIO, and CTC support chips are available either directly from Zilog or as a supplemental manual from SDS.

1. Programming The Auxiliary Control Ports

Auxiliary Control Port A

External or Internal reset will initialize all bits in this register to zero.

Bit 7: Interrupt On Input Available (Slave to Master Data Transfer)

When this bit is enabled, an interrupt will be generated whenever the S-100 PIO has a character ready to be read by the host processor. When this bit is disabled, interrupts from the S-100 PIO to the host processor are disabled.

Bit 6: Interrupt On Input Receiver Ready (Master to Slave Data Transfer)

When this bit is enabled, the SBC-100S will generate an interrupt whenever it is ready to receive a character from a host S100 buss processor. When this bit is disabled, interrupts on input receiver ready are disabled.

Bits 5 through 0 Interrupt Vector Control Address

These bits control the interrupt vector that is placed on the S100 buss during INTA (When the SBC-100S is configured in Z80 interrupt Mode 2). The following table defines the bit mapping for the INTA byte value.

Auxiliary Port Bit	Corresponding INTA Byte Bit
Bit 4	Bit 7
Bit 3	Bit 6
Bit 2	Bit 5
Bit 1	Bit 4
Bit 0	Bit 3
Bit 5	Bit 0

When the SBC-100S is configured in Mode 2, the above bit assignments correspond to the value that will be read from the S100 buss whenever an input from the SBC-100S status port is performed.

2. Auxiliary Output Port B

External or internal reset initializes all bits to zero.

Bits 7 and 6: 16K Memory Disable

These two bits determine which 16K bank is disabled on the SBC-100S when EPROM on the board is enabled.

BIT 7	BIT 6	Disabled Bank Address
0	0	C000H - FFFFH
0	1	8000H - C000H
1	0	4000H - 8000H
1	1	0000H - 4000H

Bit 0: Bank Switch Enable

When this bit is zero, the bank switching feature of the SBC-100S is enabled. When this bit is a one, the bank switching feature is disabled.

Bit 1: EPROM/RAM Enable

When this bit is zero, the on-board EPROM is enabled and occupies memory as defined by bits 6 and 7 of any port B. When this bit is a one, the on-board EPROM is disabled and RAM locations C000H through FFFFH are enabled.

The following table illustrates the means by which bits 7, 6, 1, and 0 are used to control different 16K banks of on-board memory.

BIT 7	BIT 6	BIT 1	BIT 0	Memory Map 0	16	32	48K Bank
0	0	0	0	R	R	R	P
0	0	0	1	R	R	R	E
0	0	1	0	R	R	R	R
0	0	1	1	R	R	R	R
0	1	0	0	R	R	E	P
0	1	0	1	R	R	E	R
0	1	1	0	R	R	R	R
0	1	1	1	R	R	R	R
1	0	0	0	R	E	R	P
1	0	0	1	R	E	R	R
1	0	1	0	R	R	R	R
1	0	1	1	R	R	R	R
1	1	0	0	E	R	R	P
1	1	0	1	E	R	R	R
1	1	1	0	R	R	R	R
1	1	1	1	R	R	R	R

R=On-Board RAM P=On-Board EPROM E=Extended Memory

NOTE: The extended memory refers to banks of memory accessable through the overhead X-Buss connector.

Bits 5 and 4: Block Move Enable

If bit 5 is set to one, the wait line is enabled when the host (or "master") processor attempts to read data from the SBC-100S.

If Bit 4 is set to one, the wait line is enabled when the host processor attempts to write data to the SBC-100S.

Bits 4 and 5 are used to synchronize block move transfers on the S100 buss (to and from the SBC-100S). Note that, before these bits are enabled, the S100 PIO must be in the ready state. This prevents unsolicited wait states from being placed on the buss.

Bit 2: EPROM Power Enable

When this bit is enabled, the optional EPROM programmer will be activated for EPROM 4 (position U13). To successfully program an EPROM, the user must repeatedly write to it 2000 times. Each memory write requires 25 micro-seconds (4 Mhz version). For example, burning an EPROM area of 1K will take 1024 * 25 usec * 2000, or 51 seconds. During the time that this bit is on, reading from the EPROM being programmed is inhibited. Hence, to verify the program just burned, this bit must first be reset.

Bit 3: Reset Disable

When this bit is enabled, the S100 buss reset line will be ignored by the SBC-100S. If this bit is disabled, after being enabled, an on-board reset will be immediately invoked. This is an on-board only hardware reset. If ECN #005 is applied, this function is disbled.

C. Baud Rate Generation

Baud rate clocks are generated by channels 0 and 1 of the CTC for serial channels A and B respectively. The SBC-100 CTC divides a 2 MHz clock input down to generate commonly used baud rates as shown in Table A below. The Dart/SIO is programmed with a dividing factor also shown in the table. With this scheme, baud rates up to 38.4 kilobaud are possible.

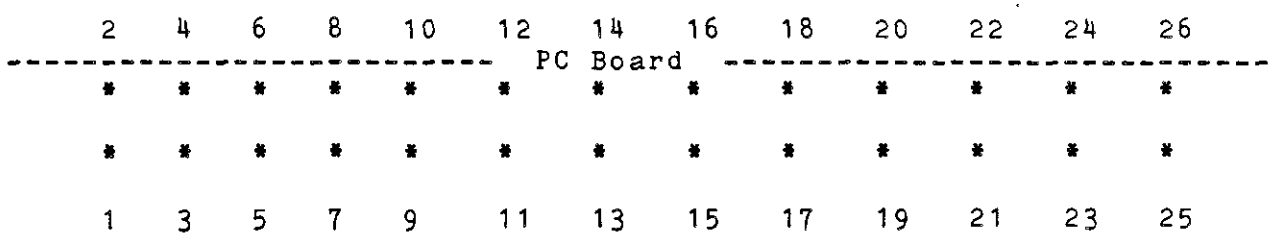
Slave Processor Baud Rate Codes

Baud Rate	CTC Time Constant	DART/SIO Dividing Factor
38.4	3D	X16
19.2	6D	X16
9600	12D	X16
4800	24D	X16
2400	48D	X16
1200	96D	X16
600	192D	X16
300	96D	X64
150	192D	X64

D. Reset/Start Sequence -

When the SBC-100S processor is reset, the on-board PROM is enabled at addresses 0C000 to 0FFFF and the CPU is forced to execute the first 3 bytes of the PROM installed at 0C000. This should be a JMP to the start of the code in the PROM. If the code in the PROM immediately follows the initial JMP, then this would be JMP 0C003H. Following this first access to the PROM memory space, the RAM memory from 0000 to 0BFFF is activated.

Figure 1 - PIO Interface Connector



	Slave	Master
1 - B3	2 - Ground	22 - ARDY
3 - B4	4 - N.C.	26 - BRDY
5 - B7	6 - B1	
7 - B6	8 - B2	
9 - B5	10 - B0	
11 - A7	12 - Reset	
13 - A6	14 - N.C.	
15 - A5	16 - +5V @100 ma	
17 - A4	18 - Ground	
19 - A3	20 - BSTB	
21 - A2	22 - BRDY	
23 - A1	24 - ASTB	
25 - A0	26 - ARDY	

Figure 1.
PIO Connections
Master Connector H4
Slave Connector J3

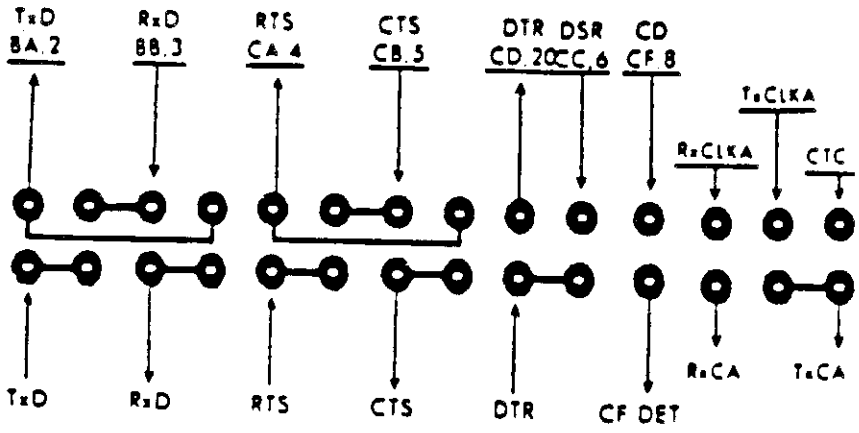


Figure 2.
SIO Configuration
Header connections
Shorting Blocks
1 and 2.

Shorting Blocks 3,4 and 5

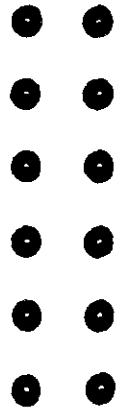


Figure 3.
Shorting Block 4
Port address selection

A Shunt in place indicates a 1 in the appropriate bit of the address. Note that bits A0 and A1 are not decoded.

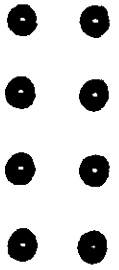


Figure 4.
Interrupt Configuration Area
Shorting Block 3

Place shunts in either Interrupt or No Interrupt Locations to control Interrupts to the S100 Master Processor. Note that two shunts are needed for both configurations.

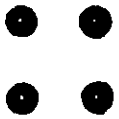


Figure 5.
Shorting Block 5

If shunt is in place, appropriate line will be readable in the interrupt vector to the S100 buss

X-Buss Expansion Interface Connectors

X-Buss Interface Connector J1

Pin Number	Name	Function
1	A7	\
3	A6	\
5	A5	\
7	A4	! Low order Address Lines
9	A3	!
11	A2	/
13	A1	/
15	A0	/
17	IORQ-	I/O Request
19	RD-	Read Cycle
21	PWR-	Write Cycle
23	WAIT-	Processor Wait
25	INT-	Processor Interrupt
27	D1	\
29	D0	\ Data Lines
31	D7	/
33	D2	/
35	M1-	M1 (Instruction Fetch) Cycle
37	D6	\
39	D5	\ Data Lines
41	D3	/
43	D4	/
45	CLOCK	System Clock (4 Mhz)
47	RESET-	Board Reset
49	IORQ'-	Delayed IORQ
50	IEO	Interrupt Daisy Chain Out

X-Buss Interface Connector J2

1	A15	Address Line
2	RFRSH-	Memory Refresh
3	A14	\
5	A13	\
7	A12	\
9	A11	! High Order Address Lines
11	A8	/
13	A9	/
15	A10	/
17	EXTRAM	X-Buss Extended Memory
19	MREQ-	Memory Request

NOTES:

1) All even numbered pins (except J1-50 and J2-2) are grounded.
2) All lines will drive **ONE** TTL load. Buffers are required on any expansion board to prevent excessive loading of the Z80 chip.
3) A dash (-) following a signal name indicated a Low True signal.

On-Board Interrupt Priority Chain

Highest:	CTC Channel 0
	CTC Channel 1
	CTC Channel 2
	CTC Channel 3
	S100 PIO Channel A
	S100 PIO Channel B
	External PIO Channel A
	External PIO Channel B
	SIO Channel A
	SIO Channel B
Lowest:	X-Buss

Configuring An OkiData Microline Parallel Printer

The following procdeure should be used when connecting an OkiData Microline 82A or 83A printer using the the parallel port of the SBC-100 or SBC-100S.

It is recommended that the parallel ports be connected to a twenty-six (26) pin socket and terminated with a DB-25 crimp-on connector. This part is available from SDS, part number SBC-CAB5. The last wire may be cut off since this wire is not used in the interface. After this is done you may use the table below to construct a printer cable. The connector that mates with the OkiData parallel interface is Amphenol part number 57-30360. Both these cables are available through SDS.

SBC-100 PIO Pin	Pin # on Microline	DB-25 Pin
PIOB Bit 6	1, Data Strobe	4
PIOA Bit 0	2, Bit 1	13
PIOA Bit 1	3, Bit 2	12
PIOA Bit 2	4, Bit 3	11
PIOA Bit 3	5, Bit 4	10
PIOA Bit 4	6, Bit 5	9
PIOA Bit 5	7, Bit 6	8
PIOA Bit 6	8, Bit 7	7
PIOA Bit 7	9, Bit 8	6
PIOA ASTRB	10, ACK	25
PIOB Bit 7	11, Busy	3
Ground	19 to 30, Ground	14 or 22

TITLE: Enginnering Change Notice
Effective Date: 10 Dec 82

Document # ECN005
Written by: T.P.Stradtman

GENERAL

This ECN describes an optional modification that may be made to the SBC-100S to allow a buss master to generate a hardware reset within the slave processor.

USAGE

After this ECN has been applied, any buss master may reset the slave proccesor by reading from the third port of the slave.

Determining Reset Address

The address to be accessed to generate the reset signal is computed by adding three (3) to the slave's base port address. For example, if a slave is addressed at 40 (hex), the reset port is at 43 (hex).

IMPLEMENTATION

To apply this ECN, one (1) trace must be cut, and four (4) jumpers must be added to the SBC-100S slave proceesor card.

Trace Cut

The only trace to be cut is connected to U35 (LS123) Pin 1. This cut may be made in of two ways. Either the trace can be cut away on the component side of the board, or pin 1 may be removed from the socket and a jumper soldered to it. Refer to Figure 1 for the location of the trace to be cut.

Jumpers

There are four jumpers to be made for this ECN. Refer to figure 2 for the exact location of these jumpers.

1. U29 (LS11) pin 3 to U25 (LS04) pin 11 [ ]

2. U29 pin 4 to U29 pin 12 [ ]

3. U29 pin 5 to J6 (S100 buss) pin 80 [ ]

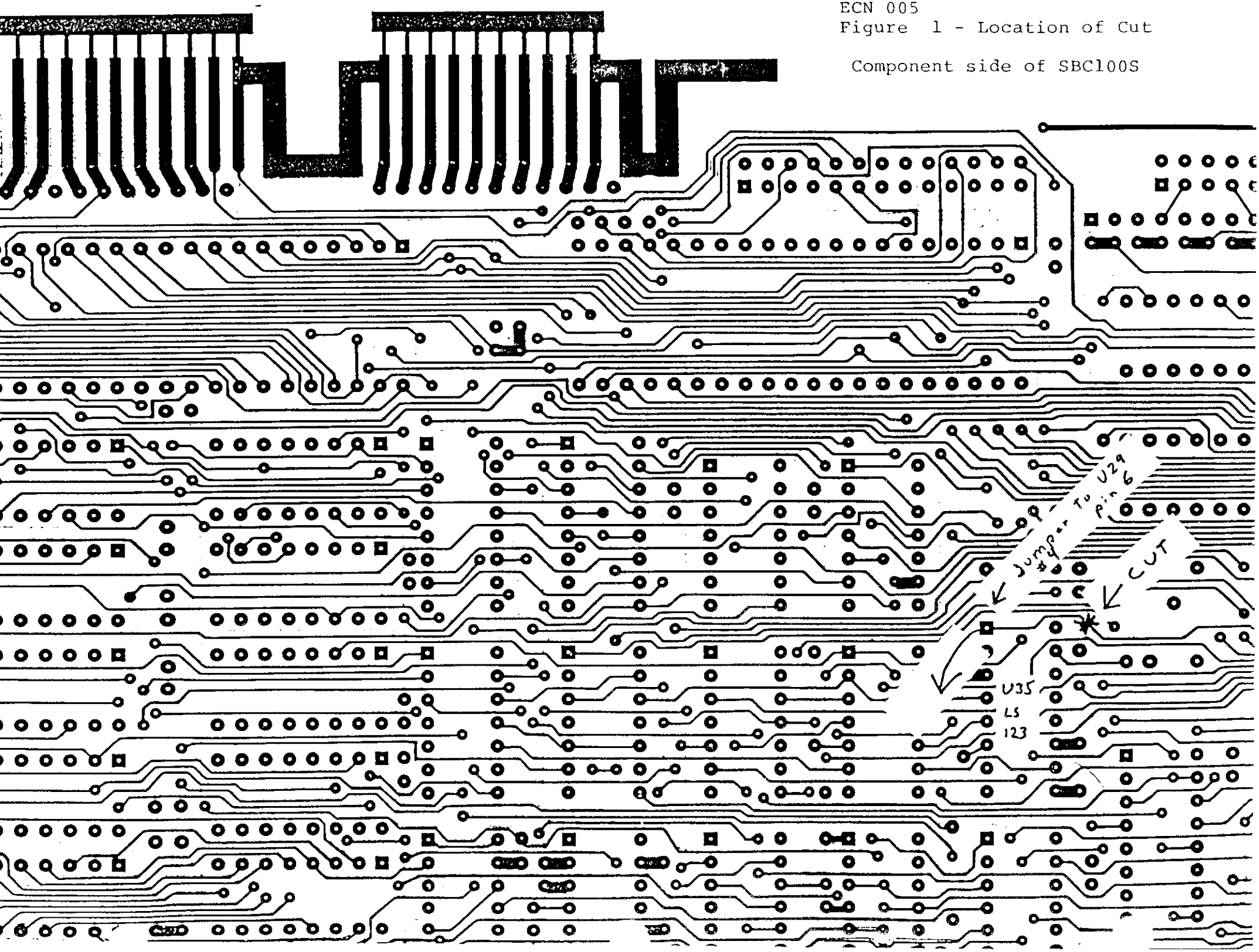
4. U29 pin 6 to U35 (LS123) pin 1 [ ]

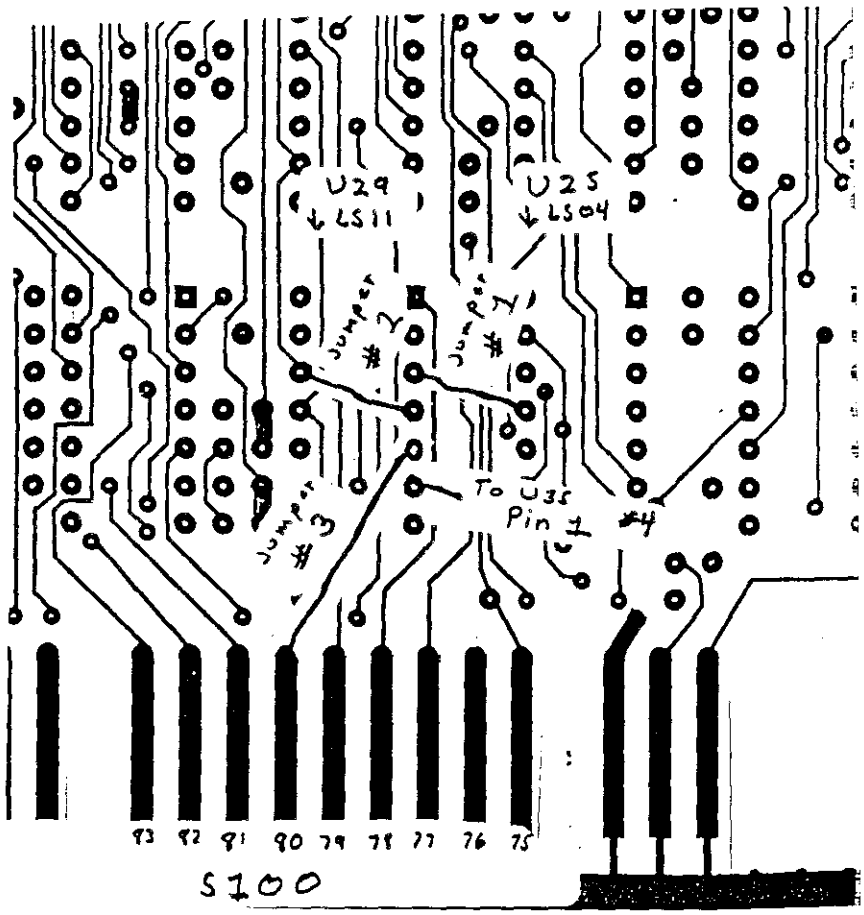
Theory Behind Changes

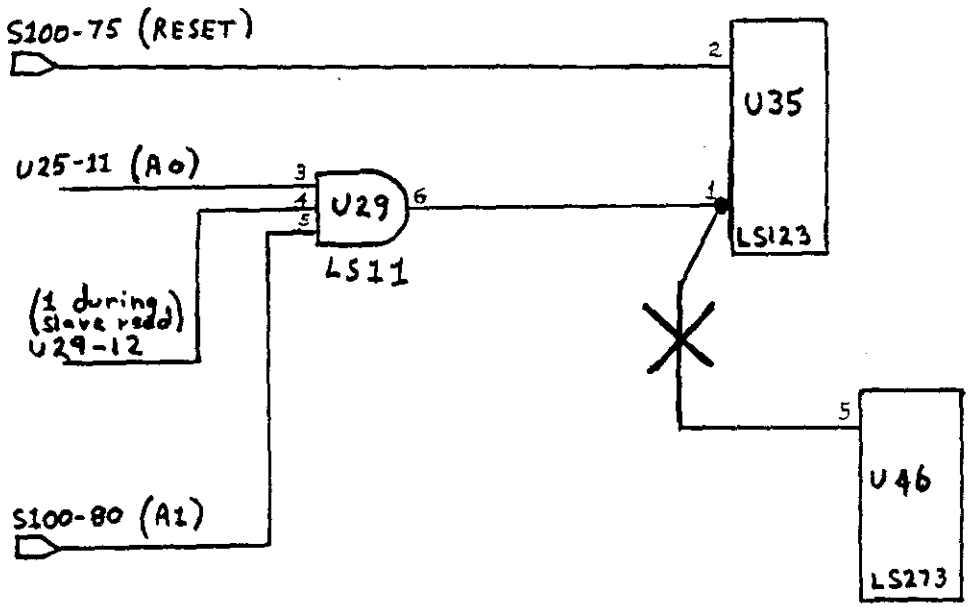
This ECN uses the S100 address line A1 in conjunction with the onboard select signal to trigger the LS123 single-shot instead of the auxiliary control register front panel reset disable signal. If this ECN is applied, the onboard reset function of auxiliary control port A is disabled.

ECN 005
Figure 1 - Location of Cut

Component side of SBC100S







ECN005
Figure 2 - Location of Jumpers

Solder side of SBC100S

If you have any questions, problems or suggestions, please send them to the following address:

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