ST225N

PRODUCT MANUAL

Seagate

ST225N PRODUCT MANUAL

February 10, 1986©
36015—001, Revision H

Seagate™ reserves the right to change, without notice, the specifications contained in this manual.

Seagate ■ 920 Disc Drive, Scotts Valley, CA 95066-4544, USA
Tel. (408) 438-6550 ■ Telex 176455 SEAGATE SCVL

TABLE OF CONTENTS

FIGURES

TABLES

INTRODUCTION

The Seagate ST225N, with its embedded controller, provides OEMs and system integrators with over 21 megabytes of guaranteed formatted capacity in a shock-resistant half-height package. Seagate's intelligent disc drive is a low-power full-function disc subsystem designed for desktop systems. Whether in rugged industrial or quiet office environments, the space-saving ST225N provides a low-cost high-performance solution for single user systems.

High-reliability is assured through the use of LSI and surface-mount devices on a single printed circuit board. The ST225N uses fewer parts, cables and connectors for improved subsystem reliability. SCSI protocol is completely device independent and supports logical addressing, implied seeks, overlapped operations and multi-sector transfers up to 1.25 megabytes/second. Media defects and error recovery are efficiently managed within the device and fully transparent to the user.

Our manufacturing facilities have been designed and located exclusively for high-volume production and testing of disc drives. Seagate's ongoing commitment to vertical integration assures availability of the latest technology at the same consistent quality and lowest possible cost.

ST225N REVISION H, February 10, 1986
Note: Sections which have been revised are highlighted with a gray screen.

ST225N INTELLIGENT DISC DRIVE SPECIFICATIONS 1.0

1.1 INTERFACE SUMMARY

SCSI as defined by ANSI X3T9.2/82-2. The ST225N supports the SCSI extended command set for self-configuring software.

- Disconnected Operations
- Linked Commands
- 1 Kbytes FIFO Buffer
- Maximum Data Transfer Rate: 1.25 Mbytes/sec.
- Average Data Transfer Rate: 625 Kbytes/sec.
- Maximum Cable Length: 19.7 ft. (6 meters)
- Provides Support for Arbitrating and Nonarbitrating Host Systems

1.2 DRIVE CAPACITY AND PERFORMANCE

1.2.1 FORMATTED CAPACITY

Guaranteed Megabytes per Drive:	22.57	21.36	20.13
Bytes per Cylinder:	36,864	34,816	37,768
Bytes per Track:	9,216	8,704	8,192
Bytes per Sector:	1,024	512	256

1.2.2 DATA ORGANIZATION

Guaranteed Sectors per Drive:	22,040	41,720	78,620
Sectors per Cylinder:	36	68	128
Sectors per Track:	9	17	32

1.3 PERFORMANCE SPECIFICATIONS

1.3.1 ACCESS TIME

Track-to-Track:	20 msec.
Average:	65 msec. [1]
Maximum Seek:	150 msec. [1]
Average Latency:	8.33 msec.

1. Nominal power and temperature

1.4 FUNCTIONAL SPECIFICATIONS

Tracks:	2,460
Cylinders:	615
Read/Write Heads:	4
Discs:	2
Rotational Speed:	3,600 ±1%
Recording Method:	MFM
Recording Density:	9,827 BPI/FCI
Track Density:	588 TPI
Interface:	SCSI
Data Command Rate:	Up to 1.25 Megabytes/sec.
Nonrecoverable Read Errors:	1 per 10^{12} bits read

1.5 RELIABILITY SPECIFICATIONS

MTBF:	20,000 Power-on hours[2]
PM:	Not Required
MTTR:	30 minutes
Component Design Life:	5 years

1.6 ENVIRONMENTAL SPECIFICATIONS

1.6.1 AMBIENT TEMPERATURE

Operating:	10°C to 45°C (50°F to 113°F)
Nonoperating:	-40°C to 60°C (-40° to 140°F)

1.6.2 TEMPERATURE GRADIENT

Operating:	10°C/hr max. (18°F/hr)
Nonoperating:	Below condensation

1.6.3 RELATIVE HUMIDITY

Operating:	8 to 80% noncondensing
Maximum Wet Bulb:	78.8°F (26°C)
Nonoperating:	Below condensation

1.6.4 ALTITUDE

Operating:	-1,000 ft to 10,000 ft
Nonoperating:	-1,000 ft to 30,000 ft

1.6.5 OPERATING SHOCK

Maximum permitted shock without incurring physical damage or degradation in performance: 10 G's[3,4]

---

2. Typical usage at 25°C, at sea level. Calculated per *Mil. Spec. Handbook 217*
3. 11 msec. half-sine wave shock pulse.
4. Input levels at the drive mounting screws. Unit mounted in an approved orientation.

1.6.6 OPERATING VIBRATION

Maximum permitted vibration, at the following frequencies, without incurring physical damage or degradation in performance: [4]

Frequency	Vibration
5 — 22 Hz	.010″ double amplitude
22 — 300 Hz	.25 G peak amplitude
300 — 22 Hz	.25 G peak amplitude
22 — 5 Hz	.010″ double amplitude

1.6.7 NONOPERATING SHOCK

Maximum permitted shock without without incurring physical damage or degradation in performance: 40 G's [3,4,5]

1.6.8 NONOPERATING VIBRATION

Maximum permitted vibration, at the following frequencies, without incurring physical damage or degradation in performance: [4,5]

Frequency	Vibration
5 — 22 Hz	.010″ double amplitude
22 — 300 Hz	.50 G peak amplitude
300 — 22 Hz	.50 G peak amplitude
22 — 5 Hz	.010″ double amplitude

1.7 PHYSICAL SPECIFICATIONS

Height:	1.63 inches max. (41.4 mm)
Width:	5.75 inches max. (146.05 mm)
Depth:	8.00 inches max. (203.2 mm)
Weight:	2.75 lbs. (1.25 Kg)

1.8 DC POWER REQUIREMENTS

The ST225N is listed in accordance with UL 478 and CSA C22.2 (0-M1982), and meets all applicable sections of IEC 380 and VDE 0806/08.81, as tested by *TUV-Rheinland, North America.*

Power may be applied or removed in any sequence without loss of data or damage to the drive.

+12 VDC

Voltage Tolerance (including ripple):	±5%
Maximum Current at Power-on:	2.2 Amps
Typical:	0.9 Amp

+5 VDC

Voltage Tolerance (including ripple):	±5%
Typical:	1.2 Amps with termination 1.0 Amps without termination

Power: 16.8 Watts nominal with termination packs installed [6]

5. Heads positioned in the shipping zone
6. Measured under the following standard operating conditions:
   a. 25 °C ambient temperature
   b. Sea level
   c. Nominal voltages applied
   d. Spindle rotating with drive not seeking.

1.8.1 INPUT NOISE RIPPLE

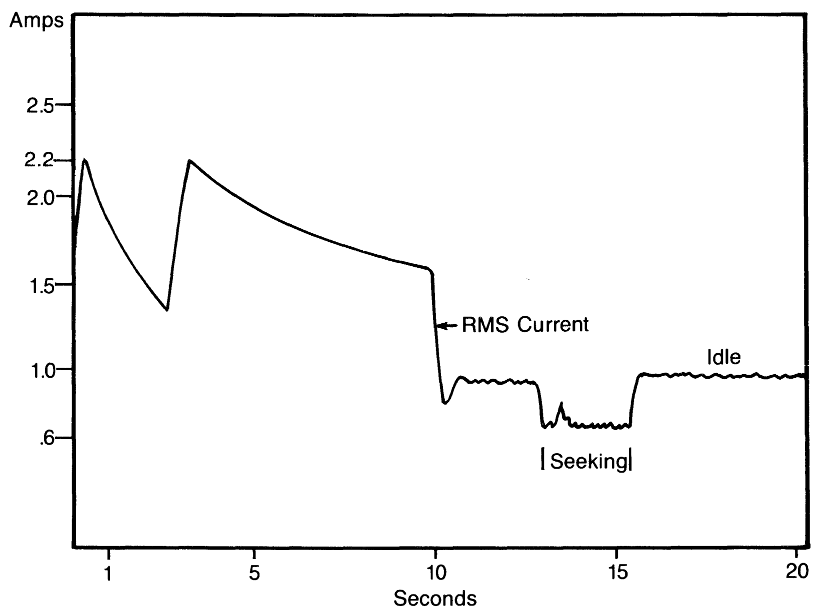
The maximum permitted input noise ripple is 100 mV (peak-to-peak) on either +5 VDC or +12 VDC measured on the host system power supply across the following equivalent resistive loads:

+12 VDC: 16 Ω
+5 VDC: 5 Ω

1.8.2 INPUT NOISE FREQUENCY

The maximum permitted input noise frequency is 20 MHz on both the +12 VDC and +5 VDC lines.

Figure 1: Typical RMS +12 VDC Start-up Current Profile



1.9 MOUNTING REQUIREMENTS

The ST225N may be mounted in the following orientations:

Horizontal:	Spindle Motor down
Sides:	Left or right

The drive should not be tilted front to back, in any position, by more than ±5°.

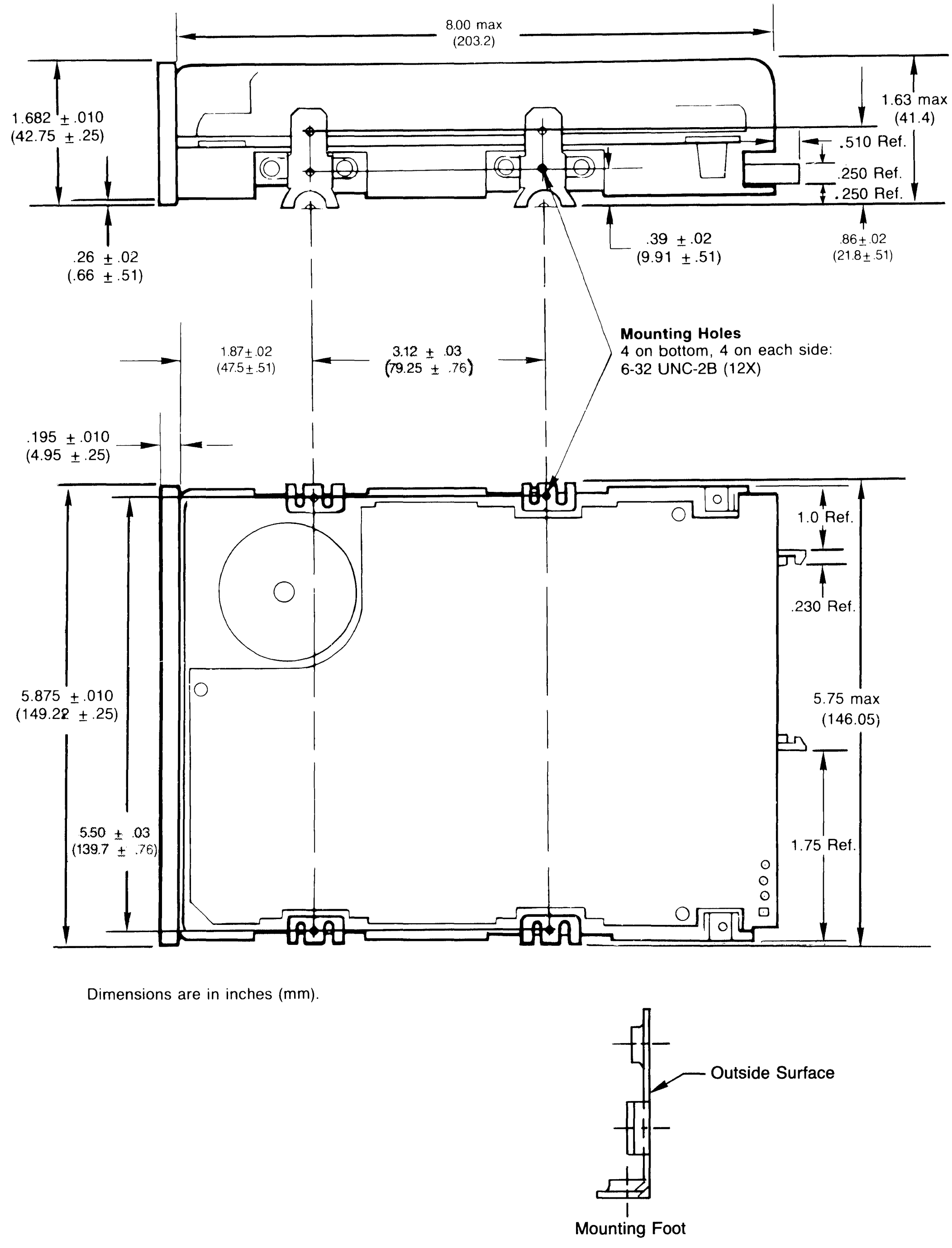
1.9.1 HANDLING AND STATIC DISCHARGE PRECAUTIONS

It is recommended that any external shock mounts between the drive and the host frame be designed so that the composite system has a vertical resonant frequency of 25 Hz or lower.

A minimum clearance of 0.050 inch should be allowed around the entire perimeter of the drive to allow for cooling airflow and mechanical vibration during shock or vibration.

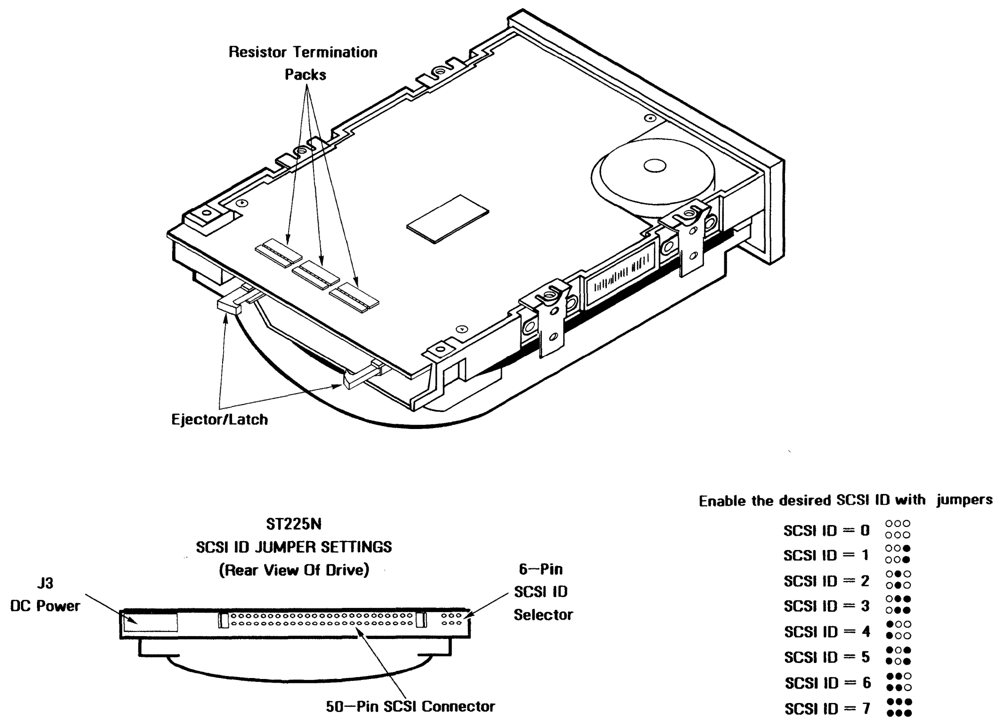
After unpacking and prior to system integration, the drive is exposed to potential handling and ESD hazard. Observe standard static-discharge precautions and handle the drive by the frame only.

Figure 2: Mounting Requirements



NOTE: The mounting screws must not extend inside the mounting feet more than 0.125 inch, measured from the outside surface of the foot. See detail in *Figure 2.*

Figure 3: Host / Drive Interface Connectors



1.10 I/O CABLE REQUIREMENTS

1.10.1 CABLE

A 50-conductor flat cable or 25-conductor twisted pair cable is required. The maximum cable length is 19.7 ft (6 meters). Each SCSI bus connection shall have a 0.1 meter maximum stub length.

The characteristic impedance for unshielded flat or twisted pair ribbon cable should be 100 Ω ±10%. A characteristic impedance greater than 90 Ω is preferred for shielded cables. It is desireable to minimize the use of cables of different impedances in the same bus, so as to minimize discontinuities and signal reflections. Various implementations may require trade-offs in shielding effectiveness, cable length, the number of loads, transfer rates, and cost to achieve satisfactory system operation.

1.10.2 BUS TERMINATION

SCSI bus termination is provided within the device by removable resistor termination pack. The termination pack must be installed on the last drive on the interface cable.

1.10.3 CONNECTOR REQUIREMENTS

The drive connector is a 50-conductor connector consisting of two rows of 25 male pins on 100 mil centers.

The cable connector is a 50-conductor nonshielded connector consisting of two rows of 25 female contacts on 100 mil. centers. Recommended strain-relief connectors are AMP part number 1-499506-2 or DUPONT part number 669002 (66900-250)

Figure 4: Nonshielded Cable Connector

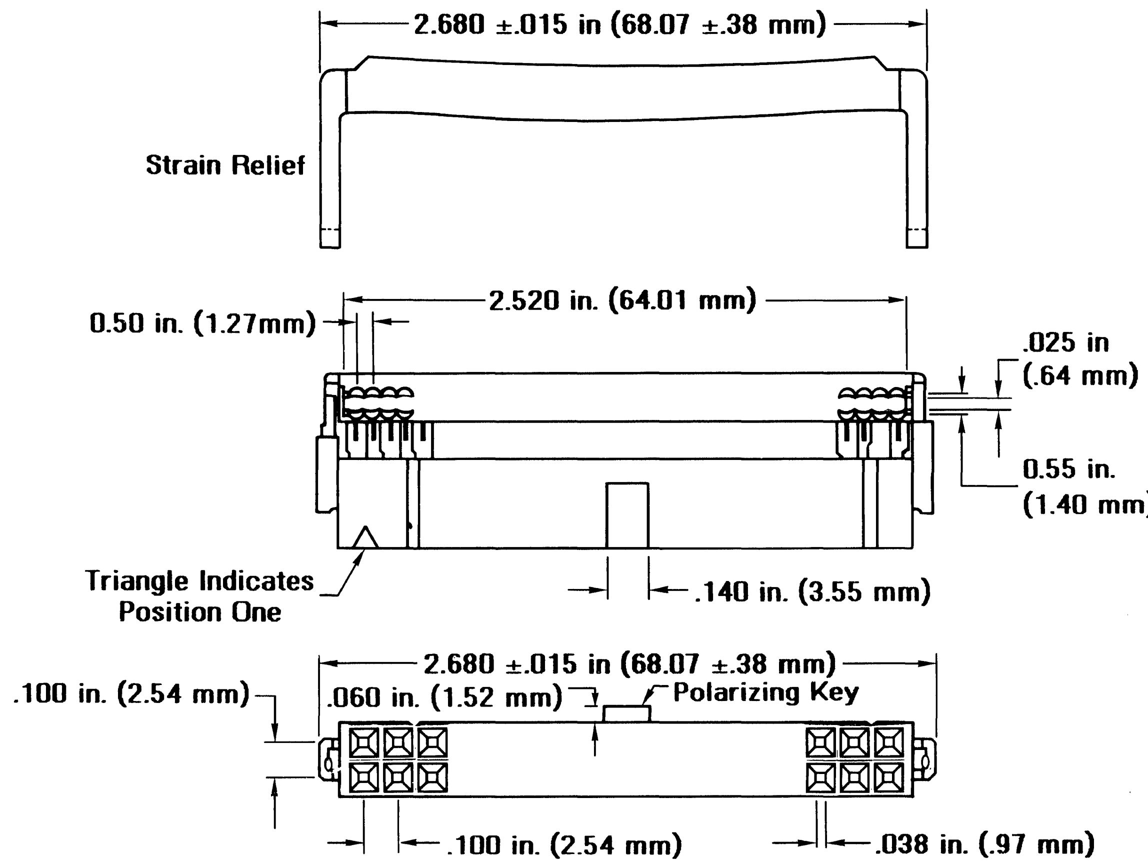


Table 1: ST225N Connector Pin Assignments

Note: All odd pins, except pin-25, must be connected to ground. Pin-25 should be left open, but may be connected to ground.

Signal	Pin Number	Signal	Pin Number
-DB(0)	2	Ground	28
-DB(1)	4	Ground	30
-DB(2)	6	-ATN	32
-DB(3)	8	Ground	34
-DB(4)	10	-BSY	36
-DB(5)	12	-ACK	38
-DB(6)	14	-RST	40
-DB(7)	16	-MSG	42
-DB(P)	18	-SEL	44
Ground	20	-C/D	46
Ground	22	-REQ	48
Ground	24	-I/O	50
Not Connected	26		

1.11 SCSI BUS DRIVERS/RECEIVERS

The ST225N uses open collector drivers which meet the electrical requirements defined below.

All signals are terminated with 220 Ω to +5 VDC (nominal) and 330 Ω to ground. The terminating resistors are removable for multi-drive configuration.

Each signal driven by the ST225N has the following output characteristics, when measured at the drive connector:

Signal assertion	= 0.0 VDC to 0.4 VDC
Minimum driver output capability	= 48 mA (sinking) @ 0.5 VDC
Signal negation	= 2.5 VDC to 5.25 VDC

Each signal received by the ST225N must have the following input characteristics, when measured at the drive connector:

Signal true:	0.0 VDC to 0.8 VDC
Maximum total input load:	-0.4 mA @ 0.4 VDC
Signal false:	2.0 VDC to 5.25 VDC
Minimum Input Hysteresis:	0.2 VDC

Note: For these measurements, SCSI bus termination is assumed to be external to the drive. A typical ST225N is supplied with the resistor termination packs installed

GENERAL PRODUCT DESCRIPTION 2.0

This section provides an overview of the product's capabilities, configurations and interface characteristics. The ST225N has an integral SCSI-compatible controller. This embedded controller performs all of the functions that were previously implemented by an add-on, or "host supplied" controller. With the controller onboard, the diagnostic capabilities of the drive are enhanced because the controller is able to optimize drive performance and error recovery.

2.1 INTERFACE

The embedded controller supports the SCSI interface as defined in the ANSI X3T9.2 document. The interface hardware is capable of transferring 1.2 Mbytes/second using asynchronous data transfer. Devices on the SCSI interface are daisy-chained together using a common cable. Both ends of the cable are terminated. All signals on the interface are common between all devices. The key elements of the interface are listed below.

- SCSI interface compatible with ANSI standard
- 1 Kbyte FIFO buffer
- 1.25 Mbyte/sec. data transfer rate (between controller and CPU)
- Selectable SCSI Bus Address
- Supports extended SCSI command set
- Supports disconnected operations
- Supports linked commands
- Extensive diagnostics and fault detection are provided
- Operates with arbitrating and non-arbitrating hosts
- Reports when error recovery was required
- Supports 1:1 interleave factor
- Reports error and usage information

2.2 ERROR RECOVERY

The controller provides error recovery routines which are necessary to assure data integrity. These techniques include ECC, seek-retry, read-retry, head-offset and defect management. To assure a high degree of data reliability, the controller utilizes a 32-bit error checking and correction polynomial.

2.3 DISC FORMAT

The disc format is flexible and supports sector sizes of 256, 512 and 1024 bytes per sector.

2.4 FORMATTING AND DEFECT MANAGEMENT

Media defects are identified and recorded on the disc during the manufacturing process. This defect map is used during formatting and enables the drive to bypass these defects. During the formatting operation, the controller uses the sector-slip technique to reassign defective sectors. A maximum of

100 sectors can be slipped by the controller. This product supports the following three variations of the Format Command:

- Format using a combined list of previously defined defects (manufacturer's list plus user-defined list)
- Format with previously defined list plus additional user-defined defects
- Format with manufacturer's list only (removes all user-defined defects)

Refer to the Format Unit Command, *Section 4.4,* for further details.

2.5 PERFORMANCE

The onboard controller allows data to be transferred to/from the host at a maximum data transfer rate of 1.25 Mbytes/second. The data is then stored in a 1 Kbyte FIFO sector buffer. The controller supports a 1:1 interleave factor which allows the drive to be configured for maximum system performance.

Note: 1,024-byte/sector requires a 2:1 interleave.

2.6 DIAGNOSTICS

The ST225N supports the following online diagnostics, which assure a high degree of data integrity. These routines are executed at power-on and verify the following controller and drive operations.

- Controller
- Read Operations
- Data Buffer
- Seek Operations
- ECC
- Spindle Speed

In the event that a failure is detected during the power-on/initialization routines, the drive will indicate the failure type by flashing the LED.

2.6.1 OFFLINE VERIFICATION PROGRAM

The ST225N provides an offline hardware and error rate verification program. A jumper at the I/O interface will enable the program. Included are the following routines:

1. Power-on hardware test
2. Read/Write verification on special test cylinder
3. Media scan of user data area
4. Seek Test

The program will continue to cycle as long as power is applied or the tests execute successfully. The LED functions as a pass/fail indicator and will remain on as long as the drive is operating and passing the verification routines. If the unit fails a test the test is terminated and the LED will be turned off.

2.7 RECORD INTERLEAVE

The ST225N supports user-specified record interleaves of 1:1 (records formatted sequentially on the disc) through the number of records per track minus one. This gives the user the ability to configure the drive for maximum performance within the operating environment.

2.8 SCSI BUS ADDRESS

Three jumpers are provided on the drive for selecting the SCSI bus address. The microprocessor accesses this information at power-on and configures its operation accordingly. Refer to *Figure 3* for address configuration details.

Note: The address jumpers are accessed during the initialization sequence. If the SCSI address is changed, the drive must be powered off/on or reset.

2.9 DRIVE CONFIGURATION

The ST225N supports four commands which determine and control the drive's operating environment.

Read Capacity:	Defines the formatted capacity
Inquiry:	Defines the drive type and identifies physical device parameters
Mode Sense:	Defines the drive's current operating environment
Mode Select:	Provides a method to change the operating characteristics of the drive

The host system can control the following key parameters:

- Total number of blocks available
- Block Length
- Record interleave
- Enable/disable of error recovery
- Enabling/disabling reporting of recovered error status
- Enabling/disabling of reporting, usage and error counter overflow

2.10 ERROR INFORMATION

The ST225N has extensive error logging and reporting capability which enables the user to design general error recovery procedures within the operating system I/O drivers.

Non device-specific error recovery procedures may be designed by using the SCSI Extended Sense capability and the Sense Keys. The error information contained within the Extended Sense bytes is sufficient to manage defects and measure error rates thereby insuring a high degree of data integrity. To retrieve the Sense information, a Request Sense Command must be sent immediately following a reported error.

3.0 SCSI INTERFACE DESCRIPTION

This is the physical path definition which is designed to provide an efficient method of communication between computers and peripheral devices, which includes the following features.

- Single daisy-chained cable with up to eight connections
- Asynchronous communications of up to 1.25 Mbytes/sec.
- Up to 19.7 ft. (6 meter) cable length
- Supports multiple overlaped disc drive operations

3.1 SCSI BUS

Communication on the SCSI bus is allowed between only two devices at any given time, with a maximum of eight (8) devices (including the host). Each device has a SCSI ID bit assigned, as indicated below in *Table 2.*

When two devices communicate on the SCSI bus, the unit originating the operation is designated as the *Initiator* and the unit performing the operation is designated as the *Target.* There may be any combination of Initiators and Targets.

Data transfers on the data bus are asynchronous and follow a defined REQ/ACK handshake protocol. One byte of information is transfered with each handshake.

Table 2: SCSI ID Bits

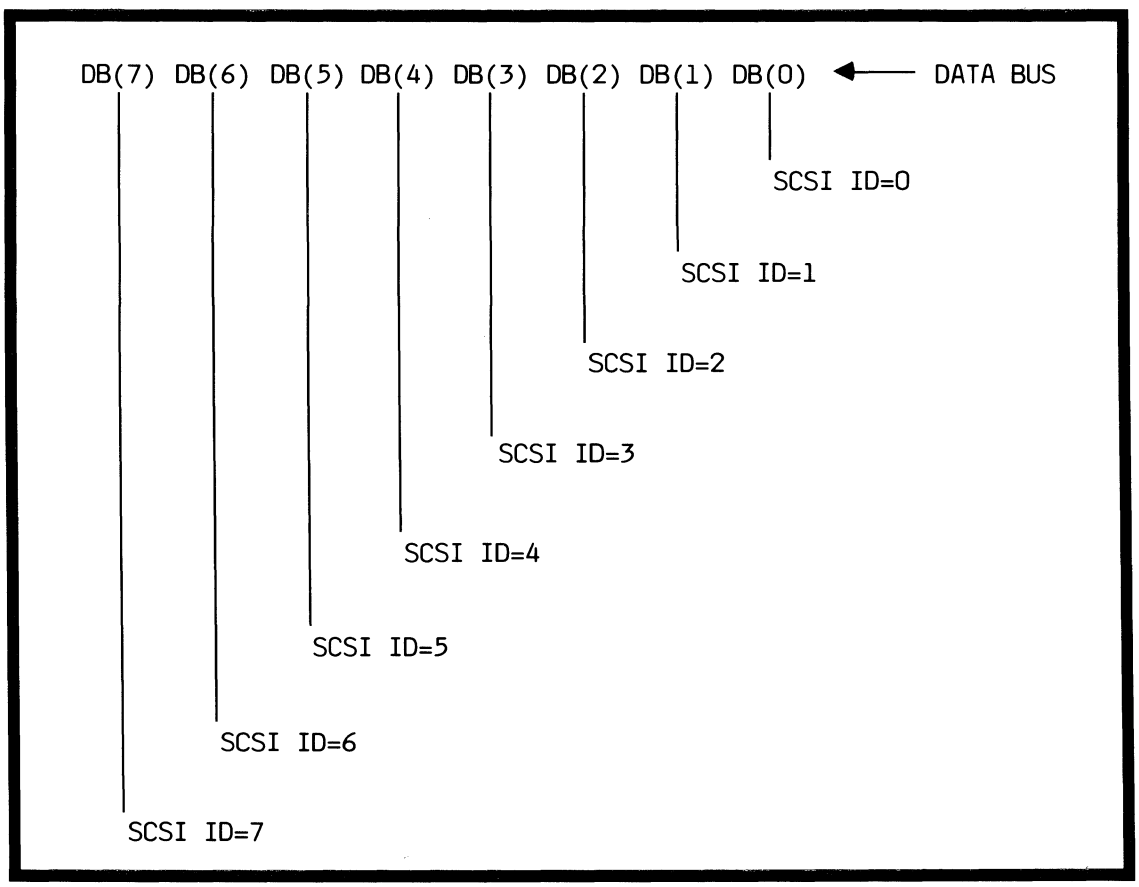
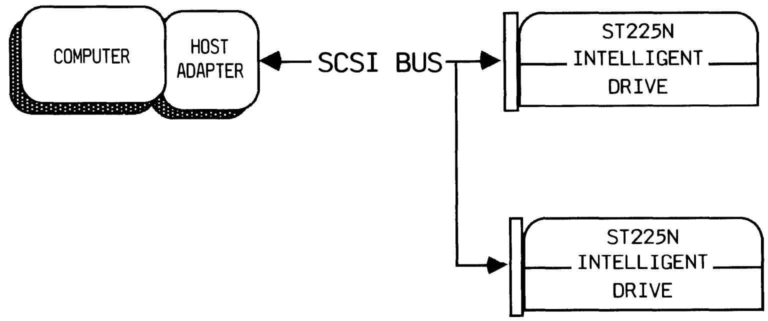
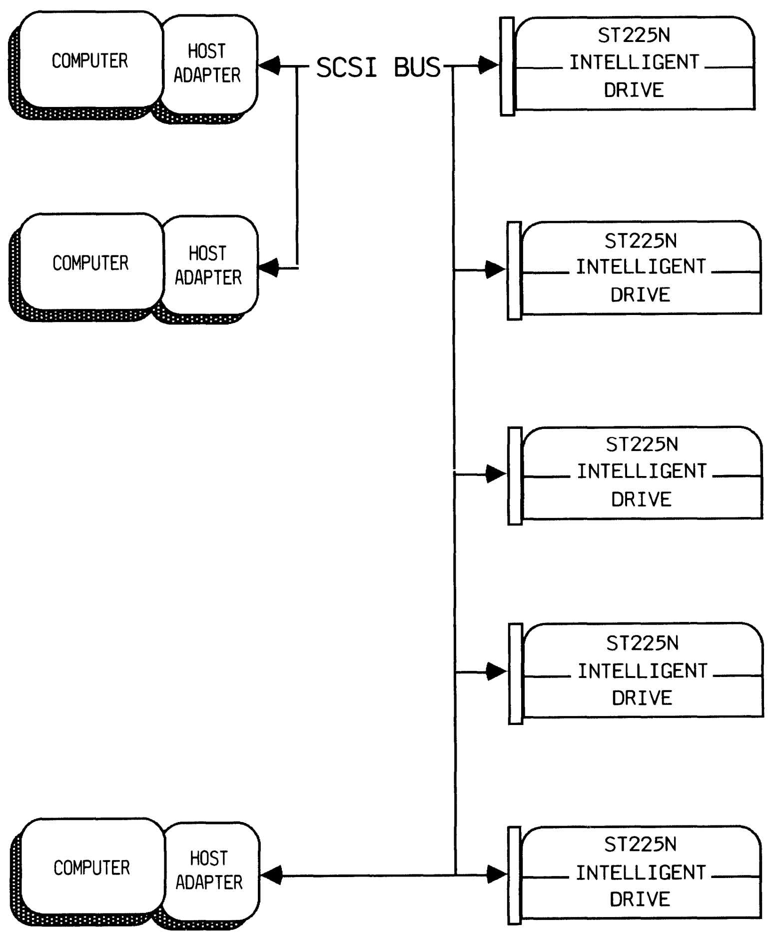


Figure 5: Sample SCSI Configurations

SINGLE INITIATOR, SINGLE TARGET



SINGLE INITIATOR, MULTI TARGET

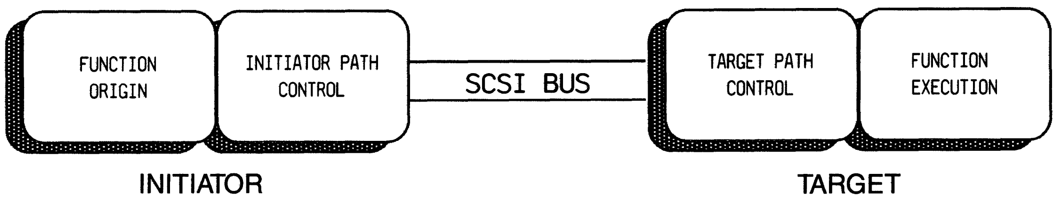


MULTI INITIATOR, MULTI TARGET

3.1.1 SCSI PHYSICAL PATH PHILOSOPHY

Figure 6 illustrates a typical Initiator/Target command execution on the SCSI bus. This is only one of a number of possible partitions of the physical/functional interface.

Figure 6: Physical Path



3.1.2 SCSI BUS SIGNALS

There are nine control signals and nine data signals.

Table 3: SCSI Bus Signals

Busy (BSY):	An "or-tied" signal which indicates that the bus is in use.
Select (SEL):	A signal used by an Initiator to select a Target or by a Target to reselect an Initiator.
Control/Data (C/D):	A signal driven by a Target. It indicates whether Control or Data information is on the data bus. True indicates Control.
Input/Output (I/O):	A signal driven by a Target which controls the direction of data flow on the data bus, with respect to an Initiator. True indicates input to the Initiator.
Message (MSG):	A signal driven by a Target during the message phase.
Request (REQ):	A signal driven by a Target to indicate a request for a REQ/ACK data transfer handshake.
Acknowledge (ACK):	A signal driven by an Initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.
Attention (ATN):	A signal driven by an Initiator to indicate the attention condition.
Reset (RST):	An "or-tied" signal which indicates the reset condition.

3.1.2.1 SIGNAL VALUES

Signals may assume either true or false values. There are two methods of driving these signals. In either case, the signal must be actively driven true.

In the case of the "or-tied" drivers, the driver does not drive the signal to the false state, instead, the bias circuitry of the bus terminators pulls the signal false whenever it is "released" (not driven by the drivers at every drive).

In the case of the "non or-tied" driver, the signal may be actively driven false or may be negated or simply released, in which case the bias circuitry will pull it false.

3.1.2.2 "OR-TIED" SIGNALS

The BSY and RST signals are "or-tied." In the ordinary operation of the bus, these signals are simultaneously driven true by several drivers. No other signals are simultaneously driven by two or more drivers. Any signal, other than BSY and RST, may employ "or-tied" or "non or-tied" drivers. There is no operational problem in mixing "or-tied" or "non or-tied" drivers on the same signal.

3.1.2.3 SIGNAL SOURCES

Table 4 indicates which type of device is allowed to source each signal. No attempt is made to show if this source is driving asserted, nonasserted or passive. All device drivers that are not active sources shall be in the passive state. Note that the RST signal may be sourced by any device.

Table 4: Signal Sources

Bus Phase	BSY	SEL	C/D, I/O MSG,REQ	ACK/ATN	DB(7-0,P)
Bus Free	None	None	None	None	None
Arbitration	All	Winner	None	None	SCSI ID
Selection	I & T	Initiator	None	Initiator	Initiator
Reselection	I & T	Target	Target	Initiator	Target
Command	Target	None	Target	Initiator	Initiator
Data In	Target	None	Target	Initiator	Target
Data Out	Target	None	Target	Initiator	Initiator
Status	Target	None	Target	Initiator	Target
Message In	Target	None	Target	Initiator	Target
Message Out	Target	None	Target	Initiator	Initiator

ALL: The signal shall be driven by all drives that are actively arbitrating.

SCSI ID: A unique data bit (the SCSI ID) must be driven by each SCSI drive that is actively arbitrating. The other seven data bits must be released, i.e., not driven by this device.

I & T: The signals are driven by the Initiator and/or Target as specified in the Arbitration and Selection phases.

INITIATOR: If this signal is driven, it may only be driven by the active Initiator.

NONE: This signal must be released, i.e., not driven by any SCSI device. The bias circuitry of the bus termninator pulls the signal to the false state.

WINNER: This signal must be driven by the one drive that wins Arbitration.

TARGET: If this signal is driven, it will be driven only by the active Target.

3.1.3 SCSI BUS TIMING

Unless otherwise indicated, the delay time measurements for each drive shall be calculated from signal conditions existing at that drive's own SCSI bus connection. Normally, these measurements need not consider delays in the cable.

Arbitration Delay (2.2 μsec. min., no max.): The minimum time that a device will wait from asserting BSY for arbitration until the data bus can be examined for an arbitration win.

Assertion Period (90 nsec. min.): The minimum time that a Target will assert REQ while using synchronous data transfers. Also, the minimum time that an Initiator will assert ACK while using synchronous data transfers.

Bus Clear Delay (800 nsec. max.): The maximum time for a device to stop driving all bus signals after:

1. BUS FREE phase is detected (BSY and SEL both false for a Bus Settle Delay)
2. Select is received from another drive during Arbitration phase.

Note: For the first condition above, the maximum time for a device to clear the bus is 1200 nsec. from BSY and SEL first becoming false. If a device requires more than a Bus Settle Delay to detect Bus Free, it shall clear the bus within a Bus Clear Delay minus the excess time.

Bus Free Delay (400 nsec. min.†): The minimum time that a device will wait for its detection of the Bus Free phase (BSY and SEL both false for a Bus Settle Delay) until its assertion of BSY when going to the Arbitration phase.

Bus Set Delay (1.8 μsec. max.): The maximum time for a device to assert BSY and its SCSI ID bit on the data bus after it detects Bus Free phase (BSY and SEL both false for a Bus Settle Delay) for the purpose of entering Arbitration phase.

Bus Settle Delay (400 nsec.): The time to wait for the bus to settle after changing certain control signals.

Cable Skew Delay (10 nsec. max.): The maximum difference in propagation time allowed between any two SCSI bus signals when measured between any two devices.

Data Release Delay (400 nsec. max.): The maximum time for an Initiator to release the data bus signals following the transition of the I/O signal from false to true.

Deskew Delay (45 nsec. min.): The minimum time required for deskew of certain signals.

Reset Hold Time (25 μsec. min., no max.) : The minimum time for which RST is asserted.

Selection Abort Time (200 μsec. max.): The maximum time that a Target/Initiator will take from its most recent detection of SEL or reselect until asserting a BSY response. This timeout is required to ensure that a Target/Initiator does not assert BSY after a selection/reselection phase has been aborted. This is not the selection timeout period.

Selection Timeout Delay (250 msec. min., recommended): The minimum time that an Initiator/Target should wait for a BSY response during the selection/reselection phase before starting the timeout procedure.

† Timing meets ANSI X3T.2, Rev. 10

3.2 LOGICAL CHARACTERISTICS

3.2.1 SCSI BUS PHASES

The SCSI architecture includes eight distinct phases:

1. Bus Free phase
2. Arbitration phase
3. Selection phase
4. Reselection phase
5. Command phase

†6. Data phase
†7. Status phase
†8. Message phase

† These phases are collectively termed the information transfer phases.

The SCSI bus can never be in more than one phase at any given time. Unless otherwise noted, signals that are not mentioned shall not be asserted.

3.2.1.1 BUS FREE PHASE

This phase indicates that no SCSI device is actively using the bus and that it is available for subsequent users.

SCSI devices will detect the Bus Free phase after SEL and BSY are both false for at least a Bus Settle delay.

SCSI devices must release all bus signals within a Bus Clear delay after BSY and SEL are continuously false for a Bus Settle delay. If a device requires more than a Bus Settle delay to detect the Bus Free phase, it must release all SCSI bus signals within a Bus Clear delay minus the excess time to detect the Bus Free phase. The total time to clear the bus must not exceed a Bus Settle delay plus a Bus Clear delay.

3.2.1.2 ARBITRATION PHASE

This phase allows one SCSI device to gain control of the bus so that it can assume the role of an Initiator or Target. The procedure by which a SCSI device gains control of the bus is as follows:

1. The device must first wait for the Bus Free phase to occur. The Bus Free phase is detected whenever both BSY and SEL are simultaneously and continuously false for a minimum of a Bus Settle delay.
2. The device must wait a minimum of a Bus Free delay after detection of the Bus Free phase (i.e., after BSY and SEL are both false for a Bus Settle delay) before driving any signal.
3. Following the Bus Free delay in Step (2), the device may arbitrate for the SCSI Bus by asserting BSY and its own SCSI ID , however the device must not arbitrate (i.e., assert BSY and its SCSI ID) if more than a Bus Set delay has passed since the Bus Free phase was last observed.
4. After waiting at least an Arbitration delay (measured from its assertion of BSY) the device must examine the data bus. If a higher priority SCSI ID bit is true on the data bus (DB 7 is the highest), then the device has lost the Arbitration and the device may release its signals and return to Step (1).

   If no higher priority SCSI ID bit is true on the data bus, the the device has won the Arbitration and it must assert SEL. Any other device that is participating in the Arbitration phase has lost the Arbitration and must release BSY and its SCSI ID bit within a BusClear delay after SEL becomes true. A device that loses Arbitration may return to Step (1).

5. The device that wins Arbitration must wait at least a Bus Clear delay plus a Bus Settle delay after asserting SEL, before changing any signals.

Note: The SCSI ID bit is a single bit on the Data bus that corresponds to the device's unique SCSI address. All other seven Data bus bits will be released by the device.

3.2.1.3 SELECTION PHASE

This phase allows an Initiator to select a Target for the purpose of initiating some Target function (e.g., Read or Write Command). During the Selection phase the I/O signal must be negated so that this phase can be distinguished from the Reselection phase.

3.2.1.3.1 NONARBITRATING SYSTEMS †

In systems with the Arbitration phase not implemented, the Initiator must first detect the Bus Free phase and then wait a minimum of a Bus Clear delay. Then, except in certain single-Initiator environments with Initiators employing the single Initiator option (refer to *Section 1.2.1.3.4*), the Initiator shall assert the desired Target's SCSI ID and its own Initiator SCSI ID on the Data bus. After two Deskew delays the Initiator must assert SEL.

3.2.1.3.2 ARBITRATING SYSTEMS †

The device that won Arbitration has both BSY and SEL asserted and has delayed at least a Bus Clear delay plus a Bus Settle delay before ending the Arbitration phase. The device that won the arbitration becomes an Initiator by releasing I/O. The Initiator will set the Data bus to a value which is the OR of its SCSI ID and the Target's SCSI ID bit. The Initiator must then wait at least a Bus Settle delay before looking for a response from the Target.

† The ST225N is compatible with both arbitrating and nonarbitrating Initiators.

3.2.1.3.3 ALL SYSTEMS

In all systems, the Target must determine that it is selected when SEL and its SCSI ID bit are true and BSY and I/O are false for at least a Bus Settle delay. The Selected Target must then assert BSY within a Selection Abort time (of its most recent detection of being selected), which is required for correct operation of the timeout procedure. If more than two SCSI ID bits are on the Data bus, the Target will not respond to selection.

The Initiator will release SEL, and may change the Data bus, at least two Deskew delays after it detects that BSY is true.

3.2.1.3.4 SINGLE INITIATOR

Initiators that do not implement the Reselection phase and do not operate in the multiple-Initiator environment are alllowed to set only the Target's SCSI ID bit during the Selection phase. This makes it impossible for the Target to determine the Initiator's SCSI ID.

3.2.1.3.5 SELECTION TIMEOUT PROCEDURE

The recommended Selection Timeout procedure for clearing the SCSI Bus after the Initiator has waited a minimum of a Selection Timeout delay and there has been no BSY response from the Target is as follows.

The Initiator will continue asserting SEL and will release the Data bus. If the Initiator has not detected BSY to be true after at least a Selection Abort time plus two Deskew delays, it will release SEL allowing the SCSI bus to go to the Bus Free phase. Devices must ensure that when responding to Selection, that selection was still valid within a Selection Abort time of their assertion of BSY.

Failure to comply with this requirement could result in an improper selection. For example, two Targets connected to the same Initiator, the wrong Target connected to an Initiator or a Target connected to a nonexistent Initiator.

3.2.1.4 RESELECTION PHASE

Reselection allows the Target to reconnect to an Initiator for the purpose of continuing some operation that was previously started by the Initiator, but was suspended by the Target, i.e., the Target disconnected by allowing a Bus Free phase to occur before the operation was complete. Reselection can only be used in systems that have the Arbitration phase implemented.

Upon completing the Arbitration phase, the winning device has both BSY and SEL asserted and has delayed at least a Bus Clear delay plus a Bus Settle delay. The winning device becomes a Target by asserting the I/O signal and setting the Data bus to a value that is the OR of its SCSI ID bit and the Initiator's SCSI ID bit. The Target must wait at least a Bus Settle delay before looking for a response from the Initiator.

The Initiator determines that it is selected when SEL, I/O and its SCSI ID bit are true and BSY is false for at least a Bus Settle delay. For correct operation of the timeout procedure; the reselected Initiator must assert BSY within a Selection Abort time of its detection of selection. If more than two SCSI ID bits are on the Data bus, the Initiator must not respond to a reselection.

After the Target detects BSY, it must also assert BSY and wait at least two Deskew delays and then release SEL. The Target may then change the I/O signal and the Data bus. The reselected Initiator will release BSY after it detects SEL false. The Target must continue asserting BSY until it is ready to relinquish the SCSI Bus.

3.2.1.4.1 RESELECTION TIMEOUT PROCEDURE

The Target will make a total of three attempts to reselect the Initiator. The following procedure is used to clear the SCSI bus after a reselection timeout.

The Target will continue asserting SEL and I/O and will release all Data bus signals. If the Target has not detected BSY to be true for at least a Selection Abort time plus two Deskew delays, the Target will release SEL and I/O allowing the SCSI bus to go to the Bus Free phase. Devices that respond to Reselection must ensure that the Reselection was still valid within a Selection Abort time of their assertion of BSY. Failure to comply with this requirement could result in an improper reselection, i.e., two Initiators connected to the same Target or the wrong Initiator connected to a Target.

3.2.1.4.2 INFORMATION TRANSFER PHASES

Command, Data and Message phases are all grouped together as the Information Transfer phases because they are all used to transfer data or control information via the Data bus.

The C/D, I/O and MSG signals are used to distinguish between the different information transfer phases. The Target drives these three signals and therefore controls all changes from one phase to another. The Initiator can request a Message Out phase by asserting ATN, while the Target can cause the Bus Free phase by releasing MSG, C/D, I/O and BSY.

Table 5: Information Transfer Phases

SIGNAL					
MSG	C/D	I/O	Phase Name	Direction of Transfer	Comment
0	0	0	DATA OUT	Initiator to target	Data Phase
0	0	1	DATA IN	Initiator from target	Data Phase
0	1	0	COMMAND	Initiator to target	
0	1	1	STATUS	Initiator from target	
1	0	0	*		
1	0	1	*		
1	1	0	MESSAGE OUT	Initiator to target	Message Phase
1	1	1	MESSAGE IN	Initiator from target	Message Phase

The Information Transfer phases use one or more REQ/ACK handshakes to control information transfer. Each REQ/ACK handshake allows the transfer of one byte of information. During the transfer BSY must remain true and SEL must remain false. Additionally, during the transfer, the Target must continuously envelope the REQ/ACK handshake(s) with C/D, I/O and MSG in such a manner that these control signals are valid for a Bus Settle delay before the assertion of REQ of the first handshake, and remain valid until the negation of ACK at the end of the last handshake.

3.2.1.4.3 ASYNCHRONOUS INFORMATION TRANSFER

The Target controls the direction of information transfer by means of the I/O signal. When I/O is true, information is transferred from the Target to the Initiator. When I/O is false, information is transferred from the Initiator to the Target.

If I/O is true (transfer to the Initiator), the Target must first drive DB(7-0) to their desired values, delay at least one Deskew delay plus a Cable Skew delay, then assert REQ. DB(7-0) must remain valid until ACK is true at the Target. The Initiator reads (DB 7-0) after REQ is true and then signals its acceptance of the data by asserting ACK. When ACK becomes true at the Target, the Target may change or release (DB 7-0) and then negate REQ. After REQ is false the Initiator must then negate ACK. After ACK is false the Target may continue the transfer by driving (DB (7-0) and asserting REQ, as described above.

If I/O is false (transfer to the Target) the Target requests information by asserting REQ. The Initiator then drives DB(7-0) to their desired values, delays at least one Deskew delay plus a Cable Skew delay and asserts ACK. The Initiator must continue to drive DB(7-0) until REQ is false. When ACK becomes true at the Target, the Target reads DB(7-0) and then negates REQ. When REQ becomes false at the Initiator, the Initiator may then change or release DB(7-0) and negate REQ.

3.2.1.5 COMMAND PHASE

The Command phase allows the Target to request command information from the Initiator.

The Target must assert the C/D signal and negate the I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

3.2.1.5.1 DATA PHASE

The term Data Phase encompasses both the Data In and Data Out phase.

3.2.1.5.2 DATA IN PHASE

The Data In phase allows the Target to request that data be sent to the Initiator.

3.2.1.5.3 DATA OUT PHASE

The Data out phase allows the Target to request that data be sent from the Initiator to the Target.

3.2.1.6 STATUS PHASE

The Status phase allows the Target to request that status information be sent from the Target to the Initiator.

The Target must assert C/D and I/O and negate the MSG signal during the REQ/ACK handshake of this phase.

3.2.1.7 MESSAGE PHASE

This refers to Message In/Out phase. The first byte transferred in either of these phases must be either a single-byte message or the first byte of a multiple-byte message. Multiple-byte messages must be wholly contained within a single message phase.

3.2.1.7.1 MESSAGE IN PHASE

This phase allows the Target to request that messages be sent to the Initiator.

The Target must assert C/D and I/O and negate the MSG signal during the REQ/ACK handshake of this phase.

3.2.1.7.2 MESSAGE OUT PHASE

This phase allows the Target to request that messages be sent from the Initiator to the Target. The Target may invoke this phase at its convenience in response to the Attention condition (refer to *Section 3.3*) created by the Initiator.

The Target must assert C/D and and negate I/O during the REQ/ACK handshake(s) of this phase. The Target shall handshake byte(s) in this phase until ATN goes false.

3.2.1.8 SIGNAL RESTRICTIONS BETWEEN PHASES

When the SCSI bus is between two information transfer phases, the following restrictions apply to the SCSI bus signals:

1. The BSY, SEL, REQ and ACK signals must not change.
2. The C/D, I/O, MSG and Data bus signals may change. When switching the Data bus direction from out to in (Target to Initiator), the Target must delay driving the Data Bus by at least a Data Release delay plus a Bus Settle delay after asserting the I/O signal and the Initiator must release the Data bus no later than a Data Release delay after I/O signal goes true. When switching the Data bus direction from in to out (Initiator to Target), the Target must release the Data bus no later than a Deskew delay after negating the I/O signal.
3. The ATN and RST signals may change as defined under the descriptions for the Attention (*3.3*) and Reset (*3.2.2*) conditions.

3.3 ATTENTION CONDITION

The Attention condition allows the Initiator to inform a Target that the Initiator has a message ready. The Target may access this message by performing a Message Out phase.

The Initiator creates the Attention condition by asserting ATN at any time, except during the Arbitration or Bus Free phases.

The Target may respond with the Message Out phase.

The Initiator may negate the ATN signal at any time, but it must not negate the ATN signal while the ACK signal is asserted during a Message Out phase. Normally, the Initiator negates ATN while REQ is true and ACK is false during the last REQ/ACK handshake of the Message Out phase.

3.3.1 RESET CONDITION

The Reset signal immediately clears all SCSI devices from the bus and take precedence over all other conditions and phases. Any SCSI device may may invoke the Reset condition by asserting RST for a minimum of a Reset Hold time. During Reset, the state of all other SCSI bus signals, other than RST, is not defined.

3.3.1.1 "HARD RESET" OPTION

The ST225N supports the "hard" RST option. Upon detection of a RST the drive will:

1. Clear all uncompleted commands
2. Release all SCSI device reservations
3. Return to normal operating mode

3.4 SCSI BUS PHASE SEQUENCES

The order in which phases are used on the SCSI bus follows a prescribed sequence. The RST condition can abort any phase and, in all systems, is always followed by the Bus Free phase. Also, any other phase can be followed by the Bus Free phase.

3.4.1 NONARBITRATING SYSTEMS

In systems where the Arbitration phase is not implemented, the permitted sequences are as illustrated in *Figure 7*. The normal progression is from Bus Free phase to Selection, and from Selection to one or more of the information transfer phases (Command, Data, Status or Message).

3.4.2 ARBITRATING SYSTEMS

In systems that implement Arbitration, the permitted sequences are as illustrated in *Figure 8*. The normal progression is from Bus Free phase to Arbitration, from Arbitration to Selection or Reselection, and from Selection or Reselection to one or more of the information transfer phases (Command, Data, Status or Message).

Figure 7: Phase Sequences Without Arbitration

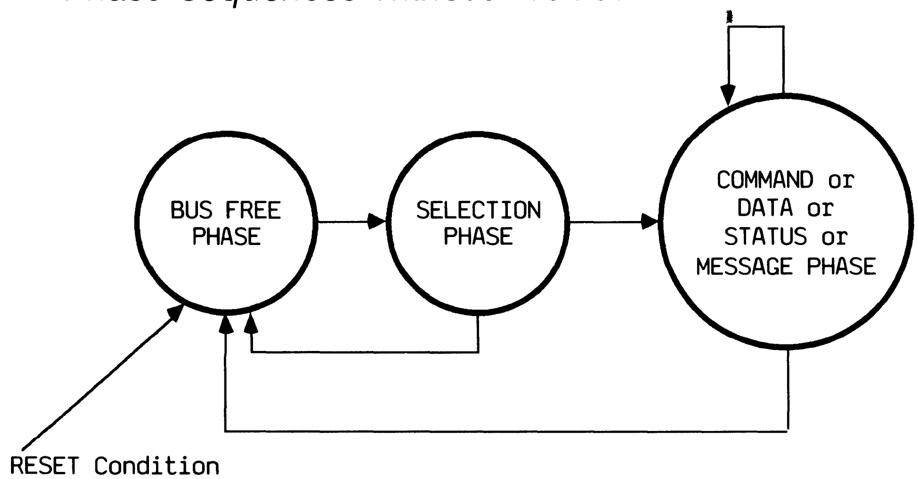
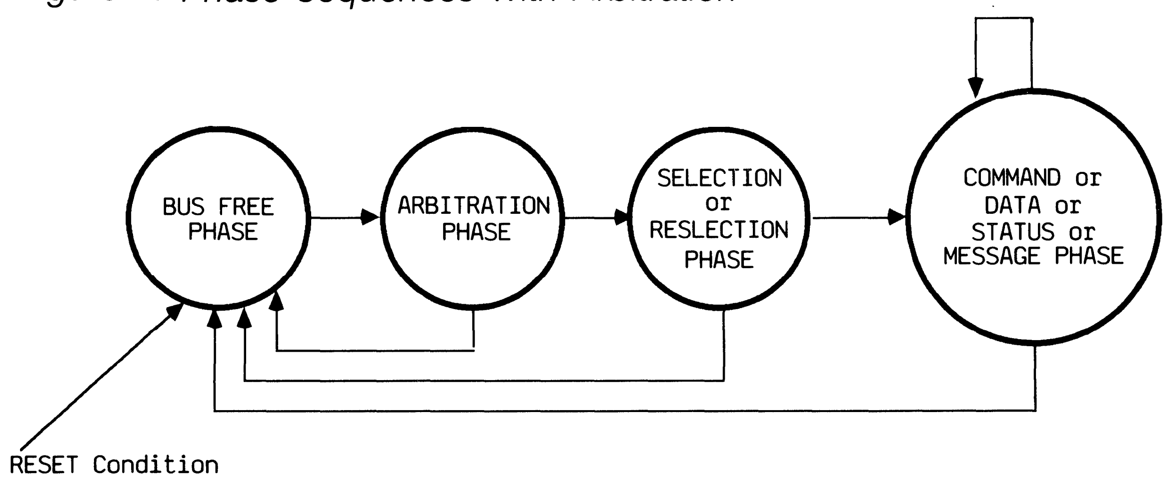


Figure 8: Phase Sequences With Arbitration



3.4.3 ALL SYSTEMS

There are no restrictions on the sequences between information transfer phases. A phase type may even be followed by the same phase type.

3.5 SCSI POINTERS

SCSI architecture provides for two sets of three pointers within each Initiator. The pointers reside in the Initiator path control. The first set of pointers are known as the current (active) pointers. These pointers represent the state of the interface and point to the next command, data or status byte to be transferred between the Initiator's memory and the Target. There is only one set of current pointers in each Initiator. The current pointers are used by the Target currently connected to the Initiator.

The second set of pointers are known as the saved pointers. There is one set of saved pointers for each command that is currently active (whether or not it is currently connected). The Saved Command pointer always points to the start of the Command Descriptor Block for the current command. The Saved Status pointer always points to the start of the status area for the current command. At the beginning of each command, the Saved Data pointer points to the start of the data area. It remains at this value until the Target sends a Save Data Pointer message to the Initiator. In response to this message, the Initiator stores the value of the current data pointer into the Saved Data Pointer. The Target may restore the current pointers to their saved values by sending a Restore Pointers message to the Initiator. The Initiator moves the saved value of each pointer into the corresponding current pointer. Whenever an SCSI device disconnects from the bus, only the saved pointer values are retained. The current pointer values are restored from the saved values upon the next reconnection.

3.6 MESSAGE SPECIFICATIONS

The message system allows communication between an Initiator and an ST225N for purposes of physical path management. The following section defines messages supported by the ST225N.

3.6.1 MESSAGE SYSTEM

The ST225N supports the messages listed in *Table 6* These messages support such special functions as disconnect/reconnect and command-linking. The Initiator indicates that it can support more than the Command Complete message by creating the Attention condition prior to the bus state of SEL asserted and BSY deasserted in the Selection phase.

When the drive recognizes the Attention condition, it will request a message byte from the Initiator by executing a Message-Out information transfer. The outcoming Identify message indicates the disconnect/reconnect functions are supported by the Initiator.

The first message sent by the Initiator after the Selection phase must be the Identify message. This permits the establishment of the physical path for a particular logical unit specified by the Initiator. After the Reselection phase, the Target's first message must be Identify. This allows the physical path to be reestablished for the Target's specified logical unit number. Under some exceptional conditions, an Initiator may send the Abort message or the Bus Device Reset message instead of the Identify message, as the first message. Only one logical unit number may be identified for any one selection sequence. A second Identify message (with a new logical unit number) must not be issued before the SCSI Bus has been released (Bus Free phase).

Whenever a physical path is established in an Initiator that can accomodate disconnection and reconnection, the Initiator must ensure that the active pointers of the physical path are equal to the saved pointers for that particular logical unit number. An implied Restore Pointers operation occurs as a result of connect or reconnect.

When the drive recognizes the Attention condition, it will request a message byte from the Initiator by executing a Message-Out information transfer.

Table 6 Message Codes

Code	Type	Description	Direction
00_H	S	Command Complete	In
04_H	O	Disconnect	In
05_H	O	Initiator Detected Error	Out
06_H	O	Abort	Out
07_H	O	Message Reject	In Out
08_H	O	No Operation	Out
$0A_H$	O	Linked Command Complete	In
$0B_H$	O	Linked Cmd. Cmplt. (With Flag)	In
$0C_H$	O	Bus Device Reset	Out
80_H-FE_H	O	Identify	In Out

3.6.2 MESSAGES

Single-byte messages are listed below.

COMMAND COMPLETE 00_H (Required): Sent from a Target to an Initiator to indicate that the execution of a command, or series of linked-commands, has terminated and that valid status has been sent to the Initiator. After successfully sending this message, the Target shall go to the Bus Free phase.

This command may have been executed successfully or unsuccessfully as indicated in the status.

SAVE DATA POINTER 02_H (Not used on the ST225): This message is sent from the Target to direct the Initiator to save a copy of the presently active data pointer for the currently attached LU.

RESTORE POINTERS 03_H (Not used on the ST225): This message is sent from a Target to direct the initiator to restore the most recently saved pointers (for the currently attached LU) to the active state.

DISCONNECT 04_H: Sent from a Target to inform an Initiator that the present physical path is going to be broken (the Target will disconnect by releasing BSY), but that a later reconnect will be required in order to complete the current operation.

ABORT 06_H: The message is sent from the Initiator to the Target to clear the present operation. All pending data and status for the issuing Initiator shall be cleared and the Target will got to the Bus Free phase. No status or ending message will be sent for the operation.

MESSAGE REJECT 07_H: This message is sent from either the Initiator or Target to indicate that the last message received was inappropriate or has not been implemented.

NO OPERATION 08_H: No operation.

LINKED-COMMAND COMPLETE $0A_H$: Sent from a Target to an Initiator to indicate that the execution of a linked-command has completed and that status has been sent.

LINKED-COMMAND COMPLETE (With Flag) $0B_H$: Sent from a Target to an Initiator to indicate that the execution of a linked-command (with the Flag set) has completed and status has been sent.

BUS DEVICE RESET $0C_H$: This message can be sent from an Initiator to direct a Target to reset all current commands. This message forces the ST225N to an initial state with no operations pending for any Initiator. Upon recognizing this message, the drive will go to the Bus Free phase.

IDENTIFY 80_H To FF_H (Optional): This message can be sent by either the Initiator or Target. It is used to establish the physical path connection between an Initiator and Target. When sent from a Target to an Initiator during reconnection, an implied Restore Pointers message must be performed by the Initiator prior to completion of this message.

Bit-7: This bit is always set to distinguish this message from the others.

Bit-6: This bit is only set by the Initiator. When it is set, it indicates that the Initiator has the ability to accommodate disconnection and reconnection.

Bits 5-3: Reserved.

Bits 2-0: These bits specify a Logical Unit Number (LUN), and must be zero.

3.7 COMPLETION STATUS

Completion Status is sent from the Target to the Initiator at the termination of a command set.

Table 7: Completion Status Byte

BIT / BYTE	7	6	5	4	3	2	1	0
0	RESERVED			Status Byte Code				(0)

Table 8: Completion Status Byte Code Bit Values

BITS OF STATUS BYTE								STATUS REPRESENTED
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Good Status
0	0	0	0	0	0	1	0	Check Condition
0	0	0	0	1	0	0	0	Busy
0	0	0	1	0	0	0	0	Intermediate Status/Good Status
0	0	0	1	1	0	0	0	Reservation Conflict

GOOD STATUS: This status indicates that the ST225N has sucessfully completed the command.

CHECK CONDITION: Any error, exception or abnormal condition which causes sense information to be set, shall cause CHECK CONDITION status. The Request Sense Command should be issued following CHECK CONDITION status, to determine the nature of the condition.

BUSY: The ST225N is busy. This status will be sent whenever the ST225N is unable to accept a command from an Initiator.

INTERMEDIATE STATUS SENT: This status is sent for every command in a series of linked-commands (except for the last command), unless an error, exception or abnormal condition causes CHECK CONDITION status to be sent. If this status is not sent, the chain of linked-commands is broken and no further commands in the series will be executed.

RESERVATION CONFLICT: This status is returned whenever an SCSI device attempts to access a logical unit or extent within the logical unit that is reserved to another SCSI device.

3.8 SCSI COMMANDS

This section defines the SCSI command structure and gives several examples.

The command definitions assume a data structure which provides the appearance at the interface of a contiguous set of logical block of a fixed or explicitly defined data length. The SCSI device maps the physical characteristics of the attached peripheral devices to one of the several logical structures defined by the device type code.

A single command may transfer one or more logical blocks of data. Multiple commands may be linked if they are sent to the same logical unit. A Target may disconnect from the SCSI bus to allow activity by the other SCSI devices while it is being prepared to transfer data.

Upon command completion (successful or unsuccessful), the Target returns a status byte to the Initiator. Since most error and exception conditions cannot be adequately described with a single status byte, one status code (Check Condition) indicates that additional information is available. The Initiator may issue a Request Sense command to retrieve this additional information.

3.8.1 COMMAND IMPLEMENTATION REQUIREMENTS

The first byte of any SCSI command must contain an operation code as defined in this manual. Three bits (bits 7-5) of the second byte of each SCSI command specify the logical unit if it is not specified using the Identify message. The last byte of all SCSI commands must contain a control byte as defined in *Section 3.8.2.6.*

3.8.1.1 RESERVED

Reserved bits, bytes, fields and code values are set aside for future standardization. A reserved bit, field or byte must be set to zero. A Target which receives a reserved bit, field or byte that is not zero, or a reserved code value must terminate the command with a Check Condition status. If Extended Sense is implemented, the Sense key must be set to Illegal Request.

3.8.2 COMMAND DESCRIPTOR BLOCK

A request to a peripheral device is performed by sending a Command Descriptor Block to the Target. For several commands, the request is accompanied by a list of parameters sent during the Data-Out phase.

The Command Descriptor Block always has an operation code as the first byte of the command, followed by a logical unit number, command parameters (if any) and a control byte.

If there is an invalid parameter in the Command Descriptor Block of any command, the ST225N will terminate the command without altering the medium.

3.8.2.1 OPERATION CODE

The operation code of the Command Descriptor Block has a group code field and a command code field. The three-bit group code field provides for eight groups of command codes. The five-bit command code field provides for thirty-two command codes in each group for a total of 256 possible operation codes.

The group code specifies one of the following groups: Group 0: six-byte commands (see *Table 10*) Group 1: ten-byte commands (see *Table 11*) Group 2: Reserved (not supported) Group 3: Reserved (not supported) Group 4: Reserved (not supported) Group 5: twelve-byte commands (not supported) Group 6: vendor-unique (not supported) Group 7: vendor-unique (not supported)

Table 9: Operation Code

BIT / BYTE	7	6	5	4	3	2	1	0
0	Group Code			Command Code				

Table 10: Typical Command Descriptor Block For Six-Byte Commands

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			Logical Block Address (if required) (MSB)				
2	Logical Block Address (if required)							
3	Logical Block Address (if required) (LSB)							
4	Transfer Length (if required)							
5	Control Byte							

Table 11: Typical Command Descriptor Block For Ten-Byte Commands

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				RELADR
2	Logical Block Address (if required) (MSB)							
3	Logical Block Address (if required)							
4	Logical Block Address (if required)							
5	Logical Block Address (if required) (LSB)							
6	RESERVED							
7	Transfer Length (if required) (MSB)							
8	Transfer Length (if required) (LSB)							
9	Control Byte							

3.8.2.2 LOGICAL UNIT NUMBER (LUN)

The LUN must be zero for the ST225N.

3.8.2.3 LOGICAL BLOCK ADDRESSES

The logical block address on logical units must begin with block zero and be contiguous up to the last logical block on that logical unit.

Group 0 command descriptor blocks contain 21-bit logical addresses. Group 1 command descriptor blocks contain 32-bit logical block addresses.

The logical block concept implies that the Initiator and Target have previously established the number of data bytes per logical block.

3.8.2.4 RELATIVE ADDRESS BIT

The Relative Address bit (RELADR) is not supported.

3.8.2.5 TRANSFER LENGTH

The transfer length specifies the amount of data to be transferred, usually the number of blocks. For several commands the transfer length indicates the requested number of bytes to be sent as defined in the command description. For these commands the transfer length field may be identified by a different name.

Commands that use one byte for transfer length allow up to 256 blocks of data to be transferred by one command. A transfer length of 1 to 255 indicates the number of blocks that will be transferred. A value of zero indicates 256 blocks.

Commands that use two bytes for transfer length allow up to 65,535 blocks of data to be transferred by one command. In this case, a transfer length of zero indicates that no data transfer will take place. A value of 1 to 65,535 indicates the number of blocks that will be transferred.

For several commands, more than two bytes are allocated for transfer length. Refer to the specific command description for further information.

The transfer length of the commands that are used to send a list of parameters to a Target is called the parameter list length. The parameter list length specifies the number of bytes sent during the Data-Out phase.

The transfer length of the commands that are used to return Sense Data (e.g., Request Sense, Inquiry, Mode Sense, etc.) to an Initiator is called the allocation length. The allocation length specifies the number of bytes that an Initiator has allocated for returned data. The Target must terminate the Data-In phase when the allocation length bytes have been transferred or when all available sense data have been returned to the Initiator, whichever is less.

3.8.2.6 CONTROL BYTE

The control byte is the last byte of every command descriptor block. *Table 12* describes a typical control byte.

Table 12: Control Byte

BIT / BYTE	7	6	5	4	3	2	1	0
Last	Vendor Unique		RESERVED				Flag	Link

BIT	DESCRIPTION
7-6	Vendor Unique - Must be zero for ST225N
5-2	RESERVED
1	Flag bit - if the link bit is zero, then the flag bit will be set to zero. If the link bit is one, and if the command terminates successfully, the Target will send LINKED COMMAND COMPLETE message if the flag bit is zero and will send LINKED COMMAND COMPLETE (WITH FLAG) message if the flag bit is one. Typically, this bit is used to cause an interrupt in the Initiator between linked commands.
0	Link bit - This bit is set to one to indicate that the Initiator desires an automatic link to the next command upon successful completion of the current command. If the link bit is one, Targets that implement linked commands(upon successful termination of the command) will return INTERMEDIATE status and will then send one of the two messages defined by the flag bit (above).

3.8.3 COMMAND EXAMPLES

3.8.3.1 SINGLE COMMAND EXAMPLE

A typical operation on the SCSI bus is likely to include a single Read command to a peripheral device. This operation is described in detail with a request from the Initiator. This example assumes that no linked commands, malfunctions or errors occur.

The Initiator has active pointers and a set of stored pointers representing active disconnected SCSI devices (an Initiator without disconnect capability does not require stored pointers). The Initiator sets up the active pointers for the operation requested, arbitrates for the SCSI bus and selects the Target. Once this process is completed, the Target assumes control of the operation.

Using a Read command as an example; the Target receives the command from the Initiator, interprets and executes it. The Target, in this case, gets data from the peripheral device and sends it to the Initiator. To end the operation, the Target sends a Command Complete message to the Initiator.

3.8.3.2 DISCONNECT EXAMPLE

In the above single command example, the length of time necessary to obtain the data may require a time consuming physical seek. In order to improve the system throughput, the Target may disconnect from the Initiator, freeing the SCSI bus to allow other requests to be sent to other logical units. To do this, the Initiator needs to be reselectable and capable of restoring the pointers upon reselection. The Target needs to be capable of arbitrating for the SCSI bus and reselecting the Initiator.

After the Target has received the Read command and has determined that there will be a delay, it disconnects by releasing BSY.

When the data are ready to be transferred, the target reconnects to the Initiator. As a result of this reconnection, the Initiator restores the pointers to their most recently saved values (which, in this case, are the initial values) and the Target continues, as in the single command example, to finish the operation. The Initiator recognizes that the operation is complete when the Command Complete message is received.

3.8.3.3 LINKED COMMAND EXAMPLE

The ST225N will accept linked command blocks from the host. It will then execute this "chain" without further system intervention.

When the Link bit is set the drive will request the next command block immediately upon presentation of the Command Complete message. Execution of linked commands is identical to commands issued separately, except that the drive will request the next command block without going through either Bus Free phase or the Selection phase.

Upon completion of a linked command, a Linked Command Complete message is sent from the drive to the Initiator. The Initiator must then set up the internal pointers for the next command chain.

Table 13: Command Summary

Operation Code	Type	Description
00_H	O	Test Unit Ready
1_H	O	Rezero Unit
3_H	O	Request Sense
4_H	S/E	Format Unit
7_H	O	Reassign Blocks
8_H	S	Read
A_H	S	Write
B_H	O	Seek
11_H	V	Read Usage Counter
12_H	E	Inquiry
15_H	O	Mode Select
16_H	O	Reserve
17_H	O	Release
$1A_H$	O	Mode Sense
$1B_H$	O	Start/Stop
$1C_H$	O	Receive Diganostic Results
$1D_H$	O	Send Diagnostic
25_H	E	Read Capacity
28_H	E	Read
$2A_H$	E	Write
37_H	O	Read Defect Data

4.1 TEST UNIT READY COMMAND

Peripheral Device Type: All
Operation Code Type: Optional
Operation Code: 00_H

Table 14: Test Unit Ready Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED							
3	RESERVED							
4	RESERVED							
5	RESERVED						Flag	Link

The Test Unit Ready Command provides a means to check if the drive is ready. This is not a request for a self-test. If the drive is ready, the command is terminated with Good Status, and the sense key is set to No Sense. Sense keys are valid only if Extended Sense is requested.

4.2 REZERO UNIT COMMAND

Peripheral Device Type: All
Operation Code Type: Standard
Operation Code: 01_H

Table 15: Rezero Unit Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED							
3	RESERVED							
4	RESERVED							
5	RESERVED						Flag	Link

The Rezero Unit Command requests that the Target set the drive to Track Ø.

4.3 REQUEST SENSE COMMAND

Peripheral Device Type: All
Operation Code Type: Standard
Operation Code: 03_H

The Request Sense Command requests that the Target transfer Sense data to the Initiator. Extended Sense is supported and will be provided if the Allocation Length is set to 5 or greater. When the Allocation Length is set to a value of 0-4 bytes, then Nonextended Sense will be generated.

The Sense data is valid for a Check Condition Status returned on the prior command. This sense data is preserved for the Initiator until retrieved by the Request Sense command, or until receipt of the next command from the Initiator. Sense shall be cleared upon receipt of any subsequent command to the drive from the Initiator receiving the Check Condition Status.

The Allocation Length specifies the number of bytes that the Initiator has allocated for returned sense data. An Allocation Length of less than five indicates that four bytes of Sense data will be transferred. Any other value indicates the number of bytes to be transferred. The ST225N will terminate the data-in phase when the Allocation Length bytes have been transferred or when all available Sense data has been transferred to the Initiator.

Maximum Sense length is 22 bytes for Extended Sense or 27 bytes when the Usage Counters are returned. The Check Condition Status is used only to report fatal errors for this command. For example:

- The Target receives a non-zero reserved bit in the Command Descriptor Block.
- An unrecovered parity error occurs on the data bus.
- A Target malfunction prevents return of the sense data.

Following a fatal error on a Request Sense Command, sense data may be invalid. Refer to *Section 5.0* for Error Codes and Sense Keys.

Table 16: Request Sense Command

BIT BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED							
3	RESERVED							
4	Allocation Length							
5	RESERVED						Flag	Link

4.3.1 NONEXTENDED SENSE

Nonextended Sense is provided for compatibility with systems that do not accept Extended Sense.

Table 17: Nonextended Sense Data Format

BIT BYTE	7	6	5	4	3	2	1	0
0	ADVALID	Error Class			Error Code			
1	Logical Block Address (MSB)							
2	Logical Block Address							
3	Logical Block Address (LSB)							

The Address Valid (ADVALID) bit indicates that the Logical Block Address bytes contain valid information related to the error code.

The error class specifies a class of errors from zero through two. The error class, together with the error code form a sense code, which is analogous to a particular sense key.

4.3.2 EXTENDED SENSE

Error class seven specifies Extended Sense. Error code zero specifies the Extended Sense data format. Error codes 1_H through F_H are reserved.

Table 18: Extended Sense Data Format

BIT BYTE	7	6	5	4	3	2	1	0
0	Valid	Error Class			Error Code			
1	RESERVED							
2	RESERVED				Sense Key			
3	Logical Block Address (MSB)							
4	Logical Block Address							
5	Logical Block Address							
6	Logical Block Address (LSB)							
7	Additional Sense Length							

Additional Sense Bytes

8	RESERVED
9	RESERVED
10	RESERVED
11	RESERVED
12	Additional Sense Code
13	RESERVED
14	RESERVED
15	RESERVED
16	RESERVED
17	RESERVED
18	Cylinder (MSB)
19	Cylinder (LSB)
20	Head
21	Sector

The Valid bit indicates that the information bytes specify the unsigned Logical Block Address associated with the Sense key. Sense keys are described in *Section 5.0.*

The Additional Sense bytes contain the Error Class and Error Code which would have been presented for Nonextended Sense and the Physical Address which corresponds with the Logical Block Address.

On Overflow of Usage Counter error, the additional bytes will contain the alternate Error Code and the nine Usage Counter bytes for an Additional Sense Length of nineteen.

Additional Sense Bytes For Usage Counters

18	Blocks Read (MSB)
19	Blocks Read (MSB)
20	Blocks Read (LSB)
21	Seeks (MSB)
22	Seeks (MSB)
23	Seeks (LSB)
24	Uncorrectable Read Errors
25	Correctable Read Errors
26	Seek Errors

4.4 FORMAT UNIT COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Standard
Operation Code: 04_H

Table 19: Format Unit Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			FMTDATA	CMPLST	Defect List Format		
2	VENDOR UNIQUE							
3	Interleave (MSB)							
4	Interleave (LSB)							
5	RESERVED						Flag	Link

The Format Command will write from Index to Index all ID and data fields with the format specified by a previous Mode Select Command. If no Mode Select Command has been executed, the previous format will be used. On unformatted discs, the default format of 512-byte sectors and a 1:1 interleave will be used. The ST225N provides a manufacturer's defect list written on the drive that is used during the format operation to bypass defects which were identified during the manufacturing process. Additional defects may be added to the manufacturer's defect list. These defects are supplied as data to the Format Command. The Interleave Field requests that the logical blocks be related in a specific fashion to the physical blocks to facilitate speed matching. An interleave value of zero requests that the Target use its default interleave (1:1). An interleave value of one requests that consecutive logical blocks be placed in physical consecutive order.

All valid interleave values, including 1:1 are supported by this product. Valid interleave values are from 0 to sectors/track minus 1, i.e., for 17 sectors/track, the valid interleave values are from 0 to 16.

Three format modes are supported by the ST225N.

- Format with known defect list (original manfacturer's defect list plus any previously supplied additions)
- Format with known defect list plus supplied defects in Logical Block Format
- Format with original manufacturer's defect list only (remove any previously supplied additions)

The Format Data (FMTDATA) bit, if one, indicates that format data is supplied during the data-out phase. The defect list included with this data specfies the defects which are to be entered onto the defect map. The FMTDATA bit, if zero, indicates that the data-out phase will not occur and no defect data will be supplied by the Initiator.

The Complete List (CMPLST) bit, if one, indicates use only original manufacturers list.

The CMPLST Bit, if zero, indicates the data supplied is in addition to existing defect data using the current format.

Note: When the physical block size is changed, no attempt will be made to map defects supplied in Logical Block format to a new record size. Any supplied defect list is assumed to be for the requested block size. If an interleave value is changed and new defects are added, then the previous interleave value will be used to physically locate defects.

Table 20: Format Command Variations

BIT REFERENCE: Format Data	Complete List	Defect List			Command Type	Comments
0	X	X	X	X	Standard	Format with known defect list. No defect data sent from Initiator to Target.
1	0	0	X	X	Extended	Format adding defects specified in defect list to known defects. See Defect List Table (Block Format).
1	1	0	X	X	Optional	Format using manufacturers defect list only. Defect list length must be set to zero.

Table 21: Defect List—Block Format

BYTE	
0	RESERVED
1	RESERVED
2	Defect List Length (MSB)
3	Defect List Length (LSB)

Defect Descriptors

0	Defect Block Address (MSB)
1	Defect Block Address
2	Defect Block Address
3	Defect Block Address (LSB)

The Defect List contains a four-byte header followed by one or more Defect Descriptors. The length of the Defect Descriptor is four bytes. The Defect List length specifies the length in bytes of the Defect Descriptors that follow. The Defect List length is equal to four times the number of Defect Descriptors.

The Defect Descriptor for the block format specifies a four-byte defect block address which contains the defect. The Defect Descriptors must be in ascending order.

A maximum of 95 total defects (manufacturer's list plus host defects) can be formatted. The total number of defects and reassigned blocks can not exceed 100.

4.5 REASSIGN BLOCKS COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Optional
Operation Code: 07_H

This command requests that the Target reassign the defective Logical Blocks to an area on the drive reserved for this purpose.

The Initiator transfers a defect list that contains the Logical Block Addresses to be reassigned. The Target will reassign the physical medium used for each Logical Block address in the list. The data contained in the logical blocks specified in the defect list will be lost.

If the drive has insufficient capacity to reassign all of the defective logical blocks, the command will terminate with a CHECK CONDITION status and the Sense key shall be set to Medium Error. The logical block address of the last Logical Block reassigned will be returned in the information bytes of the Sense data. A maximum of 18 blocks may be reassigned at any time.

The Reassign Blocks defect list contains a four-byte header followed by one or more defect descriptors. The length of each Defect Descriptor is four bytes.

The Defect List length specifies the total length in bytes of the Defect Descriptors that follow. The Defect List length is equal to four times the number of Defect Descriptors.

Table 22: Reassign Blocks Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED							
3	RESERVED							
4	RESERVED							
5	RESERVED						Flag	Link

Blocks that have been reassigned by this command will be added to the "Known Defect List." These defective sectors will then be spared by the normal defect management method by the next Format Command.

Table 23: Reassign Blocks Defect List

BYTE	Defect List Header
0	RESERVED
1	RESERVED
2	Defect List Length (MSB)
3	Defect List Length (LSB)

Defect Descriptors

0	Defect Logical Block Address (MSB)
1	Defect Logical Block Address
2	Defect Logical Block Address
3	Defect Logical Block Address (LSB)

The Defect Descriptor specifies a four-byte defect Logical Block Address that contains the defect. The Defect Descriptors must be in ascending order.

4.6 READ COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Standard
Operation Code: 08_H

Table 24: Read Command

BIT BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	RESERVED						Flag	Link

The Read Command requests that the Target transfer data to the Initiator. The Logical Block Address specifies the logical block where the Read operation shall begin.

The Transfer Length specifies the number of contiguous logical blocks of data to be transferred. A Transfer Length of zero indicates 256 logical blocks shall be transferred. Any other value indicates the number of blocks to be transferred.

4.7 WRITE COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Standard
Operation Code: $0A_H$

Table 25: Write Command

BIT BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	RESERVED						Flag	Link

The Write Command requests that the Target write the data transferred by the Initiator to the medium.

The Logical Block Address specifies the logical block where the Write operation shall begin.

The Transfer Length specifies the number of contiguous logical blocks of data to be transferred. A Transfer Length of zero indicates 256 logical blocks shall be transferred. Any other value indicates *that* number of logical blocks shall be transferred.

4.8 SEEK COMMAND

Peripheral Device Type: Direct Access
Operaiton Code Type: Optional
Operation Code: $0B_H$

Table 26: Seek Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	RESERVED							
5	RESERVED						Flag	Link

This command requests that the drive seek to the specified Logical Block Address.

4.9 READ USAGE COUNTERS COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Optional
Operation Code: 11_H

The Read Usage Counters Command is provided for tracking the number of blocks read, the number of seeks requiring carriage motion, the number of correctable/uncorrectable Read errors and the number of seek errors. Execution of this command will set the usage counters to zero.

Note: The counter information is stored in RAM and may be lost when power is removed.

When the usage or error counters overflow, an error will be generated on the next command, indicating to the host that this has occured and the counters will be contained in the Sense information. After the sense information has been retrieved, the usage counters will be reset.

The Mode Select Command is used to enable or disable the counter overflow error. the default is set so error generation is disabled (see Mode Select).

Table 27: Read Usage Counters Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED							
3	RESERVED							
4	RESERVED							
5	RESERVED						Flag	Link

Table 28: Usage Counter Format

0	Blocks Read (MSB)
1	Blocks Read
2	Blocks Read (LSB)
3	Seeks (MSB)
4	Seeks
5	Seeks (LSB)
6	Uncorrectable Read Errors
7	Correctable Read Errors
8	Seek Errors

4.10 INQUIRY COMMAND

Peripheral Device Type: All
Operation Code Type: Extended
Operation Code: 12_H

The Inquiry Command requests that information regarding parameters of the Target be sent to the Initiator.

The Allocation Length specifies the number of bytes that the Initiator has returned for Sense data. An Allocation Length of zero indicates that no inquiry data will be transferred. This is not considered an error condition. Any other value will indicate *that* number number of bytes to be transferred. The Target will terminate the data-in phase when Allocation Length bytes have been transferred or, when all available Inquiry data has been transferred to the Initiator. The Check Condition status is reported when the Target cannot return the Inquiry data.

The Inquiry data contains a five-byte header, followed by additional parameters, if any.

Table 29: Inquiry Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED							
3	RESERVED							
4	Allocation Length							
5	RESERVED						Flag	Link

Table 30: Inquiry Data

BIT / BYTE	7	6	5	4	3	2	1	0
0	Device Type Code (00)							
1	RMB (0)	Device Type Qualifier (00)						
2	Revision Level (01)							
3	Response Type SRD (00)							
4	Additional Length (39)							

Additional Bytes

5	RESERVED
6	RESERVED
7	RESERVED
8–15	SEAGATE (ASCII)
16–31	ST225N (ASCII)
32	Hardware Revision Level
33	Firmware Revision Level
34	ROM Revision Level
35	RESERVED

Command Set ID Bytes

36	Number of Extents (MSB)	(00)
37	Number of Extents (LSB)	(08)
38	Group 0 Commands	(00)
39	Commands (0-7)	(D9H)
40	Commands (8-F)	(B0H)
41	Commands (10-17)	(67H)
42	Commands (18-1F)	(3CH)
43	Group 1 Commands	(01)
44	Commands (20-27)	(04H)
45	Commands (28-2F)	(A0H)
46	Commands (30-37)	(01H)
47	Commands (38-3F)	(00H)
48	End of List	(FFH)

Number of Extents: The ST225N supports a total of eight extents. Refer to Reserve, Release.

Bytes 38 through 48 are a bit-significant list of the commands supported by the ST225N, i.e., Reassign Blocks (07) a Group Zero command, corresponds to bit 0 of byte 39 where bit 7 is MSB.

Vendor-Unique Parameters

49	DRIVE SERIAL NUMBER (MSB)
50	DRIVE SERIAL NUMBER
51	DRIVE SERIAL NUMBER
52	DRIVE SERIAL NUMBER
53	DRIVE SERIAL NUMBER
54	DRIVE SERIAL NUMBER
55	DRIVE SERIAL NUMBER
56	DRIVE SERIAL NUMBER
57	DRIVE SERIAL NUMBER (LSB)

The Removable Medium (RMB) bit is set to zero, indicating the medium is not removable.

The Device Type Qualifier is a seven-bit user specified code. This code may be set using the Mode Select Command. The default value is 0. The Revision Level is the implemented revision level of this standard and is defined as follows:

00_H	Revision Level is unspecified
01_H	First release. This should be used for disc drives that claim to comply with the ANSI standard.
02_H-FF_H	Reserved

The Additional Length specifies the length in bytes of additional drive parameters.

4.11 MODE SELECT COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Optional
Operation Code: 15_H

The Mode Select Command provides a means for the Initiator to specify or change operating parameters within the drive.

The parameter list length specifies the number of bytes of Mode Select data to be transferred during the Data-Out Phase. A parameter list length of zero indicates that no data is transferred.

The Mode Select parameter list contains a four-byte header followed by the block descriptor (if any), followed by zero or more page descriptors.

Table 31: Mode Select Command

BIT BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED							
3	RESERVED							
4	Parameter List Length							
5	RESERVED						Flag	Link

Table 32: Mode Select Header

BYTE	
0	RESERVED
1	Medium Type (00)
2	RESERVED
3	Block Descriptor Length (8)

Block Descriptors

0	Density Code (00)
1	Number of Blocks (MSB)
2	Number of Blocks
3	Number of Blocks (LSB)
4	RESERVED
5	Block Length (MSB)
6	Block Length
7	Block Length (LSB)

Page Descriptors

0	SDP	R	Page Code
1	Page Length (bytes)		
2	Refer to page definition		
n	Refer to page definition		

Each Page Descriptor supplies information regarding a particular class of functions. The page descriptors may be in any order and do not have to be supplied.

The SDP bit requests that the ST225N set the default parameters for this page. No page bytes need be sent when selecting default parameters.

The page length indicates the number of bytes to be associated with this page and may be zero.

Operating parameters format: Page Code 0_H

0	SDP	R	Page Code = 00h	
1	Page Length (02h)			
2	Usage	RECOVERY	Status	RESERVED
3	Device Type Qualifier			

Only one set of Mode Select parameters is kept for each drive.

Table 33: Page Codes

0_H	Operating Parameters
1_H	Error Recovery Parameters
2_H	Disconnection Parameters (default only)
3_H	Format Parameters (default only)
4_H	Geometry Parameters (default only)
5_H through $3F_H$	Reserved (ignored)

Only one set of Mode Select parameters is kept for each drive.

Usage specifies that upon overflow of the usage counters, an error be generated on the following command and that the usage counter data be saved in the sense information. Default (0) disables error presentation upon the overflow condition.

Recovery specifies that the ST225N report all errors without attempting error recovery, correction or retry operations. Default (0) enables all normal error recovery operations.

Status specifies that recovered error sense be reported in the event of a recoverable error, either by retry or correction. Default (0) disables recovered error sense. This bit is not applicable if retries are disabled by Recovery.

The device type qualifier may be set to further identify a device.

Page Code 01—Error Recovery parameters: This page is ignored—reported as all zeros.

Page Code 01—Disconnection parameters: This page is ignored—reported as all zeros.

Page Code 03—Format parameters: (sense only)

Page Code 04—Geometry parameters: (sense only)

Table 34: Direct Access Device Format Parameters

BIT / BYTE	7	6	5	4	3	2	1	0
0	SDP	Ø	Page Code - 3_H					
1	Page Length (in bytes)							

Handling of Defects Field

2	RESERVED
3	RESERVED
4	RESERVED
5	RESERVED
6	RESERVED
7	RESERVED
8	RESERVED
9	RESERVED

Track Format Field

10	Sectors per Track (MSB)
11	Sectors per Track (LSB)

Sector Format Fields

12	Bytes per Physical Sector (MSB)
13	Bytes per Physical Sector (LSB)
14	Interleave (MSB)
15	Interleave (LSB)
16	RESERVED
17	RESERVED
18	RESERVED
19	RESERVED

Drive Type Field

20	RESERVED
21	RESERVED
22	RESERVED
23	RESERVED

Sectors per Track: This indicates the number of physical sectors per disc track.

Bytes per Physical Sector: This indicates the number of bytes per physical sector.

Interleave: This is the same parameter passed in the Format Unit Command and is only returned by the Mode Select Command.

Table 35: Disc Drive Geometry Parameters. Page Code 4_H

BIT BYTE	7	6	5	4	3	2	1	0
0	SDP	R	Page Code – 4_H					
1	Page Length (in bytes)							
2	Number of Cylinders (MSB)							
3	Number of Cylinders							
4	Number of Cylinders (LSB)							
5	Number of Heads							
6	RESERVED							
7	RESERVED							
8	RESERVED							
9	RESERVED							
10	RESERVED							
11	RESERVED							
12	RESERVED							
13	RESERVED							
14	RESERVED							
15	RESERVED							
16	RESERVED							
17	RESERVED							

4.12 RESERVE COMMAND

Peripheral Device Type: Direct Access, Write-Once Read-Multiple, Read-Only Direct Access
Operation Code Type: Optional
Operation Code: 16_H

Table 36: Reserve Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			3rd PTY	Third Party Device ID			Extent
2	Reservation Identification							
3	Extent List Length (MSB)							
4	Extent List Length (LSB)							
5	RESERVED						Flag	Link

The Reserve command is used to reserve logical units or extents within logical units for the use of the Initiator. In the third-party reservation option the logical units or extents may be reserved for another specified SCSI device. The Reserve and Release commands provide the basic mechanism for contention resolution in multiple-initiator systems.

4.12.1 LOGICAL UNIT RESERVATION

If the extent bit is zero, this command requests that the entire logical unit be reserved for the exclusive use of the Initiator until the reservation is superceded by another valid Reserve command from the same Initiator or until released by a Release command from the same Initiator by the Send Diagnostic Self-Test, by a Bus Device Reset message from any Initiator, or by a "hard" Reset condition. A logical unit reservation will not be granted if the logical unit or any extent is reserved by another Initiator. It is permissible for an Initiator to reserve a logical unit that is currently reserved by that Initiator. If the extent bit is zero, the reservation identification and the extent list length are ignored.

If the logical unit, or any extent within the logical unit is reserved for another Initiator, the Target will respond by returning Reservation Conflict status.

If, after honoring the reservation, any other Initiator then subsequently attempts to perform any command on the reserved logical unit then the command is rejected with Reservation Conflict status.

4.12.2 EXTENT RESERVATION

The reservation identification provides a means for an Initiator to identify each extent reservation. This allows an Initiator in a multiple tasking environment, to have multiple reservations outstanding. The reservation identification is used in the Release command to specify which reservation is to be released. It is also used in superceding Reserve commands to specify which reservation is to be superceded.

If the extent bit is one then the Target processes the reservation request as follows:

1. The extent list is checked for the number of extents in the reservation request. If the extent list length is zero, no reservations shall be changed and this condition is not treated as an error. If the extent list contains more extents than are supported on the logical unit, the command is terminated with

Check Condition status and the sense key is set to Illegal Request. If the extent list contains more extents than are currently available on the logical unit (total of eight), then the target will return Reservation Conflict status.

2. The extent list is checked for valid extent logical block addresses. If any logical block address is invalid for this logical unit, the command is terminated with Check Condition status and the sense key is set to Illegal Request. The extent list is checked for conflicting extent overlaps and if overlaps are found, the command is terminated with Check Condition status and the sense key is set to Illegal Request.
3. If the requested reservation does not conflict with any active or previously requested reservation, the extents specified are reserved until superceded by another valid Reserve command from the same Initiator or until released by a Release command from the same Initiator, by a Bus Device Reset message from any Initiator, by a Send Diagnostic Self-Test command, or by a "hard" Reset condition. If either of the last two conditions occur, the next command from each Initiator is terminated with Check Condition status and the sense key is set to Unit Attention.
4. If the reservation request conflicts with a reservation already active or a reservation request that is already queued, then the Target will return Reservation Conflict status.

Table 37: Data Format of Extent Descriptions

BIT BYTE	7	6	5	4	3	2	1	0
0	RESERVED						Reservation Type	
1	Number of Blocks (MSB)							
2	Number of Blocks							
3	Number of Blocks (LSB)							
4	Logical Block Address (MSB)							
5	Logical Block Address							
6	Logical Block Address							
7	Logical Block Address (LSB)							

The size of the extent list is defined by the extent list length parameter. The extent list consists of zero or more descriptors as shown in Table 37. Each extent descriptor defines an extent beginning at the specified logical block address for the specified number of blocks. If the number of blocks is zero, the extent shall begin at the specified logical block address and continue through the last logical block address on the logical unit.

The reservation type field shall determine the type of reservation to be effected for each extent. Four types of reservations are possible as follows:

DB (1)	DB (0)	Reservation Type
1	0	Read Exclusive
0	1	Write Exclusive
1	1	Exclusive Access
0	0	Read Shared

Read Exclusive: While this reservation is active, no other Initiator will be permitted read operations to the indicated extent. This reservation will not inhibit write operations from any Initiator or conflict with a write exclusive reservation; however, read exclusive, exclusive access, and read shared reservations that overlap this extent will conflict with this reservation.

Write Exclusive: While this reservation is active, no other Initiator will be permitted write operations to the indicated extent. This reservation will not inhibit read operations from any Initiator or conflict with a read exclusive reservation from any Initiator. This reservation will conflict with write exclusive, exclusive access, and read shared reservations that overlap this extent.

Exclusive Access: While this reservation is active, no other Initiator will be permitted any access to the indicated extent. All reservation types that overlap this extent will conflict with this reservation.

Read Shared: While this reservation is active, no write operations will be permitted by any Initiator to the indicated extent. This reservation will not inhibit read operations from any Initiator or conflict with a read shared reservation. Read exclusive, write exclusive, and exclusive access reservations that overlap with this extent will conflict with this reservation.

If an Initiator attempts a command to a logical block that has been reserved and that access is prohibited by the reservation, the command will not be performed and the command will be terminated with a Reservation Conflict status. If a reservation conflict precludes any part of the command none of the command shall be performed. If any extent in a logical unit is reserved in any way, a Format Unit command will be rejected with a Reservation Conflict status.

4.12.3 THIRD PARTY RESERVATION

The third-party reservation option for the Reserve command allows an Initiator to reserve a logical unit or extents within a logical unit for another SCSI device.

If the third-party (3rdPTY) bit is zero, then the third-party reservation option is not requested. If the 3rdPTY bit is one then the Reserve command will reserve the specified logical unit or extents for the SCSI device specified in the third-party device ID field. The Target will preserve the reservation until it is superceded by another valid Reserve command from the same Initiator or until it is released by the same Initiator, Send Diagnostic Self-Test occurs, by a Bus Device Reset message from any Initiator, or a "hard" Reset condition. The Target will ignore any attempt to release the reservation made by any other Initiator.

4.12.4 SUPERCEDING RESERVATIONS

An Initiator that holds a current reservation may modify that reservation by issuing another Reserve command. The superceding Reserve command releases the previous reservation state when the new reservation request is granted. The previous reservation will not be modified if the new reservation request cannot be granted. If the superceding reservation cannot be granted because of conflicts with a previous active reservation (other than the reservation being superceded), then the target will return Reservation Conflict status.

4.13 RELEASE COMMAND

Peripheral Device Type: Direct Access, Write-Once Read-Multiple, Read-Only Direct Access
Operation Code Type: Optional
Operation Code: 17_H

The Release command is used to release previously reserved units, or previously reserved extents within logical units. It is not an error for an Initiator to attempt to release a reservation that is not currently active.

4.13.1 LOGICAL UNIT RELEASE

If the extent bit is zero, this command causes the Target to terminate all logical unit and extent reservations that are active from the Initiator to the specified logical unit.

Table 38: Release Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			3rd PTY	Third Party Device ID			Extent
2	Reservation Identification							
3	RESERVED							
4	RESERVED							
5	RESERVED						Flag	Link

4.13.2 EXTENT RELEASE

If the extent bit is one this command causes any reservation from the requesting Initiator with a matching reservation identification to be terminated. Other reservations from the requesting Initiator shall remain in effect.

4.13.3 THIRD-PARTY RELEASE

The third-party release option for the Release command allows an Initiator to release a logical unit or extents within a logical unit that were previously reserved using the third-party reservation option (see *4.12.3*).

If the third-party (3rdPTY) bit is zero, then the third-party release option is not requested. If the 3rdPTY bit is one then the target will release the specified logical unit or extents, but only if the reservation was made using the third-party reservation option by the same Initiator for the same SCSI device as specified in the third-party device ID field.

4.14 MODE SENSE COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Optional
Operation Code: $1A_H$

The Mode Sense Command provides a means for a Target to report its medium, drive, or peripheral device parameters. It is a complementary command to the Mode Select Command.

The Allocation Length specifies the number of bytes that the Initiator has allocated for returned sense data. An Allocation Length of zero indicates no sense data will be transferred. This is not considered an error condition. Any other value indicates the number of bytes to be transferred. The Target will terminate the data-in phase when Allocation Length bytes have been transferred or when all available sense data has been transferred to the Initiator.

Table 39: Mode Sense Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED		Page Code					
3	RESERVED							
4	Allocation Length							
5	RESERVED						Flag	Link

Mode Sense Header

BIT / BYTE	7	6	5	4	3	2	1	0
0	Sense Data Length (TBD)							
1	Medium Type (00)							
2	WP	RESERVED						
3	Block Descriptor Length							

The Mode Sense data contains a four-byte header, followed by zero or more eight-byte Block Descriptors, followed by the additional drive parameters, if any.

Block Descriptor

Byte	
0	Density Code (00)
1	Number of Blocks (MSB)
2	Number of Blocks
3	Number of Blocks (LSB)
4	RESERVED
5	Block Length (MSB)
6	Block Length
7	Block Length (LSB)

Page Descriptors

0	SDP	R	Page Code
1	Page Length (bytes)		
2	Refer to page definition		
n	Refer to page definition		

Table 40: Page Codes

0_H	Operating Parameters (selectable)
1_H	Error Recovery Parameters (default only)
2_H	Disconnection Parameters (default only)
3_H	Format Parameters (default only)
4_H through $3C_H$	Reserved (ignored)
$3D_H$	Report Default Values: All pages are returned with fields and bits set to their default values.
$3D_H$	Report Changeable Values: The operating parameters page is returned with all changeable bits set.
dF_H	Report Current Values: All pages are returned with their currently selected or default values.

Refer to Mode Select for a list of all page data.

4.15 START/STOP COMMAND

Peripheral Device Type: All
Operation Code Type: Optional
Operation Code: $1B_H$

Table 41: Start / Stop Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				IMMED
2	RESERVED							
3	RESERVED							
4	RESERVED							Start
5	RESERVED						Flag	Link

The Start/Stop Command requests the ST225N to move the R/W heads to/from the shipping zone. An Immediate (IMMED) bit of one indicates that status shall be returned as soon as the operation is initiated. An IMMED bit of zero indicates that status shall be presented when the operation is completed. A Start bit of one requests that the drive position itself at Track Ø. A Start bit of zero requests that the drive position itself at the shipping zone.

4.16 RECEIVE DIAGNOSTIC RESULTS COMMAND

Peripheral Device Type: All
Operation Code Type: Optional
Operation Code: $1C_H$

The Receive Diagnostic Results Command requests that analysis data be sent to the Initiator after completion of a Send Diagnostic Command.

User Diagnostic Commands: Four bytes of result data, conforming to the Nonextended Sense format, will be returned regardless of the Allocation Length. The diagnostic data returned depends on the Diagnostic Command. Following a Receive Diagnostic Command a Bus Reset must be performed to return to normal operating mode.

Table 42: Receive Diagnostic Results Command

BIT BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED							
3	Allocation Length (MSB)							
4	Allocation Length (LSB)							
5	RESERVED						Flag	Link

4.17 SEND DIAGNOSTIC COMMAND

Peripheral Device Type: All
Operation Code Type: Optional
Operation Code: $1D_H$

Table 43: Send Diagnostic Command

BIT BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED		SLFTST	RESERVED	UNITOFL
2	RESERVED							
3	Parameter List Length (MSB)							
4	Parameter List Length (LSB)							
5	RESERVED						Flag	Link

The Send Diagnostic Command requests that the Target perform self-diagnostic tests. There are no additional parameters for the user Send Diagnostic Command.

The Unit-Off-Line (UNITOFL) is not used in the ST225N.

The Self-Test (SLFTST) bit, if one, directs the Target to complete its default self-test. If this test is requested, the Parameter List Length must be set to zero. A Receive Diagnostic Results Command, or Sense Command (preferred) is required to receive self-test results.

If the SLFTST bit is not set, this command will always return with Good Status (no operation).

Note: This command allows the operating system to be independent of vendor-unique diagnostic commands. The diagnostic software then becomes more portable to various operating systems. Execution of the diagnostic self-test clears any extent reservations.

4.18 READ CAPACITY COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Extended
Operation Code: 25_H

Table 44: Read Capacity Command

BIT BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				RELADR
2	Logical Block Address (MSB)							
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address (LSB)							
6	RESERVED							
7	RESERVED							
8	RESERVED							PMI
9	RESERVED						Flag	Link

The Read Capacity Command provides a means for the Initiator to request information regarding the capacity of the drive.

The Partial Medium Indicator (PMI) bit, if zero, indicates that the information returned in the Read Capacity Data will be the Logical Block Address and Block Length of the last logical block of the drive. The Logical Block Address in the Command Descriptor Block must be set to zero for this option.

The PMI bit, if one, indicates that the information returned will be the Logical Block Address and Block Length of the last logical block after the Logical Block Address specified in the Command Descriptor Block before a substantial delay in data transfer (e.g., a cylinder boundary).

Table 45: Read Capacity Data

The following eight bytes of Read Capacity Data are sent during the data-in phase of the command.

BYTE	
0	Logical Block Address (MSB)
1	Logical Block Address
2	Logical Block Address
3	Logical Block Address (LSB)
4	Block Length (MSB)
5	Block Length
6	Block Length
7	Block Length (LSB)

4.19 READ COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Extended
Operation Code: 28_H

Table 46: Read Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				RELADR
2	Logical Block Address (MSB)							
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address (LSB)							
6	RESERVED							
7	Transfer Length (MSB)							
8	Transfer Length (LSB)							
9	RESERVED						Flag	Link

The Read Command requests that the Target transfer data to the Initiator.

The Logical Block Address specifies the Logical Block where the Read operation shall begin.

The transfer length specifies the number of contiguous blocks of data to be transferred. A transfer length of zero indicates that no logical blocks shall be transferred. This shall not be considered an error condition. Any other value indicates the number of logical blocks to be transferred.

The most recently written data value will be returned.

4.20 WRITE COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Extended
Operation Code: $2A_H$

The Write Command requests that the Target write the data transferred by the Initiator to the medium.

The Logical Block Address specifies the Logical Block where the Write operation shall begin.

The Transfer Length specifies the number of contiguous blocks of data to be transferred. A Transfer Length of zero indicates that no logical blocks shall be transferred. This is not considered an error condition. Any other value indicates the number of logical blocks to be transferred.

Table 47: Write Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	Logical Block Address (MSB)							
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address (LSB)							
6	RESERVED							
7	Transfer Length (MSB)							
8	Transfer Length (LSB)							
9	RESERVED						Flag	Link

4.21 READ DEFECT DATA COMMAND

Peripheral Device Type: Direct Access
Operation Code Type: Extended
Operation Code: 37_H

The Read Defect Data command requests that the Target transfer medium defect data to the Initiator.

The P-bit of byte-two requests that the Target return only the manufacturers defect list. The G-bit of byte-two requests that the Target return the host-added defects, as well as the reassigned block entries. This bit is only valid when the P-bit is set as well, allowing transfer of the entire defect management list.

The allocation length specifies the number of bytes reserved for the returned defect data. An allocation length of zero indicates no defect data is to be returned. Any other value indicates the maximum number of bytes that will be returned. The Target will determine the data-in phase when allocation length bytes have been transferred or all available defect data has been sent, whichever is less.

A maximum of 512 bytes of defect data can be generated by the drive.

The read defect data contains a four-byte header, followed by zero or more defect descriptors.

Byte-one indicates the defect list actually returned by the Target.

The defect list length contains the actual length of the defect list unadjusted for truncation.

The defect data returned is in physical address format.

The reassigned block entry contains the original (old) address followed by the reassigned address (new).

The defect list is supplied sorted in ascending order using the old address for the reassigned blocks. The reassigned block entries, if any, follow the complete list of defect entries.

Table 48: Read Defect Data Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			RESERVED				
2	RESERVED			P	G	RESERVED		
3	RESERVED							
4	RESERVED							
5	RESERVED							
6	RESERVED							
7	Allocation Length (MSB)							
8	Allocation Length (LSB)							
9	RESERVED						Flag	Link

Defect List Header

BIT BYTE	7	6	5	4	3	2	1	0
0	RESERVED							
1	RESERVED			P	G	RESERVED		
2	Defect List Length (MSB)							
3	Defect List Length (LSB)							

Defect Entry

BIT BYTE	7	6	5	4	3	2	1	0
0	Cylinder (MSB)							
1	Cylinder (LSB)							
2	Head							
3	Sector							

Reassigned Entry

BIT BYTE	7	6	5	4	3	2	1	0
0	Old Cylinder (MSB)							
1	Old Cylinder (LSB)							
2	Old Head							
3	Old Sector							
4	New Cylinder (MSB)							
5	New Cylinder (LSB)							
6	New Head							
7	New Sector							

5.0 SENSE KEYS AND ERROR CODE DESCRIPTIONS

Table 49: Sense Keys (0-7)

Sense Key	Description
0_H	**NO SENSE:** Indicates that there is no specific Sense Key information to be reported for the designated unit.
1_H	**RECOVERY ERROR:** Indicates that the last command was successfully completed, with some recovery action performed by the drive. Details can be determined by examining the Additional Sense bytes and the Information bytes.
2_H	**NOT READY:** Indicates that the drive cannot be accessed. Operator intervention may be required to correct this condition.
3_H	**MEDIUM ERROR:** Indicates that the command terminated with a nonrecovered error condition which was probably caused by a flaw in the medium, or an error in the recorded data.
4_H	**HARDWARE ERROR:** Indicates that the drive detected a nonrecoverable hardware failure (controller failure, device failure, etc.) while performing the command, or during a self-test.
5_H	**ILLEGAL REQUEST:** Indicates that there was an illegal parameter in the Command Descriptor Block or in the additional parameters supplied as data for some commands
6_H	**UNIT ATTENTION:** Indicates that a reset has occurred since the last selection by this initiator.
7_H	**DATA PROTECT:** Not Supported

Table 50: Sense Keys (8-F)

Sense Key	Description
8_H	**BLANK CHECK:** Not Supported
9_H	**VENDOR UNIQUE:** Reserved
A_H	**COPY ABORTED:** Not Supported
B_H	**ABORTED COMMAND:** Not Supported
C_H	**EQUAL:** Not Supported
D_H	**VOLUME OVERFLOW:** Not Supported
E_H	**MISCOMPARE:** Not Supported
F_H	This Sense key is reserved

5.1 ERROR CODES

Table 51: Error Codes

Error 02—Seek Error: This code is logged whenever a seek fails to position the Read/Write heads to the correct cylinder. This error is reported after an unsuccessful retry or when retry is disabled.

Error 03—Write Fault: When a Write Fault is detected the controller will terminate the active command and presents this error on the next command.

Error 04—Drive Not Ready: This error indicates that the drive was not up-to-speed when the command was issued.

Error 05—Address Mark Not Found: This error is presented after two revolutions on a track with no address mark found.

Error 10—ID Field ECC Error: This error indicates an ECC error in an ID field. This error is reported after an unsuccessful retry or when retry is disabled.

Error 11—Uncorrectable Data Error: This error indicates an unrecoverable data error on a data field. This error is reported after an unsuccessful retry or when retry is disabled.

Error 12—Data Address Mark Not Found: This error indicates that the data field address mark could not be read. This error is reported after an unsuccessful retry or when retry is disabled.

Error 14—No Match On ID Field: This error can occur on any Read or Write data command if two Indexes have passed without a match on the ID field. Retry is performed by reading any ID field on the track, calculating the track number and comparing it to the expected track number. If it does compare, then the error is reported to the host.

Error 1B—Recoverable ID ECC Error: This code indicates a successful retry of an ID ECC error.

Error 18—Recoverable Data Error: This code indicates retry or error correction was successful.

Error 19—Recoverable Data Address Mark: This code indicates a successful retry of a *Data Address Mark Not Found* error.
Error 1A—Recoverable ID Field: This code indicates a successful retry to match on an address mark.

Error 20—Invalid Command: This error indicates that the received command byte is illegal or not implemented.

Error 24—Invalid Parameter: This error indicates that the Command Block contained invalid parameter(s) or nonzero reserved areas.

Error 25—Invalid Logical Unit Number (LUN): This error indicates that the Command Block addressed an illegal LUN (nonzero).

Error 29—Internal Controller Error: This error indicates that an internal diagnostic has failed.

Error 2A—Defect Map Overflow: This error indicates that the total number of defective sectors to be formatted exceeds the table size.

Error 2B—Time Out On Reselection: This code indicates that following Target disconnection, three reselection attempts on the Initiator have failed.

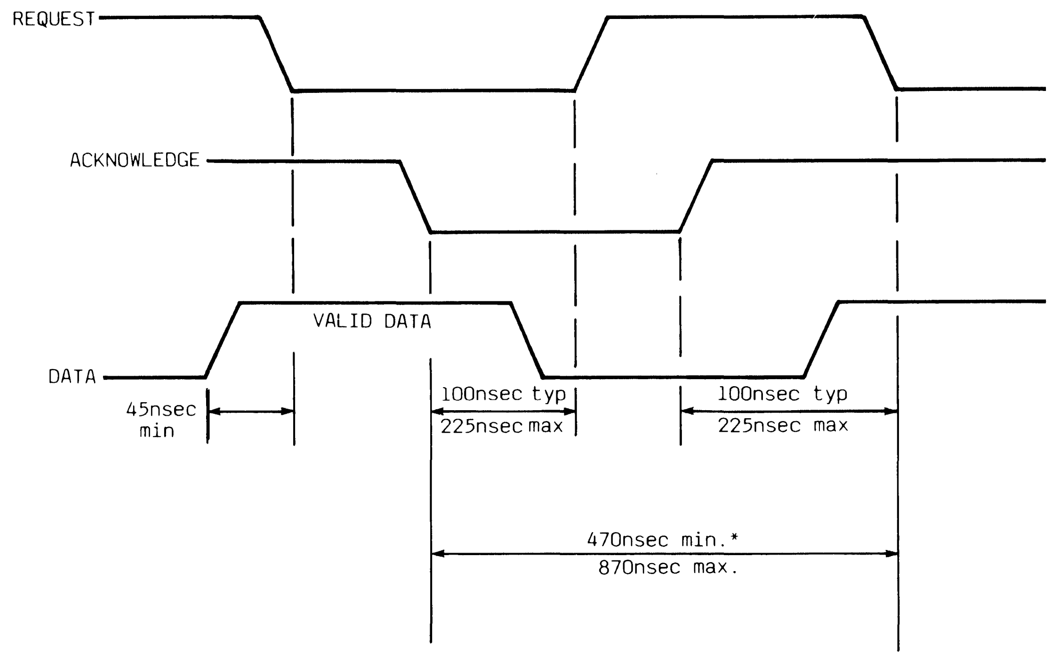
Error 2C—Overflow On Usage Counter: This error indicates that one of the usage counters overflowed on the previous command; normally disabled from Status.

Error 2D—Initiator Detected Error: This error indicates that the current command received an Initiator-detected error message.

Error 2F—Target Reset: This code indicates that the Target was reset prior to this command; accompanies Unit Attention.

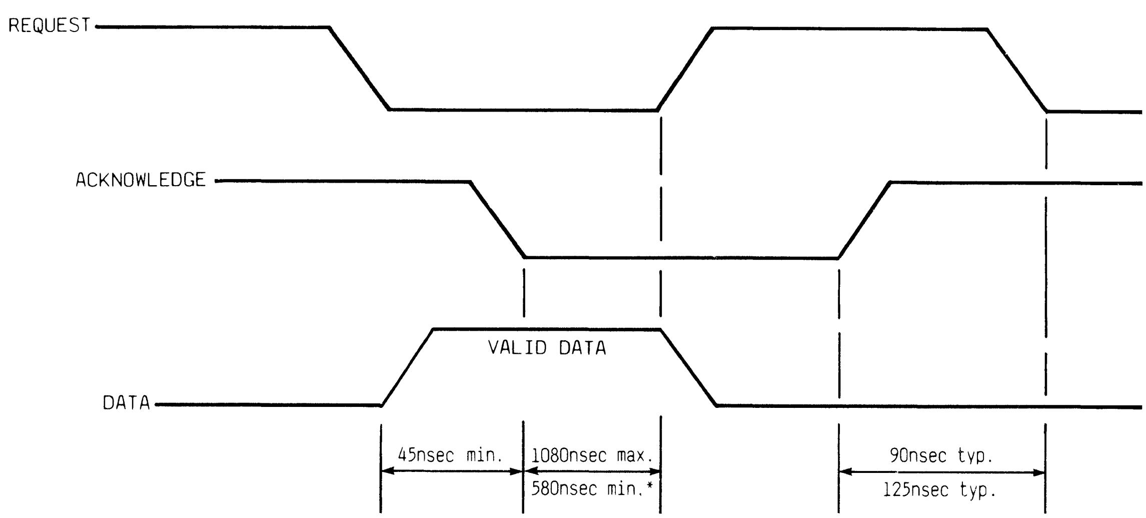
Appendix 1: Data Transfer Timing

READ DATA TRANSFER



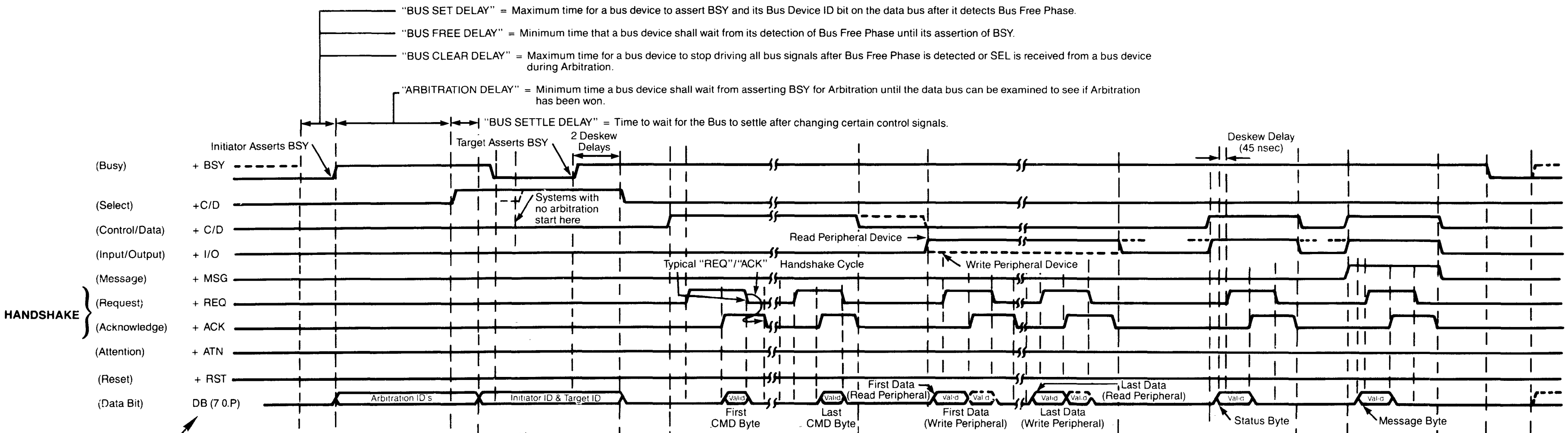
*Minimum worst case timing assumes Acknowledge is asserted 70 nsec. prior to internal clock (400 nsec.)

WRITE DATA TRANSFER



*Minimum worst case timing assumes Acknowledge is asserted 80 nsec. prior to internal clock (400 nsec.).

Appendix 2: SCSI Timing Chart



Bus Free

INITIATOR tries to gain control of the bus.

INITIATOR gained control of the Bus and selects a TARGET.

TARGET requests command bytes from the INITIATOR.

TARGET requests data transfer on the bus.

TARGET requests that status be sent to the INITIATOR.

TARGET requests INITIATOR to analyze message.

Bus is released.

NOTE:

DB (7) — Most significant bit. Pighest priority ID for Arbitration

NOTE:
DP(P) Data parity (odd)
Parity is not valid during Arbitration.

The use of parity is a system option.

NOTE:
In a typical system, a computer's host adapter will act as the "INITIATOR," and an I/O device's control unit will act as the "TARGET."

BUS FREE PHASE

Sel and BSY are both false for at least one Bus Settle Delay.

ARBITRATION PHASE

Implementation of this phase is a system option.

At least one Bus Free Delay, but no more than one Bus Set Delay, after Bus Free Phase has been detected, the INITIATOR asserts BSY and its own Bus Device ID bit on the data bus.

The INITIATOR waits an Arbitration Delay then examines the Data Bus. If a higher priority Bus Device ID bit is true on the Data Bus (DB7 is the highest), the INITIATOR loses Arbitration and releases BSY. If no higher priority Bus Devide ID bit is true on the Data Bus, the the INITIATOR wins Arbitration and asserts SEL.

SELECTION PHASE

During this phase the I/O signal is deasserted to distinguish this phase from the Reselection Phase.

NON ARBITRATING SYSTEMS. In systems with the Arbitration Phase not implemented, after detecting the Bus Free Phase, the INITIATOR waits a minimum of one Bus Clear Delay then it asserts the Data Bus with both the desired INITIATOR ID bit and the TARGET'S ID bit. After two deskew delays the INITIATOR asserts SEL.

ARBITRATION SYSTEMS: In systems with the Arbitration Phase implemented, the INITIATOR that won Arbitration has both BSY and SEL asserted and changes the Data Bus after two Bus Settle Delays. The Data Bus is then asserted with both the desired INITIATOR ID bit and the TARGET'S ID bit. Two deskew delays later BSY is released.

IN ALL SYSTEMS: The TARGET determines that it is selected when SEL and its Bus Device ID bit are true and BSY and I/O are false for at least a Bus Settle Delay. The TARGET then asserts BSY within a Selection Abort Time.

Two deskew delays after the INITIATOR detects BSY true, it releases SEL and may change Data Bus signals.

COMMAND PHASE

The TARGET asserts C/D and deasserts I/O and MSG for all of the handshakes of this phase.

The transfer is from INITIATOR to TARGET.

HANDSHAKE PROCEDURE:

The TARGET asserts REQ. The INITIATOR drives data (7-0,P) to their desired values, waits at least one deskew delay plus a cable skew delay and asserts ACK. The INITIATOR continues to drive data (7-0,P), then asserts REQ.

When REQ becomes false at the INITIATOR the INITIATOR may change or release data (7-0,P) and deassert ACK.

The TARGET continues requesting command bytes. The number of bytes depends on the command group code detected from the first command byte received.

DATA IN OR OUT PHASE

DATA IN PHASE: Read Peripheral.

Data is to be sent from TARGET to INITIATOR.

TARGET asserts I/O, deasserts C/D and MSG during the REQ/ACK handshake of this phase.

HANDSHAKE PROCEDURE:

The TARGET first drives data (7-0,P) to their desired values, waits at least one deskew delay plus a cable skew delay, then asserts REQ. Data (7-0,P) shall remain valid until ACK is true at the TARGET.

The INITIATOR shall read data (7-0,P) after REQ is true, then asserts ACK.

When ACK becomes true at the TARGET, the TARGET may change or release data (7-0,P) and deassert REQ.

After REQ is false, the INITIATOR deasserts ACK. After ACK is false, the TARGET may continue the transfer by driving data (7-0,P) and asserting REQ.

DATA OUT PHASE: Write Peripheral.

Data is to be sent from INITIATOR to TARGET.

TARGET deasserts D/D, I/O and MSG during the REQ/ACK handshake of this phase. Refer to the handshake procedure of the Command Phase.

STATUS PHASE
(ENDING STATUS)

TARGET requests that a status byte be sent to the INITIATOR.

TARGET asserts C/D and I/O and deasserts MSG during the handshake of this phase.

Only one byte of status is transferred.

See handshake procedure under Data in phase.

MESSAGE IN PHASE
(INTERRUPT)

TARGET requests message byte(s) to be sent from TARGET to INITIATOR.

TARGET asserts C/D, I/O and MSG during the REQ/ACK handshake(s) of this phase.

The message byte could indicate "Command Complete" (00) indicating interrupt.

See handshake procedure under Data in phase.

BUS FREE PHASE

TARGET deasserts BSY to indicate that the bus is available for subsequent users.

TARGET releases all bus signals within a Bus Clear Delay after BSY becomes continuously false for a Bus Settle Delay.

The following phase will be an Arbitration Phase.

SAMPLE SCSI TIMING CHART
(COMMANDS WITHOUT DISCONNECT/RECONNECT)

Appendix 3: FLOW DIAGRAM FOR DISCONNECT/RECONNECTION

1) Initiator Selects Target with ATTN Asserted

2) Target requests Message Out Transfer (Identify Message)
   - Message asserted, C/D asserted, I/O false
   - Request asserted
     (DB) Bit 7 set for Identify Message (Initiator)
     Bit 6 set for disconnect capability
     Bit 5-0 zero
   - Initiator acknowledge

3) Target Requests Command Transfer
   - Message false, C/D asserted, I/O false
   - Request asserted Target will request 6 bytes, pause and analyze command code to determine if this is a 10-byte command, if so, 4 more bytes will be requested.

4) Read, Write, Seek, Format Command

5) Target disconnection (if Identify was sent with disconnect bit)
   - Disconnect Message
     In
   - Message asserted, C/D asserted, I/O asserted (no change)
   - DB set to 04_H
   - Request asserted
     Initiator acknowledge
   - Disconnect from Bus
   - Release DB
   - Release Busy, Select
   - Clear message, I/O, L/D
     Target complete Seek or Format

Reconnection Example for Read Data

6) Target arbitrates for Bus
   - Wait for Bus Free
   - Drive Target ID on DB
   - If winner, drive Select & Busy
   - If loser & Select, complete selection, give Busy Status and disconnect

7) Target Reselects Initiator
   - Drive Initiator & Target ID bits on Bus
   - Message false, I/O asserted, C/D false
   - Release Busy
   - Wait for Busy from Initiator
   - Timeout 250msec, go to Bus Free & retry twice
     Abort Command -Error Code: Initiator reselection Timeout $2B_H$
   - Target drives Busy out
   - Target clears Select
   - Target clears I/O, Message & C/D already false

8) Target Issues Identify Message

- Message asserted, I/O asserted, C/D asserted
- DB set to 7OH -Identify, LUN 0
- Request asserted-Initiator acknowledge

9) Target Requests Data Transfer IN

- Message false, C/D false, I/O false
- Request asserted
  Data transferred from Target to Initiator

10) Target Presents Ending Status

- Status byte transfer I/O & C/D asserted
- Message In -Command complete, Message, I/O & C/D asserted
- Disconnect from Bus

Appendix 4: Glossary

Byte: Eight bits

Command Descriptor Block: The structure used to communicate requests from an Initiator to a Target.

Connect: Occurs when an Initiator selects a Target to start an operation.

Disconnect: Occurs when a Target releases control of the SCSI Bus, allowing it to go to the Bus Free phase.

Initiator: An SCSI device (usually a host system) that requests an operation to be performed by another SCSI device.

Intermediate Status: A status code sent from a Target to an Initiator upon completion of each command in a set of linked-commands (except the last command in the set).

Logical Unit: A physical or virtual device

LSB: Least significant bit

LUN: Logical unit number

MSB: Most significant bit

One: A true signal value

Peripheral Device: A peripheral device that can be attached to an SCSI device (e.g., magnetic disc, printer, optical disc or magnetic tape).

Reconnect: Occurs when a Target selects an Initiator to continue an operation after a disconnect.

Reserved: The term used for bits, bytes, fields and code values that are set aside for future standardization.

SCSI Address: The octal representation of the unique address (0-7) assigned to an SCSI device. This address would normally be assigned and set in the SCSI device during system installation.

SCSI ID: The bit-significant representation of the SCSI address referring to one of the signal lines DB(7-0).

SCSI Device: A host computer adapter, peripheral controller or an intelligent peripheral that can be attached to the SCSI Bus.

Signal Assertion: The act of driving a signal to the true state.

Signal Negation: The act of driving a signal to the false state or allowing the cable termninators to bias the signal to the false state (by placing the driver in the high impedance condition).

Signal Release: The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

Status: One byte of information sent from a Target to an Initiator upon completion of each command.

Target: An SCSI device that performs an operation requested by an Initiator.

XX_H: Numbers followed by a subscript captial H are hexadecimal values. All other numbers are decimal values.

Zero: A false signal value.

Appendix 5: Implementation Notes

Sense Command: Nonextended Sense is intended for SASI compatibility only. The Extended Sense length of 27 should always be requested to insure that all nine usage counters will be received in the event of a overflow.

Individual error codes are intended primarily for diagnostic purposes. Host recovery actions should be derived from the Sense Keys.

The physical address corresponding to a given logical block address is provided for Host verification of defect mapping only. Logical block addresses must be supplied when specifing new defects during Format.

Format Command: The Format Command should always be preceded by a Mode Select Command to set up the parameters. Three format options are provided.

1. **Format with manufacturer's defect list:** The controller will use the original manufacturer's defect list (bytes from the Index format) only to generate a new defect list table for the requested block size. This option is required when changing the formatted block size.

2. **Format with manufacturer's defect list plus supplied defects:** This option allows the host to add defects in the logical block format to the current defect table using the same blocksize. Defects must be supplied in ascending order.

3. **Format with known defect list only:** This option allows the host to re-format the drive using the current defect table (manufacturer's list plus any previously added defects) using the same blocksize. This command would typically be used to preserve the defect table when changing the interleave factor, etc.

Read Usage Counters: The usage counters provide diagnostics information since the last power on. To compile a usage history, the counters should be read before power-down and usage enabled (see Mode Select) to present an error warning upon overflow.

Upon an overflow, the counters are saved and reported in Sense or by Read Usage Counters (whichever comes first). The counters are always cleared after reading. There are five counters.

1. **Blocks Read:** The total number of data blocks transferred to the host.

2. **Seeks:** The total number of seeks requiring repositioning including seek error recovery and cylinder switch during reads.

3. **Uncorrectable Read Errors:** The total number of times that ECC was applied (including retries) without correction.

4. **Correctable Read Errors:** The total number of times that ECC was applied with correction.

5. **Seek Errors:** The total number of times that a positioning seek failed to locate the correct track.

Mode Select: Primarily used to select a blocksize prior to format. Unspecified (zero) perameters will revert to the default values for the requested blocksize. The full disc capacity will always be formatted, but an artificial maximum number of blocks may be specified.

1. The Usage, Recovery and Status bits allow host control of certain optional controller features.

2. Usage will cause command rejection with overflow sense following overflow of any counter on the previous command.

3. Recovery allows the host to disable error recovery, including ECC and retries for diagnostic purposes.

4. Status allows the host to enable error presentation which indicates if error recovery was used on the current command.

Mode Sense: reports back all Mode Select parameters plus the physical parameters for the drive including the currently formatted interleave factor.

Message Out: Transfers (Attention condition) are performed immediately following selection and during data transfers. Message Out during transfers implies immediate command termination.

920 Disc Drive, Scotts Valley, CA 95066-4544, USA ■ 408/438-6550