ST506

PRODUCT

MANUAL

Seagate

ST506
Product Manual

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1.0 Introduction

1.1 General Description:

The ST506 disc drive is a random access storage device utilizing two non-removable 5¼ inch discs as storage media. Each disc surface employs one read/write head to service 153 tracks.

Low cost and unit reliability are achieved through the use of a band actuator and open loop stepper head positioning mechanism. The inherent simplicity of mechanical construction and electronic controls allow maintenance free operation throughout the life of the drive. Both PC Boards are mounted outside the Head Disc Assembly (HDA), allowing field serviceability.

Mechanical and contamination protection for the heads, actuator, and discs is provided by an impact resistant aluminum enclosure. An integral air recirculating system provides clean air through a 0.3 micron filter. A second port in the filter assembly allows ambient air pressure equalization without chance of contamination. A patented spindle pump assures adequate air flow and uniform temperature distribution throughout the head and disc area. Thermal isolation of the stepper and spindle motor assemblies from the disc enclosure results in a very low temperature rise within the HDA. This provides significantly greater off-track margin and the ability to immediately perform read and write operations after power up with no thermal stabilization delay.

The ST506 is identical in size and mounting configuration to the industry standard minifloppy disc drives. They use the same DC voltages, and no AC power is required.

Key Features:

- Storage Capacity of 6.38 megabytes unformatted, 5.0 megabytes formatted.
- Same physical size and mounting as the minifloppy.
- Same DC voltages as the minifloppy.
- Band actuator and stepper motor head positioning.
- 5.0 megabit/second transfer rate.
- Simple floppy-like interface.
- Same track capacity as a double density 8 inch floppy.

1.2 Specification Summary

1.2.1 Physical Specifications/Environmental Limits

Ambient Temperature

Operating:	40° to 122°F (4° to 50°C)
Non-operating:	−40° to 140°F (−40° to 60°C)

Maximum Temperature Gradient

Operating:	18°F/hour or 10°C/hour
Non-operating:	Below condensation

Relative Humidity: 8 to 80% non-condensing

Maximum Wet Bulb: 78.8°F (26°C)

Maximum elevation

Operating:	10,000 feet
Non-operating:	−1,000 to 30,000 feet

Maximum Shock Without Incurring Physical Damage

Operating:	10G's*
Non-operating:	20G's*

*No mechanical damage will occur within these limits.

D.C. Power Requirements
+12V ±5%, 1.6A typical, 3.5A (At power on)
+ 5V ±5%, .7A typical, 1.0A (Maximum)
Maximum Ripple: 50mV peak to peak (12V, 5V)

Mechanical Dimensions

Height:	3.25 inches
Width:	5.75 inches
Depth:	8.00 inches
Weight:	4.6 pounds (2.1Kg)
Shipping Weight:	9.0 pounds (4.1Kg)

Heat Dissipation

Typical:	25 watts
Maximum:	29 watts

Maximum Accoustic Output: 50DBA @ 12" distance

1.2.2 Reliability Specifications

MTBF:	11,000 POH, typical usage
MTTR:	30 minutes
PM:	Not required
Component design life:	5 years

Error Rates

Soft Read Errors*:	1 per 10^{10} bits read
Hard Read Errors**:	1 per 10^{12} bits read
Seek Errors:	1 per 10^{6} seeks

*Recoverable within 16 retries

**Not recoverable within 16 retries

1.2.3 Performance Specifications

Capacity

	Formatted	Unformatted
Per Drive:	5.0 Megabytes	6.38 Megabytes
Per Surface:	1.25 Megabytes	1.59 Megabytes
Per Track:	8,182 Bytes	10,416 Bytes

Access Time		
Track To Track		3ms
Average*:		85 ms
Maximum*:	205 ms	
Settling Time:		15 ms ± 10%

*Using fast seek (includes settling)

Transfer Rate:		5.0 Mbits/sec
Average Latency:	8.33 ms	

1.2.4 Functional Specifications

Rotational Speed:	3,600 RPM ± 1%
Recording Density:	7,690 BPI
Flux Density:	7,690 FCI
Track Density:	255 TPI
Cylinders:	153
Tracks:	612
Read/Write Heads:	4
Discs:	2

2.0 **Functional Characteristics**

2.1 General Operation:

The ST506 disc drive consists of read, write, and control electronics, read/write heads, track positioning actuator, media, and air filtration system. The components perform the following functions:

1. Interpret and generate control signals.
2. Position the heads over the desired track.
3. Read and Write data.
4. Provide a contamination free environment.

2.2 Read/Write and Control Electronics

The electronic are packaged on two printed circuit boards. The Main Control PC Board, to which power, control, and data signals are connected includes:

1. Index detection circuit.
2. Head position/actuator circuit.
3. Drive up-to-speed circuit.
4. Drive select circuit.
5. Read/write circuits.
6. Head select circuit.
7. Write fault detection circuit.
8. Stepper motor drive circuit.
9. Track 0 detector circuit.

The Motor Control PCB provides the speed, power and braking controls for the spindle motor. The Motor Control PCB derives its' power from and is mounted below the Main Control PC Board.

2.3 Drive Mechanism

A direct drive brushless DC motor rotates the spindle at 3600RPM. The spindle motor is thermally isolated from the Head/Disc assembly (HDA) to minimize temperature rise within the sealed HDA chamber. The motor and spindle are dynamically balanced to ensure a low vibration level. The HDA is shock mounted to minimize transmission of vibration from the chassis or frame.

2.4 Air Filtration System (Figures 1.0 & 2.0)

The discs and read/write heads are fully enclosed in a chamber using an integral air recirculation system and a 0.3 micron filter to maintain a clean environment. The filter also contains a port which permits ambient pressure equalization without contaminate entry.

2.5 Positioning Mechanism (Figure 3.0)

The read/write heads are mounted on a ball bearing supported carriage which is positioned by a band actuator connected to the stepper motor shaft. The stepper motor is thermally isolated from the HDA to minimize temperature rise within the sealed chamber.

2.6 Read/Write Heads and Discs

The recording media consists of a lubricated thin magnetic oxide coating on a 130mm diameter aluminum substrate. This coating formulation, integrated with the low load force/low mass flying heads, permits reliable contact start/stop operation.

Data on each of the disc surfaces is read by one read/write head, each of which accesses 153 tracks.

FIGURE 1.0

AIR FILTRATION SYSTEM

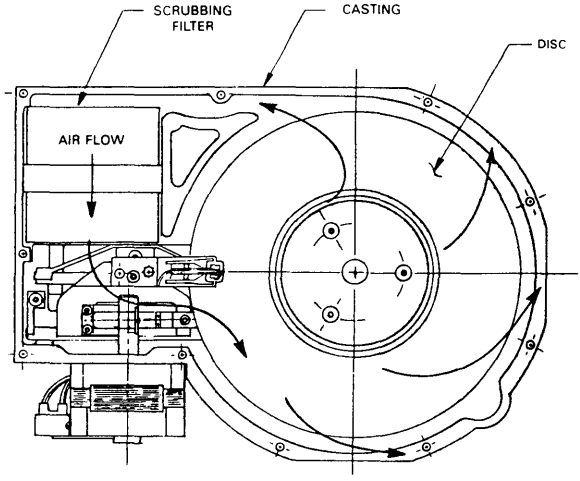


FIGURE 2.0

SPINDLE HUB AIR FLOW

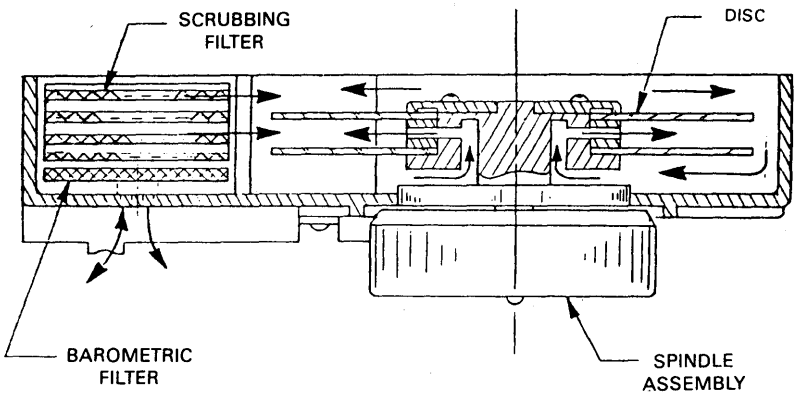
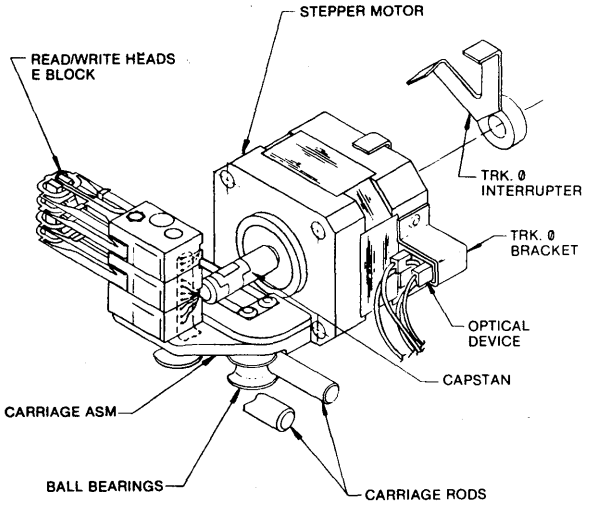


FIGURE 3.0

POSITIONING MECHANISM



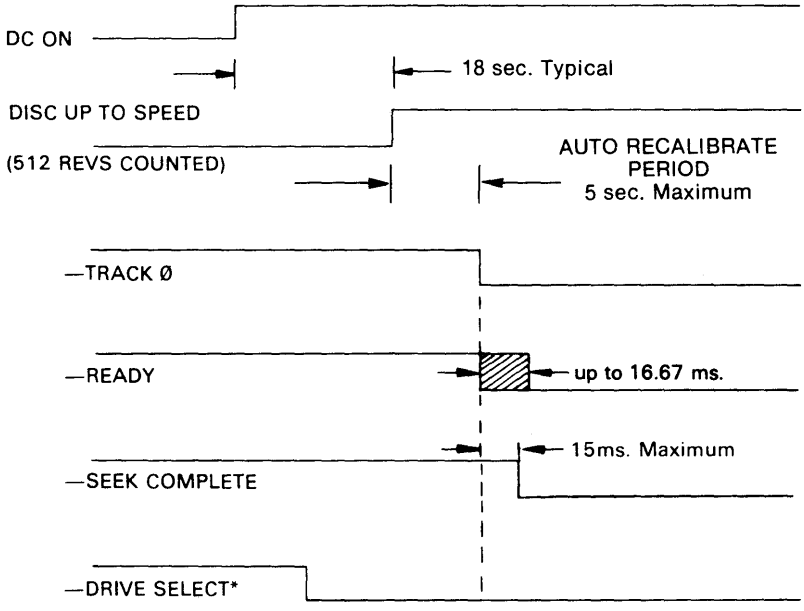
3.0 Functional Operations

3.1 Power Sequencing (Figure 4.0)

Plus 5 and +12 volts may be applied in any order; however, +12 volts must be applied to start the spindle drive motor. A speed sense circuit counts 512 disc revolutions before recalibrating the heads to Track Ø. For this recalibration to occur, the step input signal must be inactive. TRACK Ø, SEEK COMPLETE, and READY signals on the interface will become true sequentially. The drive will not perform read, write or seek functions until READY becomes true.

FIGURE 4.0

POWER UP SEQUENCE



(*GATES READY, TK Ø, SEEK COMPLETE)

3.2 Drive Selection

Drive selection occurs when one of the DRIVE SELECT lines is activated. Only the selected drive will respond to the input signals, and only that drive's output signals are then gated to the controller interface (See section 4.5 for exception).

3.3 Track Accessing

Read/write head positioning is accomplished by:

a) Deactivating WRITE GATE line.

b) Activating the appropriate DRIVE SELECT line.

c) Being in the READY condition with SEEK COMPLETE true.

d) Selecting the appropriate direction.

e) Pulsing the STEP line.

Each step pulse will cause the head to move either 1 track in or 1 track out depending on the level of the direction line. A low level on the direction line will cause a seek inward toward the spindle, a high, outward toward Track 0.

3.4 Head Selection

Any of the heads can be selected by placing the head's binary address on the Head Select lines.

3.5 Read Operation

Reading data from the disc is accomplished by:

a) Deactivating the WRITE GATE line.

b) Activating the appropriate DRIVE SELECT line.

c) Assuring the drive is READY.

d) Selecting the appropriate head.

3.6 Write Operation

Writing data onto the disc is accomplished by:

a) Activating the appropriate DRIVE SELECT line.

b) Assuring the drive is READY.

c) Selecting the appropriate head.

d) Ensuring no WRITE FAULT conditions exist.

e) Activating WRITE GATE and placing data on the WRITE DATA line.

4.0 Electrical Interface

The ST506 interface can be divided into three categories:

1. Control Signals.
2. Data Signals.
3. DC Power.

All control lines are digital in nature (open collector TTL) and either provide signals to the drive (input) or signals to the host (output) via interface connection J1/P1. The data transfer signals are differential in nature and provide data either to (write) or from (read) the drive via J2/P2 (Defined by EIA RS-422).

Tables I. through III. and Figures 5.0 through 7.0 show connector pin assignments and interconnection of cabling between the host controller and drives.

TABLE I.

J1/P1 CONNECTOR PIN ASSIGNMENTS

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	– REDUCED WRITE CURRENT
3	4	RESERVED (HD SELECT 2^2)
5	6	– WRITE GATE
7	8	– SEEK COMPLETE
9	10	– TRACK Ø
11	12	– WRITE FAULT
13	14	– HEAD SELECT 2^0
15	16	RESERVED (TO J2 PIN 7)
17	18	– HEAD SELECT 2^1
19	20	– INDEX
21	22	– READY
23	24	– STEP
25	26	– DRIVE SELECT 1
27	28	– DRIVE SELECT 2
29	30	– DRIVE SELECT 3
31	32	– DRIVE SELECT 4
33	34	– DIRECTION IN

TABLE II.

J2/P2-CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	– DRIVE SELECTED
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED (TO J1 PIN 16)
	9,10	RESERVED
12	11	GND
	13	+ MFM WRITE DATA
	14	– MFM WRITE DATA
16	15	GND
	17	+ MFM READ DATA
	18	– MFM READ DATA
20	19	GND

TABLE III.

J3/P3 CONNECTOR PIN ASSIGNMENTS

GND RTN PIN	SIGNAL PIN	DESCRIPTION
2	1	+ 12 Volts DC
3	4	+ 5 Volts DC

FIGURE 5.0
CONTROL SIGNALS

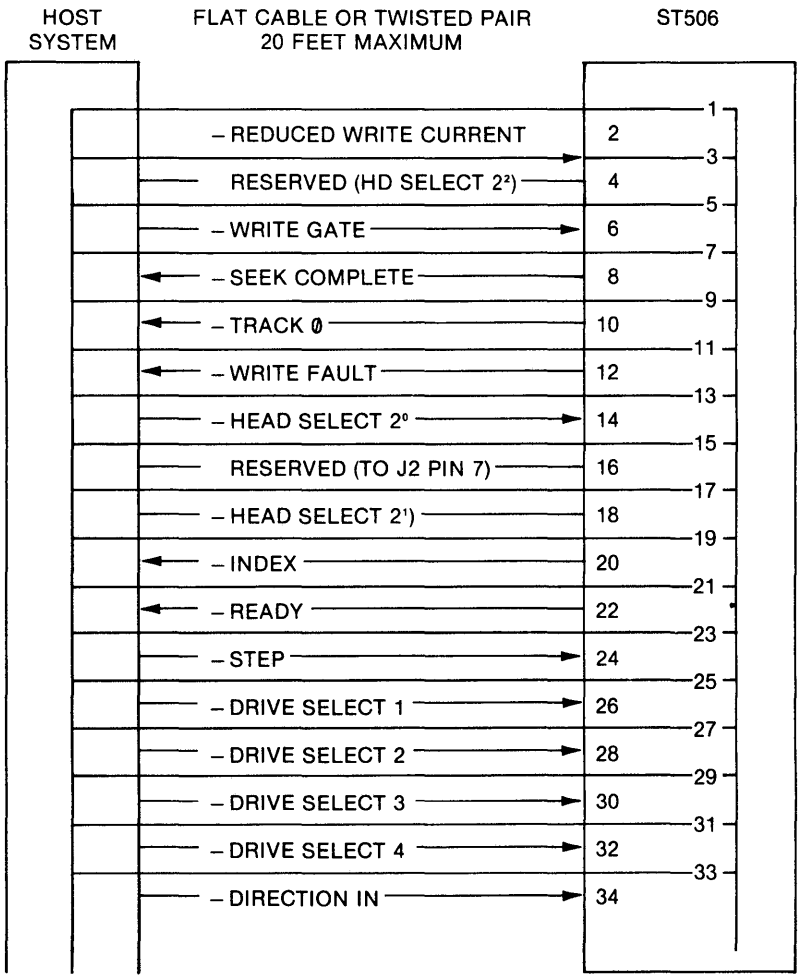


FIGURE 6.0

DATA SIGNALS

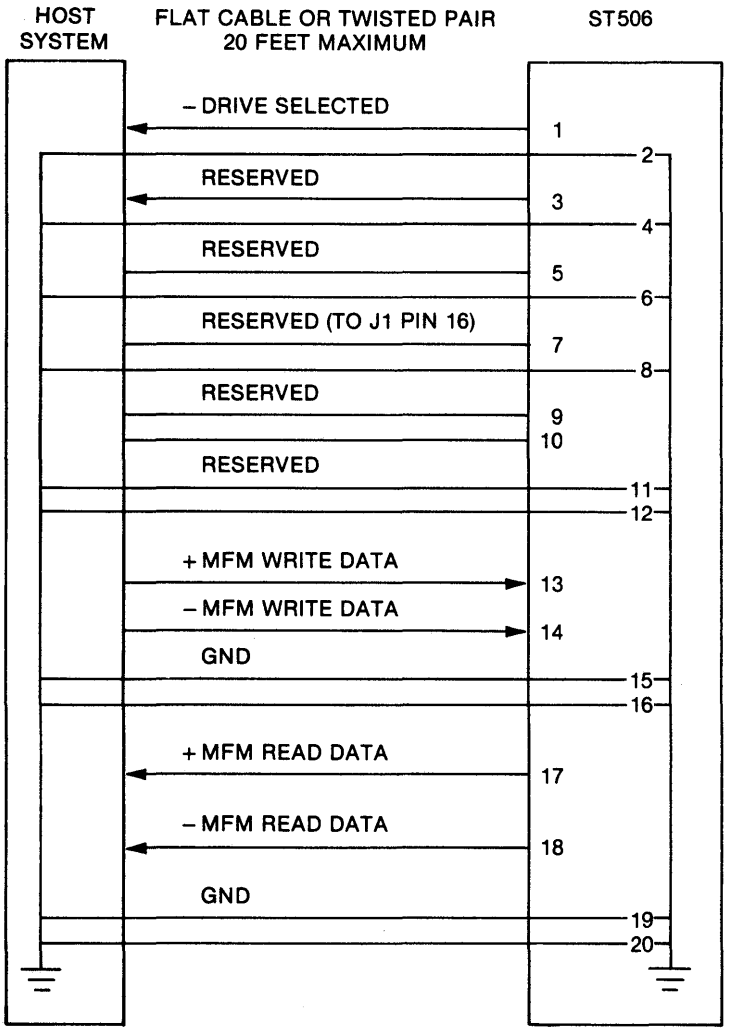
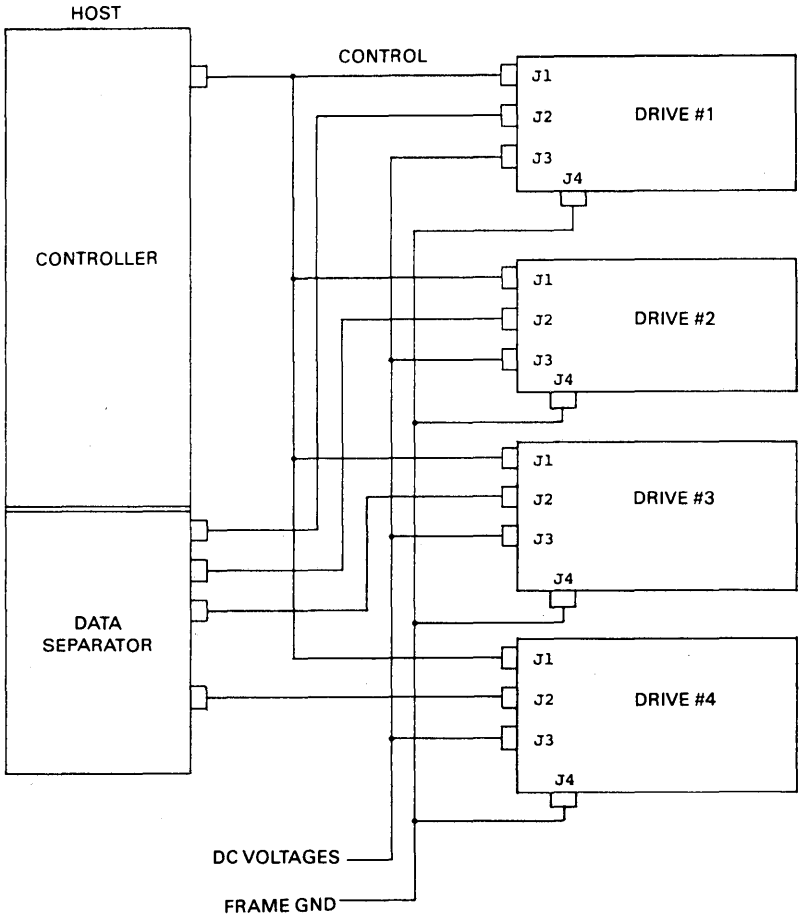


FIGURE 7.0

TYPICAL CONNECTION, 4 DRIVE SYSTEM



4.1 Control Input Lines

The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are: WRITE GATE, HEAD SELECT 2^1, HEAD SELECT 2^0, STEP, and DIRECTION IN. The signal to perform the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, or DRIVE SELECT 4.

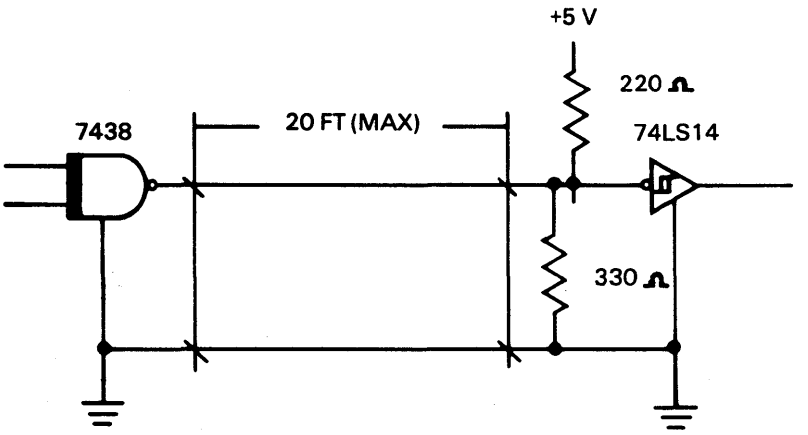
The input lines have the following electrical specifications. Refer to Figure 8.0 for the recommended circuit.

TRUE: 0.0VDC to 0.4VDC@I = −48mA (MAX)

FALSE: 2.5VDC to 5.25VDC@I = +250uA (OPEN COLLECTOR)

FIGURE 8.0

CONTROL SIGNALS DRIVER/RECEIVER COMBINATION



4.1.1. REDUCED WRITE CURRENT

This line, when active together with WRITE GATE, causes the write circuitry to write on the disc with a lower write current.

It is required that this line be set true when writing is performed on cylinders 128 through 152, and set false when writing on cylinders Ø through 127.

A 220/330 ohm resistor pack allows for line termination.

4.1.2 WRITE GATE

The active state of this signal, or low level, enables write data to be written on the disc. The inactive state of this signal, or high level, enables data to be read from the drive.

A 220/330ohm resistor pack allows for line termination.

4.1.3 HEAD SELECT 2^0, 2^1

These active low lines allow selection of each individual read/write head in a binary coded sequence. The heads are numbered Ø through 3, with head Ø being the least significant. When all HEAD SELECT lines are high (inactive), head Ø will be selected.

A 220/330ohm resistor pack allows for line termination.

4.1.4 DIRECTION IN

This signal defines direction of motion of the read/write head when the STEP line is pulsed. An open circuit or high level defines the direction as "out" and if a pulse is applied to the STEP line, the read/write heads will move toward the center of the disc. If this line is a low level, the direction is defined as "in" and the read/write heads will move toward the center of the disc. A change in direction must meet the requirements shown in Figure 9.0.

A 220/330ohm resistor pack allows for line termination.

Note: Direction must not change during step time.

4.1.5 STEP

This control signal causes the read/write heads to move in the direction of motion defined by the DIRECTION IN line.

Any change in the DIRECTION IN line must be made at least 100ns before the leading edge of the step pulse (refer to Figure 9.0 for general timing requirements).

A 220/330ohm resistor pack allows for line termination.

FIGURE 9.0

STEP GENERAL TIMING

The ST506 SEEK COMPLETE signal will go false 100 nanoseconds after the leading edge of the step pulse.

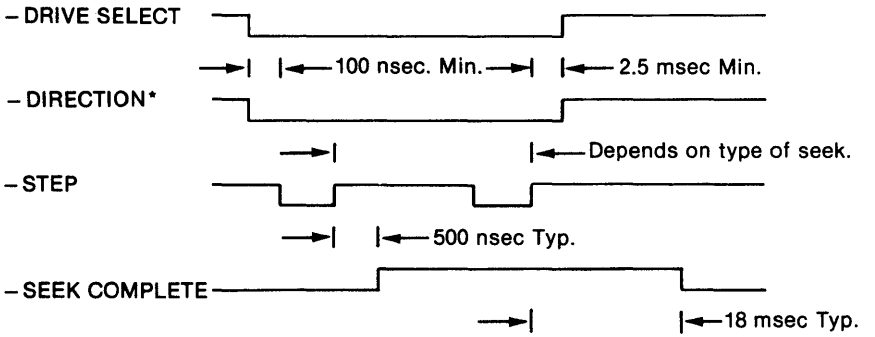


FIGURE 9.1

SLOW SEEK STEP PULSE TIMING

The read/write head will move at the rate of the incoming step pulses. The minimum time between successive steps is 3.0 ms.

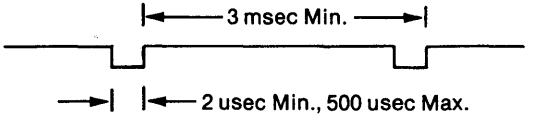
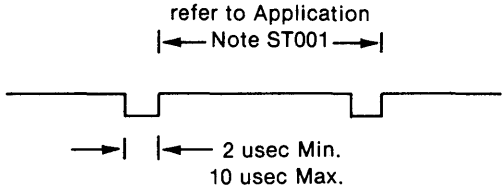


FIGURE 9.2

ALGORITHM DRIVEN SEEK



In order to better utilize the stepper motor's speed characteristics, the controller can issue step pulses at a rate faster than 3ms. This algorithm accelerates the motor to its maximum speed, steps it slightly less than the desired distance, and then decelerates it prior to arriving at the specified track. Employing this algorithm allows access time to be reduced considerably while maintaining a 15ms settling time. For more information consult Seagate Technology Application Note - ST001

4.1.6 DRIVE SELECT 1-4 (see figure 14.0)

DRIVE SELECT, when a low level, connects the drive interface to the control lines. Cutting the appropriate shunts at IC position 6B will determine which select line on the interface will activate that drive. The following table indicates which DRIVE SELECT shunts must be cut.

DRIVE SELECT	CUT SHUNTS
DS 1	10-7,11-6, and 12-5
DS 2	9-8,11-6, and 12-5
DS 3	9-8,10-7, and 12-5
DS 4	9-8,10-7, and 11-6

4.2 Control Output Lines

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48mA at low level or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and the collector leakage current is a maximum of 250uA. Figure 8.0 shows the recommended circuit

All J1 output lines are enabled by the DRIVE SELECT line.

4.2.1 SEEK COMPLETE

This line will go to a low level or true state when the read/write heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when seek complete is false.

SEEK COMPLETE will go false in 3 cases:

1) A recalibration sequence is initiated (by drive logic), at power on, if the read/write heads are not over Track 0.

2) 500nsec. after the trailing edge of a step pulse or series of step pulses.

3) If +5volts or +12volts are lost momentarily but restored.

4.2.2 TRACK 0

This interface line indicates a low level or true state when the drive's read/write heads are positioned at cylinder zero (the outermost data track).

4.2.3 WRITE FAULT

This signal is used to indicate that a condition exists at the drive that may cause improper writing on the disc. When this line is at a low level or true, further writing is inhibited at the drive until the condition is corrected. Write fault cannot be reset via the interface.

Note: The controller should edge detect this signal.

There are four conditions detected:

a) Write current in a head without WRITE GATE active or no write current with WRITE GATE active and DRIVE SELECTED.

b) Multiple heads selected, no head selected or improperly selected.

c) DC voltages grossly out of tolerance.

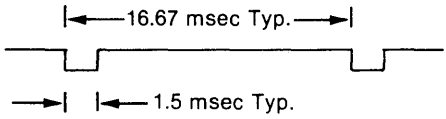
d) No SEEK COMPLETE, WRITE GATE, READY, and DRIVE SELECT.

4.2.4 INDEX (Figure 10.0)

This interface signal is provided by the drive once each revolution (16.67ms nom.) to indicate the beginning of a track. Normally, this signal is a high level and makes the transition to a low level to indicate INDEX. Only the leading edge is valid.

FIGURE 10.0

INDEX TIMING



4.2.5 READY

This interface signal when true together with SEEK COMPLETE, indicates that the drive is ready to read, write, or seek, and that the I/O signals are valid. When this line is false, all writing and seeking are inhibited.

The typical time after power on for READY to be true is 15 sec.

4.3 Data Transfer Lines

Two pairs of balanced signals are used for the transfer of data: WRITE DATA and READ DATA. These lines are differential in nature and may not be multiplexed. The WRITE DATA and READ DATE lines are on the J2/P2 connector on all drives. Figure 11.0 illustrates the proper driver/receiver combination.

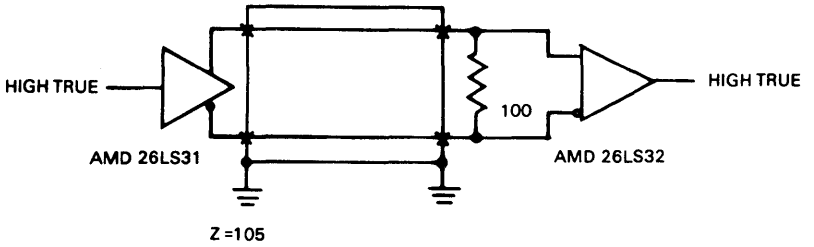
4.3.1 MFM WRITE DATA

This is a differential pair that defines the transitions to be written on the track. The transition of the + MFM WRITE DATA line going more positive than the – MFM WRITE DATA line will cause a flux reversal on the track provided WRITE GATE is active.

To ensure data integrity at the specified error-rate, the write data presented by the host must be pre-compensated on tracks 128 through 152. The optimum amount of pre-compensation is 12ns for both early and late written bits. Figure 12.0 shows the bit patterns to be compensated. All other patterns are written "on time."

FIGURE 11.0

DATA LINE DRIVER/RECEIVER COMBINATION



FLAT RIBBON OR TWISTED PAIR
MAXIMUM 20 FEET

NOTE: ANY EIA RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE.

FIGURE 12.0

WRITE PRECOMPENSATION PATTERNS

PREVIOUS		SENDING	NEXT	
X	0	1	1	WRITE DATA LATE
X	1	1	0	WRITE DATA EARLY
1	0	0	0	WRITE CLOCK LATE
0	0	0	1	WRITE CLOCK EARLY

X-Denotes a don't care state.

Writing should occur out of a shift register which is used to observe the pattern. "On time" represents a nominal delay. Early and late represent less and more delay respectively.

4.3.2 MFM READ DATA

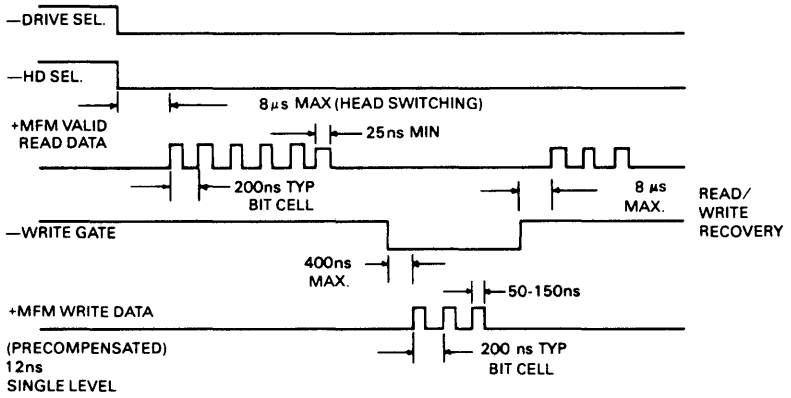
The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the −MFM READ DATA line represents a flux reversal on the track of the selected head.

4.3.3 READ/WRITE TIMING

The timing diagram as shown in Figure 13.0 depicts the necessary sequence of events (with associated timing restrictions) for proper read/write operation of the drive.

FIGURE 13.0

READ/WRITE DATA TIMING



4.4 DRIVE SELECTED

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by A TTL open collector driver as shown in Figure 8.0. This signal will go active only when the drive is programmed as drive x (x = 1,2,3, or 4) by cutting the shunt on the drive. The DRIVE SELECT X line at J1/P1 is activated by the host system.

4.5 CUSTOMER OPTIONS (Figure 14.0)

4.5.1 Radial Operation Option

The radial operation option is implemented via the option shunt block located at IC position 6B on the main circuit board. As shipped, the 14 pin shunt block (16 pin socket) is plugged in pins 2-15, leaving pins 1 and 16 open. This results in a daisy chain operation. Outputs are not active until the drive is selected. Moving the shunt block one position, to use pins 1 and 16, results in radial operation. In this case, all output signals are active, even if the drive is not selected. However, in this case, the front panel LED will not be on. Drive select must be active to light the LED.

4.5.2 "D" (Defeat Recal) Operation

As shipped, the "D" shunt, pins 2-15, is shorted. In this case, whenever a power up sequence is performed, the heads will automatically be repositioned to Track Ø. Cutting the D shunt will defeat the automatic recal operation, allowing the drive to become "Ready" earlier. However, during power up, the stepper circuitry will always put phase "A" active. Thus, there is no guarantee that the drive heads will be positioned at the same cylinder as existed when the drive was powered down. It will start at the same track only if the track corresponded to one which utilizes phase A. When using this option, issuing a Read ID command would allow determination of the active address, and could be used to initialize a present track address register.

4.5.3 "H" (Half Step) Option

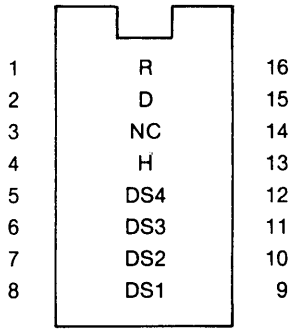
As shipped, the "H" shunt, pins 4-13, is shorted. In this case step pulses are applied to the interface at an interval of 3 milliseconds as shown in Figure 9.0. Cutting the "H" shunt allows a significant decrease in access time when used in conjunction with a simple software algorithm supplied by the user (refer to Figure 9.2). For detailed implementation information, contact the Technical Support Dept. for Application Note ST-001 (ST Part Number 36001-001).

4.5.4 Nylon Ground Washer

The ST506 main control PCB is grounded to the drive casting via the Index sensor. In some grounding configurations, it may be advisable to ground the Main Control PCB directly to the sideframes by removing the nylon washer from the screw that is in the upper corner of the Main Control PCB next to connector J2/P2.

FIGURE 14.0

OPTION SHUNT BLOCK



DS1,DS2,DS3,DS4 = DRIVE SELECTED
R = RADIAL OPERATION
D = Defeat Auto Recal
H = Half Step Option

Note: Jumper shorted is active condition for DS1, DS2, DS3, DS4, and R.
Jumper open is active condition for H and D.

5.0 Physical Interface

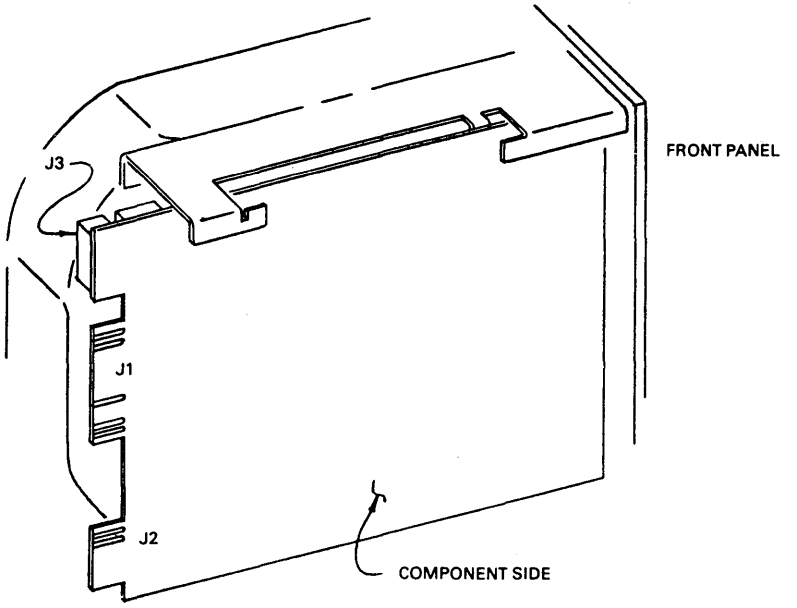
The electrical interface between the ST506 and the host controller is via four connectors:

1. J1-Control signals (multiplexed)
2. J2-Read/write signals (radial)
3. J3-DC power input
4. J10-Frame Ground

Refer to Figure 15.0 for connector locations.

FIGURE 15.0

INTERFACE CONNECTOR PHYSICAL LOCATIONS



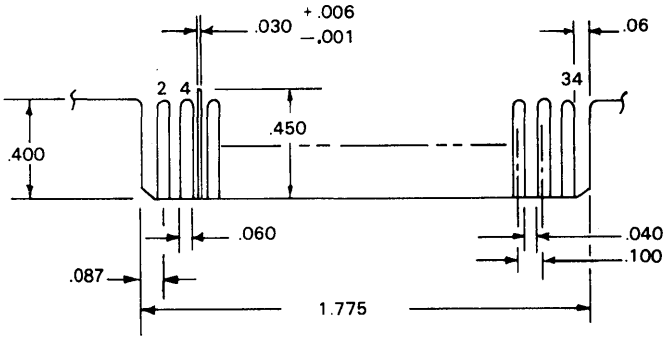
5.1 J1/P1 Connector-Control Signals

Connection of J1 is through a 34 pin edge connector. The dimensions for this connector are shown in Figure 16.0. The pins are numbered 1 through 34 with the even pins located on the component side of the PCB. Pin 2 is located on the end of the connector closest to the DC power connector J3/P3 and is labeled. The recommended mating connector for P1 is AMP ribbon connector P/N 88373-3 or Molex 15-35-1341. All odd pins are ground.

A key slot is provided between pins 4 and 6.

FIGURE 16.0

J1 CONNECTOR DIMENSIONS



Unless noted, .xx = ±.030, .xxx = ±.010

BOARD THICKNESS
.062 + .007

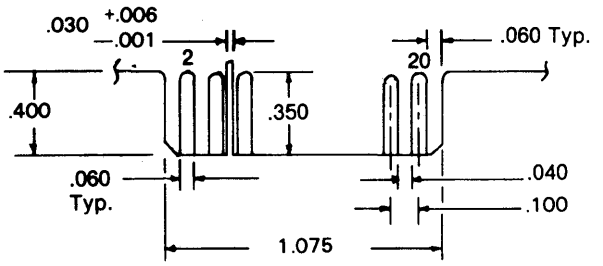
5.2 J2/P2 Connector-Data Signals

Connection to J2 is through a 20 pin edge connector. The dimensions for the connector are shown in Figure 17.0. The pins are numbered 1 through 20 with the even pins on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector P/N 88373-6, or Molex P/N 15-35-1201.

A key slot is provided between pins 4 and 6.

FIGURE 17.0

J2 CONNECTOR DIMENSIONS



5.3 J3/P3 Connector-DC Power

DC power connector (J3) is a 4 pin AMP Mate-N-Lok connector P/N 350211-1 mounted on the solder side of the PCB. The recommended mating connector (P3) is AMP P/N 1-480424-0 utilizing AMP pins P/N 350078-4 (strip) or P/N 61173-4 (loose piece). J3 pins are numbered as shown in Figure 18.0.

Current requirements and connector pin numbers are shown in Table IV.

FIGURE 18.0

J3 CONNECTOR-DRIVE PCB SOLDER SIDE

TABLE IV

DC POWER REQUIREMENTS

J3 CONNECTOR	CURRENT (AMPS)	
	MAXIMUM	TYPICAL
PIN 4 +5 VOLTS DC ±5% PIN 3 +5 VOLTS RETURN	1.0	0.7
PIN 1 +12 VOLTS DC ±5% PIN 2 +12 VOLTS RETURN	3.5*	1.6

*Occurs only during power up, per Table V.

5.4 J10/P10 Frame Ground Connector

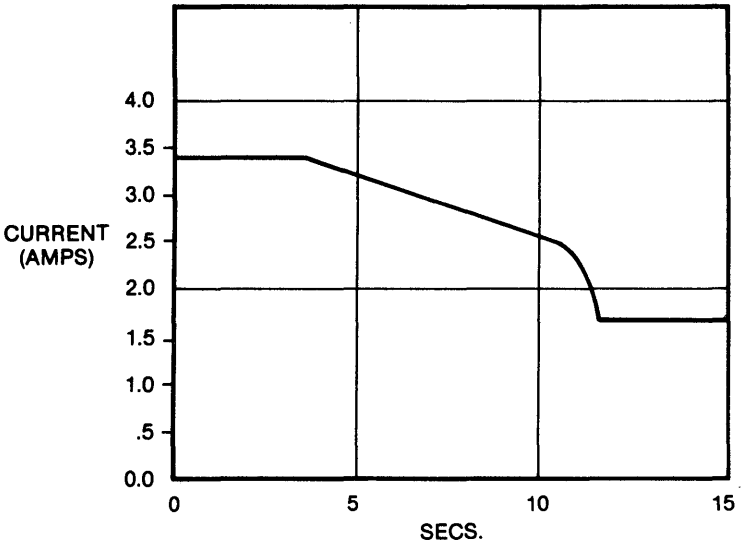
Faston AMP P/N 61761-2

Recommended mating connector AMP 62187-1

If used, the hole in J10 will accommodate a wire size of #18 AWG.

TABLE V

MOTOR START CURRENT REQUIREMENTS



+ 12V POWER-UP CYCLE

6.0 **Physical Specifications**

This section describes the mechanical dimensions and mounting recommendations for the ST506 disc drive.

6.1 Mounting Orientation

Recommended orientation is vertical on either side, or horizontal with the PCB down. The only prohibited orientation is horizontal with the PCB up. In the final mounting configuration, the four shock mounting screws must not extend more than 0.09 inches inside the frame at maximum travel.

6.2 Mounting Holes

Eight mounting holes, four on the bottom and two on each side are provided for mounting the drive to an enclosure. Position and dimensions for these holes, shown in Figure 19.0, are identical to the industry standard minifloppy drive.

6.3 Physical Dimensions

Overall height, depth and other key dimensions are shown in Figures 19.0 and 20.0. As in the case of the mounting holes, the dimensions are identical to the minifloppy, allowing a direct physical replacement.

FIGURE 19.0

MOUNTING PHYSICAL DIMENSIONS

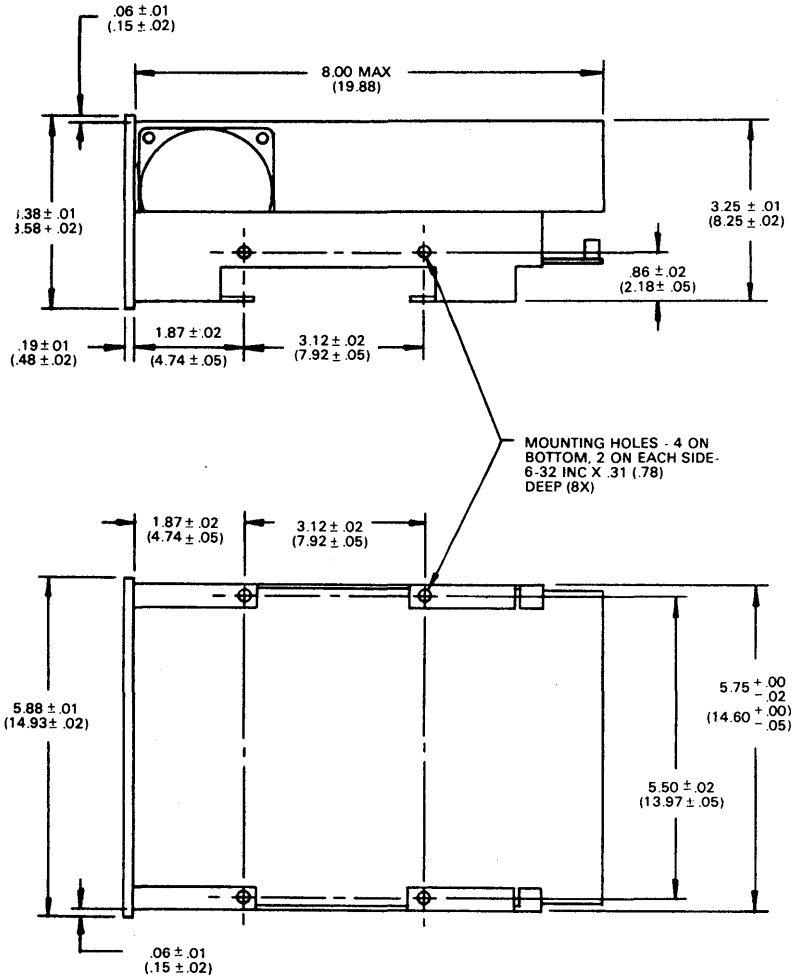
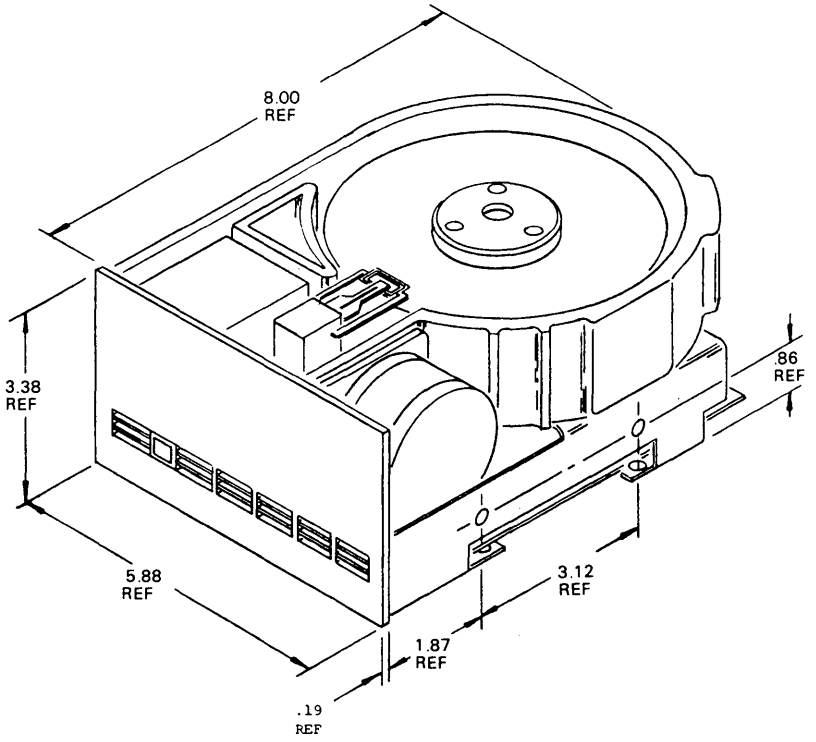


FIGURE 20.0
OVERALL PHYSICAL DIMENSIONS



7.0 Track Format

The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors. The format is a soft sectored type which means that the beginning of each sector is defined by a prewritten identification (ID) field which contains the physical sector address plus cylinder and head information. The ID field is then followed by a user supplied data field. The format also has four parts or "gaps" that are used for mechanical compensations and read/write synchronization.

The Seagate shipping format is a slightly modified version of the IBM System 34 double density format which is commonly used on floppy disc drives. The encoding method is Modified Frequency Modulation (MFM).

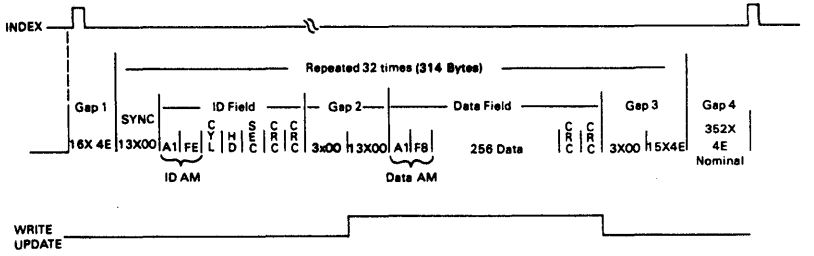
The beginning of both the ID field and the data field are flagged by unique characters called address marks. Each address mark is two bytes in length. The first byte is an "A1" data pattern. The second byte of the address mark is used to specify either an ID field or data field.

The "A1" pattern is made unique by violating the encoding rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination that could occur on the track. See Figure 22.0's depiction of the "A1" byte. Each ID and data field is followed by a 16 bit cyclic redundancy check (CRC Fire Code = $x^{16} + x^{12} + x^5 + 1$) character that is unique for each data pattern.

FIGURE 21.0

TRACK FORMAT EXAMPLE

32 SECTORS PER TRACK



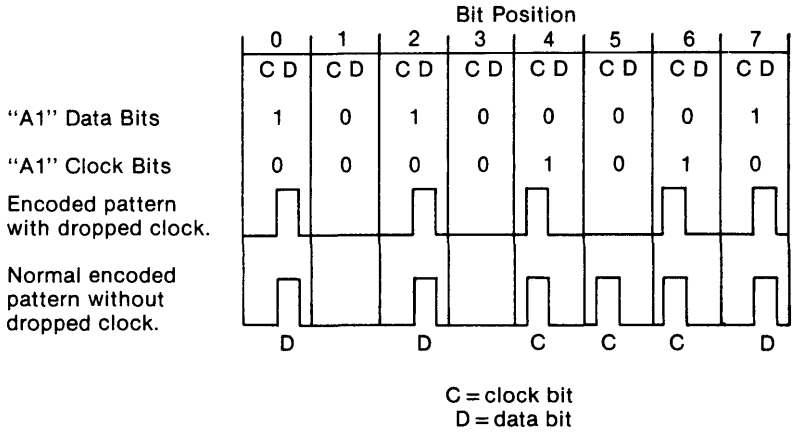
NOTES: 1. Nominal Track Capacity = 10416 Bytes

2. Total Data Bytes/Track = 256 x 32 = 8,192

3. CRC Fire Code = $x^{16} + x^{12} + x^5 + 1$

FIGURE 22.0

"A1" ADDRESS MARK BYTE



C = clock bit
D = data bit

7.1 Gap 1

Gap 1 is to provide for variations in Index detection. As shipped, gap 1 is 16 bytes long, but must be at least 12 bytes. Gap 1 is immediately followed by a sync field preceding the first ID field.

7.2 Gap 2

Gap 2 follows the CRC bytes of the ID field, and continues to the data field address mark. It provides a known area for the data field write splice to occur. The latter portion of this gap serves as the sync up area for the data field address mark. Minimum length required is determined by the "lock up" performance of the phase-lock-loop in the data separator, which is part of the host controller.

7.3 Gap 3

Gap 3 following each data field allows for spindle speed variations. This allows for the situation where a track has been formated while the disc is running faster than normal, then write updated with the disc running slower than normal. Without this gap, or if it is too small, the sync bytes or ID field of the next field could be overwritten. As shipped, the gap allows a ±3% speed variation (actual drive spec is ±1%).

7.4 Gap 4

Gap 4 is a speed tolerance buffer for the entire track, which is applicable in full track formatting operations to avoid overflow into the index area. The format operation which writes ID fields begins with the first encountered index and continues to the next index. The actual bytes in Gap 4 depends on the exact rotating speed during the format operation.

7.5 Defective Sector Flags

A printout will be provided with each drive which lists the location of defects in terms of head number, cylinder number, sector, and byte. No unit will be shipped to customers if surface analysis identifies more than 4 hard errors per surface. No errors will be present on cylinder 0.

Testing for defects involves an analysis of the total media surface under marginalized test conditions.

Seagate Publication: 36036-001
920 Disc Drive, Scotts Valley, California 95066-4544, USA