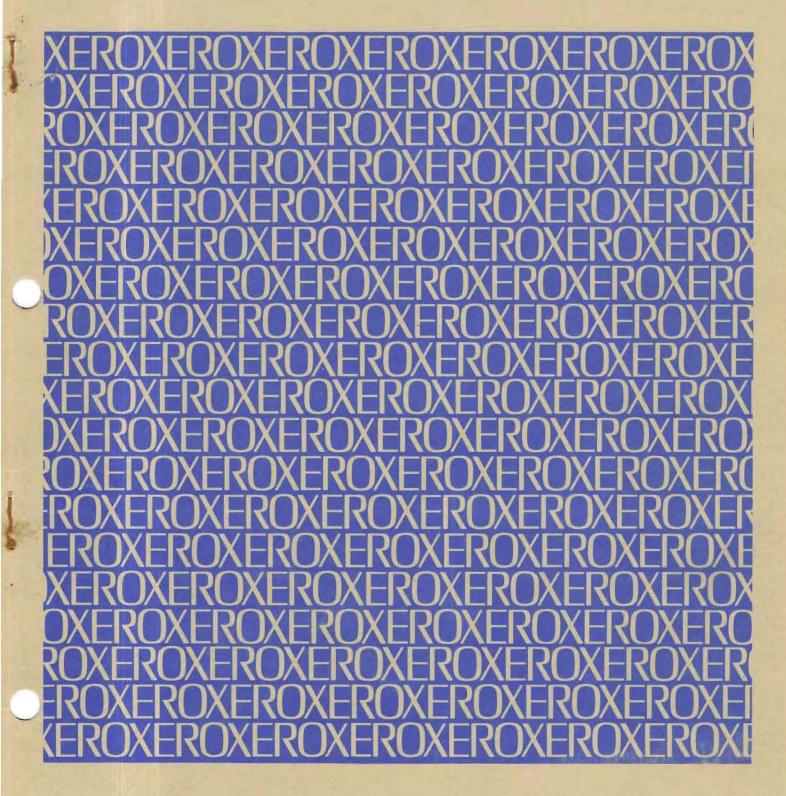
Xerox Removable Disk Storage System

Models 7275/7276

Reference Manual



DISK PACK ORDER CODES

Hexadecimal Code	Function
01	Write
02	Read 2
03	Seek
04	Sense
05	Check-write
07	Reserve
09	Header Write
0A	Header Read
0F	Condition Release Interrupt
12	Read 1
13	Select Test Mode
17	Release
lF	Condition Release Interrupt (and set a CIL on device release)
33	Restore Carriage
83	Seek (and cause a device interrupt on positioning complete or Seek timeout error)
B3	Restore Carriage (and cause a device interrupt on positioning complete)

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Xerox Removable Disk Storage System

Models 7275/7276

Reference Manual

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RELATED PUBLICATIONS

Title	Publication No.
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Xerox Sigma 7 Computer/Reference Manual	90 09 50
Xerox Sigma 8 Computer/Reference Manual	90 17 49
Xerox Sigma 9 Computer/Reference Manual	90 17 33
Xerox Stand-Alone Systems/OPS Reference Manual	90 10 53
Xerox Symbol/LN, OPS Reference Manual	90 17 90
Xerox Meta-Symbol/LN, OPS Reference Manual	90 09 52
Xerox Macro-Symbol/LN, OPS Reference Manual	90 15 78

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<u>Manual Content Codes:</u> BP – batch processing, LN – language, OPS – operations, RP – remote processing, RT – real-time, SM – system management, TS – time-sharing, UT – utilities.

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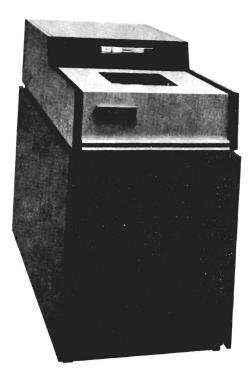
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Model 7277 Removable Disk Storage Unit

1. GENERAL DESCRIPTION

INTRODUCTION

The Xerox Models 7275/7276 Removable Disk Storage System provides high-volume, random-access storage. It is a moving-arm (head), removable-medium, rotating disk system available for use with Sigma 5-9 computers.

Model 7275 consists of a controller and three 86-million byte disk drives, providing a starter capacity of more than 258 million bytes of storage. Model 7276 consists of a controller and seven 86-million byte disk drives. A maximum of 15 Model 7277 disk drives, each providing over 86 million bytes of storage, can be added to the system to allow a total on-line capacity of 1291 million (1 billion, 291 million) bytes of storage. The optional addition of one Model 1043 controller and a Model 1044 dual access feature for each drive provides dual access to the system (see Chapter 4, "Dual Access Considerations"). The Model 7279 disk pack, an 11-high, 19-surface disk pack is the removable storage medium. (See Table 1.)

To use this manual effectively, the reader must be familiar with the applicable Xerox Sigma Computer Reference Manual, particularly the discussions of input/output instructions and input/output operations.

The particular features of the removable disk system include the following:

- Voice coil head positioner provides an average 30 msec cylinder access time.
- 2. Operation and failure interlock system assures operational system integrity.
- Dual access (optional) allows simultaneous read/read, read/write, or write/write on any two spindles in a set of 15.
- 4. Hardware write-protect assures total file protection of the entire spindle.
- Independent Seek operations allows overlapping of Seek operations to minimize access time on multiple spindle systems.

SYSTEM COMPONENTS

A system consists of some combination of the following components:

Model No.	Component	Prerequisite Component
7275	Disk controller with three 86-million byte disk drive units.	

Model No.	Component	Prerequisite Component
7276	Disk controller with seven 86-million byte disk drive units.	
1043	Additional controller allowing access of 7275/ 7276 disk drives, if dual access feature is installed (optional).	7275/7276
1044	Dual access feature – one required for each Model 7277 disk drive (optional).	7275/7276/ 7277
7277	Additional 86-million byte disk drive unit – maximum of 15 per 7275/7276 system (optional).	7275/7276
7279	Removable disk pack.	

Table 1. Characteristics

Operating Characteristics							
Recording format	1024 bytes/sector						
	11 sectors/track						
	404 tracks/surface ^t						
	19 recording surfaces, plus one positioning servo surface.						
Recording method	Track serial						
Mode	Modified frequency modulation (MFM)						
Recording frequency	6.45 Mhz						
Rotational speed	3600 rpm						
Model 7277 spindle capacity (sectored)	86, 048, 768 bytes						
On–line 7275/7276 capacity (sectored)							
Minimum	258/602 million bytes						
	al seven spare tracks per surface recording surface is flawed.						

Table 1. Characteristics (cont.)

Rotational

Instantaneous

(multiple sectors)

Model 1043 Controller (standard Sigma cabinet)

Height

Width

Depth

Weight

Model 7277 disk

Height

Width

Depth

Weight

drive

(per sector)

Average

latency

Transfer rates

Operating Characteristics (cont.)						
Maximum (15 additional units per controller)	1291 million bytes					
Nominal access (positioning) time						
Seek	30 msec average (10-55 msec)					

806K bytes/second

675.7K bytes/second

Physical Characteristics

63.5 in.

31.5 in.

35.5 in.

770 lbs.

39.5 in.

22 in.

44.5 in.

700 lbs.

8.33 msec average (0-17 msec)

Table 1. Characteristics (cont.)

Environme	ntal Characteristics
Power requirements	
Model 1043	120/208 vac, 60 Hz; three– phase. Requires 3737 watts power at a power factor of 0.7.
Model 7277	208 vac, 60 Hz or 220 vac, 50 Hz, three-phase. Re- quires 1.3 kw power at a power factor of 0.7.
Operating Temperature	60° to 90°F (15° to 32°C)
Operating humidity (relative)	25% to 80%
Cable length	
IOP to controller	40 ft. maximum
Controller to disk drives	160 ft. maximum
Operating and Physical (Characteristics of Removable Volume
Model 7279 disk pack	
Disks/pack	11
Usable recording surfaces/pack	19
Disk surface coating	Magnetic oxide
Disk surface diameter	14 in.
Disk pack canister diameter	15 in.
Disk pack canister height	7.06 in.
Weight	16 lbs.

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2. FUNCTIONAL DESCRIPTION

DATA PRESENTATION

Data is transferred between the controller and the I/O system on a four-byte interface (32-bit data path). The four-byte feature must be installed on the IOP. All controllers time share and interface between the collective controllers and the IOP. Please note that throughout this manual, "IOP" refers to the Selector Input/Output Processor (SIOP) on Sigma 5-7 systems, and the Multiplexor Input/ Output Processor (MIOP) on Sigma 8 and Sigma 9 systems. (An SIOP operates on a single-byte interface.) Data is transferred between the controller and the disk pack unit serially, two bits at a time (i.e., via a two-bit data path).

DISK SYSTEM STATES

There are four device conditions and one device mode. The conditions are

- 1. "Not operational".
- 2. "Ready".
- 3. "Busy".
- 4. "Not available" (reserved for use with devices that are accessible to more than one controller).

The mode is always automatic. Condition and mode combine to define device state, of which there are two:

- 1. "Ready automatic".
- 2. "Busy automatic".

The initial state of the device depends on its power status. Complete absence of power removes the device from the controlling system (i.e., no address recognition). If power is applied to the controller, address recognition occurs when an I/O instruction is issued.

For single CPU configurations, the disk pack system is always in "automatic release", as long as it is in the operational state. When dual CPUs can access a device, the disk system is never in automatic release; see "Dual Access Considerations" in Chapter 4.

OPERATIONAL STATES

The disk pack system reports the "operational" state if the I/O address is recognized and the device is operational as defined below.

- 1. Disk speed is within operating limits.
- 2. Temperature is within operating limits.

- 3. All interlocks are closed.
- 4. All power is normal in the controller and disk storage units.
- 5. No fault condition exists within a disk storage unit.

When operational, an SIO instruction will be accepted if

- 1. The addressed controller/device is ready.
- 2. The device is "available", that is, not reserved by another controller.
- 3. No channel interrupts are pending.

In response to the SIO, HIO, and TIO I/O instructions, the condition of the disk pack system at any time is returned to the central processor. The TDV and AIO I/O instructions obtain other specific indications of device status (see "Status Response" in Chapter 3).

READY CONDITION

In the "ready" condition, the controller can accept an SIO instruction if the addressed device is available and the system is free of pending channel interrupts. To become ready, the device must be operational and there must be no order execution in progress or pending.

BUSY CONDITION

In the "busy" condition, the controller has accepted an SIO instruction. It will not accept a new order until the current order (or orders) is completed.

UNAVAILABLE CONDITION

In the "unavailable" condition, the device is reserved by another controller; therefore, it cannot accept an SIO instruction.

TRANSITIONS BETWEEN STATES

Table 2 summarizes the state transitions and the event (events) required to cause them.

Table 2. Device State Transitions

Present State	Next State	Event
Ready automatic	Busy automatic	Acceptance of SIO instruction.
Busy automatic	Ready automatic	HIO instruction received, I/O Reset signal re- ceived, or oper- ation associated with last order completed.

DATA TRANSFER

An operation is initiated from the controlling system by an SIO instruction if the following qualifications are met:

- 1. There is I/O address recognition.
- 2. Device and controller are in "ready" condition, and no channel interrupt is pending.
- 3. Device is "available".

If these qualifications are met, the controller enters the "busy" condition and initiates the transfer of data to or from the disk pack unit as specified by the order. The data transfer continues until the required number of bytes have been transferred. The operation then terminates, and the device returns to the "ready automatic" state.

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3. PROGRAM INTERFACE

DISK PACK ORGANIZATION

Each disk pack (see Figure 1) consists of 11 disks with 19 usable recording surfaces. (The outside surfaces of the top and bottom disks are not usable, and one additional surface is used as a positioning servo.) Each surface has its own read/write head mounted in a comb assembly on a movable arm; the 19 heads are aligned in the same vertical plane and move as a unit through the stack, although only one head is reading or writing at any time. Recording head numbers range from 0 through 18.

Each recording surface is logically divided into 11 sectors numbered 0 through 10, and 411 concentric circles or tracks on which data is recorded. The tracks begin (are numbered) at the periphery of a disk and progress inward towards the center. Each vertically-aligned set of 19 tracks in the stack is referred to as a cylinder. Thus there are 411 cylinders in a disk pack, numbered 0 through 410. Cylinder 000, for example, consists of track 000 on surface 0, track 000 on surface 1, and so on through track 000 on surface 18.

The range of values in the fields of the disk address are summarized as follows:

Field	Range
Cylinder	⁰⁻⁴¹⁰ 10
Head	0-18 ₁₀
Sector	⁰⁻¹⁰ 10

DATA ORGANIZATION

Data is stored in groups of 1024 bytes. Each data group has a unique address composed of its device, cylinder, head, and sector number. Each data group is preceded by a header containing the cylinder, head, and sector number for the group. The header is used for address identification and verification.

HEADERS

Before data can be written on the disk, special records called headers that identify the addresses of all data groups (sectors) must be written. The header data received from the IOP (see "Header Write (X'09')", later in this chapter) comprises a flaw byte; head, sector, and cylinder addresses; and alternate head and cylinder addresses. Headers are used in locating the desired data group (sector) and in address verification when successive data groups are written or read. Failure to acquire a given address results in a verification error. When the program detects a flawed tracks, it must write a flaw mark (X'FF') in the flaw byte in all 11 sector headers of the track. A defective or flawed track is one in which an error has been consistently detected on successive write and then read operations. When the controller detects a flaw mark in a header, it terminates any read or write operation by indicating "unusual end". Note that the current sector address is not incremented for any unusual termination while the header is being read. Therefore, the alternate head and cylinder addresses are normally obtained from the "flawed header" by issuing a Header Read order (see "Header Read (X'OA')", later in this chapter) directly after the flaw is encountered. A new Seek order is not required in this case.

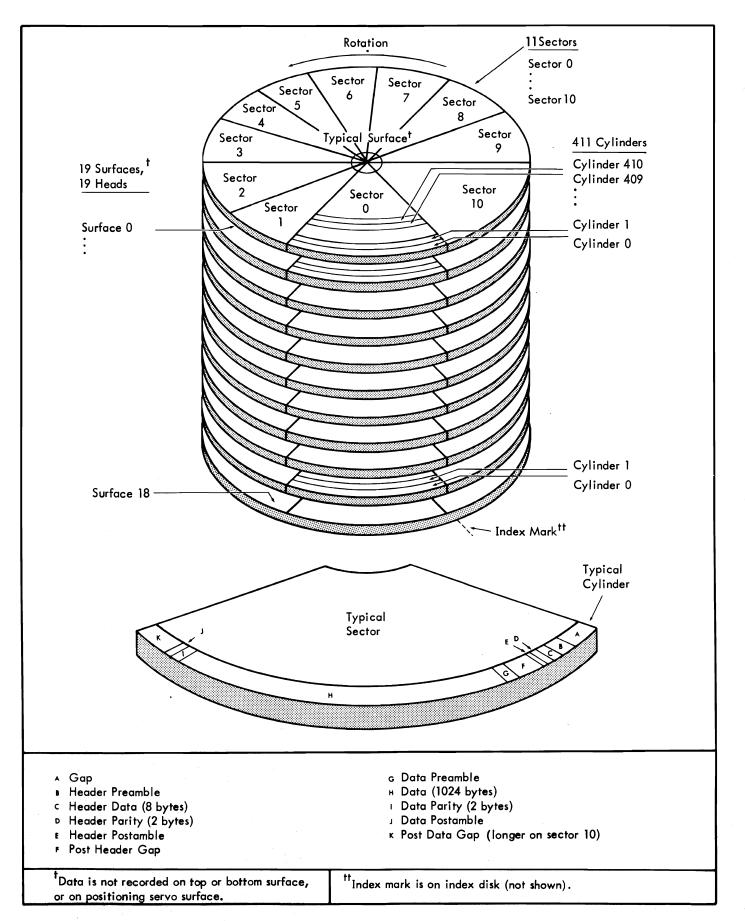
DATA ACCESS

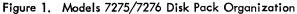
To select a device for any operation, the I/O instruction must contain an address specifying the device controller address and the device address. The Model 7275 is a multidevice controller; consequently, the controller address lies in the range 8_{16} through F16, and device addresses in the range 0_{16} through F16. Note that device address F16 is for the controller and can be used for any I/O instruction intended for the controller alone (SIO, HIO, TIO, and TDV).

To address a particular data group (sector) for reading or writing, the program must first issue a Seek order to the device to select the desired cylinder (move the heads into place), head, and sector. After reading or writing a sector, the controller automatically increments the sector address to the next sector in sequence. Upon completing the last sector of a track, the controller sets the sector address to zero and increments the head address to the next head in sequence (in the cylinder). Thus a single I/O order can cause a number of sequential sectors or tracks to be read or written. When the end of a cylinder is reached, the program must issue a new Seek order to the controller to select the next cylinder, since the controller does not automatically increment to the next cylinder.

CHECK CHARACTERS

The controller computes and writes a two-byte check character at the end of each header and at the end of each sector data field. When a header is read, the controller recomputes and compares the check characters with those read; any difference causes an "unusual end" termination. Similarly, when data is read, the controller also recomputes and compares the check characters with those read;





however, in this case, the controller signals "transmission error" and not "unusual end". (See also "I/O Fault Detection and Recovery Actions" in Chapter 4.)

DEVICE ORDERS

When the controller successfully completes the execution of an SIO instruction or a command chain, it makes a onebyte order-out service call to the IOP to obtain the I/O order for the next operation.

The following list shows order decoding of the I/O orders described in the subsequent sections. Any other code in the order byte is treated as an invalid order, as is a detected order parity error, and terminates with "unusual end". Note that all orders to device address X'F' (except in a Condition Release Interrupt order or a Select Test Mode order) are rejected.

	Binary Representation Bit Positions							Hexadecimal	
Order	0				-	5	6	7	Code
Header Write	0	0	0	0	1	0	0	1	X'09'
Seek	м	0	0	0	0	0	1	1	X'83', X'03'
Write	0	0	0	0	0	0	0	1	X'01'
Check–Write	0	0	0	0	0	1	0	1	X'05'
Header Read	0	0	0	0	1	0	1	0	X'0A'
Read 1	0	0	0	1	0	0	1	0	X'12'
Read 2	0	0	0	0	0	0	1	0	X'02'
Restore Carriage	м	0	1	1	0	0	1	1	X'B3', X'33'
Reserve	0	0	0	0	0	1	1	1	X'07'
Release	0	0	0	1	0	1	1	1	X'17'
Condition Release Interrupt	0	0	0	M	1	1	1	1	X'1F', X'0F'
Select Test Mode	0	0	0	1	0	0	1	1	X'13'
Sense	0	0	0	0	0	1	0	0	X'04'

The "M" represents a modifier bit that, when set, has specific indications for any order in which it can appear.

HEADER WRITE (X'09')

The Header Write order causes the controller to consider all subsequent data bytes as header information. Header size is eight bytes. The header format is defined as follows:

		Byte 0 Byte 1						Byte 1								Byte 2							B	yt	е	3					
		F	Flaw)-		_			0	Cylinder				(00	0		ŀ	le	ad						
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7

Byt	e 4	Byte 5	Byte 6	Byte 7
0—0	Sector	Alternate	Address	00
0 1 2 3	4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6	701234567

where

- flaw represents flaw byte and is written with all ones (X'FF') in every sector header of a track in which a flaw is detected. If there are no flaws, the flaw byte contains all zeros.
- cylinder represents current cylinder address.
- head represents current head address.
- sector represents current sector address.
- alternate address represents a field normally used to contain the address of an alternate cylinder and head to be used should this sector be marked flawed. (Set by software only.)

A single Header Write order can write a maximum of one cylinder of headers. Header writing continues until terminated by one of the following conditions:

- 1. "Count done" is signaled.
- The device becomes "not operational". The Header Write terminates with an "unusual end".
- The address increments to an out-of-bounds address; the head number is past the end of the cylinder. The programming error (bit 2) status of TDV is indicated and the Header Write is terminated with "unusual end".
- 4. A rate error (data overrun) is detected. The operation terminates with a "transmission error".
- 5. I/O Reset occurs or an HIO instruction is executed. The Header Write terminates without further communication to the IOP.
- 6. IOP Halt is indicated to the controller. If the terminal order indicating IOP Halt occurs prior to the order-in, the controller indicates "unusual end" in the order-in

and proceeds to the "ready" state. If the terminal order indicating IOP Halt occurs at the order-in, the controller proceeds to the "ready" state without further communication with the IOP.

- An output data parity error is detected from the IOP. The Header Write is immediately terminated with a "transmission error".
- 8. A write-protect signal is received from the device. The Header Write terminates with an "unusual end".

SEEK (X'83',X'03')

The Seek order alerts the controller to request a four-byte disk address from the IOP, as illustrated below. The controller then directs any subsequent data transmission operation to begin at this address.

Byte 0	Byte 1	Byte 2	Byte 3
00			0—0 Sector
0 1 2 3 4 5 6	7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7

where

- cylinder represents cylinder number and can be in the range $0 \le$ cylinder \le 410.
- head represents head number and can be in the range $0 \le head \le 18$.
- sector represents sector number and can be in the range $0 \le \text{sector} \le 10$.

Both seek forward and seek reverse operations are possible. The difference between any seek and successor seek is stored in bytes 14 and 15 of the data retrievable from the execution of a Sense order (see "Sense (X'04') later in this chapter).

A byte count of less than four causes the controller to signal "incorrect length" in the appropriate status byte for the I/O instruction, without completing the Seek operation. If the byte count exceeds four, the Seek operation is performed using the first four bytes transferred; however, "incorrect length" is still signaled. In either case, an "unusual end" termination occurs.

When bit 0 (modifier bit) of the Seek order is set (X'83'), a device interrupt is initiated when the positioning system indicates positioning is complete (on-cylinder) or a Seek timeout error (i.e., positioning error – heads are retracted to sector zero) has occurred. The interrupt call is made at the beginning of the sector prior to the one specified by the Seek operation. If the call is not acknowledged before the beginning of the next sector, it is withdrawn until the next revolution of the disk. The receipt of an SIO, HIO, TIO, or TDV instruction for another device causes the interrupt call to be withdrawn temporarily. However, if the controller is "busy" when the device signal is received, the interrupt call to the IOP is postponed until the controller is not "busy".

Seek orders can be issued successively to several devices, and each device will interrupt as it completes its operation. After the controller has sent the last communication to the device to initiate the Seek operation, it executes order-in to the IOP, and proceeds to the "ready" state. The device then stays "busy" until the heads are in position, even though it is not selected by the controller. See also "Seek and Restore Operations" in Chapter 4.

WRITE (X'01')

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The Write order causes the controller to begin writing data on the file at the current disk (file) address. Note that if the specified byte count to be written is not a multiple of the sector record length, "incorrect length" is indicated and writing does continue. Writing begins only after the header is read and the address verified, and continues until terminated by any of the conditions listed below:

- 1. Count done is signaled coincident with "end-of-sector" (i.e., after writing a record on a sector).
- Count done was received, the remainder of the sector was written with zeros, and the check character was written.
- I/O Reset occurs or an HIO instruction is executed. Writing terminates and the controller immediately becomes "ready", without further communication with the IOP.
- 4. A terminal order indicating IOP Halt occurs in the order-in sequence; the controller becomes "ready" without further communication with the IOP.
- 5. An output data parity error is detected from the IOP; the operation terminates with "transmission error".
- 6. A data overrun is detected; the operation terminates with "transmission error".
- 7. The disk system becomes "not operational"; termination indicates "unusual end".
- 8. The controller head address increments past the end of the cylinder. The sector "unavailable" status bit (bit 2 of TDV status) is set to 1, and termination indicates "unusual end".
- 9. A header flaw mark, incorrect header parity, or a verification error is encountered. The current sector address is preserved (is not incremented). Termination indicates "unusual end".

- A write-protect signal is received from the device; termination indicates "unusual end".
- 11. A terminal order indicating IOP Halt occurred before
 order-in; the controller indicates "unusual end" in the order-in and becomes "ready".

CHECK-WRITE (X'05')

The Check-Write order causes the controller to compare bytes read from disk storage with bytes received from the IOP. Check-write errors terminate the operation with "transmission error" at the completion of the sector. Note that if the byte count is not a multiple of the sector length, "incorrect length" is indicated.

The comparison continues until terminated by one of the following conditions:

- 1. Count done signal is received.
- The disk pack system becomes "not operational". Check-writing terminates with an "unusual end" indication.
- 3. The address increments to an out-of-bounds address; the incremented controller head number is past the end of the cylinder.
- 4. A rate error is detected; check-writing terminates with a "transmission error".
- 5. Data bytes do not compare or an error is encountered in the data check character. The order-in indicates "transmission error".
- 6. I/O Reset occurs or an HIO instruction is executed. Check-writing terminates and the controller proceeds immediately to "ready" without further communication with the IOP.
- 7. IOP Halt is indicated to the controller. If the terminal order indicating IOP Halt occurs prior to the order-in, the controller indicates "unusual end" in the order-in and proceeds to "ready". If the terminal order indicating IOP Halt occurs within or after the order-in sequence, the controller proceeds to "ready" without further communication with the IOP.
- The controller encounters a flaw mark or incorrect header parity in a header, or a verification error. The current disk (file) address is preserved (is not incremented).
- 9. The controller detects an IOP output parity error.
- 10. An output data parity error is detected from the IOP; the operation terminates with "transmission error".

HEADER READ (X'OA')

The Header Read order causes the controller to start reading headers beginning at the current disk address. The byte count must specify a multiple of the header record length. A maximum of 209 headers (one cylinder) can be read with a single Header Read order.

The Header Read continues until terminated by one of the following conditions:

- 1. Count done signal is received.
- 2. The device becomes "not operational". The Header Read terminates with an "unusual end" indication.
- 3. The address increments to an out-of-bounds address; the incremented controller head number is past the end of the cylinder. The illegal address fault (in byte 8, obtained with a Sense order) is indicated, and the Header Read operation terminates with "unusual end".
- 4. A rate error is detected. The Header Read operation terminates with "transmission error.
- 5. I/O Reset occurs or an HIO instruction is executed. Header Read terminates without further communication to the IOP.
- 6. IOP Halt is indicated to the controller. If the terminal order indicating IOP Halt occurs before the order-in, the controller indicates "unusual end" in the order-in and proceeds to the "ready" state. If the terminal order indicating IOP occurs at the order-in, the controller becomes ready without further communication with the IOP.
- 7. Detection of either a verification error or a header parity error terminates the operation with "unusual end" after the current record ("errored" header) has been transferred to the IOP with the current sector address preserved.
- 8. Detection of a flaw mark sets bit 1 of the TDV device status byte and reading continues.

READ 1 (X'12')

The Read 1 order causes the controller to begin reading bytes from the disk storage at the current disk address in the controller and to transmit the bytes to the IOP. Please note that data check byte errors are reported following the sector in which they occurred. Such errors are reported as "transmission errors" at I/O termination. Sector integrity is determined from the check bytes written at the end of each sector. "Incorrect length" is set in the operational status byte if the byte count is not a multiple of the sector record length. Prior to reading data from the sector and sending it to the IOP, the controller verifies the disk address by reading headers until it locates the one with the requested sector number. If a flaw mark is detected in any header, if a check byte error is detected, or if cylinder, sector, or head numbers do not compare with those stored in registers, then an "unusual end" occurs and no data is read. The pertinent TDV status bits are set to indicate a flaw mark, header check byte error, or verification error (see Table 5).

Reading is initiated at the start of the addressed sector and is continued until any of the following occur:

- 1. Count done signal is received coincident with the end of the sector and the check character has been read and compared.
- 2. Count done signal is received prior to the end of the sector. The controller reads the remaining bytes (but does not transmit them to the IOP), and reads and compares the check characters.
- 3. The disk pack system becomes "not operational". Reading terminates with an "unusual end".
- The address increments to an out-of-bounds address; the incremented controller head number is past the end of the cylinder.
- 5. A rate error (data overrun) is detected. Reading terminates with a "transmission error".
- 6. The controller encounters a check character that does not successfully compare. Termination occurs at the end of the sector in error (for the Read 1 order described in this section, or is deferred until the count done signal is received, as described below for Read 2). At read termination, "transmission error" and not "unusual end" is set in the appropriate status byte for the I/O instruction.
- I/O Reset occurs or an HIO instruction is executed. Reading terminates and the controller proceeds immediately to "ready" without further communication with the IOP.
- 8. IOP Halt is indicated to the controller. If the terminal order indicating IOP Halt occurs prior to the order-in, the controller indicates "unusual end" for the order-in and proceeds to "ready" without further communication with the IOP.
- 9. A verification error is encountered. The read operation is terminated with "unusual end", and the current file address is preserved (is not incremented).
- The controller encounters a flaw mark or incorrect header parity in a header. The read operation is terminated with "unusal end" and the file address is not incremented.

READ 2 (X'02')

The Read 2 order causes the controller to read and transmit bytes to the IOP from the disk storage at the current disk address in the controller. Sector data check byte errors are reported following the sector in which count done occurs. Otherwise, the operation is exactly as described in the previous section, "Read 1 (X'12')".

RESTORE CARRIAGE (X'B3',X'33')

The Restore Carriage order causes the controller to issue a return-to-zero signal to the addressed device; it is generally used when the exact location of the carriage becomes unknown. Internal registers are cleared, the heads are returned to cylinder zero, and no data bytes are transferred. An interrupt call is made at the beginning of the sector prior to sector zero if the order modifier bit is set (i.e., order code is X'B3'). A device interrupt is initiated when positioning is complete. (See also "Seek and Restore Operations" in Chapter 4.)

RESERVE (X'07')

For a single-CPU system, the Reserve order causes the controller to select and reserve the designated device and then to release it. For a dual-CPU system, this order causes the responsible controller to select and reserve the designated device. Because an SIO instruction and all orders cause the controller to automatically select and reserve a device, the use of the Reserve order is superfluous. (See also "Dual Access Considerations" in Chapter 4.)

RELEASE (X'17')

The Release order causes the controller to issue a release control signal to the addressed dual access device, thereby releasing that device for use by the other controller. If the device has only a single access capability (i.e., remains reserved to channel A), the controller still executes the Release order; however, no useful operation results. (See also "Dual Access Considerations" in Chapter 4.)

CONDITION RELEASE INTERRUPT (X'1F', X'0F')

The Condition Release Interrupt order is meaningful only for dual access systems. When a controller receives a "released" signal (which means the other controller has released the device), a device interrupt occurs. If the order modifier bit is set (i.e., order code is X'1F') a controller makes an interrupt request (CIL) if it receives a "released" signal from any device. If the modifier bit is not set (X'0F'), a controller does not generate any release interrupts. The program must use SIO device address X'F' to initiate this order, thereby permitting the Condition Release Interrupt mark in the controller to be set even if all devices are busy.

An HIO instruction with device address X'F' resets the release interrupt mark and any pending release interrupts. A reset signal received from the IOP also resets the release interrupt mark.

SELECT TEST MODE (X'13')

For diagnostics only. The Select Test Mode order alerts the controller to request two bytes of data from the IOP and puts the controller in test mode. The first data byte, byte 0, specifies the test mode (or modes) and forced error conditions under which subsequent operations will be performed. The second data byte, byte 1, is a test byte that specifies the device type and the device diagnostic conditions.

Byte 0

Bits	
0 1 2 3 4 5 6 7	Function
0 0 0 0 0 0 0 0	Invalid test order.
x x x x 0 0 0 1	Enter buffer test mode.
x x x x x 0 1 0	Enter controller test mode.
x x x x x 1 0 0	Enter device test mode.
x x x x 1 x x 0	Enter incremental clock test mode.
x x x 1 x x x x	Force device I/O parity error.
× × 1 × × × × ×	Force read data error.
x l x x x x x x	Force IOP input parity error.
1 × × × × × × ×	Force IOP output parity error.

Byte 1 Bits Function

0-4 Diagnostic test condition for the device.

5-7 Device type code: The bits will be set to 111 (7₁₀) for this disk drive. Required only for controller test mode.

The Select Test Mode order must be issued with device address X'F' (the controller address). The controller can be released from test mode by an HIO instruction or by manual reset.

BUFFER TEST MODE

Buffer test mode allows testing of the data path between the IOP and the controller. The 32-byte controller buffer can be filled by a Write order and read back to the IOP by a Read order. The controller indicates end-of-data after the 32nd byte has been transferred. By using controller address X'F', no device is necessary to execute buffer test mode tests.

CONTROLLER TEST MODE

Controller test mode allows testing of the controller without operating a device. This mode tests approximately 90 percent of the controller logic. All subsequent orders can be exercised in a normal or incremental clock mode; control signals to the device are blocked. For data-in type operations the byte counter simulates data; for write (data-out) operations the written data are lost. By using controller address X'F', no device is necessary to execute controller test mode tests.

DEVICE TEST MODE

Device test mode provides a means for performing special diagnostic tests of the device and controller. All normal interface and controller sequences are operative except that the device nonoperational state does not cause sequences to be terminated with "unusual end", nor does it prohibit use of an SIO instruction. These exceptions allow status to be collected from the device and device commands to be issued to the device while the device is nonoperative. The controller can be operated in an incremental clock mode, thereby allowing the diagnostic program to check each phase of a Seek operation as it occurs.

Note that in the device test mode, "implicit reserve and explicit release" is in effect for the controller, thus allowing the diagnostic program to test "implicit reserve and explicit release" without actually installing a ground jumper (on pin 06C44) to disable the automatic "implicit reserve and explicit release" feature. (See "Dual Access Considerations" in Chapter 4.)

INCREMENTAL CLOCK TEST MODE

Incremental clock test mode allows the program to step through the controller sequences by issuing TDV instructions. This feature allows the diagnostic program to take snapshots of controller and device responses to normal operating sequences. Each TDV with an X'F' device address advances the sequence one step. All other TDV device addresses operate in the normal test mode as described in the section "TDV Instruction in Test Mode", later in this chapter.

FORCE DEVICE I/O PARITY ERROR

This feature allows a diagnostic program to test the address decoding logic and error reporting of any device. A "one"

in bit 3 of the test byte (byte 0) forces a parity error in the output address lines to the device.

FORCE READ DATA ERROR

This test feature allows testing of the controller's check byte (parity) generation and detection, and its reporting logic. A "one" in bit 2 of the test byte forces a one-bit error in a read operation. Bit positions 0 and 1 of the first byte of any sector being read is forced to a "zero" state. This condition occurs for either simulated data (Controller Test Mode) or data from the device (Device Test Mode). The forcing of data errors exercises the parity logic in the controller; a check byte error detection may be exercised.

FORCE IOP INPUT PARITY ERROR

This feature allows a diagnostic program to test the controller's parity generator and computer reporting logic. A "one" in bit 1 of the test byte forces a zero on the parity line to the IOP.

FORCE IOP OUTPUT PARITY ERROR

This feature allows a diagnostic program to test the controller's parity checking and reporting logic for data transfers from the IOP. A "one" in bit 0 of the test byte forces the simulation of a "one" on the parity line from the IOP.

TDV INSTRUCTION IN TEST MODE

During the period the controller is in test mode, the TDV instruction becomes a diagnostic instruction that allows the CPU to monitor controller and device operations and to issue certain diagnostic device commands. The least significant four bits of the device address portion of the instruction points to the data source to be transferred to the IOP during the TDV. Device addresses 0 through B are used for diagnostic device commands if the controller is in Device Test Mode. In this case the address and status buses from the device are monitored for status. The actual device operated and tested in Device Test Mode is the one addressed by the last SIO, TIO, or HIO instruction. If the controller is in the Controller Test Mode, no communication to the device occurs.

A detailed discussion of the use of TDV under test conditions is beyond the scope of this manual. Note that should a program accidentally get into test mode due to a hardware error or a programming error, condition code bits 1 and 2 (CC1 and CC2) have the values 0 and 1, respectively, in all responses to TIO and TDV.

SENSE (X'04')

The Sense order causes the controller to transfer to the IOP up to 16 bytes of information that describe the controller's and device's current state. The sense orders are timed to be initiated at the start of a sector. This feature provides that approximately the time of one sector period elapses before the start of the next sector after the current angular position (sector position) is transferred to the IOP. The 16 bytes are described as follows:

Byte O	Byte 1	Ву	yte 2	В	yte 3				
w 00	Cylinder	000	Head	000	Sector				
0 1 2 3 4 5 6 7 10 1 2 3 4 5 6 7 10 1 2 3 4 5 6 7 10 1 2 3 4 5 6									
Byte 4	Byte 5	Ву	∕te 6	В	yte 7				
M R Position									
0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2	3 4 5 6 7	0 1 2	3 4 5 6 7				
Byte 8	Byte 9	Ву	te 10	Ву	/te 11				
Faults	Faults		Seek Moo	difier	Bits				
0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2	3 4 5 6 7	0 1 2	3 4 5 6 7				
Byte 12 Byte 13 Byte 14 Byte									
Check	Diff€	erence							

where

- W represents write-protect bit. If set, this bit indicates the current address is write-protected.
- cylinder represents current nine-bit cylinder address stored in the device.
- head represents current head address stored in the device.
- sector represents current sector address stored in the device.
- M represents modifier bit. This bit is set when the arm is in motion. In this case, the file is inaccessible.
- R represents reserve/release mode. Bit 1, if set, indicates that "implicit reserve, explicit release" is in effect, and if reset (zero) indicates "implicit reserve and release" is in effect. (See "Dual Access Considerations" in Chapter 4.)
- angular position represents current angular position — a sector number. When angular position equals sector address, the data file can be accessed.
- configuration represents configuration data. Bit 0, if set, indicates the addressed device has the dual access feature. Bits 1–3 contain the device type code, i.e., 111₂ for this disk drive. Bits 4–7 contain the device physical address, which may differ from the logical address.

dev	ice st rece	atus represents the diagnostic device status ived from the device, as listed below.	<u>B</u>
	Bit	Meaning	,
	0	Device fault (voltage drop occurred).	9
	1	Write fault.	
	2	Head positioning fault (loss of on-cylinder).	9

- 3 Offset polarity (used for checking head alignment).
- 4 Air flow loss occurred.
- 5 Parity error detected on device ID byte sent from controller.
- 6 Spindle speed fault.
- 7 Positioning servo fault.

faults these two bytes contain diagnostic fault data that is described below. This information is contained within the controller and indicates various faults that resulted in "transmission errors" or "unusual end" terminations. These data are accumulative and are cleared only by execution of this Sense order or by manual reset.

Byte	Bit	Meaning			
8	0	Check-write error.			
8	1	Data check byte error.			
8	2	IOP parity error.			
8	3	Rate error (data overrun).			
8	4	Head address incremented out of limits while attempting a Read or Write order.			
8	5	Arm in motion error – Seek order received while device arm in motion.			
8	6	Order parity error detected.			
8	7	Test mode order error — invalid test mode or incorrect length of test data bytes.			
9	0	Seek address transfer verification comparison error detected during Seek, Read, Check-write or Write order.			
9	1	Device "unavailable" operational error or "not operational" signal detected from device by the con- troller, or seek error during Read or Write sequence.			

Byte	Bit	Meaning			
9	2	Head address verification error detected.			
9	3	Sector address verification error detected.			
9	4	Cylinder address verification error detected.			
9	5	Not defined.			
9	6	Channel address error detected.			
9	7	Missing on-sector signal from device during multisector Read or Write op- eration; or missing read or write clock, command strobe, or status re-			

Seek modifier bits represent either Seek modifier bits, or Restore Carriage modifier bits. Bit 0 of byte 10 represents device address 0 and bit 6 of byte 11 represents device address X'14'. A "one" set in any bit position means an interrupt is pending when the device reaches "on-cylinder" (positioning is complete) or Seek timeout.

quest acknowledgement from device.

- Check bytes represent the last check bytes received by the controller from any device.
- difference represents the difference (absolute value) last computed by the controller during a Seek order execution. The least significant bit is bit 7 of byte 15.

KEY EVENTS

The following key events can occur during a disk I/O operation:

Start of I/O 1.

- 2. Unusual end error condition.
- 3. Channel end error condition.
- Transmission error condition. 4
- 5. Incorrect length error condition.

These key events are described in the following sections. Assume no chronological order of occurrence from the order here presented, for none is intended. For what generally occurs is that I/O is started, and sometime subsequently terminated with an interrupt. The interrupt is queried to determine whether it was device-generated (and indicating successful completion) or generated because of an error (unsuccessful termination), or by a timeout occurrence (hardware malfunction – generally recoverable).

START INPUT/OUTPUT

An I/O operation begins with the execution of an SIO instruction by the controlling system. If the I/O address is recognized and the device is "ready" and "available", the controlling system sets its "I/O address recognition" and "SIO accepted" indicators. The device advances from the "ready" to the "busy" condition. It then requests an I/O order byte from the controlling system and proceeds with the operation defined by the order byte.

UNUSUAL END CONDITIONS

Unusual end always results in a TDV status bit being set to indicate a means of recovery. After an order is received, the detection of any of the following conditions causes the device to signal "unusual end" to the controlling system:

- 1. An out-of-range or illegal Seek address.
- 2. Receipt of Seek order while arm in motion.
- 3. Invalid order or order parity error.
- 4. Device becomes "not operational" while the controller is "busy".
- Incorrect header parity, or a verification error for devices that use headers during a Read, Write, Checkwrite, or Header Read order operation. (The current address is not incremented.)
- 6. IOP Halt signaled.
- 7. Flaw byte encountered during a Read, Write, or Checkwrite order operation.
- Seek timeout (positioning error) occurs when controller receives a Seek, Read, Write, Check-write, Header Read, or Header Write order.
- 9. Incorrect length on Seek, Header Read, or Sense order.
- 10. Device interface error detected by controller.
- 11. Write-protect violation.
- 12. Control signal or address IOP parity error.

CHANNEL END CONDITIONS

"Channel end" is signaled with each order-in. The order-in takes place after the occurrence of any of the following conditions:

- 1. "Count done" signal received during a Sense order.
- 2. The controller executes a Seek order to a device.
- 14 Key Events

- 3. The check character bytes are written in the last sector for a Write or Header Write order following a "count done" signal.
- 4. Receipt of check character bytes of the last sector of a Header Read or Check-write order following a "count done" signal.
- 5. Receipt and execution of a Restore Carriage, Release, Select Test Mode, or Condition Release Interrupt order.
- 6. Detection of an IOP data-out parity error.
- 7. Detection of data overrun (rate error).
- 8. After reading the check bytes during a Read 1 or Check-write order that has a "transmission error".
- 9. Detection of an "unusual end" condition.

TRANSMISSION ERROR CONDITIONS

The controller signals "transmission error" to the controlling system upon detecting any of the following conditions:

- 1. Failure of an end-of-sector check bytes check during a Read or Check-write operation.
- 2. Failure of data comparision during a Check-write operation.
- 3. Data overrun (rate error).
- 4. An IOP data-out parity error.

INCORRECT LENGTH CONDITIONS

The controller detects "incorrect length" errors and reports them to the controlling system for any of the following conditions:

1. A byte count other than four was specified in a Seek order.

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- 2. A byte count other than an integral multiple of the sector data record (1024 bytes) was specified for a Read, Write, or Check-write order.
- 3. A byte count other than a multiple of the sector header record (eight bytes) was specified for a Header Write or a Header Read order.
- 4. A byte count of 0 or greater than 16 was specified for a Sense order.

STATUS RESPONSE

The I/O instructions can request a device to return detailed I/O status information when the instruction is executed. Detailed descriptions of the Sigma I/O instruction are in the Sigma Computer Reference Manuals; summary status information is discussed in the following sections and related tables and figures.

CONDITION CODES

When an I/O instruction is executed, condition code bits 1 and 2 are set to describe the general status of the addressed I/O device and controller. (Condition code 3 is also meaningful for an I/O instruction; when set, it means either the status returned in the registers is not reliable or the status has not been returned to the registers; when reset (zero), it means the status information is reliable. Note, however, that the device and controller do not influence CC3 – the IOP does.) Table 3 lists the CC1 and CC2 settings and their significance for the I/O instructions.

Table 3. Condition Code Settings

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I/O Instruction	CC1	CC2	Significance
SIO	0	0	I/O address recognized and SIO accepted.
	0	1	I/O address recognized, SIO not accepted.
	1	0	Not applicable.
	1	1	I/O address not recognized.
HIO	0	0	I/O address recognized and device not "busy" when halt occurred.
	0	1	I/O address recognized and de- vice "busy" when halt occurred.
	1	0	HIO not accepted; controller "busy" with device other than one addressed.
	1	1	I/O address not recognized.
TIO	0	0	I/O address recognized and SIO can currently be accepted.
	0	1	I/O address recognized, but SIO cannot be currently accepted.
	1	0	Not applicable.
	1	1	I/O address not recognized.

I/O Instruction	CC1	CC2	Significance			
TDV	0	0	I/O address recognized.			
	0	1	Device controller in test mode.			
	1	0	Controller busy with a device other than one addressed.			
	1	1	I/O address not recognized.			
AIO	0	0	Normal interrupt recognition,			
	0	1	Unusual condition [†] , interrupt condition, or controller is switched to a test mode.			
	1	0	Not applicable.			
	1	1	No interrupt recognition.			
^t An unusual condition is one in which the Seek timeout error, unusual end, or transmission error storage elements						

were set in the previous operation.

DEVICE STATUS BYTE

A device status byte is returned to the register when an I/O instruction is executed. This byte also describes the status of the addressed device and its controller, but in more detailed fashion than do CC1 and CC2. The significance of each bit is shown in Tables 4, 5, and 6.

The device status byte is set at the beginning of an SIO, TIO, or HIO instruction. It is set as the result of a TDV instruction. For an SIO, it is set upon receipt of the instruction if there is an interrupt pending.

OPERATIONAL STATUS BYTE

In addition to the information returned in the device status byte, the operational status byte generated at the end of each SIO, HIO, TIO, and TDV instruction execution also provides indicators to the controlling system (see Table 7).

IOP STATUS BYTE

In place of an operational status byte, an AIO instruction returns an IOP status byte in the same bit positions of the register. Table 8 summarizes the meanings of the settings of these bit positions.

Bit Position	Function	Value	Meaning
0	Interrupt pending	1	Set if interrupt is pending (issued, but not acknowledged by an AIO instruction).
1,2	Device condition		Describes the current device condition as follows:
		00	Device "ready".
		01	Device "not operational".
		10	Device "unavailable" (reserved by other controller).
		11	Device "busy".
3	Mode	1	Always set to automatic mode.
4	Unusual end	1	Set if previous controller operation terminated with "unusual end".
5, 6	Controller condition		Describes the current controller condition as follows:
		00	Controller "ready".
		01	Controller "not operational".
		10	Not applicable.
		11	Controller "busy".
7	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.

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Table 4. Device Status Response for SIO, HIO, and TIO

Table 5. Device Status Response for TDV

Bit Position	Function	Value	Meaning
0	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.
1	Flaw detection	1	Flaw byte detected during Header Read, Write, Read, or Check-write.
2	Programming error	1	Invalid order detected; illegal address (address X'F' used for orders other than Select Test Mode or Conditional Release Interrupt); invalid Seek address; address incremented out of limits while attempting a Read or Write order; invalid test mode; Seek order received while arm was in motion; first seven bits of Seek order were not zero; or incorrect length detected for Seek, Sense, Header Read, or Header Write order.
3	Write protection	1	Write-protect violation.
4	Parity error (IOP)	1	Order parity error detected; Seek address parity error detected; even parity received on a terminal order; or IOP detected an address parity error (channel address parity error).

Table 5.	Device	Status	Response	for	TDV	(cont.)	,
	001100	010105	11000001100			(0001110)	ζ.

Bit Position	Function	Value	Meaning
5	Operational Error	1	Device interface error detected; missing an on-sector signal from device during a multisector Read or Write; missing Read or Write clock, command strobe, or status request acknowledgment from the device; detection of Seek address transfer verification comparison error during Seek, Read, or Write; device unavailable error or "not operational" signal detected from device by the controller; or a Seek error during a Read or Write.
6	Verification	1	Head address verification error detected; sector address verification error detected; or cylinder address verification error detected while reading a header.
7	Header check byte	1	Header check byte error.

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Table 6. Device and Controller Status Response for AIO

Bit Position	Function	Value	Meaning
0	Data overrun	1	Data overrun (rate error) has occurred during execution of the previous order.
1	Attention interrupt	1	Attention interrupt acknowledged.
2	Release interrupt	1	Release interrupt acknowledged.
3	Reser∨ed	0	This bit is currently zero; however, it may be used in future enhancements.
4 [′]	On-sector interrupt	1	On-sector interrupt acknowledged. Note that either bit 4 or bit 6 can be set; both cannot be set.
5	Reserved	0 .	This bit is currently zero; however, it may be used in future enhancements.
6	Seek timeout error interrupt	1	Seek timeout error interrupt acknowledged. See note for bit 4. If bit 6 is set, program must issue a Restore Carriage order and retry the previous operation.
7	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.

Table 7. Operational Status Byte for SIO, HIO, TIO, and TDV

Bit Position	Function	Value	Meaning
8	Incorrect length	1	Incorrect length condition has occurred.
9	Transmission data error	1	IOP or controller detected a parity error or data overrun in the transmitted information.
10	Transmission memory error	1	Memory parity error detected during a data I/O operation since last accepted SIO.

Table 7. Operational Status Byte for SIO, HIO, TIO, and TDV (cont.)

Bit Position	Function	Value	Meaning
11	Memory address error	1	Nonexistent memory address detected during a chaining operation or a data I/O operation.
12	IOP memory error	1	IOP detected a memory parity error while fetching a command.
13	IOP control error	1	IOP detected two successive Transfer in Channel commands.
14	IOP Halt	1	An error condition is detected that causes the IOP to issue a halt order to the addressed I/O device.
15	SIOP busy	0	Always zero for I/O instruction addressed to an MIOP.

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Table 8. IOP Status Byte for AIO

Bit Position	Function	Value	Meaning
8	Incorrect length	1	Incorrect length condition has occurred.
9	Transmission data error	1	IOP or controller detected a parity error or data overrun in trans- mitted information.
10	Zero byte count interrupt	1	Zero byte count is detected and zero byte count flag is set.
11	Channel end interrupt	1	Device reports channel end to the IOP and the channel end flag is set.
12	Unusual end interrupt	1	IOP reports unusual end to the device and the unusual end flag is set; or the IOP signaled IOP Halt to the device controller.
13-15	Not assigned	-	Setting is indeterminate; program should mask these bits.

4. PROGRAMMING CONSIDERATIONS

SEQUENCE OF ACTIVITY

Figures 2 through 16 summarily illustrate the sequential relationship of the main events that occur during disk pack operations.

COMMAND CHAINING

Command chaining is allowed during the intersector gap for changing the order or file address from one type to another, or another order of the same type. Loss of rotational latency may be avoided only if command chaining occurs between sectors 10 and 0. Chaining from a Read or Write to another Read or Write is not allowed if the end of the cylinder has been reached. At the end of a cylinder, a Seek or Restore Carriage order must be given before additional data can be transferred.

SURFACE FLAWING

When the program determines that a sector's data field is unusable because of a defective surface area, it must write flaw marks in the headers of the sectors of the associated cylinder and head where flaws are detected. (Note that the controller is designed to flaw single sectors.) The use of the alternate cylinder and head assignments fields of these headers is, of course, optional.

SURFACE OPERATIONS

Sector and head addresses are automatically incremented after a surface operation (Read, Write, etc.); however, the cylinder address is never automatically incremented. The program must issue a Seek order to cross cylinder boundaries to prevent an "unusual end" condition.

When the controller detects a flaw mark during a surface operation, automatic surface address incrementation is inhibited to allow for an immediate Header Read operation to obtain the alternate address.

Note that frequent TIO and TDV instructions during surface operations may cause data overrun conditions.

SEEK AND RESTORE OPERATIONS

The Seek operation can be performed only when the disk is on-cylinder. When the Seek modifier bit (bit 0) is set, an interrupt occurs when the minimum access position is reached. The interrupt can be used to maximize controller activity. When the modifier bit in a Restore Carriage order is set, an interrupt occurs when the head has completed movement thereby avoiding having to issue Seek orders during head movement. When Seek or Restore Carriage orders with the modifier bit set occur in a command list, the modifier bit is ignored and the on-sector interrupt is lost.

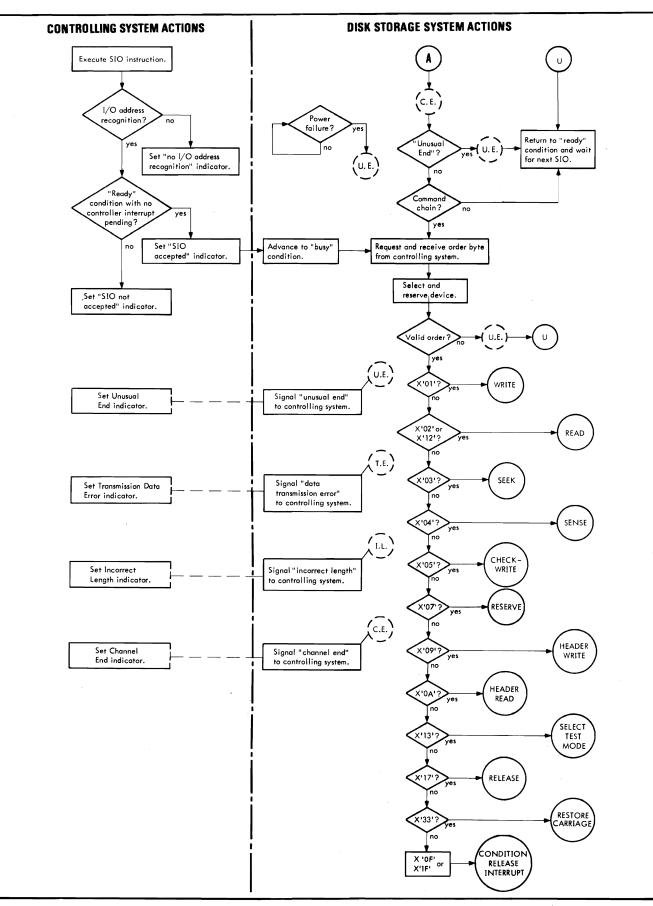
The on-sector interrupt has a window that is one sector ahead of the addressed sector. Thus it is possible for the condition code bits CC1 and CC2 of an AIO instruction to be set to a binary 11 configuration, indicating that no interrupt was recognized.

DUAL ACCESS CONSIDERATIONS

There are two types of dual access configurations possible: a single CPU with two controllers sharing a device or devices; and dual CPUs sharing a device or devices, each through a separate controller and with no status communications shared between the CPUs.

In the first case (single CPU), the disk system is always in automatic release and "implicit reserve and release" is in effect. This means that the device is always selected and reserved upon acceptance of an SIO instruction, and is not released until the controller goes "ready". Please note that it is not released during command chaining or data chaining. For the Restore Carriage order and Seek order, the controller automatically releases the device when the carriage first starts movement. This is when the controller is "ready" for another SIO; the device goes "on-cylinder" some time later. For other operations the controller automatically releases the device at the completion of each operation (at the time the controller goes "ready"). If a channel program is used that includes Seek and Read or Write orders, the device remains reserved throughout the operation; if a regular program is used that issues an SIO for each Seek and Read or Write order, the device is released between orders at channel end. Thus the Reserve and Release orders are not required and are effectively no-ops. If the Reserve and Release orders are used, they operate in this manner: an executed Release order first reserves the device and then issues a release.

In the second case (dual CPUs) the disk system is not in the automatic release and "implicit reserve, explicit release" is in effect. This means that the acceptance of the first SIO from either controller causes the pertinent controller to select and reserve the device, and that all orders automatically reserve the device. Thus the Reserve order is not required and is effectively a "no-op". The device remains reserved and must be explicitly released by some action: execution of a Release order, manual depression of I/O RESET or SYS RESET pushbuttons on the CPU control panel, switching of the reserving controller to off-line, or by power failure or shutdown in the reserving controller. The release interrupt is used to control the availability of the device to the two systems.

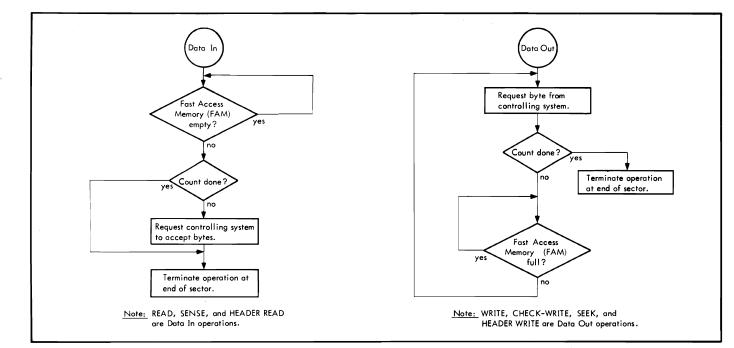


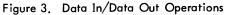
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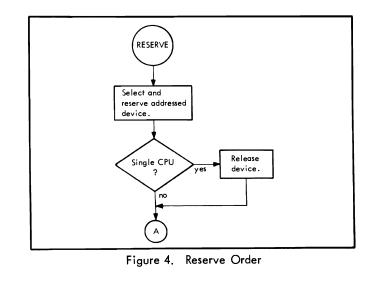
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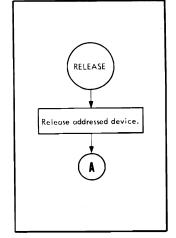
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Figure 2. Controlling/Disk Storage System Actions



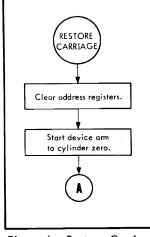




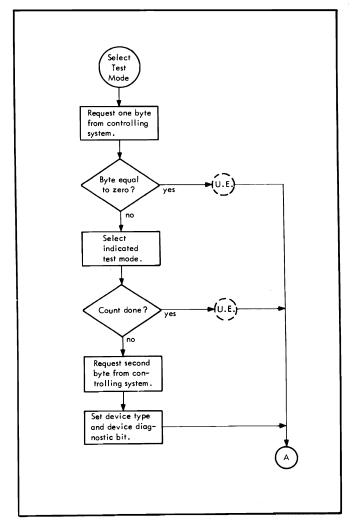


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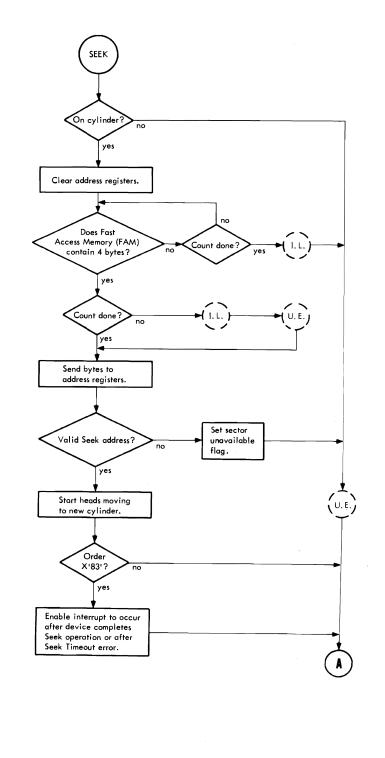
Figure 5. Release Order

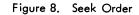


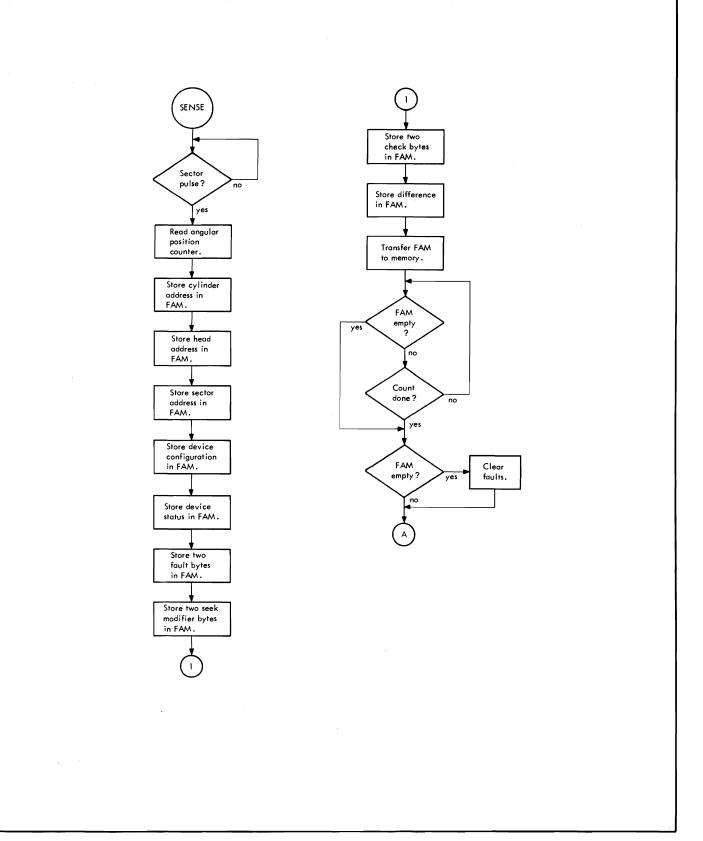












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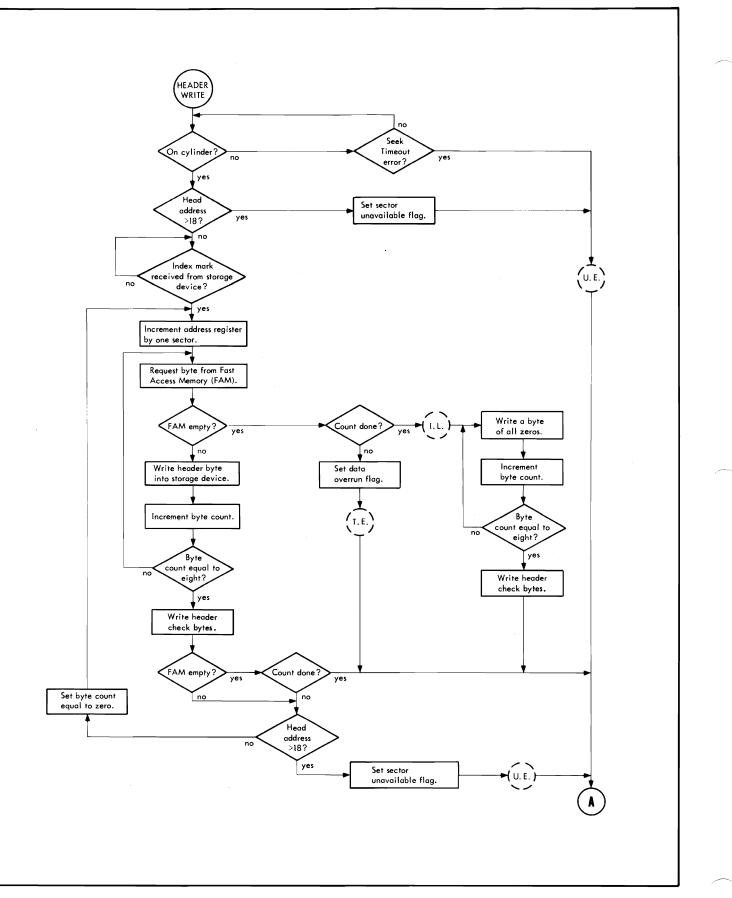


Figure 10. Header Write Order

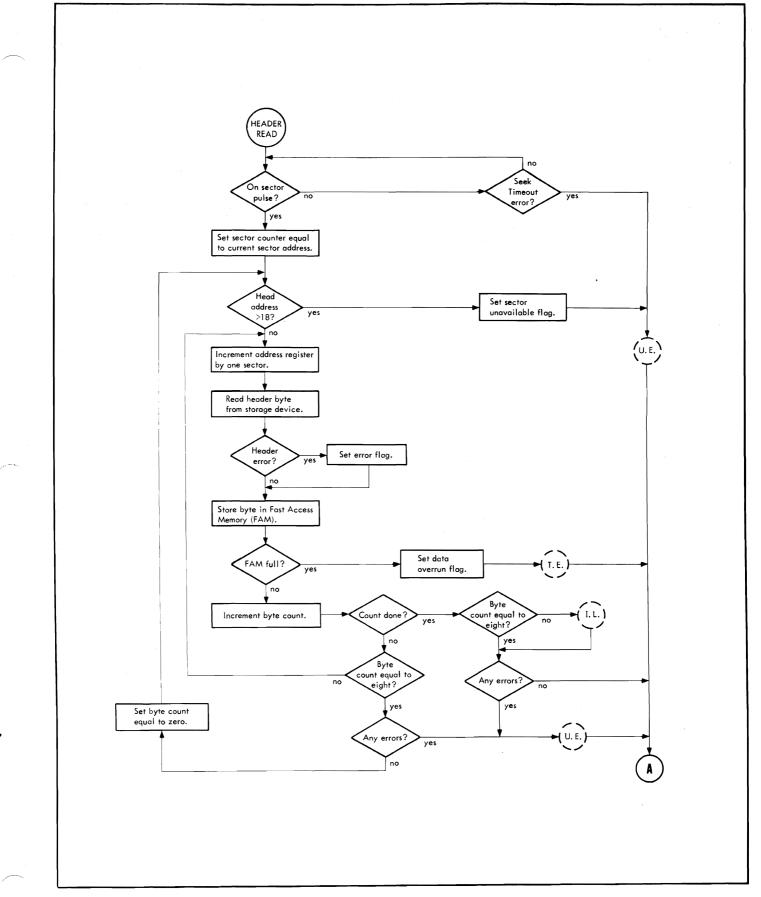
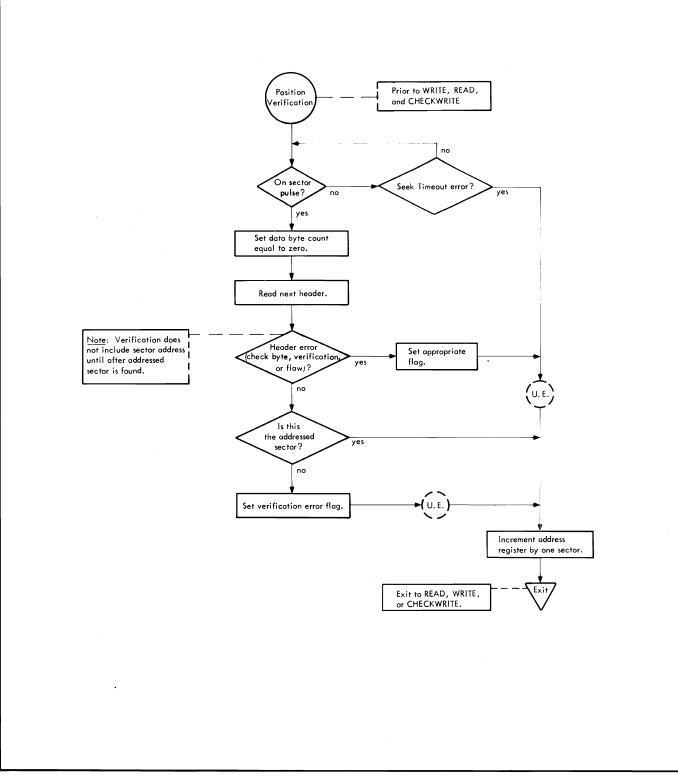
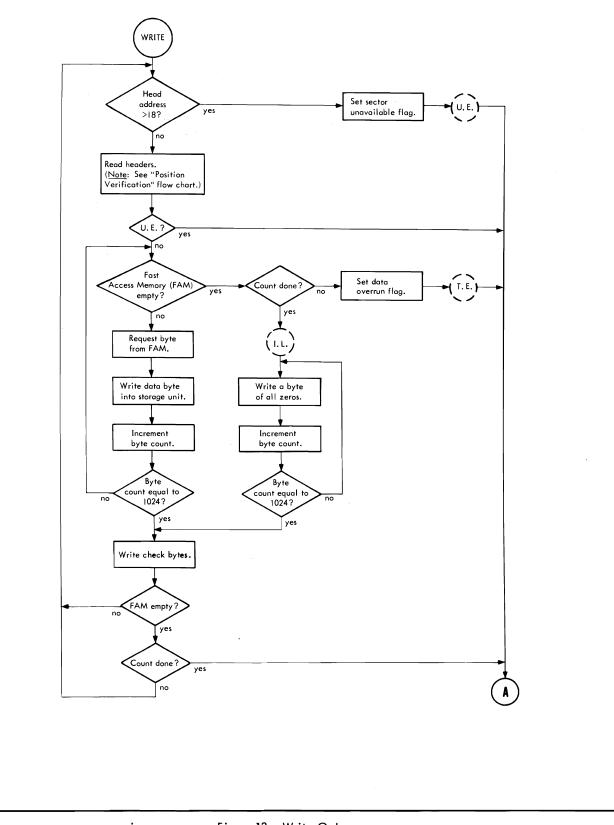


Figure 11. Header Read Order



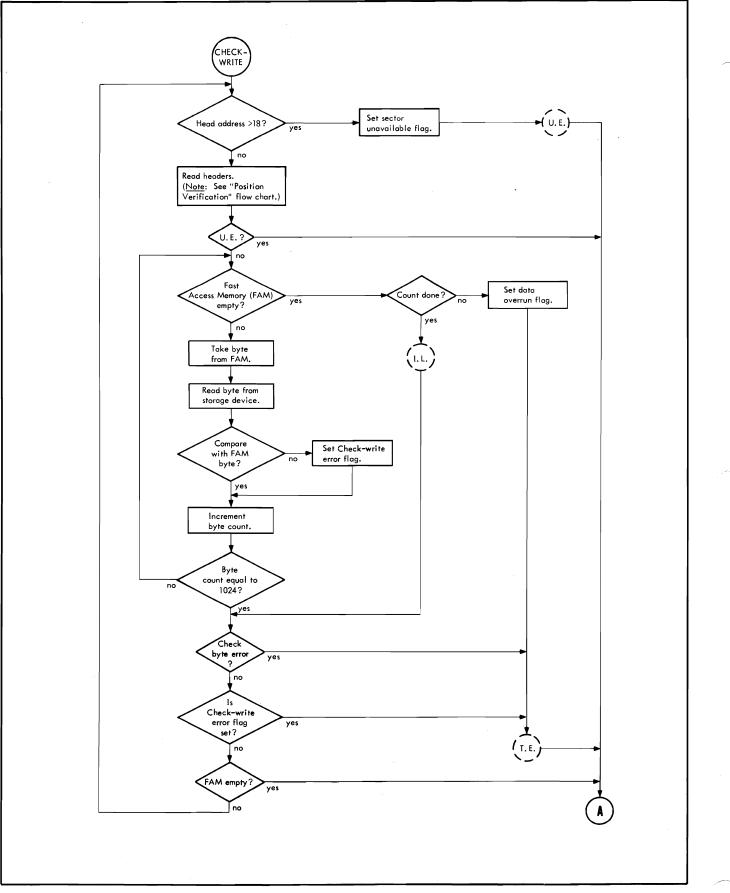
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Figure 12. Position Verification



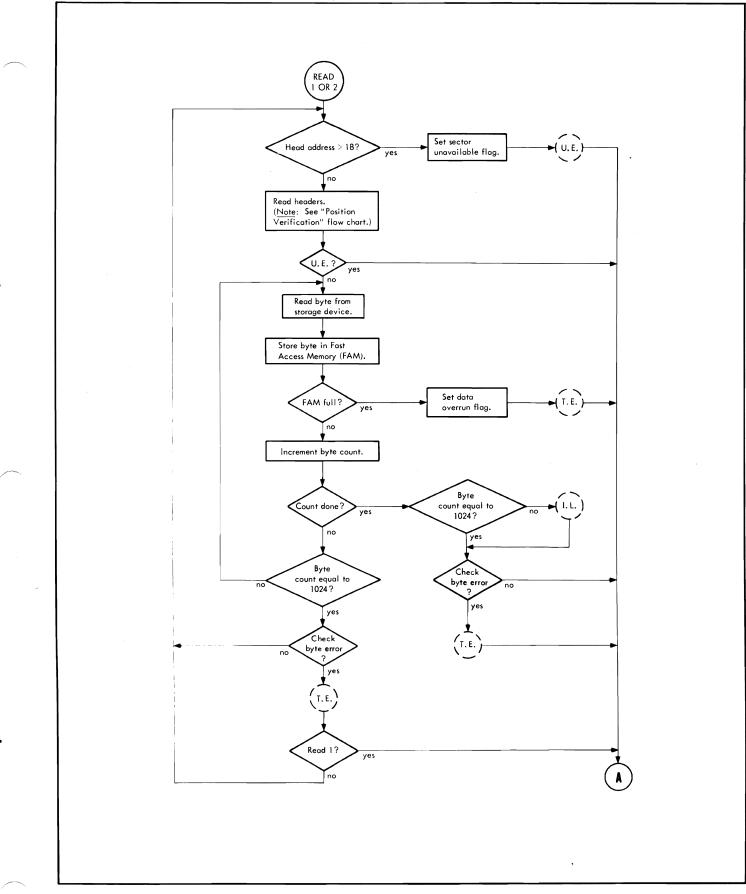
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Figure 13. Write Order



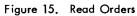
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Figure 14. Check-Write Order



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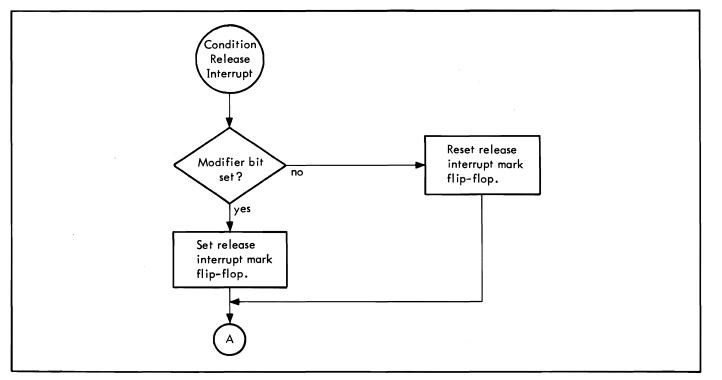


Figure 16. Condition Release Interrupt Order

PROGRAM I/O INTERRUPT ENVIRONMENT

The program establishes an I/O interrupt environment by setting the flags in the second word of the IOP command doublewords in the command lists, and by using specified timeout delays within software timeout routines. The recommended software timeout delay for disk operations is a minimum of 2 seconds.

The following flags must be set:

- ICE Interrupt at Channel End. Set only in last command of a command list.
- IUE Interrupt at Unusual End. Set in all commands.
- HTE Halt on Transmission Error. Set in all commands.
- SIL Suppress Incorrect Length. Set whenever the size of data transferred is not equal to the normal size for the operation (e.g., a Write operation with a byte count other than 1024). Thus an incorrect length indication is inhibited from causing an IOP Halt and a subsequent "unusual end" I/O interrupt.

The IZC flag (Interrupt at Zero Byte Count) is not necessarily set.

DISK SYSTEM INTERRUPT ENVIRONMENT

The disk system interrupt environment comprises interrupts generated by the controller and the device.

CONTROLLER-INITIATED INTERRUPTS

The controller generates two types of interrupts. The first is the result of an IOP-generated interrupt to indicate unusual end, channel end, etc. The second type is deviceinitiated and indicates Seek or Restore Carriage completed, device released, or attention required. The IOP interrupts have priority over device-initiated interrupts. The controller "busy" condition has priority over a device interrupt.

Interrupts are cleared by an AIO or HIO instruction to device address X'F' or by I/O Reset. An AIO clears only one interrupt whereas the I/O Reset and the HIO with device address X'F' clear all interrupts by clearing all device interrupt flags. An HIO to the device initiating the interrupt clears the interrupt.

The various interrupts are discussed individually in the subsequent sections.

IOP-INITIATED INTERRUPT

The IOP can set an interrupt call (CIL) by setting data bit 0 in a terminal order. This interrupt is cleared by an AIO or HIO instruction or by I/O Reset.

ATTENTION INTERRUPT

A device initiates an attention interrupt by setting its attention flag (status bit 7). If the controller is not busy, it scans the devices for initiation of a device interrupt. If the controller receives a TDV, TIO, HIO, or SIO instruction for another device, the interrupt is temporarily removed until the instruction is completed. An AIO or HIO to the initiating device clears the attention interrupt.

RELEASE INTERRUPT

A device initiates a release interrupt when it is released by another controller. The controller does not respond to any release signals from devices unless the Condition Release Interrupt order first enables the release interrupt logic. If a TIO, TDV, HIO, or SIO instruction is issued to another device, the interrupt call is temporarily removed until the instruction is completed. An AIO or HIO to the interrupting device clears the interrupt.

ON-SECTOR INTERRUPT

An on-sector interrupt indicates one of two things: a device has completed a Seek order or a Restore Carriage order (bit 4 of AIO); or a Seek timeout has occurred (bit 6 of AIO). The device signals on-sector to the controller when the heads are not in motion and the head is accessing the sector prior to the one addressed. Before the controller will generate an on-sector interrupt for any device, it must receive a Seek or a Restore Carriage order with the modifier bit set. An interrupt call (CIL) is set at the start of the sector prior to the one addressed by the order and is dropped at the start of the next sector if not cleared by an AIO instruction. The CIL is reinitiated the next revolution, however. An on-sector interrupt is temporarily removed by a TIO, TDV, HIO, or SIO to another device. An AIO, HIO, or I/O Reset clears it. Please note that an AIO or HIO clears only the single interrupt, whereas I/O Reset also clears pending interrupts (CIL not set).

DISK SYSTEM ERROR DETECTION ENVIRONMENT

Logic is provided within the controller for automatic detection of errors in the data flow in and out of the controller. Included are IOP parity check, device address parity, read check character bytes, and file address verification.

IOP AND CONTROLLER PARITY CHECKS

Odd parity is generated and checked for data transfers. Both the IOP and the controller can drive odd parity and perform parity checking. On the Sigma 8 and 9 computers, parity checking is performed on all data transfers, singleand four-byte. However, on the Sigma 5-7 computers, parity is checked only for these specific data: seek address, sense bytes, headers, and single-byte transfers.

Generally, this is what occurs (qualified by the Sigma 5-9 restrictions just cited); The controller drives odd parity for all data-in transfers to the IOP for single- and four-byte transfers, and drives parity checking on all transfers initiating from it. Odd parity is checked for all data-out on the single-byte interface. If the IOP drives the parity check, the check includes all data transfers on single- or four-byte transfers. "Transmission error" indicates data parity errors and "unusual end" indicates order and address parity errors.

DEVICE ADDRESS PARITY

The controller generates odd parity for the four device address lines; the device goes "not operational" if a parity error is detected.

READ CHECK CHARACTER BYTES

A two-byte check character is written at the end of each record (header or data). The controller initially computes and inserts these check characters, and recomputes and compares them with those read on any Read or Check-write order. "Transmission error" indicates any check byte error on data records, and "unusual end" indicates any check byte error on headers.

FILE ADDRESS VERIFICATION

File addresses are verified by several means. During each Seek, the controller automatically reads back from the device and verifies the file address (cylinder, head, track, sector) and any differences. It verifies the angular position of the heads for multiple sector-record Read and Write orders. The controller also verifies file address by comparing it with that read in the header. Any file address verification error results in order termination with "unusual end".

I/O FAULT DETECTION AND RECOVERY ACTIONS

The program can determine whether a disk pack I/O operation was completed successfully or terminated due to a fault condition by evaluating the status response and condition code bits obtained by issuing AIO and TDV instructions after an I/O interrupt.

The program must perform tests to determine whether the I/O interrupt is due to a device-generated interrupt or a channel end or unusual end interrupt – the two are mutually exclusive. If the status bytes received with an AIO do not indicate a device-generated interrupt, assume a channel end or unusual end interrupt.

TESTS FOLLOWING DEVICE I/O INTERRUPTS

The following tests can be performed after receipt of a device interrupt to determine the type of interrupt:

- Seek timeout error interrupt. If AIO status bit 6 is set, the device has generated the Seek timeout error interrupt as a result of a hardware malfunction during head movement. Use recovery action 3 (see "Recovery Actions" later in this chapter).
- On-sector interrupt. If AIO status bit 4 is set, the device has generated the on-sector interrupt to indicate the addressed sector's minimum access position time, or to indicate head motion completion for a Restore Carriage order.

- 3. Release interrupt. If AIO status bit 2 is set, the device, operating in dual access mode, has generated an interrupt after its release by the other controller.
- 4. Attention interrupt. If AIO status bit 1 is set, the device has generated an interrupt to inform the system that it has been started up and is ready to be connected to the disk system.

The testing described in this and the preceding section is applicable to all peripheral devices. If no error is found, device-dependent fault testing (see below) is not required.

PRIORITY OF DEVICE-DEPENDENT TESTING

One or more status bits may be set when a fault occurs. Thus to properly describe the fault, testing must be performed in a predefined sequence. Table 9 shows the testing sequence priorities.

Before performing device-dependent testing, the program must issue a TIO instruction to determine the state of the device. In case of software timeout, the TIO has already been issued.

The recovery actions annotated in Table 9 are more thoroughly described in the section subsequent to the table – "Recovery Actions".

TESTS FOLLOWING CHANNEL END OR UNUSUAL END INTERRUPTS

The following tests can be performed after receipt of a channel end or an unusual end interrupt:

- 1. CC1 and CC2 are zero for an AIO instruction.
- 2. AIO status bits 8, 9, and 12 are zero.
- 3. CC1 and CC2 are zero for a TDV instruction.
- 4. TDV status bits 8 through 15 are zero.

Table 9. Xerox Removable Disk Storage System Testing Sequence

Sequence and Summary Description	Condition Code, Status Response Bits, and Detailed Information	Seek	Sense , Release , Condition Release Interrupt	Restore Carriage	Read 1, 2, Write, or Checkwrite	Header Read	Header Write	Recommended Corrective Action
Step 1.	TDV CC1, CC2 = 01	X	×	х	x	X	х	See recovery action 1.
Perform if TDV CC1, CC2 ≠00, in- dicating TDV condition code error.	<u>Test mode</u> . The controller has been placed in test mode due to a hardware failure or a programming error.							
	TDV CC1, CC2 = 10.		x	х				See recovery action 2.
	Busy. The controller indicates it is currently "busy" with a				х	х	х	See recovery action 4.
	device other than the one addressed; this is the result of a hard- ware failure.	X						See recovery action 3.
Step 2.	TIO 5,6 - 01.	x	x	×	x	х	х	See recovery action 1.
Perform if TIO 5,6 ≠ 00, indicating controller is not "ready" immediately	Not operational. The controller has sensed that a power shutdown is in progress or that its control memory does not respond correctly.							
following an I/O interrupt.	TIO 5,6 = 10.		x	x				See recovery action 2.
	Not defined.				х	х	х	See recovery action 4.
		X						See recovery action 3.
	TIO 5,6 = 11.		x	х				See recovery action 2.
	Busy. The controller failed to return to the "ready" condition.				х	х	х	See recovery action 4.
	This can occur if a command list is coded for multiple interrupts or if hardware malfunction prevented the controller's return to the "ready" condition.							See recovery action 3.

Table 9. Xerox Removable Disk Storage System Testing Sequence (cont.)

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Sequence and Summary Description	Condition Code, Status Response Bits, and Detailed Information	Seek	Sense, Release, Condition Release Interrupt	Restore Carriage	Read 1, 2, Write, or Checkwrite	Header Read	Header Write	Recommended Corrective Action
Step 3.	TIO 1, 2 = 01	×	x	x	x	х	x	See recovery action 1.
Perform if TIO 1,2 ≠ 00, indicating device is not "ready" immediately following an I/O interrupt.	Not operational. The device has detected a hardware malfunction or a controller-to-device communication malfunction and has dis- allowed further operations to be performed on the device.							
	TJO 1,2 = 10.	x	х	х	х	х	х	See recovery action 1.
	Unavailable. The device is unavailable for usage through the addressed controller during dual access hardware configuration. Its unavailability is the result of its being presently reserved by the other controller of the dual access pair. <u>Note:</u> This could be a normal response if a dual-CPU system is not using interrupts.							
	TIO 1,2 = 11.	-	x	x				See recovery action 2.
	Busy. The device did not return to the "ready" condition. This				х	х	х	See recovery action 4.
	can occur if a channel command list is coded for multiple interrupts; if a hardware malfunction has prevented the return to "ready"; or if the I/O interrupt was other than an on-sector interrupt for a Seek or a Restore Carriage order.	×						See recovery action 3.
Step 4.	TDV 11 = 1.	х	×	х				See recovery action 2.
Perform if TDV 10,11, 12, or 13 ≠ 0, indicating IOP operation error.	Memory address error. This error can occur because of programming errors or hardware malfunction.				x	x	x	See recovery action 4.
	TDV 12 = 1.	x	x	x				See recovery action 2.
	<u>IOP memory error</u> . This error is due to hardware malfunction.				х	X	X	See recovery action 4.
	TDV 13 = 1.	x	×	x				See recovery action 2.
	<u>IOP control error.</u> This error is due to programming errors or hard- ware malfunctions.				x	х	x	See recovery action 4.
	TDV 10 = 1.	x	x	х				See recovery action 2.
	Transmission memory error. This error is due to hardware malfunction.				х	х	х	See recovery action 4.
Step 5.	TDV 4 = 1.	x	x	х	х	х	х	See recovery action 2.
Perform if TDV 4≠0, indicating parity error.	<u>IOP parity error.</u> The controller has detected a data parity error during the data-out phase of a seek operation.							
Step 6.	TDV 5 = 1.		х	x				See recovery action 2.
Perform if TDV 5≠0, indicating	Operational error. The controller or device (or both) has detected		_		х	x	х	See recovery action 4.
an operational error.	an operational error as a result of a hardware malfunction.	X						See recovery action 3.
Step 7.	TDV 2 = 1.	-	Х	X	~	x	~	See recovery action 2.
Perform if TDV 2 ≠ 0, indicating a programming error.	Programming error. The controller has detected one of these: an invalid order; an illegal address or cylinder overflow; the arm in	x	-		×	^	X	See recovery action 4.
	motion at the start of a seek operation; a byte count other than four for a seek operation; a byte count unequal to a multiple of the header size for a header operation; or an incorrect use of device address X'F'.							,
Step 8.	TDV 3 = 1.				x	x		See recovery action 6.
Perform if TDV 3≠0, indicating a write-protect violation.	<u>Write-protect violation</u> . The controller has detected that a write operation was about to be performed on a write-protected surface and has aborted the write operation.							
Step 9.	TDV 7 = 1.				х	x		See recovery action 2.
Perform if TDV 7≠0, indicating header parity error.	Header parity error. The controller has detected a parity error in the header during address verification.							

Sequence and Summary Description	Condition Code, Status Response Bits, and Detailed Information	Seek	Sense , Release, Condition Release Interrupt	Restore Carriage	Read 1,2, Write, or Checkwrite.	Header Read	Header Write	Recommended Corrective Action
Step 10.	TDV 6 1.			х				See recovery action 2.
Perform if TDV 6≠0, indicating	Verification or seek timeout error. The seek address does not compare				Х	Х	х	See recovery action 4.
seek timeout or verification error.								See recovery action 3.
Step 11.	TDV 1 = 1.				x			See recovery action 5.
Perform if TDV 1≠0, indicating a header flaw byte was detected.	Header flaw byte. A flaw byte has been detected in the header and the read, write, or check-write operation has been aborted.					×		See recovery action 6.
Step 12.	TDV 9 = 1.	x	x	х				See recovery action 2.
Perform if TDV 9 ≠ 0, indicating transmission data error.	<u>Transmission data error</u> . The controller has detected a data error that may be due to a check-write comparison error, an IOP parity error, a data overrun (rate) error, or a data check byte comparison error. The IOP can set this error if it detects a data parity error during data-in.				×	×	x	See recovery action 4,
Step 13.	TDV 8 = 1.	x		х				See recovery action 2.
Perform if TDV 8≠0, indicating	Incorrect length. The controller has detected that the byte count					X	×	See recovery action 4.
incorrect length error.	is not the nominal byte count for the operation being performed.		x		х			See recovery action 6.
Step 14. (Steps 1 through 13	Status inconsistent error. The device-dependent status has failed		x	х				See recovery action 2.
passed.)	to indicate the specific failure for which the device-dependent status checking was evoked. Consider this to be a hardware status malfunction.				х	×	X	See recovery action 4.
								See recovery action 3.

RECOVERY ACTIONS

Table 10 annotates the recovery actions for the channel end and the unusual end interrupts by I/O order. To determine the correct recovery action, first determine the order (Seek, Sense, etc.). You may assume that for multisector operations the failing sector can be determined and recovery action taken on the appropriate sector. Therefore we recommend that read operations use the Read 1 order (order code X'12') to ensure that a failure is reported immediately following the failing sector. If the Read 2 order (X'02') is used, the fault indications may be attributable to a number of sectors, and for this reason an alternate fault testing sequence may be necessary.

In the case of command lists, a sequence of operations are performed before the I/O interrupt occurs and status is made available. When an error occurs, the command list sequence is terminated and the failing order can be determined from the TIO current command doubleword address. The programming system then has its choice of repeating the entire command list or rebuilding the command list (bypassing all nonfailing surface operations) to repeat the operation that failed.

Perhaps it would be beneficial to give a few error definitions at this point – "soft" and "hard" read and write errors and seek errors. An error can be considered a read error only if the data were read correctly at least once after they were written. A soft read error is an error that occurs during a Read operation and can be corrected as a result of one or more reread operations (not to exceed 10). A hard read error is a read error that cannot be corrected during as many as 10 reread operations. Similarly, errors can be considered write errors only if a Write operation is immediately followed by a verification by reading; only if such verification is successful can the data be considered error-free. A soft write error is one that can be corrected after one rewrite, whereas a hard write error is one that cannot be corrected by one rewrite – it is an irrecoverable error. (See "Irrecoverable Errors", following this section.) A seek error is declared if a carriage positioning operation is not completed within 3 seconds. The verification of proper cylinder location is done in the controller during a subsequent Read, Write, or Check-write operation.

The recovery actions are described forthwith:

Action Description

- Abort operator intervention. The current operation must be aborted and operator notification given that the device or controller (or both) has become "not operational", "unavailable", or entered the test mode. The operator must then perform the appropriate action before returning the controller and device to the "operational" state.
 - 2 Order retry program recovery. Issue an HIO instruction (in the case of controller "busy") and retry the operation. Repeat the HIO-retry order sequence 10 times before considering the fault irrecoverable.

Action Description

- 3 Order retry after Restore Carriage program recovery. Issue an HIO instruction (in the case of controller "busy") followed by a Restore Carriage order to reestablish head positional reference. Then retry a Seek operation followed by the original operation (if it was not a Seek). Repeat this sequence 10 times before considering the fault irrecoverable.
- 4 Order retry after Seek program recovery. Issue an HIO instruction (for controller "busy") followed by a Seek order to reestablish the surface address and head position. Then retry the original order. Repeat this sequence 10 times before considering the fault irrecoverable.
- 5 Alternate surface selection program recovery. Issue a Header Read order to determine the assigned alternate surface address. This action is, of course, appropriate only when the header area is used for alternate assignment.
- 6 Program notification no recovery required. The program is notified of the following occurrences for which a recovery action is not necessarily required:
 - A write-protect violation occurred on a writeprotected surface.
 - A header flaw byte was detected during a Header Read operation.
 - An incorrect length indication appeared during an operation for which partial information transfer was acceptable.

FAULT LOGGING

Part of the fault recovery procedure is the obtaining and logging of additional failure indicators using the Sense operation. The sense data comprises 16 bytes of status and fault information. Place bytes 0 through 15 in the error log along with the I/O instruction status. The two reasons for obtaining and logging the sense data are

- The specific failure information provided in sense bytes 8 and 9 is valuable for hardware repair. The physical device on which the faults occurred, regardless of the device's logical address, can be determined from byte 5.
- 2. The Sense order with a byte count of 16 resets these failure indicators that otherwise would remain set after the first occurrence of each fault.

If Sense operations are performed only occasionally after faults, the Sense information could contain misleading, past history, failure data.

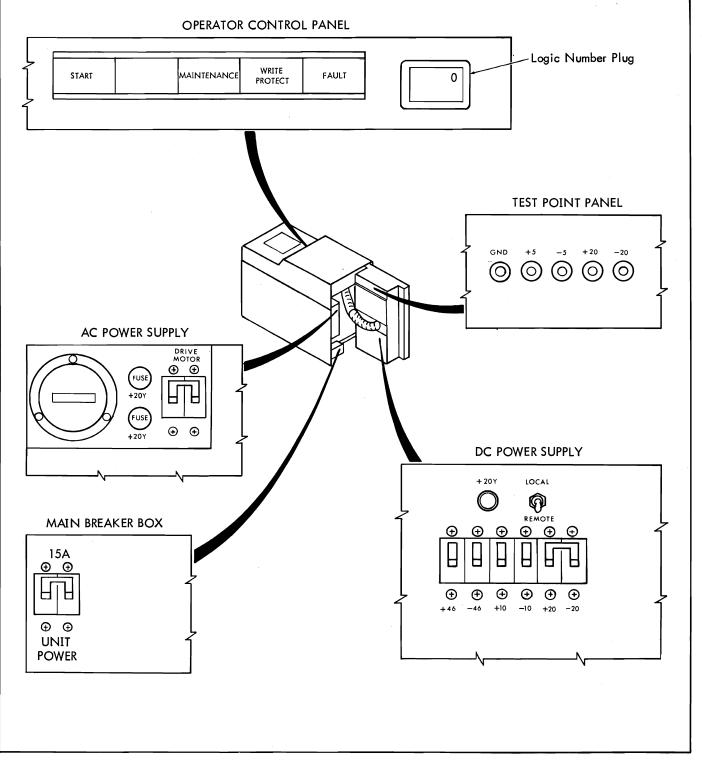
IRRECOVERABLE ERRORS

To discuss the specific action to take after an irrecoverable error falls outside the scope of this manual, for the action varies with the order and the user's application. For instance, the system may tolerate sense failures, whereas read failures can cause an action range from job abortion to system shutdown. Irrecoverable write failures may merely require the choice of another surface area and the disallowance of further operations on the failing sector (or sectors) to remedy the situation.

5. OPERATIONS

CONTROLS AND INDICATORS

The disk drive storage unit houses two types of controls and indicators: one group for use by the operator, and one group for troubleshooting and preventative maintenance use by a customer service engineer (CE). The following sections describe the two groups; the locations of all controls and indicators are pictured in Figure 17.





OPERATOR CONTROL PANEL

The operator pushbutton controls and lighted indicators are located on a horizontal panel on the front of the disk storage unit (see Figure 17). The controls and indicators serve these functions:

Control or Indicator	Function						
START switch/indicator	When all conditions for starting disk spin (see below) are satisfied, depression causes the disk to start and the backlight to illuminate. Depression while the disk is spin- ning extinguishes the backlight and causes the disk to stop.						
	These are the conditions for start- ing disk spin:						
	• Disk pack is installed.						
	• Disk pack cover is removed.						
	 Storage unit top cover is closed. 						
	• Carriage is retracted.						
	• Air flow is normal.						
	• Temperature is normal.						
	• AC and DC power are ON.						
Unit ready and unit number indicator	Illumination of this backlight in- dicates that the disk storage unit is ready to transfer data (i.e., the spindle has reached the required rotational speed and the heads are loaded). This indicator may be blank, or (optionally) a numbered lens may be inserted to show the physical device address (0-14).						
MAINTENANCE indicator	Illumination of the MAINTENANCE backlight indicates that the disk storage unit is operating off-line. The unit may be taken off-line by the Field Test Exerciser (FTE), or by setting the LOCAL/REMOTE switch on the DC power supply						

WRITE PROTECT switch/indicator

Control or Indicator

FAULT switch/indicator

Function

Illumination of the FAULT backlight indicates that a fault condition has occurred and must be cleared before the device will become operational. Momentary depression causes the following actions:

- Resets any nonpersistent fault condition.
- Resets the device release flag bit if it is set.
- Causes the device to report "not operational" during the duration of the depression.
- Terminates any function currently in progress.

Logic Number Plug

switch on the DC power supply panel to the LOCAL position.

Illumination of the WRITE PRO-

TECT backlight indicates that the

device is prevented from writing on the disk pack. Alternate action switch. Depression inhibits writing

on the entire pack. Depression while the pack is write-inhibited

releases the write inhibition.

This interchangeable plug-in device assigns the disk a logical unit address. Unit addresses 0 through 14 are available.

CE MAINTENANCE PANELS

The test point panel, AC power supply panel, DC power supply panel, and the main breaker box are located inside the rear panel of the disk drive unit (see Figure 17). The operator is only concerned with the main UNIT POWER circuit breaker, and the circuit breakers and LOCAL/ REMOTE switch on the DC power supply panel. See "Disk Drive Power Turn On" for a description of their settings in that procedure.

OPERATING PROCEDURES

The following sections describe the day-to-day operations on the disk controller and disk drives, and the procedures for taking care of the disk packs.

Note: Disk packs must be initialized before they can be used. See, for example, the discussion of volume initialization in the Xerox UTS/SM Reference Manual, 90 16 74.

DISK PACK INSTALLATION

This is the procedure for installing a disk pack:

Open the top door on the disk drive. A spindle lock 1. mechanism will be activated when the door is opened. This locking mechanism holds the spindle stationary while the disk pack is being inserted.

- 2. Lift the disk pack by the top canister handle. Remove the bottom cover of the canister by squeezing together the parallel plastic flanges in the center of the bottom cover. Set the bottom cover aside.
- 3. Carefully position the disk pack onto the spindle.
- 4. Turn the top canister handle clockwise until you feel a positive stop.
 - Note: Should the canister release early from the disk pack, continue turning the canister handle until you do feel the stop.
- 5. Carefully lift the top canister cover clear of the disk pack and rejoin it with the bottom canister cover.
- 6. Close the top door on the disk drive.
- 7. Enter the disk pack identifier in the disk pack usage log.

SYSTEM POWER TURN ON

To power-on the entire removable disk system, perform both the controller power turn on procedure and the disk drive power turn on procedure described below. Note that turning on the power of an individual disk drive or controller ought not affect the rest of the removable disk system.

CONTROLLER POWER TURN ON

This is the procedure for turning on the power of a disk controller:

- 1. Open the front door on the controller and swing open the swing frame.
- 2. Set the PT38 power supply circuit breaker (CB1) to ON.
- 3. Set the SET/RESET switch to SET.
- 4. Set the CABINET POWER circuit breaker to ON.
- 5. Set the appropriate CONTROLLER POWER circuit breaker to ON. Now the controller fans will come on and the power supply AC lamp will light.
- 6. Close the swing frame and set the controller VOLTAGE MARGIN switch to NORM.
- 7. Set the POWER switch on the maintenance panel to REMOTE. When the remote power sequencing becomes enabled, the power supply DC lamp and the controller POWER lamp will light and the controller will go online if the MODE switch is in the ONLINE position.
- 8. Set the MODE switch to ONLINE.
- 9. Close the front door on the controller.

DISK DRIVE POWER TURN ON

This is the procedure for turning on the power of a disk drive:

- 1. Set the UNIT POWER circuit breaker (main breaker box) to ON. The blower fans will come on.
- Set the LOCAL/REMOTE switch on the DC power supply panel to REMOTE. (The switch is set to LOCAL if maintenance is to be performed on the unit.)
- 3. Set all circuit breakers on the DC power supply panel to ON. The +20Y lamp will light, indicating the presence of the necessary voltage for the power up sequence circuit.
- 4. Close the rear panel of the disk drive unit.

DISK DRIVE START UP PROCEDURE

The following recommended procedure is for starting up a disk drive:

- 1. Perform the disk pack installation procedure (see "Disk Pack Installation").
- 2. If the FAULT indicator on the operator control panel is lighted, clear any existing nonpersistent fault by depressing the FAULT switch. However, for any indication of a persistent fault, immediately notify your CE or supervisor.
- 3. Depress the START switch to start the device; the START indicator will light.
- 4. The disk drive will complete the first Seek ("first Seek" means the heads are automatically loaded to the flying position and then returned to track zero). The disk drive will generate an attention interrupt to signal the controller that a new disk drive and pack have joined the removable disk system.

This then is the sequence in which the disk comes up to operational force. If all conditions for starting the disk drive are present (refer back to the description of the START switch/indicator in "Operator Control Panel"), the mounted disk pack will come up to required rotational speed and the brush cycle will begin. In the brush cycle, the brush carriage simultaneously sweeps 20 disk brushes (one brush per surface) across the disk surfaces to loosen any foreign material that may have accumulated there. When the brush cycle completes, the heads will load and the disk drive becomes operational, providing the servo system is operational and there are no existing fault conditions.

38 Operating Procedures

In summary, then, these conditions must be satisfied before the controller can be allowed to operate the device:

- AC and DC power are ON.
- The heads have loaded, there are no fault conditions, and the first Seek is completed.
- The device is not in the maintenance mode.

The START indicator will now light.

DISK DRIVE STOPPING PROCEDURE

This procedure stops a disk drive:

- 1. Depress the START switch on the operator control panel to stop the rotating disk.
- 2. Wait until the disk pack stops spinning (approximately 30 seconds) and the START indicator goes off.
- 3. Open the top door of the disk drive.
- 4. Remove the disk pack (see "Disk Pack Removal" below, for the appropriate procedure to use).
- 5. Either close the top door of the disk drive or install a new disk pack and start up the drive again (see "Disk Drive Start Up Procedure"), as applicable.

SYSTEM POWER TURN OFF

To power-off the entire removable disk system, perform both the controller power turn off procedure and the disk drive power turn off procedure described below. Note that turning off the power of an individual disk drive or controller ought not affect the rest of the removable disk system.

CONTROLLER POWER TURN OFF

This is the procedure for turning off the power of a disk controller:

- 1. Open the front door on the controller and swing open the swing frame.
- 2. Set the applicable CONTROLLER POWER circuit breaker to OFF.

DISK DRIVE POWER TURN OFF

This procedure turns off the power of a disk drive:

- 1. Depress the START switch on the operator control panel and wait for the disk pack to stop spinning (START indicator is off).
- 2. Set the UNIT POWER circuit breaker to OFF.

DISK PACK REMOVAL

This is the procedure for removing a disk pack:

- 1. Observe that the disk pack is not spinning (START indicator is off).
- 2. Open the top door on the disk drive.
- 3. Separate the top and bottom canister covers.
- 4. Carefully place the top canister cover over the disk pack so that the post protruding from the center of the disk pack is received into the top canister handle.
- 5. Turn the canister handle counterclockwise until you hear a clicking sound. This sound means the disk pack is secured to the top canister cover.
- 6. Carefully lift the canister and disk pack clear of the disk drive.
- 7. Close the top door of the disk drive.
- 8. Secure the bottom cover of the canister to the disk pack.

CARE AND MAINTENANCE OF DISK PACKS

Disk packs are precision devices. With proper care, handling, and storage they can have long and useful lives; and the installation can be assured of the integrity of the data recorded on them.

HANDLING

Always follow these precautions when handling disk packs:

- 1. Handle a disk pack with the canister (both top and bottom covers) attached, except, necessarily of course, while installing or removing the disk pack.
- 2. Never touch a disk surface with your fingers, or with pencils, clothing, or any other objects.
- 3. Be especially careful when installing or removing a pack from a drive unit to avoid damaging the disks or pack hub by rough handling.
- Do not drop a disk pack. Misalignment of the surfaces with the heads most assuredly can occur. Should you drop a disk pack, immediately inspect it for damage (see "Inspection").
- 5. When stopping a disk drive (see "Disk Drive Stopping Procedure"), do not try to "help" the disk to stop spinning by pressing on the top disk – wait until the disk stops by itself.
- 6. Be especially careful to keep ashes, tobacco, and coffee away from disk packs; ashes, tobacco and sugar are prime sources of disk contamination.

7. Before using a disk pack, condition it to machine room temperature for a minimum of one hour.

LABELING

There are certain rules to follow in labeling a disk pack.

- 1. Use only the center trim shield of the disk pack for labeling.
- 2. Use only labels designed for use as disk pack labels.
- 3. Do not use grease pencils, crayons, or pencils to write on labels; use ball point pens or felt tip pens.
- 4. Write label identification on a label before affixing it to the disk pack. In this way there is no danger of your bending the top disk from hand and arm pressure while writing on the label.
- 5. Do not try to erase the information on a label to correct it; remove the label and apply a new one.
- Do not put notes, markers, identification cards, etc., inside a disk pack.

INSPECTION

Note: Use only Model 7279 disk packs or packs that meet Xerox specifications.

When a disk pack is received, and every time a disk pack is to be installed on a drive unit, the pack must be inspected for possible damage. A damaged disk pack can cause head-to-disk interference (a head crash), and because a pack can be used on any number of disk drives, a single defective pack or drive unit can spread a malfunction to all drives and packs. Use the following recommended procedure to inspect a disk pack for damage before installing it on a disk drive unit:

- 1. Remove the bottom canister cover and carefully set it aside.
- Turn the pack upside down and hold it level so that you can spin the pack freely inside the top canister cover; apply the spinning force to the center hub, not to the disk.
- 3. While the pack is spinning, visually inspect it for excessive up and down motion (runout) of any of the recording disks or the sector disk. If you do not runout, bring the defective pack to the attention of the CE or your supervisor.

<u>Caution:</u> Under no circumstance allow the read/write heads to load on a defective disk pack; the heads will be damaged.

4. If the pack passes visual inspection, install it on a disk drive unit and depress the START switch.

- 5. Listen as the cleaning brushes move across the pack. If you hear any noise, this means a brush arm is contacting a disk surface. Stop the pack and immediately bring the problem to the attention of the CE or your supervisor.
- 6. Should the pack pass the brush test, continue as follows: As a final test after the heads have loaded, listen for any head-to-disk contact. If you hear contact, stop the pack immediately and notify a CE or your supervisor.

Should the pack pass inspection, it can safely be used. If there is head-to-disk interference, under no circumstances install the pack on another disk drive or another pack on this same disk drive, for both the original pack and drive may have sustained damage that can be passed to other packs and drives.

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USAGE LOG

A log must be attached to each disk drive unit for identifying all packs that have been used on that unit. Because one defective pack or drive unit can spread damage to other units in an installation, it is important to check which packs have been used when a malfunctioning disk drive unit or a defective pack has been discovered.

A log entry consists of at least these three items of information: pack identification, and date and time of pack insertion.

CLEANING

Disk pack canister covers and hubs, and disk drive shrouds and spindles must be checked frequently for contaminants and cleaned with 91 percent pure isopropyl alcohol and a lint-free cloth. This is the procedure for cleaning a drive unit shroud and spindle:

- 1. Stop the spindle motor.
- 2. Open the top cover of the drive unit.
- 3. Remove the disk pack (see "Disk Pack Removal").
- Clean the shroud with the lint-free cloth slightly dampened with alcohol. Wipe the shroud to remove all dirt and smudges. Thoroughly wipe the spindle surface.
- 5. After cleaning the shroud, use a pad of adhesive-type tape to pick up any particles that were not removed with the dampened cloth.
- 6. Make certain that all particles have been removed from the interior of the shroud by rewiping the shroud with the alcohol-dampened cloth.

Only competent maintenance personnel (e.g., customer service engineers) must be allowed to clean disk pack recording surfaces. The disk surfaces need be cleaned only when the pack is suspected of being the source of errors. The procedure for cleaning a pack is available in the appropriate customer service maintenance manual for the customer service engineer.

STORAGE

These precautions apply to the storage of disk packs:

- 1. Always store disk packs flat, with the bottom canister cover installed.
- 2. Replace cracked, distorted, or damaged canisters.
- 3. Do not stack disk packs one upon the other; to do so increases the likelihood of their being dropped and therefore damaged.

- 4. Do not store disk packs in direct sunlight or in areas exposed to magnetic fields from transformers, high current electric cables, or similar equipment. For high security storage, observe the same precautions used for storing magnetic tapes or microfilm records.
- 5. Keep the storage area free of dust and contaminants. The computer room is the best environment for disk pack storage. If during storage (storage conditions, nonoperating, are 8 to 80 percent humidity with no condensation over a temperature range of -30° to +150°) packs are exposed to temperatures of less than 60° or more than 90°, recondition the packs to normal computer room environment for one hour before use.

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