901179A
TECHICAL MANUAL

DATA SET CONTROLLER
MODELS 7601,7602,7603

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TECHNICAL MANUAL

DATA SET CONTROLLER

MODELS 7601, 7602, 7603

Specifications, equipment descriptions, and procedures contained herein are subject to change without notice.

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Total number of pages is 84, as follows:

Page No.	Issue	Page No.	Issue
Title	Original		
A	Original		
i thru iv	Original		
1-1 thru 1-6	Original		
2-1 thru 2-12	Original		
3-1 thru 3-44	Original		
4-1 thru 4-16	Original		

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF RELATED PUBLICATIONS

The following publications contain information which is not included in this manual, but which contributes to a complete understanding of Data Set Controller Model 7601 when used with related SDS equipment.

Publication Title	Publication No.
Diagnostic Control Program for Sigma 2 Computer Peripheral Devices, Reference Manual	900839
Diagnostic Control Program for Sigma 5/7 Computer Peripheral Devices, Reference Manual	900712
Sigma 2 Data Set Controller, Diagnostic Program Manual	901510
Sigma 5 and 7 Data Set Controller, Diagnostic Program Manual	901509
Sigma Computer Systems/Interface Design Manual	900973
Power Supply Model PT16, Technical Manual	901080
Sigma 7 Computer, Reference Manual	900950
Sigma 5 Computer, Reference Manual	900959
Sigma 5 and 7 Relocatable Diagnostic Program Loader, Diagnostic Program Manual	900972
Sigma Symbol and Meta-Symbol Reference Manual	900952

SECTION I
GENERAL DESCRIPTION

1-1 INTRODUCTION

This manual describes Data Set Controller (DSC) Models 7601, 7602, and 7603, manufactured by Xerox Corporation. The information in this manual is arranged in the following format:

a. Section I - General Description
b. Section II - Operation and Programming
c. Section III - Principles of Operation
d. Section IV - Maintenance and Parts List

The DSC enables Sigma computers to connect to a synchronous or asynchronous data set and to transmit and receive data over common carrier private lines or public switched network facilities, in a half-duplex or full-duplex mode of operation.

1-2 LIST OF RELATED PUBLICATIONS

The related publications listed in the front matter of this manual contain the following information:

a. The diagnostic control program manuals for Sigma 2, 5, and 7 computers describe the diagnostic control programs that serve as interface between the user and the specific peripheral program.

b. The data set controller diagnostic program manuals for Sigma 2, 5, and 7 computers describe the self-loading and object programs used to test and exercise the data set controller.

c. The Sigma computer interface design manual describes how external devices are connected to Sigma computers.

d. The Power Supply Model PT16 technical manual describes the principles of operation, adjustments, operational checks, and methods of installing Power Supply Model PT16.

e. The Sigma 2, 5, and 7 computer reference manuals describe Sigma computer program format and application and computer operation.

f. The Sigma relocatable diagnostic program loader manual describes the program used to load peripheral diagnostic programs into main memory.

g. The symbol and metasymbol reference manual describes the symbolic source language programs and how these programs are converted to machine language.

1-3 PHYSICAL DESCRIPTION (Figure 1-1)

The basic DSC consists of two chassis mounted in a standard Sigma swing frame. The two chassis contain 64 module positions (32 in each chassis). During the asynchronous mode of operation, 46 module positions are used. During the high-speed synchronous mode of operation, 49 module positions are used. Four standard eight-bit input/output channel interface cables and one data set cable are used to connect the DSC to the IOP and the data set. When an option such as automatic dialing is added, an additional cable assembly and two modules are required to connect the dialing unit to the DSC.

Power Supply Model PT16 supplies power to the DSC. The supply is external to the DSC and is mounted on the standard Sigma swing frame. Refer to publication 901080 for a complete physical description of this power supply.

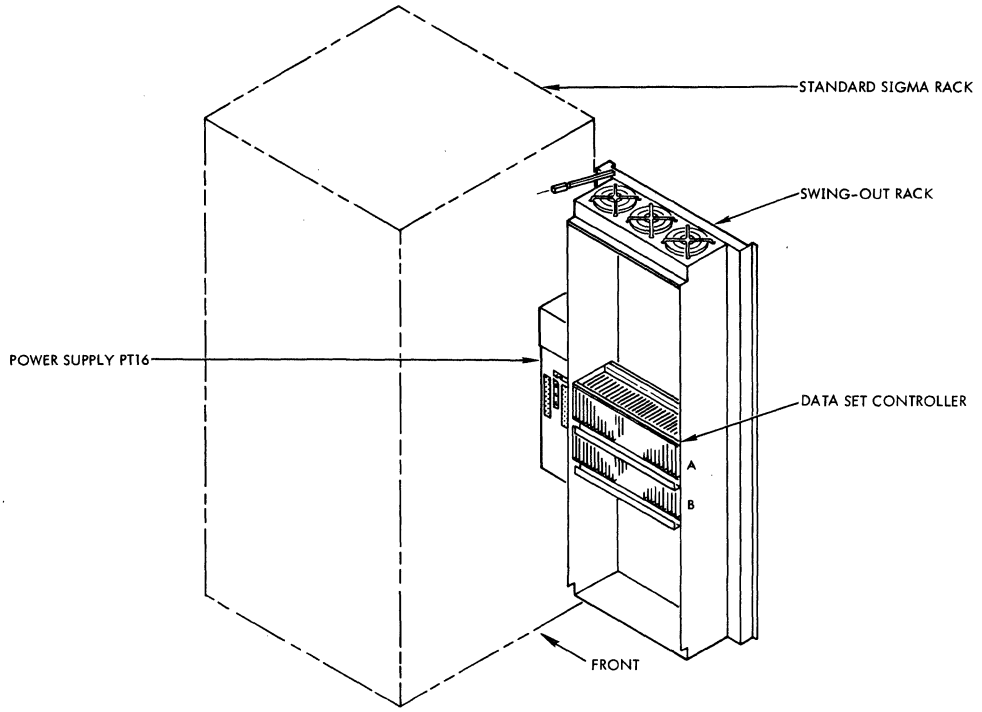
1-4 FUNCTIONAL DESCRIPTION (Figure 1-2)

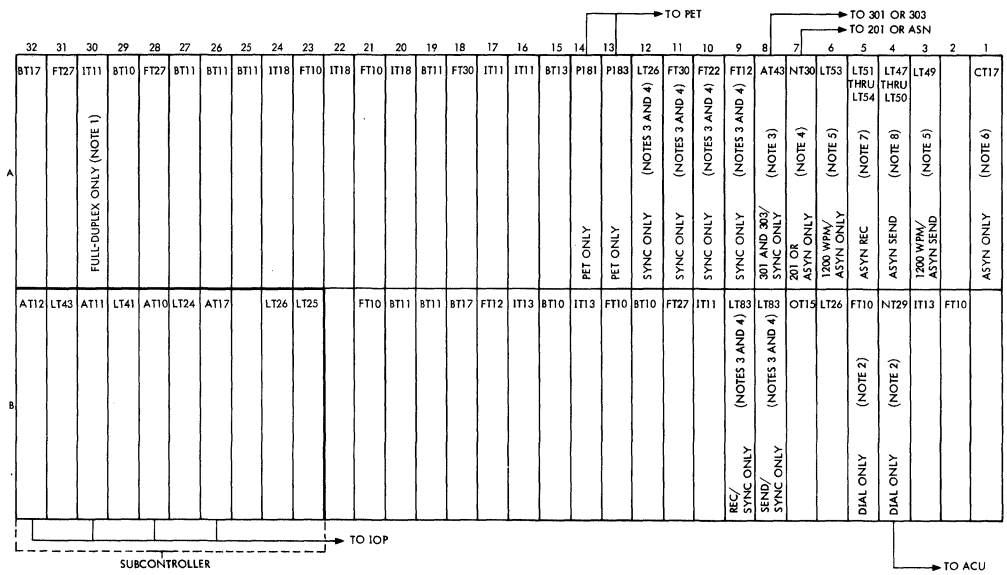
Figure 1-2 illustrates a communication link diagram of the DSC. Most of the blocks in the figure are not integral parts of the DSC; they are shown merely to illustrate how data is transmitted and received between the Sigma computer system and the remote device, as well as how the DSC controls the application of this two-way exchange.

The Sigma computer system communicates with the IOP. Communication begins with an SIO directive from the CPU. The IOP communicates with the DSC subcontroller (which is an integral part of the DSC), and the DSC communicates with a local data set. The local data set in turn communicates with a remote data set, which communicates with the devices connected to it for service.

The DSC is capable of communicating with asynchronous or synchronous data sets in a half-duplex or full-duplex mode of operation. (See table 1-1 for a description of these modes and other options.) The basic DSC provides the half-duplex send and receive capability plus a ring detection circuit with interrupt features. Adding modules to the basic DSC provides the DSC with full-duplex capabilities. The full-duplex feature provides the capabilities of sumultaneously sending and receiving data over a private line or over standard telephone lines.

If standard telephone lines are used, communication with a remote data set must be established manually or programmatically before data exchange can take place. To programmatically establish communication with the remote data set, an automatic dialing system, consisting of two modules is added to the basic DSC configuration. The dialing system is then





NOTES:

1. PART OF MODEL 7602 (OPTIONAL)
2. PART OF MODEL 7603 (OPTIONAL)
3. PART OF ASSEMBLY 145302 (OPTIONAL)
4. PART OF ASSEMBLY 139855 (OPTIONAL)
5. PART OF ASSEMBLY 139852 (OPTIONAL) OR ASSEMBLY 139853 (OPTIONAL)
6. PART OF ASSEMBLIES 139846 THROUGH 139854 (OPTIONAL)
7. THE MODULE OCCUPYING THIS POSITION SHALL BE IN ACCORDANCE WITH THE FOLLOWING:
   LT51 PART OF ASSEMBLIES 139846, 139847, 139848, 139849 (OPTIONAL)
   LT52 PART OF ASSEMBLY 139850 (OPTIONAL)
   LT53 PART OF ASSEMBLY 139851 (OPTIONAL)
   LT54 PART OF ASSEMBLY 139854 (OPTIONAL)
8. THE MODULE OCCUPYING THIS POSITION SHALL BE IN ACCORDANCE WITH THE FOLLOWING:
   LT47 PART OF ASSEMBLIES 139846, 139848, 139847, 139849 (OPTIONAL)
   LT48 PART OF ASSEMBLY 139850 (OPTIONAL)
   LT49 PART OF ASSEMBLY 139851 (OPTIONAL)
   LT50 PART OF ASSEMBLY 139854 (OPTIONAL)

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Figure 1-1. Data Set Controller Models 7601, 7602, and 7603

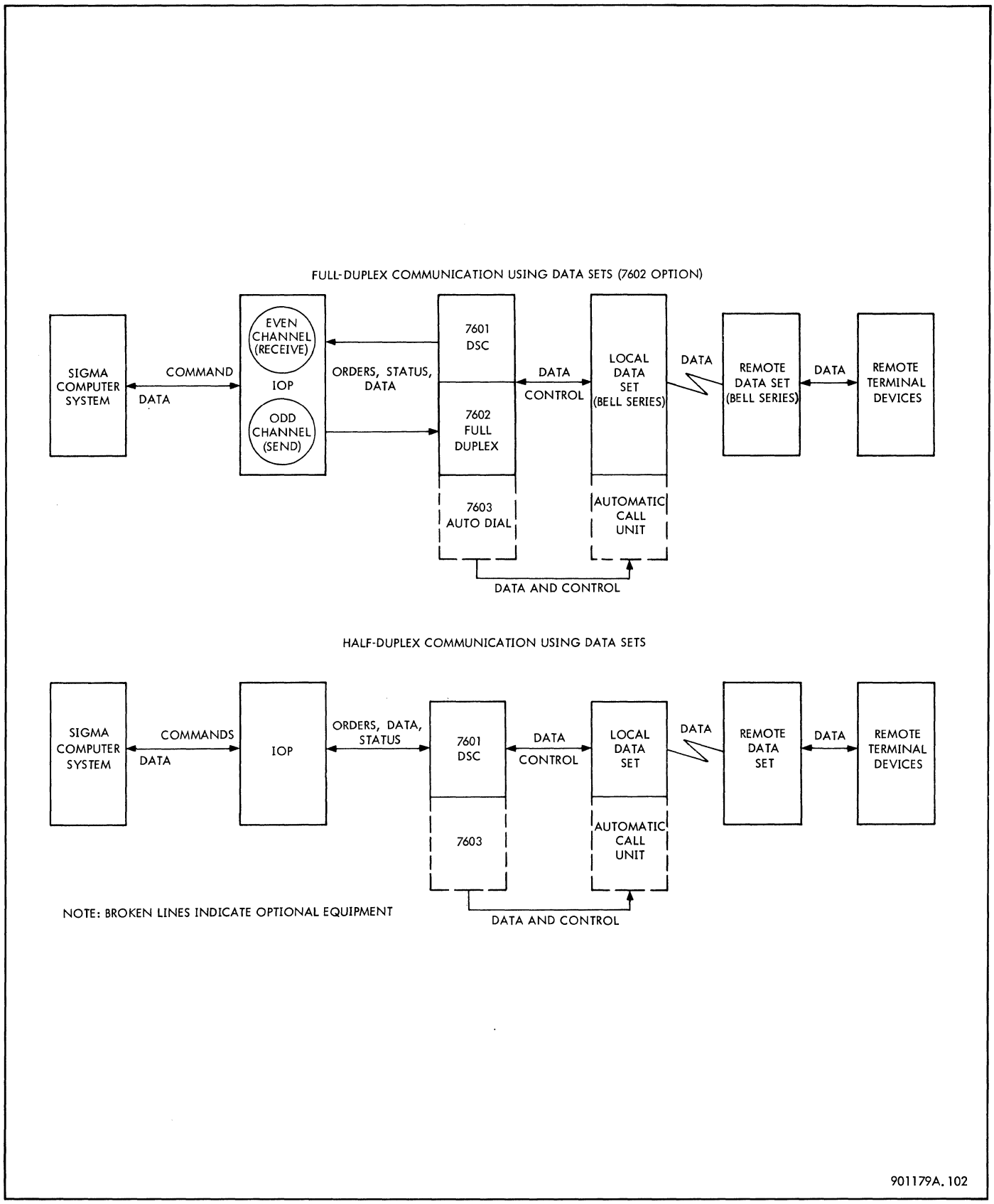

Figure 1-2. Communication Link Diagram

Table 1-1. Data Set Controller Options

Option	Model	Configuration	Additional Modules	Format	Description
Half duplex	7601		None		Capable of sending and receiving data plus providing a ring detection circuit with interrupt features. Communicates with one IOP channel
Full duplex	7602		1		Permits DSC to simultaneously send and receive data. Communicates with two consecutive IOP channels – odd and even. Odd channel is associated with send; even, with receive. Read channel is highest priority
Automatic dial	7603		2		Allows outgoing calls over standard telephone lines to initiate remote data set ring circuit. When full-duplex option is installed, dialing feature is extension of write operation
Asynchronous		103A, 103F, 301B, 303, 202C, 202D		5-7.5 7-9 8-10 8-11	Transmits and receives data at a rate determined by the DSC. Supplies no clock or timing pulses to distinguish data pulses from non-data pulses. Transmits all data in a selected format
Synchronous		201A, 201B, 301B, 303B6, 303C6, 303D6, 303E6	None		Transmits and receives data in a back-to-back fashion

programmed to ring the remote data set before data transfer takes place. When the local and remote data sets are connected together by a private line, the automatic dialing system is not required.

The rate at which data is transmitted and received over a private line or standard telephone lines is determined by the DSC and the type of data set used. If an asynchronous set is used, no timing or clock pulse is supplied by the data set to distinguish data pulses from non-data pulses. Consequently, all data is transmitted in a preselected data format containing a group of data bits preceded by a start pulse and followed by one or more stop pulses. If the data set used is synchronous, clock timing pulses are supplied by the data set while data is transmitted and received. Thus, synchronization is controlled by the data set and the responsibility for generating start and stop pulses is removed from the DSC. With this arrangement, the DSC is able to transmit and receive data in a back-to-back fashion.

In full-duplex operation, the DSC responds to two IOP address channels that have identical coding on the first seven most significant digits of the eight-digit address. The IOP address channels are referred to by the DSC as the odd channel address and the even channel address. The odd channel address is associated with writing, disconnecting, generating long space, or dialing. The even channel is associated with reading data or disabling or enabling the DSC ring detection circuit. If the DSC is in the half-duplex mode of operation, the DSC will respond to only one IOP channel address. This channel address is determined by all eight digits of the eight digit address and is decoded by the eight toggle switches on the subcontroller.

1-5 SPECIFICATIONS AND LEADING PARTICULARS

Table 1-2 lists the power requirements, environmental requirements, physical characteristics, and performance characteristics of the data set controller.

Table 1-2. Data Set Controller Specifications and Leading Particulars

POWER REQUIREMENTS	
Unit	Requirement
Data set controller	+4V, 5.0A
	+8V, 3.5A
	-8V, 1.0A
Power Supply Model PT16	120V (±5%), 2000 Hz, 15.0A
Fan	120V, 60 Hz, 0.2A

ENVIRONMENTAL REQUIREMENTS	
Unit	Requirement
Data set controller	Temperature
	Operating: +5°C - +50°C
	Nonoperating: -40°C - +60°C
	Humidity
	Operating: 10% - 95%
	Nonoperating: No limits
	Temperature change rate: -12°C/hr max
	Wet bulb temperature: 30°C max

PHYSICAL CHARACTERISTICS

Unit	Height	Width	Depth	Weight	Service Clearance
Data set controller	10.5 in.	19 in.	6 in.	18 lb. approx.	15 in.

PERFORMANCE CHARACTERISTICS

Feature	Characteristic
Bit transmission rate	45-230.4 kilobit/s
Rate classification	Low to high speed, message oriented
Maximum possible byte rate	100 kilobit/s
Disconnect time	50 ms
Successful dialing operation	5-50 plus digit dialing time

SECTION II
OPERATION AND PROGRAMMING

2-1 INTRODUCTION

This section describes the programmed function indicators issued by the IOP to the DSC, and the response of the DSC to these programmed function indicators. The different format units used by the DSC to accommodate a wide variety of remote terminals are also described.

2-2 FUNCTION INDICATORS

The function indicators issued by the CPU via the IOP to the DSC are as follows:

a. Start input/output (SIO)

b. Halt input/output (HIO)

c. Test input/output (TIO)

d. Test device (TDV)

e. Acknowledge interrupt (AIO)

f. Acknowledge service call (ASC)

2-3 SIO, HIO, AND TIO INDICATORS

The SIO, HIO, or TIO function indicator is issued by the IOP along with an address to initiate a start, halt, or test operation within the addressed DSC. In response to the function indicator, the DSC supplies status information to the IOP according to table 2-1. In full- or half-duplex operation, the status reported applies to the channel being addressed. If an HIO is issued on either channel during full-duplex operation, the HIO causes both channels (odd and even) to go to the ready state.

2-4 TDV INDICATOR

The TDV function indicator permits the IOP to test specific conditions within the DSC. In response to a TDV, the DSC provides the IOP with status information according to table 2-2.

Note

Although the HIO function indicator and the IOR signal reset the usual DSC flip-flops (unusual end, busy, interrupt), they have no effect on the data set in auto-dial device condition.

Table 2-1. Data Set Controller Response to SIO, HIO or TIO

STATUS	FUNCTION RESPONSE LINES								DORD	IORD	CONDITION
	0	1	2	3	4	5	6	7	CC1	CC2	
Interrupt pending	1										DSC has issued an interrupt which has not been acknowledged. An interrupt is issued when any of the following conditions exists: a. DAOR is true during a terminal order (TO) b. Ring detect is enabled and carrier is received c. Long space has been detected (asynchronous mode)

(Continued)

Table 2-1. Data Set Controller Response to SIO, HIO or TIO (Cont.)

STATUS	FUNCTION RESPONSE LINES								DORD	IORD	CONDITION
	0	1	2	3	4	5	6	7	CC1	CC2	
Device ready		0	0								DSC is in ready state and will accept an SIO unless an interrupt is pending
Device not operational		0	0								Cannot occur
Device unavailable		0	1								Cannot occur
Device busy		1	1								DSC is busy performing a task initiated by a previous SIO
Automatic mode				1							Always true (1)
Unusual end					1						Unusual end occurred while terminating last operation. Unusual end is caused by any of the following: a. Loss of data set ready during a read or write operation b. Loss of clear-to-send signal during write operation c. Failure to complete dialing operation d. Line occupied and dialing operation attempted e. Data set ready is off and a read or write order is received f. Rate error occurred during a read or write operation (cannot occur on asynchronous write) g. DSC received IOP halt during a TO
DSC ready						0	0				DSC is in ready state and will accept an SIO unless an interrupt is pending
DSC not operational						0	1				Cannot occur
DSC unavailable						1	0				Cannot occur
DSC busy						1	1				DSC busy performing a task initiated by previous SIO

(Continued)

Table 2-1. Data Set Controller Response to SIO, HIO or TIO (Cont.)

STATUS	FUNCTION RESPONSE LINES								DORD	IORD	CONDITION
	0	1	2	3	4	5	6	7	CC1	CC2	
Not used								0			Always false (zero)
SIO successful (SIO)										1	
DSC not busy when HIO occurred (HIO)										1	
SIO can be accepted (TIO)										1	
Address recognition									1		

Table 2-2. Data Set Controller Response to TDV

STATUS	FUNCTION RESPONSE LINES								DORD	IORD	CONDITION
	0	1	2	3	4	5	6	7	NCC1	NCC2	
Rate error	1										Rate error occurred during read or write operation. (Rate error cannot occur during asynchronous write)
Local phone in use				1							Local phone in use (used with auto dialing)
Carrier detect off								1			Local data set not receiving carrier from remote data set. During connect sequence, this indicates handshaking not complete
Local data set in data mode					1						Local data set in data mode (used with auto dialing)
Data set not ready							1*				Data set not ready caused by any of the following conditions: a. No power b. Data set in talk, test, or local mode (controlled by data set switches) c. "Originate" data set has not received carrier from "answer" data set during connect sequence or "answer" data set has not received ring indicator

*After completion of data exchange, bit remains false until IOP issues a disconnect order to disconnect the data set from the switched message network

(Continued)

Table 2-2. Data Set Controller Response to TDV (Cont.)

STATUS	FUNCTION RESPONSE LINES								DORD	IORD	CONDITION
	0	1	2	3	4	5	6	7	NCC1	NCC2	
Automatic dial not available		1									Automatic dial feature not installed
Automatic dial does not have power			1								Auto-dial unit does not have power
Abandon call and retry						1					Dialing operation not successful
Undefined										0	Always zero
Address recognition									1		

2-5 AIO INDICATOR

When the DSC has an interrupt pending, the low priority interrupt call line to the IOP via the subcontroller is pulled high. The IOP acknowledges the interrupt call by pulling the AIO function indicator and the function strobe lines high. During the time the function strobe line is high, status is supplied to the IOP according to table 2-3.

2-6 ASC INDICATOR

The ASC function indicator is generated by the IOP in response to a service call from the DSC. If the DSC is the highest priority with a service call pending, the DSC connects itself for a service request cycle. This service request cycle is part of the input/output operation routine.

2-7 OUTPUT ORDERS

The response of the DSC to orders such as write, dial, read, enable ring detect, disable ring detect, disconnect call, or generate long space is described in the following paragraphs. Table 2-4 should be referred to for the program code and the bits sampled by the DSC to define the correct order.

2-8 WRITE ORDER

The DSC has four different timing sequences that can occur during the processing of a write order. Each timing sequence is unique to the option installed in the DSC and the type of data set that is communicating with the DSC. One timing sequence occurs when the DSC is operated in the full-duplex mode of operation. A second timing sequence occurs when the DSC is operated in the half-duplex mode of operation. A third timing sequence occurs when the DSC is operating with an asynchronous data set. A fourth and final timing sequence occurs when the DSC is operating with a synchronous data set.

A write order is initiated when the DSC accepts an SIO on the odd channel input/output address during full-duplex operation or on the odd or even channel input/output address during half-duplex operation. Accepting the SIO sets the appropriate busy flip-flop and transfers the DSC to the order output state. In the order output state, the DSC decodes the write order. The decoded write order initiates the transmission of a number of characters from computer memory to the data set after the clear-to-send signal is received from the data set.

The three-bit C field of the write order shown in table 2-4 is ignored if an asynchronous format unit is installed in the DSC. However, if a synchronous format unit is installed in the DSC, the three-bit C field specifies the number of bits to be transmitted out of each eight-bit byte from memory. A value of 000 in the C field signifies that eight bits per byte are to be transmitted.

Values of 010 through 111 (count of 001 is not allowed) correspond to two through seven bits per byte. That is, a value of 010 in the C field will cause only the information contained in data lines 6 and 7 to be transmitted, whereas another value in the C field will cause different data line bits to be transmitted. Also during the synchronous mode of operation the programmer must send at least four synchronizing characters at the beginning of each message.

2-9 DIAL ORDER

Table 2-4 illustrates the dial order that initiates dialing if the automatic dialing feature is installed. If the automatic dialing feature is not installed, an unusual end will be reported to the IOP. With the automatic dialing feature

Table 2-3. Data Set Controller Response to AIO

STATUS	FUNCTION RESPONSE LINES 0	1	2	3	4	5	6	7	DORD NCC1	NORD NCC2	CONDITION
Rate error	1										Rate error occurred during read or write operation (cannot occur during asynchronous write)
Ring (even channel only for full-duplex operation)		1									DSC sensed carrier detection after receiving an enable ring detect order. This bit signifies that connection has been established between the two data sets and that data exchange may start
Long space detected (even channel only for full duplex operation)			1								Long space has been received
Address recognition									1		
No faults exist										1	Rate error not being reported
Not used				0	0	0	0	0			

Table 2-4. DSC Response to Output Orders

WRITE								
	DATA LINES 0	1	2	3	4	5	6	7
Programmed code	C	C	C	0	0	0	0	1
Bits sampled by DSC to define write	C field				X	X	X	X
DIAL								
	DATA LINES 0	1	2	3	4	5	6	7
Programmed code	0	0	0	0	0	1	0	1
Bits sampled by DSC to define dial						X	X	X
READ								
	DATA LINES 0	1	2	3	4	5	6	7
Programmed code	C	C	C	0	0	0	1	0
Bits sampled by DSC to define read	C field							X

Table 2-4. DSC Response to Output Orders (Cont.)

ENABLE RING DETECT								
	DATA LINES 0	1	2	3	4	5	6	7
Programmed code	0	0	0	0	0	1	1	1
Bits sampled to define enable ring detect					X	X	X	X
DISABLE RING DETECT								
	DATA LINES 0	1	2	3	4	5	6	7
Programmed code	0	0	0	0	0	0	1	1
Bits sampled by DSC to define disable ring detect					X	X	X	X

(Continued)

Table 2-4. DSC Response to Output Orders (Cont.)

DISCONNECT CALL								
	DATA LINES							
	0	1	2	3	4	5	6	7
Programmed code					1	0	1	1
Bits sampled by DSC to define disconnect call					X		X	X
GENERATE LONG SPACE								
	DATA LINES							
	0	1	2	3	4	5	6	7
Programmed code	0	0	0	0	1	0	0	1
Bits sampled by DSC to define generate long space					X	X	X	X

installed and data lines 5, 6, and 7 of the dial order as shown, the DSC forwards the four least significant digits of each data byte to the automatic call unit (ACU) in a binary coded decimal (BCD) configuration.

The BCD string to the ACU can be of any length because the BCD string is controlled completely by the program. That is, the DSC will continue to request digits until count done is received from the programmer. When the DSC is operating in the full-duplex mode, the dial order from the IOP must be presented on the odd-numbered input/output address channel. If the dial order is presented on the even-numbered input/output address channel with the full-duplex feature installed, a channel end will occur. If the local data set is busy or the connection to the remote terminal is not completed when the dial order is initiated, an unusual end will also occur.

2-10 READ ORDER

Table 2-4 illustrates the read order that causes the DSC to assemble bits received from the data set into bytes which are then forwarded to computer memory. In the synchronous mode of operation the C field of the read order specifies the number of bits to be assembled per computer memory byte. A value of 000 in the C field signifies that eight bits per byte are to be read. Values of 010 through 111 (count 001 is not allowed) in the C field correspond to two through seven bits per byte respectively. That is, count 010 will cause data line 6 (DA6) and data line 7 (DA7) to contain data. All unused bits will contain zeros.

In the asynchronous mode of operation, the C field of the write order is ignored. The number of bits assembled into a byte is determined by the format unit installed in the DSC. All unused data bits will contain binary ones. Channel end is reported if count done occurs, end-of-text character is received, or end-of-text character plus one is received.

2-11 ENABLE RING DETECT ORDER

The enable ring detect order (table 2-4) enables the DSC to generate a device interrupt when the carrier detect signal from the data set is on. Thus, before transmission actually commences, the computer can be interrupted when dialed via the switched network. If the full-duplex feature is installed, the enable ring detect order is only accepted by the DSC on the even-numbered input/output address channel.

2-12 DISABLE RING DETECT ORDER

The disable ring detect order (table 2-4) prevents a device interrupt from occurring when the carrier detect signal from the data set is on by disabling the ring detect circuit. The ring detect circuit is also disabled by the HIO and input/output reset signals. If the full-duplex feature is installed, the disable ring detect order is only accepted by the DSC on the even-numbered input/output address channel.

2-13 DISCONNECT CALL ORDER

The disconnect call order described in table 2-4 disconnects the local data set from the switched telephone network and terminates all dialed calls. If the full-duplex feature is installed, the disconnect call order is accepted by the DSC on either the odd or the even-numbered input/output address channel.

2-14 GENERATE LONG SPACE ORDER

The generate long space order detailed in table 2-4 applies to asynchronous format units only. When this order is issued, it causes the DSC to generate long spaces. The byte count determines how many continuous long space characters are transmitted. (Long-space characters are defined as continuously transmitted zero characters without intervening stop bits.) If the generate long space order is received during synchronous mode of operation, channel end is reported and the DSC will not generate long space.

2-15 INPUT ORDERS

Table 2-5 presents the information supplied by the DSC to the IOP in response to input orders.

2-16 TERMINAL ORDER

Table 2-6 gives the response of the DSC to a terminal order (TO).

2-17 FORMAT UNITS

The basic DSC does not include a format unit. However, each basic DSC is prewired to accept different format units. This arrangement allows the basic DSC to accommodate a

Table 2-5. Information Supplied by Data Set Controller During Order Input

STATUS	DATA LINES								CONDITION
	0	1	2	3	4	5	6	7	
Transmission error	1								Transmission error has occurred during a read or write operation (cannot occur during asynchronous write)
Incorrect length		0							Not applicable
Chaining modifier			0						Not applicable
Channel end				1					Input/output operations are terminated
Unusual end					1				Unusual end is reported if any of the following conditions exists: a. The data set ready signal goes off during a read or write operation b. An IOP halt signal is received during a terminal order c. A transmission rate error occurs during a read or write operation d. A dial order is attempted and dialing option is not available e. Line is occupied and dialing operation is attempted f. Dialing operation is not completed g. The clear to send signal goes off during a write operation
Unused bits						0	0	0	

Table 2-6. Data Set Controller Response to Terminal Orders

STATUS INDICATOR	DATA LINES								RESPONSE
	0	1	2	3	4	5	6	7	
Interrupt	1								DSC causes an interrupt call
Count done		1							DSC completes input/output operation, reports channel end, and enters not busy state

(Continued)

Table 2-6. Data Set Controller Response to Terminal Orders (Cont.)

STATUS INDICATOR	DATA LINES								RESPONSE
	0	1	2	3	4	5	6	7	
Command chain			1						Senses command chain following reporting of channel end. Causes DSC to request a new order. Command chaining during synchronous receive causes DSC to search for a minimum of two more synchronizing characters before transferring data to computer memory
IOP halt				1					DSC immediately reports unusual end and enters not busy state
Unused bits					0	0	0	0	

wide variety of remote terminal devices. Selection of a format unit is determined by the remote input/output terminal device that is to communicate with the DSC. If the DSC is to communicate with an asynchronous data set, an asynchronous format unit is installed in the DSC; if with a synchronous data set, a synchronous unit is installed. Table 2-7 lists the standard format units along with the speeds, format unit modules, data sets, crystals, and typical terminal devices required for each format unit. Table 2-8 gives the various data sets and dialing units along with a brief description of each.

2-18 ASYNCHRONOUS UNITS

When the asynchronous data format unit is installed in the DSC, the DSC communicates with an asynchronous data set. In this configuration, the rate at which data is transmitted and received is determined by the DSC, because the data set does not supply timing pulses for data transmission or reception. For this reason, all data is transmitted and received in a preselected format having a group of data bits preceded by a start pulse (space) and followed by one or more stop pulses (mark). Four data formats are available as options on the DSC:

Format 1: 5-7.5. This format consists of five data bits preceded by one start pulse and followed by 1.5 stop pulses.

Format 2: 7-9. This format consists of seven data bits preceded by one start pulse and followed by one stop pulse.

Format 3: 8-10. This format consists of eight data bits preceded by one start pulse and followed by one stop pulse.

Format 4: 8-11. This format consists of eight data bits preceded by one start pulse and followed by two stop pulses.

2-19 SYNCHRONOUS UNITS

In the synchronous mode of operation, the DSC communicates with a synchronous data set. The synchronous data set supplies the clock timing pulses that determine the data transmission and reception rate. With the data set supplying the clock timing pulses, the DSC transmits and receives data in a back-to-back fashion. Thus, all data bits transferred from the DSC are in synchronization with the data set clock. For a more detailed description of the synchronous format unit see paragraph 3-2.

When communicating in synchronous mode, from two to eight bits can be accumulated in each data word. When transferring data via a synchronous data set, at least four start-of-transmission characters must be transferred at the beginning of each message sent, along with an end-of-transmission character at the end of the message. The start-of-transmission characters allow the remote device to synchronize with the incoming data. The end-of-transmission character notifies the remote device that the last of the data has been transmitted.

DATA FORMAT	SPEED	MODULES			CRYSTAL	DATA SET	TYPICAL REMOTE DEVICE CONTROLLED
		Send	Receive	Timing			
5 level/7.5 unit	60 wpm	LT47	LT51	CT17	128131-010	103A, 103F	Teletype Models 28 and 32
5 level/7.5 unit	66 wpm	LT47	LT51	CT17	128131-011	103A, 103F	Teletype Models 28 and 32
5 level/7.5 unit	75 wpm	LT47	LT51	CT17	128131-012	103A, 103F	Teletype Models 28 and 32
5 level/7.5 unit	100 wpm	LT47	LT51	CT17	128131-018	103A, 103F	Teletype Models 28 and 32
7 level/9 unit	148 wpm	LT48	LT52	CT17	128131-013	103A, 103F	IBM 1050
8 level/10 unit	150 wpm	LT49	LT53	CT17	128131-015	103A, 103F	Multipurpose keyboard display, Teletype Model 37
8 level/10 unit	1200 wpm	LT49	LT53	CT17	128131-015	202C, 202D	Multipurpose keyboard display
8 level/10 unit	1800 wpm	LT49	LT53	CT17	128131-012	202C, 202D	Multipurpose keyboard display
8 level/11 unit	100 wpm	LT50	LT54	CT17	128131-014	103A, 103F	Teletype Models 33, 35
2 to 8 level, synchronous	2000 bit/s	LT83	LT83	None	None	201A	General purpose, medium speed devices
2 to 8 level, synchronous	2400 bit/s	LT83	LT83	None	None	201B	General purpose, medium speed devices
2 to 8 level, synchronous	40800 bit/s	LT83	LT83	None	None	301B	General purpose, high speed devices
2 to 8 level, synchronous	19.2 kilobit/s	LT83	LT83	None	None	303	General purpose, high speed devices
2 to 8 level, synchronous	50.0 kilobit/s	LT83	LT83	None	None	303	General purpose, high speed devices
2 to 8 level, synchronous	230.0 kilobit/s	LT83	LT83	None	None	302	General purpose, high speed devices

Table 2-7. Data Set Controller Format Units

Table 2-8. Data Set Description (Continued)

Data Set/Dialing Unit Designation	Maximum Data Rate Bit/s	Used With Auto-Dial	Clocking	Full-Duplex Capability	Typical Service	Remarks
103 A1	150	No	Asynchronous	Yes	TWX-CE	None
103 A2	300	Yes	Asynchronous	Yes	Dataphone	None
103F	300	No	Asynchronous	Yes	Private line	Specify mode – answer or originate
201 A3	2000	Yes	Synchronous	Yes	Switched voice or private line	Specify EIA and internal clock
201B	2400	No	Synchronous	Yes	Private line	None
202C	1200	Yes	Asynchronous	Yes	Dataphone	None
202D	1800	Yes, when used with 804A*	Asynchronous	Yes	Private line	None
301B	40800	No	Synchronous	Yes	Wideband, TELEPAC channel	Specify internal clock
801 A1*	Not applicable	Not applicable	Not applicable	Not applicable	Auto-dial (dc pulse)	Terminate call by data set. Z option required. Stop timer by DSS. Y option required
801 C2*	Not applicable	Not applicable	Not applicable	Not applicable	Auto-dial (touch-tone)	Terminate call by data set. Z option required. Stop timer by DSS. Y option required
303 B6	19.2K	No	Synchronous	Yes	Wideband channel and switched voice channel	None
303 C6	50.0K	No	Synchronous	Yes	Wideband channel and switched voice channel	None

*Dialing unit

Table 2-8. Data Set Description (Cont.)

Data Set/Dialing Unit Designation	Maximum Data Rate Bit/s	Used With Auto-Dial	Clocking	Full-Duplex Capability	Typical Service	Remarks
303 D6	230.4K	No	Synchronous	Yes	Wideband channel and switched voice channel	None
303 E6	200.0K	No	Synchronous	Yes	Wideband channel and switched voice channel	None

SECTION III
PRINCIPLES OF OPERATION

3-1 INTRODUCTION

This section contains the general and detailed principles of operation for the data set controller. The general principles describe the overall operation of the DSC. The detailed principles describe the operation of the DSC in terms of detailed logic elements (flip-flops, gates, one-shots, etc). Flow diagrams, tables, timing diagrams, illustrations, and schematics are used to explain and illustrate each logical element.

3-2 GENERAL PRINCIPLES

The basic DSC requires one IOP channel. If the full-duplex feature is installed, two consecutive IOP channels are required. The first (even) channel is used for receiving data and the second (odd) channel is used for sending data and for automatic dialing. Before the DSC can receive or send data, however, operating power must be supplied. Operating power is supplied by external Power Supply Model PT16. Power Supply Model PT16 supplies the DSC with the following operating voltages:

a. +4V

b. +8V

c. -8V

The IOP and DSC are interconnected by four interface cables, which allow the exchange of information between the DSC and the IOP. One cable interconnects the DSC and data set. The two different types of cables for interconnecting the DSC and data set during full-duplex or half-duplex mode of operation are listed in table 3-1.

Table 3-1. Interconnecting Cable Assemblies

Cable Name	Part Number	Quantity	Remarks
Data set	145585	1	Full-duplex, 300 series
Data set	146379	1	Full-duplex, 100/200 series
Data set	146344	1	Half-duplex, 100/200 series
ACU	145283	1	Required to connect to ACU
IOP/DSC interface	127314	4	IOP/DSC interface cables

If power is supplied and interconnection between units is accomplished, the DSC will provide the control logic and signal conditioning required for the exchange of data between the IOP and the data set. This exchange of data can be accomplished in a full-duplex or half-duplex mode of operation, over a private line or standard telephone network lines. If the full-duplex feature is installed, the DSC permits simultaneous operation (send and receive) and two consecutive IOP channels are used to effect this simultaneous operation. If the simultaneous operation is done over standard telephone network lines, communication between the data sets must first be established. That is, some way must be found to alert the data set that communication is desired.

The automatic dialing feature installed in the DSC performs this task by transferring the dialing information received from the IOP to the ACU. The ACU then makes the telephone connection. During simultaneous operation, the automatic dialing feature is an extension of the write (send) operation. If communication is done over a private line, the automatic dialing unit is not required.

The DSC can transmit in an asynchronous or synchronous format unit to communicate with a wide variety of terminal devices. The format units are used in the full- or half-duplex mode of operation. Selection of the format unit is determined by the type of remote terminal device that is to communicate with the DSC.

If the DSC is connected for private line service and the asynchronous format unit and the full-duplex features are installed in the basic DSC, the data sets are always sending a carrier frequency that signifies that data is ready to be exchanged at all times, unless a component failure renders the data set inoperative.

If no failure occurs, the programmer can initiate the read and write operations. Data will be transferred from computer memory during send and stored in computer memory during receive. At the end of each operation, the DSC reports channel end and immediately proceeds to the ready state if command chaining is not required. Unusual end is reported immediately if any of the following conditions occurs:

a. The data set ready signal goes off.

b. A rate error occurs during read operation (transmission error is also reported).

c. The clear-to-send signal goes off during write operation.

d. An IOP halt is signaled.

Note

If the half-duplex feature is installed, read and write operations do not occur simultaneously. The carrier detect, data set ready, and rate error conditions can be interrogated by means of the TDV function indicator.

When the synchronous format unit is installed in the DSC, clock timing pulses are supplied by the data set and the DSC transmits and receives data bits in a back-to-back fashion at a rate determined by the data set clock. It is a programmer option as to how many data bits will be accumulated into each data word. It is possible to accumulate from two to eight bits in each data word.

When data is transferred, it is necessary to transmit at least four start-of-transmission characters at the beginning of each message and an end-of-transmission character to terminate each message. A switch option feature is also installed in the DSC either to terminate a read operation and report channel end immediately after the end-of-text character has been transferred to computer memory or to terminate read operations and report channel end when the end-of-text character plus one additional character have been transferred. The use of start-of-transmission characters and the end-of-transmission character allows the remote terminal devices to synchronize with incoming data and notify the remote terminal devices that the last of the data has been transmitted.

The CPU via the IOP initiates an input/output operation within the DSC by executing an SIO. During this execution, the DSC address is presented on the eight data lines. The DSC interrogates the data lines to determine whether the address placed on the data lines matches the address set in the switch comparator module.

If the full-duplex feature is installed in the DSC during the execution of an SIO, the DSC interrogates the first seven most significant digits of the IOP address with the DSC address signal (DCA). The eighth digit of the IOP address does not affect signal DCA because it is clamped to ground during full-duplex operation. Grounding data line 7 and pulling signal DCA high during the SIO determines whether the BUSY0 or the BUSY1 flip-flop is set.

The BUSY0 flip-flop is set when data line 7 is at ground and signal DCA is high. The BUSY1 flip-flop is set when data line 7 and signal DCA are both high. Setting flip-flops BUSY0 and BUSY1 transfers the DSC to the order output state for the even and odd channels respectively.

During half-duplex operation, the DSC will respond to only one IOP channel address (odd or even) during an SIO execution. This channel address, odd or even, will cause flip-flop BUSY0 to set during the half-duplex mode of operation. The setting of flip-flop BUSY0 represents the busy condition of the entire DSC during the half-duplex mode of operation. Flip-flop BUSY1 is prevented from setting during the half-duplex mode of operation by the input logic to BUSY1. When flip-flop BUSY0 sets, the DSC transfers to the order output state for the even channel.

After the DSC enters the order output state, an order is requested from the IOP. The order obtained from the IOP determines the future action of the DSC. In full-duplex mode, the only orders acknowledged during the even channel order output state are read, enable ring detect, disable ring detect, or disconnect. In the half-duplex mode, the orders acknowledged during the even channel order output state are dial, write, send long space, or disconnect. The read order enables the DSC to assemble data bits received from a data set into data bytes and then forward the data bytes to computer memory.

The write order enables the DSC to transfer data from computer memory to the data set. The enable and disable ring detect orders enable the DSC to generate a device interrupt or prevent the DSC from generating a device interrupt. The dial order allows the DSC to dial the automatic dialing unit. The disconnect order disconnects the local data set from the switched telephone network and terminates all dialed calls.

3-3 DETAILED PRINCIPLES

The detailed principles of operation of the DSC are considered under the following 10 typical major categories:

a. Function indicator acknowledgment

b. States and state flow

c. Service cycle

d. Read order timing sequence

e. Write order timing sequence

f. Dial order timing sequence

g. Disconnect order timing sequence

h. Disable-enable ring order timing sequence

i. Automatic hangup

j. PET operation

3-4 FUNCTION INDICATOR ACKNOWLEDGMENT

3-5 SIO

The IOP executes an SIO command by pulling the SIO function indicator and function strobe (FS) lines high and placing a DSC address on data lines DA0 through DA7. (See figure 3-1 for a logic diagram of the subcontroller.) The DSC connected to the IOP interrogates data lines DA0 through DA7 to determine whether the address placed on the data lines matches the address manually set in the switch comparator module in the subcontroller.

If the half-duplex option is installed, and data lines DA0 through DA7 match the switch setting, the DSC address signal (DCA) is pulled high. If the full-duplex option is installed, signal DCA is pulled high when the first seven most significant digits (DA0 through DA6) of the data lines match the switch setting on the switch comparator module. The eighth digit of the IOP address (DA7) does not affect signal DCA during full-duplex operation because the eighth digit input logic (signals SWA7C and NSWA7C) is clamped to ground when the full-duplex operation is installed in the DSC. If signal DCA is pulled high during an SIO, then data line 7 (DA7) determines whether flip-flop BUSY0 or BUSY1 is set (see figure 3-2). Data line 7 at ground and signal DCA high sets flip-flop BUSY0. With data line 7 held high and signal DCA high, flip-flop BUSY1 is set:

S/BUSY0 = NBUSY0 NINT0 SIOU DCAU NDA7X

C/BUSY0 = FSU + ...

NDA7X = NFULLDUP + PETCON
+ NPETCON NDA7U

S/BUSY1 = NBUSY1 NINT1 SIOU DCAU
FULLDUP
(DA7U + NFULLDUP
+ PETCON)

C/BUSY1 = FSU + ...

Note

The letter U attached to the last letter of a signal name represents a usable signal combination from the PET or IOP. Refer to table 3-2 for a description of the logic terms used throughout this section.

In full-duplex operation, when flip-flop BUSY0 sets, the DSC transfers to the order output state for the even channel address (OOUT0-A), and when flip-flop BUSY1 sets, the DSC transfers to the order output state for the odd channel address (OOUT1-A). During the half-duplex mode of operation, the DSC responds to only one input/output channel address during an SIO.

The DSC response to this SIO on the odd or even channel always causes flip-flop BUSY0 to set. Flip-flop BUSY1 is prevented from setting in half-duplex operation by the FULLDUP term in the set equation. The input/output address that the BUSY0 flip-flop responds to during half-duplex operation is decoded by signal DCA, which interrogates all eight data lines from the IOP.

This is accomplished by removing the ground clamp from signals SWA7C and NSWA7C. The ground clamp is removed when the full-duplex option is not installed in the DSC. That is, during half-duplex operation, the two signal lines are floating electrically, and as a result, the only order output state that the DSC can enter is defined by signal OOUT0-A.

Table 3-2. Glossary of Terms

Term	Description
2NDSYNC	Second sync character detected
ABORT	Terminate auto-dial sequence
ACRS	Abandon call and retry signal from ACU
ACU	Automatic call unit
AIO	Acknowledge input/output indicator
AIOC	AIO clamp
AIOC0	Transfers AIO status to data lines during AIO for even channel
AIOC1	Transfers AIO status to data lines during AIO for odd channel
AIODC	Dc sets DISRING flip-flop during an AIO
AIOM	AIO to me (from controller point of view)
AIOR	AIO receiver
ASC	Acknowledge service call indicator
ASCB	Acknowledge service call buffer latch
ASCM	Acknowledge service call for me (from controller point of view)
ASCR	ASC receiver
ASCR1	ASC receiver for odd channel

(Continued)

Table 3-2. Glossary of Terms (Cont.)

Term	Description
AVI	Available input signal
AVIR	Available input receiver
AVO	Available output signal
AVOD	Available output driver signal
BFSD	Buffered FSD signal
BIT1-BIT4	Four dial bits to dialer (ACU)
BSYC	Busy clamp
BSYP	Busy indicator driver to PET
BUSY0	Busy condition for even channel
BUSY1	Busy condition for odd channel
BUSYTSH	Busy status condition for TIO, SIO, or HIO
CARNDET	Carrier detect signal from the data set not detected
CARDTF	Carrier detect filter flip-flop
CARRDT	Common carrier detect signal from asynchronous or synchronous data sets
CARRDT200	Carrier detect signal for 200 series data set
CARRDT300	Carrier detect signal for 300 series data set
CDN0	Count done flip-flop for even channel
CDN1	Count done flip-flop for odd channel
CHEVEN	Even channel
CIL	Low priority interrupt call
CL1	1 MHz clock from IOP
CL1P	1 MHz clock from PET
CL1R	CL1 receiver

Table 3-2. Glossary of Terms (Cont.)

Term	Description
CL1U	Usable 1 MHz clock from PET or IOP
CL1X	Unbuffered 1 megacycle clock from PET or IOP
CL001X	Oscillator jumper wire
CL002	Crystal oscillator 2nd count
CL004	Crystal oscillator 4th count
CL008	Crystal oscillator 8th count
CL016	Crystal oscillator 16th count
CL032	Crystal oscillator 32nd count
CL064	Crystal oscillator 64th count
CL128SYN	Crystal oscillator 128th count (in sync with 1 MHz clock)
CL256	Crystal oscillator 256th count
CL512	Crystal oscillator 512th count
CL1024	Crystal oscillator 1024th count
CL2048	Crystal oscillator 2048th count
CL4096	Crystal oscillator 4096th count
CL8192	Crystal oscillator 8192nd count
CL16384	Crystal oscillator 16384th count
CLEARS	Common clear-to-send signal from asynchronous or synchronous data sets
CMPER	Comparison error from PET comparator circuit
CMPRSTR	Compare strobe to PET (combination of logic and compare input [CMPIN] switch on the PET)
CRQ	Call request signal to ACU when DSC wants to dial a distant data set
CSL	Low priority service call to subcontroller

(Continued)

Table 3-2. Glossary of Terms (Cont.)

Term	Description
CSLI	Special 150 ns delay for NFSC
CTSF	Clear-to-send flip-flop
CTS200	Clear-to-send signal for 200 series synchronous data set
CTS300	Clear-to-send signal for 300 series synchronous data set
C4SA3	External jumper wire that connects internal logic on inserted module
C4SA4	External jumper wire that connects internal logic on inserted module
DA0-DA7	Eight data lines from IOP
DA0D-DA7D	DA0-DA7 drivers
DA0P-DA7P	Eight data lines (order or data) from PET
DA0R-DA7R	DA0-DA7 receivers
DA0U-DA7U	Eight usable data lines from PET or IOP
DA7F	Data line 7 for full-duplex operation
DA7H	Data line 7 for half-duplex operation
DA7NDA56	Write or generate long space control logic
NDA7X	Inverted data line 7 for full-duplex operation
DADIN	Transfer data lines to IOP during data input state
DAOIN	Transfer data lines to IOP during order input state
DAOUT	Data output state flip-flop
DAOUTCL	Clock that occurs during data output state to load data into BIT1-BIT4 or WBR0-WBR7 register
DAOUTLK	Data output state lock flip-flop

Table 3-2. Glossary of Terms (Cont.)

Term	Description
DAOUTP	Data output state amplified for PET operation
DATAP0-DATAP7	Eight data lines from PET
DCA	Device controller address
DCAU	DCA from PET or IOP
DELAYRS	Delay request strobe
DI, DO	Data input, data output state
NDI, NDO	Not data input, not data output state
DIAL	Dial order flip-flop
DIALAVL	Dial option (ACU) available
DIALCYC	Dial cycle state
DIALNOP	Dialer not operational
DIN	Data input state flip-flop
DININLK	Data input state interlock flip-flop
DIO	ACU cable signal
DISCON	Disconnect data set
DISEL	Selected dial status
DISRING	Disable ring detect flip-flop
DLOS	Dialer telephone line occupied
DLYSC	Delay service call control
DLYSS	Output signal of 5 sec special delay one-shot (dial option only)
DOR	Data order request line during service and condition code line during function acknowledgement
DORD	Data order driver for subcontroller
DPR	Digit present signal from digit present flip-flop

(Continued)

Table 3-2. Glossary of Terms (Cont.)

Term	Description
DPRINLK	Dialer digit present interlock flip-flop
DSNOP	Data set not operational
DSNR	Data set ready signal not ready
DSR	Data set ready signal
DSR200	Data set ready signal for 200 series data set
DSR300	Data set ready signal for 300 series data set
DSS	Data set status signal
DSSD	ACU data set status delayed (5s)
DSSI	Input signal to special delay one-shot (5s)
DSSS	ACU data set status
DTR200	Data terminal ready signal from asynchronous and synchronous series data sets
DTR300	Data terminal ready signal from asynchronous and synchronous series data sets
ED	End data
EDD	ED driver
EDR	ED receiver
EOM	End-of-message character
EOMS1-EOMS7	End-of-message comparator switches
EOMP1	End-of-message plus one selection switch
ES	End service
ESR	ES receiver
ESU	End service from PET or IOP
EVENP	Even channel control from PET

Table 3-2. Glossary of Terms (Cont.)

Term	Description
EXDIAL	Exit from dial cycle state
EXEVEN	Service cycle exit of even channel
EXODD	Service cycle exit of odd channel
EXOIN1	Exit from odd channel order input state
EXOUT1	Exit from odd channel order output state
FCHEVEN	Even channel flip-flop
FCRQ	Call request flip-flop
FDPR	Digit present flip-flop
FEOM	End-of-message character plus one flip-flop
FIGS	Figures character for 5L/7.5U format
FNCTS	Not-clear-to-send flip-flop, energized when clear-to-send signal not clear for transmission
FR0-FR7	Subcontroller function response lines
FR0D-FR7D	FR0-FR7 drivers
FR7CNT	Bit 7 of device controller address for function response lines
FS	Function strobe from IOP
FSC	Service connect flip-flop
FSCL	Service connect flip-flop latch
FSCP	Service connect flip-flop for PET control
FSCU	Service connect signal from PET or IOP
FSD	Function strobe driver
FSL	Function strobe leading indicator
FSLD	FSL driver
FSP	Function strobe from PET

(Continued)

Table 3-2. Glossary of Terms (Cont.)

Term	Description
FSR	FS receiver
FSRC	Function strobe receiver clamped
FSSRM	Delayed SSRM signal
FSU	Usable function strobe from PET or IOP
FULLDUP	Full-duplex option available
HALT0	Halt condition on even channel (UNE0, CDN0, or EOM)
HALT1	Halt condition on odd channel (UNE1 or CDN1)
HANGUP	Data set disconnect control
HIOFS	Dc reset logic function during HIO instruction
HIO	Halt input/output indicator
HIOR	HIO receiver
HIOU	HIO from PET or IOP
HIOX	Signal derived from terms HIOU and DCAU
HPI	High priority interrupt call
HPID	HPI driver
HPIL	HPI latch
HPIR	HPI receiver
HPS	High priority service call
HPSD	HPS driver
HPSL	HPS latch
HPSR	HPS receiver
IC	Interrupt call
ICD	IC driver
INC	Inhibit service and interrupt calls

Table 3-2. Glossary of Terms (Cont.)

Term	Description
INI	Disable cable drivers from IOP (disconnect DSC from IOP)
INPUT	Data received from data set
INT0	Interrupt for even channel
NINT0FUL	Negated INT0 signal for full-duplex operation only
INT1	Interrupt flip-flop for odd channel
INTP	Interrupt indicator driver to PET
INTTSH	Interrupt status bit for TSH status
INWAIT	Input wait state flip-flop
IOPI0	IOP terminal order interrupt flip-flop for even channel
IOR	Input/output condition code line
IORD	IOR driver
LEADSYN	Leading sync flip-flop
LIH	High priority interrupt line
LIL	Low priority interrupt line
LOAD	Load count data into count register on synchronous send module
LOADI1, LOADI2	Inverted LOAD signal
LOADCNT	Load counter for synchronous receive
LSH	High priority service line
LSL	Low priority service line
LTRS	Letters character for 5L/7.5U
MANHIO	Manual reset or HIO reset
MANRST	Manual reset
ODR0-ODR7	Synchronous receive data register

(Continued)

Table 3-2. Glossary of Terms (Cont.)

Term	Description
OIN	Order input state for odd or even channel
OIN0	Order input state for even channel
OIN0DLY	Order input delay for even channel
OIN1	Order input state flip-flop for odd channel
OIN1DLY	Order input delay for odd channel
OOUT	Order output state for odd or even channel
OOUT0	Conditional order output state flip-flop for even channel
OOUT0-A	Order output state for even channel
OOUT1	Conditional order output state flip-flop for odd channel
OOUT1-A	Order output state for odd channel
OOUTNOP	Data set not operational during odd or even channel order output state
OOUTP	Order output state amplified for PET operation
ORD0P-ORD7P	Eight order control lines from PET
OUTPUT	Data transmitted from send module to data sets
NOUTPUTS	Not output operation
OUTUNE1	Unusual end on odd channel during order output state
OUTWAIT	Output wait state flip-flop
PETCON	PET control
PND	Present next digit signal from ACU
PNDS	ACU present next digit control

Table 3-2. Glossary of Terms (Cont.)

Term	Description
PNDU	Usable present next digit signal from PET or IOP
PRELEAD	Logic control detects presync characters
PRESYNC	Start-of-transmission character
PRESYNCS7	Start-of-transmission character comparator switches
PT18S	Switched ground source from sub-controller ON/OFF switch
PWI	ACU power indication
PWIS	Selected ACU power indication
RATER0	Rate error on even channel
RATER1	Rate error on odd channel
RATERP	Rate error signal for odd and even channel from PET
RATERTDV	Rate error status bit for TDV status
RB0-RB2	Synchronous receive buffer register
RBCMIN	Selects common input for synchronous register (RB0-RB2) during PET or IOP operation
RC0-RC2	Synchronous receive count register
RCN00-RCN03	Control for RCNTRL0-RCNTRL7 signals
RCNTRL0-RCNTRL7	Read synchronous count control (count 0-7)
RD0-RD7	Synchronous receive data register
RDORDP	Read order from PET
READ	Read order received from IOP
READCYC	Read cycle state flip-flop
READM	Signals the asynchronous receive module that controller has taken last character

(Continued)

Table 3-2. Glossary of Terms (Cont.)

Term	Description
RECLSP	Receive long space flip-flop
NRESET	Resets asynchronous send module (when at ground potential)
RESYNC	One ms time delay; prevents RTS from going false until one ms after data transmission is complete
RING	Ring flip-flop that sets when carrier detect is present
RLSPM	Receive long space control from asynchronous receive module
RM0-RM7	Synchronous receive data buffer register
RM1I-RM7I	Inverted RM1-RM7
RSA	Request strobe acknowledge
RSA-R	Reset logic for RSA1 and RSA2 flip-flops
RSA1	No. 1 delay control flip-flop for request strobe
RSA2	No. 2 delay control flip-flop for request strobe
RSAR	RSA receiver
RSARC	RSAR clamped
RS	Request strobe
RSD	RS driver
RSDC	RS amplified for loading purposes
RSRM-A	Buffered RSRM
RSRM	Receive service request signal from asynchronous send module
RST	Reset signal from IOP
RSTR	RST receiver
RTS	Request to send flip-flop
RTS 200	Request to send signal for 200 series data sets

Table 3-2. Glossary of Terms (Cont.)

Term	Description
RTS 300	Request to send signal for 300 series data sets
RUN	Continuous operation control from PET
SB-S	Common term into set side of SB register
SB0-SB2	Synchronous send buffer register
SC0-SC2	Synchronous send count register
SC	Service call
SCD	SC driver
SCR	Synchronous serial clock to receive
SCR 200	Synchronous receive clock for 200 series data sets
SCR 300	Synchronous receive clock for 300 series data sets
SCT	Synchronous serial clock to transmit
SCT 200	Synchronous transmit clock pulse for 200 series data sets
SCT 300	Synchronous transmit clock pulse for 300 series data sets
SD	Send data flip-flop
SENDNOP	During a send operation, a not operational condition has occurred
SERV1	Service cycle flip-flop
NSERVCN1	Not service cycle for odd channel
SERVEX	Exit from service cycle state
SIO	Start input/output function indicator from IOP
SIOR	SIO receiver
SIOU	SIO from PET or IOP
SLNGRST	Send long space reset control for asynchronous send module

(Continued)

Table 3-2. Glossary of Terms (Cont.)

Term	Description
SLNGSP	Send long space flip-flop
SSRM	Send service request signal from asynchronous send module
STOPPET	DSC stop condition when in PET control
SWA0-SWA3	Four most significant bits of DSC address
SWA4C-SWA7C	Four least significant bits of DSC address
SYNC	Synchronous option available
NSYNC	Ground source for sync option; NSYNC is at ground potential when sync option is installed
SYNCDN	Synchronous count done flip-flop
SYNCHALT	Stop condition (count done or unusual end) for synchronous operation
SYNCL	Synchronous clock to synchronous send module
SYNCRS	Synchronous request to send flip-flop
SYNCWRT	Synchronous write control flip-flop
TD 200	Cable signal indicating that data has been transmitted to an asynchronous or synchronous 200 series data set
TD 300	Cable signal indicating that data has been transmitted to an asynchronous or synchronous 300 series data set
TDVFR	Transfers TDV status to function response lines
TDV	Test device function indicator from IOP
TDVR	TDV receiver
TIO	Test input/output function indicator from IOP

Table 3-2. Glossary of Terms (Cont.)

Term	Description
TIOR	TIO receiver
TO	Terminal order flip-flop
TRANER	Rate (transmission) error for odd or even channel
TSH	TIO, SIO, or HIO function indicator
TTA	Starts asynchronous send cycle (transmitter activate)
TTSH	DCA (TIO, TSH, SIO, or HIO) logic
TTSHDCA	Signal derived from TTSH and DCA terms
UNE	Unusual end for odd or even channel
UNE0	Unusual end for even channel
UNE1	Unusual end for odd channel
UNEP	Unusual end driver for PET indicator
UNETSH	Unusual end status bit for TSH status
WBR0-WBR7	Synchronous write data buffer register (synchronous data set only)
WRITE	Write order flip-flop
WRTCYC	Write cycle state
WRTGO	Write cycle go control (transfer from outwait state to data output state)
WRTSLS	Write or send long space control

3-6 TIO or TDV

The DSC, in acknowledging a TIO or TDV function indicator from the IOP, supplies status information to the IOP on function response lines FR0 through FR7 and condition code lines DORD and IORD. The gating of data onto FR0 through FR7 and DORD and IORD lines is done by the

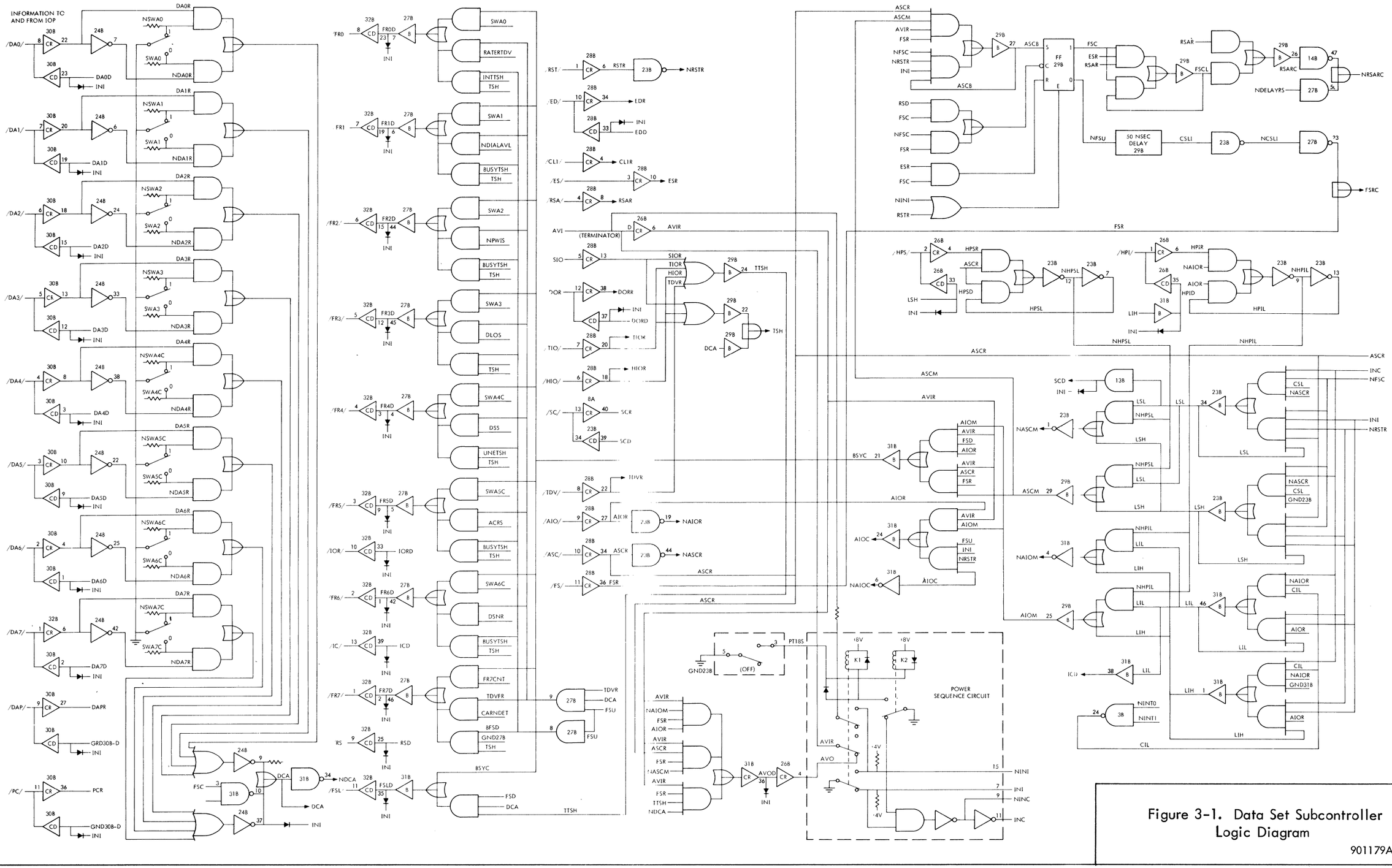

Figure 3-1. Data Set Subcontroller Logic Diagram

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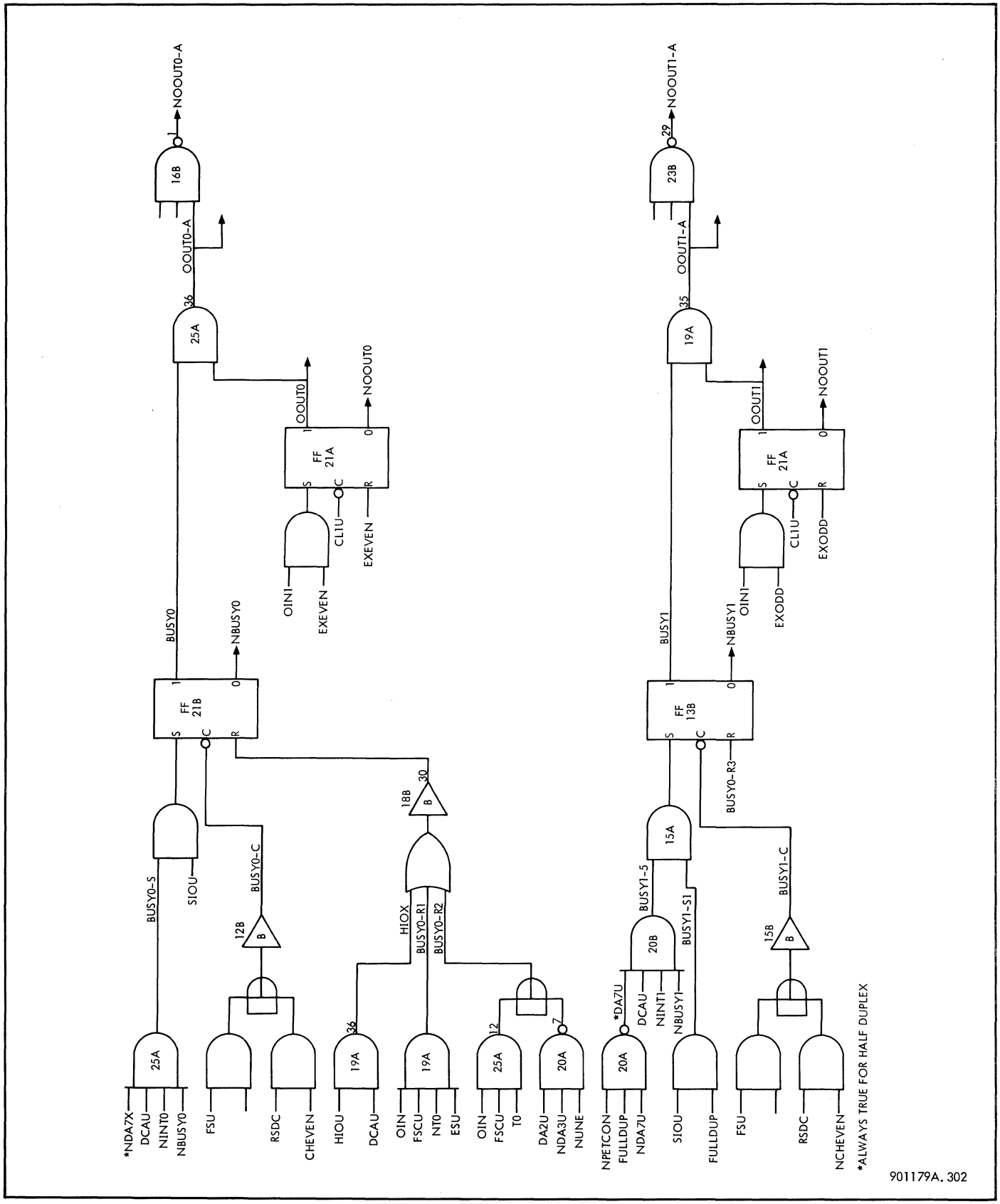


Figure 3-2. Flip-flops BUSY0 and BUSY1, Functional Diagram

subcontroller. The timing for a TIO or TDV function indicator is identical to the timing for an SIO function indicator. (See paragraph 2-3.)

3-7 HIO

When an HIO is issued to the DSC, the DSC responds by ceasing all communication with the data set. At the trailing edge of the function strobe, the DSC resets flip-flops BUSY0 and BUSY1 and directly resets all pertinent flip-flops within the DSC. During the HIO, the DSC reports status information to the IOP via function response lines FR0 through FR7.

3-8 AIO

When the DSC has an interrupt pending on the odd or even channel, the low priority interrupt call line to the subcontroller (CIL) is pulled high:

$$CIL = INT0 + INT1$$

The IOP acknowledges the interrupt by pulling the AIO function indicator and the function strobe (FS) lines high. During the time the FS line is high, the DSC supplies status information to the IOP. This status information is placed on data lines DA0 through DA7 and condition code lines DORD and IORD. The status of data lines DA0 through DA7 and condition code lines DORD and IORD are determined by the input/output channel accepting the AIO. In full-duplex operation, the even channel input/output address has priority over the odd channel input/output address, but in half-duplex operation, only one input/output address is available. Thus, only one interrupt can occur at a time.

When the DSC has placed the status on the data and condition code lines, the function strobe leading signal (FSL) generated by the DSC is pulled high. The IOP recognizes signal FSL by dropping signal FS. When signal FS is dropped, the condition that caused the responding interrupt to occur is removed. Conditions that can cause an interrupt on the even channel input/output address are as follows:

a. Long space received from data set (RECLSP flip-flop is set).

b. IOP halt detected during a terminal order (IOPIO flip-flop is set).

c. Carrier detect signal received from data set after an enable ring order has been executed (DISRING flip-flop is reset). An interrupt on the odd channel input/output address is caused by an IOP halt signal being detected during a terminal order (INT1 flip-flop is set).

3-9 STATES AND STATE FLOW

During full-duplex operation, the DSC has two sets of operating states. One set is associated with the odd channel input/output address; the other, with the even channel address. In half-duplex operation, the same states are used; however, in this type of operation, the various states have no relation to odd or even channel input/output address. Rather, they are used for input/output operations determined by the orders received. The various states and the function performed by each state are described in paragraphs 3-10 through 3-24.

3-10 Even Channel States

3-11 NOT BUSY STATE. The not busy state (NBUSY0) for the even channel is defined by flip-flop BUSY0 being in the reset condition. In full-duplex operation, flip-flop BUSY0 sets only when an SIO is acknowledged by the even channel. Once flip-flop BUSY0 is set, it remains set until the even channel is capable of receiving another SIO.

During half-duplex operation, the DSC responds only to an SIO on one IOP channel address, because either channel address, odd or even, sets flip-flop BUSY0. The setting of flip-flop BUSY0 during half-duplex operation represents the busy condition of the entire DSC. When flip-flop BUSY0 sets, the DSC transfers to the order output state for the even channel (OOUT0-A). Figure 3-3 illustrates the state flow diagram for the even channel input/output address during full-duplex operation.

3-12 ORDER OUTPUT STATE. The order output state is defined by signal OOUT0-A. During full-duplex operation, the DSC enters the order output state after acknowledging an SIO on an even input/output channel address. During half-duplex operation, the DSC enters the OOUT0-A state after acknowledging an SIO on either the odd or the even input/output channel address. In the OOUT0-A state, the DSC communicates with the IOP to obtain orders.

The orders obtained from the IOP determine what future action is to be performed by the DSC. If the mode of operation is full duplex, only a read, disable, enable, or disconnect order can be acknowledged. If the mode of operation is half duplex, an order to dial, write, disconnect, or send long space is acknowledged. The DSC exits the order output state and enters a new state under the conditions given in table 3-3.

3-13 INPUT WAIT STATE. The INWAIT flip-flop defines the input wait state (INWAIT). The DSC enters the INWAIT state when a read order is received from the IOP. If the DSC is communicating with an asynchronous data set when the read order is received, the DSC exits the INWAIT state and transfers to the read cycle state (READCYC) immediately. However, if the DSC is communicating with a synchronous data set when it receives the read order, the DSC will wait in the INWAIT state until the second of two consecutive start-of-transmission characters have been received from the data set before transferring to the READCYC state.

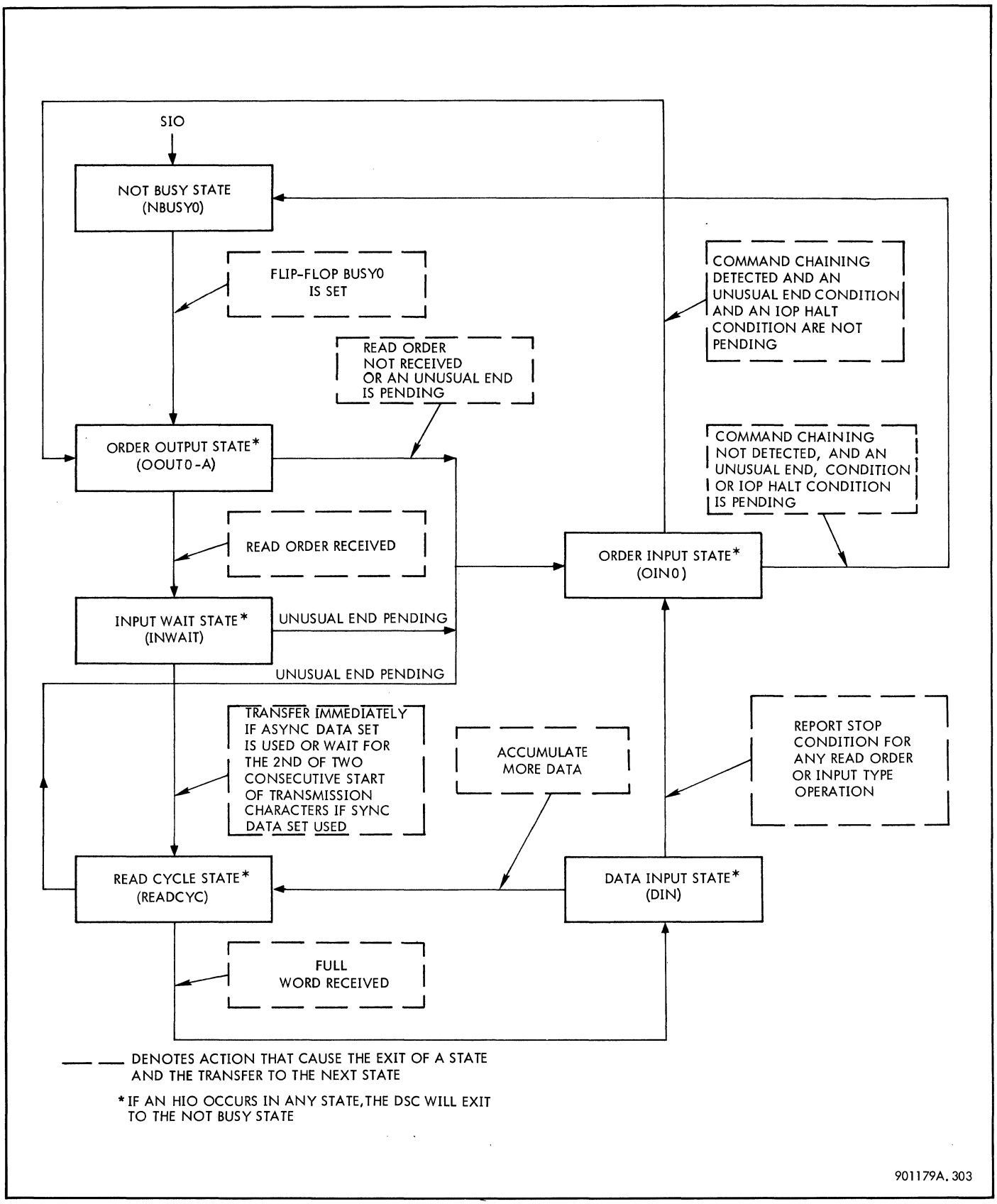


Figure 3-3. Even Channel Input/Output State (Full-Duplex Operation), Flow Diagram

Table 3-3. Exiting Conditions, Even Channel Order Output State

New State	Mode of Operation	Condition
Order input (OIN0)	Full duplex	A read order not received from IOP, or an unusual end (UNE0) detected
Order input (OIN0)	Half duplex	A read, write, dial, or send long space order not detected, or an unusual end (UNE0) detected
Input wait (INWAIT)	Full duplex	A UNE0 not pending and a read order received from IOP
Output wait* (OUTWAIT)	Half duplex	A write or send long space order received from IOP and an unusual end (UNE1) not pending
Data output* (DAOUT)	Half duplex	A dial order received from IOP and a UNE1 not pending
*In full-duplex operation, the DSC cannot transfer from the order output state (OOUT0-A) to the output wait state (OUTWAIT) or the data output state (DAOUT)		

3-14 READ CYCLE STATE. The read cycle state is defined by the READCYC flip-flop. If the DSC is communicating with an asynchronous data set when the read cycle state is entered, the DSC waits in the read cycle state until a full data word has been accumulated before transferring to the data input state. However, if the DSC is communicating with a synchronous data set when the read cycle state is entered, the DSC remains in the read cycle state until the first nonstart-of-transmission character is received from the synchronous data set.

This wait is necessary for synchronous operation because the start-of-transmission characters (approximately four) that precede each block of data must be received from a synchronous data set. After detecting only two of the start-of-transmission characters the DSC will have entered the READCYC state.

The DSC exits the read cycle state and immediately transfers to the order input state (OIN0) if an unusual end (UNE0) is detected any time during the read cycle state. If no unusual end occurs during the read cycle state, the DSC exits the read cycle state and transfers to the data input state (DIN) after a full data word has been assembled.

3-15 DATA INPUT STATE. The data input state is defined by the DIN flip-flop. In the data input state, the DSC communicates with the IOP and transfers to the IOP the accumulated data word that was assembled in the READCYC state. After transferring the data word, the DSC exits the data input state and either transfers to the order input state to report a stop condition if a stop condition is pending, or returns back to the read cycle state to accumulate more data if a stop condition is not pending. A stop condition consists of a count done received from the IOP, an unusual end pending, or the last data word received from the data set being an end-of-message character.

3-16 ORDER INPUT STATE. The order input state is defined by signal OIN0. The DSC enters the order input state when a stop condition has been detected for any read or input operation. During the order input state, the DSC communicates with and transfers data to the IOP. As soon as the DSC has transferred a word of data to the IOP, it exits the order input state and transfers to the order output state (OOUT0-A) or to the not busy state (NBUSY0). The DSC transfers to the order output state if command chaining has been detected and neither an unusual end (UNE0) condition nor an IOP halt condition is pending. The DSC transfers to the not busy state if command chaining has not been detected, and an unusual end condition or an IOP halt condition is pending.

3-17 Odd Channel States

Figure 3-4 illustrates the state flow diagram for the odd channel input/output address during full-duplex operation. Figure 3-5 illustrates the state flow diagram for half-duplex operation only.

3-18 NOT BUSY STATE. The not busy state for the odd channel input/output address during full-duplex operation is defined by flip-flop BUSY1 being reset (NBUSY1). Flip-flop BUSY1 in the DSC sets only during the acknowledgment of an SIO to the odd channel input/output address. When the DSC acknowledges an SIO on the odd channel input/output address, flip-flop BUSY1 sets and remains in the set condition until the DSC is capable of accepting another SIO on the odd channel input/output address. When the DSC accepts another SIO, the odd channel input/output section goes to the busy condition and the DSC transfers to the odd channel order output state (OOUT1-A).

3-19 ORDER OUTPUT STATE. The order output state is defined by signal OOUT1-A. In the order output state, the DSC communicates with the IOP to obtain an output order.

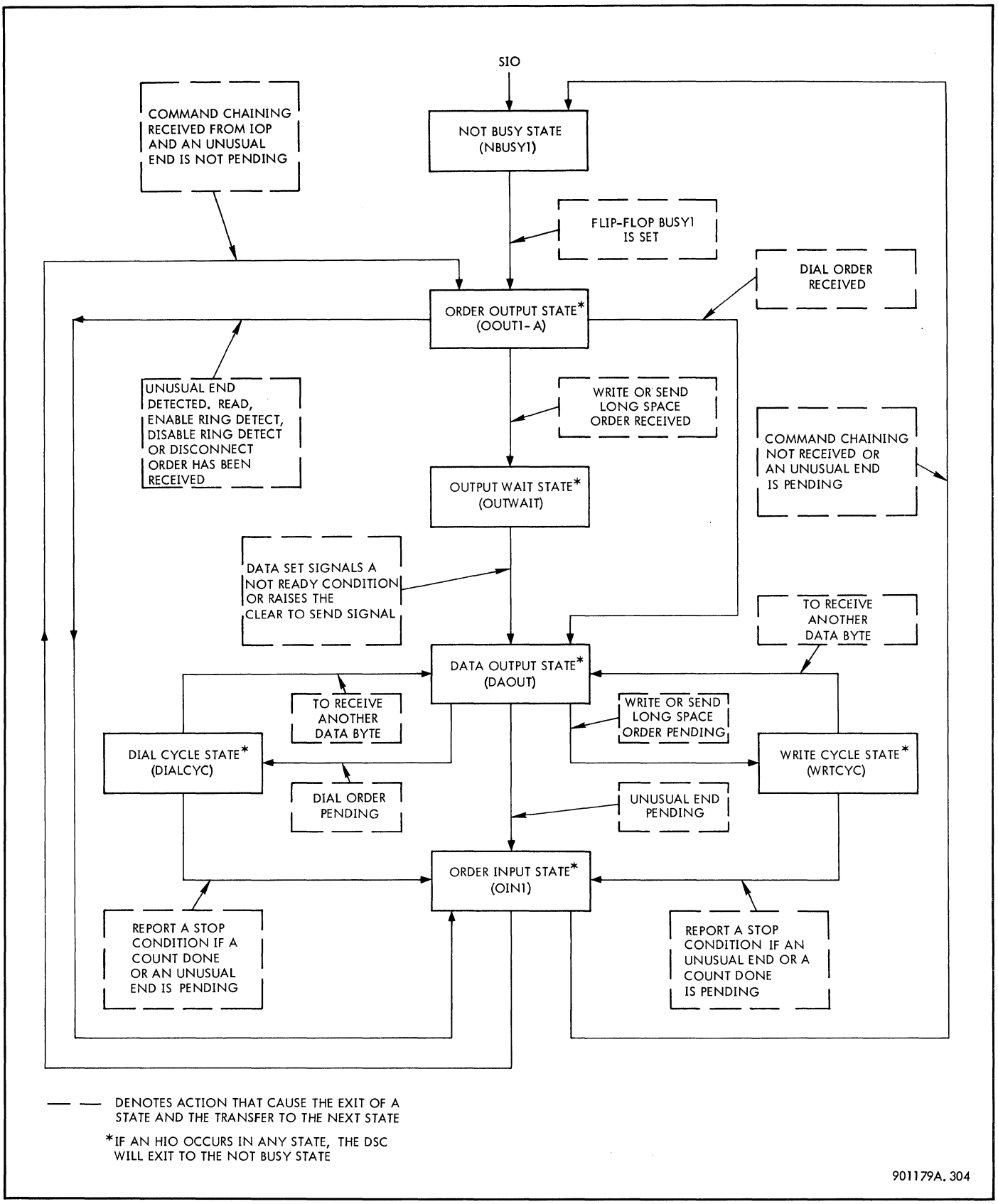


Figure 3-4. Odd Channel Input/Output State Flow Diagram

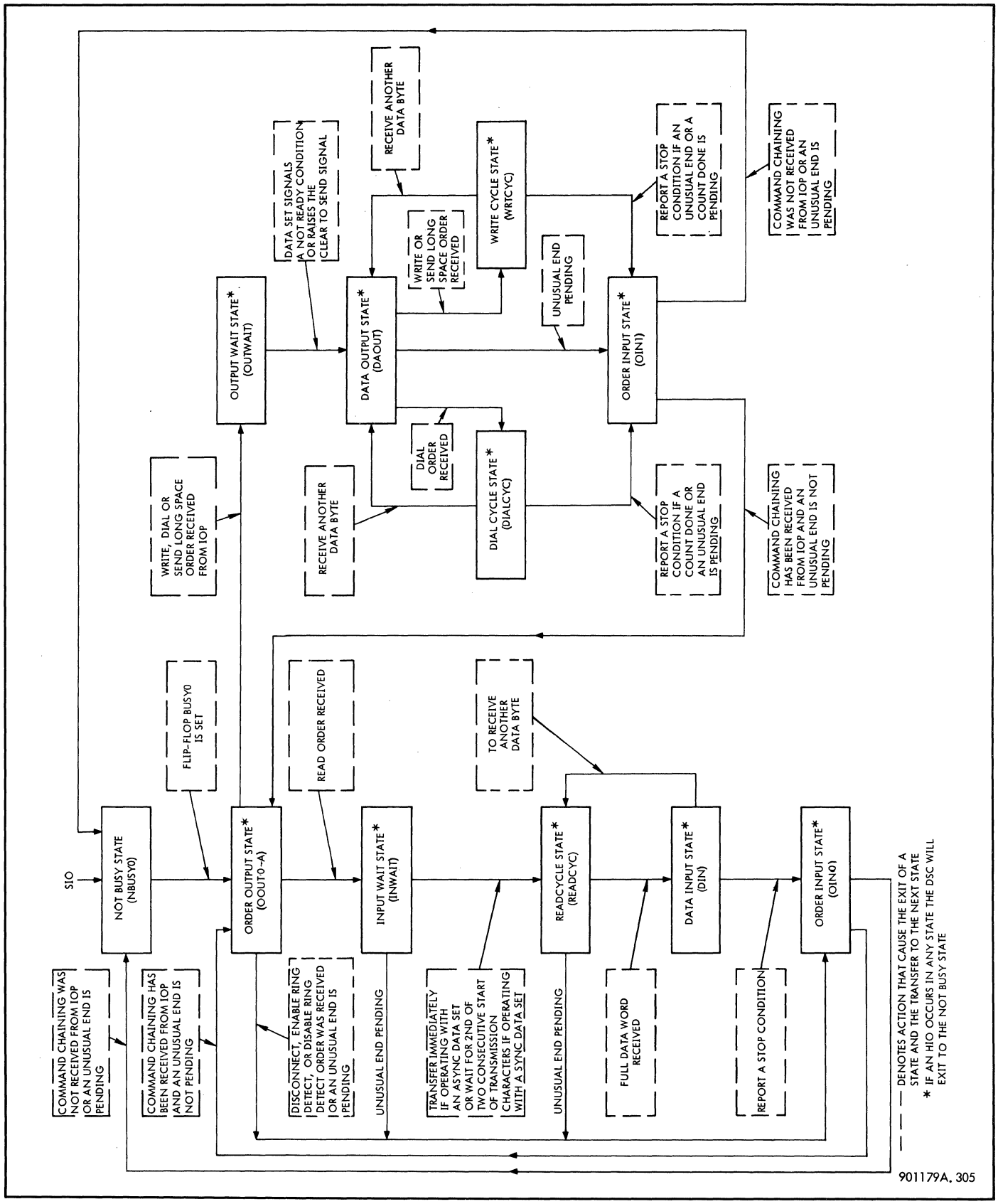


Figure 3-5. Odd Channel Input/Output State (Half-Duplex Operation), Flow Diagram

The four recognizable output orders associated with the odd channel input/output address are write, disconnect, dial, and generate long space.

If an order other than these four is received, the DSC recognizes it as a stop condition and reports channel end to the IOP via the order input state (OIN1). The DSC exits the order output state and transfers to the OIN1, OUTWAIT, or DAOUT state under the conditions given in table 3-4.

3-20 OUTPUT WAIT STATE. The output wait state is defined by flip-flop OUTWAIT being in the set condition. The output wait state is entered when an order to write or send long space has been received from the IOP. The DSC remains in the state until the data set is ready to transmit data. The data set signals when it is ready to transmit data by raising the clear-to-send signal (CLEARS). The DSC exits the output wait state when the data set signals a not ready condition or when it raises the clear-to-send signal. Upon exiting the output wait state, the DSC transfers to the DAOUT state.

3-21 DATA OUTPUT STATE. Flip-flop DAOUT defines the data output state. The DSC communicates with the IOP to obtain a data word. After obtaining the data word, the DSC exits the DAOUT state and transfers to the dial cycle state (DIALCYC), write cycle state (WRTCYC), or order input state (OIN1) under the conditions shown in table 3-5.

3-22 DIAL CYCLE STATE. Signal DIALCYC defines the dial cycle state. The dial cycle state is entered while the DSC is transferring a byte of data (last four bits) to the data set automatic call unit (ACU). When the ACU signals the DSC that the byte of data has been accepted, the DSC exits the dial cycle state. The DSC also exits the dial cycle state if an unusual end (UNE1) is detected. After exiting the dial cycle state, the DSC transfers to the order input state or data output state. The DSC transfers to the order input state to report a stop condition if a count done (CDN1) or an unusual end (UNE1) is pending. If the DSC does not have a CDN1 or an unusual end (UNE1) pending, the DSC exits the dial cycle state and transfers back to the data output state (DAOUT) to receive another byte of data.

3-23 WRITE CYCLE STATE. Signal WRTCYC defines the write cycle state. The write cycle state is entered during the time that the DSC is transferring a byte of data to the data set. The DSC exits the write cycle state and transfers to the order input state (OIN1) or DAOUT state. The DSC transfers to the order input state to report a stop condition if a count done (CDN1) or a UNE1 is pending. The DSC transfers to the DAOUT state to receive another data byte if a CDN1 or an unusual end (UNE1) is not pending.

3-24 ORDER INPUT STATE. Flip-flop OIN1 defines the order input state. The DSC enters the order input (OIN1)

Table 3-4. Exiting Conditions, Odd Channel Order Output State

New State	Mode of Operation	Conditions
Order input (OIN1)	Full duplex	Disconnect order received, write, dial, disconnect, or generate long space order not received, or an unusual end (UNE1) detected for odd channel
Output wait (OUTWAIT)	Full duplex	An unusual end (UNE1) not pending. Write or send long space order received from IOP
Data output (DAOUT)	Full duplex	An unusual end (UNE1) not pending. Dial order received from IOP

Table 3-5. Exiting Conditions, Odd Channel Data Output State

New State	Mode of Operation	Conditions
Order input (OIN1)	Full duplex	Unusual end pending
Dial cycle (DIALCYC)	Full duplex	Unusual end not pending and dial order received from IOP
Write cycle (WRTCYC)	Full duplex	An unusual end (UNE1) not pending and a write order received from IOP

state whenever a stop condition associated with the odd channel input/output address is detected. During the order input (OIN1) state, the DSC communicates with the IOP and transfers data to it. As soon as data is transferred to the IOP, the DSC exits the order input state and transfers to the even channel order output state (OOUT0-A), the odd channel order output state (OOUT1-A), the even channel not busy state (NBUSY0), or the odd channel not busy state (NBUSY1) under the conditions given in table 3-6.

3-25 SERVICE CYCLE

3-26 Service Cycle States

A service cycle is defined as the period of time during which the DSC communicates with the IOP. During this service cycle, the DSC transfers data and order information to the IOP and receives data, orders, and terminal order information from the IOP. The states of operation within the DSC that require communication with the IOP are called service cycle states. There are six service cycle states:

a. Order output state for even channel address (OOUT0-A)

b. Data input state for even channel address (DIN)

c. Order input state for even channel address (OIN0)

d. Order output state for odd channel address (OOUT1-A)

e. Data output state for odd channel address (DAOUT)

f. Order input state for odd channel address (OIN1)

Note

Reference to states such as odd and even channel input/output address holds significance only when the DSC is operating in the full-duplex mode. During half-duplex operation, there is only one input/output channel address, and the various states within the DSC are entered strictly as a result of the operation to be performed.

3-27 Service Cycle Timing (Figure 3-6)

When the DSC enters a service cycle state, the service cycle flip-flop (SERV1) is set. Flip-flop SERV1 sets on the rising edge of the 1 MHz clock from the IOP. If the service cycle state that caused SERV1 to set was associated with the even channel input/output address, the even channel flip-flop (FCHEVEN) sets:

S/FCHEVEN = OOUT0-A + DIN + OIN0 NDISCON NRESYNC

C/FCHEVEN = NSERV1

R/FCHEVEN = Always true

If the service cycle state that caused flip-flop SERV1 to set was not associated with the even channel address, flip-flop FCHEVEN resets. The odd and even channel input/output logic is formed from the FCHEVEN flip-flop:

CHEVEN = FCHEVEN

NCHEVEN = NFCHEVEN

Table 3-6. Exiting Conditions, Odd Channel Order Input State

New State	Mode of Operation	Condition
Even channel order output (OOUT0-A)	Half duplex	Command chaining received from IOP and an unusual end (UNE0 or UNE1) not pending
Even channel not busy (NBUSY0)	Half duplex	Command chaining not received from IOP or an unusual end (UNE0 or UNE1) pending
Odd channel order output (OOUT1-A)	Full duplex	Command chaining received from IOP and an unusual end (UNE1) not pending
Odd channel not busy (NBUSY1)	Full duplex	Command chaining not received from IOP or an unusual end (UNE1) pending

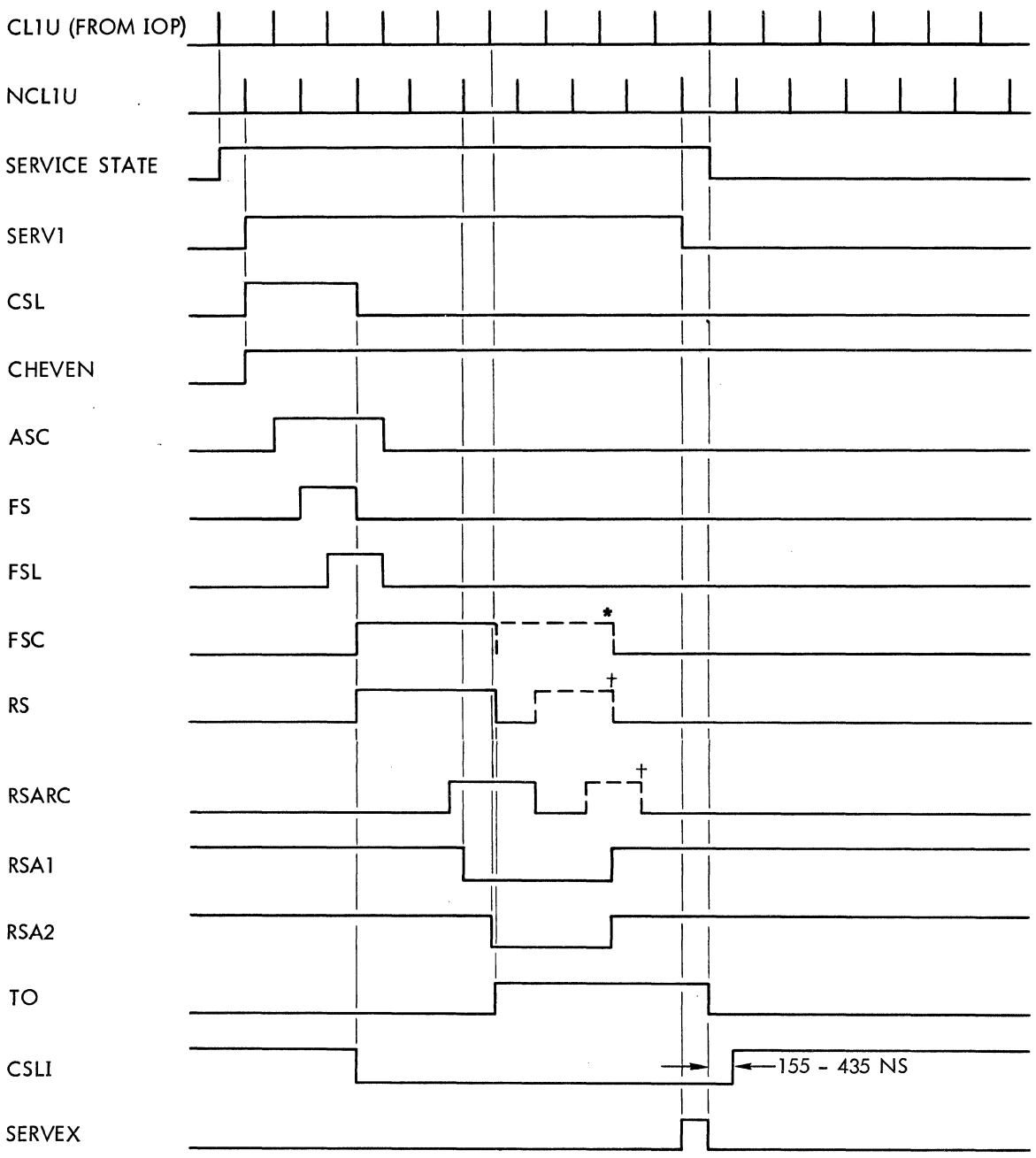


Figure 3-6. Even Channel Service Cycle, Timing Diagram

Signals CHEVEN and NCHEVEN are used to distinguish whether the service cycle is associated with the even or odd channel address. In half-duplex operation, however, both signals (CHEVEN and NCHEVEN) are always true – no distinction is made between the odd and even channel address. The reason for this is that the source of the two signals is removed and the two signal lines are left floating electrically, which denotes a true condition.

After flip-flop SERV1 is set, the low priority service call line (CSL) to the IOP is pulled high:

CSL = SERV1 CSLI

The DSC waits for the IOP to acknowledge the service call line. The IOP acknowledges the service call line by pulling the acknowledge service call line (ASC) and the function strobe line (FS) high. The DSC then places data onto the function response lines (FR0 through FR7) and the condition code lines (DOR and IOR). The data placed on data lines FR0 through FR7 represents the channel address of the DSC that is responding to signal ASC. Data placed on lines DOR and IOR represents the type of service call that is requested by the DSC. The types of calls requested by the DSC may be as follows:

a. Data input

b. Data output

c. Order input

d. Order output

After data has been placed on the function response and condition code lines, the DSC pulls the function strobe leading signal (FSL) high. When signal FSL is recognized by the IOP, data placed on the function response and condition code lines is stored in the IOP, and signal FS is dropped. When signal FS is dropped, the service connect flip-flop (FSC) in the DSC is set and signal FSL is dropped. After flip-flop FSC sets, the DSC then pulls the request strobe signal (RS) and the end data signal (ED) high. If the DSC attempts to transfer data to the IOP when the FSC flip-flop is set, the data is placed on data lines DA0 through DA7.

When the IOP recognizes the RS signal in the high state, the IOP stores the data on data lines DA0 through DA7, or if data is to be transferred to the DSC, the IOP places data onto data lines DA0 through DA7. The decision of whether to store data from data lines DA0 through DA7 or to place data on data lines DA0 through DA7 was determined by information previously transferred to the IOP via the condition code lines. The storing of data from the data lines or the placing of data onto the data lines by the IOP causes the request strobe acknowledge line (RSA) to be raised. A maximum of one microsecond after signal RSA is raised, signal RS is dropped. During the data output state or the order output state, the dropping of signal RS is delayed:

a. During data output state. To allow sufficient time after signal RSA is pulled high for reliable dc strobing of the data lines into the asynchronous send module data register

b. During order output state. To allow sufficient time for reliable dc strobing of the data lines in case a disconnect order has been executed

Control flip-flops RSA1 and RSA2 help to delay the dropping of signal RS by remaining set until signal RSA is pulled high. As soon as the IOP pulls signal RSA high, flip-flops RSA1 and RSA2 reset in synchronization with the 1 MHz clock:

R/RSA1 = RSARC NPETCON + ...

C/RSA1 = CL1U

R/RSA2 = RSARC NPETCON + ...

C/RSA2 = NCL1U

RSARC = RSAR + ...

When signal RS is dropped for the first time during any service cycle, the terminal order flip-flop (TO) is set. If data is being received from the IOP at this time, it is clocked into the appropriate storage flip-flops. During an order output state, data received from the IOP is clocked into the following control flip-flops: WRITE, DIAL, SLNGSP, READ, DISRING, and DISCON. During the data output state, data received from the IOP is clocked into data register WBR0 through WBR7 for synchronous operation or the data register on the asynchronous send module for asynchronous operation.

If terminal order information is not transferred between the IOP and the DSC, the IOP pulls the end service line (ES) high before raising signal RSA, and the DSC resets flip-flop FSC as soon as signal RS is dropped. If terminal order information is transferred between the IOP and DSC, the IOP does not raise signal ES before signal RSA, and the DSC does not reset flip-flop FSC when signal RS is dropped, but rather pulls signal RS high for a second time after signal RSA has been dropped:

R/FSC = ESR FSC

C/FSC = RSD FSC + ...

RSD = RS

When the IOP recognizes signal RS high for a second time, the IOP places terminal order information on data lines DA0 through DA7. The IOP then raises the ES line and the RSA line.

When line RSA is pulled high a second time, the DSC immediately drops signal RS. This causes the terminal order information to be clocked into the appropriate control flip-flops, and the service connect flip-flop (FSC) to be reset.

The dropping of signal RS again causes the IOP to drop signal RSA.

Information contained in a terminal order received from the IOP is as follows:

a. Interrupt. On data line 0 (sets IOPI0 or INT1 flip-flop)

b. Count done. On data line 1 (sets CDN0 or CDN1 flip-flop)

c. Command chain. On data line 2 (prevents resetting of BUSY0 or BUSY1 flip-flop)

d. IOP halt. On data line 3 (sets UNE0 or UNE1 flip-flop)

After the service connect flip-flop resets, the rising edge of the next one megacycle clock resets the SERV1 flip-flop. One-half μs after the SERV1 flip-flop resets, the terminal order flip-flop resets, causing the DSC to exit the exiting service cycle state and transfer to the next operating state.

3-28 READ ORDER TIMING SEQUENCE

The DSC has four timing sequences that can occur during the processing of a read order. Each timing sequence is unique to the data format unit installed in the DSC. One timing sequence occurs when the DSC is operating in the full-duplex mode. The second timing sequence occurs when the DSC is operating in the half-duplex mode. The third timing sequence occurs when the DSC is operating with a synchronous format unit, and the fourth timing sequence occurs when the DSC is operating with an asynchronous format unit. Each timing sequence will be considered in the following paragraphs.

3-29 Full-Duplex Versus Half-Duplex Read Order Timing

To process a read order during full-duplex operation, the DSC must first accept an SIO on the even channel address. When the SIO is acknowledged by the DSC on the even channel address, flip-flop BUSY0 sets, transferring the DSC to the order output state (OOUT0-A):

S/BUSY0 = SIOU NBUSY0 NINT0 DCAU
(NFULLDUP
+ FULLDUP NDA7U NPETCON
+ FULLDUP PETCON)

C/BUSY0 = FSU + ...

OOUT0-A = BUSY0 OOUT0

To process a read order during half-duplex operation, the DSC must first accept an SIO on either the even or odd input/output channel address. In half-duplex operation, the DSC can only respond to one input/output channel address and that address could be an odd or an even channel address. For this reason, when the DSC acknowledges an SIO during half-duplex operation, flip-flop BUSY0 always sets and transfers the DSC to the order output state associated with the even channel address (OOUT0-A). When the DSC enters the order output state (OOUT0-A), it then requests a low priority service call (CSL) from the IOP by raising the CSL line. When the IOP acknowledges the service call, the DSC sets the order control flip-flop associated with the order received from the IOP.

In full-duplex operation, the only order flip-flops that can be set during the even channel order output state are those associated with input operations. The orders and associated flip-flops are as follows:

a. Read order (set read flip-flop)

b. Disable ring order (reset ring flip-flop)

c. Enable ring order (set ring flip-flop)

In half-duplex operation, the following orders are recognized during the even channel order output state:

a. Write order (set write flip-flop)

b. Dial order (set dial flip-flop)

c. Generate long space order (set write flip-flop)

d. Disconnect order (set dc latch circuit DISCON)

e. Read order (set read flip-flop)

f. Disable ring order (reset ring flip-flop)

g. Enable ring order (set ring flip-flop)

Read orders detected during the order output state cause the DSC to transfer to the input wait state (INWAIT).

3-30 Asynchronous Read Order Timing

When the DSC is receiving data from an asynchronous data set, it responds to an SIO and transfers to the input wait state (INWAIT) in the sequence described in paragraph 3-29. One clock time after the INWAIT state is entered, the DSC transfers to the read cycle state (READCYC) if communication is with an asynchronous data set (figure 3-7). The DSC transfers through the INWAIT state when operating with an asynchronous data set for rules of logic simplification. During the read cycle state, the data input interlock flip-flop (DININLK) is set:

F/DININLK = READCYC

While operating with an asynchronous data set, the DSC waits in the READCYC state until a full byte of data has been received from the data set. An asynchronous receive module removes start and stop pulses from the data format

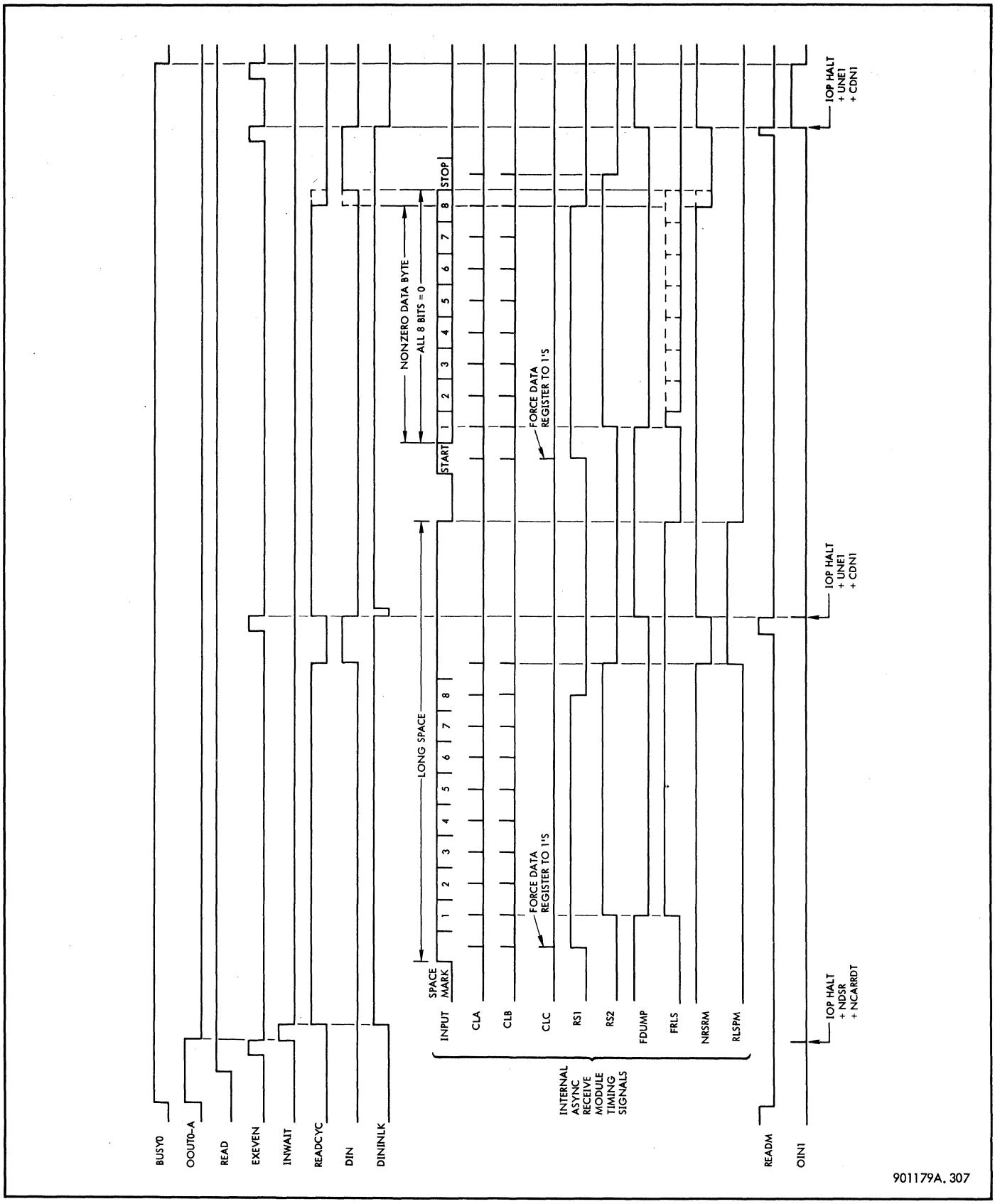


Figure 3-7. Asynchronous Read (Format 3 8L/10U), Timing Diagram

and presents only usable data bits to the DSC. Unused data bits always appear as binary ones. The asynchronous receive module signals when a full data byte has been received from the data set by pulling the receive service request signal (RSRM) high. With signal RSRM high, the DSC exits the READCYC state (reset flip-flop READCYC) and enters the data input state (set flip-flop DIN):

R/READCYC = RSRM NSYNC + ...

C/READCYC = CL1U NSYNC + ...

S/DIN = NUNE0 NDIN NREADCYC NOIN0 DININLK

C/DIN = CL1U

During the DIN state, the DSC requests a low priority service call from the IOP. When the service call is acknowledged by the IOP, the DSC transfers the accumulated data to the IOP as follows:

DA0D = RM0 (DIN NTO CHEVEN FSC)
⋮ ⋮
DA7D = RM7 (DIN NTO CHEVEN FSC)

If the DSC is still in the data input state (waiting to transfer data to the IOP) when the asynchronous receive module begins to accumulate another data byte, a rate error and an unusual end occur. The rate error (RATER0) and unusual end (UNE0) flip-flops are set:

S/RATER0 = DIN NTO

C/RATER0 = RSRM NRATER0 NSYNC + ...

F/UNE0 = DIN RATER0

During the data input state DIN the DSC sets the count done flip-flop (CDN0) if a count done terminal order was signalled to the DSC by the IOP:

S/CDN0 = DA1U TO NOIN

C/CDN0 = RSDC CHEVEN

When the DSC exits the data input state, signal READM to the asynchronous receive module is pulled high. Signal READM resets the dump flip-flop (on the asynchronous receive module) and pulls signal RSRM to ground. Signal RSRM is not pulled high again until another full data byte is received from the data set.

When the DSC completes the transfer of data to the IOP, it exits the DIN state and transfers to the order input state (OIN0) or the read cycle state (READCYC). The DSC transfers to the ION0 state to report a halt condition if a halt condition is pending. The DSC transfers back to the READCYC state to receive another byte of data if a halt condition is not pending:

R/DIN = EXEVEN

C/DIN = CL1U

S/READCYC = DIN NSERV1 NHALT0 CHEVEN NCSLI + ...

C/READCYC = CL1U DI + ...

OIN0 = BUSY0 NOOUT0 NDIN NINWAIT NDININLK NREADCYC (FULLDUP + NOUTPUTS)

NOUTPUTS = NSLNGSP NDIAL

R/DININLK = Always true

C/DININLK = EXEVEN

A halt condition consists of an unusual end (UNE0), a count done (CDN0), a detected end-of-message character (EOM), or the first character after an EOM character is detected. The coding of the EOM character is determined by the setting of seven of the switches shown in figure 3-8 (the signal comparator module). Only the seven least significant data bits are used to test for an EOM character. The eighth switch (EOMP1) shown in figure 3-8 is used to determine whether a halt condition is signalled when the EOM character is detected or when the first character after the EOM character is detected. Flip-flop FEOM is set when the EOM character is received:

S/FEOM = EOM DIN EXEVEN

C/FEOM = CL1U

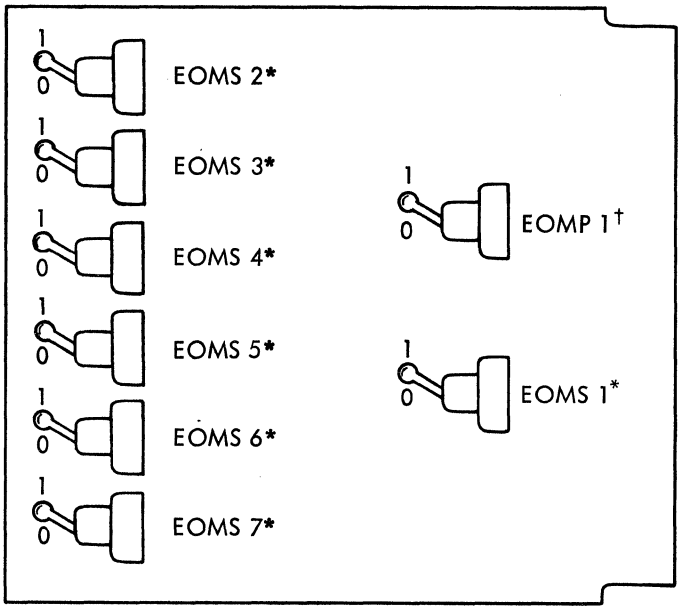
The end-of-message character is decoded by comparing switches EOMS1 through EOMS7 with data bits 1 through 7 of the receive data register (RM1 through RM7). Switch EOMP1 determines whether a halt condition (HALT0) occurs when the EOM character is received or whether it occurs on the first character after the EOM character is received (EOMP1):

HALT0 = UNE0 + CDN0 + EOM NEOMP1 + FEOM EOMP1

When the DSC transfers to the order input state (OIN0) it requests a low priority service call from the IOP. After the IOP acknowledges the service call, the DSC reports the halt condition. At the completion of the OIN0 state, the DSC transfers to the not busy state or to the order output state (OOUT0-A). Exiting from the OIN0 state and transfer to the not busy state occurs if one of the following conditions exists: command chaining not specified, unusual end (UNE0) pending, or an IOP halt pending. When the DSC transfers to the not busy state, flip-flop BUSY0 resets:

R/BUSY0 = OIN FSCU NTO ESU + OIN FSCU TO (NDA2U + DA3U + UNE)

C/BUSY0 = RSDC CHEVEN + ...



*SWITCHES USED TO DECODE END-OF-MESSAGE CHARACTER

SWITCH USED TO DETERMINE IF A HALT CONDITION IS SIGNALLED WHEN END-OF-MESSAGE CHARACTER IS DETECTED OR WHEN ONE CHARACTER AFTER THE END OF MESSAGE CHARACTER IS DETECTED. THE UP POSITION STANDS FOR END-OF-MESSAGE PLUS ONE CHARACTER AND THE DOWN POSITION STANDS FOR NOT END-OF-MESSAGE PLUS ONE (OR END-OF-MESSAGE)

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Figure 3-8. End-of-Message Decoding Switches

The DSC exits the order input state (OIN0) and transfers back to the order output state (OOUT0-A) if command chaining has been specified and neither an unusual end nor an IOP halt is pending:

S/OOUT0 = OIN EXEVEN

C/OOUT0 = CL1U

OOUT0-A = OOUT0 BUSY0

Once flip-flop BUSY0 resets, the DSC is capable of accepting another SIO from the IOP.

3-31 Synchronous Read Order Timing

When the DSC is receiving data from a synchronous data set it responds to an SIO from the IOP and transfers to the INWAIT state as described in paragraph 3-29 (for the timing diagram, see figure 3-9). The DSC waits in the INWAIT state until two consecutive synchronizing characters are received from the synchronous data set. The synchronizing characters are preselected character codes that must precede each block of data received from a data set. The coding of the synchronizing characters is determined by setting the switches shown in figure 3-10 (this setting can vary from system to system). Switches PRESYNC0 through PRESYNC7 are compared with data bits 0 through 7 of the synchronous receive data buffer register (RD0 through RD7) to decode the synchronizing characters. A minimum of two and an average of four synchronizing characters precede each block of data received from a synchronous data set.

While communicating with a synchronous data set, the DSC receives information from the IOP during the order output state that specifies the number of data bits that are to be accumulated into each data byte. This information is stored in the synchronous receive buffer register (RB0 through RB2):

S/RB0 = DA0U NDA7U

S/RB1 = DA1U NDA7U

S/RB2 = DA2U NDA7U

C/RB0-RB2 = RSDC NTO OOUT0-A CHEVEN

The receive buffer register (RB0 through RB2) is decoded to determine how many incoming data bits are to be accumulated into each data byte. A binary count of zero specifies that eight data bits are to be accumulated into each data byte. A binary count of two through seven specifies that data bits 1 through 7 are to be accumulated into each data byte.

The decoding of the receive buffer register (RB0 through RB2) also determines where the incoming serial data is to begin serially shifting into the synchronous receive data register.

A count of zero on the receive buffer register allows the incoming serial data to shift into data bit 0 of the receive data register (RD0), a binary count of seven allows the incoming serial data to shift into data bit 1 (RD1), a binary count of six allows the incoming serial data to shift into data bit 2 (RD2), and so on, until a binary count of two allows the incoming serial data to shift into data bit 6 (RD6).

The data register always shifts in a serial fashion from the most significant digit (RD0) to the least significant digit (RD7). The DSC is capable of assembling a maximum of eight data bits and a minimum of two data bits for every data byte. The unused data bits of RD0 through RD7 are always loaded with zeros.

In the INWAIT state, the DSC continuously compares the contents of the receive data register with the contents of the switches shown in figure 3-10. The switches are set to correspond to the character code of the synchronizing character that precedes each block of data transfer. When the contents of the switches agree with the receive data register contents, signal PRESYNC is pulled high, indicating that the DSC recognizes the coding of the synchronizing character. The 2NDSYNC flip-flop is set and the receive count register (RC0 through RC2) is loaded with the count that was previously stored in the receive buffer register (RB0 through RB2):

S/2NDSYNC = PRESYNC INWAIT

C/2NDSYNC = SCR

S/RC0 = RB0 INWAIT PRESYNC + ...

S/RC1 = RB1 INWAIT PRESYNC + ...

S/RC2 = RB2 INWAIT PRESYNC + ...

C/RC0-RC2 = SCR

Receive count register RC0 through RC2 in the DSC counts the number of bits to be accumulated in each data byte. When the receive count register reaches a binary count of one, signal RSRM is pulled high. On the next synchronous receive clock signal (SCR) that occurs, the DSC exits the INWAIT state and transfers to the READCYC state, provided that the DSC has accumulated another synchronizing character in receive data register RD0 through RD7.

If a second synchronizing character is not present in the receive data register, flip-flop 2NDSYNC resets and the DSC waits for the second of the next two consecutive synchronizing characters before it exits the INWAIT state:

S/2NDSYNC = INWAIT PRESYNC (Set overrides reset)

R/2NDSYNC = RSRM

C/2NDSYNC = SCR

S/READCYC = RSRM INWAIT 2NDSYNC PRESYNC + ...

C/READCYC = SCR SYNC NDIN NUNE0

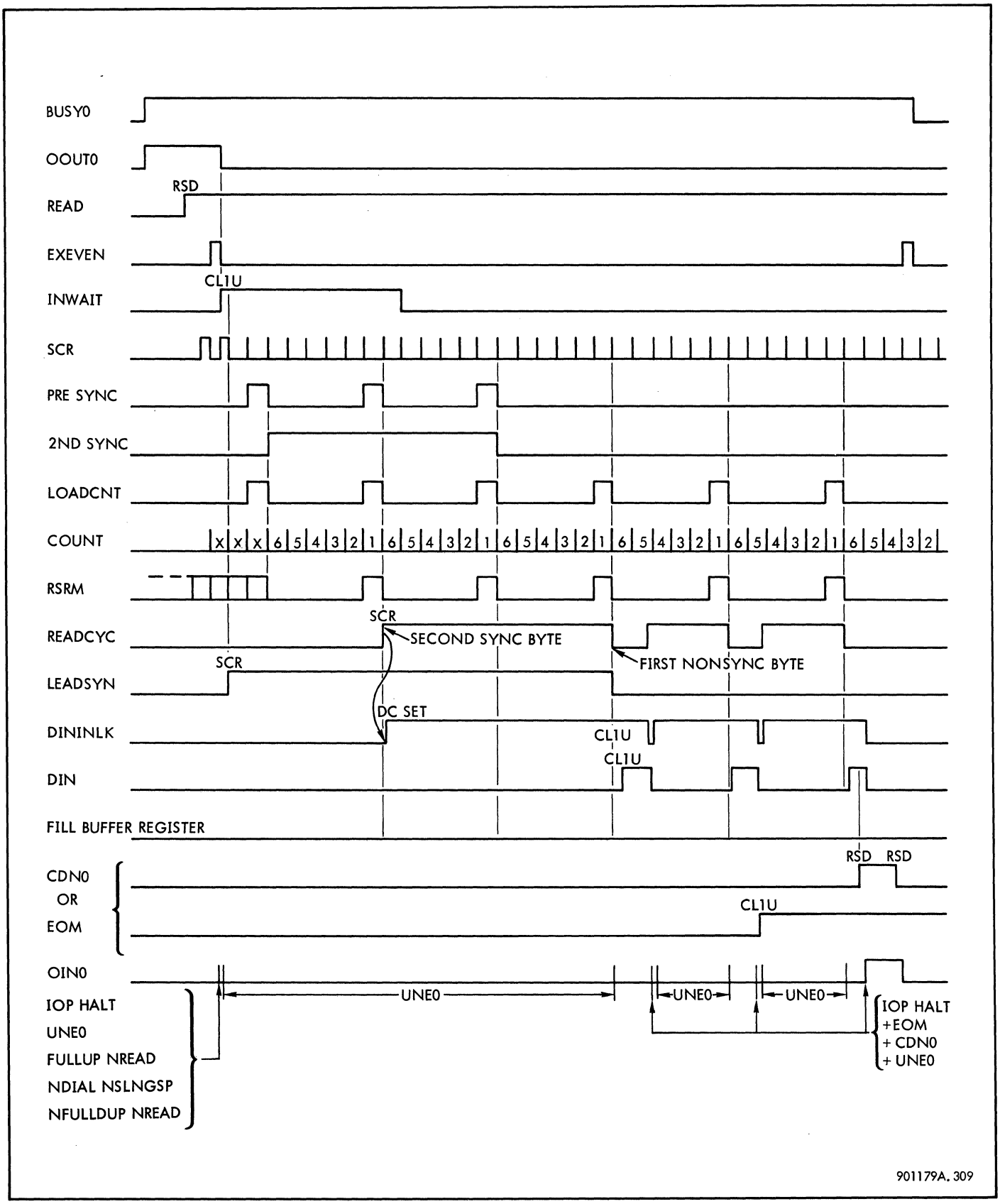

Figure 3-9. Synchronous Read (Six Bits/Byte), Timing Diagram

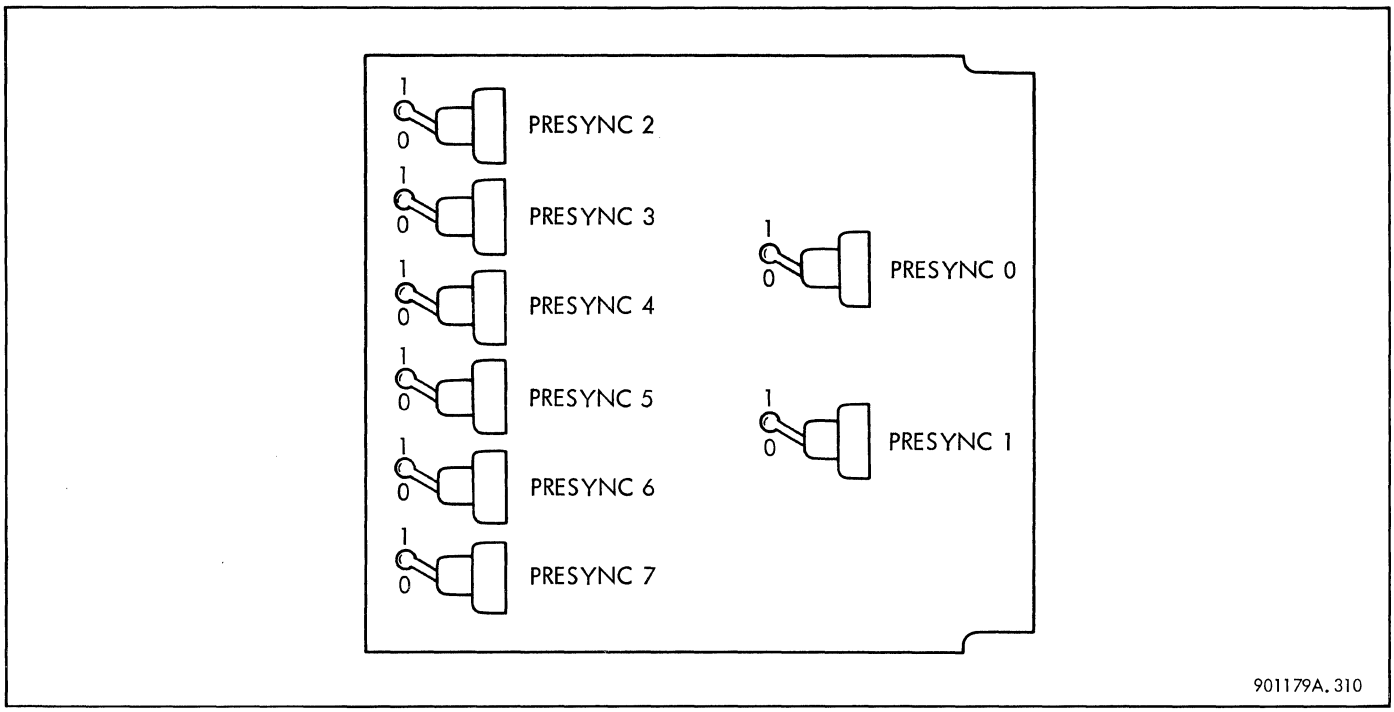

Figure 3-10. Synchronous Character Decoding Switches

R/INWAIT = READCYC

C/INWAIT = CL1U

RSRM = NRC0 NRC1 RC2

After the DSC enters the READCYC state, flip-flop DININLK is set:

S/DININLK = READCYC

In the read cycle state, the contents of receive buffer register RB0 through RB2 are transferred to receive count register RC0 through RC2 every time signal RSRM is pulled high:

S/RC0 = RB0 READCYC RSRM + ...

S/RC1 = RB1 READCYC + ...

S/RC2 = RB2 READCYC RSRM + ...

C/RC0-RC2 = SCR

RSRM = NRC0 NRC1 RC2 + ...

The DSC waits in the READCYC state until the first non-synchronizing character is received. When the first non-synchronizing character is recognized by the DSC, the DSC exits the READCYC state and transfers to the input data state (DIN). The lead synchronizing flip-flop (LEADSYNC) resets as the DSC transfers to the DIN state to allow succeeding data bytes that are decoded as synchronizing characters to be processed the same as any other data byte. The LEADSYNC flip-flop is set when the DSC enters the INWAIT state:

R/READCYC = RSRM (NPRESYNC + NLEADSYNC + ...)

C/READCYC = SCR SYNC NDIN NUNE0

S/LEADSYNC = INWAIT

C/LEADSYNC = SCR

R/LEADSYNC = RSRM NPRESYNC READCYC

S/DIN = NUNE0 NDIN NREADCYC DININLK NOIN0

C/DIN = CL1U

Each time signal RSRM goes true, the data accumulated by receive data register RD0 through RD7 is transferred to buffered receive register RM0 through RM7. Thus, whenever the DSC enters the DIN state, the data byte accumulated during the read cycle state is stored in RM0 through RM7:

S/RM0 = RSRM RD0
⋮ ⋮ ⋮
S/RM7 = RSRM RD7

C/RM0-RM7 = SCR

In the DIN state, the DSC requests a low priority service call from the IOP. When the service call is acknowledged by the IOP, the DSC transfers the contents of RM0 through RM7 to the IOP via the data lines:

```
DA0D  =  RM0 (DIN NTO FSC CHEVEN)
  :        :   :   :   :     :
DA7D  =  RM7 (DIN NTO FSC CHEVEN)
```

Note

Two data registers carry the designators RM0 through RM7. One register is used for synchronous operations, and the other is used for asynchronous operations. Since both registers perform the same function for their respective mode of operation, the outputs of the two registers are wired together. Wiring the outputs together does not affect the performance of the DSC, however, since only one of the registers is installed in the DSC at any one time.

While the DSC is in the DIN state, receive data register RD0 through RD7 continues to receive the next byte of data. If the DSC is waiting to transfer the last data byte to the IOP (the DSC is still in the DIN state) when the receive data register has received the next full byte of data, the rate error (RATER0) and unusual end (UNE0) flip-flops set:

```
S/RATER0  =  DIN NTO

C/RATER0  =  RSRM NRATER0 NSYNC + ...

F/UNE0    =  DIN RATER0
```

Also during the DIN state, the DSC sets the count done flip-flop (CDN0) if a count done terminal order is signalled to the DSC by the IOP:

```
S/CDN0  =  DA1U TO NOIN

C/CDN0  =  RSDC CHEVEN
```

When data transfer to the IOP is complete, the DSC exits the DIN state and either transfers to the order input state (OIN0) or returns to the READCYC state. It transfers to the OIN0 state to report a halt condition or a pending halt condition to the IOP. It returns to the READCYC state to receive another byte of data if a halt condition is not pending:

```
R/DIN      =  EXEVEN
C/DIN      =  CL1U
S/READCYC  =  DIN NSERV1 NHALT0
              CHEVEN NCSLI + ...
C/READCYC  =  CL1U DIN + ...
```

```
OIN0       =  BUSY0 NOOUT0 NDIN
              NINWAIT NDININLK NREADCYC
              (FULLDUP + NOUTPUTS)

NOUTPUTS   =  NSLNGSP NWRITE NDIAL

R/DININLK  =  Always true

C/DININLK  =  EXEVEN
```

A halt condition consists of an unusual end (UNE0), a count done (CDN0) or a detected end-of-message (EOM) character. When the DSC transfer to the OIN0 state, it requests a low priority service call from the IOP. After the IOP acknowledges the service call, the DSC reports halt conditions to the IOP. At the completion of the order input state (OIN0), the DSC transfers to the not busy state or to the order output state. It transfers to the not busy state if one of the following conditions exists: command chaining not specified, unusual end pending, or IOP halt pending. When the DSC transfers to the not busy state, flip-flop BUSY0 resets:

```
R/BUSY0  =  OIN FSCU NTO ESU
            + OIN FSCU NTO
            (NDA2U + DA3U + UNE)

C/BUSY0  =  RSDC CHEVEN + ...
```

The DSC exits the OIN0 state and transfers to the order output state (OOUT0-A) if command chaining has been specified, an unusual end (UNE0) is not pending, and an IOP halt is not pending. Flip-flop BUSY0 does not reset when the DSC enters the OOUT0-A state:

```
OOUT0-A  =  OOUT0 BUSY0

S/OOUT0  =  OIN CHEVEN

C/OOUT0  =  CL1U
```

Once flip-flop BUSY0 has been reset, the DSC is capable of accepting another SIO.

3-32 WRITE ORDER TIMING SEQUENCE

The DSC has four different timing sequences that occur during the processing of a write order. Each timing sequence is unique to the option installed in the DSC and the data set communicating with the DSC. The basic timing differences are given in paragraphs 3-33 through 3-35.

3-33 Full-Duplex Versus Half-Duplex Write Order Timing

To process a write order during full-duplex operation, the DSC must first accept an SIO on the odd channel input/output address. When the DSC acknowledges the SIO,

flip-flop BUSY1 sets and the DSC transfers to the order output state associated with the odd input/output channel address (OOUT1-A):

S/BUSY1 = SIOU FULLDUP NBUSY1 NINT1 DCAU (DA7U + PETCON + NFULLDUP)

C/BUSY1 = FSU + ...

OOUT1-A = BUSY1 OOUT1

To process a write order during half-duplex operation, the DSC must first accept an SIO on the odd or even channel input/output address. When an SIO is accepted, flip-flop BUSY0 sets and transfers the DSC to the order output state normally associated with the even channel input/output address (OOUT0-A):

S/BUSY0 = SIOU NBUSY0 NINT0 DCAU NFULLDUP + ...

C/BUSY0 = FSU + ...

OOUT0-A = BUSY0 OOUT0

Note

It should be remembered that during the full-duplex order output state (OOUT0-A) only input orders are decoded, but in half-duplex operation, both input and output orders are decoded during OOUT0-A. It should also be remembered that during half-duplex operations, the DSC can only respond to one input/output channel address and that channel address can be an odd or even channel input/output address.

When the DSC receives a write order during the order output state (OOUT1-A for full-duplex mode and OOUT0-A for half-duplex mode), the write flip-flop (WRITE) is set:

S/WRITE = NDA4U NDA5U NDA6U DA7U

C/WRITE = RSDC NTO OOUT NCHEVEN

Note

Signal CHEVEN is always true for half-duplex operation.

After the write flip-flop sets, the DSC transfers to the output wait state (OUTWAIT):

S/OUTWAIT = EXOUT1 NUNE1 (WRITE + SLNGSP)

C/OUTWAIT = CL1U

At the same time that the DSC transfers to the OUTWAIT state, the request to send flip-flop (RTS) is set. Flip-flop RTS controls the request to send signal to an asynchronous data set. Signal RTS to a synchronous data set is controlled by the synchronous request to send flip-flop (SYNCRS). The SYNCRS flip-flop is set on the first positive-going transition of the SCT clock pulse after flip-flop RTS has been set:

S/RTS = EXOUT1 NUNE1 (WRITE + SLNGSP)

C/RTS = CL1U

S/SYNCRS = RTS NUNE1

C/SYNCRS = NSCT

The DSC waits in the OUTWAIT state until the clear-to-send signal (CLEARS) is received from the data set. Signal CLEARS is received from the data set 8.5-150 ms after signal RTS has been sent to the data set. The data set pulls signal CLEARS high when it is capable of transmitting data.

When the clear to send signal is received by the DSC, the DSC transfers to the data output state (DAOUT) by setting the DAOUT flip-flop and resetting the OUTWAIT flip-flop:

S/DAOUT = NDAOUT OUTWAIT CLEARS + ...

C/DAOUT = CL1U

R/OUTWAIT = DAOUT

C/OUTWAIT = CL1U

3-34 Asynchronous Write Order Timing

When the DSC is transmitting data to an asynchronous data set it responds to an SIO and transfers to the data output state (DAOUT) in the sequence described in paragraph 3-33. Figure 3-11 illustrates the asynchronous write timing diagram.

During the DAOUT state, the DSC requests a low priority service call from the IOP. When the service call is acknowledged, the DSC then requests a data byte from the IOP. The data received from the IOP is stored in the asynchronous send module data register. Clock pulse TTA controls the storing of data into the data register during the DAOUT state:

TTA = DAOUT NDIAL RSDC RSARC NTO NCHEVEN NPETCON
+ DAOUT NDIAL RSDC FSCU NTO NCHEVEN PETCON

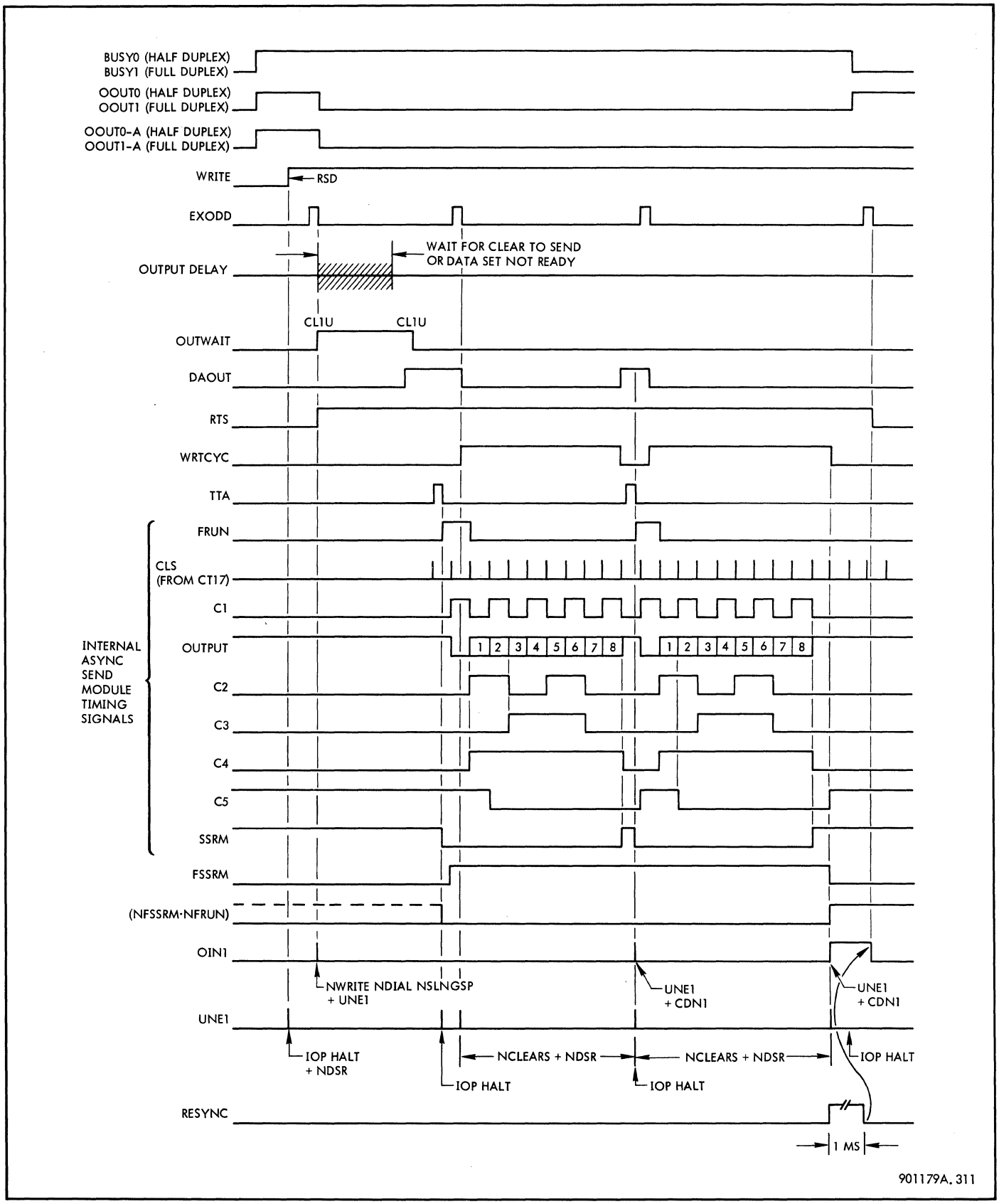

Figure 3-11. Asynchronous Write, Timing Diagram

Also during the DAOUT state, the DSC sets the count done flip-flop if a count done terminal order is signalled to the DSC by the IOP:

S/CDN1 = DA1U TO NOIN

C/CDN1 = RSDC NCHEVEN

When the DSC has received data from the IOP, the DSC then exits the DAOUT state and transfers to the write cycle state (WRTCYC) by resetting the DAOUT state flip-flop:

R/DAOUT = EXODD

C/DAOUT = CL1U

WRTCYC = RTS NDAOUT NOUTWAIT NOIN1 NSERVCN1 NSYNCWRT

During the WRTCYC state, the DSC transfers the received data from the IOP to the data set. If the data is transferred to an asynchronous data set, it is transferred in one of the four data formats described in section II. Each data format is controlled by the asynchronous send module installed in the DSC. Four different types of asynchronous send modules can be installed in the DSC. The four correspond to the four different data formats available to the DSC. Internal logic contained in each module allows the DSC to control all of the various data formats in the same manner. That is, data is loaded into the data register under the control of pulse TTA, and then the DSC waits for the asynchronous send module to pull the send service request signal (SSRM) high.

The asynchronous send module serializes data, affixes the proper start and stop pulses to the data, and transfers the serialized data to the data set through the output signal according to the data format installed in the DSC. At the beginning of the stop pulse, the asynchronous send module pulls signal SSRM high.

Some asynchronous data formats do not use all eight data bits received from the IOP. Data formats not using all eight data bits ignore the most significant data bits. For example, format 5L/7 uses only five data bits of the eight-bit data byte. The three most significant data bits of the byte are ignored.

The rate at which this serialized data is transmitted from the DSC asynchronous send module to the data set is controlled by a crystal oscillator. The frequency of the crystal oscillator is counted by binary counters CL002, CL004, and CL008 through CL16384. The clock rate frequency of each data format can be changed by changing the frequency of the crystal oscillator. The frequency of the crystal oscillator is changed by changing the crystal installed on the oscillator.

Note

All of the control signals for the four synchronous send modules are on identical pins. The clock for each data format is on a different pin. This arrangement allows all four modules to be inserted into the same module location, and yet each data format can be controlled by a different clock rate frequency.

The clock pulse sent to the asynchronous send module is synchronized with the 1 MHz clock pulse from the IOP. The logic on the 128 count (CL128) of the oscillator synchronizes the oscillator clock pulse with the 1 MHz clock pulse.

After the asynchronous send module has serially transferred the start pulse and all of the data pulses to the data set, the asynchronous send module pulls signal SSRM high. With signal SSRM high, the DSC exits the WRTCYC state and transfers back to the DAOUT state or to the odd channel order input state (OIN1). It transfers back to the DAOUT state to receive another data byte from the IOP if a halt condition is not pending. The DSC transfers to the order input state (OIN1) to report a halt condition if a halt condition is pending. A halt condition (HALT1) consists of an unusual end (UNE1) or a count done (CDN1) detected:

S/DAOUT = NDAOUT NHALT1 NSYNC WRTCYC SSRM + ...

C/DAOUT = CL1U

S/OIN1 = HALT1 NSYNC WRTCYC NFSSRM + ...

C/OIN1 = CL1U

WRTCYC = RTS NDAOUT NOUTWAIT NOIN1 NSERVCN1 NSYNCWRT

If the DSC transfers back to the data output state, the DSC repeats the previously described sequence of events by receiving another byte of data from the IOP. However, if a halt condition exists, the DSC exits the WRTCYC state and enters the order input state (OIN1) under the control of the send service request flip-flop (FSSRM). Flip-flop FSSRM delays signal SSRM by one clock pulse. This allows the asynchronous send module to transmit the stop pulse to the data set before the DSC enters the order input state (OIN1). When the DSC transfers to the OIN1 state, it requests a low priority service call from the IOP. When the service call is acknowledged by the IOP, the DSC reports the halt condition

to the IOP. After transferring the halt condition to the IOP, the DSC exits the OIN1 state by resetting flip-flops OIN1 and RTS:

R/OIN1 = EXODD

C/OIN1 = CL1U

R/RTS = EXODD

C/RTS = CL1U

When flip-flop RTS resets, the request to send signal (RTS200) is removed from the asynchronous 200 series data sets. If the DSC is communicating with an asynchronous 300 series data set, the request-to-send signal (RTS300) is not removed from the data set until the SYNCRS flip-flop has been reset. The SYNCRS flip-flop is set on the first positive-going transition of the SCT clock pulse after flip-flop RTS has been reset:

RTS200 = RTS

RTS300 = SYNCRS

R/SYNCRS = NRTS

C/SYNCRS = NSCT

After the request-to-send signal is removed from the data set, the data set drops the clear-to-send signal (CTS200 or CTS300) within 0.5 ms.

During full-duplex operation, the DSC exits the OIN1 state and transfers to the odd channel not busy state (NUBUSY1) or the odd channel order output state (OOUT1-A). Transfer is to the odd channel NBUSY1 state if command chaining has not been specified or if a halt condition is pending. The DSC transfers to the odd channel order output state (OOUT1-A) if command chaining has been specified and a halt condition is not pending. When the DSC transfers to the odd channel NBUSY1 state, flip-flop BUSY1 resets. When the transfer is to the odd channel OOUT1-A state, flip-flop OOUT1- is set and flip-flop BUSY1 is prevented from resetting:

R/BUSY1 = OIN FSCU NTO ESU
+ OIN FSCU TO
(NDA2U + DA3U + UNE)
+ ...

C/BUSY1 = RSDC NCHEVEN + ...

S/OOUT1 = OIN1 EXODD

C/OOUT1 = CL1U

OOUT1-A = OOUT1 BUSY1

During half-duplex operation, the DSC is prohibited from transferring to the odd channel NBUSY1 state and the odd channel OOUT1-A state. Instead, the DSC exits the odd channel order input state (OIN1) and transfers to the even channel not busy state (NBUSY0) or the even channel order output state. The DSC transfers to the even channel NBUSY0 state if command chaining has not been specified during the OIN1 state or if a halt condition is pending. The DSC transfers to the even channel OOUT0-A state if command chaining has been specified and a halt condition is not pending. A halt condition consists of an IOP halt or an unusual end (UNE1) detected. The DSC transfers to the even channel not busy state by resetting the BUSY0 flip-flop. The DSC transfers to the even channel order output state (OOUT0-A) by setting the order output flip-flop and not resetting the even channel busy flip-flop (BUSY0):

R/BUSY0 = OIN FSCU NT0 ESU
+ OIN FSCU TO
(NDA2U + DA3U + UNE)
+ ...

C/BUSY0 = RSDC CHEVEN + ...

S/OOUT0 = OIN EXEVEN

C/OOUT0 = CL1U

OOUT0-A = BUSY0 OOUT0

The DSC is capable of accepting another SIO after the BUSY0 (half-duplex) or BUSY1 (full-duplex) flip-flop resets.

3-35 Synchronous Timing

When the DSC is transmitting data to a synchronous data set, it responds to an SIO and transfers to the DAOUT state in the sequence described in paragraph 3-33. Before the DSC can transmit data to the synchronous data set during the order output state, the IOP must supply and the DSC must have received information specifying the number of bits that are to be transferred to the data set for each byte of data received from the IOP. This information is stored in the DSC send buffer register (SB0 through SB2):

S/SB0 = DA0U (NDA4U NDA5U
NDA6U DA7U)

S/SB1 = DA1U (NDA4U NDA5U
NDA6U DA7U)

S/SB2 = DA2U (NDA4U NDA5U
NDA6U DA7U)

C/SB0-SB2 = RSDC NTO OOUT NCHEVEN

During the DAOUT state, the DSC requests a low priority service call from the IOP. When the IOP acknowledges the service call, the DSC requests a data byte from the

IOP. Data received from the IOP is stored in the synchronous write buffer register (WBR0 through WBR7):

S/WBR0 = DA0U
⋮ ⋮
S/WBR0 = DA7U

C/WBR0-WBR7 = RSDC NTO DAOUT NCHEVEN

During the DAOUT state, the DSC sets the count done (CDN1) flip-flop if a count done is signalled to the DSC during a data output terminal order (figure 3-12):

S/CDN1 = DA1U TO NOIN

C/CDN1 = RSDC NCHEVEN

The DSC also sets the data output interlock flip-flop (DAOUTLK) during the DAOUT state:

S/DAOUTLK = DAOUT WRITE

C/DAOUTLK = CL1U

After data has been received from the IOP, the DSC exits the DAOUT state and transfers to the write cycle state (WRTCYC) by resetting flip-flop DAOUT:

R/DAOUT = EXODD

C/DAOUT = CL1U

WRTCYC = RTS NDAOUT NOUTWAIT NOIN1 NSERVCN1 NSYNCCWRT

During the WRTCYC state, the DSC initiates the start of data transfer to the data set by setting the load flip-flop (LOAD) within one μs after the synchronous transmit clock (SCT) is pulled high:

S/LOAD = NLOAD WRTCYC SCT DAOUTLK

C/LOAD = CL1U

Data transferred from the DSC to the data set is in synchronization with the positive-going transition of the data set SCT clock pulse. After the DSC detects the first SCT clock pulse during the WRTCYC state, it continues transferring data to the data set on each successive positive-going transition of the SCT clock pulse.

One μs after the load flip-flop sets, the following occurs: the load flip-flop resets, DAOUTLK flip-flop resets, and the output data register (ODR0 through ODR7) is loaded with the contents from the write buffer register (WBR0 through WBR7). That is, the first data byte and the send count register (SC0 through SC2) are loaded with the contents of the send buffer register (SB0 through SB2):

R/LOAD = Always true

C/LOAD = CL1U

R/DAOUTLK = LOAD

C/DAOUTLK = CL1U

S/ODR0 = LOAD WBR0 + ...
⋮ ⋮ ⋮ ⋮
S/ODR7 = LOAD WBR7 + ...

C/ODR0-ODR7 = LOAD CL1U + ...

S/SC0 = LOAD SB0 + ...

S/SC1 = LOAD SB1 + ...

S/SC2 = LOAD SB2 + ...

C/SC0-SC2 = LOAD CL1U + ...

On the positive-going transition of the SCT clock pulse after the DAOUTLK flip-flop has been reset, the DSC sets the synchronous write flip-flop (SYNCWRT) and transfers the first data bit to the data set (figure 3-12):

S/SYNCWRT = WRTCYC NDAOUTLK

C/SYNCWRT = NSCT

The output data register (ODR0 through ODR7) is used as a serial shift register to transfer data to the data set. Data is shifted from the most significant bit (ODR0) to the least significant bit (ODR7) of the output data register through the send data flip-flop (SD) to the data set (TD300):

TD300 = NSD
S/SD = ODR7
R/SD = Always true
C/SD = NSCT
S/ODR7 = ODR6 NLOAD + ...
S/ODR1 = ODR0 NLOAD + ...
R/ODR0-ODR7 = Always true
C/ODR0-ODR7 = NSCT (NDAOUTLK + SYNCWRT) + ...

On the positive-going transition of the SCT clock pulse that sets the SYNCWRT flip-flop, the DSC decrements the

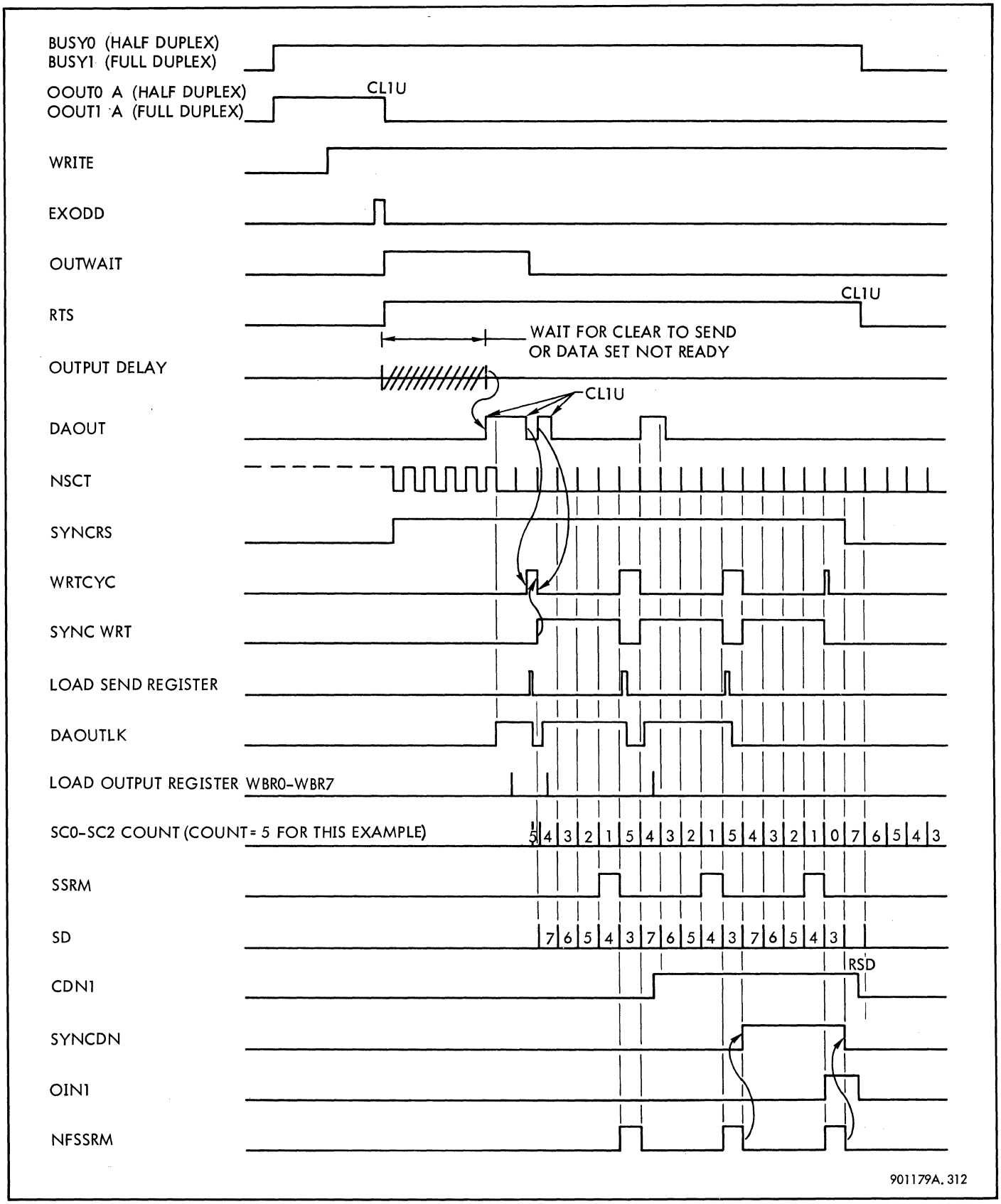

Figure 3-12. Synchronous Write (Five Bits/Byte), Timing Diagram

synchronous send counter register (SC0 through SC2). The synchronous send count register continues decrementing on each SCT clock pulse. When the synchronous send count register reaches a binary count of one, signal SSRM is pulled high to indicate that more data is required by the output data register (ODR0 through ODR7). The synchronous send count register is used to count the number of bits transferred to the data set for each data byte received from the IOP:

SSRM = SYNCWRT NSC0 NSC1 SC2

After the SYNCWRT flip-flop is set, the DSC exits the WRTCYC state and transfers to the odd channel order input state (OIN1) or the DAOUT state. The DSC transfers to the DAOUT state if a halt condition is not pending. The DSC transfers to the order input state (OIN1) if a halt condition is pending:

S/DAOUT = NDAOUT SYNC SYNCWRT NDAOUTLK (CDN1 + UNE1) + ...

C/DAOUT = CL1U

The DSC transferring back to the DAOUT state again requests a low priority service call from the IOP. When the IOP acknowledges the service call, the DSC requests another byte of data from the IOP. The write buffer register (WBR0 through WBR7) again stores the data received from the IOP. If a count done is signalled by the IOP, the DSC sets the count done flip-flop (CDN1). The DAOUTLK flip-flop is again set during the DAOUT state.

After the DSC has received the second or succeeding data bytes from the IOP, the DSC then exits the DAOUT state by resetting the data output flip-flop. If the DSC is still waiting to receive data from the IOP (DAOUT state) when the last byte of data has been transferred to the data set, a rate error occurs and the rate error flip-flop (RATER1) is set:

S/RATER1 = DAOUT SYNC

C/RATER1 = NSCT SSRM NRATER1

If the rate error flip-flop sets, the unusual end flip-flop (UNE1) sets when the DSC transfers to the WRTCYC state:

F/UNE1 = WRTCYC RATER1 CL1U + ...

After the DSC exits the DAOUT state for the second time or during successive intervals without a halt condition pending, the DSC transfers to the write cycle state when flip-flop SYNCWRT resets. The resetting of flip-flop SYNCWRT is controlled by signal SSRM. Signal SSRM is pulled high when the send count register (SC0 through SC2) reaches a count of binary one. Resetting flip-flop SYNCWRT by signal SSRM occurs when the last bit of data from the preceding data byte has been transferred to the send data (SD) flip-flop:

R/SYNCWRT = SSRM

C/SYNCWRT = NSCT

SSRM = SYNCWRT NSC0 NSC1 SC2

After flip-flop SYNCWRT resets, the DSC transfers to the write cycle state and sets the load flip-flop a second time. When the load flip-flop is set, the data output interlock flip-flop again resets; the output data register (ODR0 through ODR7) is loaded with the second byte of data from the write buffer register (WBR0 through WBR7), and the send count register (SC0 through SC2) is again loaded by the send buffer register (SB0 through SB2) with the number of bits per byte to be transmitted to the data set. On the positive-going transition of the SCT clock pulse, after the data output interlock flip-flop resets, flip-flop SYNCWRT sets and the DSC again exits the write cycle state. As the DSC exits the write cycle state for the second time, the synchronous count done flip-flop (SYNCDN) sets if a count done condition was detected in the DAOUT state:

S/SYNCDN = NOIN1 CDN1

C/SYNCDN = NFSSRM

If a count done is pending when flip-flop SYNCWRT is set, the DSC is inhibited from transferring to the DAOUT state to receive more data. Instead of transferring to the DAOUT state when flip-flop SYNCWRT sets, the DSC transfers the last data byte to the data set, and when flip-flop SYNCWRT resets, the DSC transfers to the write cycle state. When the DSC enters the write cycle state and flip-flop SYNCDN is in the set condition, the DSC transfers to the odd channel order input state by setting the odd channel flip-flop OIN1:

S/OIN1 = NOIN1 WRTCYC NFSSRM SYNCDN + ...

C/OIN1 = CL1U

While in the odd channel order input state and operating with a synchronous data set, the DSC delays requesting a low priority service call from the IOP. This delay allows the last bit of the last data byte to be transferred to the data set before communication with the data set is terminated. This delay is accomplished by the send service request flip-flop (FSSRM). Flip-flop FSSRM sets on the positive-going transition of the SCT clock pulse after signal SSRM has gone false. After flip-flop FSSRM has been set, the last bit of the last data byte will have been transferred to the data set. After this transfer, the DSC proceeds to terminate communication with the data set by requesting a low priority service call (CSL) from the IOP. The DSC requests a low priority

service call from the IOP by allowing the SERV1 flip-flop to set:

S/SERV1 = NSERV1 OIN1 NDISCON NRESYNC FSSRM + ...

C/SERV1 = NCL1U

When the IOP acknowledges the service call, the DSC transfers the halt condition to the IOP. After transferring the halt condition, the DSC exits the odd channel order input state by resetting flip-flop OIN1:

R/OIN1 = EXODD

C/OIN1 = CL1U

When the DSC exits the OIN1 state, the request to send (RTS) flip-flop also resets:

R/RTS = EXOIN1

C/RTS = CL1U

When flip-flop RTS resets, the request-to-send signal (RTS200) is removed from the synchronous 200 series data set. If the DSC is communicating with a synchronous 300 series data set, the request-to-send signal (RTS300) is removed from the data set when the synchronous request to send flip-flop (SYNCRS) has been reset. The SYNCRS flip-flop resets on the first positive-going transition of the SCT clock pulse after flip-flop RTS has been reset:

RTS200 = RTS

RTS300 = SYNCRS

R/SYNCRS = NRTS

C/SYNCRS = NSCT

After signal RTS200 or RTS300 has been removed from the data set, the data set drops the clear-to-send signal (CTS200 or CTS300) within 0.5 ms.

Whether operating with a synchronous data set or an asynchronous data set, the DSC exits the OIN1 state under the same condition.

3-36 DIAL ORDER TIMING SEQUENCE (Figure 3-13)

The DSC can dial a distant data set through the normal switched telephone network. In order to do this, the DSC communicates with an automatic call unit (ACU). The DSC transfers dialing information to the ACU. The ACU makes the telephone connection. The DSC communicates with the ACU every time a dial order is received from the IOP. Dial orders can be received from the IOP while the DSC is operating in the full- or half-duplex mode of operation. In either mode, the dial order flip-flop (DIAL) is set during the order output state (OOUT0-A) for half duplex and the order output state (OOUT1-A) for full duplex:

S/DIAL = DA5U NDA6U DA7U

C/DIAL = RSDC NTO OOUT NCHEVEN

The DSC accepts an SIO from the IOP in full- or half-duplex operation and transfers to the order output state in the same manner as described for a write order (paragraphs 3-33 through 3-35). When the DSC exits the order output state with a dial order pending, it transfers to the DAOUT state by setting flip-flop DAOUT:

S/DAOUT = DIAL EXOUT1 NUNE1 + ...

C/DAOUT = CL1U

In the DAOUT state the DSC requests a low priority service call from the IOP. When the service call is acknowledged, the DSC then requests a data byte from the IOP. Data received from the IOP is stored in the bit register (BIT1 through BIT4):

S/BIT1 = DA7U

S/BIT2 = DA6U

S/BIT3 = DA5U

S/BIT4 = DA4U

C/BIT1-BIT4 = RSDC NTO DAOUT NCHEVEN

During the DAOUT state, and for a dial order only, the four least significant data bits of the data byte are used. The DSC sets the count done flip-flop if a count done condition is signalled to the DSC during a data output terminal order:

S/CDN1 = DA1U TO NOIN

C/CDN1 = RSDC NCHEVEN

When the DSC has received the data from the IOP, the call request flip-flop (FCRQ) sets, the DAOUT flip-flop resets, and the DSC transfers to the dial cycle state (DIALCYC):

R/DAOUT = EXODD

C/DAOUT = CL1U

S/FCRQ = DAOUT EXODD DIAL NONE1

C/FCRQ = CL1U

DIALCYC = FCRQ NDAOUT NOIN1

Signal FCRQ is sent to the ACU as a call request signal (CRQ). Signal CRQ signals the ACU when the DSC wants to dial a distant data set. The DSC takes no further

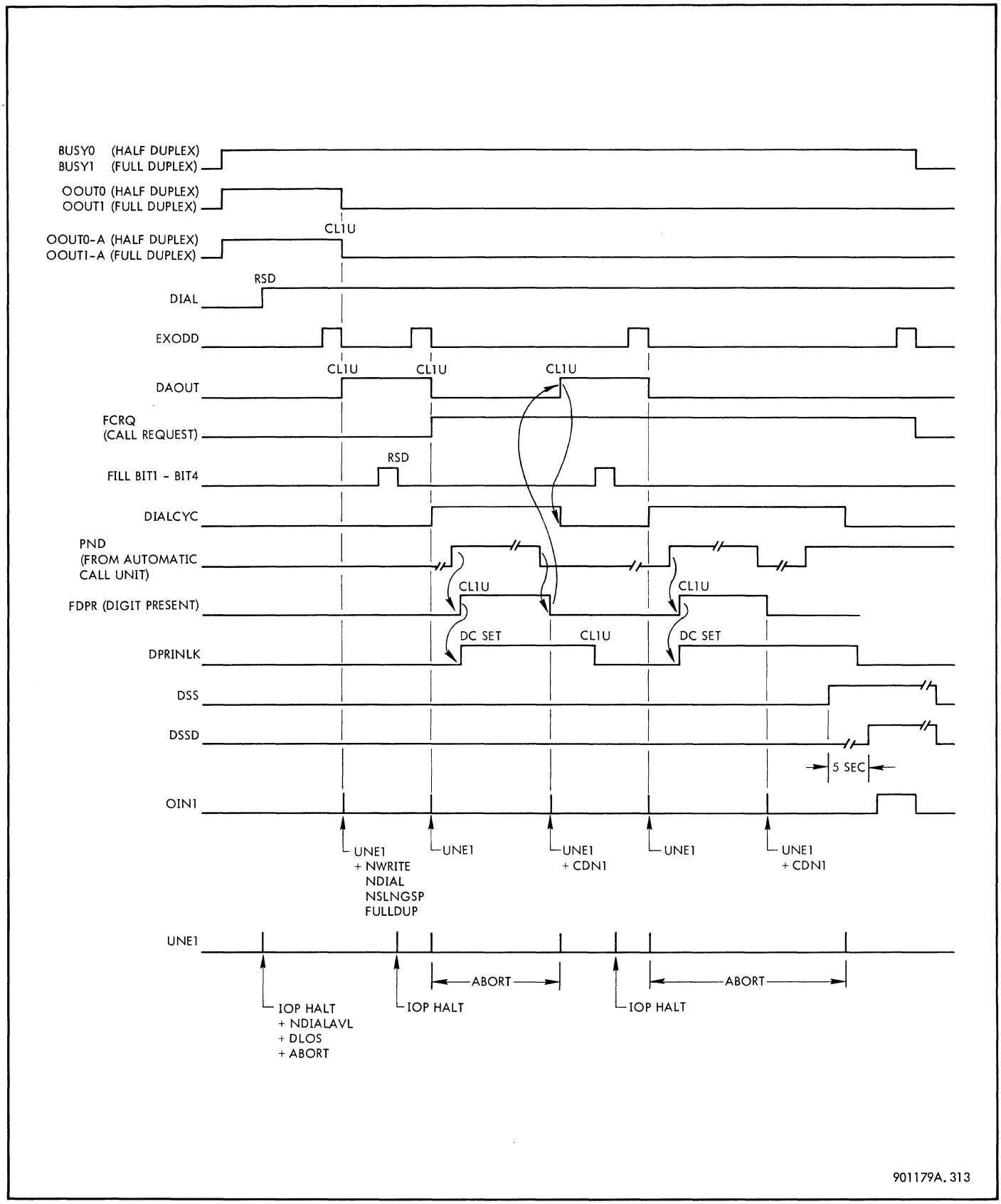

Figure 3-13. Dial Order, Timing Diagram

action in the dial cycle state until the ACU raises the present next digit signal (PND):

CRQ = FCRQ

When the ACU recognizes signal CRQ, it makes the telephone line associated with the data set go to an off-hook condition. This condition is similar to the busy condition of an ordinary telephone when the receiver is off the cradle – any other telephone user who dials that particular telephone number receives a busy signal.

Signal PND is pulled high when the ACU is ready to simulate dialing of the first telephone number. The ACU decodes the digit to be dialed from signals NB1 through NB4.

When the DSC recognizes signal PND, the DSC sets the digit present flip-flop (FDPR) and the digit present interlock flip-flop (DPRINLK). The digit present flip-flop signals the ACU via the digit present signal (DPR) that the four data bits (NB1 through NB4) can be sampled by the ACU:

S/FDPR = DIALCYC NDPRINLK

C/FDPR = CL1U

DPR = FDPR

NB1 = BIT1

NB2 = BIT2

NB3 = BIT3

NB4 = BIT4

F/DPRINLK = FDPR

After the ACU samples the four data bits, signal PND is dropped. When signal PND is dropped, the DSC resets the FDPR flip-flop:

R/FDPR = NPND

C/FDPR = CL1U

When flip-flop FDPR resets, the DSC exits the dial cycle state. If a halt condition is not pending, the DSC transfers to the DAOUT state to receive another byte of data. If a halt condition is pending, the DSC transfers to the odd channel order input state to report the halt condition. A halt condition consists of a detected unusual end (UNE1) or a count done (CDN1) condition:

S/DAOUT = DIALCYC NFDPR DPINLK NUNE1 NCDN1 + ...

C/DAOUT = CL1U

S/OIN1 = DIALCYC UNE1 + ...

C/OIN1 = CL1U

If a halt condition is not pending, the DSC continues to transfer to the DAOUT state to receive additional bytes of data from the IOP until all dialing digits have been transferred to the ACU. When the last dialed digit has been transferred to the DSC, flip-flop CDN1 is set during the terminal order of the data output state:

S/CDN1 = DA1U TO NOIN

C/CDN1 = RSDC NCHEVEN

If a count done is pending during the dial cycle state, the DSC does not exit the dial cycle state when flip-flop FDPR resets. Instead, the DSC waits for the ACU to raise the data set status signal (DSS). Signal DSS is pulled high by the ACU when the call that has been dialed by the ACU is answered by a distant data set. If the number dialed by the ACU is not connected to the data set, if the telephone number is incorrectly dialed, or if the dialed data set is not in the automatic answer mode, the call is not answered. A data set answering a call is similar to an individual removing the receiver from the cradle of an ordinary telephone when the telephone is ringing. If a call is not answered within a fixed interval of time, a signal called abandon call and retry (ACR) is pulled high by the ACU. When signal ACR is received by the DSC, flip-flop UNE1 is set and the DSC terminates the attempted dialing operation by transferring to the odd channel order input state:

F/UNE1 = DIALCYC ABORT

ABORT = ACR + NPWI

S/OIN1 = DIALCYC UNE1 + ...

C/OIN1 = CL1U

The amount of time between the dialing of the last digit by the ACU and the raising of signal ACR due to an unanswered call is selected by a manual control on the ACU. This control can be set between 7 and 40 seconds, in increments of 7, 10, 15, 25, or 40 seconds.

When the call initiated by the ACU is answered by a distant data set, the ACU places the local data set in the data mode and then raises signal DSS. For some telephone data sets, the ACU pulls signal DSS high before the data set is capable of transmitting data. However, under the worst case condition the data set will be capable of transmitting data 3.6 seconds after signal DSS has been pulled high.

To allow for the worst case data set conditions, the DSC does not respond to the data set in the data mode until five seconds after signal DSS has been pulled high. Signal DSS is delayed by the DSC adjustable five second one-shot multivibrator (DSSD) being pulled high five seconds after signal DSS goes high. When signal DSSD is pulled high, the DSC exits the dial cycle state and transfers to the odd channel order input state by setting flip-flop OIN1:

S/OIN1 = DIALCYC CDN1 NFDPR DPRINLK DSSD + ...

C/OIN1 = CL1U

DIALCYC = FCRQ NDAOUT NOIN1

The DSC enters the OIN1 state to report a halt condition to the IOP. In this state, the DSC also requests a low priority service call from the IOP. When the service call is acknowledged, the DSC transfers the halt condition to the IOP. After this transfer, the DSC exits the odd channel order input state by resetting flip-flop OIN1:

R/OIN1 = EXODD

C/OIN1 = CL1U

When processing a dial order, the DSC exits the OIN1 state under the same conditions that it exits the OIN1 state when it transmits data to a synchronous or asynchronous data set.

3-37 DISCONNECT ORDER TIMING SEQUENCE

After the DSC has completed transmitting and receiving data from the data set, the DSC must hang up the local data set in a fashion that is similar to hanging up a regular telephone, by placing the receiver back on the cradle. The DSC performs the hangup by executing a disconnect order, which disconnects the data set on both transmitting and receiving channels. Disconnect orders should never be executed unless the DSC is completely finished transmitting and receiving data.

The disconnect order can be executed on either channel. When the disconnect order is received during an odd or even channel order output state, the disconnect logic (DISCON) latches in the true state:

DISCON = OOUT RSDC NTO RSARC DA4U DA6U DA7U + DISCON DSR

DSR = DSR200 or DSR300

After a disconnect order has been received, the DSC exits the order output state (odd or even) and transfers to the order input state (OIN0 or OIN1). When the DSC enters the order input state, the DSC delays requesting a low priority service call until the data set has been completely disconnected from the telephone lines by the DISCON signal.

When signal DISCON is pulled high, the DSC removes the data terminal ready signal (DTR200) from the asynchronous data sets and the synchronous 200 series data sets.

Approximately 50 ms after the DSC removes the data terminal ready signal, the data set signals the DSC that it is disconnected from the telephone line by dropping signal DSR200. This causes the DSC to drop the DISCON signal and request a low priority service call (CSL) from the IOP by setting the SERV1 flip-flop:

S/SERV1 = OIN0 NDISCON NRESYNC + OIN1 NDISCON NRESYNC NSYNC

C/SERV1 = NCL1U

CSL = SERV1 CSL1

When the service call is acknowledged by the IOP, the DSC signals channel end to the IOP. The DSC exits the order input state (OIN0 or OIN1) and transfers to the not busy state or, if command chaining has been specified during the terminal order of the order input state, the DSC transfers to the order output state (OOUT0-A or OOUT1-A).

The synchronous 300 series data set cannot operate on a switched telephone network line, and as a result, if a disconnect order is attempted while the DSC is operating with a synchronous 300 series data set, the DSC responds by immediately reporting a channel end to the IOP. This is due to the disconnect latch (DISCON) on a synchronous 300 data set being grounded during operation. If a disconnect order is attempted, the DSC requests a service call and signals a channel end to the IOP immediately upon entering the order output state.

3-38 DISABLE OR ENABLE RING ORDER TIMING SEQUENCE

The DSC has the capability of enabling or disabling the ring detect circuit within the DSC. Enabling or disabling this circuit generates an interrupt when a distant data set begins transmitting data to the local data set.

To enable the ring detect circuit, the DSC must first receive an SIO and transfer to the even channel order output state by setting the even channel busy flip-flop. If the DSC is operating in full-duplex, the SIO must be received on the even channel. If the DSC is operating in half-duplex, the SIO can be received on either the even or odd channel input/output address, but the even channel busy flip-flop will be set:

S/BUSY0 = SIOU NBUSY0 NINT0 DCAU FULLDUP + SIOU NBUSY0 NINT0 DCAU NFULLDUP (PETCON + NDA7U)

C/BUSY0 = FSU + ...

OOUT0-A = OOUT0 BUSY0

When the DSC enters the order output state associated with the even channel address, the DSC requests a low priority service call from the IOP. When the IOP acknowledges the service call, the DSC sets the order control flip-flop associated with the order received from the IOP. If the order received from the IOP is an enable or disable ring detect order, the disable ring detect flip-flop (DISRING) then resets or sets, respectively:

S/DISRING = NDA4U NDA5U DA6U DA7U

R/DISRING = NDA4U DA6U DA7U

C/DISRING = RSDC OOUT0-A NTO CHEVEN

Note

The set condition overrides the reset.

After flip-flop DISRING sets or resets, the DSC exits the OOUT0-A state and transfers to the even channel order input state (OIN0). When the DSC enters the OIN0 state, it requests a low priority service call from the IOP. When the IOP acknowledges the service call, the DSC exits the OIN0 state and transfers to the not busy state for the even channel if command chaining was not specified during the OIN0 state, or to the order output state (OOUT0-A) if command chaining was specified during the OIN0 state.

If the disable ring flip-flop has been reset, the DSC generates an even channel input/output interrupt (INT0) whenever the next carrier detect signal is received from the data set. The carrier detect signal (NCARNDET) sets the ring flip-flop:

S/RING = NRING

C/RING = NRING NDISRING NCARNDET CL1U + ...

INT0 = RING + ...

The carrier detect signal is received from the local data set whenever a carrier signal has been established between the two data sets. The carrier detect signal is established when the two data sets have been connected through a telephone network and one data set begins transmitting data to the other. For some sets, the carrier detect signal is established as soon as the two data sets are connected together, before any data is transmitted between the sets.

3-39 AUTOMATIC HANGUP

There is a possibility that a regular telephone user may dial the number of the data set connected to the DSC; if this happens, the local data set connects to the telephone line, but is not able to receive any data because only a distant data set and not a human voice can transmit data to the local data set. When the local data set has been connected to the telephone line, it signals the DSC by raising the data set ready signal (DSR). Once the local data set has been connected to a telephone line it must hang up before another distant data set can be connected to the local data set. This is similar to a regular telephone user placing the telephone receiver on the cradle at the end of a telephone conversation. When a regular telephone user dials the number of the data set connected to the DSC, the data set raises the data set ready signal (NDSNR), but does not raise the carrier detect signal (NCARNDET).

Having signal NDSNR high and signal NCARNDET low allows the DSC to determine whether the local data set is connected to the telephone network due to a faulty telephone call. If the DSC recognizes signal NDSNR high for 30 seconds without signal NCARNDET, the DSC automatically disconnects the data set from the telephone network by dropping the data terminal ready signal. The data set in turn signals the DSC that it is disconnected from the telephone network by dropping signal NDSNR. The DSC then raises the data terminal ready line to allow future calls to be accepted by the data set.

The DSC disconnects the data set from the switched telephone network if a misplaced telephone call is placed on the line by activating a special 30 second one-shot timing multivibrator. The output of this multivibrator remains high as long as the input stays high and for 30 seconds after the input is removed. When the input to the multivibrator drops to ground (longer than 30 seconds), the output (hangup) drops to ground and removes the data terminal ready signal (DTR200) from the data set:

S/HANGUP = NDSNR NCARNDET + DSNR CARNDET

DTR200 = NDISCON HANGUP

Due to the automatic hangup feature of the DSC, it is necessary for some data sets to receive data within 30 seconds after the telephone connection has been established between the two data sets. In some data sets, such as the 202C, the data set ready signal (NDSNR) is pulled high when connection between the two data sets has been completed, but signal NCARNDET is not received until data is transmitted. Thus, for data set 202C, if data is not received within 30 seconds after the two data sets have been connected (signal NDSNR high), the data set is disconnected by the HANGUP signal dropping signal DTR200.

3-40 PET OPERATION (Figure 3-14)

The peripheral equipment tester (PET) can only operate with the DSC when the full-duplex option is installed in the DSC. The simulated SIO executed by the PET activates both the even and odd channel input/output address. The even and odd channels are activated by the PET, which forces flip-flops BUSY0 and BUSY1 to set each time an SIO is issued. An SIO is issued each time the function strobe switch (FS) is pressed.

Any recognizable order (read order excluded) may be placed in the order switches. The odd or even input/output channel associated with the inserted order remains active after an SIO is simulated by the PET. The remaining input/output channel reports channel end via the order input state. During an SIO, a read order is executed by placing the read switch in the up position. With the read switch up, a read order is simulated by forcing the read flip-flop to set at the proper time during the order output state (OOUT0-A).

Logic associated with each order (read order excluded) may be tested by placing the order via the order select switches on the PET and simulating an SIO. To test the logic associated with a read order, the read switch must be placed in the up position when a simulated SIO is being executed.

To activate the logic associated with each order (read order excluded), it is only necessary to place the order via the switches and simulate an SIO. When an SIO is simulated,

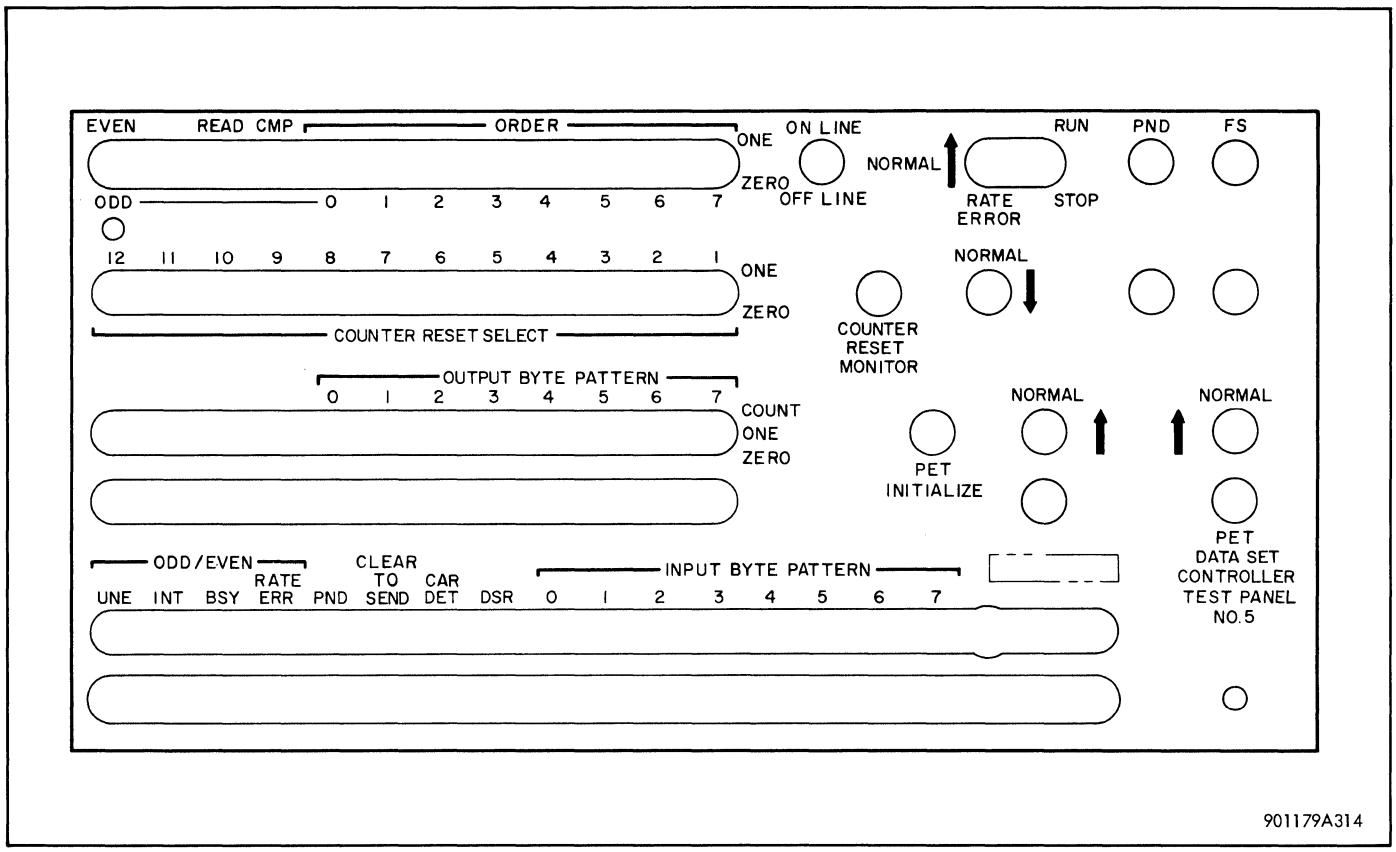

Figure 3-14. PET Panel Overlay Diagram

both channels (even and odd) become active, but only the input/output channel that processes the order in the switches remains active. The remaining input/output channel reports channel end via an order input due to an unrecognizable order.

To test logic associated with the read order, the read switch is placed in the up position, a write order is placed by means of the write switches, and an SIO is simulated. When the SIO is simulated, both channels (even and odd) remain active. One channel receives data and the other channel transmits data. With the DSC just transmitting data it is possible to loop the transmitted data back onto the data line and into the receive module. Thus, with just the transmitting signal it is possible to check the DSC transmitting and and receive logic.

Note

The data transmitted as a result of the write order being executed always comes from the OUTPUT BYTE PATTERN switches.

When the asynchronous option is installed in the DSC, it is possible to transmit, receive, and test a varying count pattern that can be placed on the OUTPUT BYTE PATTERN switches. By placing all but the most significant switch of the OUTPUT BYTE PATTERN switches to the count position and executing a read and a write order simultaneously, a binary count pattern is transmitted and received by the DSC.

If, when the DSC is transmitting and receiving data, the compare input switch (CMP) is set to the up position, the received data is compared with the data transmitted from the OUTPUT BYTE PATTERN switches. If an error occurs, the DSC detects a count done on both the even and the odd channel (CDN0 and CDN1). The DSC also reports channel end on both channels via the order input state. The compare error indicator on the PET lights to indicate the error.

Reading, writing, or both can be done in the single-step mode or the continuous-run mode by setting the STOP/RUN switch to STOP, for single-step mode; to RUN, for continuous mode. When the DSC is operating in continuous mode, the DSC can be stopped by setting the STOP/RUN switch to STOP. Doing this forces a count done condition on both channels.

When testing the DSC with the synchronous option installed, it is not possible to transmit and receive a varying count pattern. However, it is possible to transmit, receive, and

test a fixed pattern. The fixed pattern transmitted must be placed through the OUTPUT BYTE PATTERN switches. To test the synchronous logic, the proper bit/byte count must be set in the most significant three bits of the order switches and a read and a write order must be simultaneously executed in the run mode. The OUTPUT BYTE PATTERN switches must, however, first be set to represent the synchronizing character that has been set in the sync comparator circuit of the read logic. After at least two synchronizing characters have been transmitted, the true data byte must be set in the OUTPUT BYTE PATTERN switches. Only then can switch CMP be set to the up position to test for transmit and receive errors.

Note

The synchronous option can only be tested in the RUN mode.

To change the test pattern merely requires setting the CMP switch to the down position, setting the new data via the OUTPUT BYTE PATTERN switches, and setting the CMP switch back to the up position. It must be remembered that if the run sequence is stopped, at least two leading synchronizing characters must be transmitted before additional data can be recognized by the read logic.

Note

While testing the synchronous DSC logic option the sequence of operation can be stopped by setting the STOP/RUN switch to STOP. Doing this forces a count done condition on both channels.

The entire controller can be initialized from the PET by setting the OFF LINE/ON LINE switch to ON LINE. The EVEN/ODD switch on the PET is used to switch a number of even or odd channel input/output conditions onto the PET panel indicators. The following indicators represent even or odd channel conditions:

a. UNE (unusual end)

b. INT (interrupts)

c. BSY (busy flip-flop)

d. RATE ERROR (rate error flip-flop)

The remaining indicators represent the following:

a. PND (present next digit signal from ACU)

b. CLEAR TO SEND (clear to send signal from ACU)

c. CAR DET (carrier detect signal from data set)

d. DSR (data set ready signal from data set)

e. INPUT BYTE PATTERN (last data byte received from data set)

The rate error switch is used to create rate errors. When the DSC is transmitting and receiving data, a rate error can be simulated by setting the RATE ERROR switch to the down position. This generates a rate error on both the even and the odd channel by setting flip-flops BUSY0 and BUSY1 respectively. A rate error is forced by inhibited service calls as long as the RATE ERROR switch is in the down position. The RATE ERROR switch must be set back to the up position for the DSC to proceed to report the rate error condition. The RATE ERROR switch inhibits service calls by grounding the set input to the SERV1 flip-flop.

SECTION IV
MAINTENANCE AND PARTS LIST

4-1 INTRODUCTION

This section contains instructions for performing maintenance on the DSC and a list of replaceable parts, arranged in tables.

4-2 MAINTENANCE

4-3 SPECIAL TOOLS AND TEST EQUIPMENT

Table 4-1 lists the tools and test equipment required to perform maintenance on the DSC.

4-4 CLEANING AGENTS

No cleaning agents are required to clean the DSC. The only material required to remove foreign matter from the DSC is a clean, dry, lint-free cloth or a soft bristle brush.

4-5 PREVENTIVE MAINTENANCE SCHEDULE

Table 4-2 gives the preventive maintenance schedule for routine maintenance.

Table 4-1. Special Tools and Test Equipment

Name of Tool or Equipment	Part Number	Manufacturer	Quantity
Power Supply Model PT16 or equivalent	117264	XEROX	1
Oscilloscope Model 531 or equivalent		399	1
Preamplifier, type CA or equivalent		399	1
Multimeter, type 267 or equivalent		398	1
Peripheral Equipment Tester (PET) Model JT14	127492	XEROX	1
PET panel overlay	139841		1
Timing generator CT17*	135351		1
Masterite connector	115833		2
Assembly, printed wiring, NAND gate IT11†	116994		1
Assembly, modification kit, sync 200**	139855	XEROX	1

*Required when modification kit sync 200 (part no. 139855) or modification kit sync 300 (part no. 145302) is installed in the DSC

†Required if the full-duplex option is not supplied with the DSC

**Required if no other modification kit is supplied with the DSC

Table 4-2. Preventive Maintenance Schedule

Step	Routine	Frequency
1	For Sigma 2, 5, and 7 computers, run the DSC diagnostic program	As required
2	Perform the checkout procedures given in paragraphs 4-7 through 4-18	Quarterly

Table 4-3. Modification Kit Installation Checks

ITEM	MODIFICATION KIT	PART NUMBER	JUMPER REQUIRED				REMARKS
			Module	Pin No.	Module	Pin No.	
1	5L/7.5U, 60W	139846	1A	33	2B	46	Jumper wire connects the proper oscillator frequency from the CT17 module to the serial transmit clock (NSCT) during asynchronous operation. See also note 2
2	5L/7.5U, 66W	139847	1A	33	2B	46	
3	5L/7.5U, 75W	139848	1A	33	2B	46	
4	5L/7.5U, 100W	139849	1A	33	2B	46	
5	7L/9U, 148W	139850	1A	35	2B	46	
6	8L/10U, 150W	139851	1A	35	2B	46	
7	8L/10U, 1200W	139852	1A	20	2B	46	
8	8L/10U, 1800W	139853	1A	20	2B	46	
9	8L/11U, 100W	139854	1A	33	2B	46	
10	Synchronous 200	139855	7A	14 (NSCT)	7A	40 (NSCR)	See notes 1 and 2
11	Synchronous 300	145302	7A	14 (NSCT)	7A	40 (NSCR)	See notes 1 and 3
12	Auto-dial	139831	-	-	-	-	
13	Full duplex modification kit	139833	-	-	-	-	Kit consists of an IT11 module installed in module position 30A. See note 4

Note 1

When the synchronous 200 or synchronous 300 modification kit is installed in the DSC, add the output of a square wave generator (if used) to the listed pins and connect the ground return of the square wave generator to the ground plane of the DSC

Set the square wave generator output frequency to 230.4 kHz/s (approximately 4.34 μs) at an amplitude of approximately +4V. If a CT16 module is used instead ot the square wave generator, add the CT16 module to

(Continued)

Table 4-3. Modification Kit Installation Checks (Continued)

Note 1 (Continued)

module position 1B and add the following temporary jumper wires: module 1B, pin 9 to module 1B, pin 10; module 1B, pin 45 to module 7A, pin 14 and to pin 40 of module 7A; and module 1B, pin 50 to module 1A, pin 50. Adjust oscillator CT16 for 230.4 kHz per second on pin 45 of module 1B

Note 2

When one of items 1-10 is installed in the DSC, add two Masterite connectors to the NT30 module in module position 7A, and add the following jumpers to the Masterite connector that is placed on the component side of the NT30 module: 1-6, 6-9, 2-5, and 13-14

Note 3

When the synchronous 300 modification kit is installed in the DSC, temporarily ground pins 11 (NCARRDT) and 14 (NDSR) of module 8A and add two Masterite connectors to the AT43 module in module position 8A. Add the following jumper wires to the Masterite connector placed on the component side of the AT43 module: 3-13 (RTS300 to CTS300) and 7-14 (TD300 to RD300)

Note 4

If the DSC is received without the full-duplex modification kit (item 13) installed and one of the modification kits listed in items 1-10, the full-duplex kit and one of the other kits (items 1-10) must be installed in order to perform the testing procedures in paragraphs 4-7 through 4-18

4-6 PERFORMANCE TESTING (USING THE PET)

The peripheral equipment tester (PET) is used to test the performance of the DSC before the DSC is operated with a Sigma computer. Paragraphs 4-7 through 4-18 describe the procedures that are used to verify the operation of the DSC, and table 4-3 lists the thirteen different modification kits that are used to modify the operation of the DSC.

4-7 Preliminary Procedures

Paragraphs 4-8 through 4-11 describe the preliminary procedures that are to be performed before testing the DSC with the PET.

4-8 Installation Checks

Perform the following checks on the DSC during installation:

a. Visually inspect the DSC for loose or broken wires, small pieces of loose solder, and bent or loose pins.

b. Make sure that all modules are installed according to the module location chart in section I, and that they are well seated.

c. Make sure that at least one of the modification kits listed in table 4-3 is installed in the DSC, and if the full-duplex option modification kit (item 13 of table 4-3) is not supplied with the DSC, temporarily install an IT11 module in position 30A.

d. Set the ON/OFF switch on the LT25 module (located in module position 23B) to the OFF (down) position for PET operation.

e. Insert the PET cable plug modules P181 and P183 into module positions 14A and 13A respectively.

f. Add the DSC panel overlay to the front panel of the PET.

g. Using table 4-3, verify that the proper modification kit jumper wire has been installed in the DSC when any of the asynchronous modification kits (items 1 through 9 of table 4-3) is installed in the DSC.

4-9 Selecting the End-of-Message Character

Select the end-of-message character as follows:

a. Set the switches on the switch comparator module (6B) as shown in figure 4-1. Setting the switches to this configuration selects hexadecimal character 04 for the end-of-message character.

b. If an asynchronous modification kit is installed in the DSC, set all switches representing unused data bits to the 1 position.

An example of this is as follows:

If modification kit 5L/7.5U, 60W is used, only five data bits are used and the three most significant bits of an eight

bit byte are unused. As a result, set the two switches representing the two unused data bits (EOMS1 and EOMS2) to the up (1) position.

4-10 Selecting the Synchronizing Character

Select the synchronizing character as follows:

a. When the synchronous 200 or synchronous 300 modification kit is installed in the DSC, set the switches on the switch comparator module (position 12A) to the positions shown in figure 4-2. This setting selects hexadecimal character 06 for the synchronizing character.

b. Apply dc power (+4V, +8V, and -8V) to the DSC.

c. When one of the asynchronous modification kits (items 1-9 of table 4-3) is installed in the DSC, adjust the output of the CT17 oscillator module (position 1A) in the following manner:

1. Add a temporary jumper wire between pins 2 and 5 of module 1A.

2. Adjust the adjustable capacitor on module CT17 to obtain an output frequency on pin 12 of 1A that matches the frequency of the crystal installed on module CT17.

3. Remove the jumper wire between pins 2 and 5 on 1A and verify that the oscillator output frequency on pin 12 of 1A still matches the crystal frequency.

4-11 Interpretation of ODD/EVEN Switch on PET Panel Overlay

Four conditions are displayed on the PET indicators for both the odd and the even channel:

a. Unusual end (UNE indicator)

b. Interrupt (INT indicator)

c. Busy (BSY indicator)

d. Rate error (RATE ERR indicator)

When the ODD/EVEN switch on the PET panel is set to ODD, the PET indicator displays the odd channel conditions. Setting the switch to EVEN displays the even channel conditions.

4-12 Read/Write Asynchronous Test

The read/write asynchronous test is performed to evaluate the ability of the DSC to transmit and receive asynchronous data simultaneoulsy. This test is performed on all DSCs that have an asynchronous modification installed in them. Proceed as follows to perform the test:

a. Set the READ switch to the up position.

b. Set the CMP switch to the up position

c. Set the ORDER switch to hexadecimal 01.

d. Set the OFF LINE/ON LINE switch to ON LINE.

e. Set the RATE ERR switch to the up position.

f. Set the RUN/STOP switch to RUN.

g. Set COUNTER RESET SELECT switches 1 through 12 to the up position.

h. Set the OUTPUT BYTE PATTERN switches as follows:

1. Set the most significant data bit switch and the unused data bit switches to the 1 (center) position.

2. Set all the other data switches to the up (count) position. For example, using the 5L/7.5U, 60W format, only five data bits are used. As a result, the unused data bit switches (0 through 2) and the most significant data bit switch (3) are set to the 1 (center) position. Set all other data bit switches (4 through 7) to the up (count) position.

i. Press the COMPARE ERROR switch to extinguish the compare error indicator if it is lit.

j. Initialize the DSC by setting the OFF LINE/ON LINE switch to OFF LINE, and then back to ON LINE and check that the following occurs:

1. The UNE, INT, BSY, and RATE ERR indicators for the odd and even channels and the PND and the CLEAR TO SEND indicators extinguish.

2. The DSR and CAR DET indicators light.

3. The INPUT BYTE PATTERN indicators are indeterminate.

k. Press the PET INITIALIZE switch.

l. Press switch FS. The DSC begins transmitting and receiving data. The following indications should then be observed:

1. The UNE, INT, and RATE ERR indicators for the odd and even channels and the PND indicator remain extinguished.

2. The BSY indicator lights for the odd and even channels after switch FS is released.

3. The CLEAR TO SEND indicator lights after switch FS is released.

4. The DSR and CAR DET indicators remain lit.

5. The INPUT BYTE PATTERN indicators flicker.

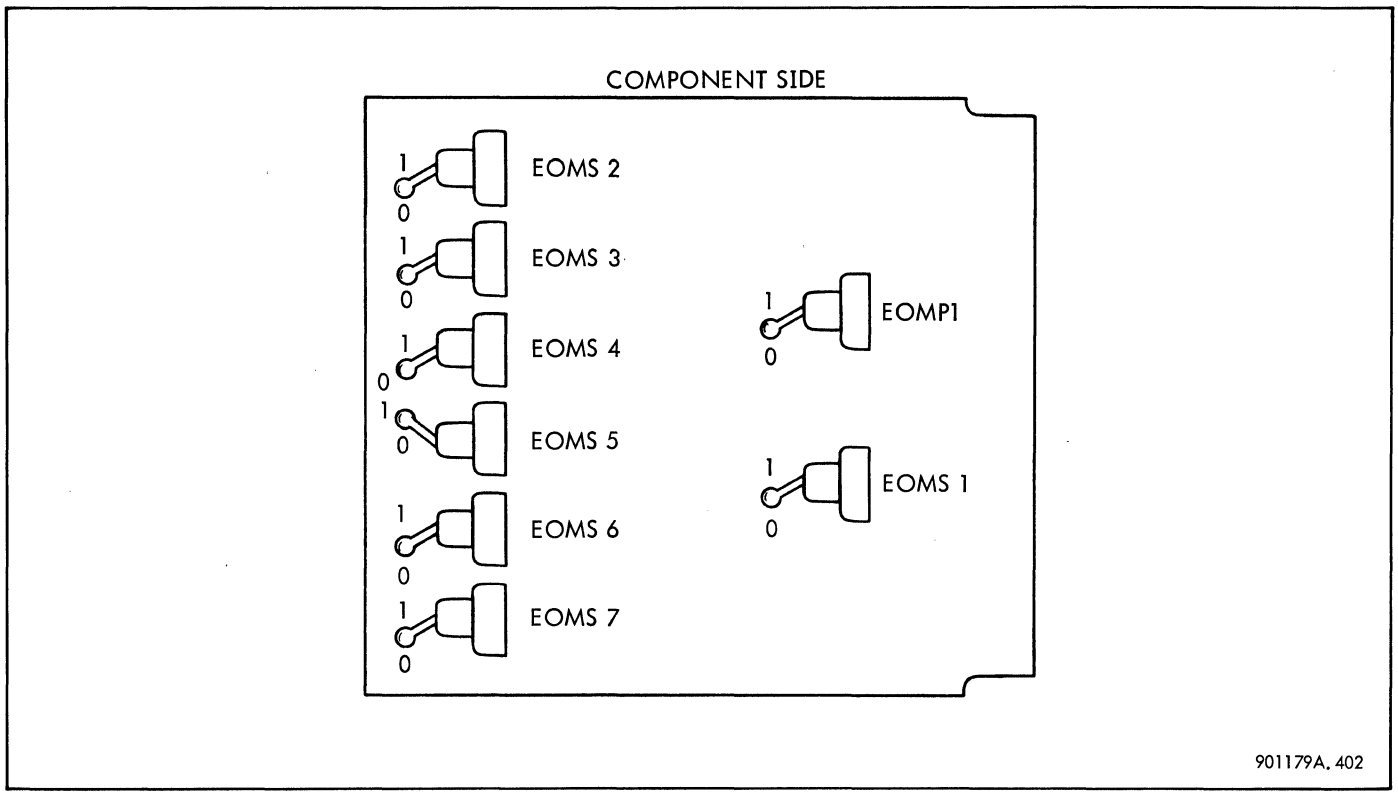

Figure 4-1. Switch Settings, End-of-Message Character

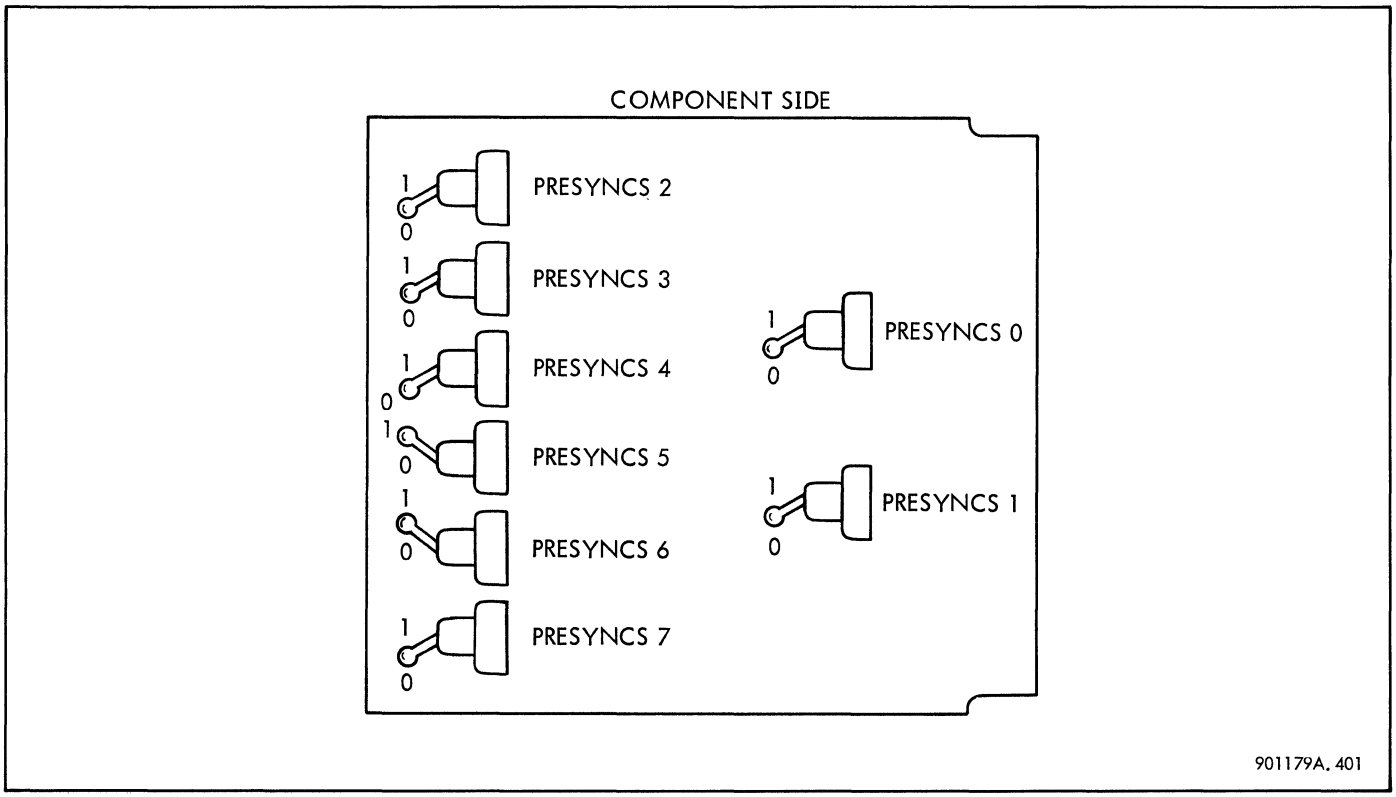

Figure 4-2. Switch Settings, Synchronous Character

The DSC next compares each received data byte with the corresponding data byte transferred. The data transmitted will be a sequential binary count for each data byte transmitted. The DSC must transmit and receive data without detecting an error for a minimum of 15 minutes. If an error is detected during the 15 minutes, the results are these:

1. The COMPARE ERROR indicator lights.

2. The BSY (odd and even channel) and the CLEAR TO SEND indicators go out.

3. Indicator PND remains extinguished and the CAR DET and DSR indicators remain lit.

4. The INPUT BYTE PATTERN indicators indicate the last byte of data received.

5. The OUTPUT BYTE PATTERN test jacks indicate the last data byte transmitted.

Note

By comparing the output of the OUTPUT BYTE PATTERN test jacks and the INPUT BYTE PATTERN indicators, the bit in error can be determined.

m. To ensure that the DSC is comparing data properly, force one of the error conditions described in step l (second enumeration) by changing the setting of the least significant OUTPUT BYTE PATTERN switch (No. 7) from the count (up) position to the 1 (center) position while the DSC is transmitting and receiving data. After an error is detected, the DSC is restarted by pressing the COMPARE ERROR RESET switch (COMPARE ERROR indicator goes out) and then pressing the FS switch.

n. After the DSC has transmitted and received data for 15 minutes without detecting an error, set the STOP/RUN switch to STOP. The results of doing this are these:

1. The BSY (odd and even) and the CLEAR TO SEND indicators go out.

2. The INPUT BYTE PATTERN indicators retain the last data byte received.

3. The UNE, INT, and RATE ERR indicators for the odd and even channels and the PND and COMPARE ERROR indicators remain extinguished.

4. The CAR DET and DSR indicators remain lit.

o. To test the ability of the DSC to terminate receiving data when an end-of-message character is received, proceed as follows:

1. Reestablish the conditions described in steps a through l.

2. Set switch CMP to the down position.

3. Set the OUTPUT BYTE PATTERN switches as follows: switch 5 to the center position; all others to the down (zero) position.

4. After performing substep 3, check for the following indication: BSY indicator for the even channel goes out, BSY indicator for the odd channel CLEAR TO SEND, CAR DET, and DSR indicators remain lit; COMPARE ERROR and PND indicators remain extinguished; INPUT BYTE PATTERN indicators flicker; UNE, INT, and RATE ERR indicators for the odd and even channels remain extinguished.

p. Set the STOP/RUN switch to STOP, and look for the following results:

1. The BSY, UNE, INT, and RATE ERR indicators for the odd and even channels go out.

2. The CLEAR TO SEND, PND, and the COMPARE ERROR indicators go out.

3. The CAR DET and DSR indicators remain lit.

4. The INPUT BYTE PATTERN indicators retain the last byte of data received.

q. To test the ability of the DSC to terminate receiving data one character after the end-of-message character is received, proceed as follows:

1. Set the EOMP 1 shown in figure 4-1 to the 1 (up) position.

2. Reestablish conditions described in steps a through l.

3. Set the CMP switch to the down position.

4. Set the OUTPUT BYTE PATTERN switches as follows: switch 5 to the center position; all other switches to the down (zero) position.

5. After performing step 4, look for the following results:

(a) The BSY indicator for the even channel goes out.

(b) The BSY indicator for the odd channel, the CLEAR TO SEND, CAR DET, and DSR indicators remain lit.

(c) The COMPARE ERROR and PND indicators remain extinquished.

(d) The INPUT BYTE PATTERN indicators continue to flicker.

(e) The UNE, INT, and RATE ERR indicators for the odd and even channels remain extinguished.

r. After completing step q, set the EOMP 1 switch back to the down (zero) position.

4-13 Read/Write Synchronous Test

The read/write synchronous test checks the ability of the DSC to transmit and receive synchronous data sumultaneously. The read/write synchronous test is performed whenever a synchronous modification kit is installed in the DSC. Proceed as follows to run the synchronous read/write test:

a. Set the PET switches as follows:

1. The READ switch to the up position

2. The CMP switch to the down position

3. The ORDER switches to hexadecimal 01

4. The OFF LINE/ON LINE switch to ON LINE

5. The RATE ERROR switch to the up position

6. The RUN/STOP switch to RUN

7. The OUTPUT BYTE PATTERN switches 0 through 4 and switch 7 to the down (zero) position. Switches 5 and 6 to the center (1) position

b. Press the COMPARE ERROR RESET switch to extinguish the COMPARE ERROR indicator (if lit).

c. Initialize the DSC by setting the OFF LINE/ON LINE switch to OFF LINE and back to ON LINE.

d. After performing step c, check for the following results:

1. The UNE, INT, BSY, and RATE ERR indicators for odd and even channels and the PND and CLEAR TO SEND indicators go out.

2. The DSR and CAR DET indicators light.

3. The INPUT BYTE PATTERN indicators are extinguished.

e. Press switch FS. The DSC begins transmitting and receiving data. While data is being transmitted and received, check for the following results:

1. The UNE, INT, and RATE ERR indicators for the odd and even channels and the PND indicator remain extinguished.

2. The BSY indicator for the odd and even channels lights after switch FS is released.

3. The CLEAR TO SEND indicator lights after switch FS is released.

4. The DSR and CAR DET indicators remain lit.

5. The INPUT BYTE PATTERN indicators indicate the setting of the OUTPUT BYTE PATTERN switches.

Note

At this point, the DSC is transferring and receiving synchronizing characters. The DSC must receive at least two synchronizing characters before other data can be received by the DSC.

f. Set the OUTPUT BYTE PATTERN switches to hexadecimal 02. Set the CMP switch to the up position. Make sure that none of the OUTPUT BYTE PATTERN switches is set in the count position.

Note

At this point, the DSC begins comparing each received data byte with the corresponding data byte that was transferred. The PET indicators remain as described in step e.

g. The DSC transmits and receives data for one minute without detecting an error. If an error is detected, the following indications are observed:

1. The COMPARE ERROR indicator lights.

2. The BSY for the odd and even channel and the CLEAR TO SEND indicators go out.

3. The UNE, INT, and RATE ERR indicators for the odd and even channel and the PND indicators remain extinguished.

4. The INPUT BYTE PATTERN indicators go out.

Note

If an error is detected, it is imperative that steps a through f be repeated in order to continue testing.

h. To ensure that the DSC is comparing data properly, force an error condition described in step g by changing the setting of the least significant OUTPUT BYTE PATTERN switch (switch 7) while the CMP switch is in the up position and the DSC is transferring and receiving data. The forced error should cause the conditions described in step g.

i. Test other data transmission patterns as follows:

1. Reestablish conditions described in steps a through f.

2. Set switch CMP to the down position.

3. Set the OUTPUT BYTE PATTERN switches to hexadecimal 01.

4. Set switch CMP to the up position.

5. Transmit and receive data without error for one minute. The PET indicators must be as described in step e.

6. Repeat substeps 2 through 5 and substitute each of the following hexadecimal characters for substep 3: 02, 08, 10, 20, 40, 80, AA, 55, A5, 5A, FF.

The DSC should perform substeps 1-6 without detecting a data transmission error. If an error is detected, the PET indicators will be as described in step g. To continue operation after an error has been detected, conditions described in steps a through g must be reestablished.

j. After steps 1 through 6 have been successfully completed, set the RUN/STOP switch to STOP. The following indications are observed:

1. The BSY indicator for the odd and even channels and the CLEAR TO SEND indicator go out.

2. The UNE, INT and RATE ERR indicator for odd and even channels and the PND indicator remain extinguished.

3. The CAR DET and DSR indicators remain lit.

4. The INPUT BYTE PATTERN indicators go out.

k. Test the ability of the DSC to terminate receiving data when an end of message character is received as follows:

1. Reestablish conditions described in steps a through g.

2. Set switch CMP to the down position.

3. Set the OUTPUT BYTE PATTERN switch to hexadecimal 04. The results should be as follows:

(a) The BSY indicator for the even channel goes out.

(b) The BSY indicator for the odd channel and the CLEAR TO SEND, CAR DET, and DSR indicators remain lit.

(c) The UNE, INT, RATE ERR indicators for the odd and even channels and the PND indicator remain extinguished.

(d) The INPUT BYTE PATTERN indicators indicate the setting of the OUTPUT BYTE PATTERN switches

Note

If at any time during the tests described in paragraph 4-13, steps a through k, the DSC receives an end of message character (hexadecimal 04), the BSY indicator for the even channel will go out. For this reason, the OUTPUT BYTE PATTERN switches should never be set in the hexadecimal 04 configuration except during step k.

l. To test the ability of the DSC to terminate receiving data one character after the end of message character is received, proceed as follows:

1. Set the EOMP1 switch shown in figure 4-1 to the 1 (up) position.

2. Reestablish conditions described in steps a through f.

3. Set the CMP switch to the down position.

4. Set the OUTPUT BYTE PATTERN switches to hexadecimal 04 and look for the following results:

(a) BSY indicator for the even channel goes out.

(b) BSY indicator for the odd channel, and the CLEAR TO SEND, CAR DET, and DSR indicators remain lit.

(c) The UNE, INT, and RATE ERR indicators for the odd and even channels, and the PND indicator remain extinguished.

(d) The INPUT BYTE PATTERN indicators indicate the setting of the OUTPUT BYTE PATTERN switches.

m. After completing step l, set the EOMP1 switch back to the down (zero) position.

n. To test the ability of the DSC to transmit and receive data at the rate of 7 bits per byte through 3 bits per byte, proceed as follows:

1. Perform steps a through h with the exception of the ORDER switch setting described in step a. As each step (a through h) is executed, set the ORDER switches to one of the following hexadecimal numbers: E1, C1, A1, 81, or 61.

2. If the COMPARE ERROR indicators or any of the PET indicators react differently than what is described in steps a through h, the test should be repeated.

o. To test the DSC's ability to detect rate errors, proceed as follows:

1. Reestablish conditions described in steps a through g.

2. Set the RATE ERROR switch to the down position and check for the following results:

(a) The RATE ERR indicator for the odd and even channels and the UNE indicator for the even channel lights.

(b) The UNE indicator for the odd channel, the INT indicator for the odd and even channels, the PND indicator, and the COMPARE ERROR indicator remain extinguished.

(c) The BSY for the odd and even channels and the CLEAR TO SEND, CAR DET, and DSR indicators remain lit.

(d) The INPUT BYTE PATTERN indicators go out.

(e) The COMPARE ERROR indicators remain extinguished.

3. Set the RATE ERROR switch back to the up position and check that the following results occur:

(a) The UNE indicator for the odd and even channels and the COMPARE ERROR indicators light.

(b) The BSY indicator for the odd and even channels and the CLEAR TO SEND indicators go out.

(c) The INT indicator for the odd and even channels and the PND indicators remain extinguished.

(d) The UNE indicator for the even channel, the RATE ERROR indicator for the odd and even channels, and the CAR DET, and DSR indicators remain lit.

4-14 Enable Ring Detect Test

This test checks the ability of the DSC to generate an interrupt when the enable ring detect order is executed. Proceed as follows to run the enable ring detect test:

a. Set up the PET as follows:

1. The READ switch to the down position

2. The ORDER switches to hexadecimal 07

3. The OFF LINE/ON LINE switch to ON LINE

4. The CMP switch to the down position

5. The RATE ERROR switch to the up position

6. The RUN/STOP switch to RUN

b. Initialize the DSC by setting the OFF LINE/ON LINE switch to OFF LINE and then back to ON LINE and check for the following results:

1. The UNE, INT, BSY, and RATE ERR indicators for the odd and even channel go out. The PND and CLEAR TO SEND indicators go out.

2. The DSR and CAR DET indicators light.

3. The INPUT BYTE PATTERN indicators are indeterminate.

c. Press switch FS and check that the following results occur:

1. The UNE, BSY, and RATE ERR indicators for the odd and even channels remain extinguished. The PND and CLEAR TO SEND indicators remain extinguished.

2. The DSR and CAR DET indicators remain lit.

3. The INPUT BYTE PATTERN indicators are indeterminate.

4. The INT indicator for the odd channel goes out and the INT indicator for the even channel lights.

4-15 Disconnect Test

The disconnect test is performed on a DSC installed with an asynchronous or synchronous 200 modification kit. The disconnect test is performed as follows:

a. Set the PET up as follows:

1. Set the READ and CMP switches to the down position.

2. Set the ORDER switches to hexadecimal OB.

3. Set the OFF LINE/ON LINE switch to ON LINE.

4. Set the RATE ERROR switch to the up position.

5. Set the RUN/STOP switch to RUN.

b. Initialize the DSC by setting the OFF LINE/ON LINE switch to OFF LINE and then back to ON LINE. Check that the following results occur:

1. The UNE, INT, BSY, and RATE ERR indicators for the odd and even channel go out. The PND and CLEAR TO SEND indicators also go out.

2. The DSR and CAR DET indicators light.

3. The INPUT BYTE PATTERN indicators are indeterminate.

c. Press switch FS and check that the following results occur:

1. None of the PET indicators change from the conditions described in step b.

2. The DISCON signal on pin 4 of module 29A latches to the true condition.

d. Set the OFF LINE/ON LINE switch to OFF LINE and then back to ON LINE. The results of this switching should be these:

1. None of the PET indicators change from the conditions described in step b.

2. The DISCON signal on pin 4 of module 29A resets to the false condition.

4-16 Generate Long Space Test

When an asynchronous modification kit is installed in the DSC, the generate long space test should be performed to test the ability of the DSC to properly transmit and receive a long space character. Perform the test as follows:

a. Set the PET up as follows:

1. The READ switch to the up position

2. The CMP switch to the down position

3. The OFF LINE/ON LINE switch to ON LINE

4. The RATE ERROR switch to the up position

5. The RUN/STOP switch to RUN

6. The OUTPUT BYTE PATTERN switches to the center (1) position

b. Initialize the DSC by setting the OFF LINE/ON LINE switch to OFF LINE and then back to ON LINE. Check for the following results:

1. The UNE, INT, BSY, and RATE ERR indicators for the odd and even channels go out. The PND and CLEAR TO SEND indicators go out.

2. The CAR DET and DSR indicators light.

3. The INPUT BYTE PATTERN indicators are indeterminate.

c. Press switch FS. The results of doing this should be these:

1. The UNE, INT, and RATE ERR indicators for the odd and even channels and the PND indicator remain extinguished.

2. The BSY indicator for the odd and even channels and the CLEAR TO SEND indicator light.

3. The DSR and CAR DET indicators remain lit.

4. The INPUT BYTE PATTERN indicators for unused bits light; all other INPUT BYTE PATTERN indicators go out.

d. Set the RUN/STOP switch to STOP. The results of doing this are these:

1. The BSY indicator for the odd channel and the CLEAR TO SEND indicator go out.

2. The BSY indicator for the even channel and the CAR DET and DSR indicators remain lit.

3. The UNE, INT, and RATE ERR indicators for the odd and even channel remain extinguished. The PND and the INPUT BYTE PATTERN indicators that are used also remain extinguished.

e. Momentarily ground signal NDSNR on pin 25 of module 2B. The results of doing this should be as follows:

1. The BSY indicator for the even channel goes out.

2. The UNE indicator for the even channel lights.

3. The BSY and UNE indicators for the odd channel, the INT and RATE ERR indicators for the odd and even channels, and the PND, CLEAR TO SEND, and INPUT BYTE PATTERN indicators that are used remain extinguished.

4. The CAR DET indicator remains lit.

5. The DSR indicator momentarily goes out while signal NDSNR is grounded.

4-17 Dial Option Test

When the dial option modification kit is installed in the DSC, the dial option test is performed to test the ability of the DSC to communicate with an ACU. Perform the test as follows:

a. Remove module NT29 (position 4B) and ground pins 30 (DLOS), 34 (NDIALAVL), and 36 (NDSSD), located on module 4B.

b. Set up the PET as follows:

1. The READ and CMP switches to the down position

2. The OFF LINE/ON LINE switch to ON LINE

3. The RATE ERROR switch to the up position

4. The RUN/STOP switch to RUN

5. The ORDER switches to hexadecimal 05

c. Initialize the DSC by setting the OFF LINE/ON LINE switch to OFF LINE and then back to ON LINE. The results are these:

1. The UNE, INT, BSY, and RATE ERR indicators for the odd and even channels go out. The PND and the CLEAR TO SEND indicators also go out.

2. The CAR DET and DSR indicators light.

3. The INPUT BYTE PATTERN indicators are indeterminate.

d. Press switch FS. The results should be these:

1. The BSY indicator for the odd channel and the CLEAR TO SEND indicator light.

2. The UNE, INT, and RATE ERR indicators for the odd and even channels and the BSY indicator for the even channel remain extinguished.

3. CAR DET and DSR indicators stay lit.

4. The call request signal (FCRQ) located on pin 37 of module 23A is true.

e. Repeatedly press switch PND; the results are these:

1. When switch PND is pressed, the PND indicator lights and the digit present signal (FDPR) located on pin 21 of 5B is true.

2. Each time switch PND is pressed, the contents of the four least significant OUTPUT BYTE PATTERN switches are stored in the bit register (bit 1 - bit 4). Using the OUTPUT BYTE PATTERN switches and table 4-4, verify that a binary zero (false) and a binary one (true) condition can be stored in each bit of the register.

f. After performing step e, set the RUN/STOP switch to STOP. Press switch PND twice in succession. After pressing and releasing the PND switch a second time, check that the following results occur:

1. The BSY indicator for the odd channel and the CLEAR TO SEND indicator go out.

2. The UNE, INT, and RATE ERR indicators for the odd and even channels, the BSY indicator for the even channel, and the PND indicator remain extinguished.

3. The CAR DET and DSR indicators remain lit.

g. Force an unusual end during a dial cycle as follows:

1. Reestablish steps a through d.

2. Momemtarily ground signal NABORT on pin 14 of module 4B. The results of doing this should be these:

(a) The BSY indicator for the odd channel and the CLEAR TO SEND indicator go out.

(b) The UNE indicator for the odd channel lights.

(c) The UNE and BSY indicators for the even channel, the INT and RATE ERR indicators for the odd and even channels, and the PND indicator remain extinguished.

(d) The CAR DET and DSR indicators remain lit.

h. Attempt to perform the following dial option test when the dialer portion of the DSC is nonoperational:

1. Ground the NABORT signal on pin 14 of module 4B.

2. Reestablish steps a through d.

Table 4-4. Storage Bit Register

OUTPUT BYTE PATTERN Switch	Bit Register Signal Name	Pin Number	Module
4	BIT4	38	5B
5	BIT3	7	5B
6	BIT2	23	5B
7	BIT1	37	5B

i. Press switch FS. The results of doing this are:

1. The INT, BSY, and RATE ERR indicators for the odd and even channels, the UNE indicator for the even channel, and the CLEAR TO SEND indicator remain extinguished.

2. The DSR and CAR DET indicators remain lit.

3. The UNE indicator for the odd channel lights.

j. Remove the ground applied to signal NABORT in step h.

k. Adjust the timing delay circuit for the data set status signal (NDSSD) as follows:

1. Remove ground jumpers installed in step a and install module NT29 back into module position 4B.

2. Add two Masterite connectors to module NT29.

3. Apply a +8V through a 330 ohm resistor to pin 13 of the Masterite connector placed on the component side of module NT29.

4. Adjust the potentiometer on module NT29 so that signal NDSSD will go to ground potential five seconds after the positive voltage described in step 3 is applied to pin 13.

Note

Signal NDSSD can be located on pin 36 of module 4B.

4-18 Automatic Disconnect Timing Adjustment

Make the adjustment as follows:

a. Ground the HANGUP-S signal on pin 41 of module 7B.

b. Adjust the potentiometer on the OT15 module (7B) to allow the maximum amount of time between the time the ground is applied to pin 41 of module 7B and the time signal HANGUP-S (pin 40 of 7B) goes to ground potential. This time duration must be between 20 and 30 seconds.

Note

The ground on the timing input signal (HANGUP-S) must be maintained during the entire 20 to 30 seconds interval of time.

4-19 Voltage Margins

Vary the DSC voltages (+8V, -8V, +4V) individually ±10% during the tests described in paragraph 4-12, substeps a through m and paragraph 4-13, substeps a through h. The DSC must operate without error for a period of 10 minutes on each voltage margin. If an error occurs, repeat test. An error consists of any PET indicator reacting in a manner different than those described in the test procedures.

4-20 PARTS LIST

4-21 PARTS LIST TABLE AND MODULE LOCATION CHART

Parts that require replacing due to wear or damage are shown in the parts list table (table 4-5). Standard hardware such as nuts, screws, clamps, and washers, is not listed.

(Modules are considered replaceable parts; they are listed in the table but are not broken down. Module location is shown in figure 4-3. For a complete breakdown of each module, refer to the applicable module data sheet drawing number given in table 4-5.)

4-22 Arrangement of Parts List Table

The parts list table is arranged in six columns as follows:

a. Figure and index number

b. Description

c. Reference designator

d. Manufacturer

e. Part number

f. Quantity

4-23 MANUFACTURERS CODE INDEX

Table 4-6 lists by code number the names and addresses of the manufacturers who supply the parts given in table 4-5.

Table 4-5. Data Set Controller Models 7601, 7602, and 7603, Replaceable Parts

Fig. & Index No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-3	Data Set Controller Models 7601, 7602, and 7603		XEROX	139834	1
-1	Timing Generator	1A		133920	1
-2	Send Module LT49	3A		133908	1
-3	Receive Module LT53	6A		133912	1
-4	Interface Module NT30	7A		146102	1
-5	Interface Module AT43	8A		145717	1
-6	Gated Flip-Flop FT12	9A, 17B		117028	2
-7	Universal Flip-Flop FT22	10A		124713	1
-8	Basic Flip-Flop FT30	11A, 18A		129933	2
-9	Switch Comparator Module LT26	12A, 6B, 24B		126982	3
-10	Plug Connector P183 (PET)	13A		126567	1
-11	Plug Connector P181 (PET)	14A		126566	1
-12	Buffered Matrix Module BT13	15A		116407	1
-13	NAND Gate Module IT11	16A, 17A, 30A, 10B		116994	4
-14	Band Gate Module BT11	19A, 25A, 26A, 27A, 19B, 20B		116029	6
-15	NAND Gate Module IT18	20A, 22A, 24A		126372	3
-16	Basic Flip-Flop Module FT10	21A, 2B, 5B, 13B, 21B, 23A		116380	6
-17	Buffered Latch No. 2 Module FT27	28A, 31A, 11B		126986	3
-18	Buffered AND/OR Gate Module BT10	29A, 12B, 15B		116056	3
-19	Gated Buffer Module BT17	32A, 18B		126330	2
-20	Inverted Matrix Module IT13	3B, 14B, 16B		117000	3
-21	ACU Interface Module NT29	4B		145402	1
-22	One-Shot 10 Sec Module OT15	7B		130689	1
-23	Synchronous Send/Receive Module LT83	8B, 9B		146272	2
-24	Logic Element Module LT25	23B		126712	1
-25	Driver-Receiver Module AT17	26B		126714	1
-26	Logic Element Module LT24	27B		126710	1
-27	Receiver Module AT10	28B		123018	1
-28	Logic Element Module LT41	29B		133392	1
-29	Driver-Receiver Module AT11	30B		123019	1
-30	Logic Element Module LT43	31B		133657	1
-31	Driver Module AT12	32B	XEROX	124665	1

Table 4-6. Manufacturers Code Index

Code No.	Name	Address
398	Simpson Electric Co.	5200 W. Kinzie St., Chicago, Illinois 60644
399	Tektronic, Inc.	P. O. Box 500, Beaverton, Oregon 97005

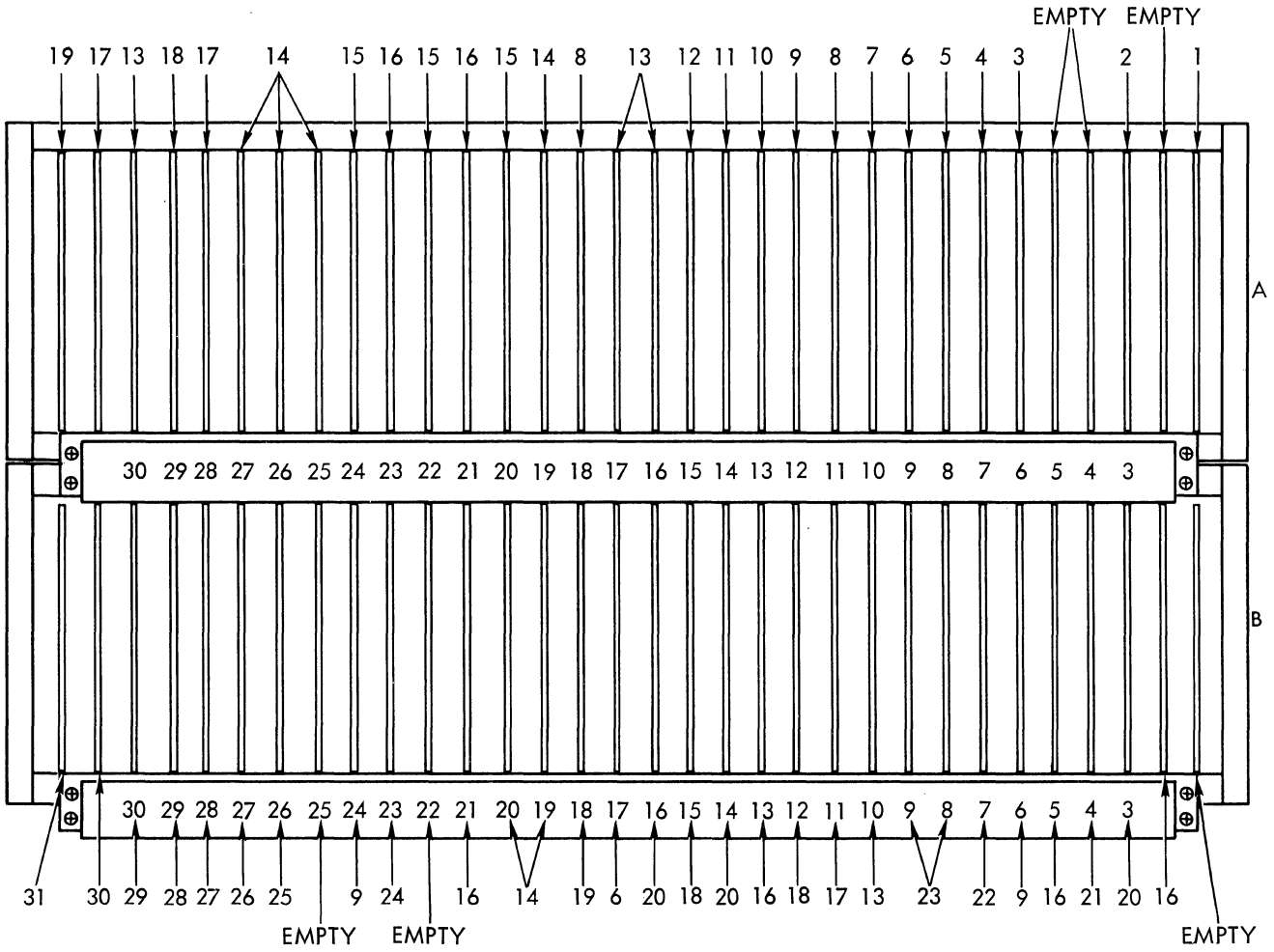

Figure 4-3. Data Set Controller Module Location Chart

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