THE IMPACT OF DSP ON

FUTURE GENERATION HDDS

A SHORT COURSE

DEC. 1991

INSTITUTE FOR INFORMATION STORAGE
TECHNOLOGY

DIGITAL SIGNAL PROCESSING IN DISC DRIVES

INTRODUCTION/OVERVIEW

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December 1991

DSP AND DISC DRIVE SUBSYSTEMS

- DIGITAL DATA STORAGE <u>IS</u> DSP

  => DIGITAL IN, DIGITAL OUT

- DRIVE EXTERNAL/INTERNAL INTERFACES ARE DIGITAL

  CONTROLLED BY DRIVE μPROCESSOR

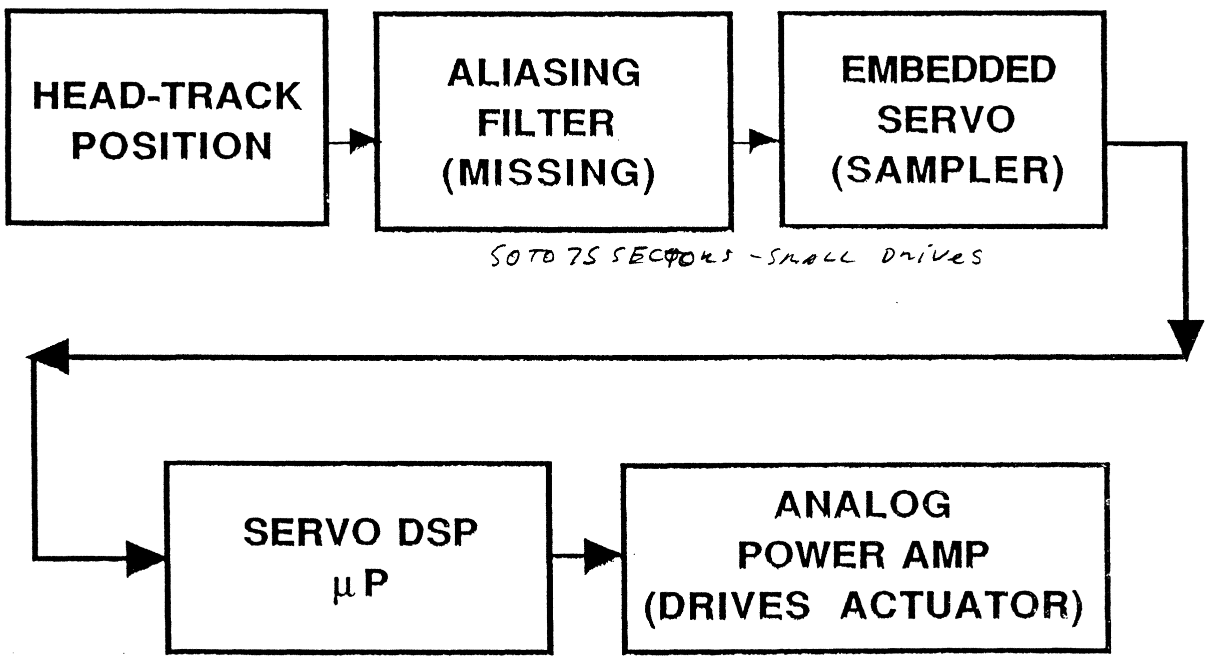
- EXCEPT THREE CLASSICALLY ANALOG INTERNAL SERVO SYSTEMS

  => HEAD SERVO: TRACK SEEK AND POSITION HOLD

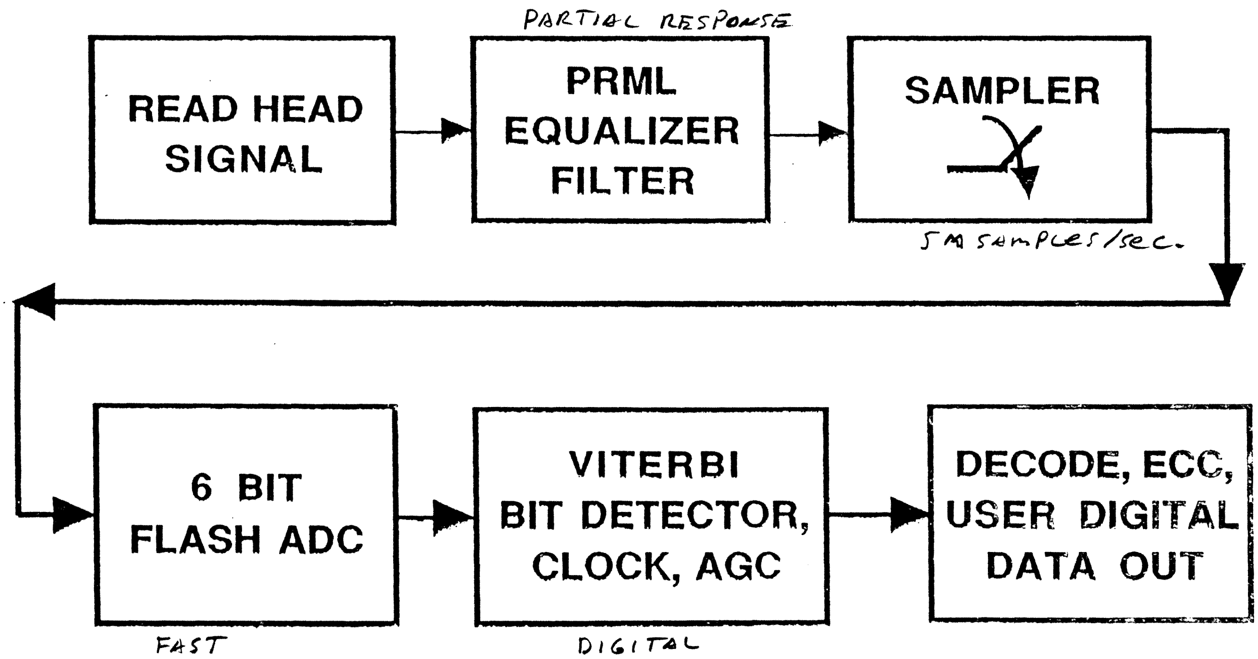
  => RECORDING (READ-WRITE) CHANNEL

  => DISC SPINDLE MOTOR SPEED SERVO

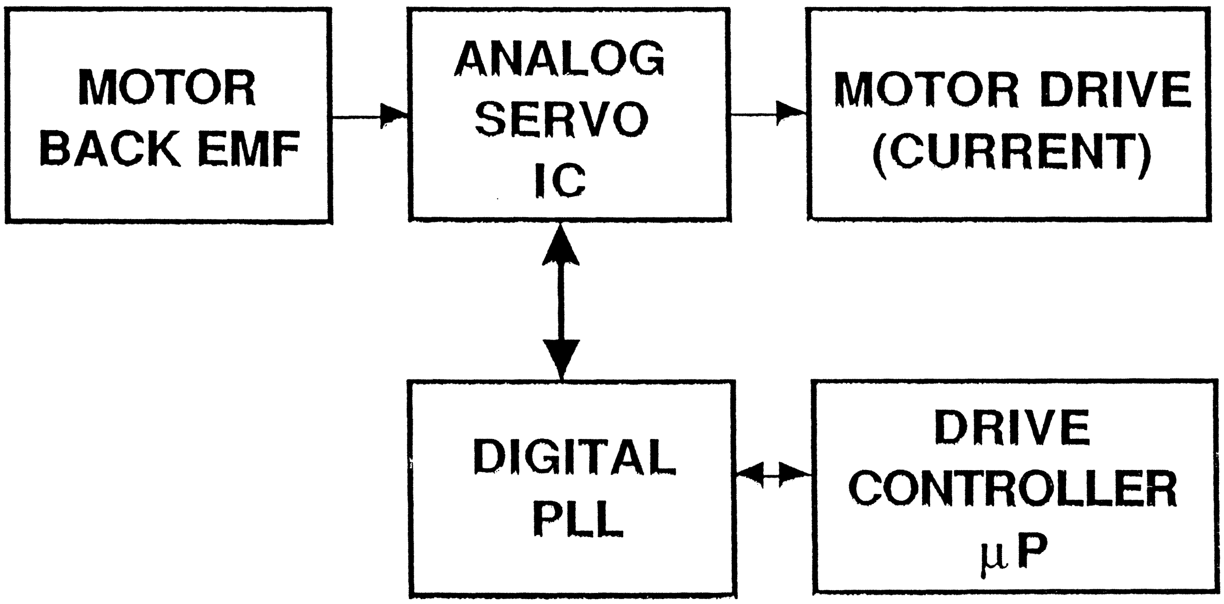
DSP HEAD TRACKING SERVO



DSP READ CHANNEL



SPINDLE SPEED SERVO



POTENTIAL DSP ADVANTAGES

- BETTER DRIVE PERFORMANCE SPECS,

  FROM TIGHTER WORST-CASE TOLERANCES TO COMPONENTS, TIME, AND TEMPERATURE.

- OR LESS STRINGENT COMPONENT TOLERANCES.

- MORE DRIVE I/O'S PER SECOND,

  FROM OFFLOADING SERVO CONTROL FUNCTIONS FROM DRIVE'S μPROCESSOR

- ADAPTIVE CONTROL ALGORITHMS,

  UTILIZING PERFORMANCE DATA,
  OVERLAPPED WITH DATA ACCESSING
  (NO OVERHEAD PENALTY)

DSP ADVANTAGES (con't)

- MANUFACTURABILITY:

  SELF CALIBRATION

  SELF TEST/DIAGNOSIS

  SELF TUNING FOR YIELD ENHANCEMENT

- DRIVE ERROR RECOVERY

  FROM OPERATING SHOCK,

  MIS-TRACKING,

  MIS-READ

- LOWER SERVO POWER CONSUMPTION,
  FROM OPTIMAL PLANT CONTROL MODELS

READ/WRITE CHANNELS

• EXAMPLE: IBM'S DSP PRML CHANNELS
MAXIMUM LIKELYHOOD

• CONVENTIONAL CHANNEL DIGITALELEMENTS

USER DIGITAL DATA INPUT

COMPUTE AND APPEND ERROR CORRECTION CODE

ENCODE (END~~A~~EC)

(ANALOG WRITE-READ CHANNEL)

DECODE (END~~A~~EC)

DETECT AND CORRECT BURST ERRORS

USER DIGITAL DATA OUTPUT

READ/WRITE CHANNELS (con't)

CONVENTIONAL R/W CHANNEL ANALOG ELEMENTS

- WRITE DRIVER
    - WRITE CURRENT
    - WRITE PRECOMPENSATION
- MAGNETIC RECORDING WRITE/READ PROCESS
- READ PREAMP
- READ EQUALIZATION AND NOISE FILTER
    - AGC CONTROL AND SETTING
    - BIT QUALIFIER (THRESHOLD LEVEL(S))
    - BIT TRANSITION DETECTOR
    - TIMING RECOVERY (PHASE LOCK LOOP)
    - DATA SEPARATION (TIMING SYNC)

R/W CHANNEL
DSP POTENTIAL ADVANTAGES:

- CONVENTIONAL PEAK DETECTION CHANNELS
  FACE INABILITY TO GET NECESSARY 26 dB SNR,
  100 MBITS/SQ"
  AT HIGH MBITS/IN^2 AREAL DENSITIES
  .5 nV/HZ NOISE LEVEL INHERENT IN R/W IC'S.

- ...ESPECIALLY 65 mm AND SMALLER DRIVES

- TELEPHONE
  COMMUNICATIONS CHANNELS OPERATE AT 15-20 dB,
  USING HEAVY ERROR CORRECTION (10^{-4} RAW BER)

- IBM'S SOLUTION IS DSP PRML,
  (PARTIAL RESPONSE MAXIMUM LIKELIHOOD)

- PARTIAL RESPONSE EQUALIZATION
  ALLOWS BITS TO BE PACKED CLOSER TOGETHER,
  BY ALLOWING CONTROLLED INTERFERENCE.

- A PENALTY IS THAT EQUALIZATION MUST BE PRECISE

=> USE DSP DIGITAL FILTER EQUALIZER

NEED 3% ACCURACY – TUNABLE TO COMPENSATE FOR HEAD/MEDIA'S VARIATIONS.

R/W CHANNEL DSP ADVANTAGES (con't)

- A SAMPLED VITERBI BIT DETECTOR IS OPTIMAL

=> A DIGITAL SIGNAL PROCESSING METHOD

PEAK LOCATION NOT COHERENT

- CLOCKING AND AGC CAN ALSO BE DONE IN THE DSP

....(PR'S HIGH BIT DENSITY DESTROYS THE PEAKS USED FOR CONVENTIONAL CLOCKING)

- DSP READ CHANNEL RESULTS IN:

  HIGHER BPI, BY USING PARTIAL RESPONSE.

  HIGHER TPI, SINCE VITERBI ALLOWS LOWER PLAYBACK AMPLITUDES (NARROW TRACKS)

- => HIGHER AREAL DENSITY (MBITS/IN^2)

  IBM IS SAYING 15-30% FOR FIRST GENERATION

  EVEN MORE LATER   150 M BITS / SQ" DENSITY

HEAD/TRACK SERVOS

- SERVO INPUT: HEAD-TRACK POSITION:
  INTEGER TRACK NUMBER (GRAY CODE),
  PLUS FRACTIONAL TRACK ERROR

- SERVO OUTPUTS:
  ACCELERATION COMMAND (ACTUATOR CURRENT),
  SEEK COMPLETE, SEEK ERROR, HEAD OFF TRACK
  IMBEDDED SERVO WEAK – NO TRACK WHILE WRITING.

- CONTINUOUS SERVO SIGNAL IN LARGER DRIVES

- SAMPLED SERVO COMMON IN SMALL DRIVES (3-5 KHZ)

- NOTE: SERVO SYSTEM SAMPLING OCCURS BEFORE ANY
  ANTI-ALIASING FILTER POSSIBLE.
  THIS CAN ALIAS HEAD FLEXURE 3-7 KHZ RESONANCE
  INTO SERVO PASSBAND.
  HEAD/GIMBEL RESONANCE
  USE NOTCH FILTER + TIGHTLY
  CONTROLED RESONANCE SPEC. OF HEAD
  ASSY.
  MEANS RESONANCE MUST BE HELD WITHIN LIMITS,
  MINIMUM RESONANCE SPEC NO LONGER ENOUGH.

PLANT MODEL ("OBSERVER")

- A POWERFUL CONCEPT FOR DSP

- CAN EFFECTIVELY ALLOW SAMPLED SERVO TO
  APPROACH SEEK/SETTLE PERFORMANCE
  OF A CONTINUOUS SERVO,
  WITHOUT THE WASTED DISC SURFACE OVERHEAD,
  AND MECH/THERMAL MISREGISTRY PENALTY.

- CAN REDUCE OFFTRACK DATA RISK
  CAUSED BY MECHANICAL SHOCK/VIBRATION

  (VALIDATE SERVO PES SAMPLES
  AGAINST OBSERVER PREDICTION)

DSP PLANT MODEL (con't)

- CONVENTIONAL LINEAR FREQUENCY DOMAIN ANALYSIS MODELS SECOND ORDER PLANT MECHANICAL SYSTEM, INCLUDING CRITICAL ARM-HEAD RESONANCES

- STATE VARIABLES ARE HEAD POSITION AND VELOCITY

- DSP TIME DOMAIN OBSERVER

  PREDICTS PRESENT STATE.

  MINIMIZES SERVO LAGS,

  ALLOWS NONLINEAR ELEMENTS.

  EXAMPLES:

    ACTUATOR FORCE CONSTANT V.S. POSITION

    HEAD-ARM SETTLING TIME VARIATIONS

DSP PLANT MODEL (con't)

- SERVO ERROR MODELS ALLOW SELF CAL/ADAPTATION:
  1) ACTUATOR FORCE CONSTANT,
     OVER TIME, TEMPERATURE, TRACK (NONLINEAR)
     DRIVE CURRENT SATURATION (NONLINEAR)
  2) ACTUATOR BIAS FORCE OVER TRACK POSITION
     (FROM HEAD FLAT CABLE, WINDAGE) (LINEAR)
  3) INDIVIDUAL HEAD THERMAL OFFSETS (LINEAR)

- REPETITIVE RUNOUT ELIMINATION POSSIBLE
  LINEAR FEEDFORWARD CONTROL,
  BY RUNOUT-LEARNING DSP FILTER

- ADAPTIVE SEEK ALGORITHM:
  MONITOR SEEK SETTLING TIME DURING DATA ACCESS
  TO MINIMIZE TOTAL SEEK TIME AND OFFTRACK

DISC SPINDLE SERVO

- **CONTROLS DISC SPIN MOTOR:**

  3-Ø BRUSHLESS PERMANENT MAGNET MOTOR,

  HAS NO FEEDBACK SENSORS (SPACE LIMITATION IN SMALL DRIVES
  LIMITED TO 3600 RPM BY LIMITED MOTOR
  TORQUE + 5V ONLY REQUIREMENT.

  (NO HALL SENSORS)

- **EXAMPLE DRIVE SPINDLE SERVO:**

  RPM IS PERFECTLY FREQUENCY LOCKED,

  USING DISC POSITION PHASE LOCK LOOP.

  POSITION NOISE SIGMA ≈ 50 NSEC — ~ NO GAP AT END OF ROTATION.

DISC SPINDLE SERVO (con't)

<u>CONVENTIONAL DIGITAL SERVO ELEMENTS</u>:

- A DIGITAL PHASE LOCK LOOP

- USES WRITE CLOCK CRYSTAL AS POSITION REFERENCE

- USES INPUT FEEDBACK SIGNAL FROM MOTOR BACK EMF
  MEASURED OFF THE TWO UNDRIVEN PHASES:
  THE TIMES WHEN THE PHASE VOLTAGES ARE EQUAL.
  => AN APERIODIC DIGITAL SAMPLED SIGNAL,

- GENERATES ANALOG COMMAND VOLTAGE
  TO COMMAND MOTOR ACCELERATION PUMP UP/DOWN

DISC SPINDLE SERVO (con't)

CONVENTIONAL ANALOG SERVO ELEMENTS

- START AND COMMUTATION LOGIC
- ANALOG FEEDBACK STABILIZATION LOOP
- INPUT IS DIGITAL PLL ACCELERATION COMMAND.
- OUTPUT IS SPINDLE MOTOR COIL CURRENT,
  FROM 3-Ø ANALOG POWER DRIVERS.
- INTERFACE TO DRIVE µP MINIMAL.
  POSITION PHASE ERROR CAN BE INTERROGATED.
  SPINDLE EXTERNAL SYNC SIGNAL (OPTIONAL)
- IS THIS AN ERSATZ DSP?
  ...ITS SAMPLED, PARTLY DIGITAL
  ...BUT SAMPLING TIMES ARE APERIODIC,

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Discrete-time and Digital Signal Processing

David G. Messerschmitt

Discrete-time and digital signal processing are increasingly prevalent, due to many factors. Increasingly, analog signal processing is employed only at the very highest speeds where digital solutions are not available.

Objectives:

- **What are the differences and similarities between discrete-time and continuous-time? How do we convert between the two?**
- **What are the differences and similarities between digital and analog?**
- **What are the advantages and disadvantages of digital and discrete-time?**

Typical Configuration

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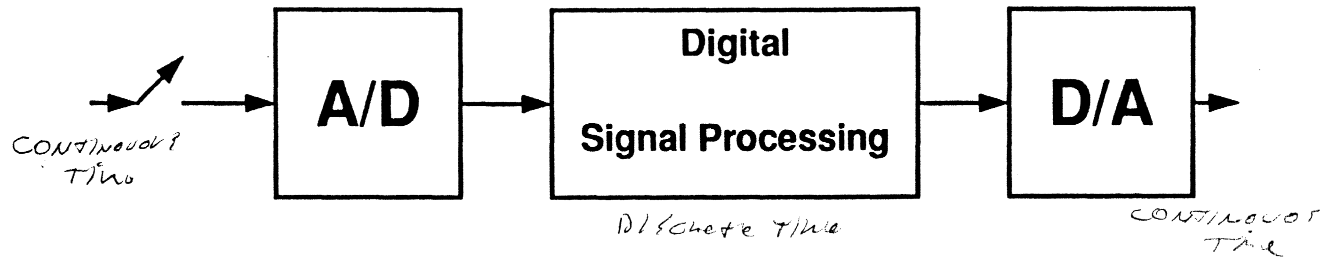

Oversimplified!

Basic elements:

- **Sampler to convert continuous-time to discrete-time**
- **Analog-to-digital converter to convert from analog to digital**
- **Signal processing implemented in the digital and discrete-time domain**
- **Digital-to-analog converter to convert from digital to analog**

Also required are anti-aliasing and reconstruction low-pass filters

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Comparison of Continuous- and Discrete-Time Signals

Different time variables: $x(t)$ **and** $x[n]$

Both can be periodic:

- $x(t+T) = x(t)$

  Time

- $x[n+N] = x[n]$

  samples

Sinusoids exist (and are very important):

- $x(t) = \cos(\omega_0 t)$
- $x[n] = \cos(\lambda_0 n)$

Continuous-time (but not discrete-time) sinusoids are always periodic:

- $\cos\left(\omega_0 \cdot \left(t + \frac{2\pi}{\omega_0}\right)\right) = \cos(\omega_0 \cdot t)$
- $\cos(\lambda_0 \cdot (n+N)) = \cos(\lambda_0 \cdot n)$ for $\lambda_0 = \frac{2\pi}{N} \cdot k$

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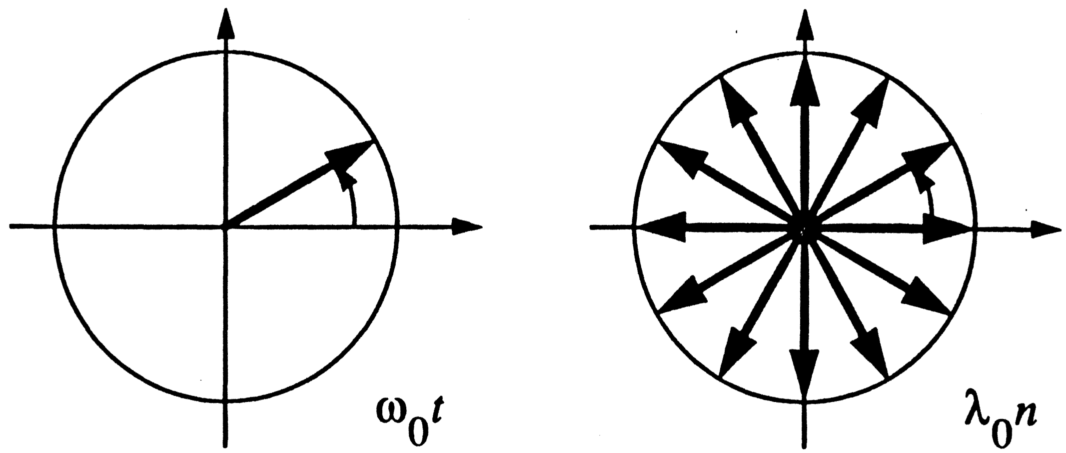
Why Discrete-Time Sinusoids are Not Always Periodic

Represent sinusoid as real part of complex exponential $e^{j\omega_0 t}$ or $e^{j\lambda_0 n}$:



Discrete-time vector moves in discrete steps, only retraces the same points for specific values of λ_0

Discrete-Time Sinusoids Are Periodic in Frequency

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When we increase the frequency by 2π, a discrete-time sinusoid does not change:

- $\cos((\lambda_0 + 2\pi) \cdot n) = \cos(\lambda_0 \cdot n)$

The interesting range of frequencies is an interval of length 2π

- $\lambda_0 \in [-\pi, \pi]$

This is a form of frequency aliasing

For example, frequency $\lambda_0 = 2\pi$ results in the same samples as frequency $\lambda_0 = 0$ (d.c.)

Some Examples of Frequency Aliasing

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$$\cos(\omega_0 t) \xrightarrow{\;n \cdot T\;} \cos(\lambda_0 \cdot n)$$

$$\lambda_0 = \omega_0 \cdot T$$

Increasing λ_0 by 2π (ω_0 by $\frac{2\pi}{T}$) results in the same samples!

Sampling is not reversible: many input continuous-time signals can result in the very same samples!

Normal response is to limit input frequencies to half the sampling rate: $|\omega_0| < \frac{\pi}{T}$

Some Examples of Frequency Aliasing

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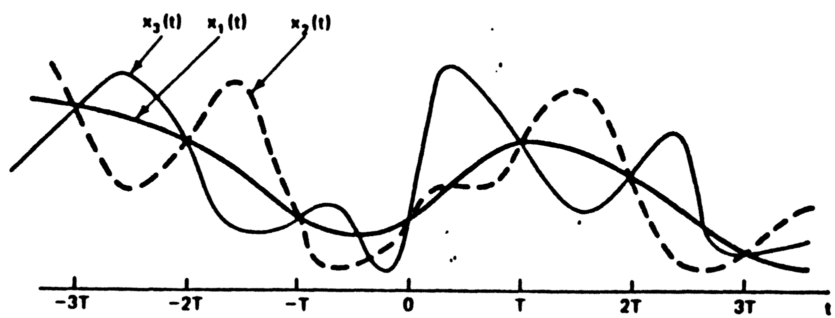
Several continuous-time waveforms have the same samples:

$x_1(kT) = x_2(kT) = x_3(kT)$



However, there is only one waveform bandlimited to $\frac{\pi}{T}$ with that set of samples (the others all have higher frequency components)

LIMIT TO BW = 1/2 SAMPLE RATE.

NYQUIST RATE = 1/2 SAMPLE RATE.

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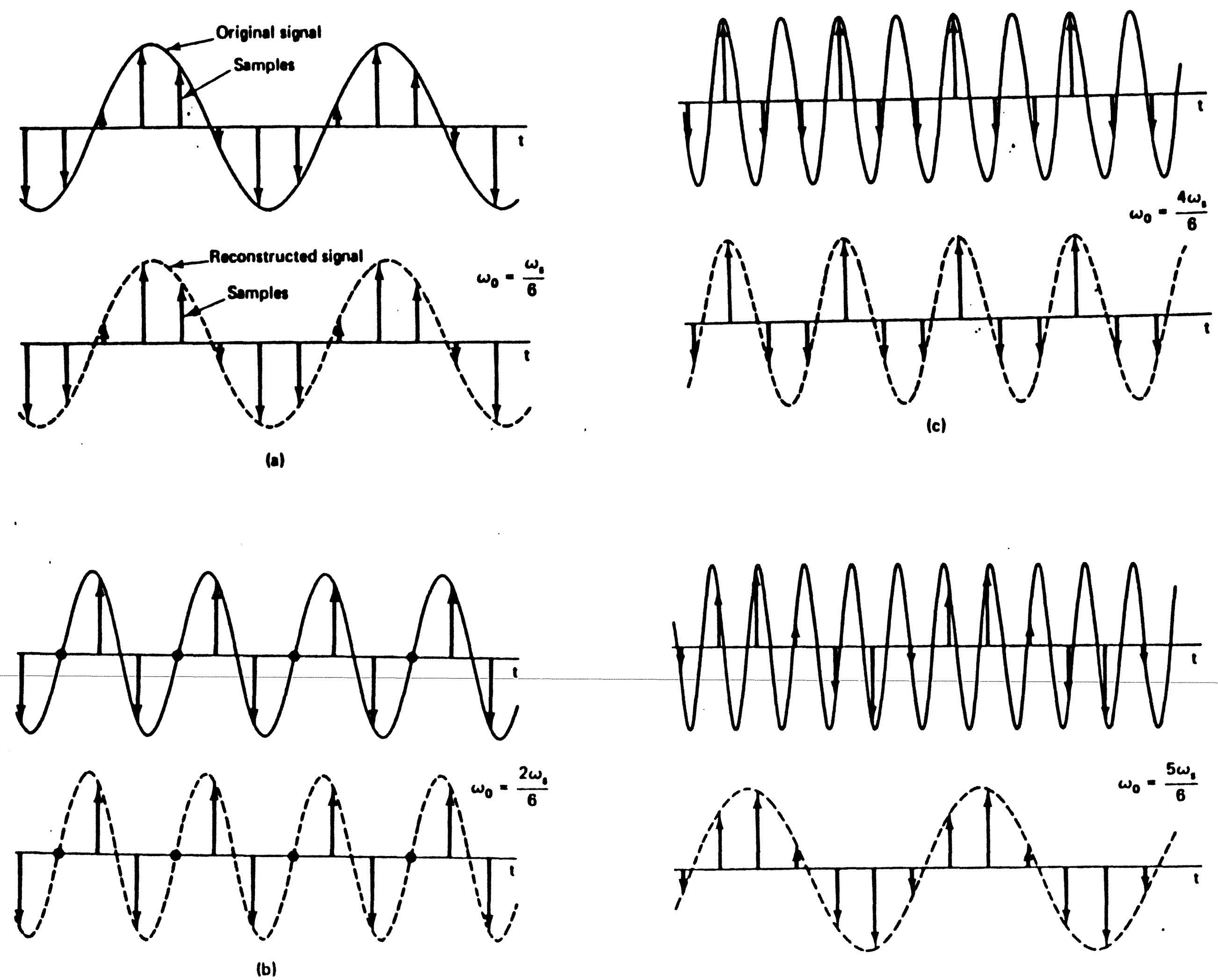
Some Examples of Frequency Aliasing

Need 3 samples / period for correct decode



Digital Filters (LTI Systems)

LINEAR TIME INVARIENT

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$$e^{j\omega t} \longrightarrow \boxed{\begin{array}{c} h(t) \\ H(j\omega) \end{array}} \longrightarrow H(j\omega) \cdot e^{j\omega t}$$

$$e^{j\lambda n} \longrightarrow \boxed{\begin{array}{c} h[n] \\ H(e^{j\lambda}) \end{array}} \longrightarrow H(e^{j\lambda}) \cdot e^{j\lambda n}$$

These functions $H(j\omega)$ and $H(e^{j\lambda})$ are known as the frequency response, $h(t)$ and $h[n]$ are the impulse responses

Input complex exponentials of a given frequency result in output complex exponential at the same frequency

Equivalent effect on sinusoids is an amplitude and phase shift

$H(e^{j\lambda})$ is periodic in 2π: Only range $|\lambda| < \pi$ is of interest

Two Types of Implementable Digital Filters

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Finite impulse response (FIR):

- $y[n] = \sum_{k=0}^{M} b_k \cdot x[n-k]$

- $H(e^{j\lambda}) = \sum_{k=0}^{M} b_k \cdot e^{-j\lambda k}$

Infinite impulse response (IIR):

- $y[n] = \sum_{k=0}^{M} b_k \cdot x[n-k] - \sum_{k=1}^{N} a_k \cdot y[n-k]$

- $H(e^{j\lambda}) = \dfrac{\sum_{k=0}^{M} b_k \cdot e^{-j\lambda k}}{\sum_{k=0}^{N} a_k \cdot e^{-j\lambda k}}$

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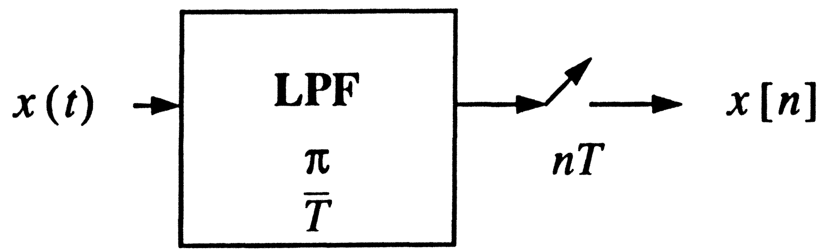
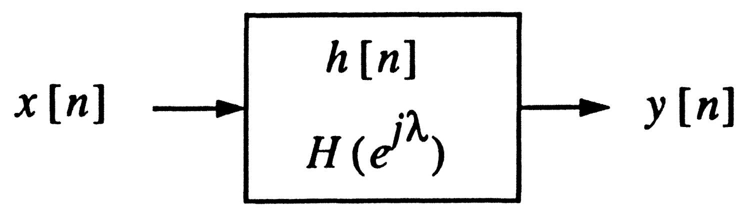
Continuous-Time Filter Implemented in Discrete Time

Sample, preceded by anti-alias lowpass filter:



Discrete-time filter:



Continuous-Time Filter Implemented in Discrete Time (Con't)

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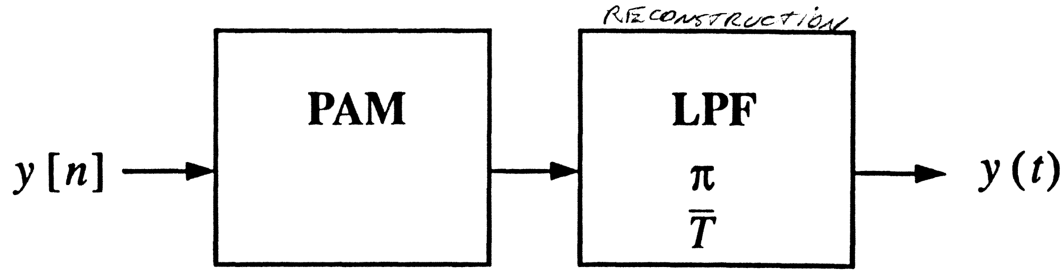
Reconstruct continuous-time signal:



APERTURE "DROOP" CAN BE COMPENSATED WITH GAIN BOOST NEAR NYQUIST RATE.

Pulse-amplitude generator produces sequence of pulses amplitude-modulated by $y[n]$

Lowpass filter reconstructs continuous-time signal by interpolation

Within the bandwidth $\frac{\pi}{T}$, $Y(j\omega) = H(e^{j\lambda T})$

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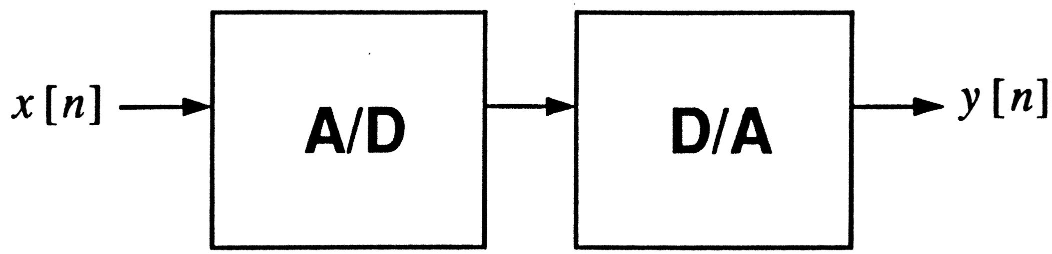
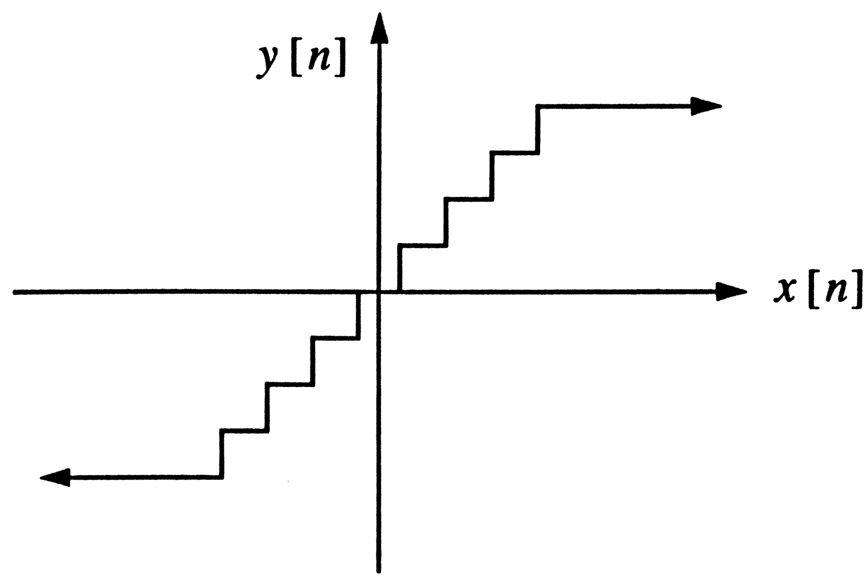
Quantization Distortion





For K bit quantizer, there are 2^K quantization intervals, with overload point at $2^{K-1} \cdot \Delta$ with step-size Δ

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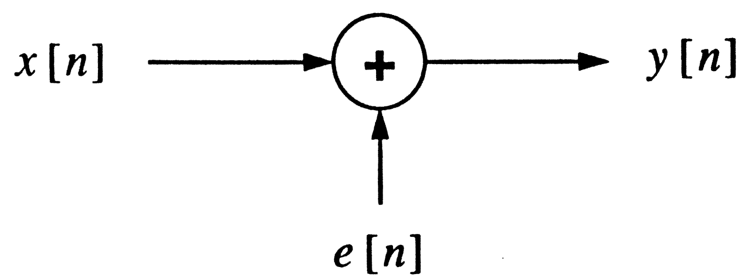
Quantization Distortion is Often Modeled as Additive White Noise



The successive samples of "quantization error" are approximately uncorrelated if the input signal is "random"

For step-size Δ, the quantization error power is approximately $\frac{\Delta^2}{12}$, or easily related to K and the overload point

In contrast to thermal noise, quantization distortion goes away when the signal is absent!

Effect of Quantization Error

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Added quantization noise at A/D converter: a price to be paid for A/D conversion

- Control by adjusting precision (number of bits)

Roundoff errors in internal computations

- Control by adjusting precision of internal arithmetic, which is typically greater than input/output

Overflow problems due to overload point of quantizer

- Limits dynamic range
- Scaling is big issue in fixed point arithmetic
- Floating point arithmetic increases the dynamic range dramatically

Change in filter frequency response due to quantization of coefficients

- Coefficient quantization normally taken account of in filter design

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Some Advantages of Digital Systems

Highest-density IC technologies (based on DRAMs) are primarily digital: poor or non-existent capacitors, etc.

Regenerative property of digital systems is extremely important in storage and transmission applications (avoids the "multiple generation problem" of analog)

Accuracy can be increased arbitrarily by increasing the precision of the arithmetic

Accuracy is forever: no component drift or temperature variations

Digital systems are deterministic: testing and fault detection are much easier

Design abstraction makes complexity easier to manage, reduces designer skill level required (analog designers difficult to find)

- Programmable solutions

Much more complex algorithms are feasible

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Design Abstraction in Digital Systems

Program
Instruction Set
Architecture
Register
Logic Element
Circuit
Device

Typically designers are split into three semi-independent groups: logic/circuit/device, instruction set/architecture/register, programmers

Much higher complexity designs become feasible

Some Disadvantages of Digital Discrete-Time Systems

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In a continuous-time world, A/D/A conversion incurs an extra cost

Quantization error is incurred at the A/D converter and internal to the computations (although it can be controlled to whatever extent necessary)

Highest-speed systems must be implemented in analog

- A/D converters and multipliers are typical bottlenecks
- Example: microwave RF

Design effort expended in finite precision issues (quantization, dynamic range)

Synchronization is major issue, particularly as the signal propagation times increase in relation to the clock cycle

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Some Examples of DSP Commercial Applications

Digital compact disk

Compressed digital television (NTSC, HDTV)

Digital television receivers

Digital audio broadcast

Digital transmission and switching in telephony

Digital cellular telephone

Voiceband data modems

Compressed video conferencing

Digital Filters

December 14, 1991

Hemant K. Thapar

IBM Corporation
San Jose, California
Telephone 284-0308

TOPICS

- Why Consider Digital Filters
- Filter Design Problem
- Digital Filter Design Tools
- Digital Filter Design Methods
- Applications

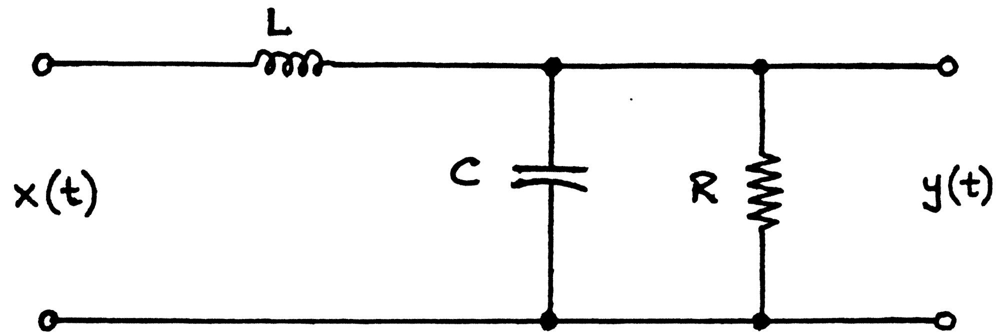
1. WHY CONSIDER DIGITAL FILTERS

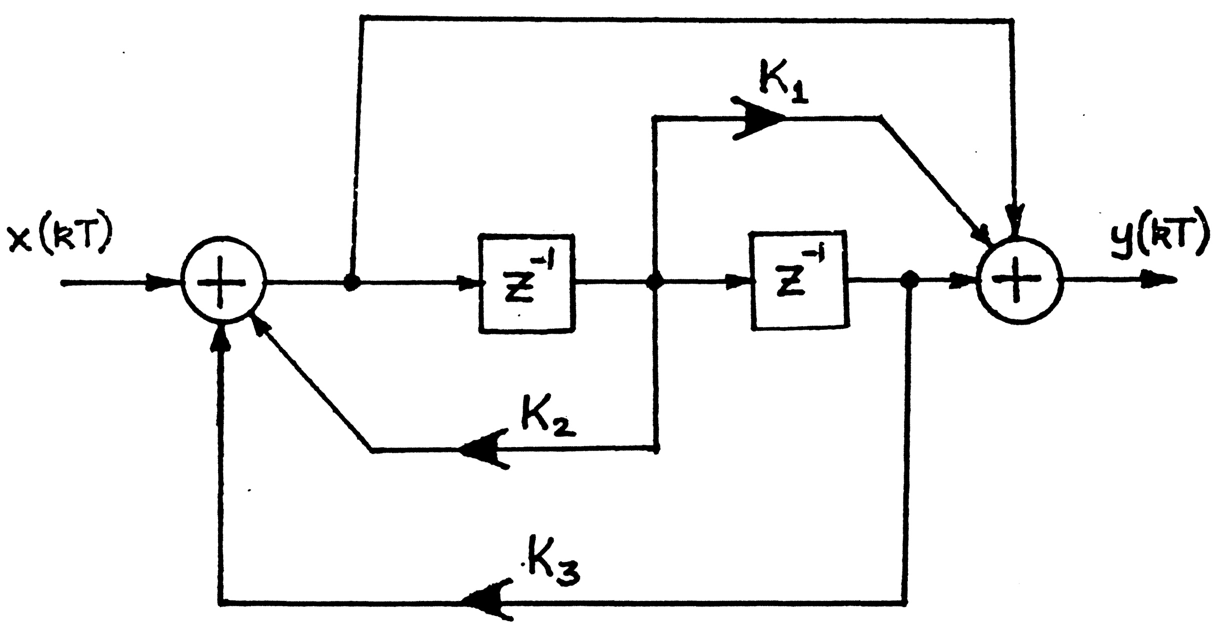
- Component tolerances (Accuracy)
- End-of-life component tolerances (Reproducibility)
- Implementation of Time-Varying Filters

  Presettable filters

  Adaptive filters
- Size
- Power Dissipation
- Control of transient response

Analog and Digital Components



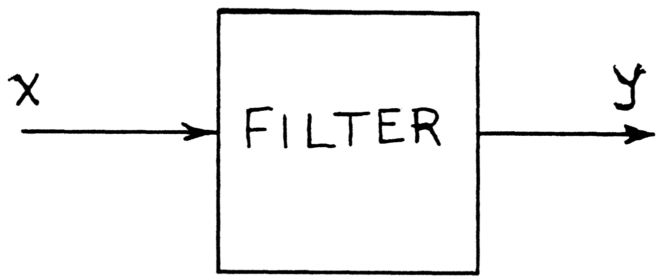


A Second-order Bandpass Filter

TOPICS

- Why Consider Digital Filters
- Filter Design Problem
- Digital Filter Design Tools
- Digital Filter Design Methods
- Applications

2. FILTER DESIGN PROBLEM



Motivation

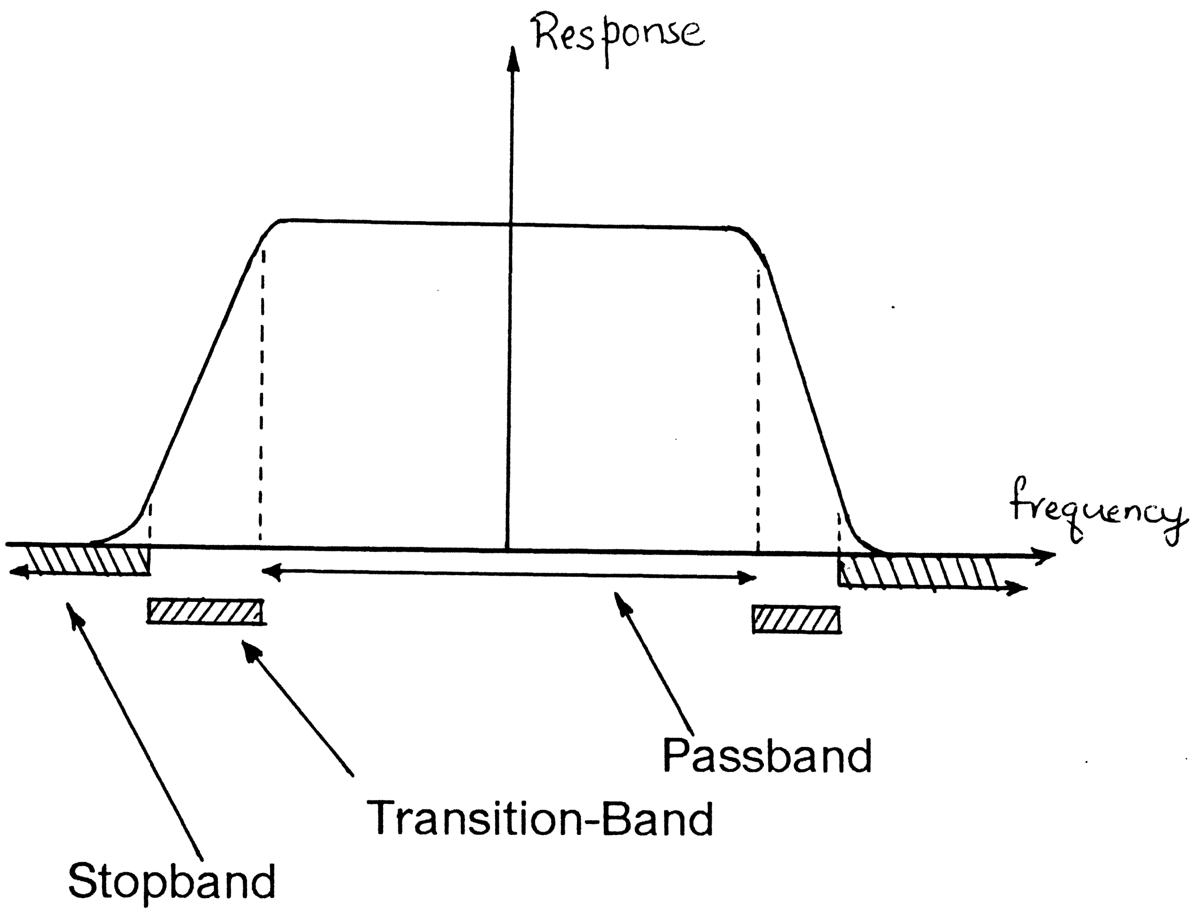
- Improve quality of the output signal:

  Remove noise, interference, and distortion.

- Process or extract information from the input:

  Estimation and prediction.

- Some notion of frequency discrimination is involved:



- Linkage between time-domain and frequency-domain behavior:

$$y(n) = \frac{1}{2\pi} \int_{-\pi}^{\pi} Y(\omega) d\omega$$

Analog and Digital Frequencies

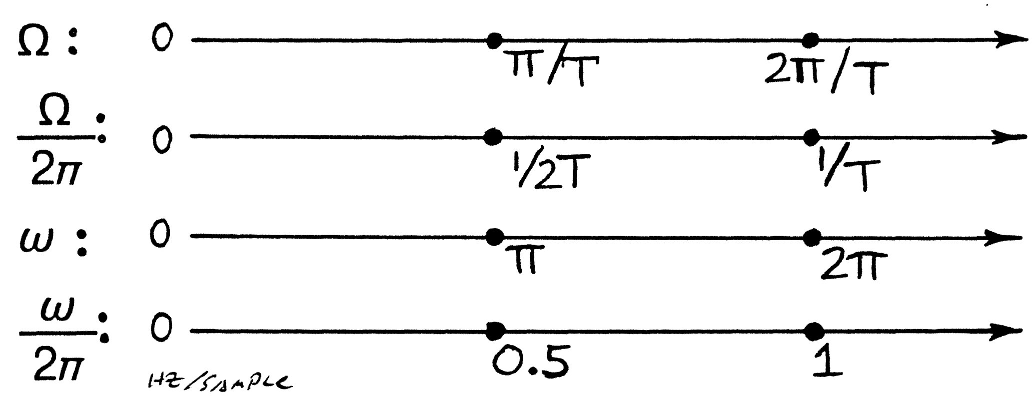
- Sampling of the analog signal

$$x_a(t) = A\cos(\Omega t + \theta)$$

produces

$$x(kT) = A\cos(\Omega kT + \theta) \;\triangleq\; A\cos(\omega k + \theta)$$

- Ω rad/ sec $\Longleftrightarrow$ $\omega = \Omega T$ *rad/sample*
- Relationship between analog and digital frequencies:



- When the Nyquist sampling theorem is satisfied, the digital frequency is always less than π radians; that is

$$\omega = \Omega T < \pi$$

TOPICS

- Why Consider Digital Filters
- Filter Design Problem
- Digital Filter Design Tools
- Digital Filter Design Methods
- Applications

3. Filter Design Tools

- Restrict the allowed structures to:

  Non-Recursive Filters

  Recursive Filters

Non-Recursive Filters

- Output is formed by linearly combining a sequence of inputs:

$$y_k = \sum_{i=-N}^{N} a_i x_{k-i}$$

Samples: $\ldots x_{k+2} \quad x_{k+1} \quad x_k \quad x_{k-1}\ldots$

Multiply: ... $x \quad x \quad x \quad x\ldots$

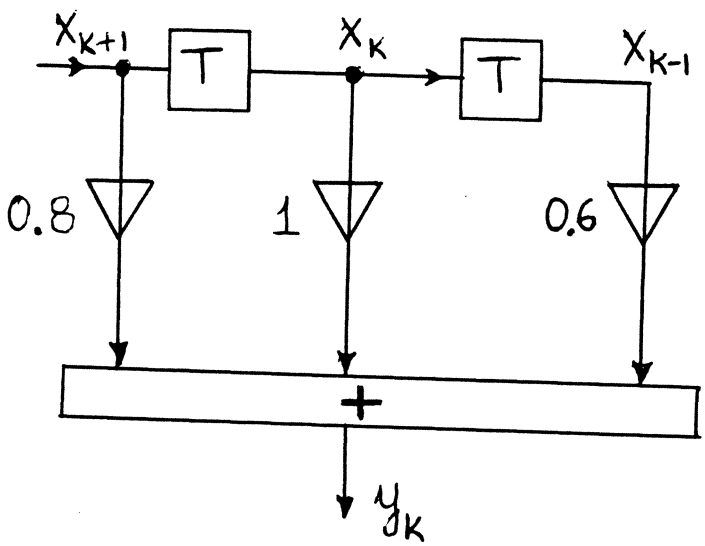
Coefficients: $\ldots a_{-2} \quad a_{-1} \quad a_0 \quad a_1 \quad \ldots$

Sum: $+$

Output: y_k

Example: $a_{-1} = 0.8, \quad a_0 = 1, \quad a_1 = 0.6$

$$\Rightarrow \quad y_k = 0.8x_{k+1} + x_k + 0.6x_{k-1}$$



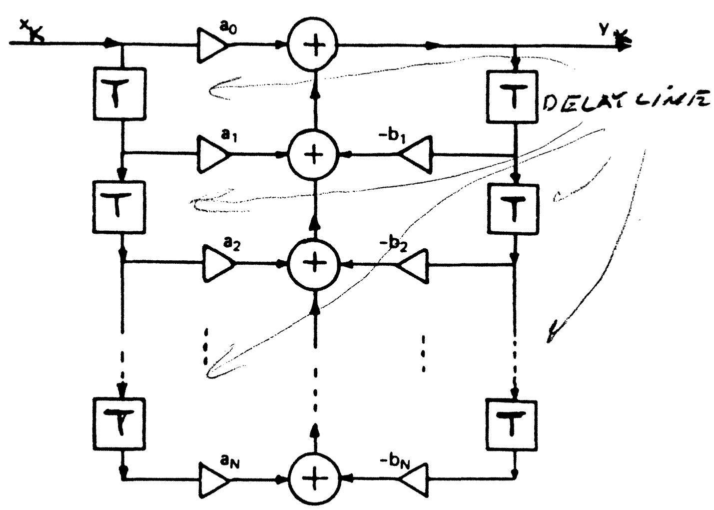
Recursive Filters

UNSTABLE - SINUSOIDAL OUTPUT UNDESIRABLE

- Output is formed by linearly combining sequences of inputs and previous outputs:

$$y_k = \sum_{i=0}^{N} a_i x_{k-i} + \sum_{l=1}^{M} b_l y_{k-l}$$

- Output at time k depends upon the previous outputs. Therefore, initial conditions must be known before the output due to the first input can be computed.



CAN NOT BE OPTIMIZED.

Unit Pulse Response

- Response for a unit pulse input, defined as:

$$x_k = \begin{cases} 1 & , k = 0 \\ 0, & otherwise \end{cases}$$

Nonrecursive Filters: VERY STABLE, CAN BE OPTIMIZED

$$h_k \triangleq y_k = \sum_{i=-N}^{N} a_i x_{k-i}$$

$$= a_k$$

- The unit pulse response is a finite sequence of (2N + 1) terms. Such filters are, therefore, often referred to as FINITE IMPULSE RESPONSE (FIR) filters.

Recursive Filters:

$$h_k \triangleq y_k = \sum_{i=0}^{N} a_i x_{k-i} + \sum_{l=1}^{M} b_l y_{k-l}$$

- Even though there are a finite number of a_ks, the second term can continue to generate an output long after the first term is zero. Such filters are, therefore, often referred to as INFINITE IMPULSE RESPONSE (IIR) filters.

Properties

- Homogeneity and Superposition:

$$\text{if} \quad x_k \Rightarrow y_k \quad \text{and} \quad s_k \Rightarrow r_k$$

$$\text{then} \qquad f x_k + g s_k \Rightarrow f y_k + g r_k$$

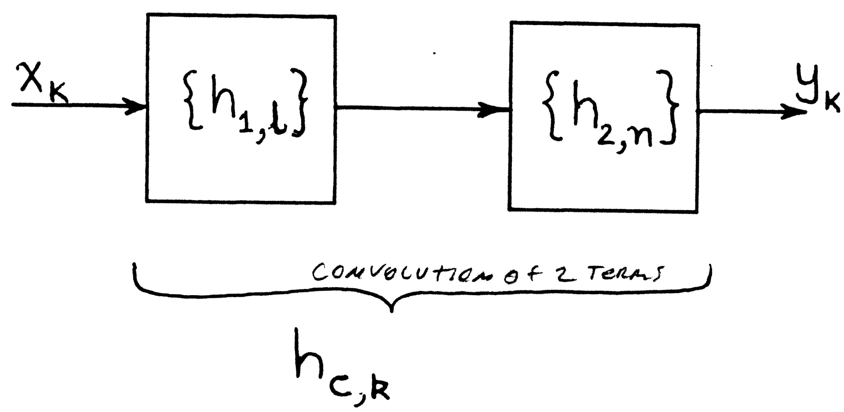
- Shift-invariance:

$$\text{if} \quad x_k \Rightarrow y_k \quad \text{then} \quad x_{k-l} \Rightarrow y_{k-l}$$

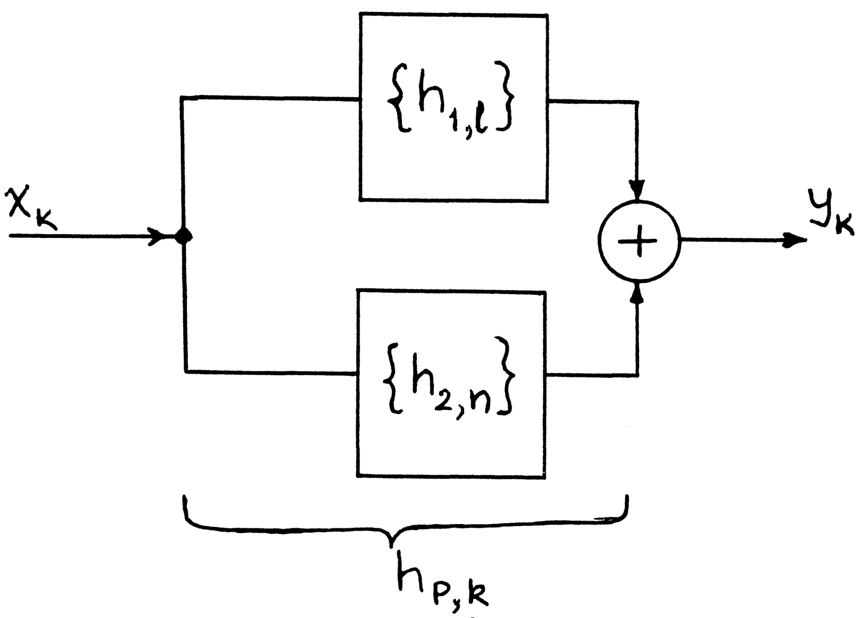
- Filters that admit homogeneity, superposition, and shift-invariance are referred to as linear, time-invariant (LTI) filters.
- Input-Output of such filters can be defined by the discrete-time convolution:

$$y_k = \sum_{i=-\infty}^{\infty} x_i h_{k-i}$$

Structures

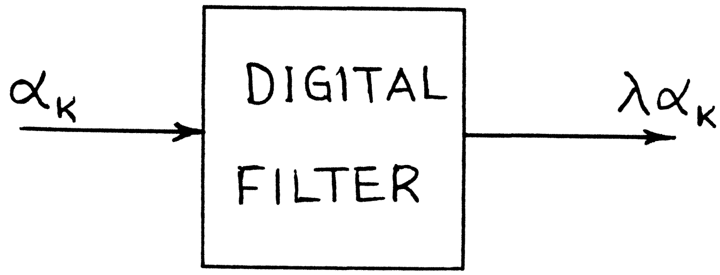


- Cascade: $h_{C,k} = \sum_{l=-\infty}^{\infty} h_{1,l} h_{2,k-l}$



- Parallel: $h_{P,k} = h_{1,k} + h_{2,k}$

Eigenfunctions



- Def: α_k is an eigenfunction of the digital filter iff the application of α_k produces the scaled output $\lambda\alpha_k$. λ is referred to as the eigenvalue.

$$\lambda\alpha_a = \sum_{j=-\infty}^{\infty} h_a - \alpha_{k-i}$$

Eigenfunction 1:

$$a_k = \exp(j\omega k) = \cos(\omega k) + j\sin(\omega k)$$

produces an output

$$\exp(j\omega k)\left[\sum_{l=-\infty}^{\infty} h_l e^{-j\omega l}\right]$$

- $H(\omega) = \sum_{l=-\infty}^{\infty} h_l e^{-j\omega l}$ is referred to as the frequency response of the digital filter. Note that h_l uniquely determines $H(\omega)$.
- $H(\omega)$ is, in general, complex, and may be written as

  $H(\omega) = |\, H(\omega) \,|\, e^{\phi(\omega)}$

  Then, if the input is $\cos \omega k$, the output is given by $|\, H(\omega) \,| \cos(\omega k + \phi)$.

Eigenfunction 2:

$$a_k = z^k$$

produces an output

$$z^k \left[\sum_{l=-\infty}^{\infty} h_l z^{-l} \right]$$

- $H(z) = \sum_{l=-\infty}^{\infty} h_l z^{-l}$ is referred to as the transfer function of the digital filter. Note that h_l uniquely determines $H(z)$.

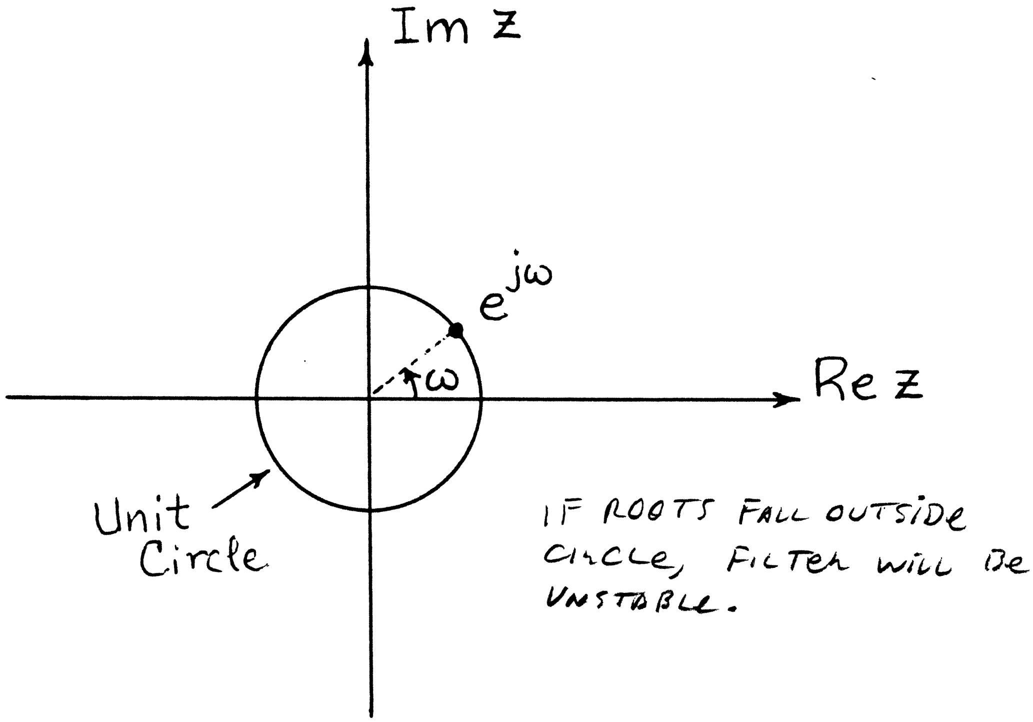
- $$Y(z) = H(z) X(z)$$

$$Y(z) = \ldots + y_0 + y_1 z^{-1} + y_2 z^{-2} + y_3 z^{-3} + \ldots$$

$$y(k) = \{\ldots y_0 \; y_1 \; y_2 \; y_3 \ldots\}$$

Z-transform and Frequency Response

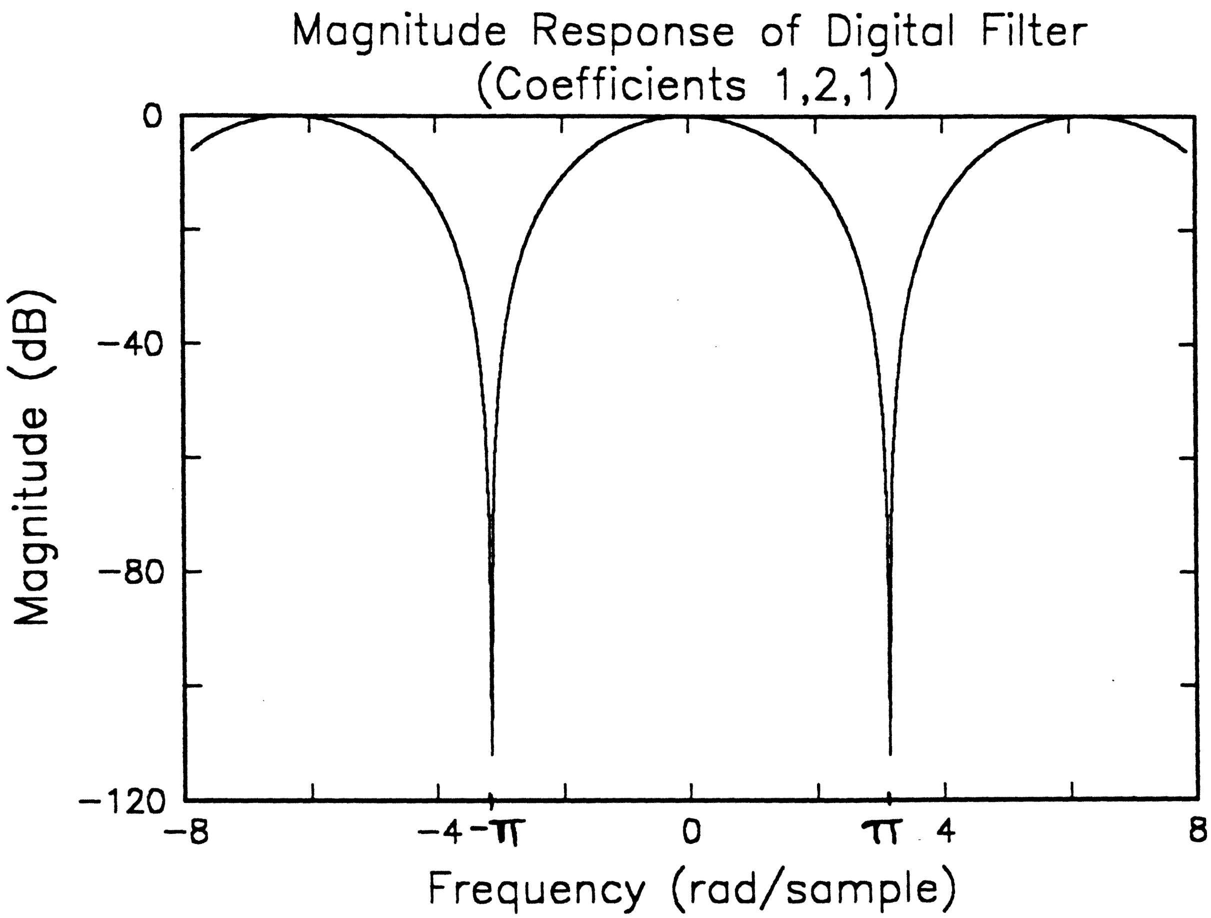
- $H(\omega) = H(z)\,\Big|_{z=\exp(-j\omega)} = \sum_{l=-\infty}^{\infty} h_l e^{-j\omega l}$
- Geometrical interpretation



- Frequency response for digital filters is periodic in 2π.

An Example

$$h_{-1} = 1, \qquad h_0 = 2, \qquad h_1 = 1$$



Frequency Response of FIR and IIR Filters

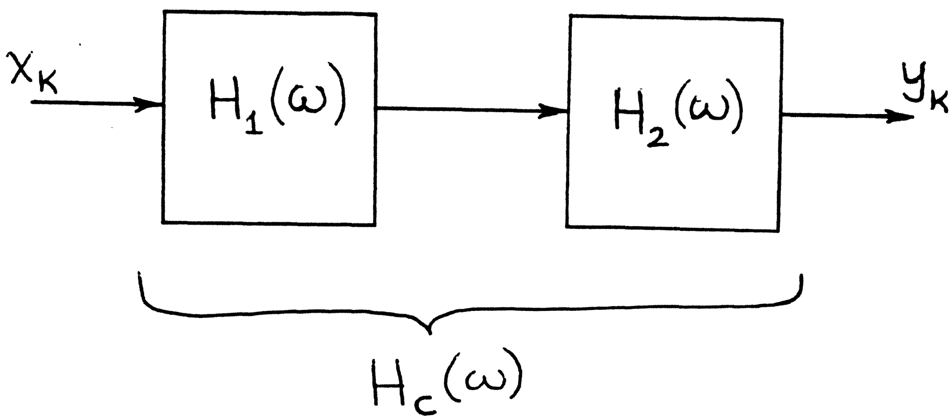
- FIR Filters

$$H(\omega) = \sum_{l=-N}^{N} a_l e^{-j\omega l}$$

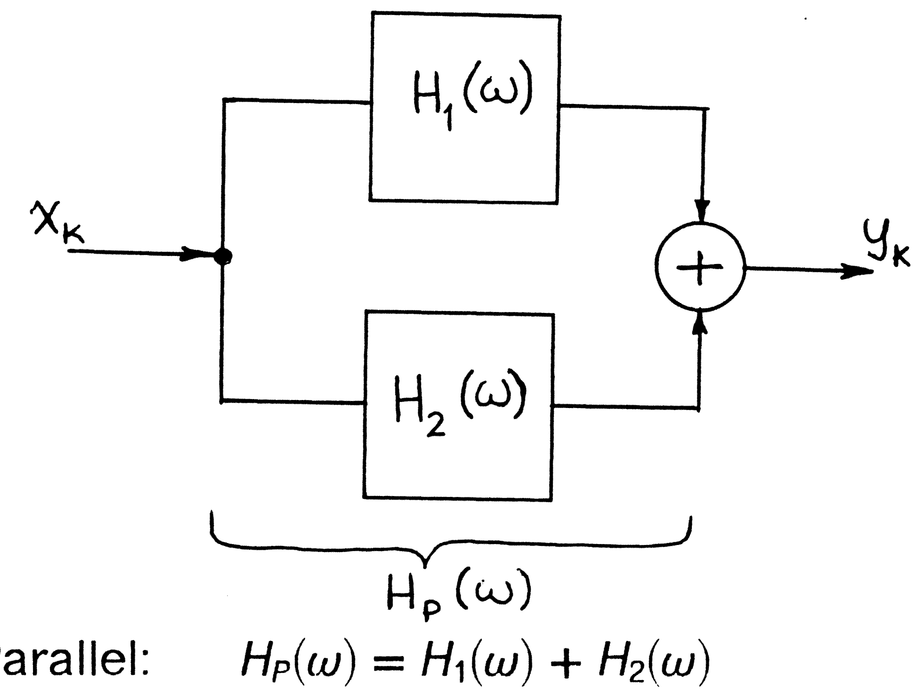
- Recursive Filters

$$H(\omega) = \frac{\sum_{i=0}^{N} a_i e^{-j\omega i}}{1 - \sum_{m=1}^{M} b_m e^{-j\omega m}}$$

Cascade and Parallel Forms



- Cascade: $H_C(\omega) = H_1(\omega)H_2(\omega)$



- Parallel: $H_P(\omega) = H_1(\omega) + H_2(\omega)$

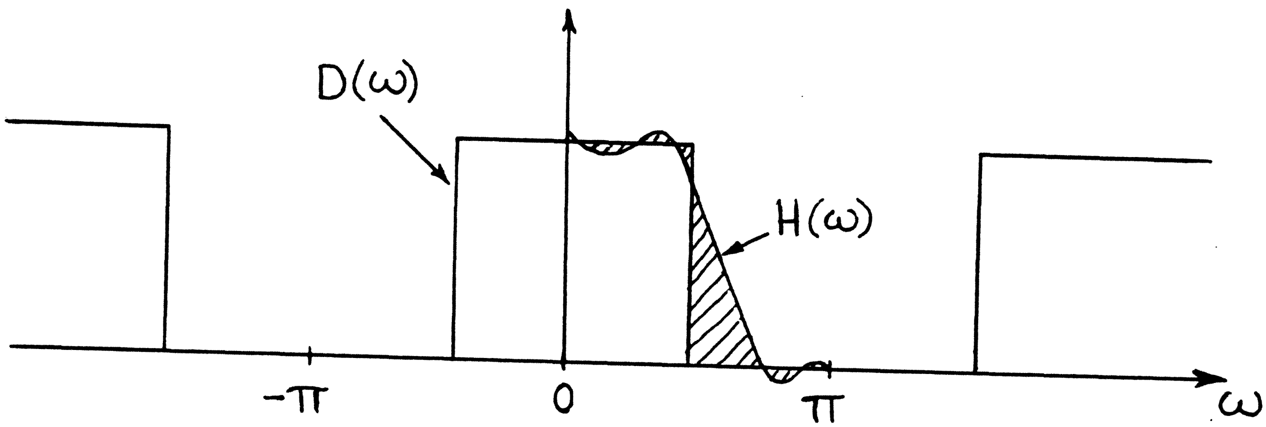
COMPLEX NUMBERS — TAKE CARE IF CIRCUIT // TO WORK.

TOPICS

- Why Consider Digital Filters
- Filter Design Problem
- Digital Filter Design Tools
- Digital Filter Design Methods
- Applications

4. Filter Design Methods

Fourier Series



$$\textit{Error:} \quad E(\omega) = D(\omega) - H(\omega)$$

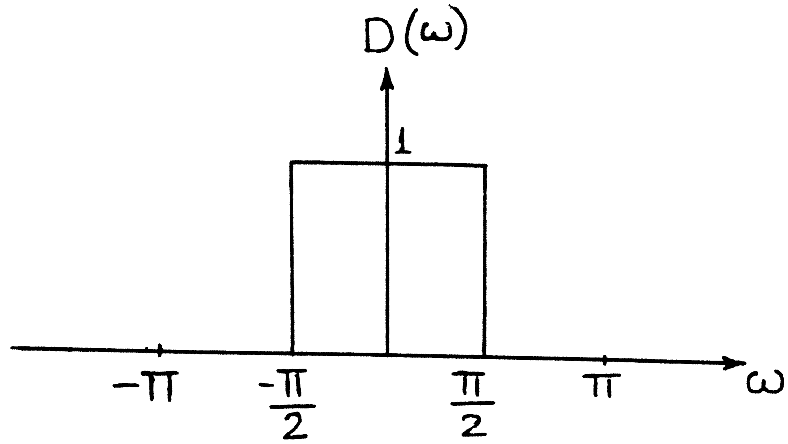
$$\textit{Squared-error:} \quad \varepsilon = \int_{-\pi}^{\pi} |E(\omega)|^2 d\omega$$

$$\min \varepsilon \ \Rightarrow \ h_k = \frac{1}{2\pi} \int_{-\pi}^{\pi} D(\omega) e^{j\omega k} d\omega$$

- The h_k sequence generates the smallest integral squared-error than any other response.
- Each h_k is computed independently; value of one term does not affect the other.
- Set $a_k = h_k$.
- Truncation error is given by:

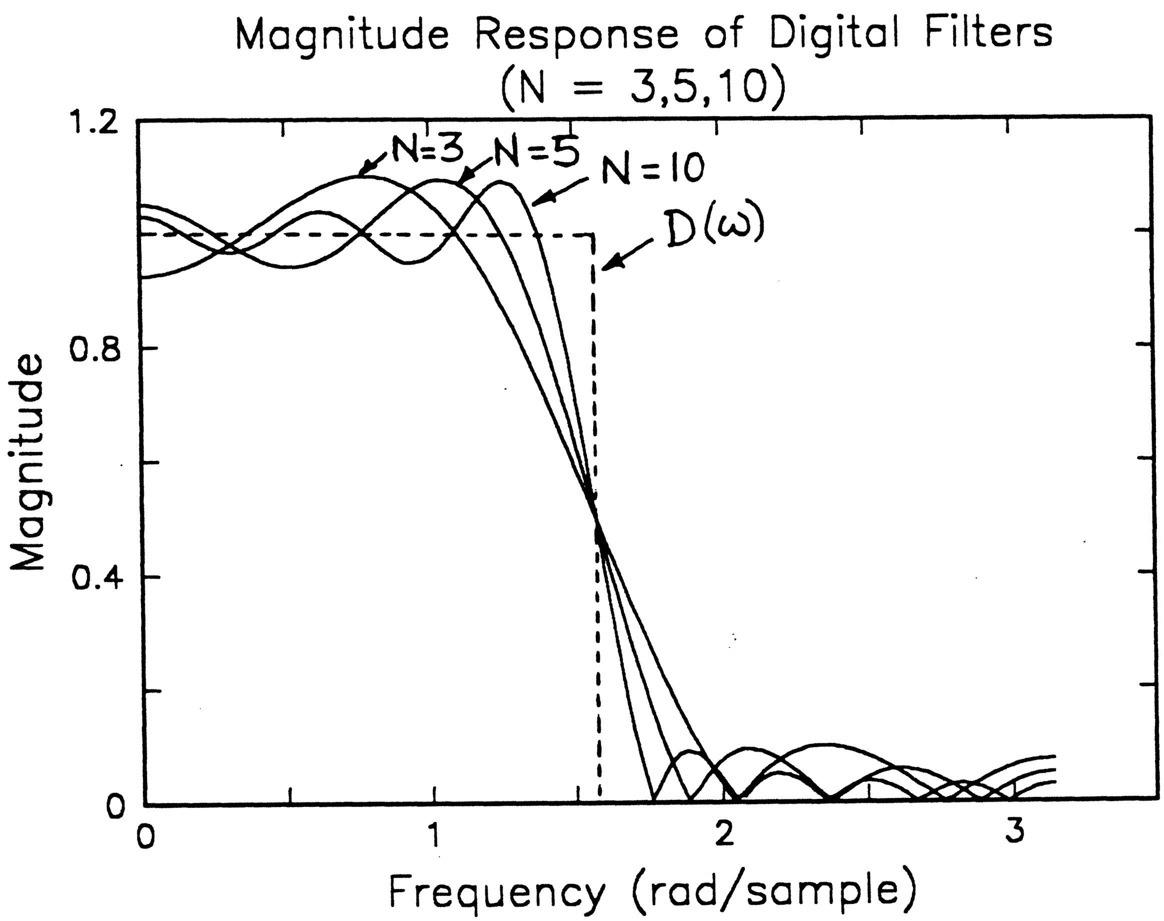
$$\varepsilon_T = \int_{-\pi}^{\pi} | D(\omega) |^2 d\omega - 2\pi \sum_{i=-N}^{N} | a_i |^2$$

An Example

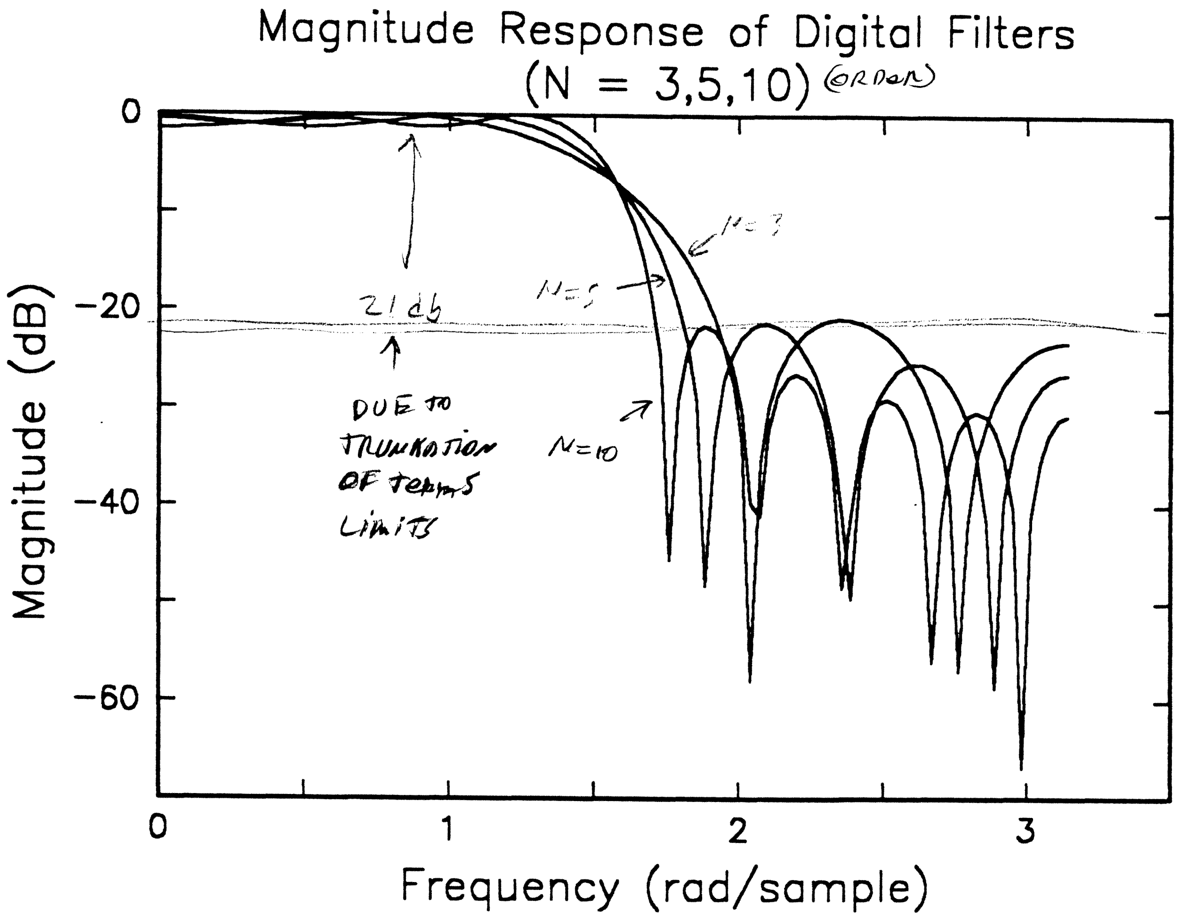


$$h_k = \frac{1}{\pi k}\sin\left(\frac{\pi k}{2}\right), \qquad h_0 = 0.5$$

Frequency Response as a function of N



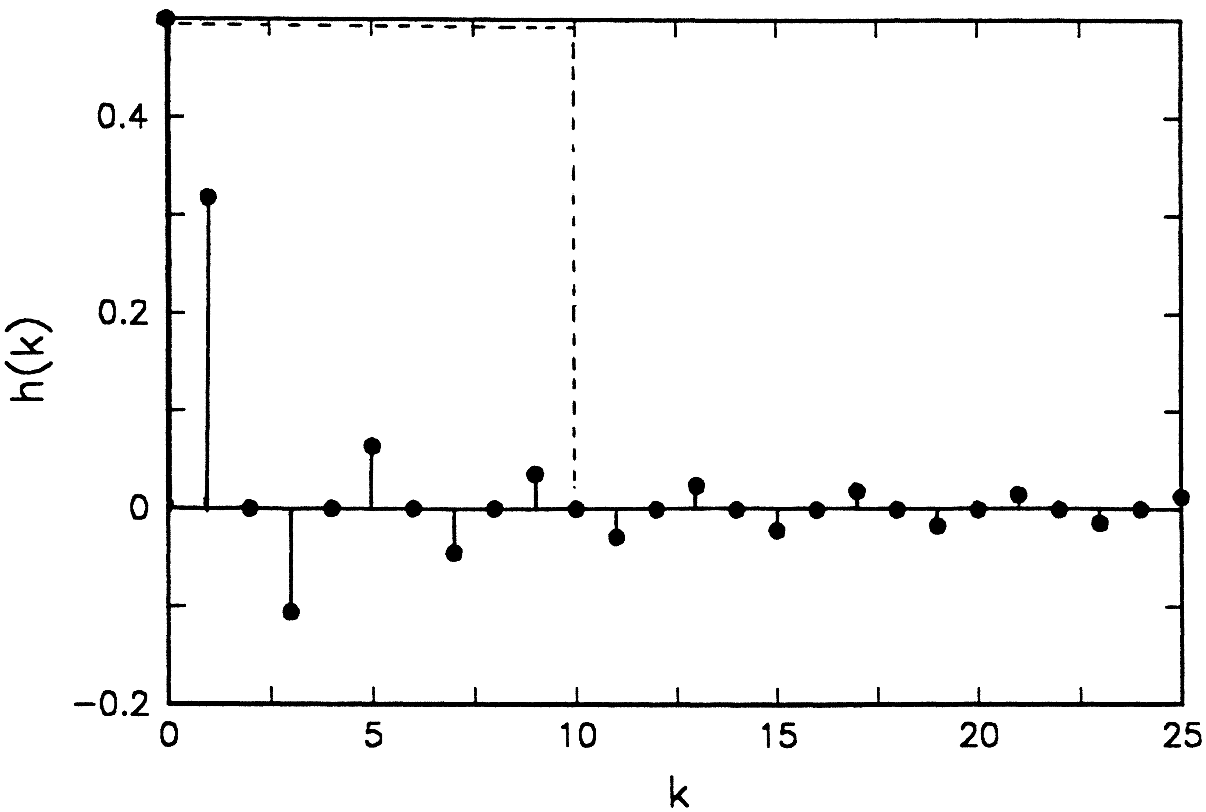
Frequency Response as a function of N



Windowing

- Rectangular Window

Low–pass Filter Coefficients based on the Fourier Series Method



- Other windowing functions are used to achieve more desirable control of passband ripple and/or stopband attenuation.

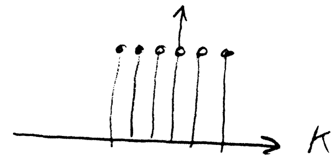
$$a_K = w_k \, h_K$$

WINDOW FUNCTION COEF.

Commonly-used Windowing Functions

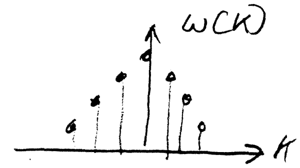
- Rectangular:

$$w(k) = 1$$



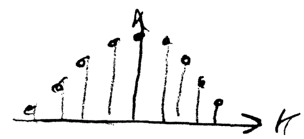
- Triangular:

$$w(k) = 1 - \frac{|k|}{M+1}, \quad M = 2N + 2$$



- Hann:

$$w(k) = \frac{1}{2}\left(1 + \cos\frac{2\pi k}{M}\right), \quad M = 2N + 2$$



- Hamming:

$$w(k) = 0.54 + 0.46 cos\frac{2\pi k}{M}, \qquad M = 2N + 2$$

- Blackman:

$$w(k) = 0.42 + 0.5 cos\frac{2\pi k}{M} + 0.08\cos\frac{4\pi k}{M}, \qquad M = 2N + 2$$

- Kaiser:

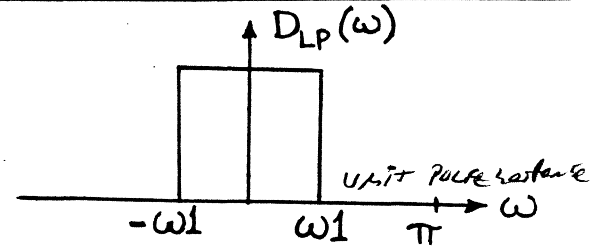
$$w(k) = \begin{cases} I_0\left[\beta\sqrt{1-\left(\frac{k}{(2N+1)/2}\right)^2}\right] \Big/ I_0(\beta) & ; -N \le k \le N \\ 0 & , \text{otherwise} \end{cases}$$

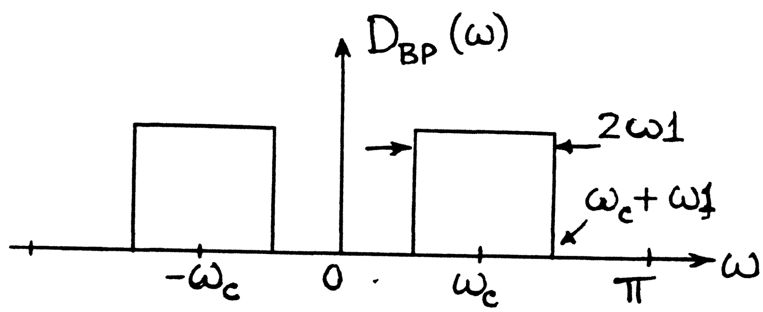
where

$$I_0(z) = 1 + \sum_{m=1}^{\infty}\left[\frac{(z/2)^m}{m!}\right]$$

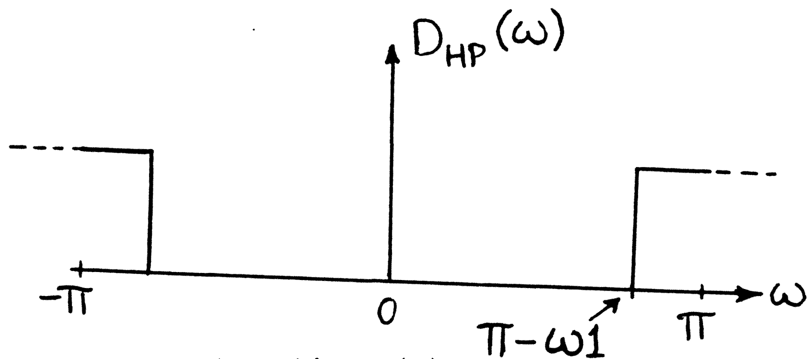
Filter Transformations

Low-pass	$h_{LP}(k)$

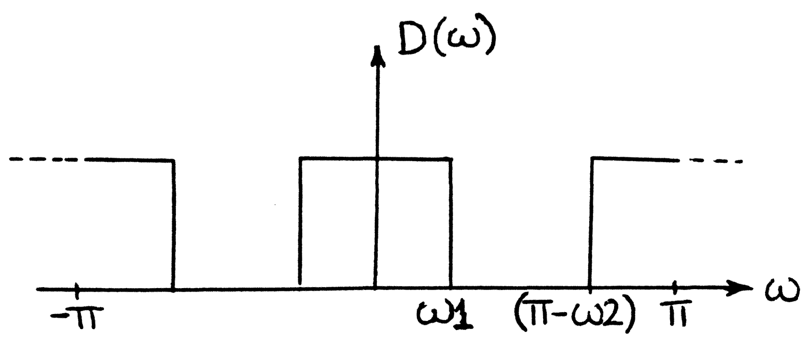




- Band-pass $\quad 2h_{LP}(k)\cos(\omega_c k)$

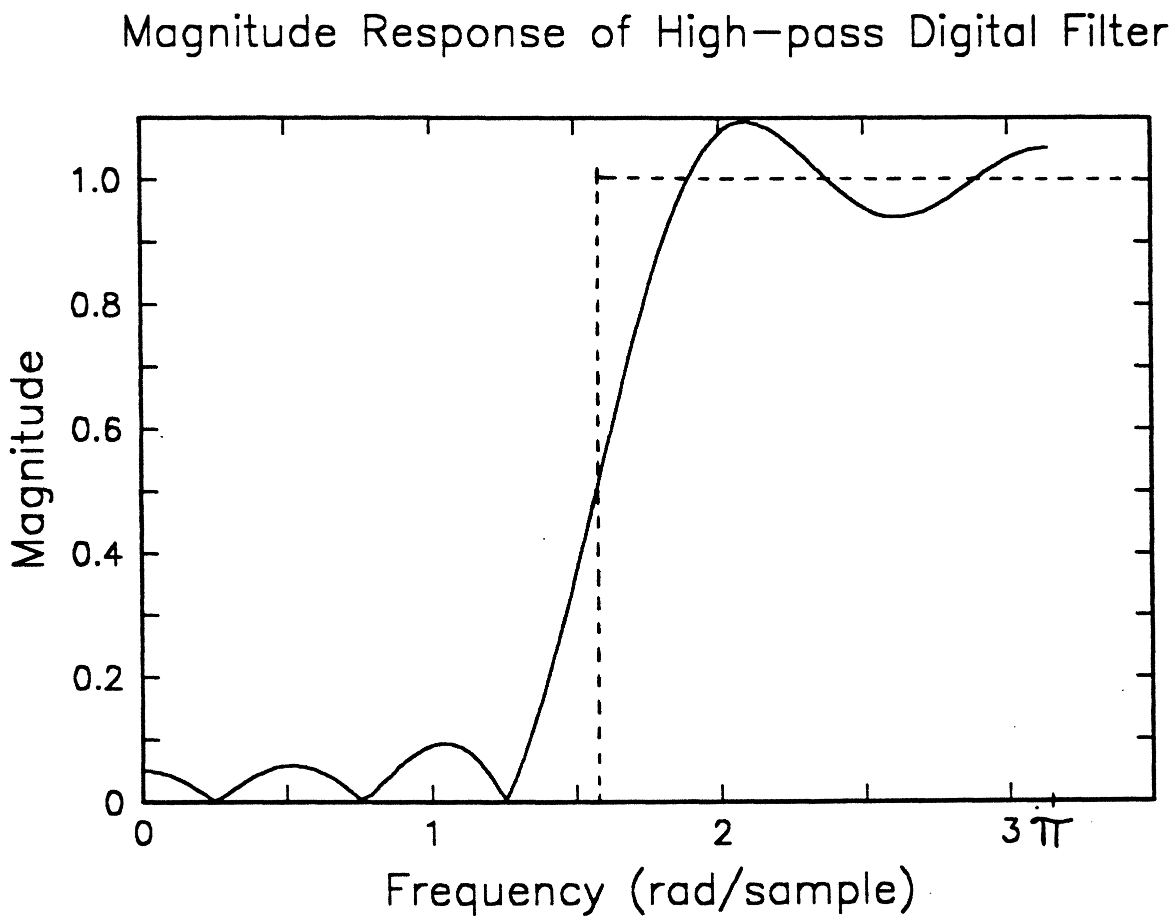


- High-pass $\quad (-1)^k h_{LP}(k)$



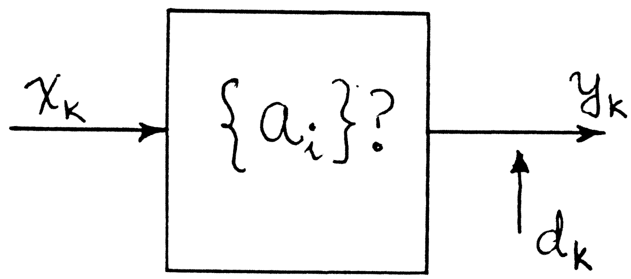
- Notch $\quad h_{LP,\,\omega 1}(k) + (-1)^k h_{LP,\pi-\omega 2}$

An Example



Low−pass Coefficients: 0.064 1.6E−17 −0.11 −1.6E−17 0.32 0.5 0.32 −1.6E−17 −0.11 1.6E−17 0.064
High−pass Coefficients: −0.064 1.6E−17 0.11 −1.6E−17 −0.32 0.5 −0.32 −1.6E−17 0.11 1.6E−17 −0.064

Time-Domain Design Method



- Input sequence, x_k, and the desired output sequence, d_k are known; the problem is to determine a_k.
- Define

$$\underline{a} = [\ a_{-N}\ \ a_{-N+1}\ \ \cdots\ \ a_N]$$

$$\underline{d} = [\ d_0\ \ d_1\ \ \cdots\ \ d_p], \qquad p \geq 2N+1$$

$$\underline{x} = [\ x_{-N}\ \ x_{-N+1}\ \ \cdots\ \ x_{p+N}].$$

- Set-up p + 1 equations of the form

$$\underbrace{\begin{bmatrix} x_{-N} & x_{-N+1} & \cdots & x_N \\ x_{-N+1} & x_{-N+2} & \cdots & x_{N+1} \\ \vdots & & & \\ x_{p-N} & x_{p-N+1} & \cdots & x_{p+N} \end{bmatrix}}_{\triangleq \underset{\sim}{H}} \underbrace{\begin{bmatrix} a_{-N} \\ a_{-N+1} \\ \vdots \\ a_N \end{bmatrix}}_{\underline{a}^T} = \underbrace{\begin{bmatrix} d_0 \\ d_1 \\ d_2 \\ \vdots \\ d_p \end{bmatrix}}_{\underline{d}^T}$$

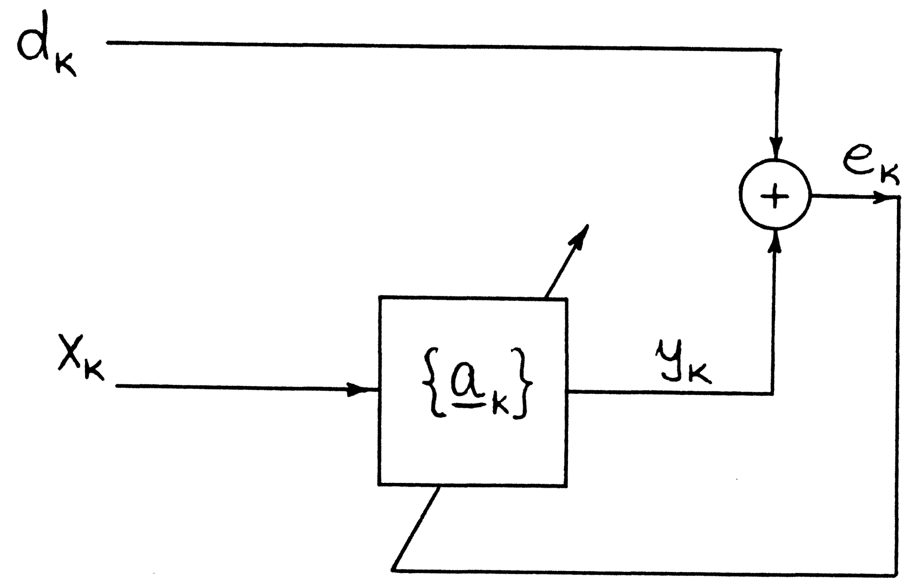
- Use least-squares solution to the over-determined system of equations to obtain

$$\underline{a}_{OPT}^{T} = (\underset{\sim}{H}^{T}\underset{\sim}{H})^{-1}\underset{\sim}{H}^{T}\underline{d}^{T}$$

- The above equation is of the form

$$\underline{a}_{OPT} = \underset{\sim}{\Phi}^{-1}\underline{\xi}$$

Adaptive Filtering



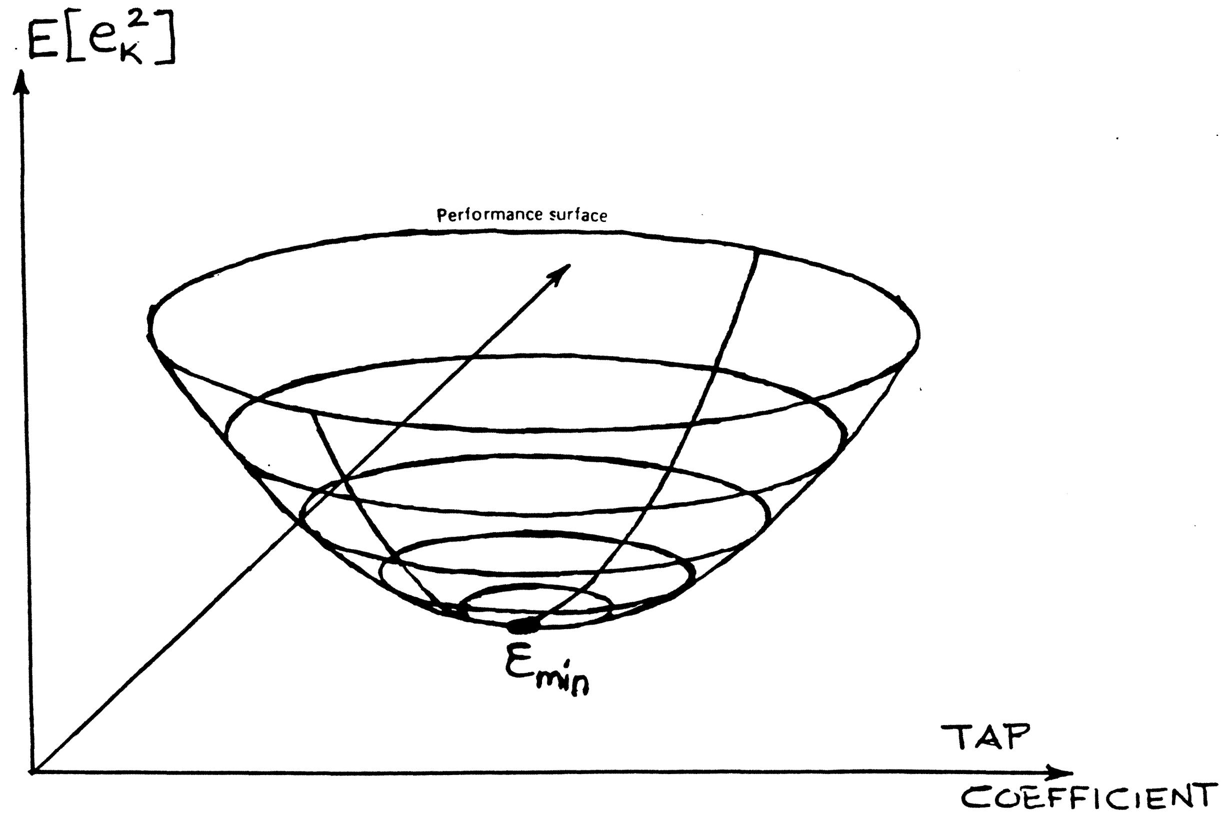
Application	x	d
System Identification	Known Data	Output Signal
Equalization	Distorted Signal	"Known" Data
Prediction	Past Input	Present Input

Commonly-used Approach

- Minimize the mean-squared error between the desired output, d, and a linear combination of the input, x; that, is:

$$E[e_k{}^2] = E[(d_k - y_k)^2] = E[(d_k - \sum_i a_i x_{k-i})^2]$$

- The above error criterion defines a convex surface for the mean-squared error as a function of the tap weights:



- The adaptive filter starts with an initial guess on the coefficients, $\underline{a}_0$, and progressively moves down the well using:

$$\underline{a}_k = \underline{a}_{k-1} - \beta \nabla_{\underline{a}_k} E\left[e_k^{\,2}\right]$$

- In practice, the gradient of the instantaneous squared-error is substituted for the mean squared-error, resulting in the following adaptive algorithm (most commonly referred to as the LMS algorithm):

$$\underline{a}_k = \underline{a}_{k-1} + 2\beta e_k \underline{x}_k$$

- The LMS algorithm is the most commonly-used algorithm in real-time adaptive filtering.

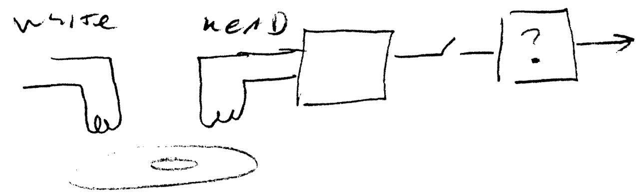
TOPICS

- Why Consider Digital Filters
- Filter Design Problem
- Digital Filter Design Tools
- Digital Filter Design Methods
- Applications

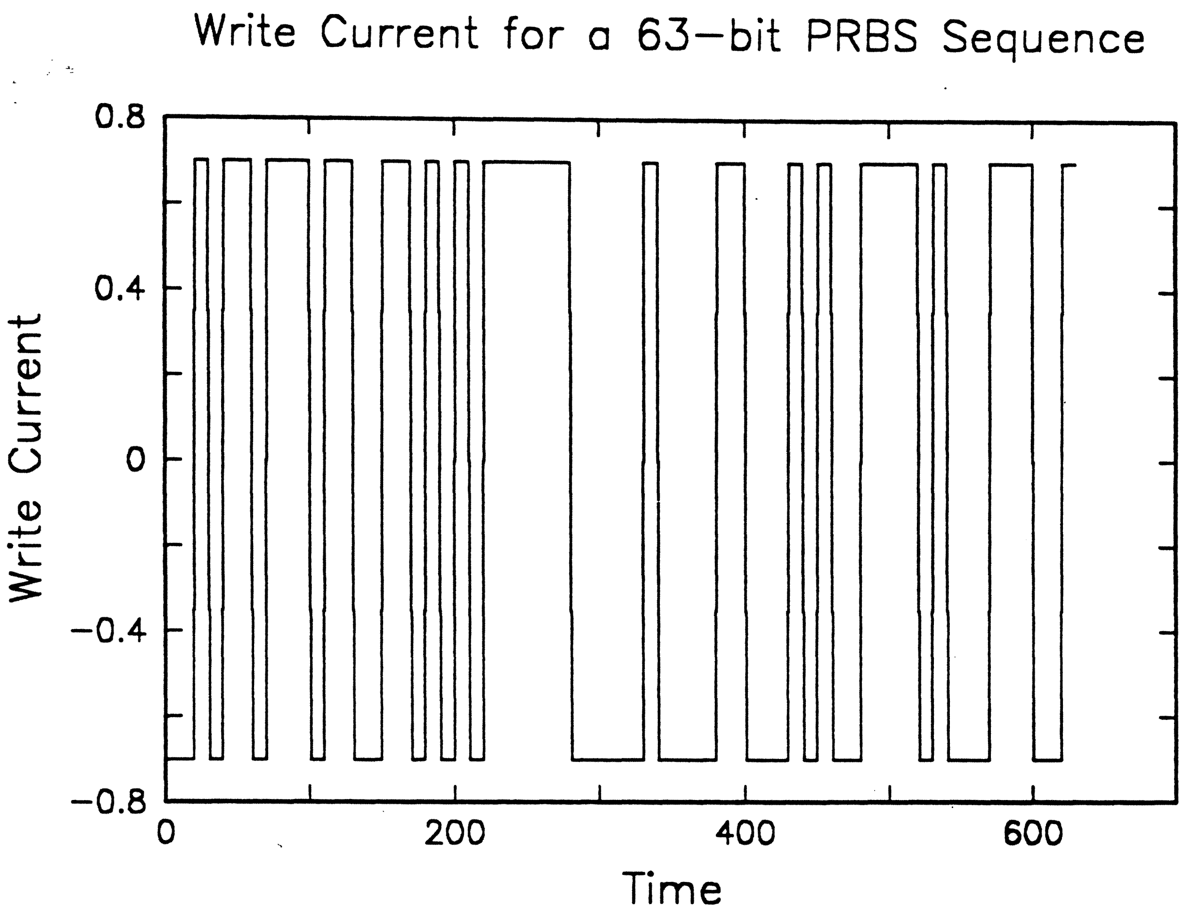
5. Applications in Digital Storage

- Recording Channel Identification
- Equalization
- Timing and Gain Control
- Digital servo

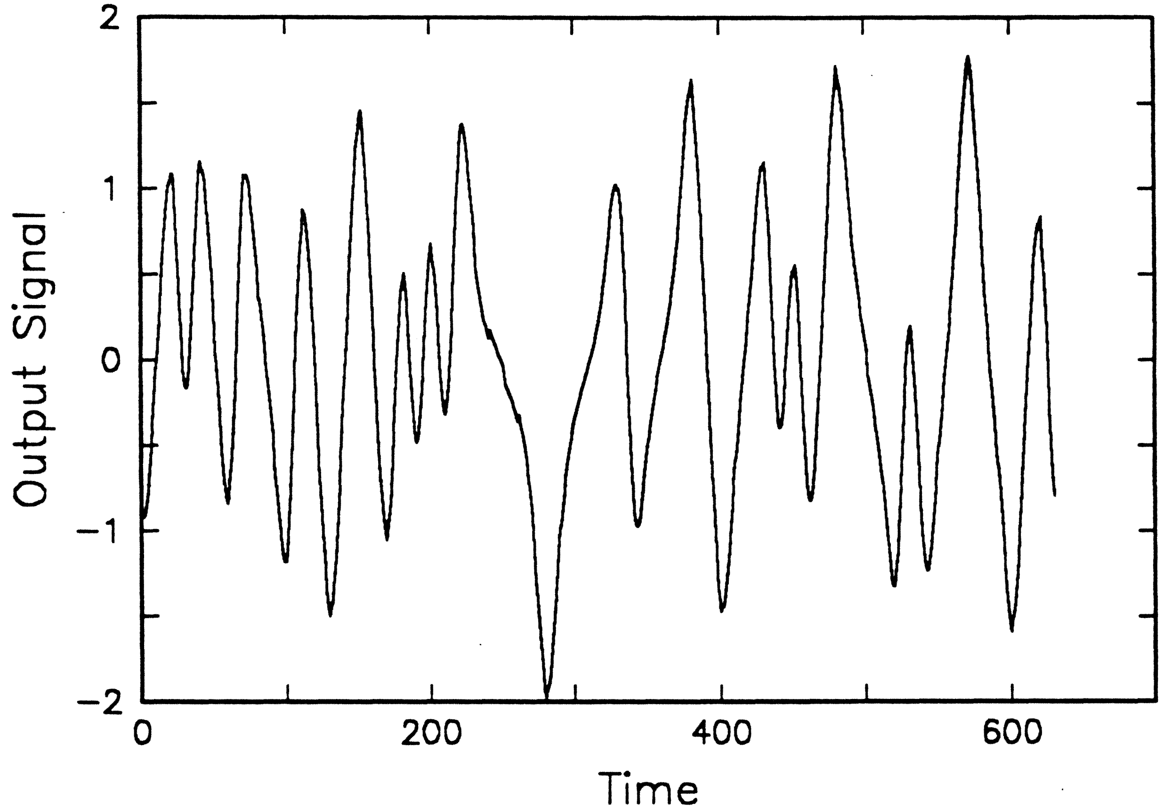
Recording Channel Identification



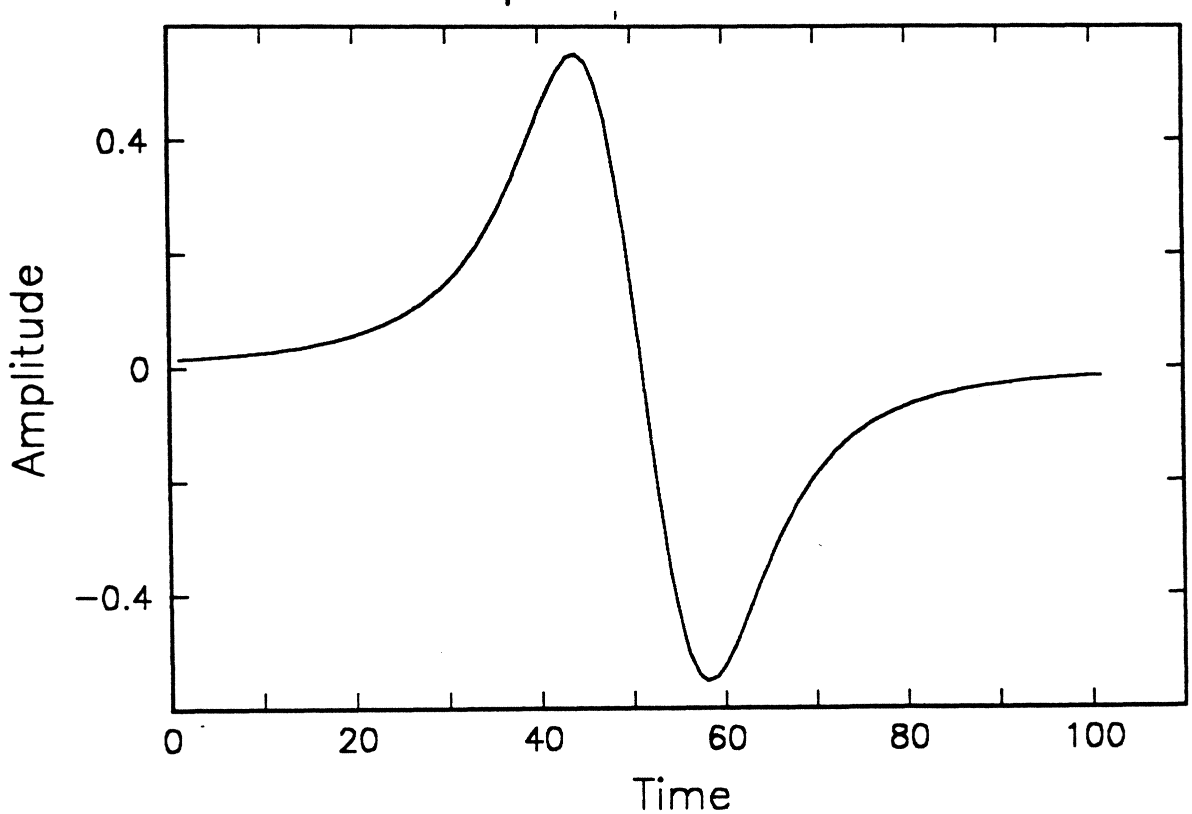
- Input Sequence



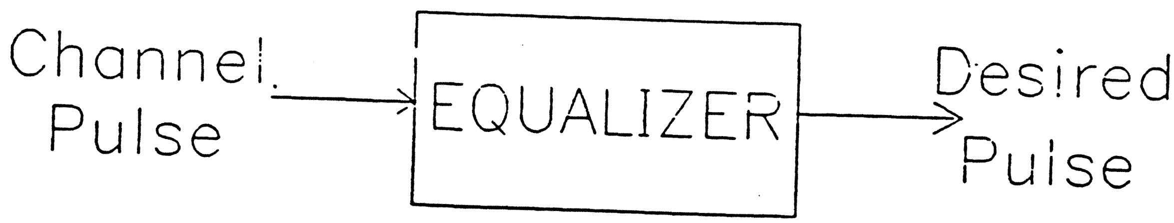
- Averaged Output Waveform

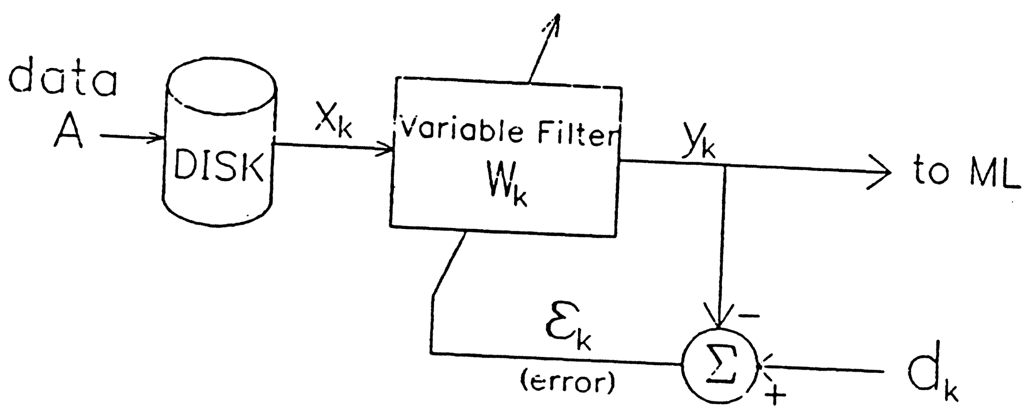


- Identified Pulse Response



Equalization





6. SUMMARY

- Why consider digital filters:

  Component tolerances (Accuracy)

  End-of-life component tolerances (Reproducibility)

  Implementation of Time-Varying Filters

  Size

  Power Dissipation

  Control of transient response

  Design abstraction

- Pitfalls in digital filter design:

  Relationship between analog and digital frequencies

  Direction of sample shifting

  Aliasing

  Finite precision and arithmetic

  Step-size selection

A/D AND D/A CONVERTERS IN HDD SYSTEMS:

- Servo Channel Requirements/Solutions
    - High Capacity Drives
    - Small Size Drives
- Technology options for a possible read – channel architecture.

BILL HUNT
ANALOG DEVICES
DEC '91.

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"DEDICATED V'S EMBEDDED SERVO"

Complete embedded servo front end for HDD

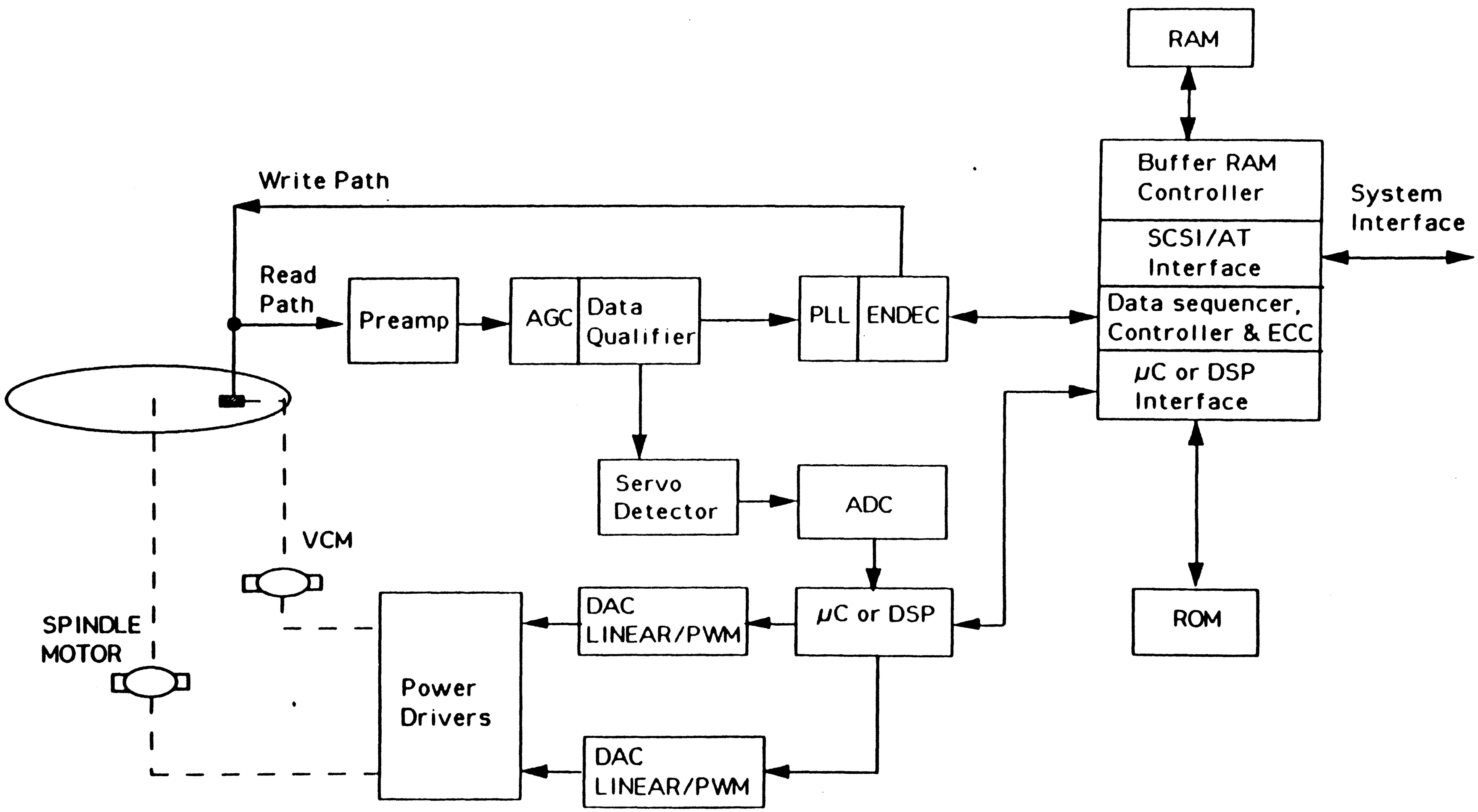
Trends in HDD servo electronics: a) New demodulator techniques

ii) Embedded servo vs dedicated surface

- 3 platters => 6 surfaces
  use 5 for data, 1 for servo
- surfaces mechanically linked
- continuous position f/back

- 1 platter => 2 surfaces
  interleave data and servo
- no registration problems
- sampled position f/back

GENERIC BLOCK DIAGRAM FOR CLASSICAL LARGE CAPACITY/SMALL SIZE HDD'S



"CAPACITY"

– a possible classification

HIGH CAPACITY: > 300 MBYTE

- Size 5 1/4" to 3 1/2 x 1"
- Capacity 300 Mb – > 1Gb
- Access time: 10 mSEC
- Transfer rate: > 15 MB/S
- Improved Reliability (ELF)/(MTTF)
- Reducing cost

SMALL SIZE < 100M BYTES

- Size 3 1/2" to 2 1/2" to 1.8"
- Capacity 20 to 100 mb
- Low power
- "Zero" power in power down mode
- Lower supply voltage (smaller batteries) 3V
- Improved Reliability (ELF)/(MTTF)
- Reducing Cost

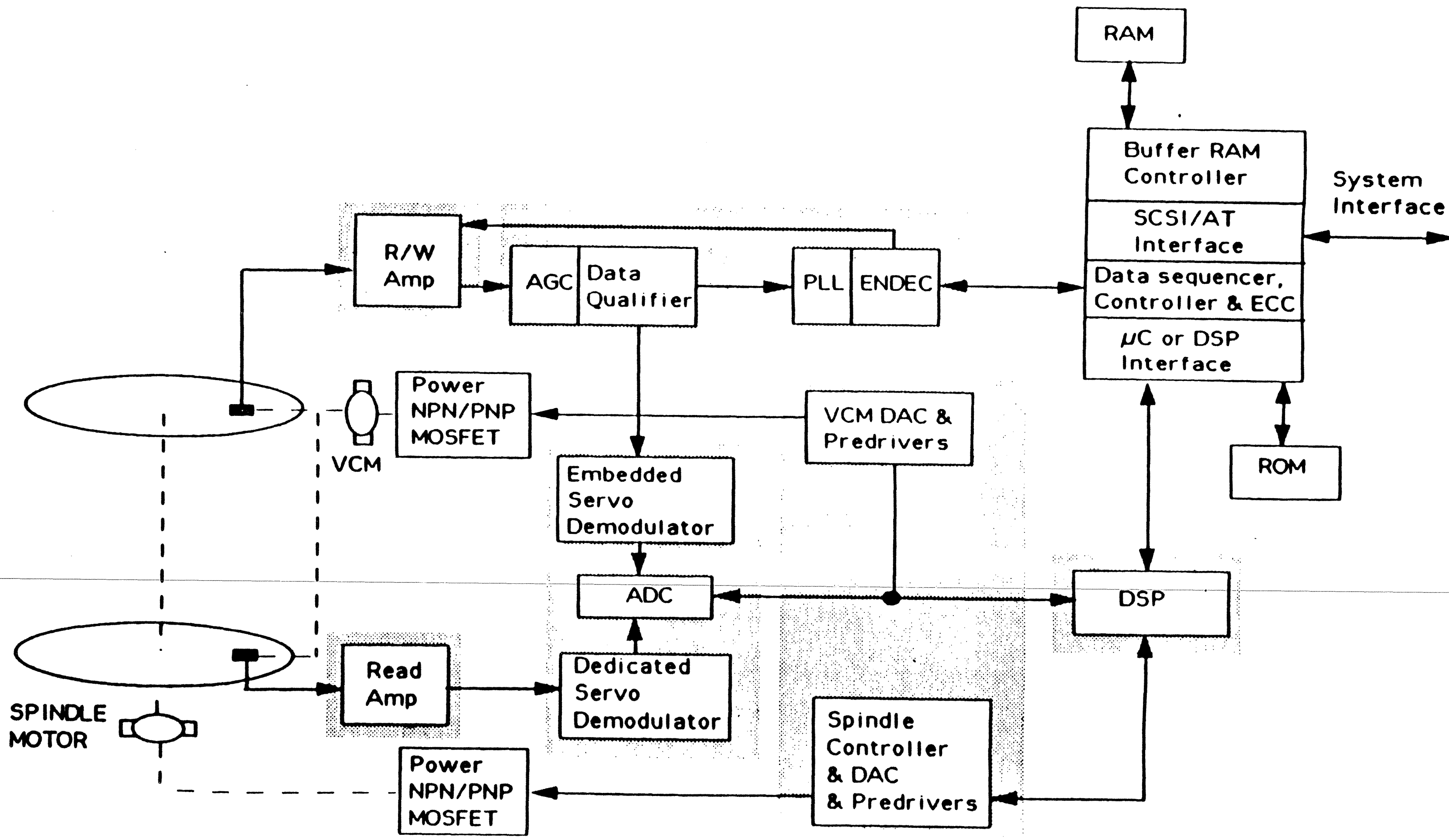
">4"

"LARGE" DRIVE:

system requirements

- Power control of VCM/Spindle Motors
- For increasing capacity
  - An increase in T.P.I.
  - An increase in data transfer rate
- Dedicated/Hybrid servo.
- Reduced access time requires adaptive servo control.
- More measurement of system parameters required.
- More control of system parameters.
- Increased integration to reduce foot print.
- Reduced costs.

3.5" DRIVES — 'LARGE' CAPACITY

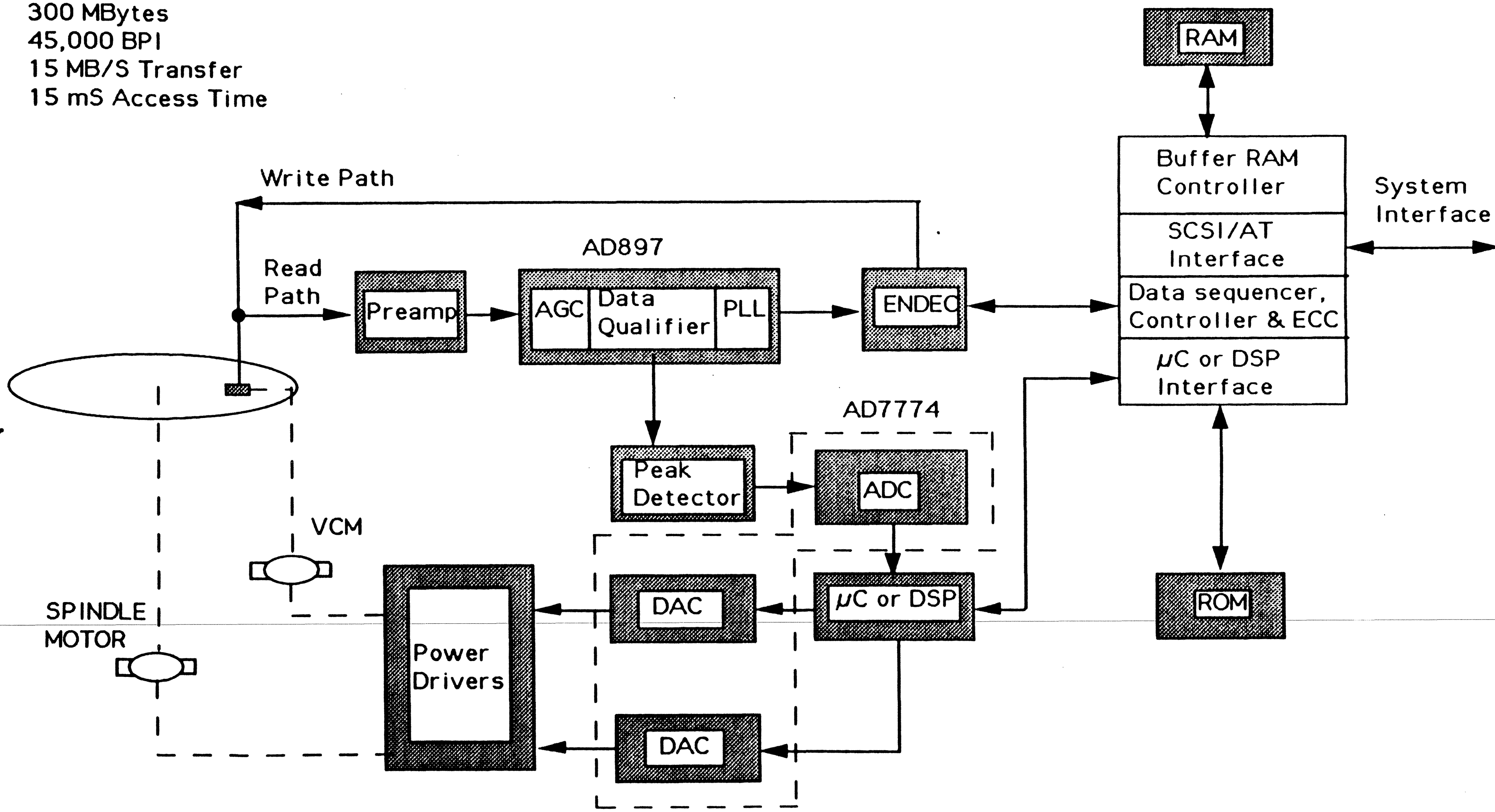


'LARGE' DRIVE: TECHNOLOGY REQUIREMENTS

- + 5V/+12v operation (+12 V to drive motors) $\pm$ 10%.
  10V to 13.2V
- Increased T.P.I.
  - More resolution on VCM control (> 10 bits).
  - More resolution on position sensing (> 8 bits).
- Maximise Channel S/N Ratio Use 'Bias' referenced signals.
- Dedicated/Hybrid servo control:
- Reduced Access Time
  - Faster through – put through servo demod. channel.
  - Faster ADC conversion time. equivalent.
  - Faster processing uP/DSP.
  - Adaptive control bandwidth; AGC, rectifier discharge rate..
- Fast interface speed for high speed uP's/DSP.
- Integration to give smaller foot print.
  - Multiple small pin count SMD's (SOIC).
  - Single large pin count SMD's (PQFP).
- Functional integration:

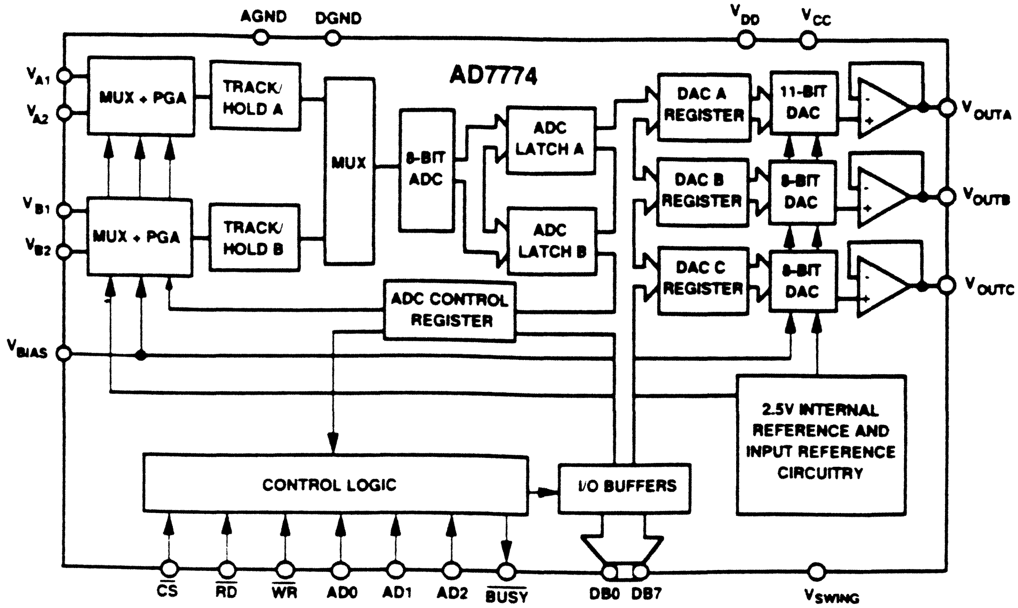
  Include power pre – drivers; loop control element; with VCM DAC.

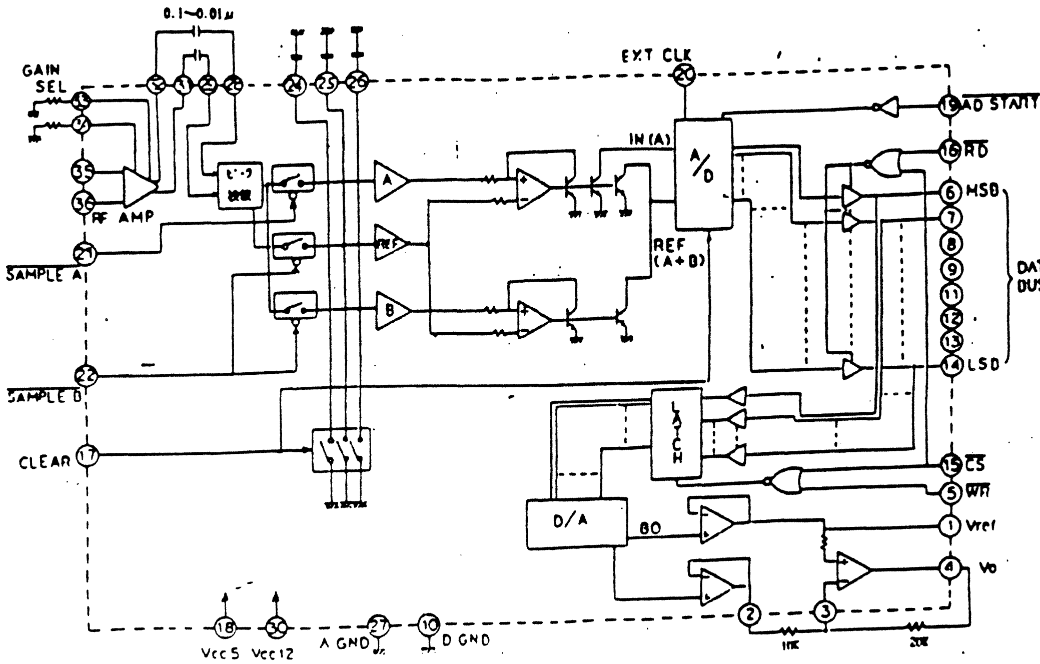
Typical 3.5"/5.25" Medium/High Performance HDD
300 MBytes
45,000 BPI
15 MB/S Transfer
15 mS Access Time



ANALOG DEVICES

AD7774 FUNCTIONAL BLOCK DIAGRAM





0.1~0.01μ
GAIN
SEL
RF AMP
SAMPLE A
SAMPLE B
CLEAR
A
REF
B
IN (A)
A/D
REF
(A+B)
EXT CLK
AD START
RD
MSB
LSB
DATA
BUS
CS
WR
Vref
Vo
LATCH
D/A
80
Vcc5
Vcc12
A GND
D GND

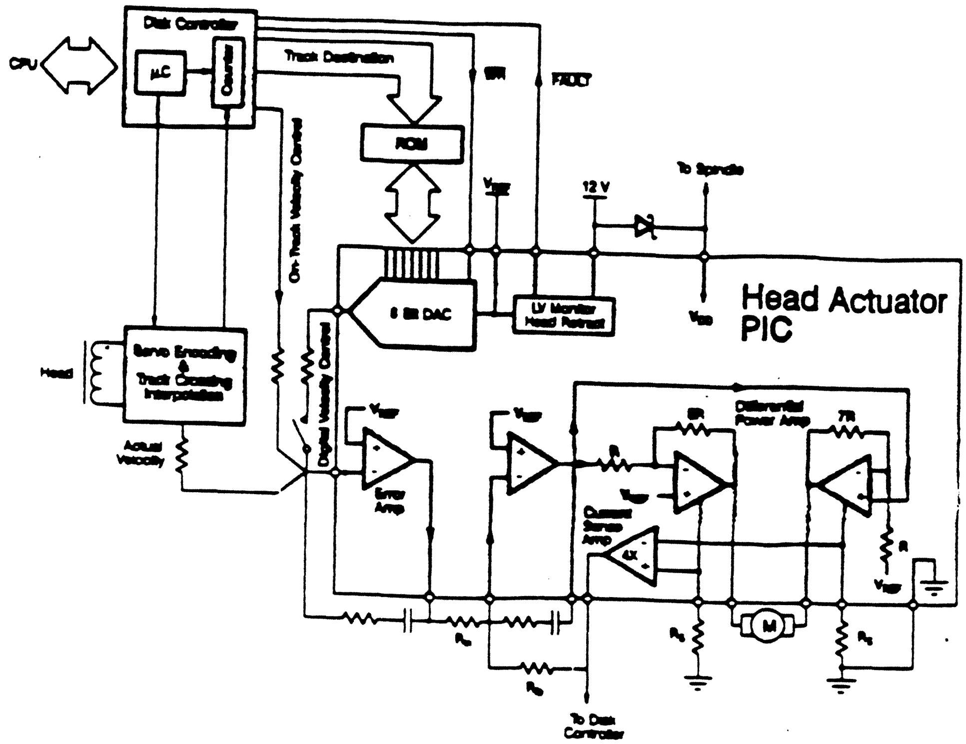
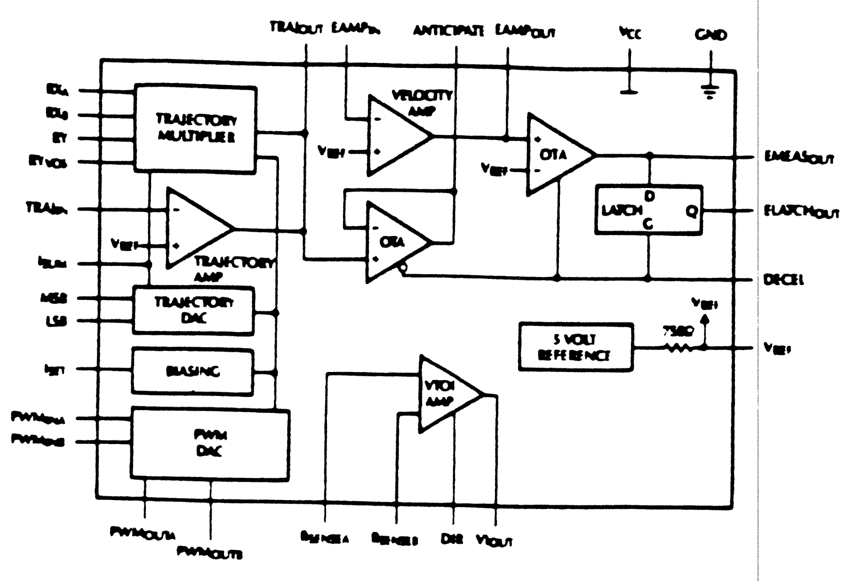


Fig. 1. HDD head-positioning servo system.



TRAJOUT
EAMPIN
ANTICIPATE
EAMPOUT
VCC
GND
TRAJECTORY MULTIPLIER
VELOCITY AMP
VREF
OTA
EMEASOUT
LATCH
D
Q
G
FLATCHOUT
TRAJIN
VREF
OTA
TRAJECTORY AMP
DECEL
MSB
LSB
TRAJECTORY DAC
VREF
5 VOLT REFERENCE
VREF
BIASING
VTOI AMP
PWM DAC
PWMOUTA
PWMOUTB
DIR
VIOUT

'SMALL' SIZE

S1

SYSTEM REQUIREMENTS:

- Reducing size 3 1/4 to 2 1/2 to 1.8".
- For increasing capacity to 80 mb.
  - an increase in T.P.I.
  - an increase in data transfer rate.
- Single platter.
- Power save mode for portable PC's (Laptop/notebooks).
- Low volume battery.
- Low – Low cost.

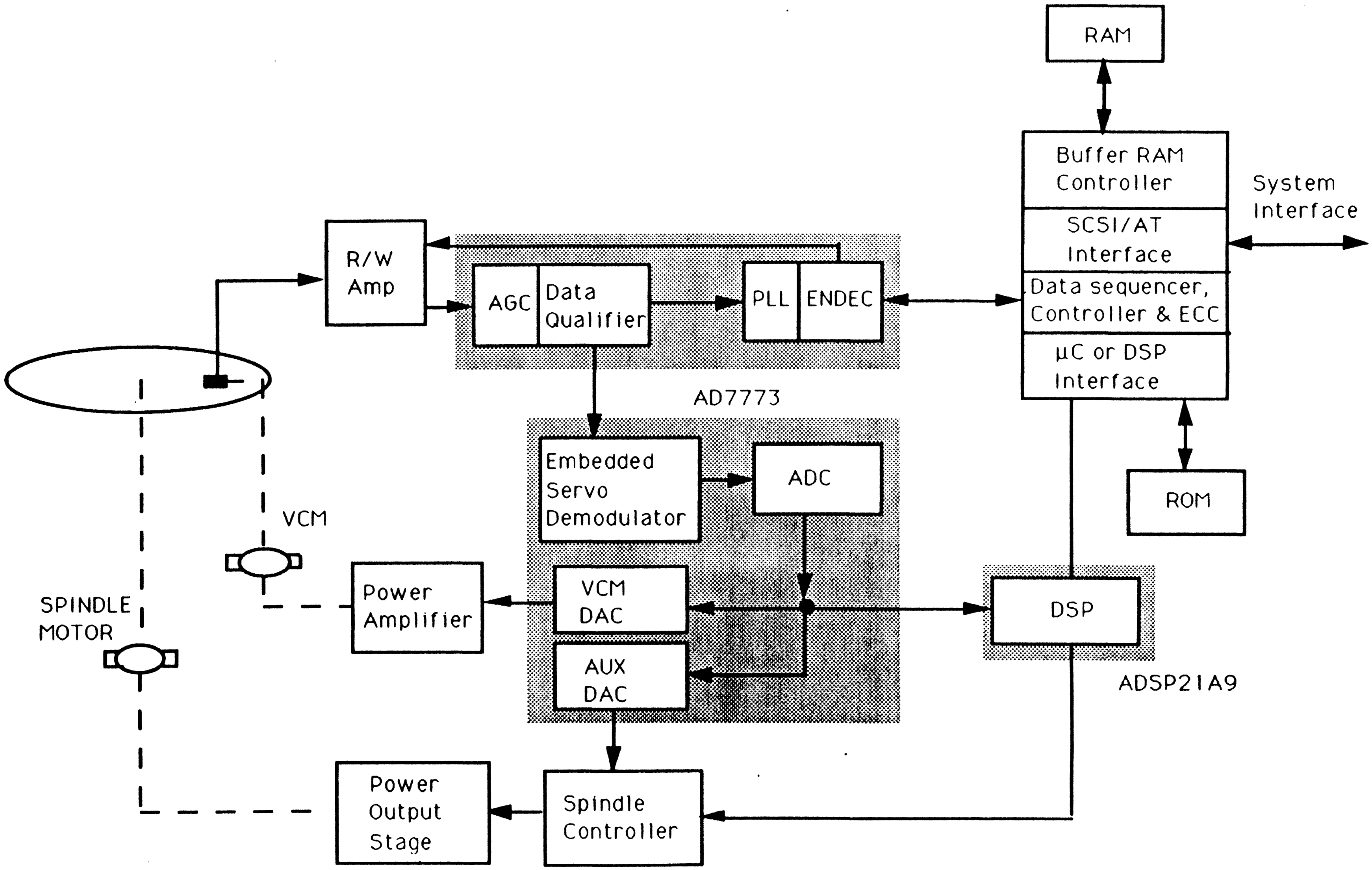
'SMALL' SIZE

Technology Requirements:

- For reduced size to < 1.8"
  - Component height reduction
  - Foot print reduction
- Embedded servo technique – single platter.
- Increased capacity by BPI/TPI increase, requiring more bandwidth/resolution (> 10 bits).
- Power save requires power down mode to < 1% normal.
- Minimize normal power drain to maximize life of fixed size battery.
- 5V only operation reducing to 3V $\pm$ 10%.
- Fast Interface speed for high speed uP's/DSP.
- Integration of additional functions.
  - Power drivers/devices and control circuits for VCM.
  - Servo demodulation spindle control functions.
- SMD packaging SOIC/PQFP for small foot print.
- TSOP/TPQFP for low (thin) packages.

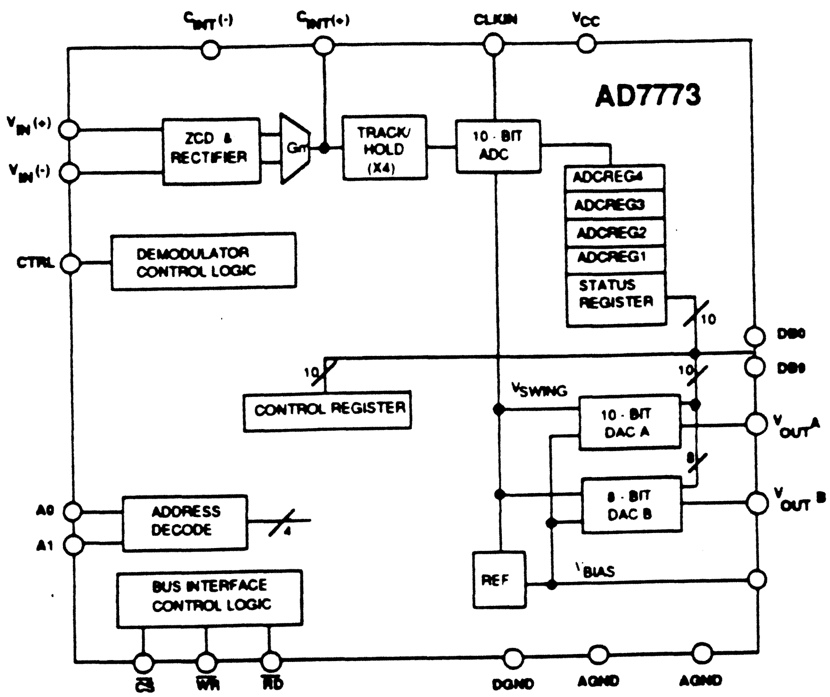
Complete embedded servo front end for HDD

Demodulator channel block diagram



DEC '91 16-Nov-91

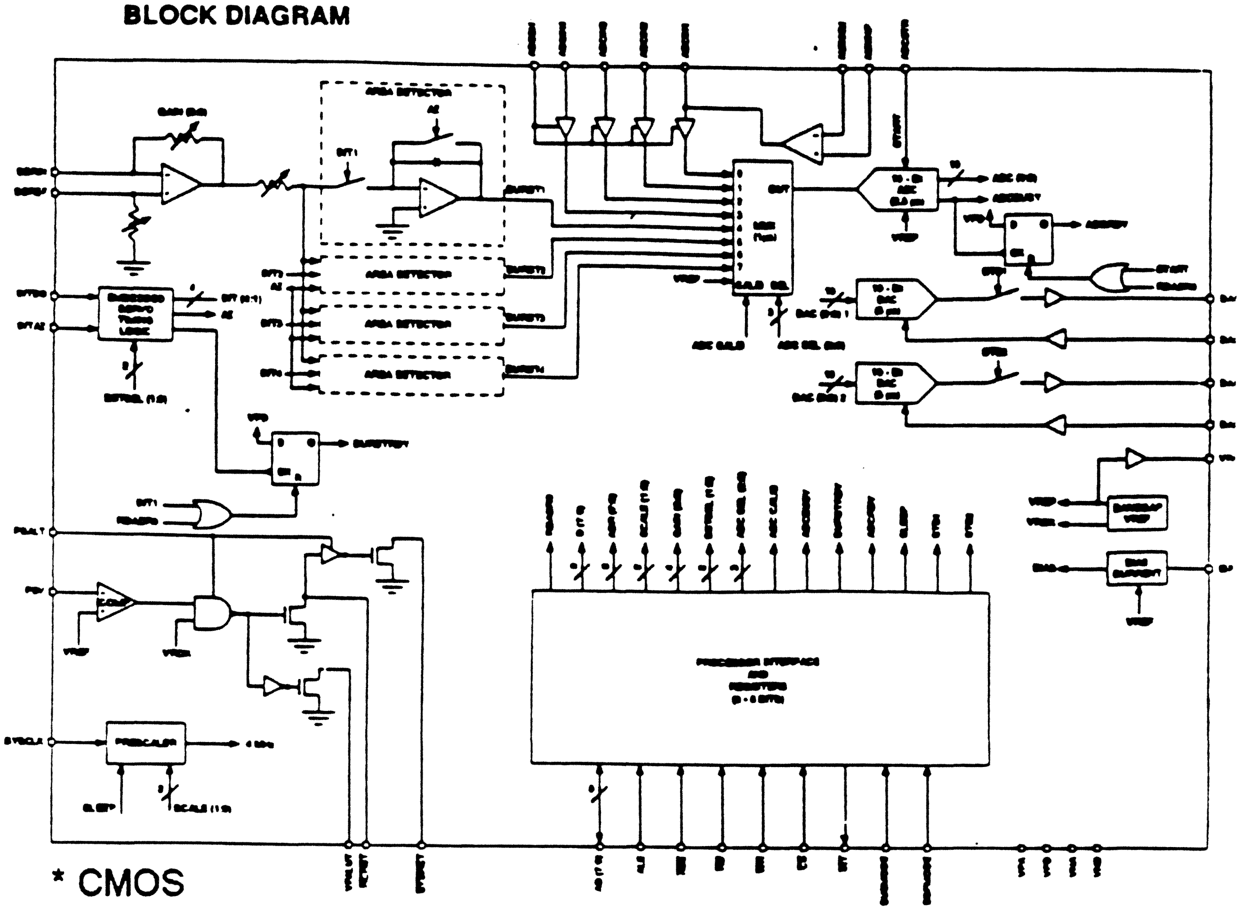
Complete embedded servo front end for HDD



DEC '91 16-Nov-91

- Embedded Servo Demod.
- BICMOS Technology
- 10 Bit Resolution DAC (VCM) + ADC
- Area detect for increased noise immunity
- 'MOTEL' Interface
- 5V operation + 10%
- Power Down option
- On chip ref.
- Gated/Signal Sync'd mode (ZCD)
- Additional 8 bit DAC – for spindle control
- 5MHz signal input allowed
- 2.1 uSEC conversion time per acquired burst.
- Software control # of bursts, # cycles/burst.
- 28 SOIC /32 pin TSOP

BLOCK DIAGRAM



* CMOS

* 5V + 5%

* 8 CH 10 bit ADC 2.5 uSEC.

* Two 10 bit DAC's

* Area Detection

* PGA, software control

* Gated control of integration

* # bursts software control

* Voltage fault detection

* On chip ref.

* Motel Interface

* 44 SOIC

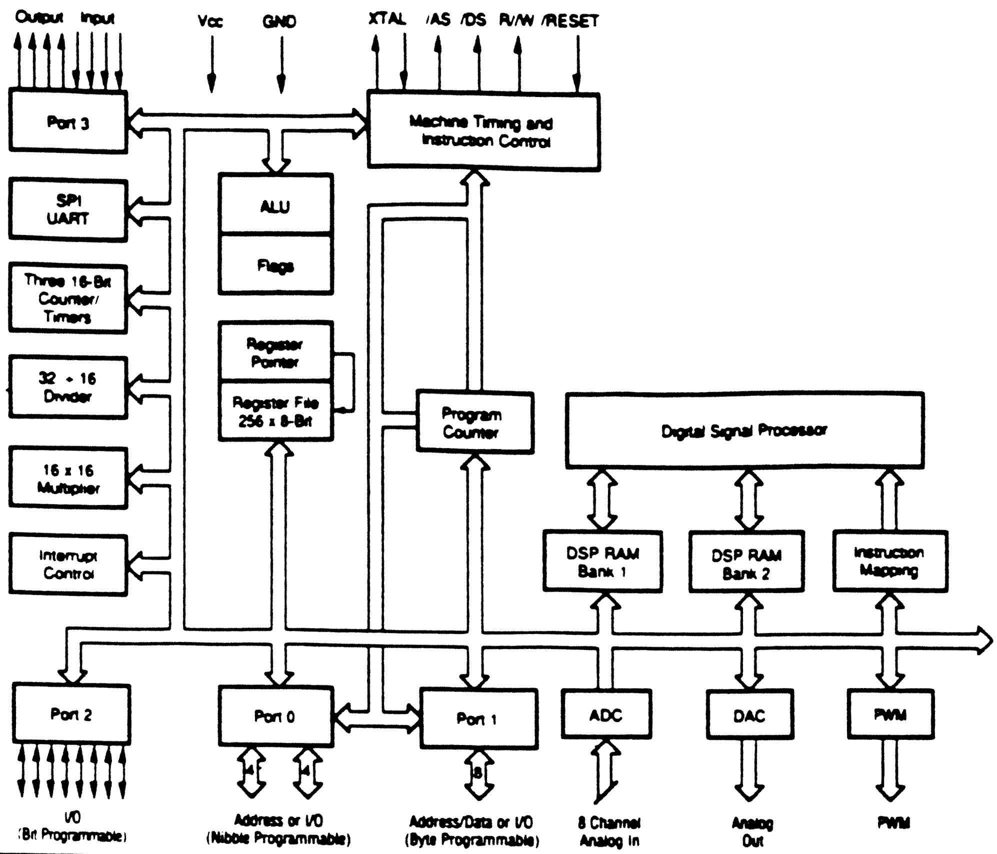
SMALL DRIVE

Further Integration : Options:

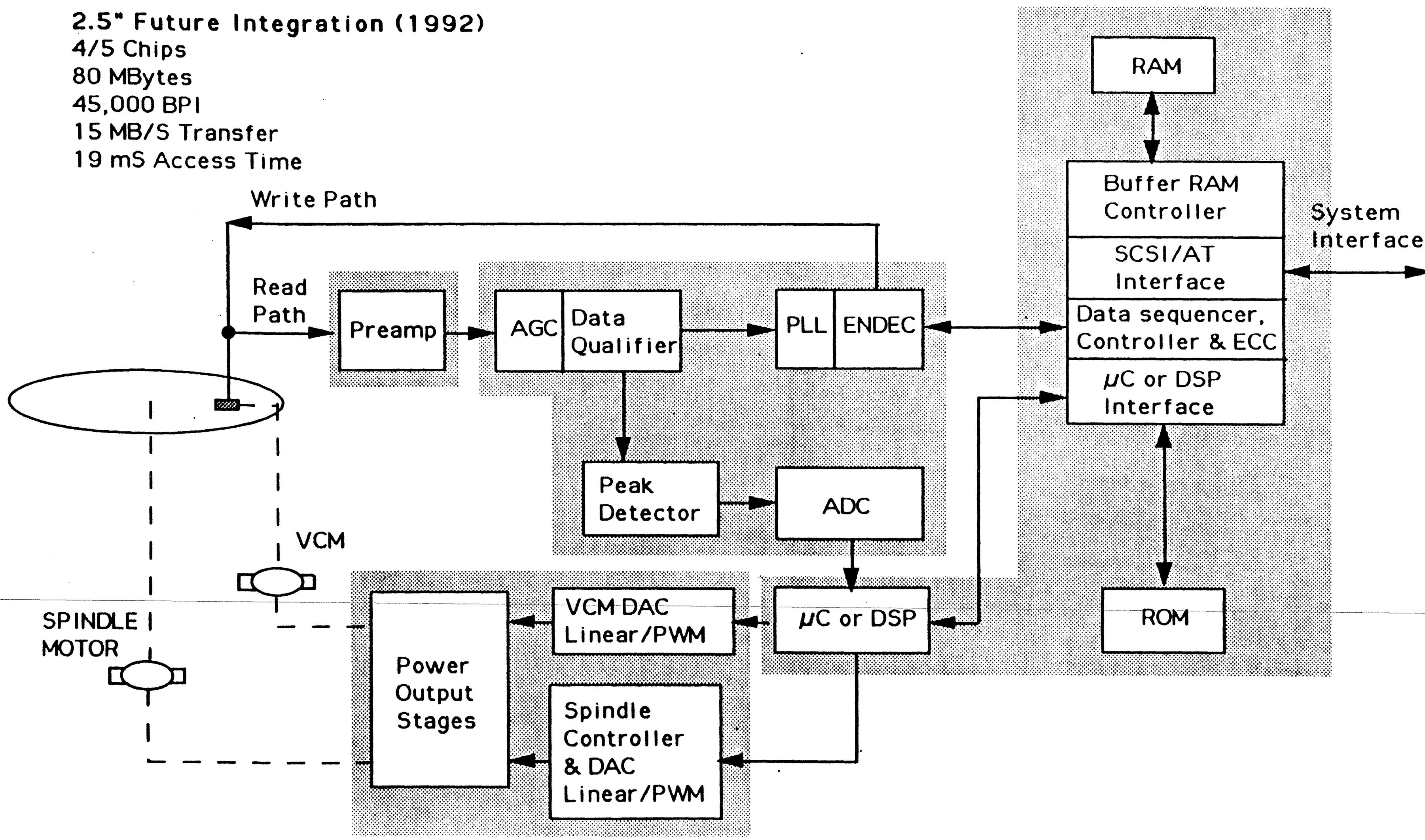
* Merge A/D and D/A function with DSP/uP — (1)

* Merge A/D & D/A function with
- VCM Power Control
- All Spindle Control Functions
- Programmable servo timing control

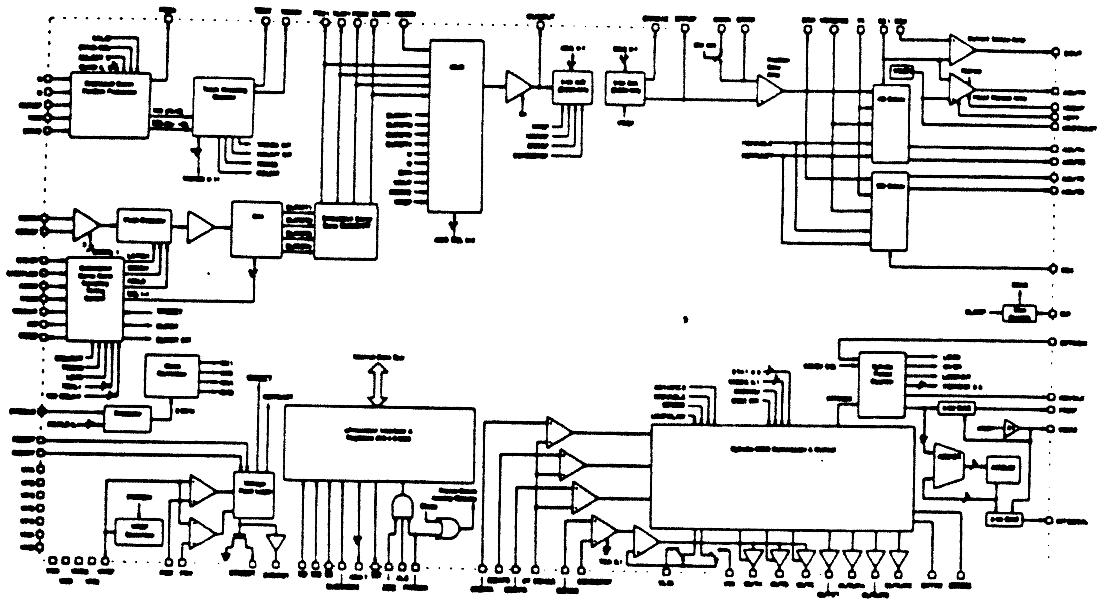
(Servo demod. merged with Read Channel — (2)


Output
Input
Vcc
GND
XTAL
/AS
/DS
R/W
/RESET
Port 3
Machine Timing and Instruction Control
SPI UART
ALU
Flags
Three 16-Bit Counter/ Timers
Register Pointer
Register File 256 x 8-Bit
32 ÷ 16 Divider
Program Counter
Digital Signal Processor
16 x 16 Multiplier
Interrupt Control
DSP RAM Bank 1
DSP RAM Bank 2
Instruction Mapping
Port 2
Port 0
Port 1
ADC
DAC
PWM
4
4
8
I/O
(Bit Programmable)
Address or I/O
(Nibble Programmable)
Address/Data or I/O
(Byte Programmable)
8 Channel
Analog In
Analog
Out
PWM

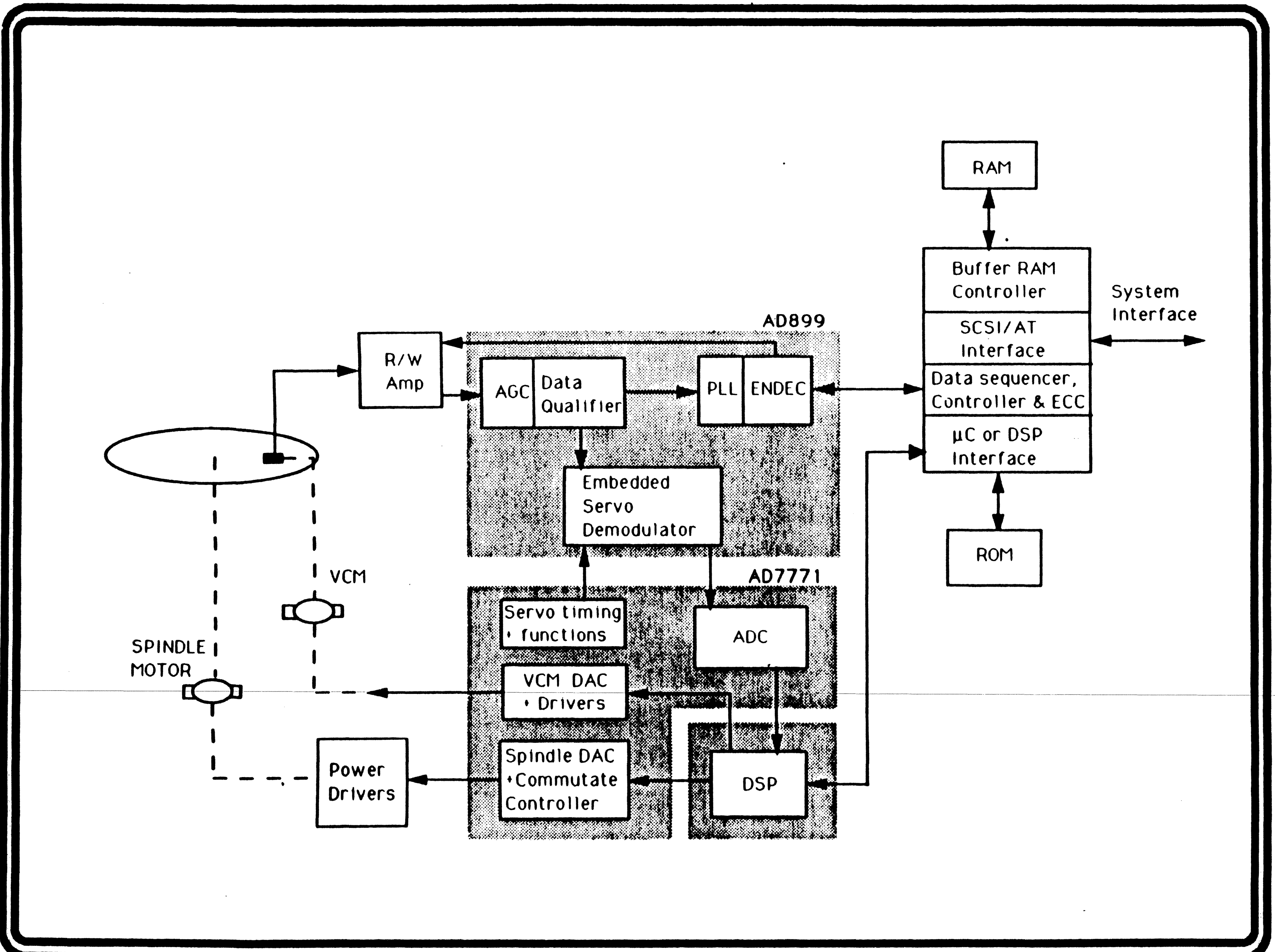
2.5" Future Integration (1992)
4/5 Chips
80 MBytes
45,000 BPI
15 MB/S Transfer
19 mS Access Time



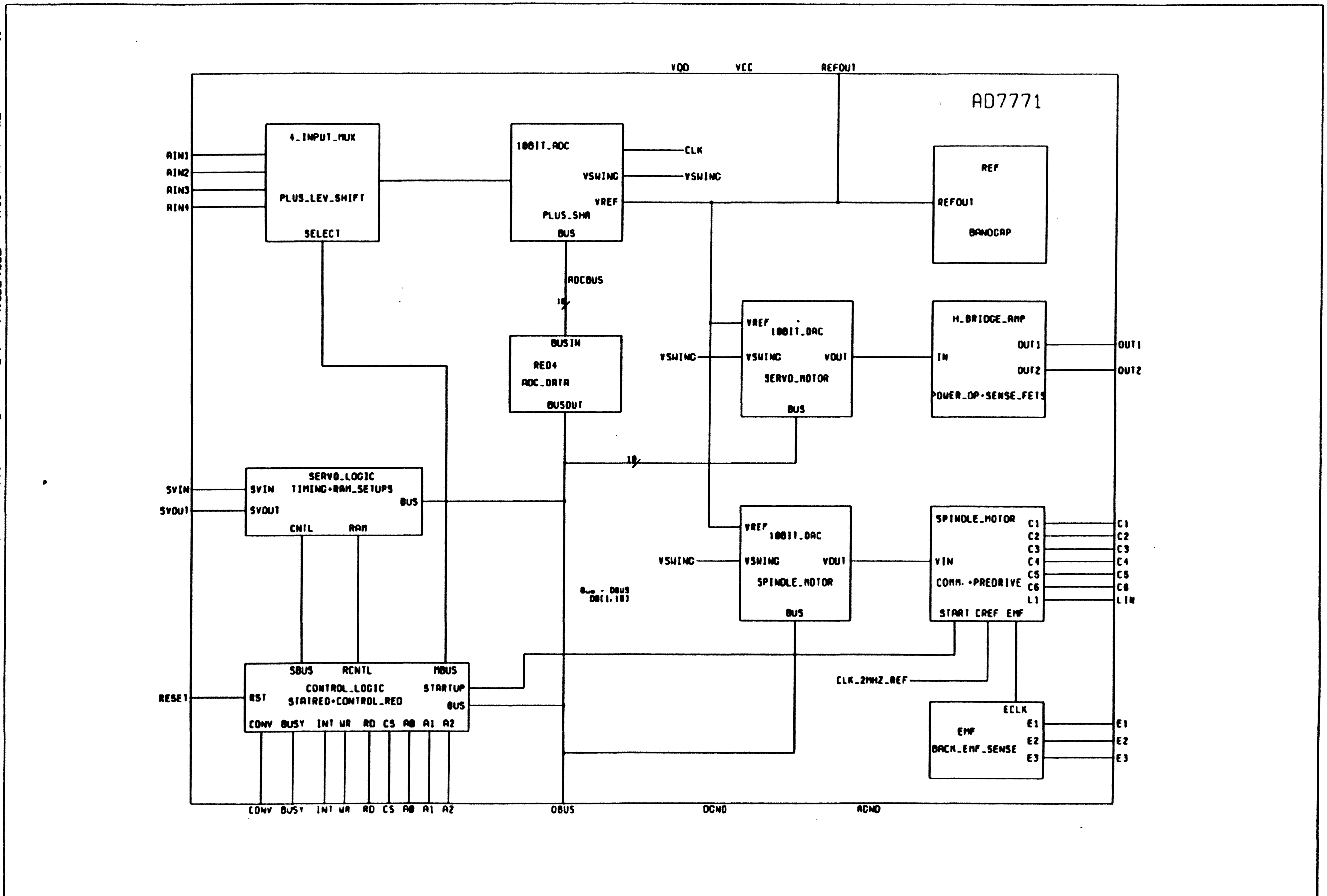
ANALOG DEVICES



BLOCK DIAGRAM
SSI 32H4631



RAM
Buffer RAM Controller
SCSI/AT Interface
Data sequencer, Controller & ECC
μC or DSP Interface
ROM
System Interface
AD899
R/W Amp
AGC
Data Qualifier
PLL
ENDEC
Embedded Servo Demodulator
AD7771
Servo timing + functions
ADC
VCM DAC + Drivers
Spindle DAC +Commutate Controller
DSP
Power Drivers
VCM
SPINDLE MOTOR



User: deevy, File: /usr/dsun39/deevy/7771/7771bd.cmd, Page: 1, Revised: 22/Nov/91 17:02, Plotted: 22/Nov/91 17:33

SMALL DRIVES

FUTURE:

- 3V Operation
- Smaller motors
- Lower power drive < 250 mA (included on chip)
- CMOS
- Single chip embedded servo?
- Semiconductor Memories!!

ADC FOR PRML CHANNEL

– TECHNOLOGY OPTIONS

PROPOSED ADC SPECIFICATION

Resolution:		6 Bits
Accuracy:	Target	5.8 ENOB EFFECTIVE NUMBER OF BITS
Sampling Rate:		72 MSPS
Error Rate:		10 E – 10
Input Bandwidth:		5.8 ENOB to 25 MHZ
		5.0 ENOB to 50 MHZ (1.4 NyQuist)
Input Signal Range:		1.5 Vpp differential
		+/– 375 mV about 2.5V
Input Capacitance		5 PF DIfferential

Jitter	< 40 PS
PSRR	< 30db at 30 MHZ
Assumed Driving Impedance:	100 ohms
Power Supply:	5V ± 10%
Power Dissipation	200 mW total
	100 mW for comparators
Temperature Range	0° to 70° C Ambient
	0° to 125° C Junction Temp.
Package	Surface Mount: (SOIC/PQFP)

2

KEY COMPARATOR SPEC'S DEDUCED FROM ADC SPEC

- Error Rate (ER).
- Input signal bandwidth (B.W.).
- Power dissipation (per comparator) (P.D.).
- L.S.B. size/input signal range.

p5

COMPARATOR EVALUATION

- Bipolar, CMOS, BICMOS circuits studied.
- Relationships between technology/P.d/ER/BW established.

BIPOLAR RESULTS:

- > 5 GHZ devices will meet 72 msps rate.
- Power dissipation is marginal.
- Dynamic range good.
- > 100 MHZ input bandwidth possible.
- Good tolerance of temp/supply variations.
- Major problem with ECL to CMOS/TTL conversion.
- Can be extended to higher resolution.

CMOS RESULTS:

- Technology $\leqslant$ 1u meets 72 Msps rate.
  (No auto zero cycle).
- Power dissipation just O.K.
- Marginal on input bandwidth, sharp break – off.
- Concern on dynamic range, comparator offset.
- Solves the level shift problem.
- More sensitive to temp/supply variations than bipolar.

BICMOS:

- Needs $\leq$ 1u CMOS Technology.
- Needs good bipolar device $\geq$ 5GHz.
- Meets power requirements.
- Input bandwidth to > 100 MHZ possible.
- Dynamic range O.K., due to low offset.
- Good tolerance to supply/temp variations.
- Possible to increase resolutions.

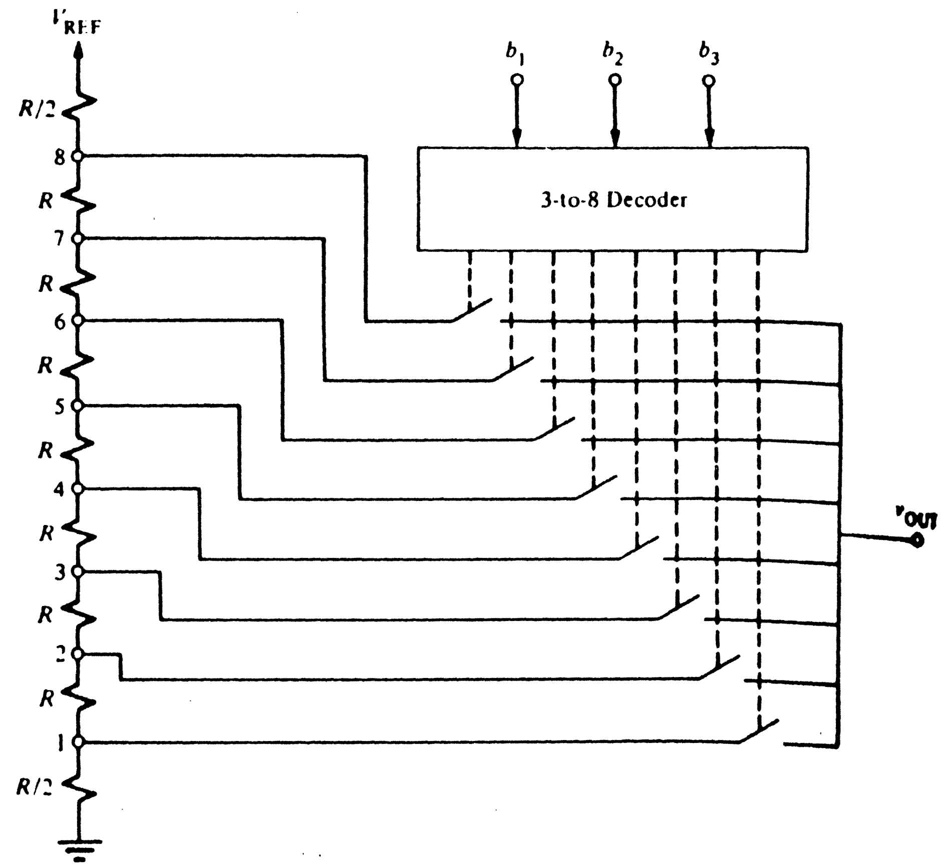
— Best Choice for Target Spec.

DAC's FOR SMALL DRIVES OPERATING AT 3V.

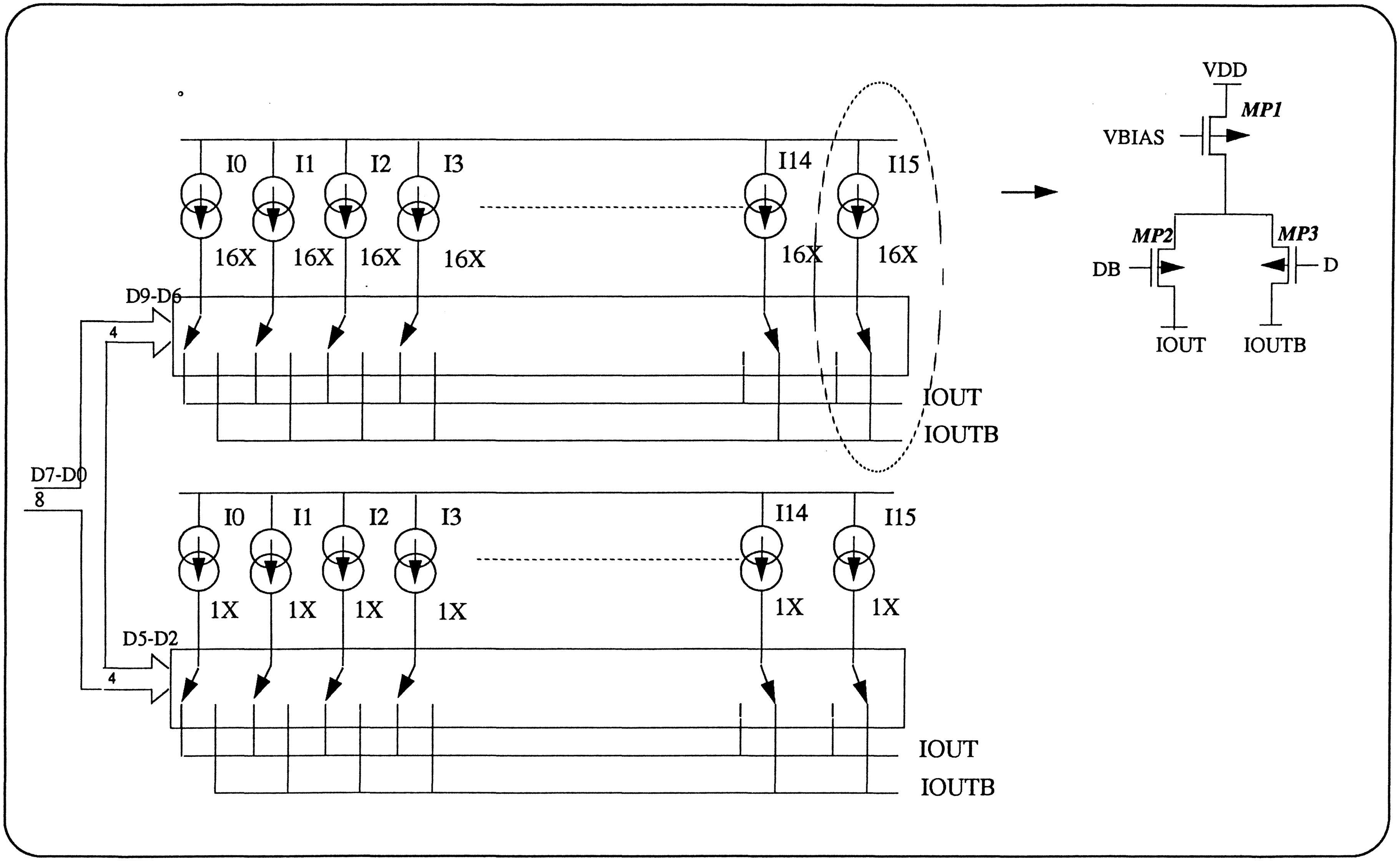
- What's the best architecture?
- Assume Fine Line CMOS technology:
  - (a) String Dac:
    - 2^N Switches (256/1024)
    - Poly Resistor string
    - Guaranteed monotonic to resolution
    - 7/8 bits accurate
    - Vout range; 0 to Vref
    - Static output
    - Needs high impedance load
    - Not very fast

10.2.2.

8



C



VDD
MP1
VBIAS
MP2
MP3
DB
D
IOUT
IOUTB
I0
I1
I2
I3
I14
I15
16X
D9-D6
4
D7-D0
8
D5-D2
1X
IOUT
IOUTB
IOUT
IOUTB

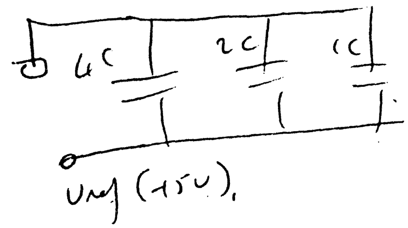
(b) – <u>Current Source DAC</u>
(e.g. RAM DAC)

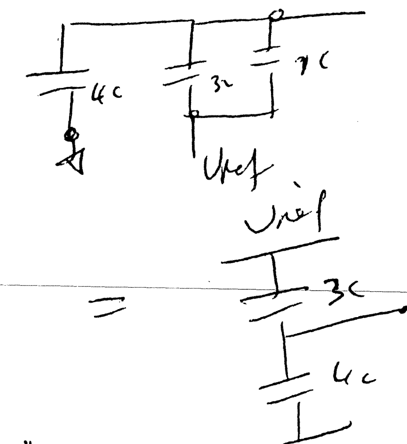
- Can be very fast
- Limited voltage output range (0 – 1.5V).
- 10 bits monotonicity possible
- 8/9 bits accurate
- Static output
- Could be calibrated.

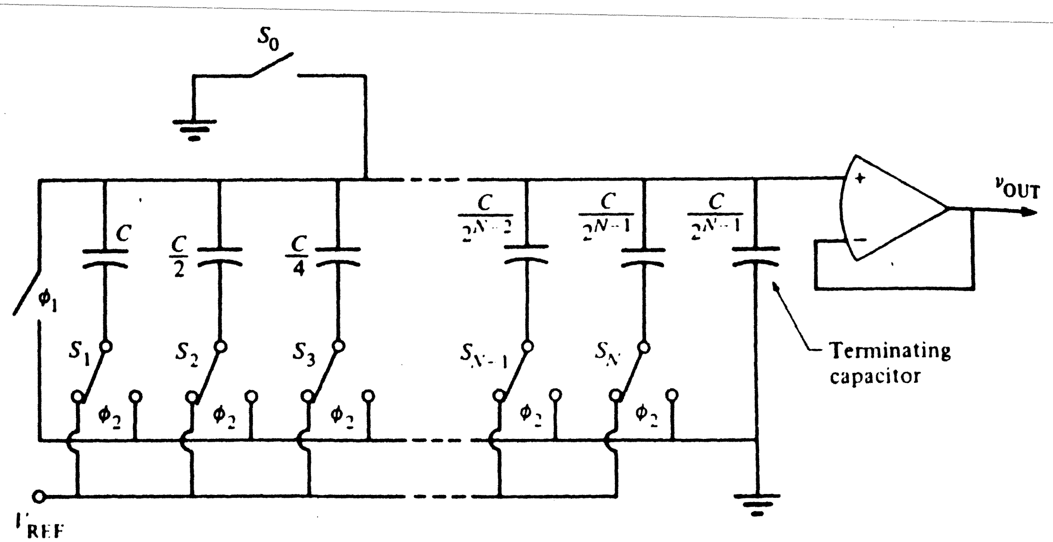
(c) <u>Switch Cap DAC</u>

- C – 2C architecture or variations there of
- Dynamic output for fixed input code
- Needs post filtering
- Needs poly – poly caps. for 10 bits monotonicity
- Could be calibrated.

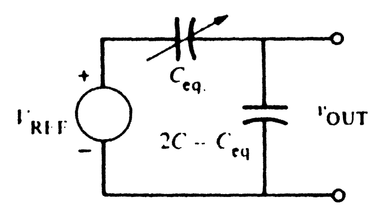
3 bit DAC


4C
2C
1C
Vref (+5V).


4C
3C
1C
Vref
Vref
3C
4C

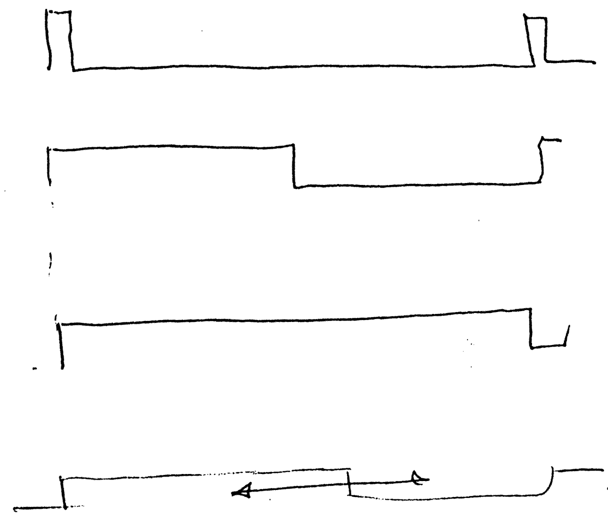

S_0
C
$\frac{C}{2}$
$\frac{C}{4}$
$\frac{C}{2^{N-2}}$
$\frac{C}{2^{N-1}}$
$\frac{C}{2^{N-1}}$
v_{OUT}
ϕ_1
S_1
S_2
S_3
S_{N-1}
S_N
ϕ_2
Terminating capacitor
V_{REF}

(a)


C_{eq}
V_{REF}
$2C - C_{eq}$
v_{OUT}

G

(d) (P.W.M) DAC

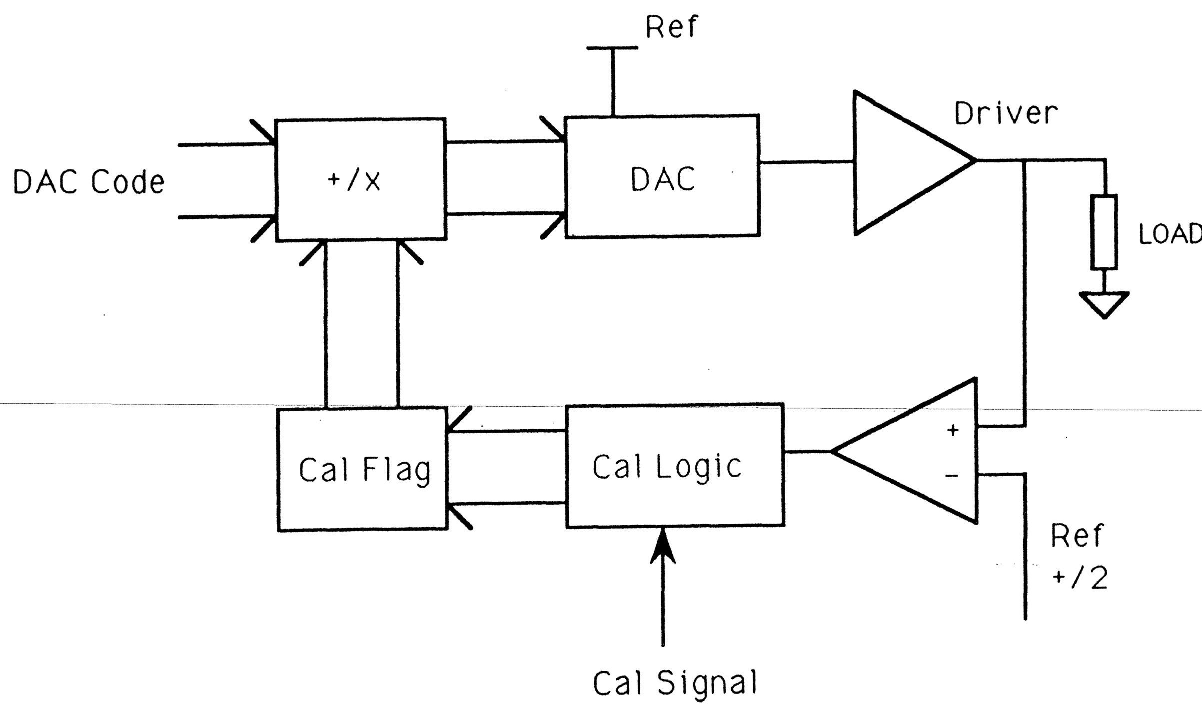


- 10 bits in 100uSEC possible
- Dynamic output
- Needs post filtering
- Small size.

H

- Choice of architecture should consider complete function not just D/A function i.e. follow on amplifiers; power drivers etc..
- Adjustment required to zero – out accumulated offsets in the DAC/Driver chain.
  - Use Calibration

But when can we calibrate??



I

ADC'S for Small Drives operating at 3V

- What's the best architecture?
- Assume fine line CMOS Technology

(a) SAR Technique:

- Efficient in area
- Low Power Consumption
- Limited in conversion speed
  (1 uSEC at 8 bits, 3 uSEC at 10 bits)
- Use string DAC/Switch Cap. DAC/ Current Source DAC.
- Sampled data comparator design
- 9 bits no missed codes possible
- 7/8 bits accurate
- Could be calibrated.

SUCCESSIVE APPROXIMATION A/D CONVERTER ENCODER

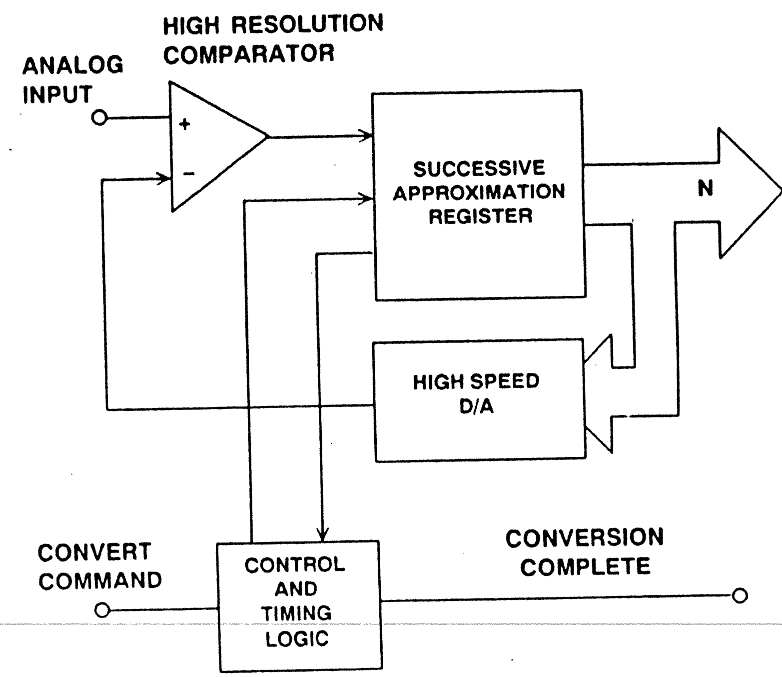
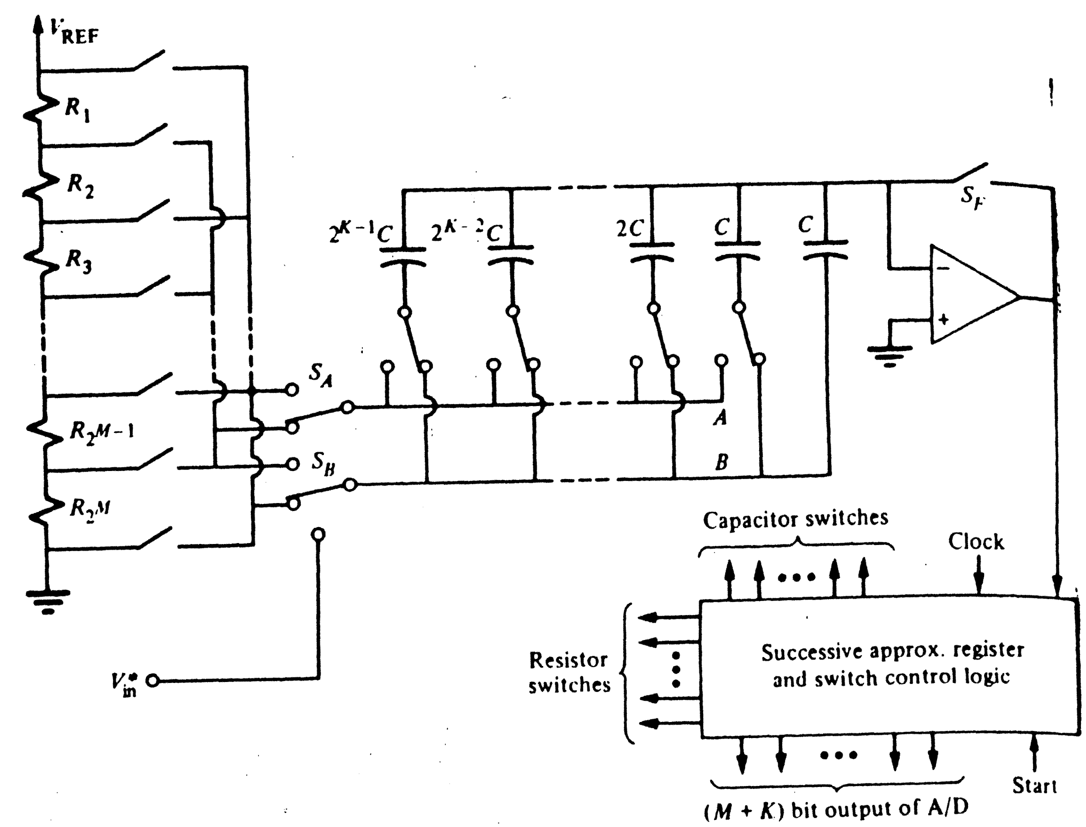


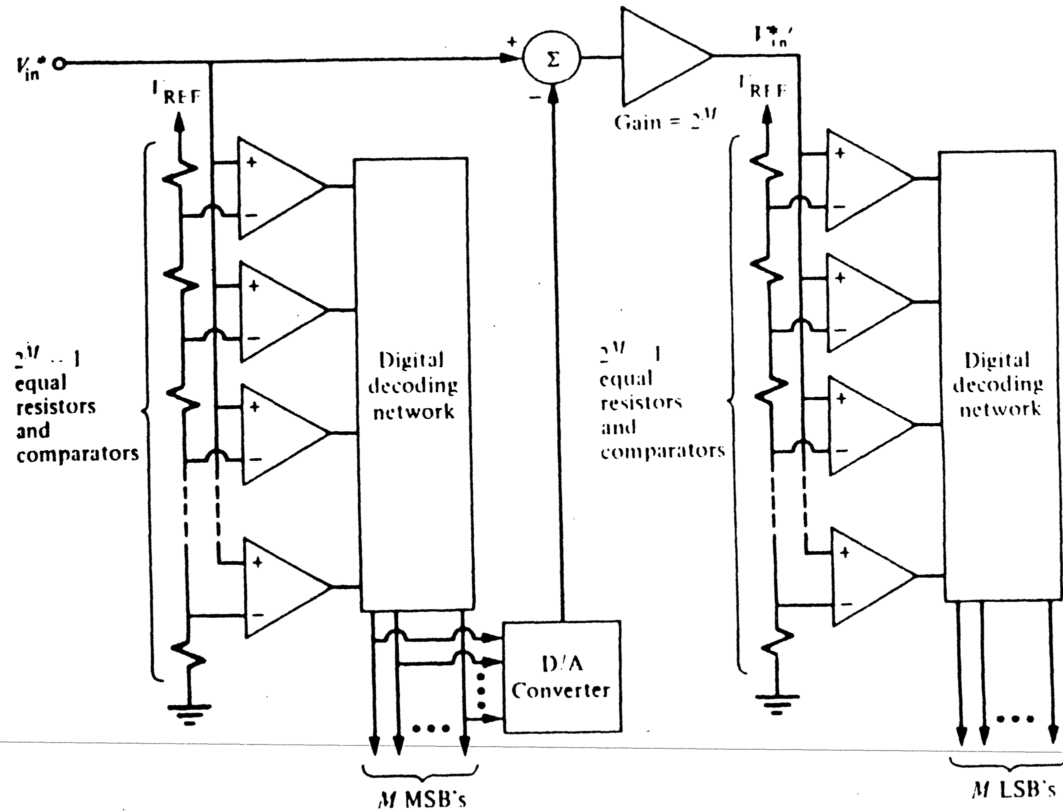
Figure 4.2

10.6.4. K



V_{REF}
R_1
R_2
R_3
R_{2^M-1}
R_{2^M}
S_A
S_B
V_{in}^*
$2^{K-1}C$
$2^{K-2}C$
$2C$
C
C
S_F
A
B
Capacitor switches
Clock
Resistor switches
Successive approx. register and switch control logic
Start
$(M + K)$ bit output of A/D

10.4.3.



V_{in}
V_{REF}
Σ
Gain = 2^M
V_{in}'
V_{REF}
$2^M - 1$ equal resistors and comparators
Digital decoding network
D/A Converter
$2^M - 1$ equal resistors and comparators
Digital decoding network
M MSB's
M LSB's

M.

(b) Flash – Flash technique:

- Achieves faster conversion time (200/400 nSEC).
- Greater power consumption
- Larger in area
- 8 bits (4 + 4)/10 bits (5 + 5) resolution
- 7/8 bits accurate
- Sensitive to noise.

N

N-BIT FLASH CONVERTER

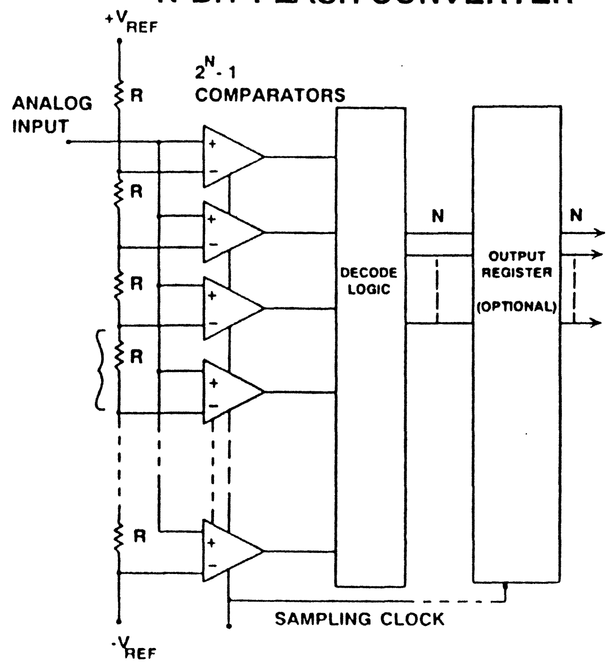
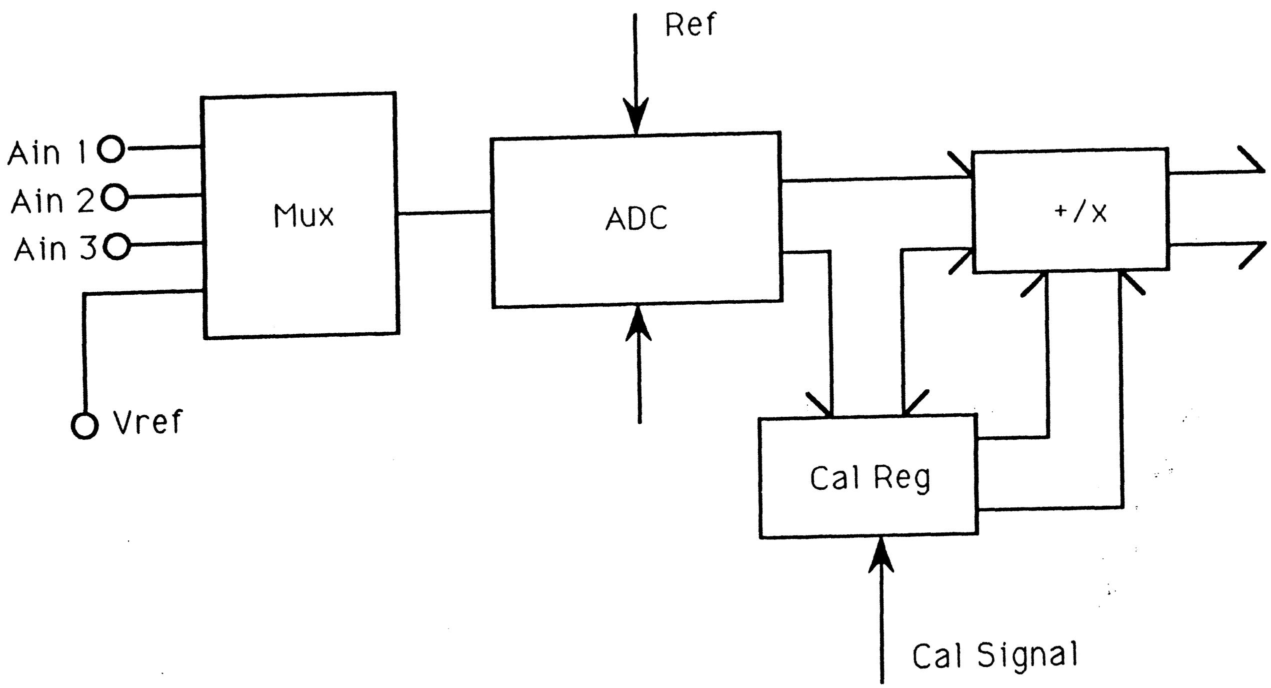


Figure 4.4

- Choice of architecture should consider complete function not just the A/D function, i.e. pre conditioning stages etc..
- With small signal span offsets become a problem.
    - Use calibration
  - when can we calibrate?



(c) Full Flash Technique:

- Very fast (50/100 nSEC)
- Power consumer
- large in area
- 8 bit resolution upper limit due to size
- Sensitive to noise

MAGNETIC CHANNEL CHARACTERISTICS

EDGAR M. WILLIAMS
READ-RITE CORPORATION

- ○ Recorded Magnetization Patterns
- ○ Zig-Zag Transitions in Thin Films
- ○ Mathematical Approximations of Transitions
- ○ Estimation of the Transition Parameter
- ○ Write Field Gradient Limits on Transitions
- ○ Writing at High Transition Densities
- ○ Time-Domain Asymmetry and Overwrite
- ○ Readback Pulses and Transition Shape
- ○ Readback Pulse Shape and Head Geometry
- ○ Pulse Interference and Amplitude Spectra
- ○ Pulse Shape Influence on Complex Data Patterns
- ○ Pulse Shape Influence on Peak Shift
- ○ Head and Medium Noises
- ○ Influence of Noise and Interference on Error Rate

IEEE TRANSACTIONS ON MAGNETICS, VOL. MAG-19, NO. 5, SEPTEMBER 1983

(p. 1600 – 1604)

OBSERVATION OF RECORDED MAGNETIZATION PATTERNS BY ELECTRON HOLOGRAPHY

K. Yoshida, T. Okuwaki, N. Osakabe, H. Tanabe
Y. Horiuchi, T. Matsuda, K. Shinagawa
A. Tonomura and H. Fujiwara.

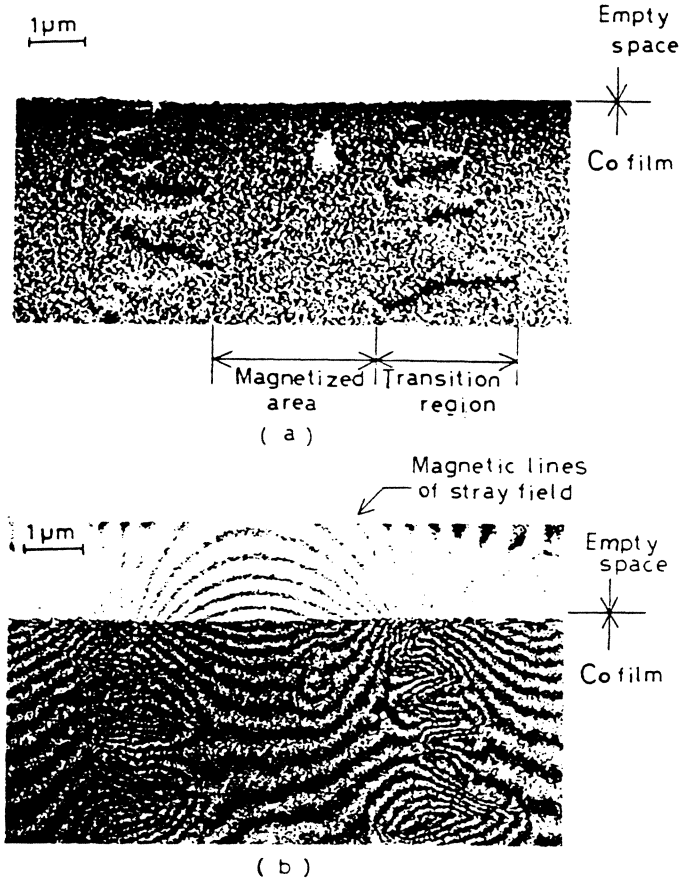


Fig. 5. Recorded magnetization pattern on a Co film (film thickness=45nm, coercivity=27kA/m, saturation induction=1.1T). A bit length is 5μm. (a) Lorentz micrograph. (b) Interference micrograph.

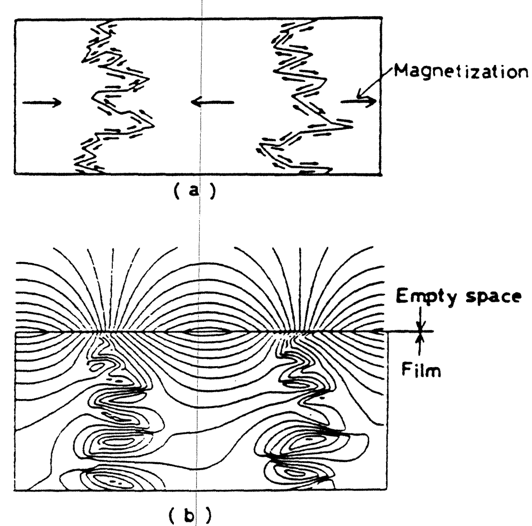
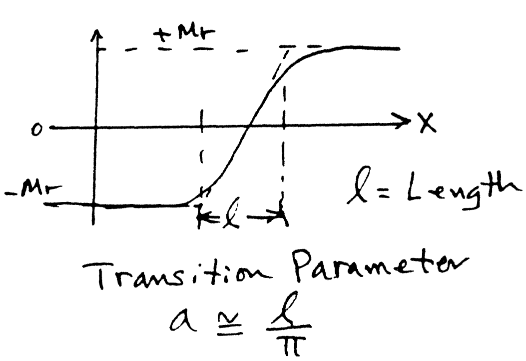


Fig. 6. Calculated interference image.
(a) Presumed magnetization distribution.
(b) Calculated interference image using the model of (a).



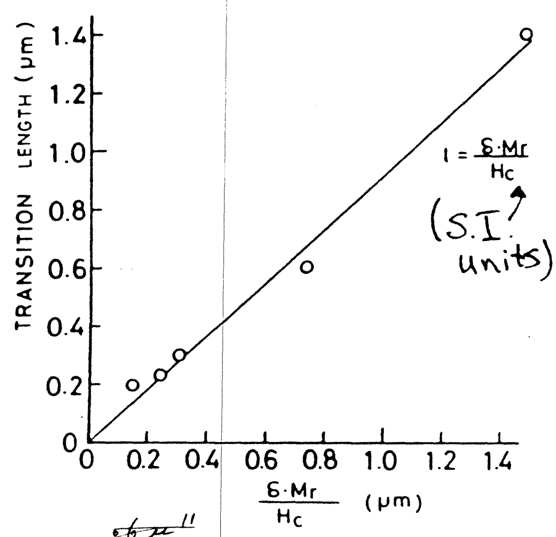


Fig. 7. Transition length as a function of $6M_r/H_c$.

IEEE TRANSACTIONS ON MAGNETICS, VOL. MAG-22, NO. 5, SEPTEMBER 1986 (p.889-891)

Zigzag Transition Profiles, Noise, and Correlation Statistics in Highly Oriented Longitudinal Film Media

by

T. C. Arnoldussen

H. C. Tong

International Business Machines Corporation
General Products Division
San Jose, California

Figure 1: Lorentz micrograph of 300 fr/mm track. Track direction is left to right.

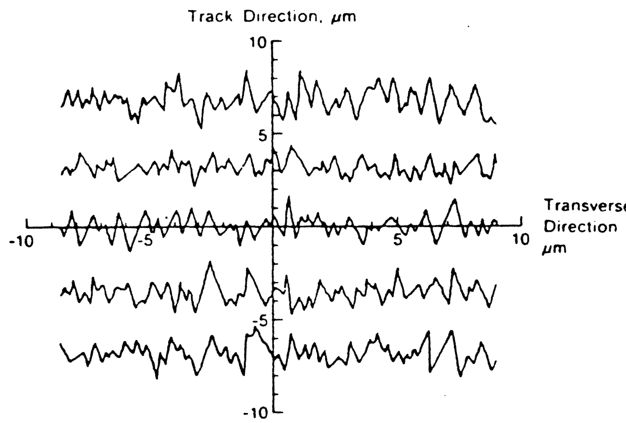


Figure 2: Digitized zigzags.

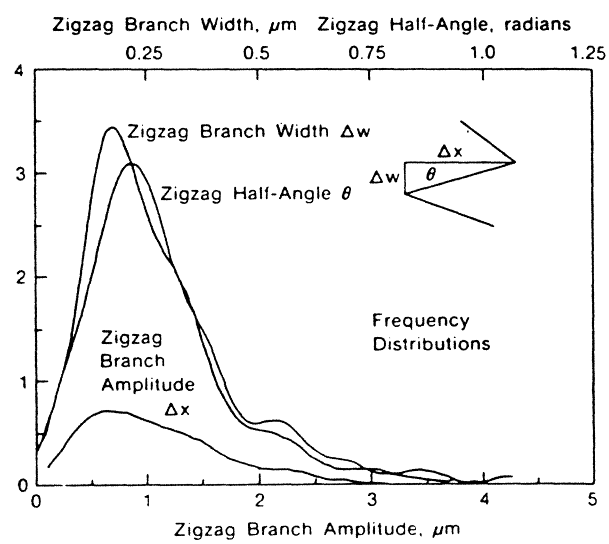


Figure 5: Zigzag dimensional distributions.

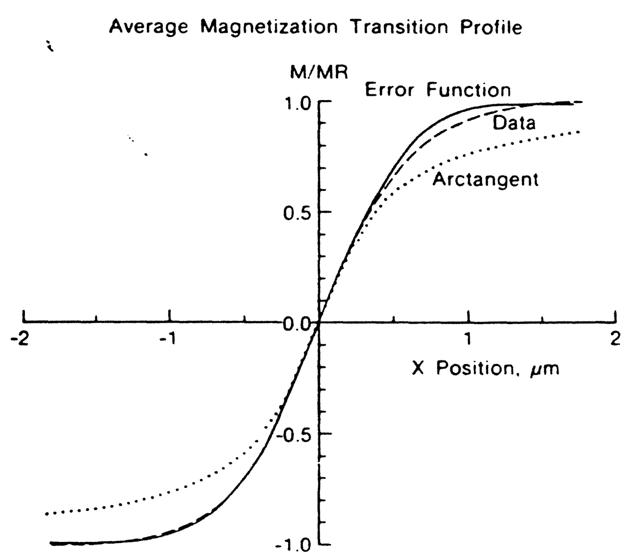
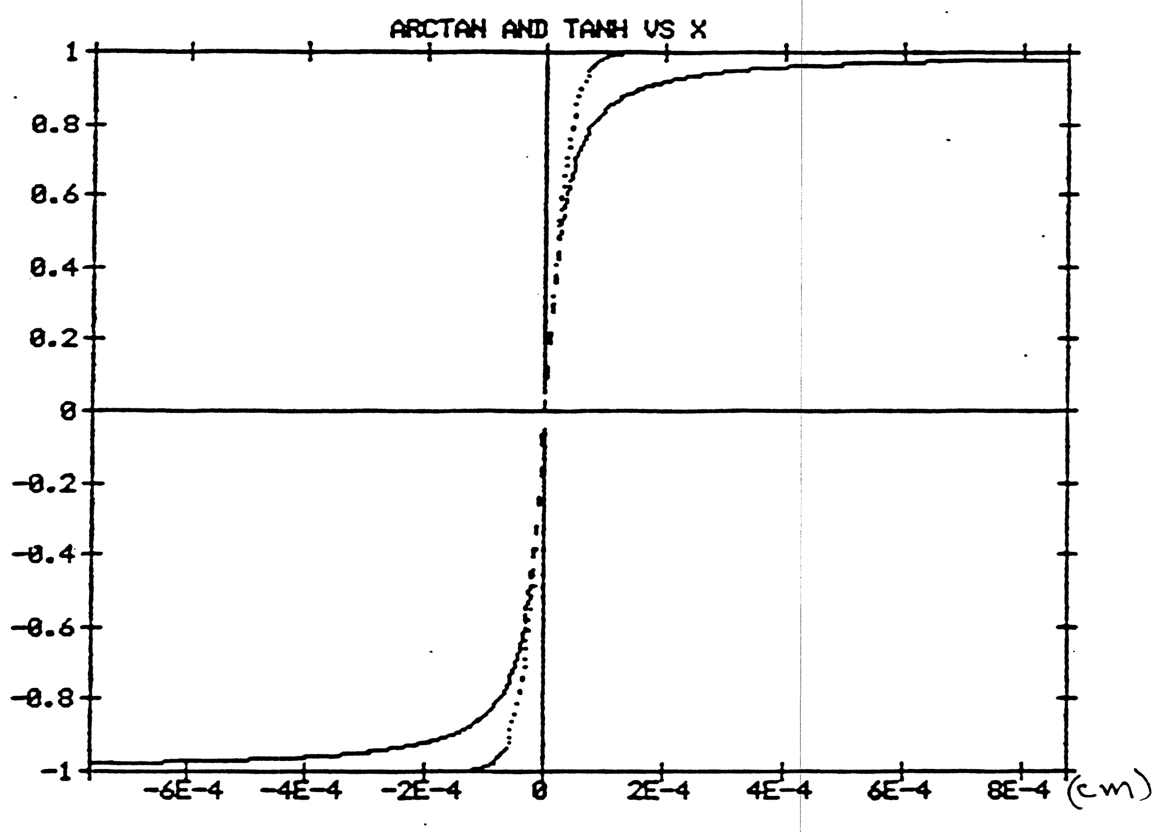


Figure 3: Composite magnetization transition profile.

ROS COMP CURVE USED TO MODEL

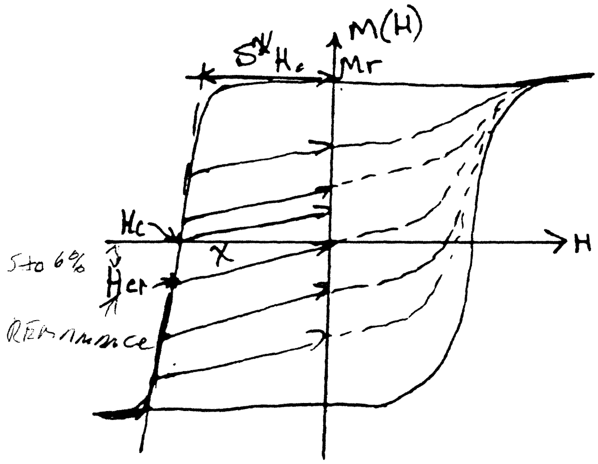


$a = 0.253\mu$

$\frac{2}{\pi} \tan^{-1}\left(\frac{x}{a}\right) \quad \& \quad \tanh\left(\frac{2x}{\pi a}\right)$

THE WRITTEN TRANSITION

Ref.: M.L. Williams & R.L. Comstock, PROC. A.I.P. Conf. on Magnetism & Magnetic Materials, 1971.



$$\left.\frac{dM}{dx}\right|_{x=0} = \frac{dM}{dH}\left(\frac{dH_h}{dx} + \left.\frac{dH_d}{dx}\right|_{H=H_{cr}}\right)$$

① $M(x) = \frac{2M_r}{\pi}\tan^{-1}\left(\frac{x}{a}\right)$

② Demagnetizing Field Gradient

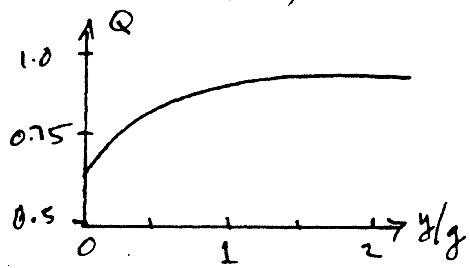
$$\left.\frac{dH_d}{dx}\right|_{H=H_{cr}} = -\frac{4M_r\delta}{a_1^2}$$

(δ = magnetic film thickness)

Intermediate Transition:

$$\frac{a_1}{r} = \frac{y(1-S^*)}{\pi Q} + \left\{\left[y(1-S^*)/\pi Q\right]^2 + (2M_r\delta/H_c)(2y/Qr)\right\}^{1/2}$$

$$r = 1 - \chi(1-S^*)H_c/M_r\,, \quad \chi = M_r/4H_c$$



Assumes $\frac{dH_h}{dx}$ is at maximum

$$\therefore \frac{dH_h}{dx} = Q\frac{H_c}{yr}$$

SPACING FROM GAP ℄

Final Transition:

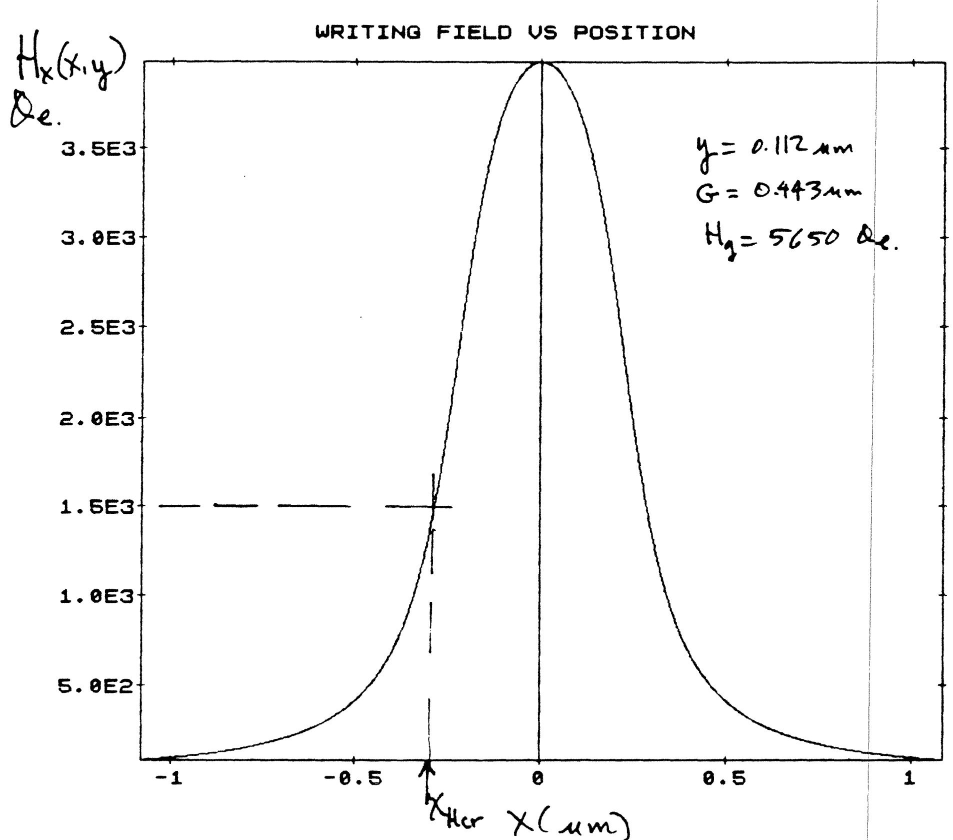
$$a_2 = \frac{a_1}{2r} + \left[(a_1/2r)^2 + 2\pi\chi\delta a_1/r\right]^{1/2}$$

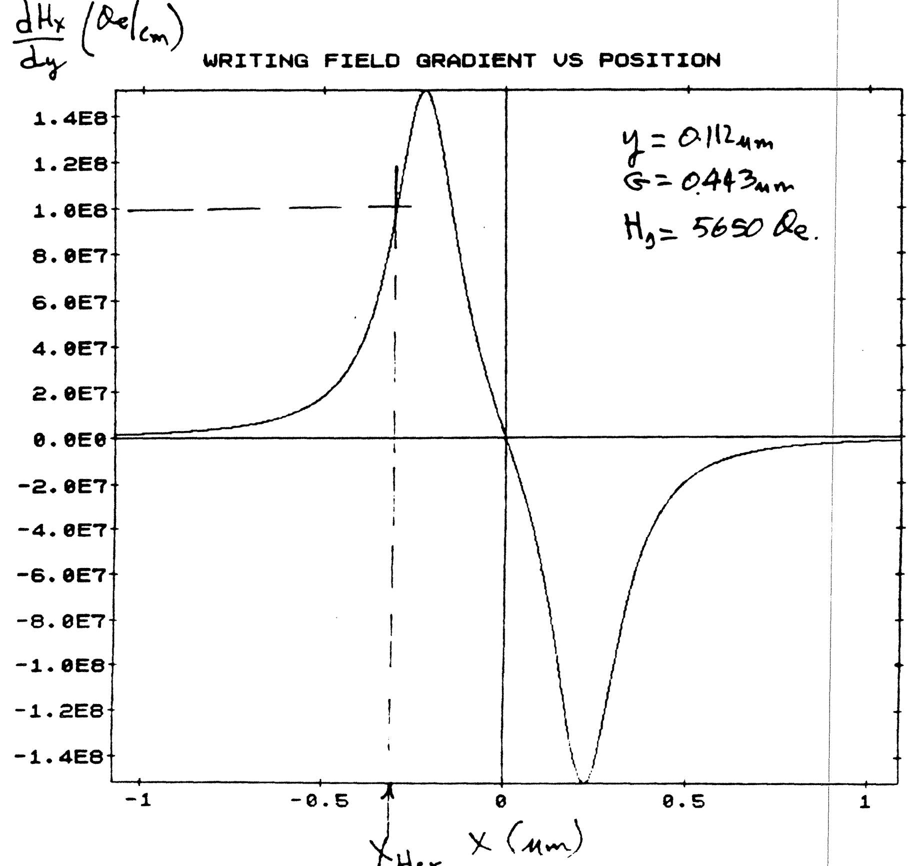
$a_2 > a_1$ (i.e. transition broadens after leaving write field)

Head-Limited Transition:

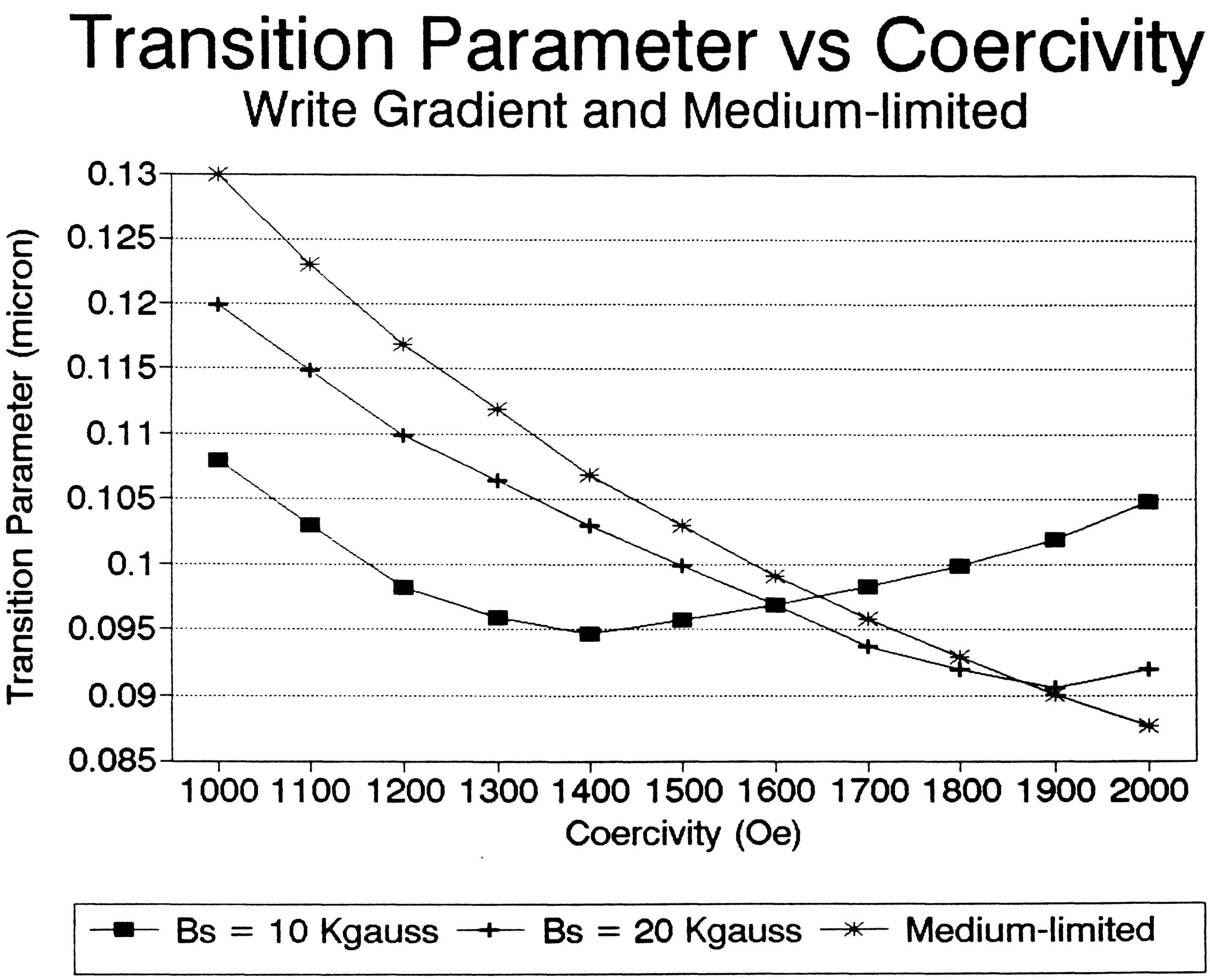
$$a_h = \frac{H_c}{\frac{dH_h}{dx}} \quad (\text{at } H_x = H_{cr})$$

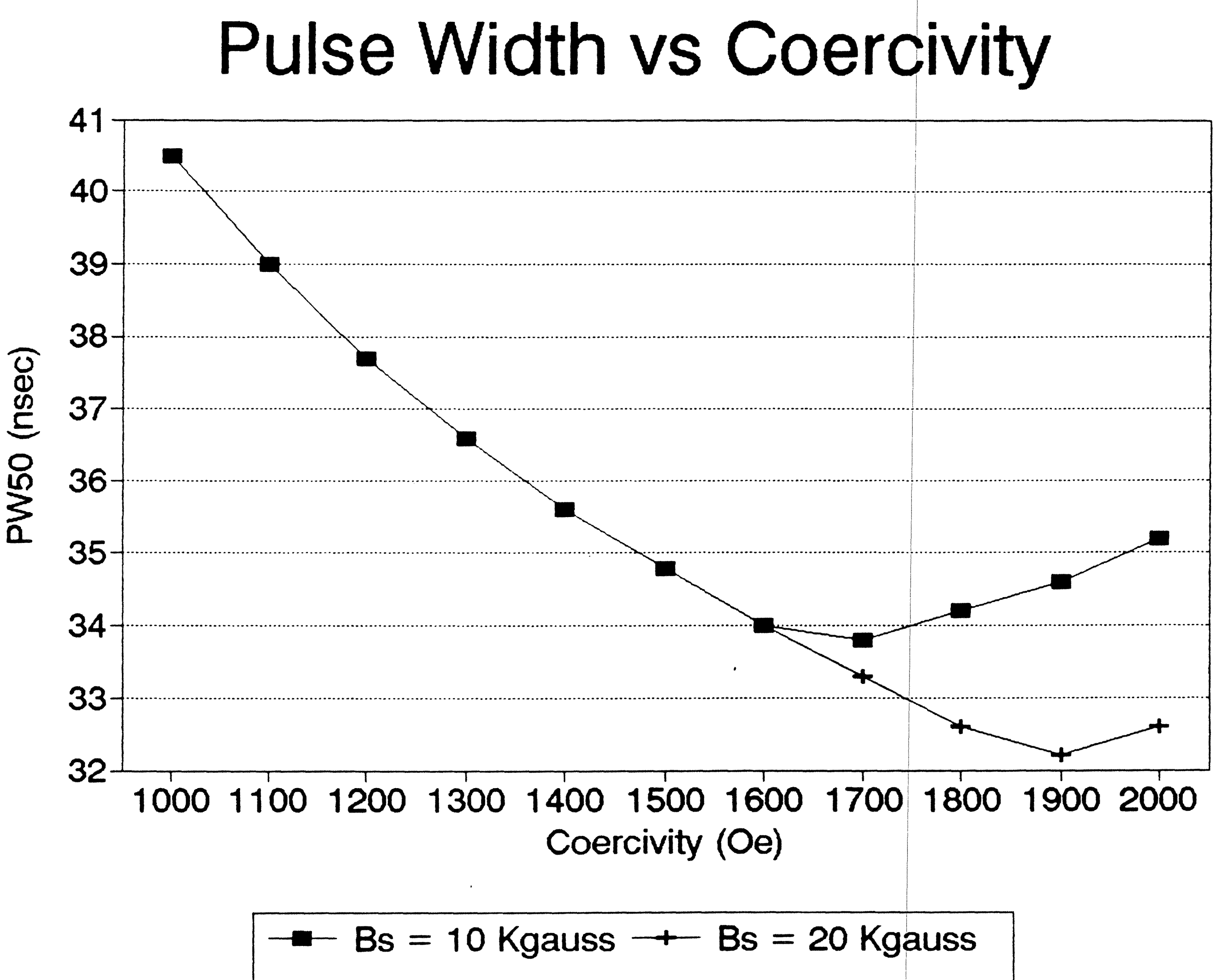
EM Williams
12/7/91

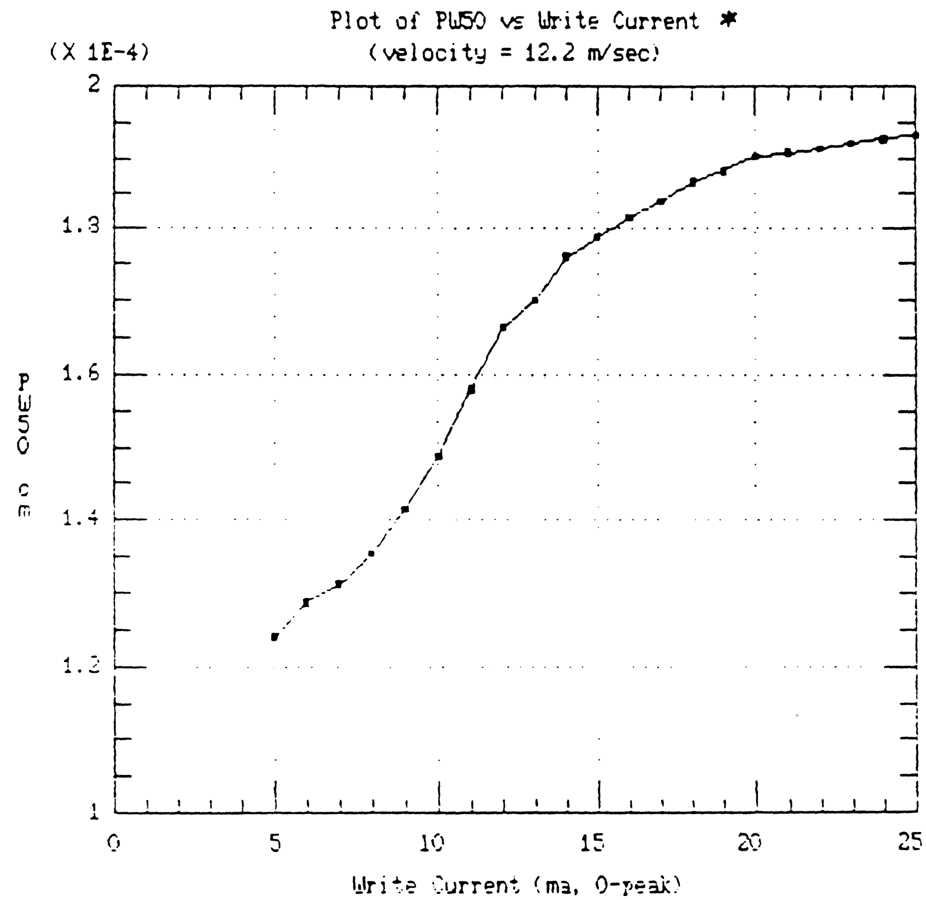




EM Williams
12/7/91


Transition Parameter vs Coercivity
Write Gradient and Medium-limited
Transition Parameter (micron)
0.13
0.125
0.12
0.115
0.11
0.105
0.1
0.095
0.09
0.085
1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000
Coercivity (Oe)
Bs = 10 Kgauss
Bs = 20 Kgauss
Medium-limited


Pulse Width vs Coercivity
PW50 (nsec)
41
40
39
38
37
36
35
34
33
32
1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000
Coercivity (Oe)
Bs = 10 Kgauss
Bs = 20 Kgauss



Thin Film Head: P1/G/P2 ≅ 3.2/0.5/3.2 um ; 32 turns

Thin Film Disk: M_r = 750 emu/cc ; H_c = 1100 Oe ;

δ = 650 Å ; S* = 0.90

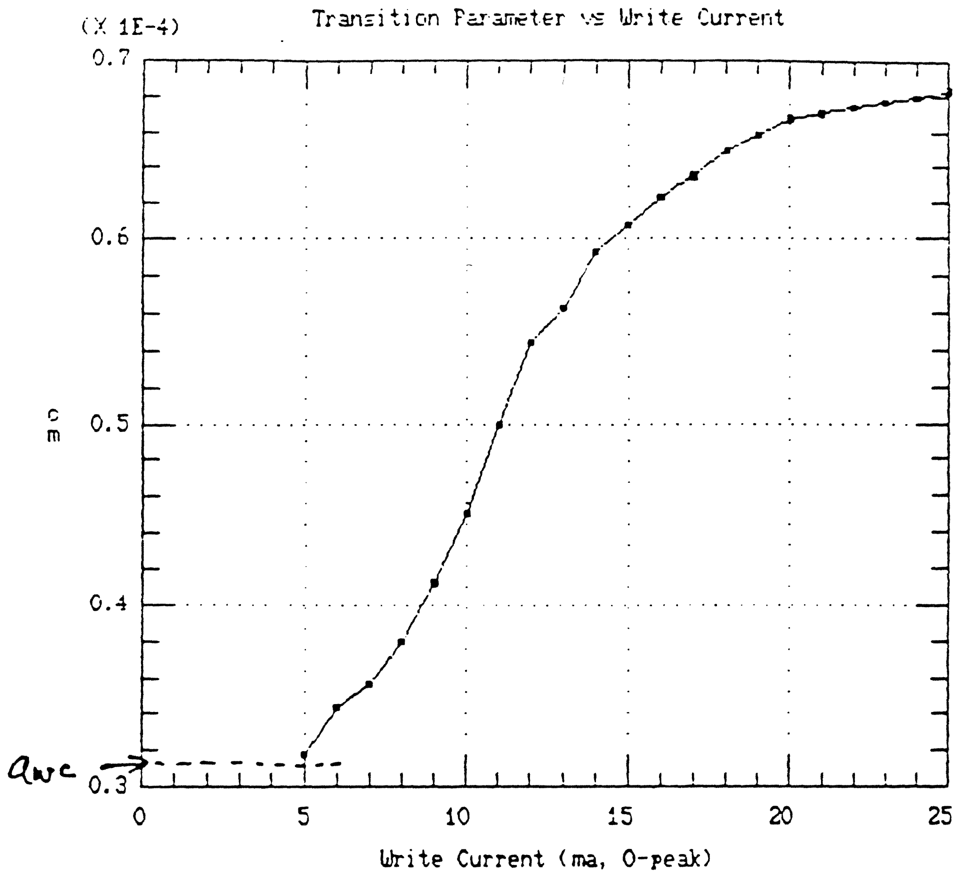
overcoat = 350 Å

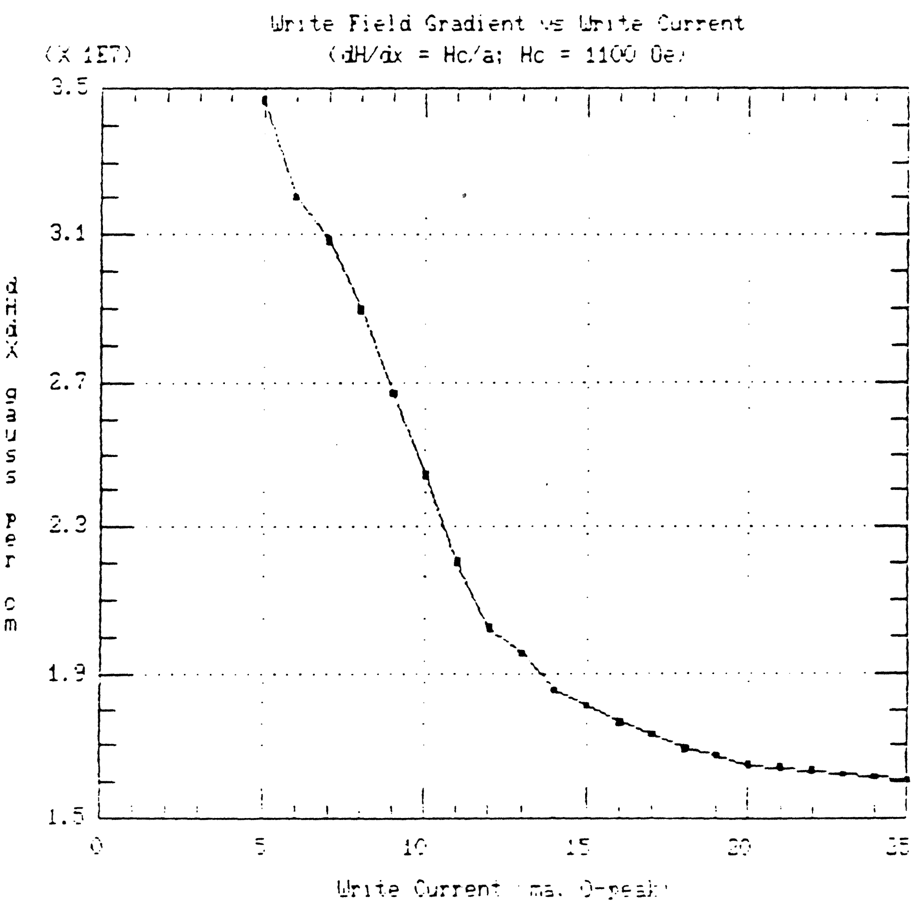
Fly Height ≅ 0.225 um

* Head over-lapped: Throat ≈ 1.53 um
to demonstrate
gradient limitations

E.M. Williams
Read-Rite Corp.

19/24





Deconvolved Parameter:

$$a = \left[\frac{PW50^2 - g^2}{4} \right]^{1/2} - d$$

d = fly. ht.

Medium-limited transition parameter (Williams-Comstock):

$a_{wc} \simeq 0.31$ um

Gradient is computed from experiment, under the assumption that transition parameter is limited by head field gradient.

"a" is the deconvolved value

E. M. Williams
Read-Rite Corp.

WRITING AT HIGH TRANSITION DENSITIES

- Partial erasure of previously written transitions (sometimes called "non-linear writing effects").

- Writing occurs near the trailing edge of the gap.

- Gap edge saturation exacerbates partial erasure effects (writing field spreads and write gradient decreases).

- Transition Density

$$\text{Density} = 1/(T_{min} \text{ x Velocity})$$

- Partial erasure of previous transition is likely if

$$\text{Density} \approx 2/G \qquad (G = \text{gap length})$$

$$\text{or} \quad T_{min} \approx G/(2 \text{ x Velocity})$$

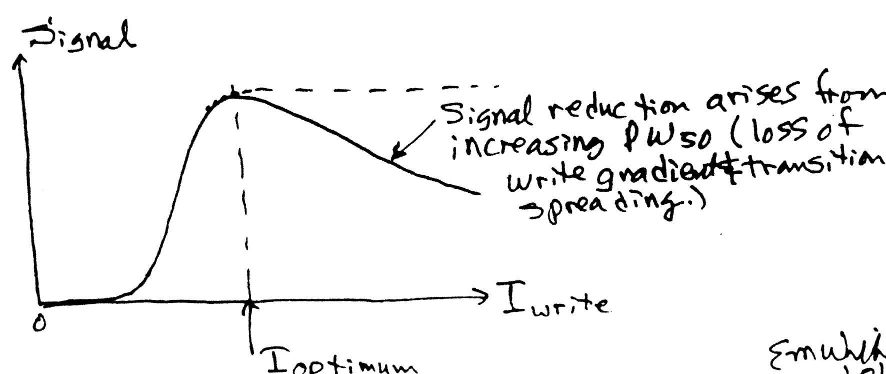
- Simple Example:

Velocity = 6 meters/sec (236 in/sec)

G = 0.40 μm

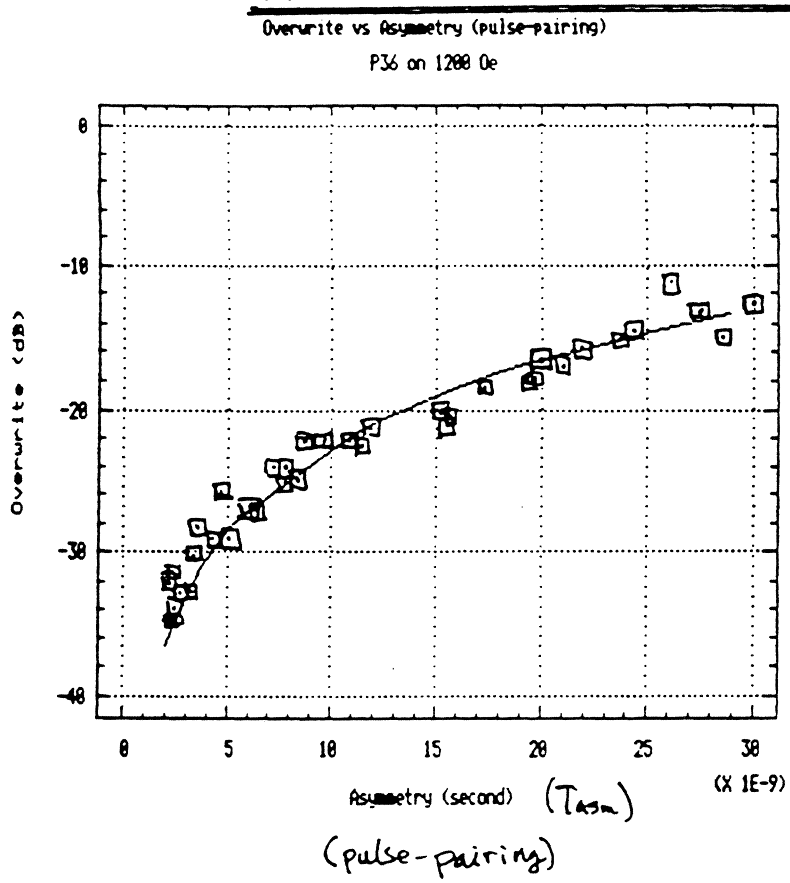
For $T_{min} \approx$ 33 nsec, partial erasure may occur.

- Effective gap length increases when writing with excessive write current.



E M Williams
12/8/91

TIME-DOMAIN NATURE OF OVERWRITE



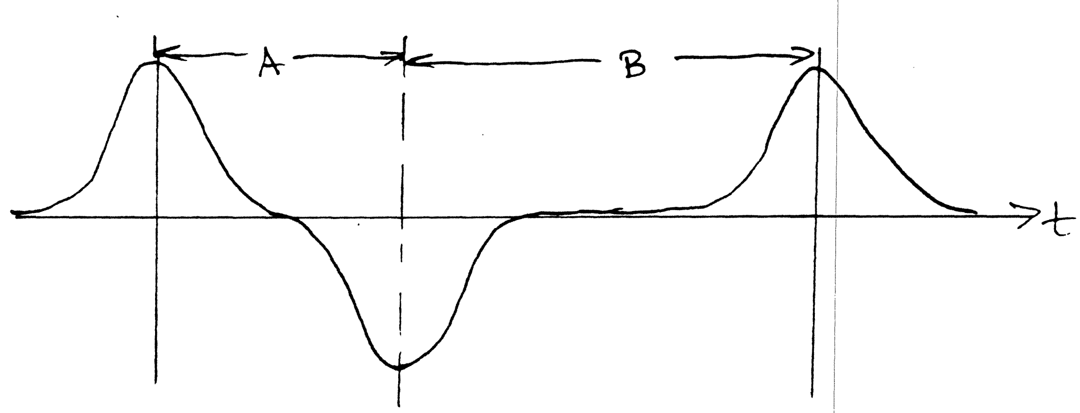
□-□ R&D Gazik Experiments at Read-Rite

—— Computed from $OW = 20 \log \Delta\phi$
5 MHz ; T_o = 4ns ; H_c = 1200 Oe
R = 0.95 (95%) ; $T_{asm} = 4T_{wo}$

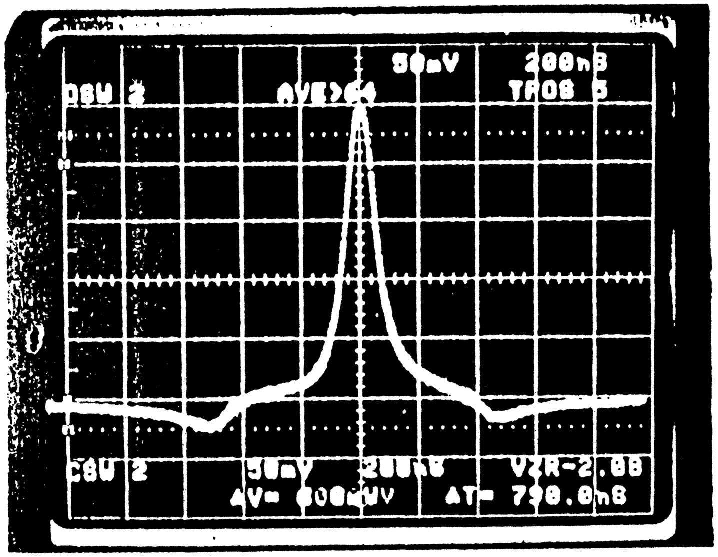
$$\boxed{OW(dB) = 20 \log_{10}\left(\frac{\pi f \cdot R \cdot T_{asm}}{2}\right)}$$

E M Williams
6/14/88
Read-Rite

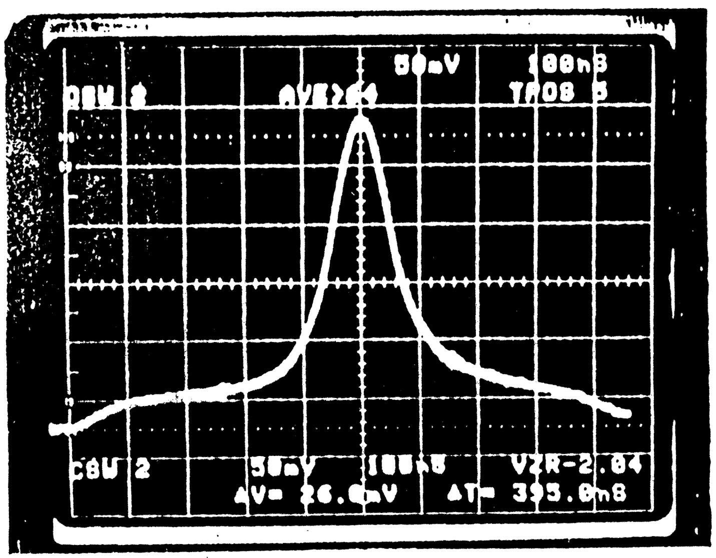
$$\boxed{\text{Write-induced Phase-shift} = T_{wo} = \frac{T_{asym}}{4}}$$

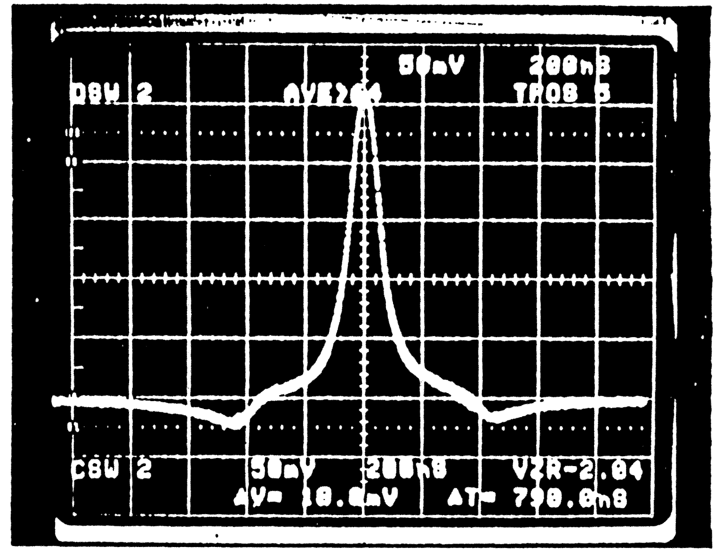


$T_{asym} \triangleq B - A$

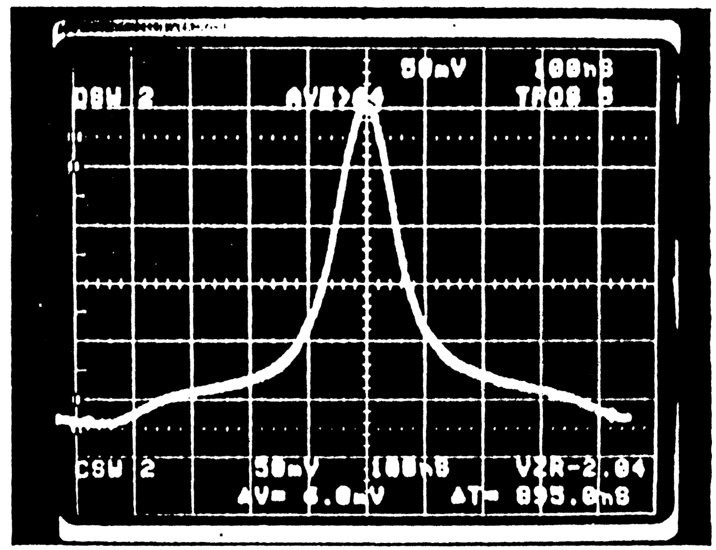


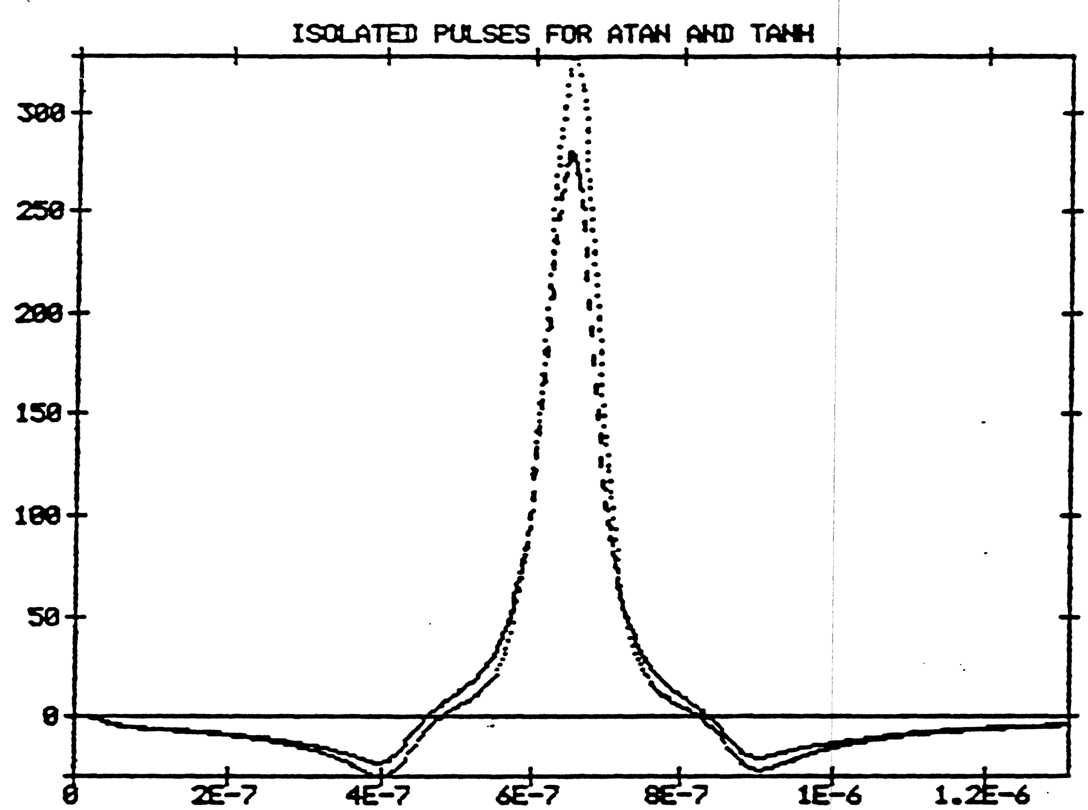
M38 #415403-137 on Denka 1100; 300 in/sec
Filter 2 (20 MHz)





M38 #415984-369 on Denka 1100; 300 in/sec
Filter 2 (20 MHz)





	$\frac{2}{\pi}\tan^{-1}\left(\frac{x}{a}\right)$	$\tanh\left(\frac{2x}{\pi a}\right)$	TFH Experiment
PW50	1.02 um	1.06 um	1.03 um
PW25	1.70	1.61	1.61
PW10	2.70	2.33	2.66
PW50/PW25	0.60	0.66	0.65
PW50/PW10	0.38	0.46	0.43

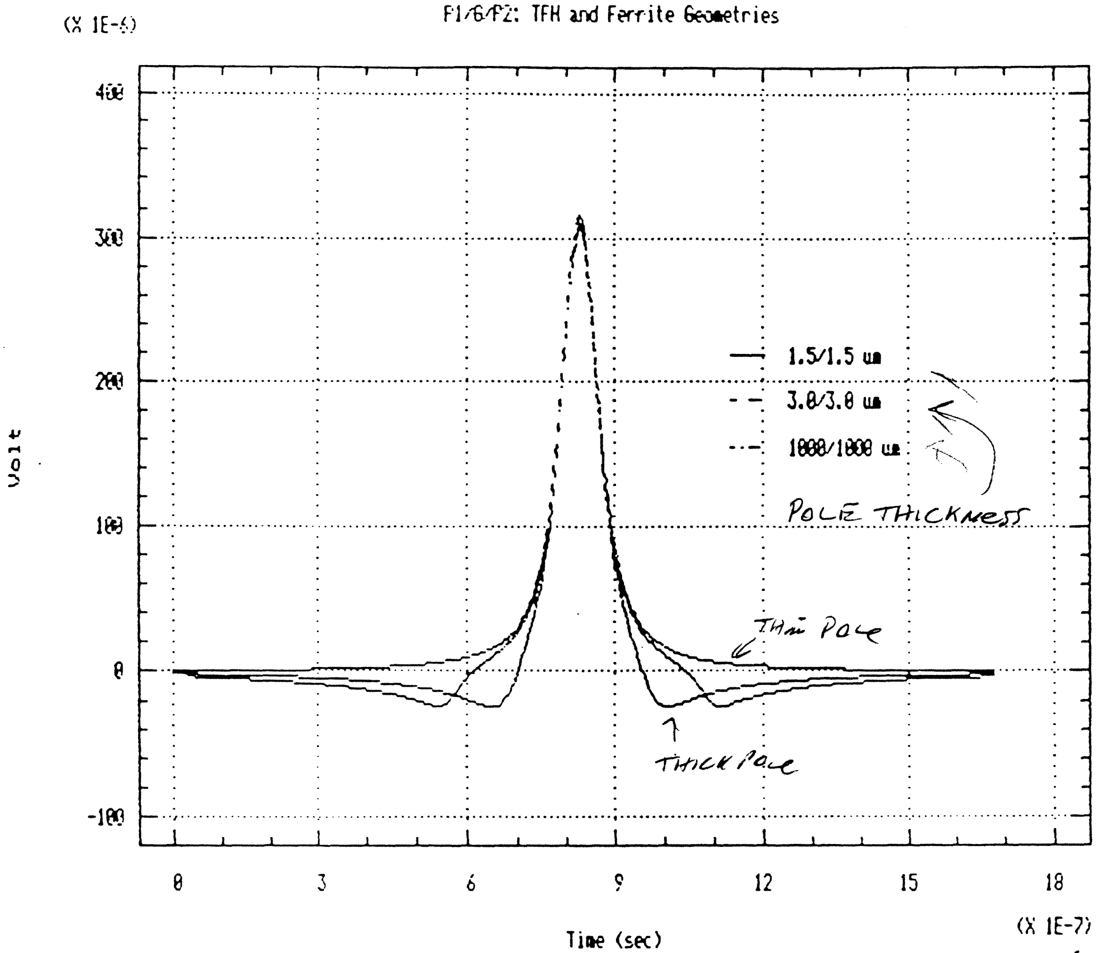
See also Noyan et al, ~~IEEE~~ Trans. Magn., MAG-24, 1811-1813, Mar (1988).

Middleton, B.K., IEEE Trans. Magn., MAG-27, 3563-3569, Jul (1991).

EMWilliams
12/7/91

Isolated Pulses vs Time

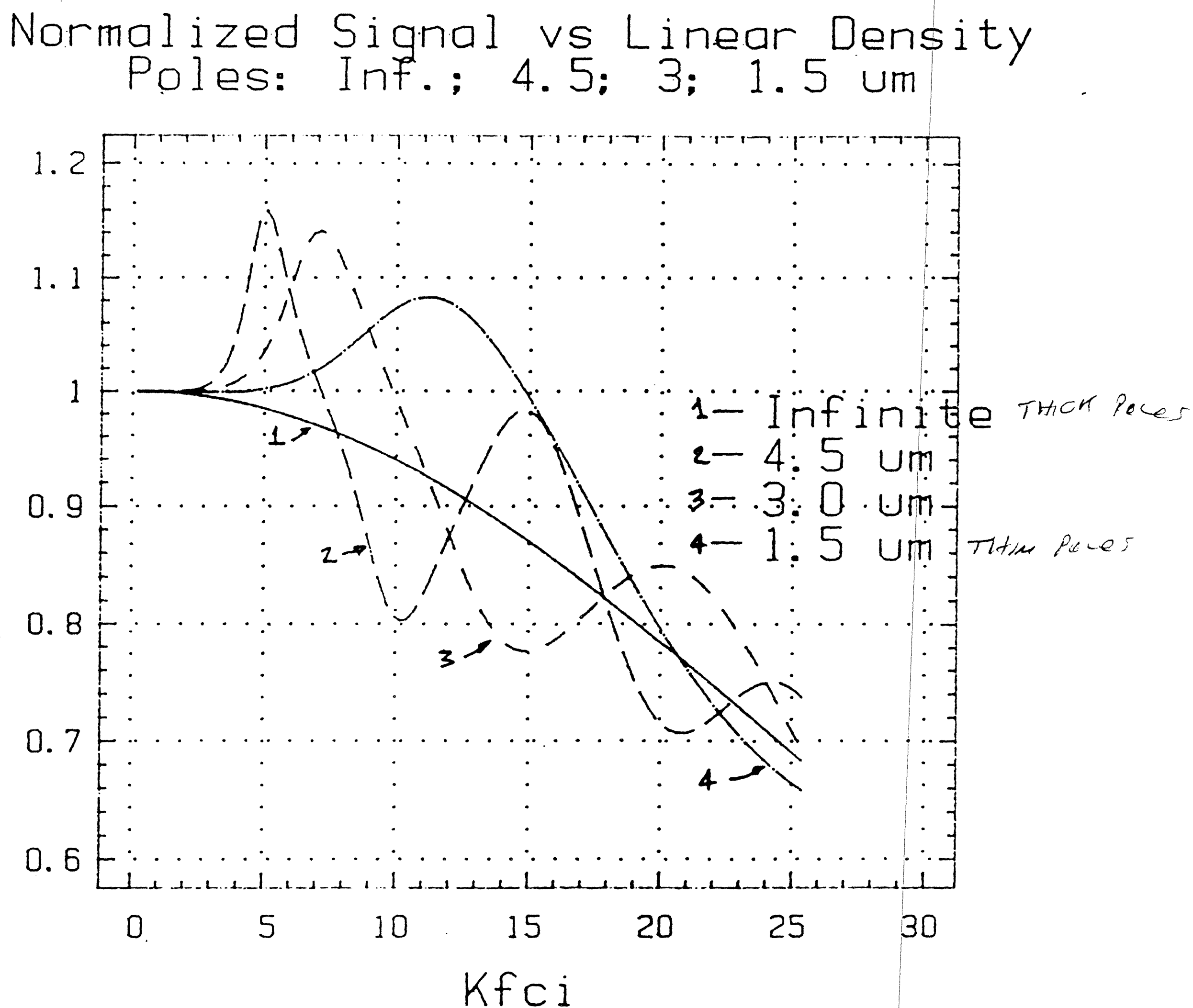
F1/6/P2: TFH and Ferrite Geometries



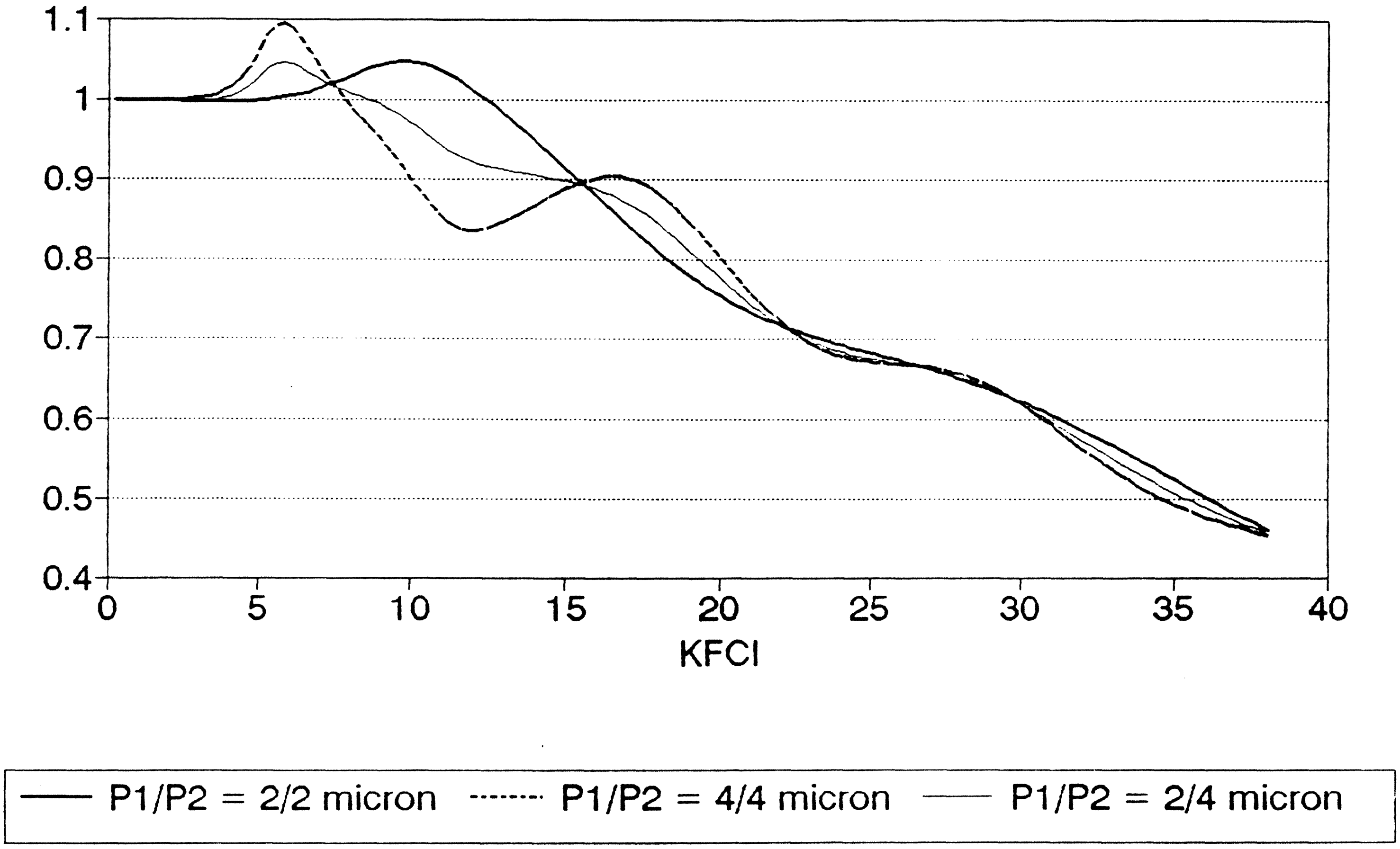
PW50 = 92 nsec

V = 1200 cm/sec

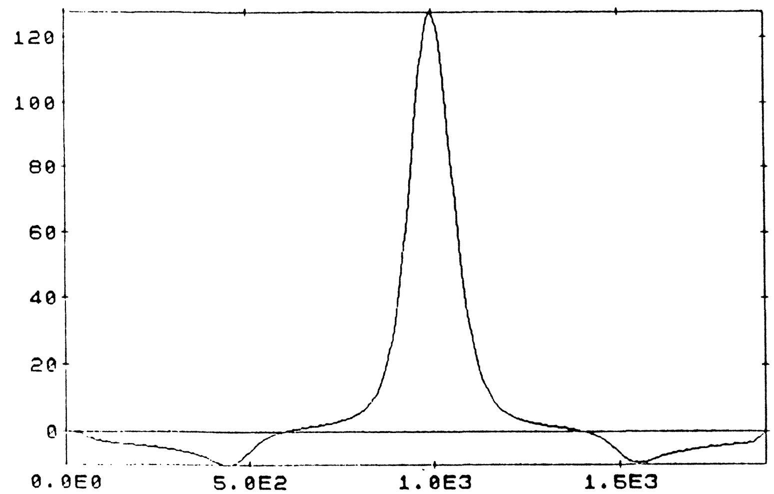
USE HYPERBOLIC TANGENT FOR MODELING NOT ARCTANGENT.


Normalized Signal vs Linear Density
Poles: Inf.; 4.5; 3; 1.5 um
1.2
1.1
1
0.9
0.8
0.7
0.6
0
5
10
15
20
25
30
Kfci
1— Infinite
2— 4.5 um
3— 3.0 um
4— 1.5 um
THICK Poles
THIN Poles
1
2
3
4

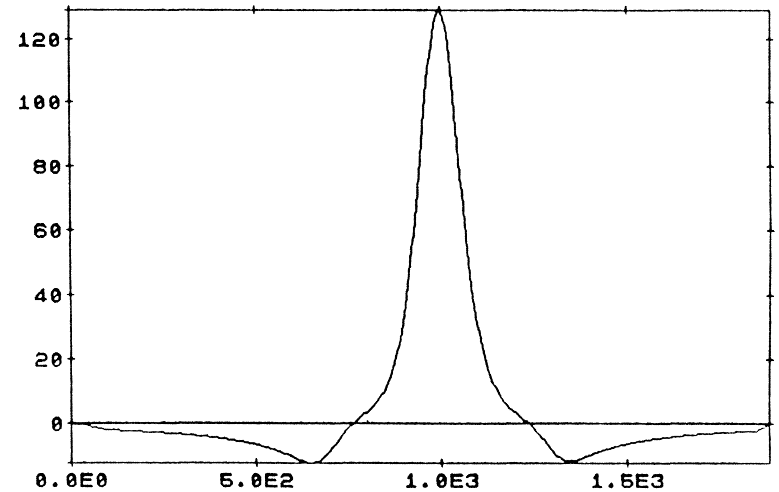
Normalized Signal vs Density
(Thin, Thick, Asymmetric Poles)



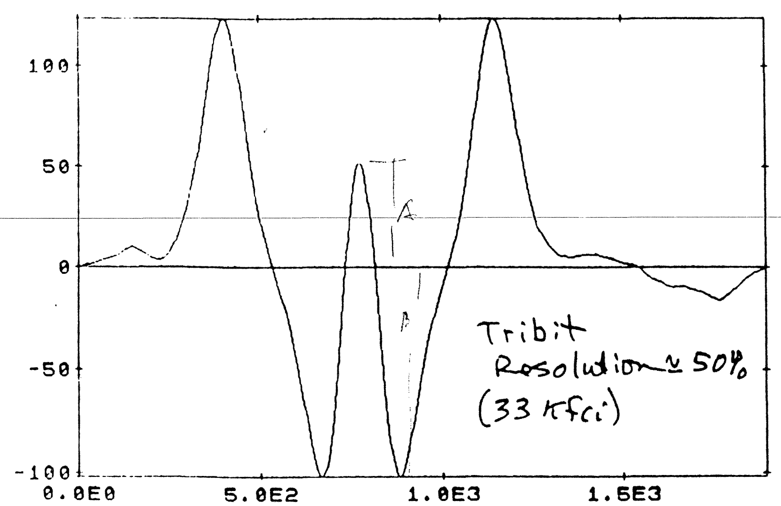
ISOLATED PULSE VS TIME: 3.5 um POLES



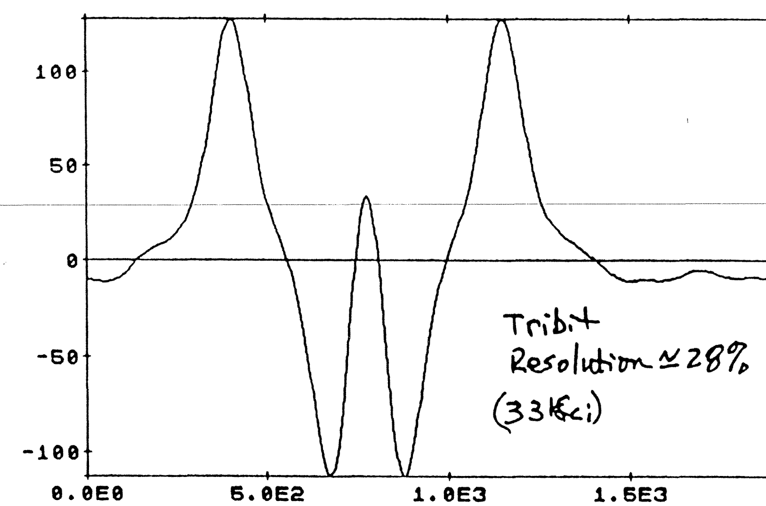
ISOLATED PULSE VS TIME: 2.0 um POLES



TRIBIT PATTERN: 3.5 um POLES



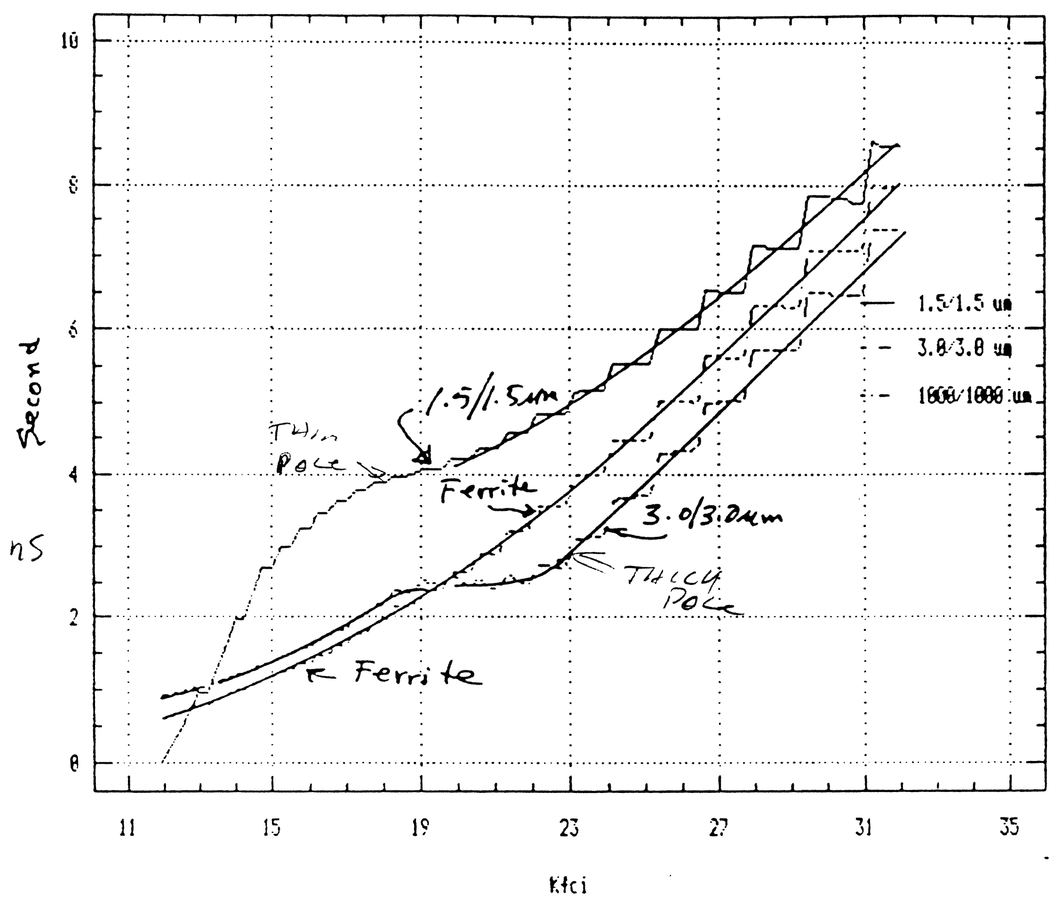
TRIBIT PATTERN: 2.0 um POLES



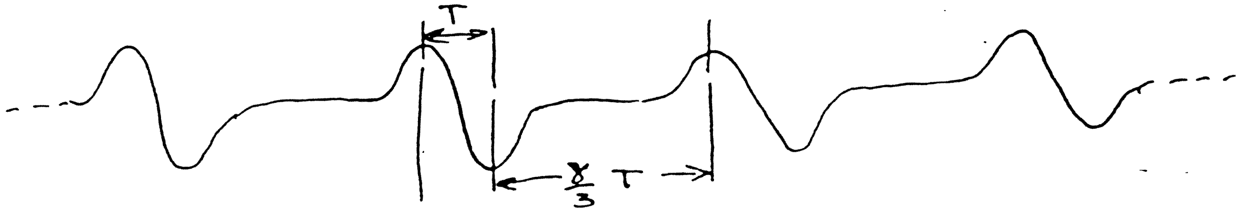
EMWilliams

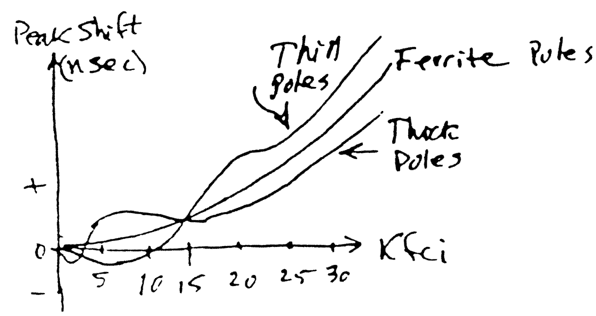
Dibit Peakshift vs Linear Density

F1/G/P2: TFH and Ferrite Pole Geometries (2,7) RLL



Velocity = 1200 cm/sec





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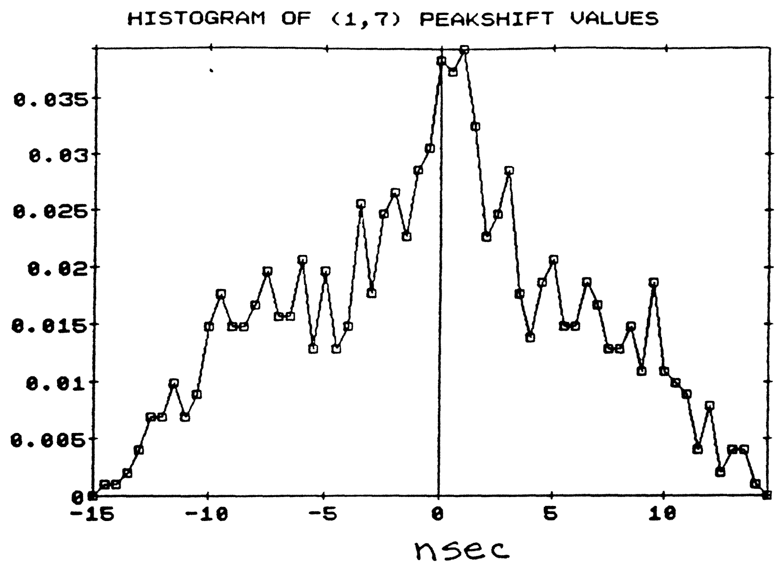
Random Data RLL Encoded

Window = ± 27.8 nsec (43.7 Kbpi ; 12 Mb/sec)



P1|G|P2

3.5/0.40/3.5 um

THICK POLE

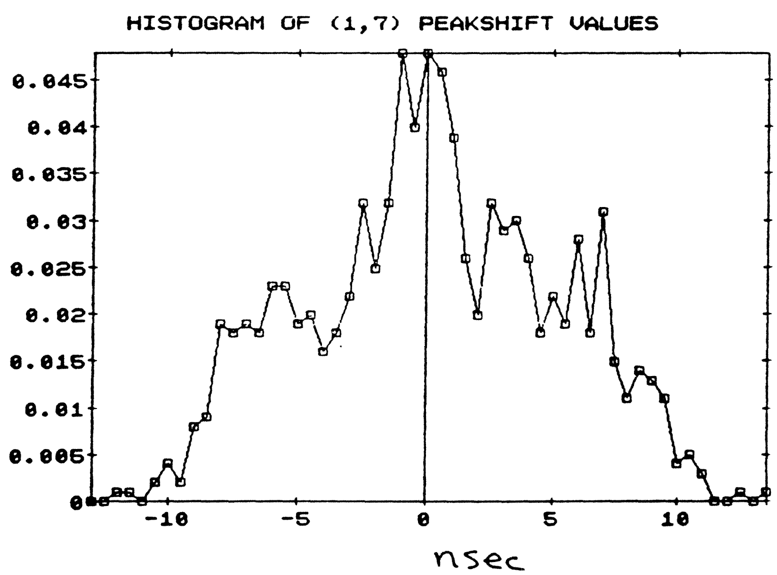
931 transitions

$\bar{X}$ = -0.41 nsec

σ = 6.19 "

Max = 14.8 "

Min = -14.6 nsec



P1|G|P2

2.0|0.4|2.0 um

Thin Pole

929 transitions

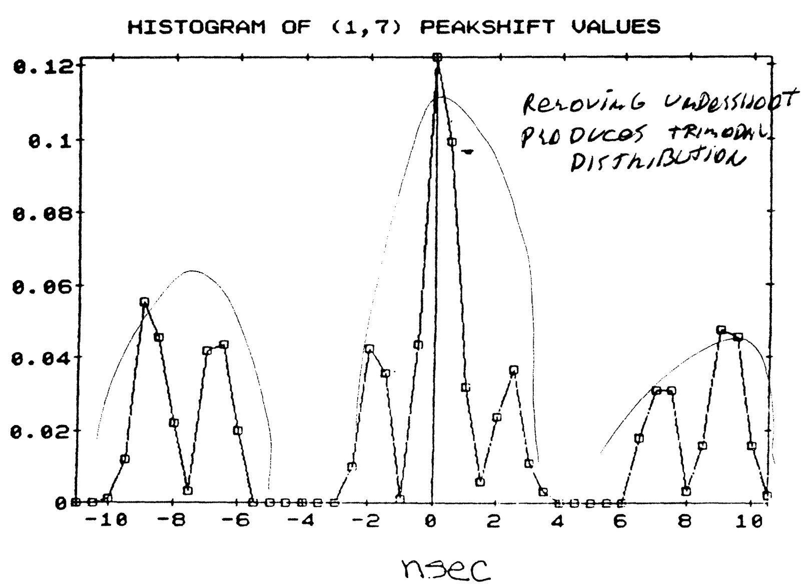
$\bar{X}$ = 0.102 nsec

σ = 4.88 "

Max = 13.3 "

Min = -12.5 nsec

Remove undershoot



P1|G|P2

∞/0.40/∞ um

927 transitions

$\bar{X}$ = -0.31 nsec

σ = 5.82 "

Max = 10.2 "

Min = -10.0 nsec

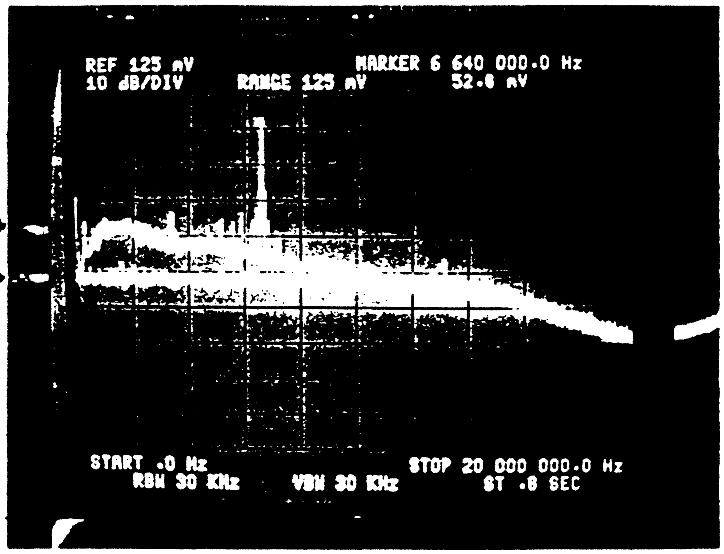
E M Williams

Head, Preamp & Medium Noises

TRANSITION NOISE

$5.8 \frac{nV}{\sqrt{Hz}}$ →

$1.1 \frac{nV}{\sqrt{Hz}}$ →



Disk "A" (Thin Film)

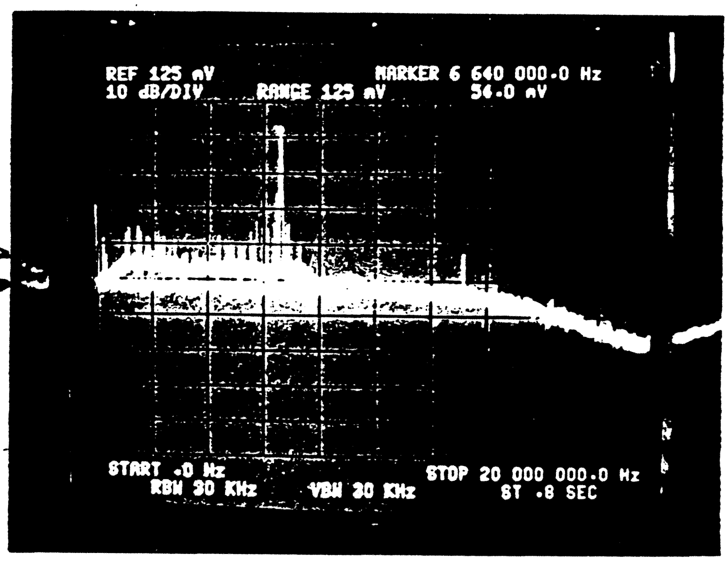
28 Kfci

Signal ≅ 190 mv (p-p)

$2.5 \frac{nV}{\sqrt{Hz}}$ →

$1.1 \frac{nV}{\sqrt{Hz}}$ →

INTRINSIC



Disk "B" (Thin Film)

28 Kfci

Signal ≅ 194 mv (p-p)

Head Noise Spectral Density $N_h \approx 0.56$ nv/$\sqrt{Hz}$

Preamp " " " $N_p \approx 0.95$ nv/$\sqrt{Hz}$

Head + Preamp $= [N_h^2 + N_p^2]^{1/2} \approx 1.1$ nv/$\sqrt{Hz}$

$$E.R. = 1 - erf(z) = erfc(z) \,,$$
$$where\ z = SNR \frac{T_W}{PW50} \,.$$

If $T_{asym} = 0$ & ISI Shift $= 0$, then

$$T_W = T_{WSNR} = \frac{4.57\ PW50}{SNR} \,.$$

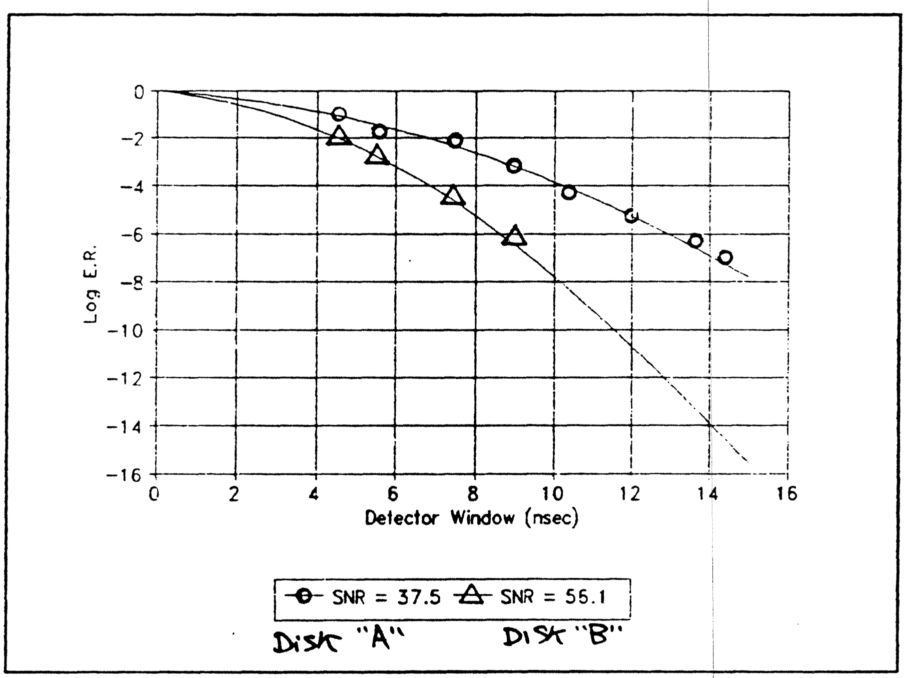
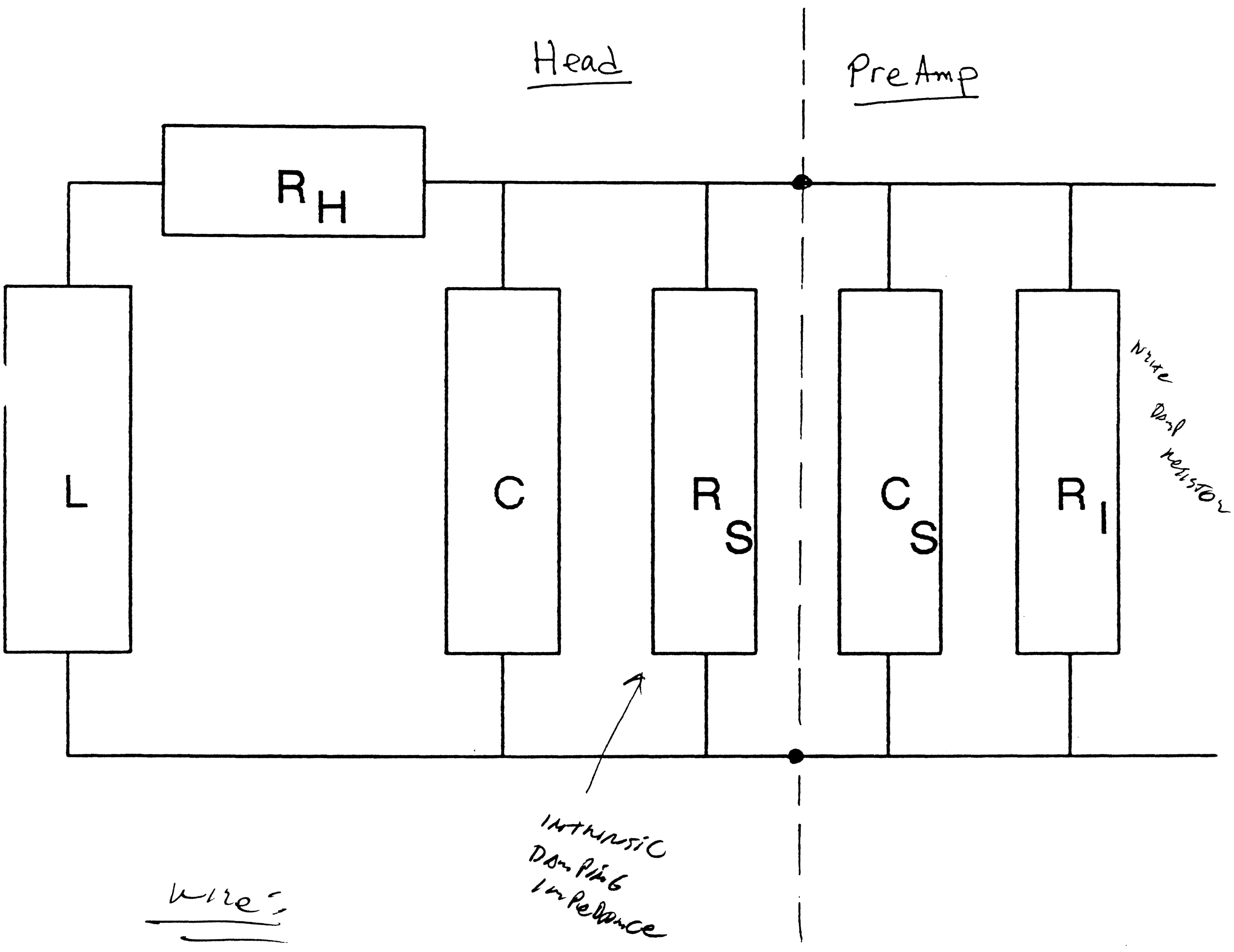


Figure 5: Log_{10} E.R. vs Detector Window Size



Wire:

20nH / ~~[illegible]~~ cm length

.8pF / cm of length

GM Williams

Table 1: Electrical Properties of Inductive Heads

Head Type	$R_H(\Omega)$	$R_S(\Omega)$	L(nH)	C(pF)	f_R(MHz)
TFH (30-turn)	31.0	292	475	5.2	101.3
TFH (42-turn)	45.0	417	.825 μH 825	5.0	78.4
MIG (34-turn)	4.4 [illegible]	2805	1580	5.0	56.8
Mini-Composite	6.0	3410	4200	5.2	33.9
Mini-Monolithic	6.0	5410	14 μH 14000	6.0	17.4

4cm long wire

If a head is loaded by a preamplifier differential input resistance (R_I) and input capacitance (C_S), the real part of the total impedance is

$$Re[Z] = \frac{R_p}{D}[(R_H)(R_H+R_p) + (\omega L)^2], \tag{2}$$

where the terms R_P and D are defined by the relations

$$R_p = \frac{R_S\ R_I}{R_S+R_I} \tag{3}$$

$$D = [R_H+R_P-J(\omega^2)]^2+[F\omega]^2 \tag{4}$$

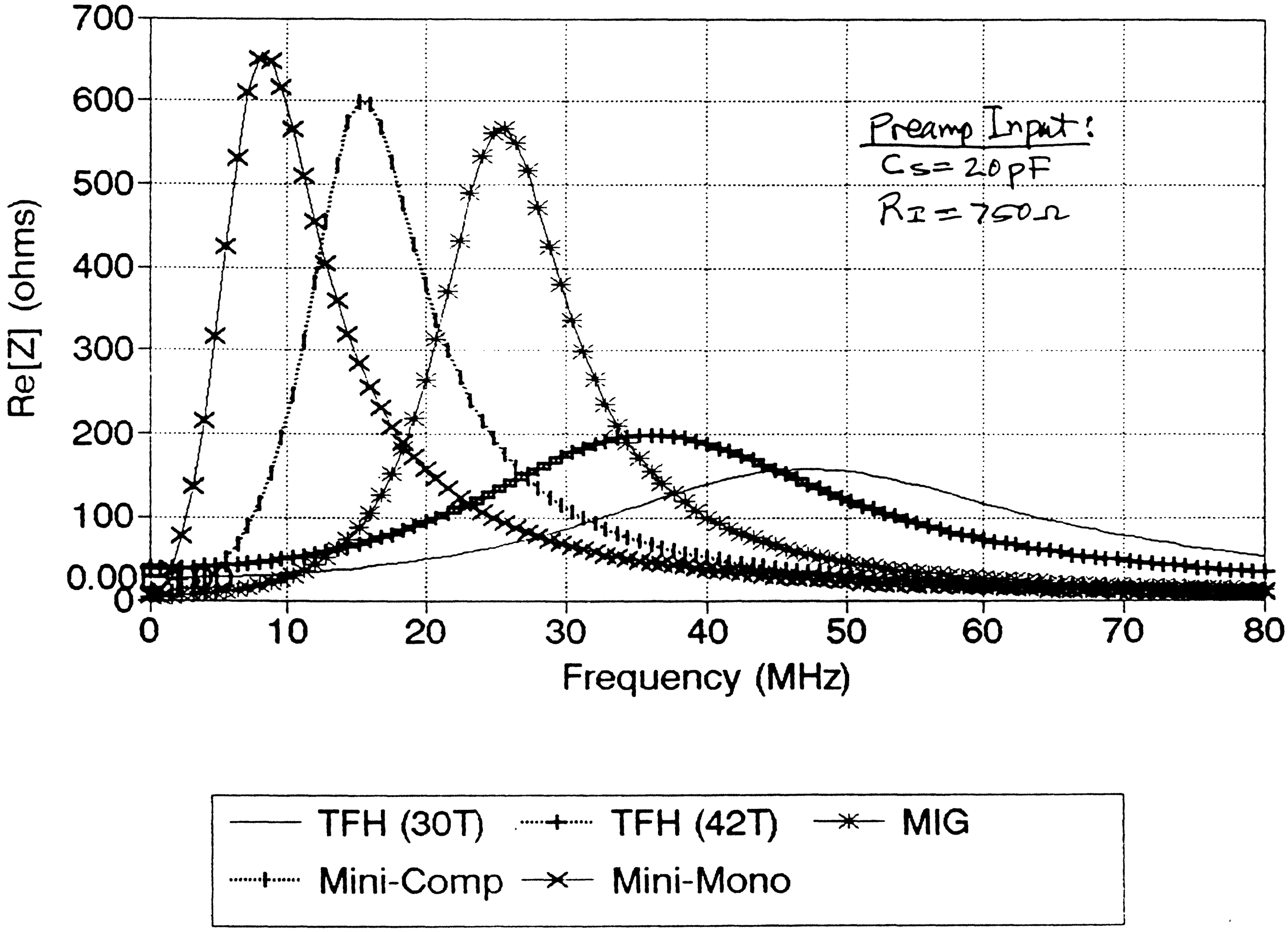
and F and J are given by

$$F = L + [R_H\ R_P(C+C_S)], \tag{5}$$

$$J = R_P\ L\ (C+C_S). \tag{6}$$

When a head is loaded by a preamp (assume R_I = 750Ω and C_S = 20 pF), Re[Z] changes substantially; Figure 2 is a plot for the heads in Table 1, and resonant frequencies are reduced by the input capacitance of the preamp.

Noise Impedance of Heads



S. M. Williams

TIMING WINDOW and MARGIN BUDGET

Error Rate = erfc(z)

$z \cong (SNR/PW50)(Tw - Tp - Two)$

$Tp \cong 0$ for symmetric patterns (1111, 1010, etc.)

$Two \cong 0$ for any pattern written on same pattern

$erfc(4.50) \cong 1E-10$ Error Rate

(NOTE: $4.50 \simeq \frac{6.36134}{\sqrt{2}}$ where 6.36134 is the argument for the normal probability function)

$Tw10 = (4.50\ PW50/SNR) + Tp + Two$

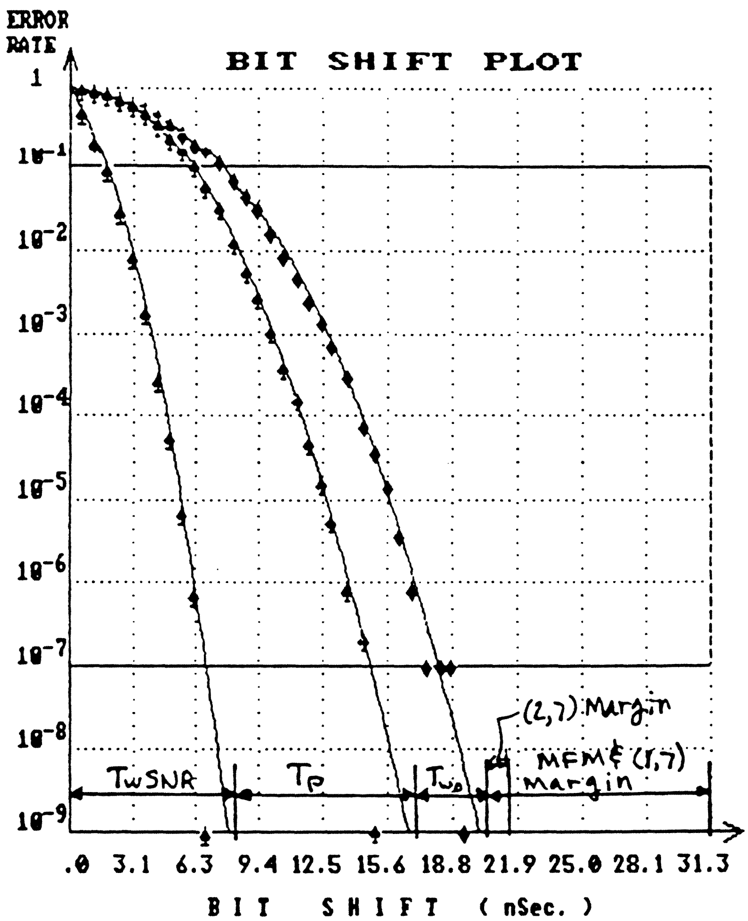
$= TwSNR + Tp + Two$

= Noise + Pattern + Write-induced Shifts

SNR is pk-pk signal to RMS noise ratio

EMW
READ-RITE

DETECTOR WINDOW (MARGIN) TESTING



TRAK	HD	PTRN	ZERO	S	THRS	
♦ 1145	0	B6D9	20.0	I	49.8	B6D9 on DC Erase
FILTER 1		15mA	125nS	F		
♦ 1145	0	B6D9	16.6	I	49.8	B6D9 on B6D9
FILTER 1		15mA	125nS	F		
♦ 1145	0	FFFF	7.8	I	49.8	FFFF on FFFF
FILTER 1		15mA	125nS	F		

$$\boxed{\begin{aligned} T_{w10} &= \text{Timing window at } 10^{-10} \text{ B.E.R.} \\ &= T_{wSNR} + T_p + T_{wo} \end{aligned}}$$

T_{wSNR} = Noise-induced shift
T_p = Pattern-induced "
T_{wo} = Write-induced "

♦ |r|= .999669

ID: P38/K1200

11/21/88 08:52:50

$$\text{Error Rate} = \operatorname{erfc}(z)$$

$$z \cong \frac{SNR}{PW50}(T_w - T_p - T_{wo}) \quad \text{where} \left(SNR : \frac{P\text{-}P}{rms} \right)$$

For $E.R. = 10^{-10}$; $z_{10} \cong 4.50$

$$\therefore \quad T_{w10} \cong \frac{4.50\ PW50}{SNR} + T_p + T_{wo} = T_{wSNR} + T_p + T_{wo}$$

$$\left(T_{wo} \cong \frac{T_{asym}}{4} \right)$$

The Read/Write Channel:

Opportunities for Digital Signal Processing

Tom Howell
Quantum Corporation

IIST
December 1991

Outline

1. Review of Peak Detection

2. Sampling Detection

3. Gain and timing control

4. Equalization

5. Performance

Comparison of RLL (D,K) Constraints

<table>
<tr><td>Data:</td><td colspan="6">1</td><td colspan="6">1</td><td colspan="6">0</td><td colspan="6">0</td></tr>
<tr><td>FM:</td><td colspan="3">1</td><td colspan="3">1</td><td colspan="3">1</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">1</td></tr>
<tr><td>MFM:</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">1</td></tr>
<tr><td>(2,7):</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">0</td></tr>
<tr><td>(1,7):</td><td colspan="4">1</td><td colspan="4">0</td><td colspan="4">1</td><td colspan="4">0</td><td colspan="4">0</td><td colspan="4">0</td></tr>
</table>

FM → MFM → (2,7) Same clock, reduced pulse crowding

(1,7) vs (2,7) Involves trade-offs

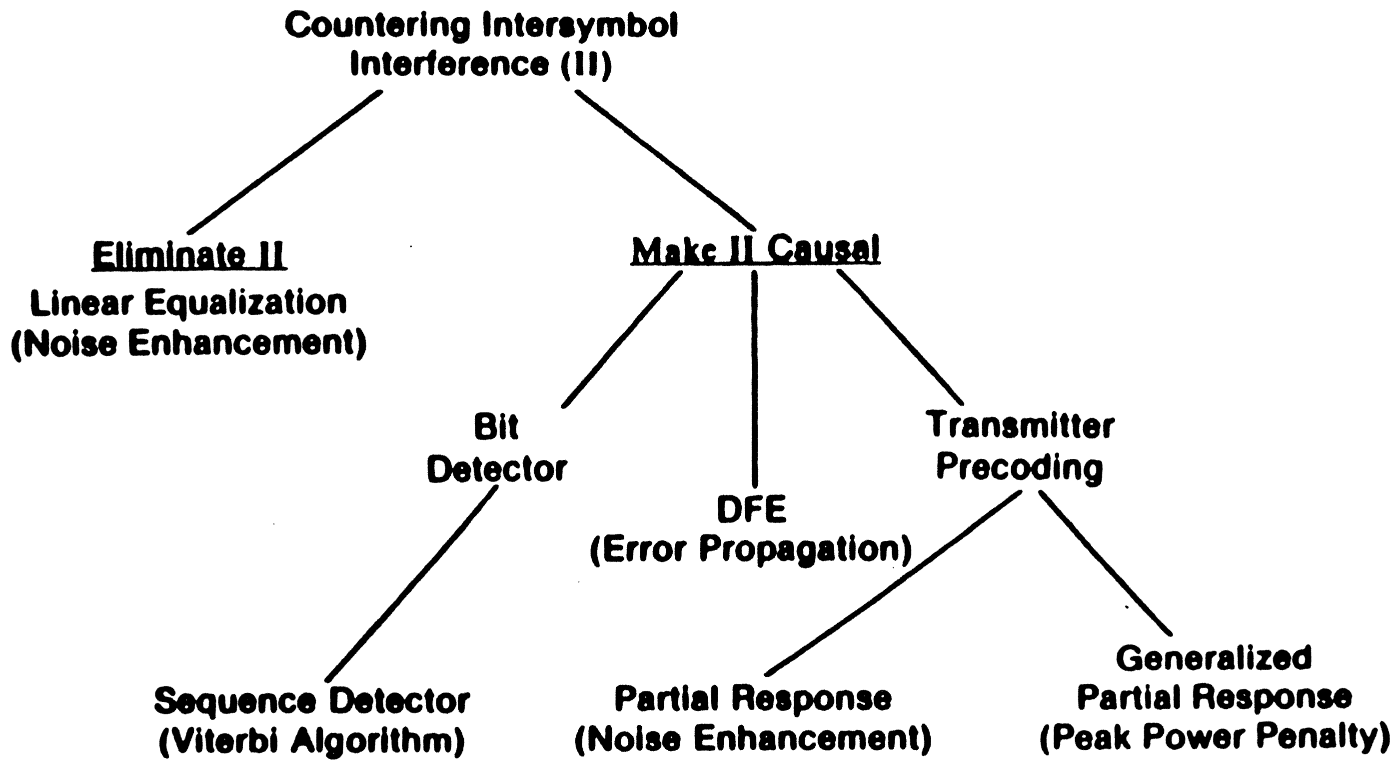
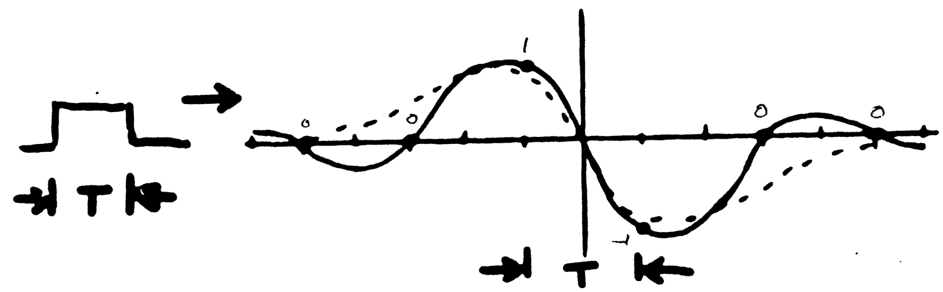
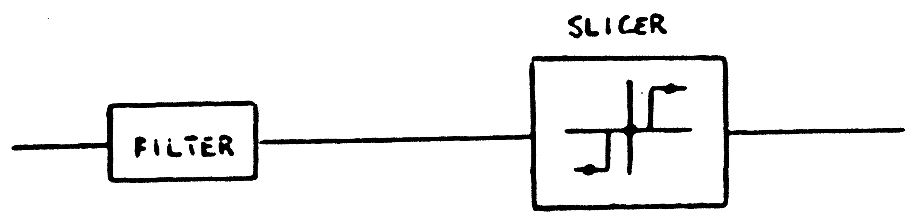


Figure 1. Summary of available methods of countering intersymbol interference in sampling detectors.

Zero-Forcing Equalization

- Equalize NRZ bit response to:

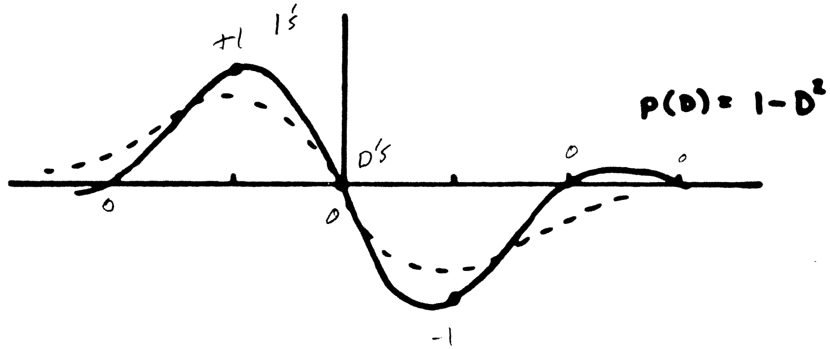


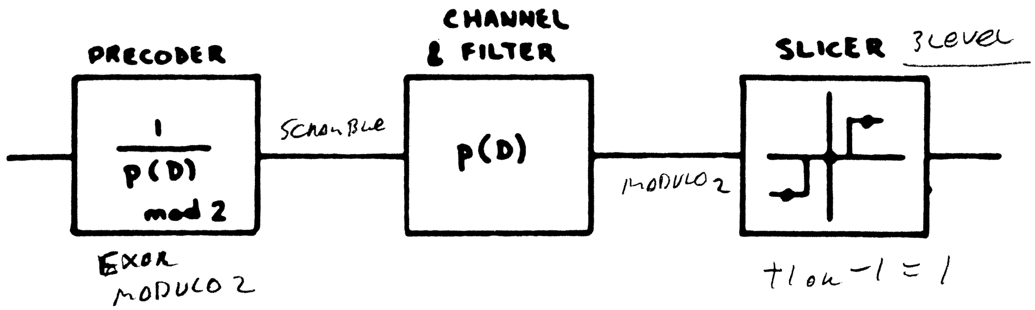


- limited by noise enhancement

Partial Response

- Equalize NRZ bit response to:



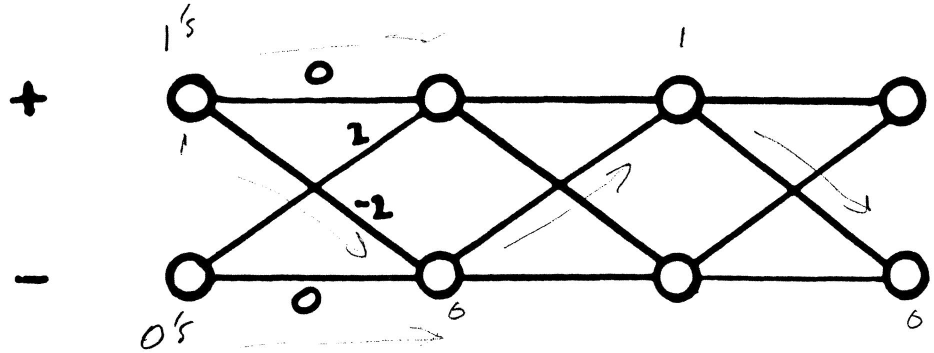


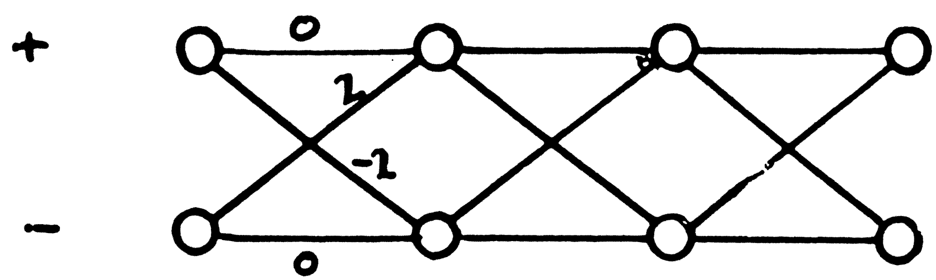
- no error propagation
- less noise enhancement than ZFE or Flat
- more noise enhancement than DFE

3db of noise immunity compared to peak detection method. (take 2x much noise)

Trellis Diagram

1010





The Recursive Algorithm

DIFF. SUM OF SQUARES USED:

DECISION

PREVIOUS SUM OF SQUARES

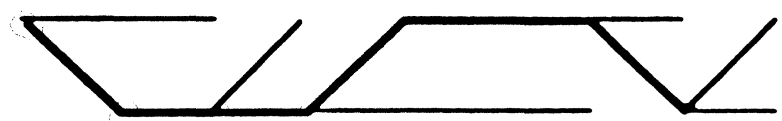
COMPARE

$$DJ_n = \begin{cases} y_n + 1 & \text{if } +1 < (DJ_{n-2} - y_n) \\ DJ_{n-2} & \text{if } -1 < (DJ_{n-2} - y_n) < +1 \\ y_n - 1 & \text{if } (DJ_{n-2} - y_n) < -1 \end{cases}$$

WHAT IS TRUE?

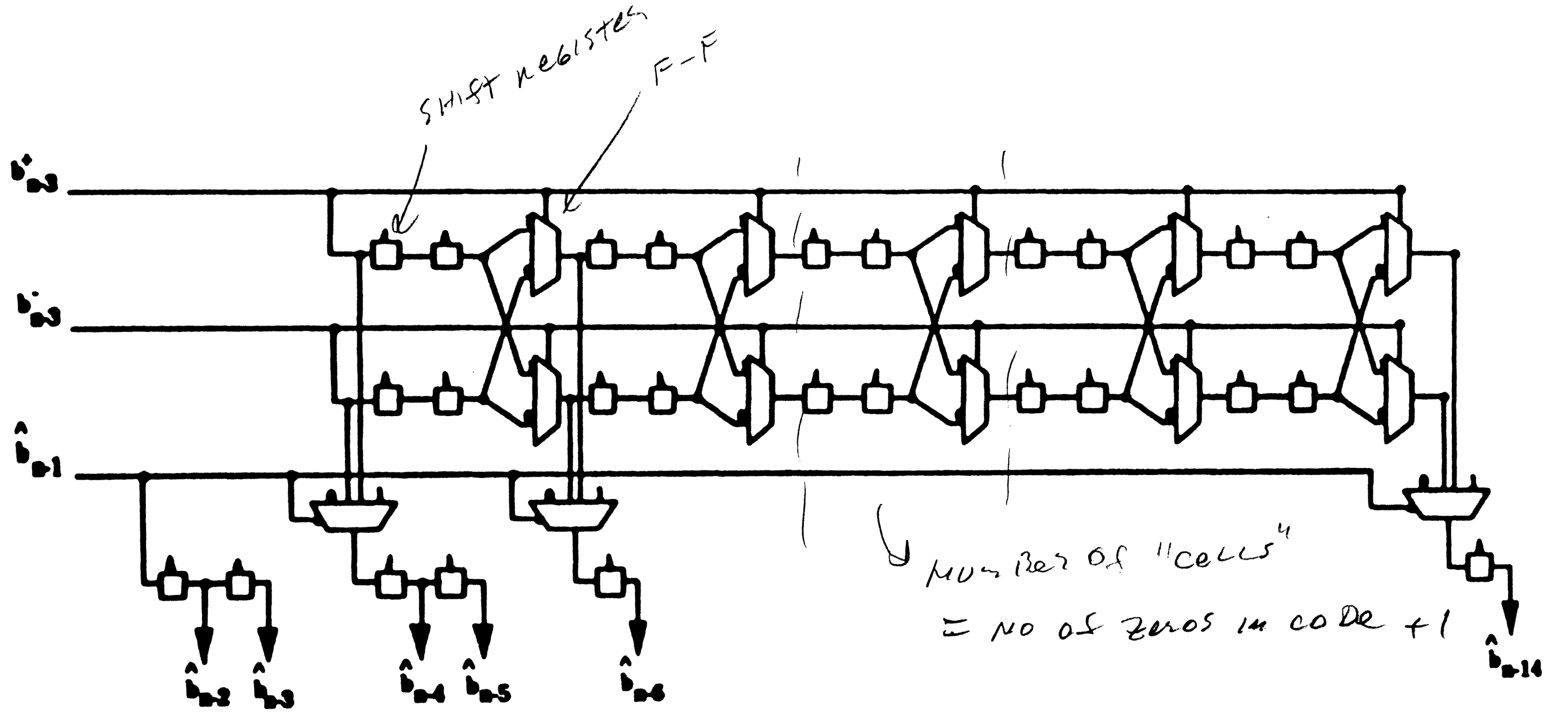
ENTER TRUTH

Example:

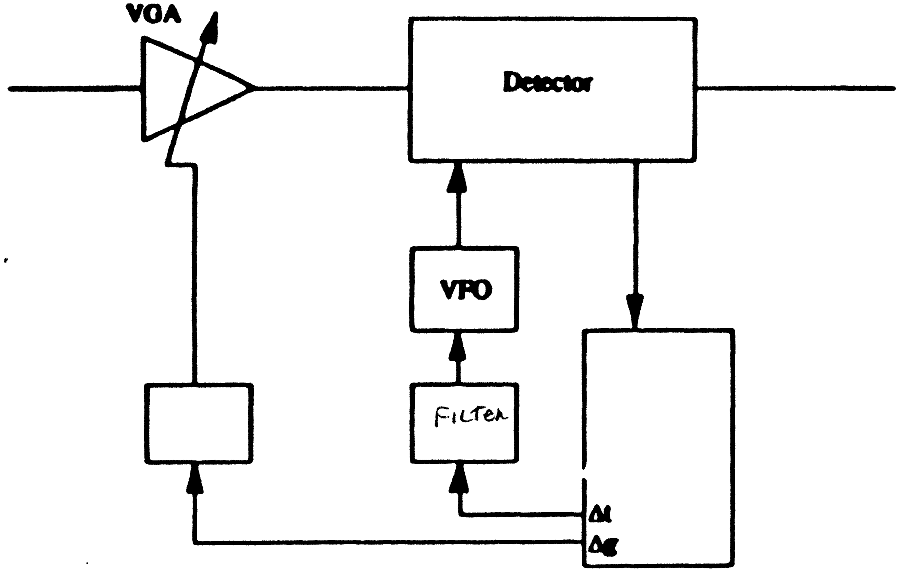


1 0 0 0 1 1 1 0

Path Memory


SHIFT REGISTERS
F-F
$\hat{b}_{n-1}$
$\hat{b}_{n-2}$
$\hat{b}_{n-3}$
$\hat{b}_{n-4}$
$\hat{b}_{n-5}$
$\hat{b}_{n-6}$
$\hat{b}_{n-14}$
NUMBER OF "CELLS"
= NO OF ZEROS IN CODE +1

Timing and Gain Control

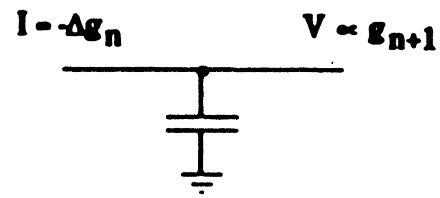


Filtering the Error Signals

CHARGE COUPLED LOGIC IMPLEMENTATION!

$$g_{n+1} = g_n - \gamma \Delta g_n$$

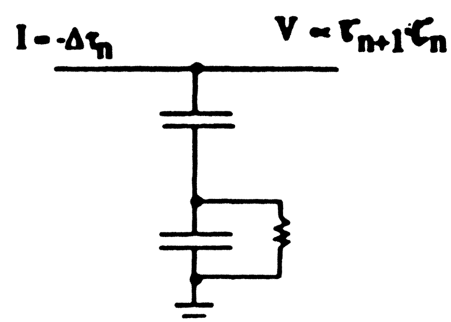
DIGITAL

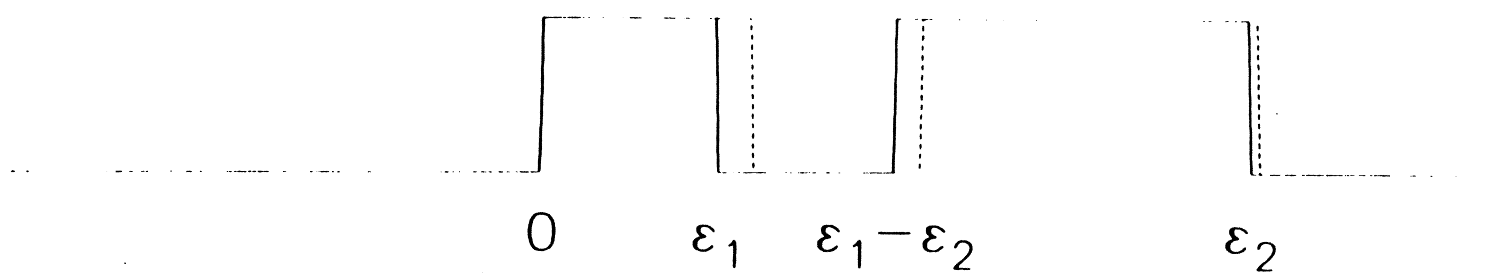


ANALOG

$$\Delta T_{n+1} = \Delta T_n + \zeta \Delta \tau_n$$

$$\tau_{n+1} = \tau_n - \beta \Delta \tau_n - \Delta T_n$$

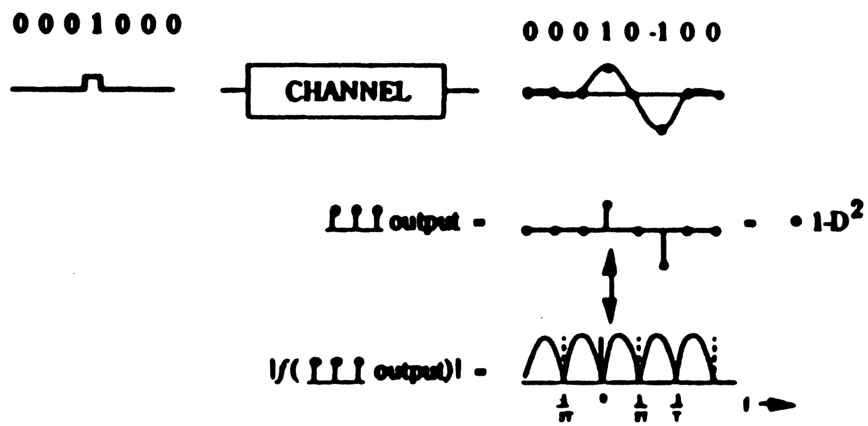




Nominal write current

Precompensated write current

Class IV (Modified Duobinary)



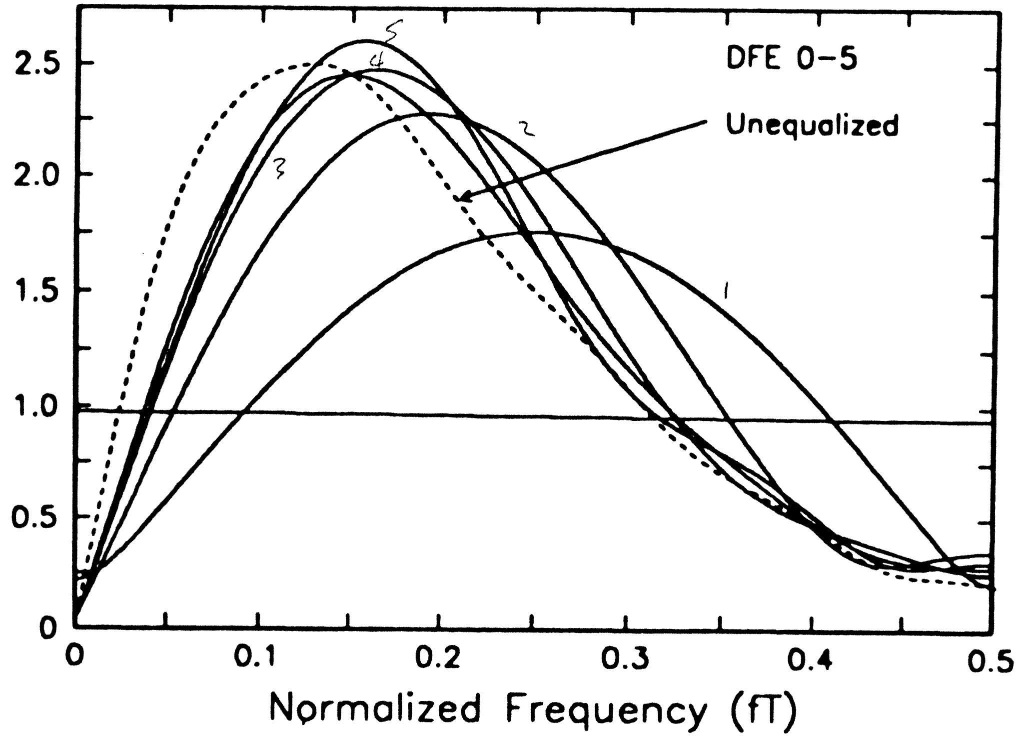
$$\mathcal{F}(\ast\, 1\text{-}D^2) = 1\text{-}e^{iw2T}$$

$$= e^{iwT}\ 2i \sin wT$$

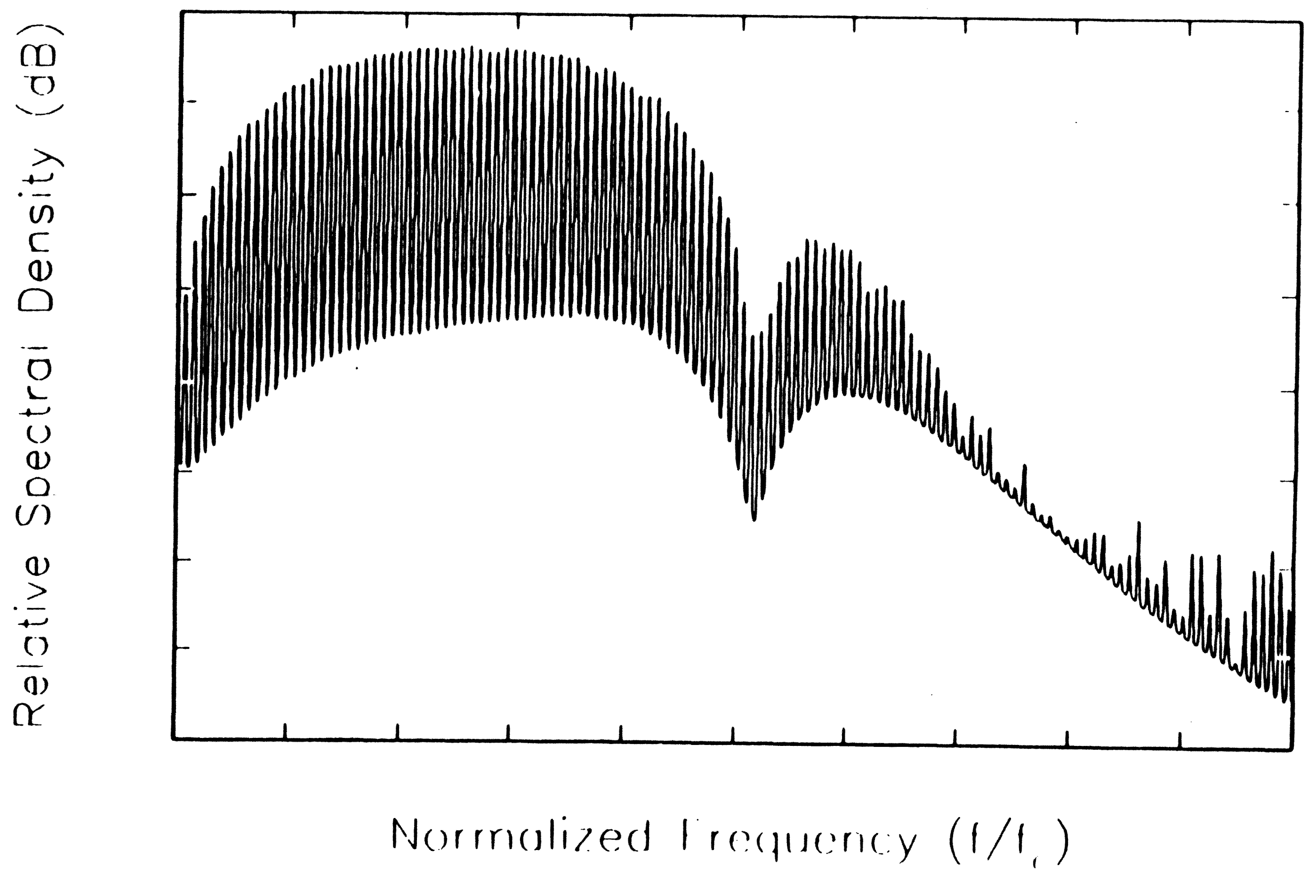
$$= e^{i2\pi fT}\ 2i \sin 2\pi fT$$

DELAY FUNCTION

3-level output: y_n = -2, 0, 2


DFE 0-5
Unequalized
2.5
2.0
1.5
1.0
0.5
0
0
0.1
0.2
0.3
0.4
0.5
Normalized Frequency (fT)
5
4
3
2
1

HOWELL D EQUPRBS3 January 24, 1990 at 17:48:16 by GDFTRN (V-88.322)



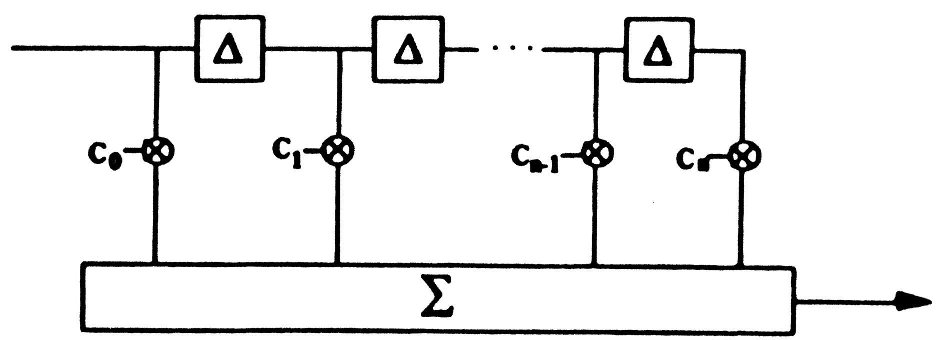
IIST 12/91

Implementation

1. R-L-C Network

$$H(w) = \frac{N(z)}{d(z)} = \frac{\pi(z-z_j)}{\pi(z-P_j)}\Bigg|_{z=iw}$$

2.



$$H(w) = \int (\sum_k c_k \partial(t-k\Delta))$$

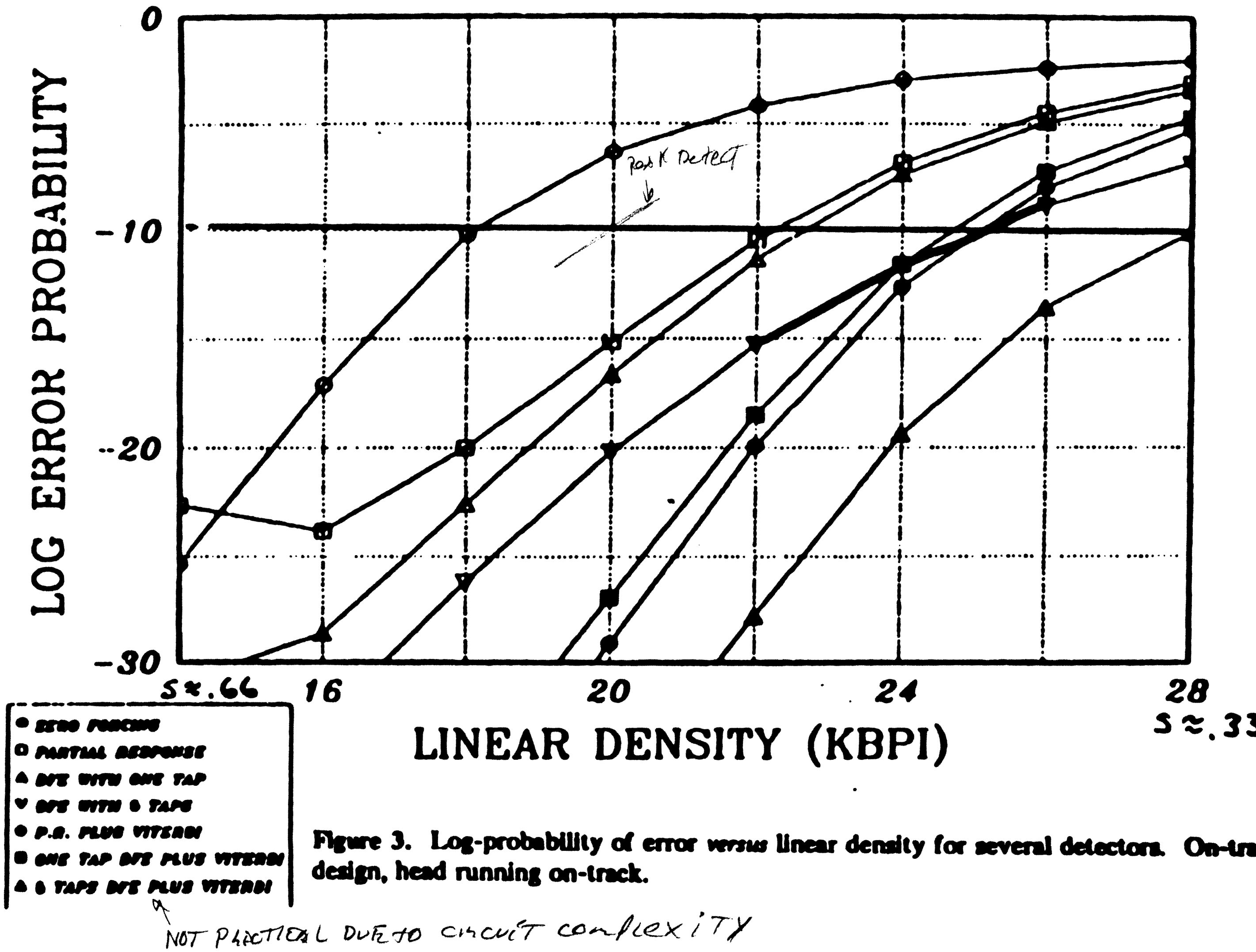
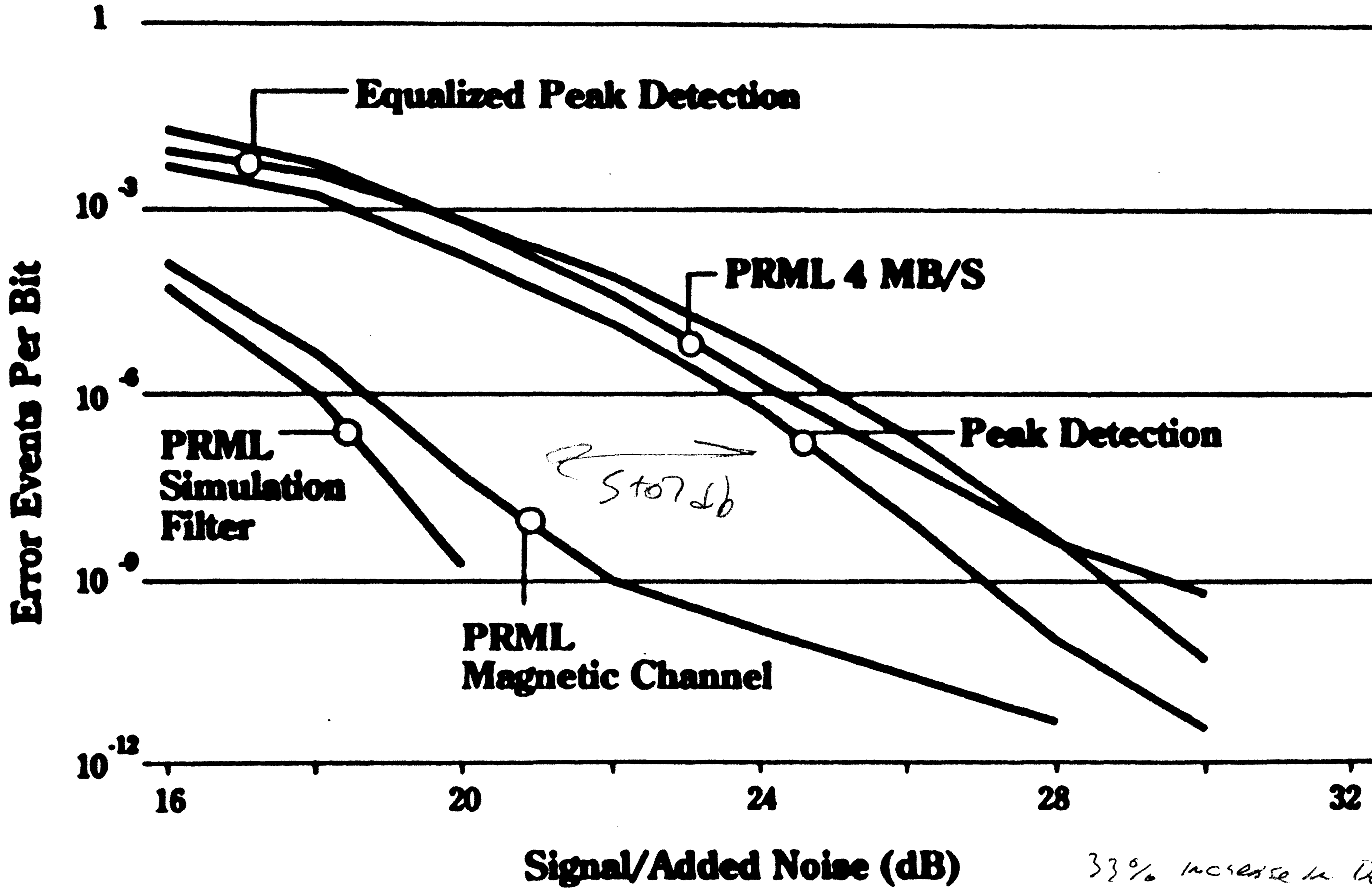


Figure 3. Log-probability of error *versus* linear density for several detectors. On-track design, head running on-track.

Model Results On-Track



33% increase in density
at same error rate.

Conclusions

Best aternatives are PRML and DFE

<u>Compared wtith the best peak detector, they offer:</u>

- **25 - 40% linear density improvement at the same error rate and noise level or...**
- **5 - 7 dB more noise tolerance at the same linear density and error rate or...**
- **Several orders of magnitude improvement in on-track error rate at given linear density and noise.**

The Read/Write Channel:

Opportunities for Digital Signal Processing

Tom Howell
Quantum Corporation

IIST
December 1991

Outline

1. Review of Peak Detection
2. Sampling Detection
3. Gain and timing control
4. Equalization
5. Performance

Outline

1. Review of Peak Detection

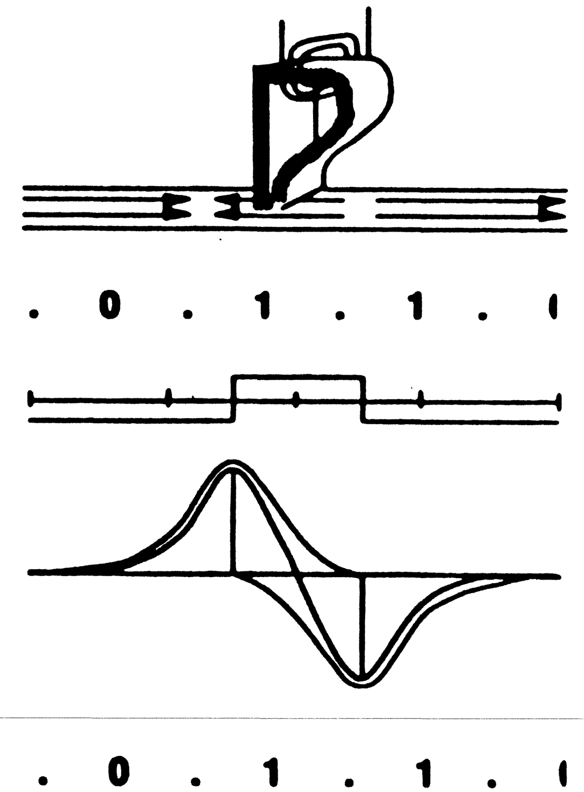
2. Sampling Detection

3. Gain and timing control

4. Equalization

5. Performance

Digital Magnetic Recording Channel



Causes of bit detection errors

- Random noise
- Pulse crowding
  (1's close together)
- Loss of clock synchronization
  (1's far apart)

Comparison of RLL (D,K) Constraints

<table>
<tr><td>Data:</td><td colspan="6">1</td><td colspan="6">1</td><td colspan="6">0</td><td colspan="6">0</td></tr>
<tr><td>FM:</td><td colspan="3">1</td><td colspan="3">1</td><td colspan="3">1</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">1</td></tr>
<tr><td>MFM:</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">1</td></tr>
<tr><td>(2,7):</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">1</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">0</td><td colspan="3">0</td></tr>
<tr><td>(1,7):</td><td colspan="4">1</td><td colspan="4">0</td><td colspan="4">1</td><td colspan="4">0</td><td colspan="4">0</td><td colspan="4">0</td></tr>
</table>

FM → MFM → (2,7) Same clock, reduced pulse crowding

(1,7) vs (2,7) Involves trade-offs

Outline

1. Review of Peak Detection

2. Sampling Detection

3. Gain and timing control

4. Equalization

5. Performance

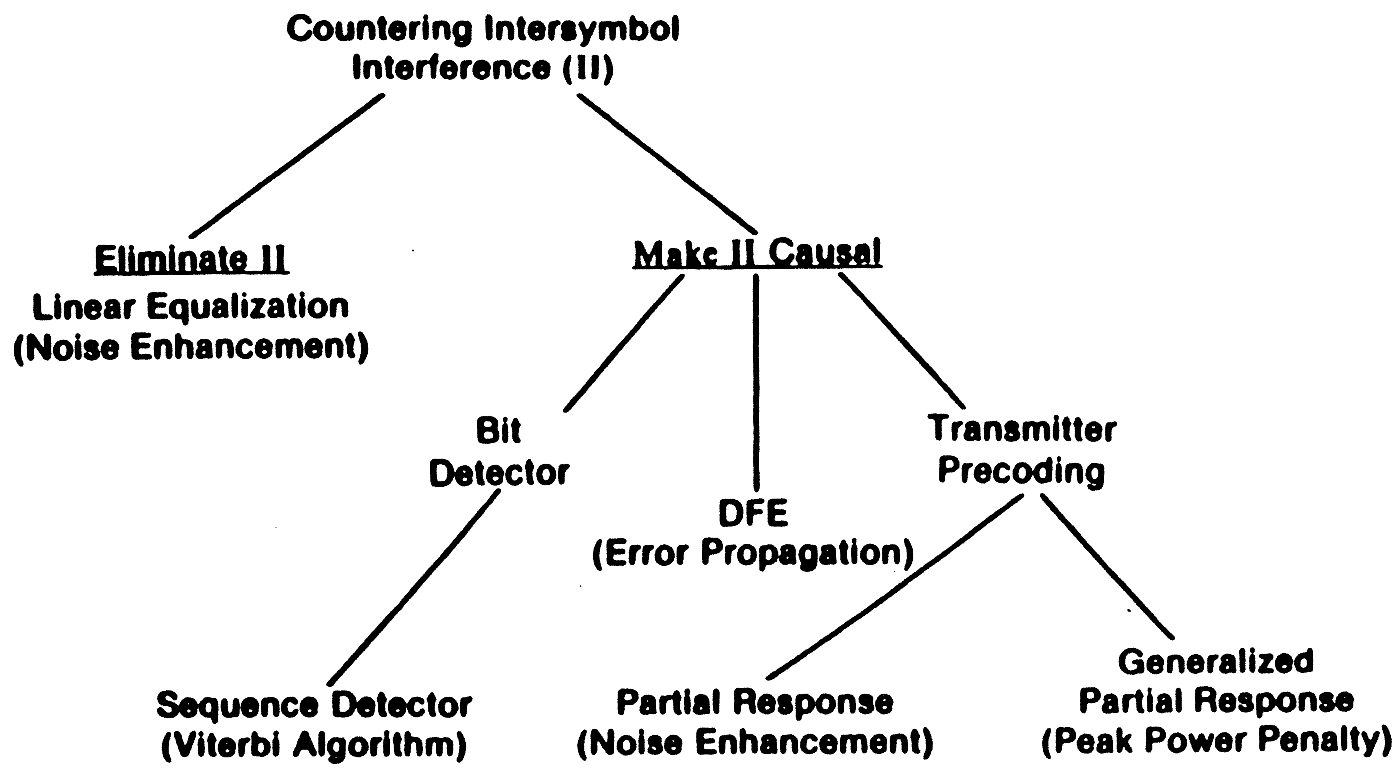
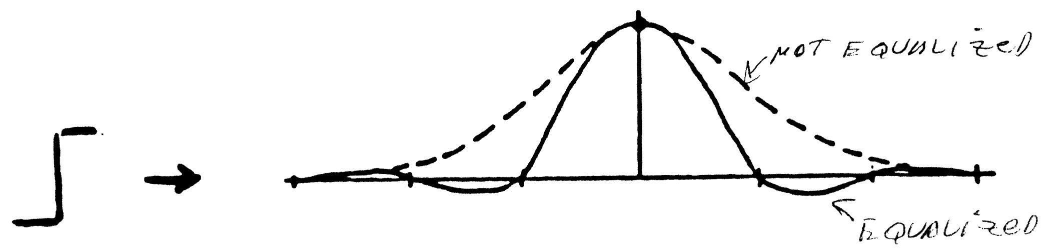
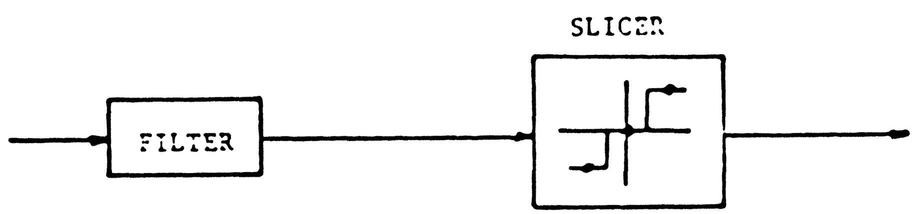


Figure 1. Summary of available methods of countering intersymbol interference in sampling detectors.

Zero-Forcing Equalization

- Equalize step response to:

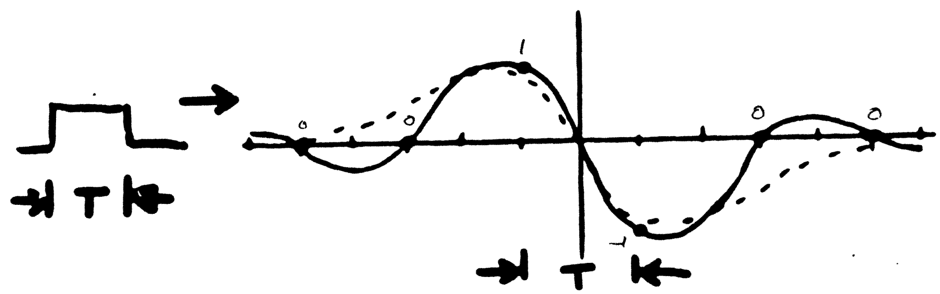


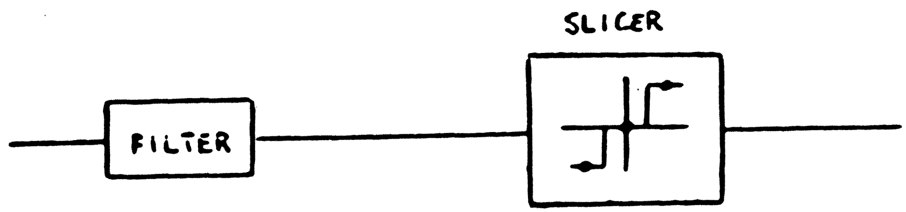


- limited by noise enhancement

Zero-Forcing Equalization

- Equalize NRZ bit response to:

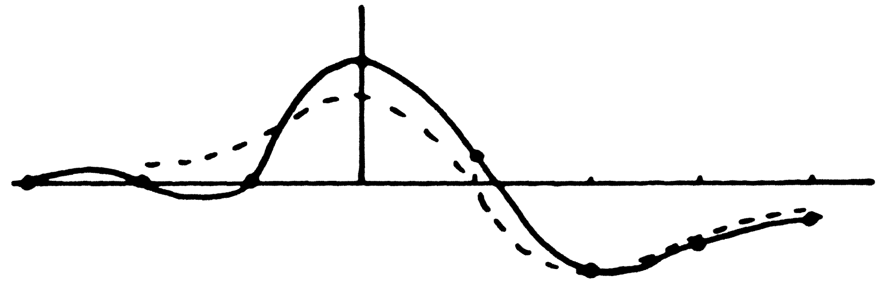




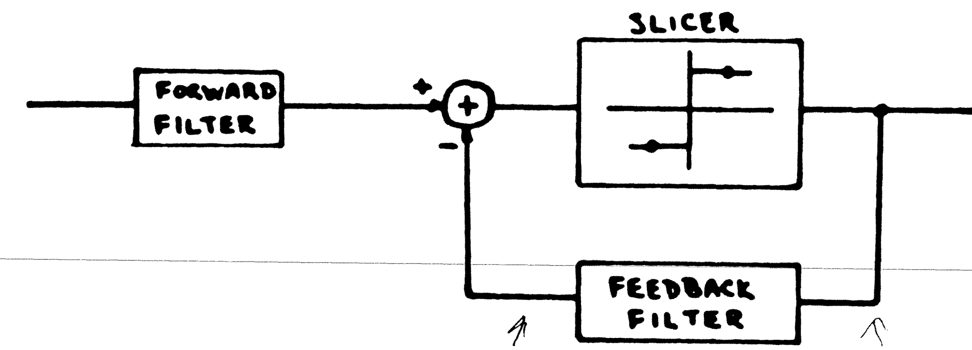
- limited by noise enhancement

Decision Feedback Equalization

- Equalize NRZ bit response to: ~~SS~~ BETTER SNR



PRODUCES MUCH LESS ERRORS; LENGTH OF ERRORS LONG.

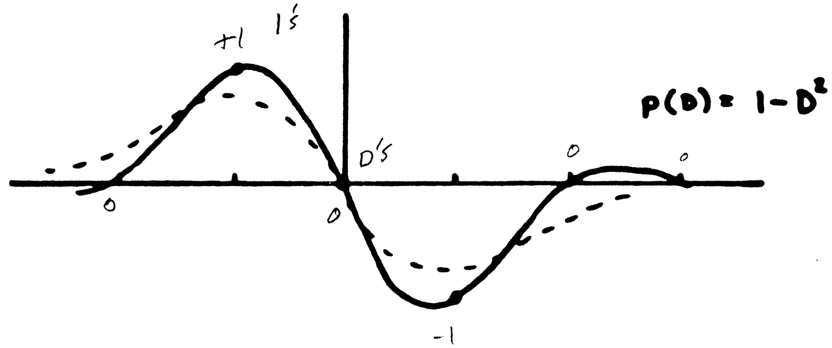


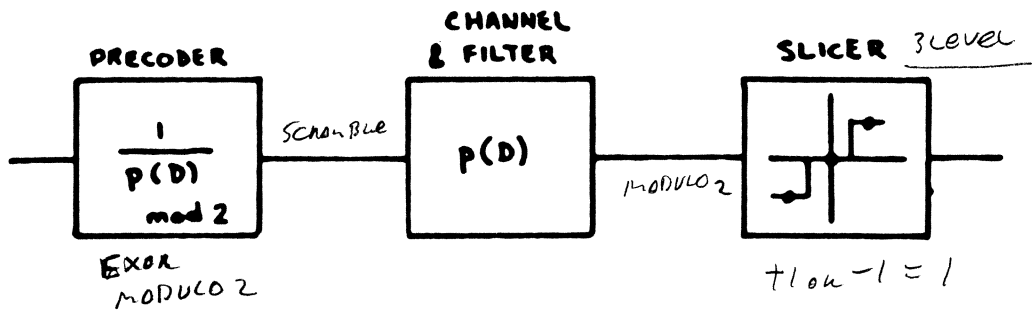
CANCEL INTERFERENCE
INTERFERENCE

- subject to error propagation

Partial Response

- Equalize NRZ bit response to:





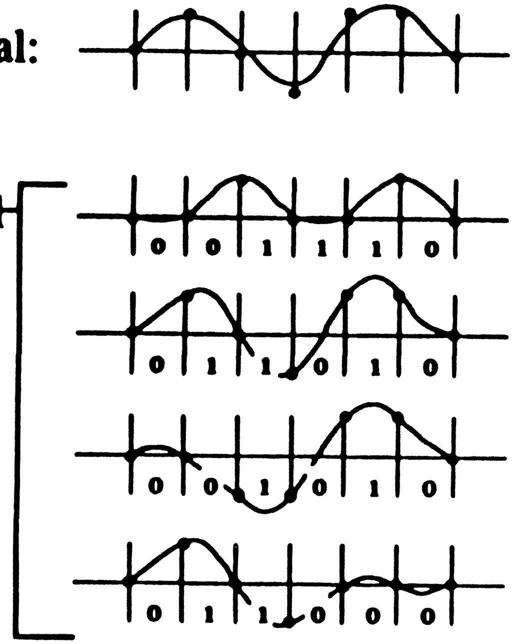
- no error propagation
- less noise enhancement than ZFE or Flat
- more noise enhancement than DFE

3db of noise immunity compared to Peak Detection method. (take as much noise)

Maximum Likelihood Sequence Detector

Received Signal:

Compare to All



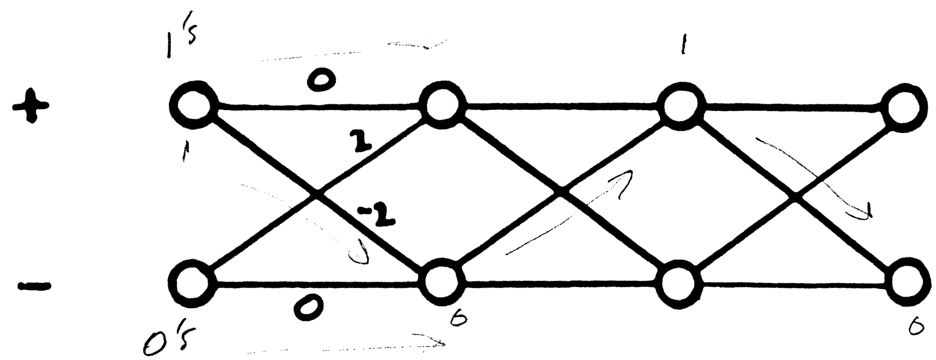
Best Match

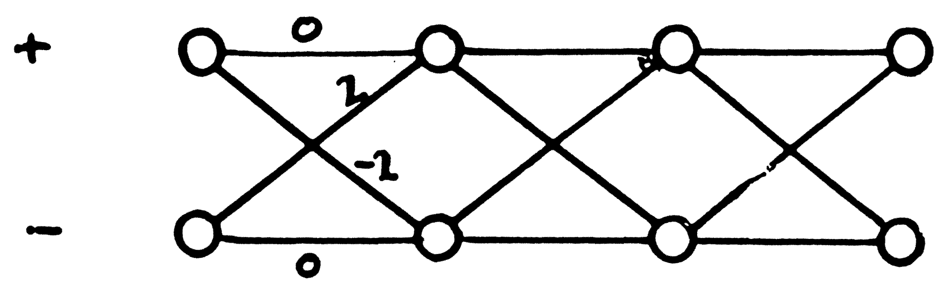
Most likely information sequence:

. . . 0 1 1 0 1 0 . . .

Trellis Diagram

1010





Viterbi Algorithm Path Metrics

y_n = INPUT SAMPLE, SUBTRACT IDEAL SAMPLE VALUE

SQUARE

ACCUMULATING SUM OF SQUARES

$$J_n(+1) = \min \{J_{n-2}(+1) + (y_n - 0)^2, J_{n-2}(-1) + (y_n - 2)^2\}$$

$$J_n(-1) = \min \{J_{n-2}(+1) + (y_n + 2)^2, J_{n-2}(-1) + (y_n - 0)^2\}$$

The Recursive Algorithm

DIFF. SUM of SQUARES USED:

Decision

Previous sum of squares

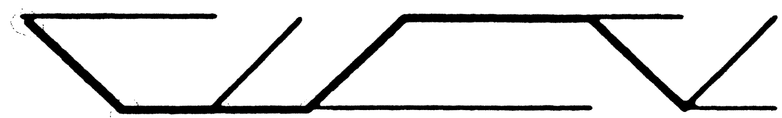
compare

$$DJ_n = \begin{cases} y_n + 1 \text{ if } +1 < (DJ_{n-2} - y_n) \\ DJ_{n-2} \text{ if } -1 < (DJ_{n-2} - y_n) < +1 \\ y_n - 1 \text{ if } (DJ_{n-2} - y_n) < -1 \end{cases}$$

WHAT IS TRUE?

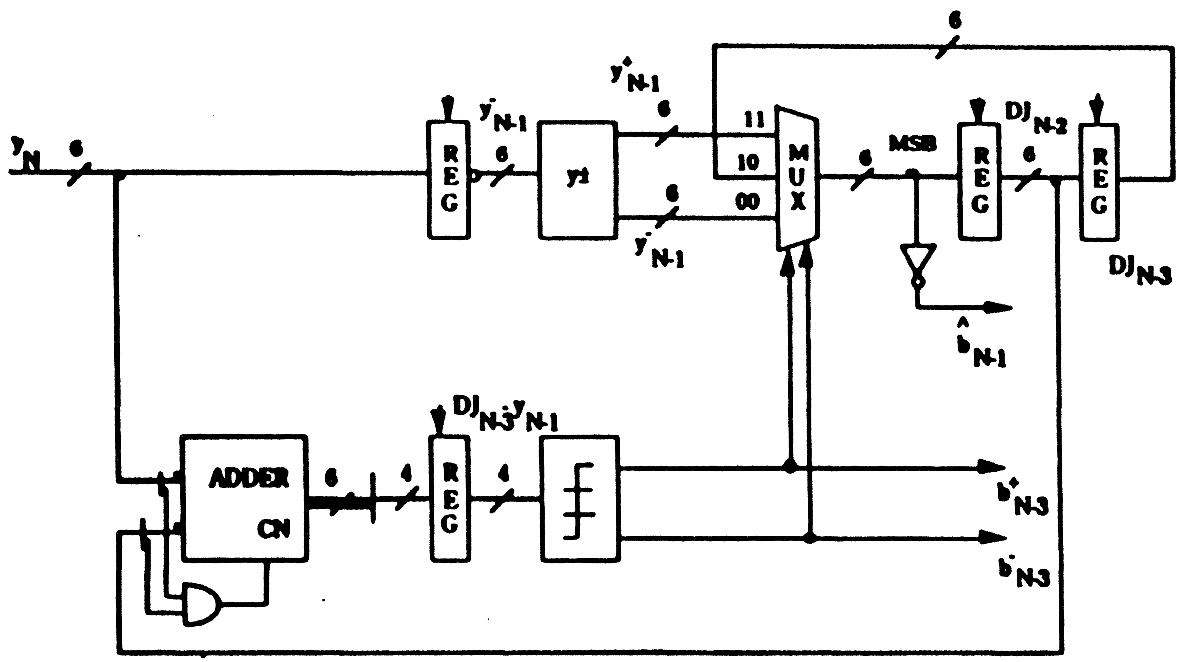
Enter truth

Example:



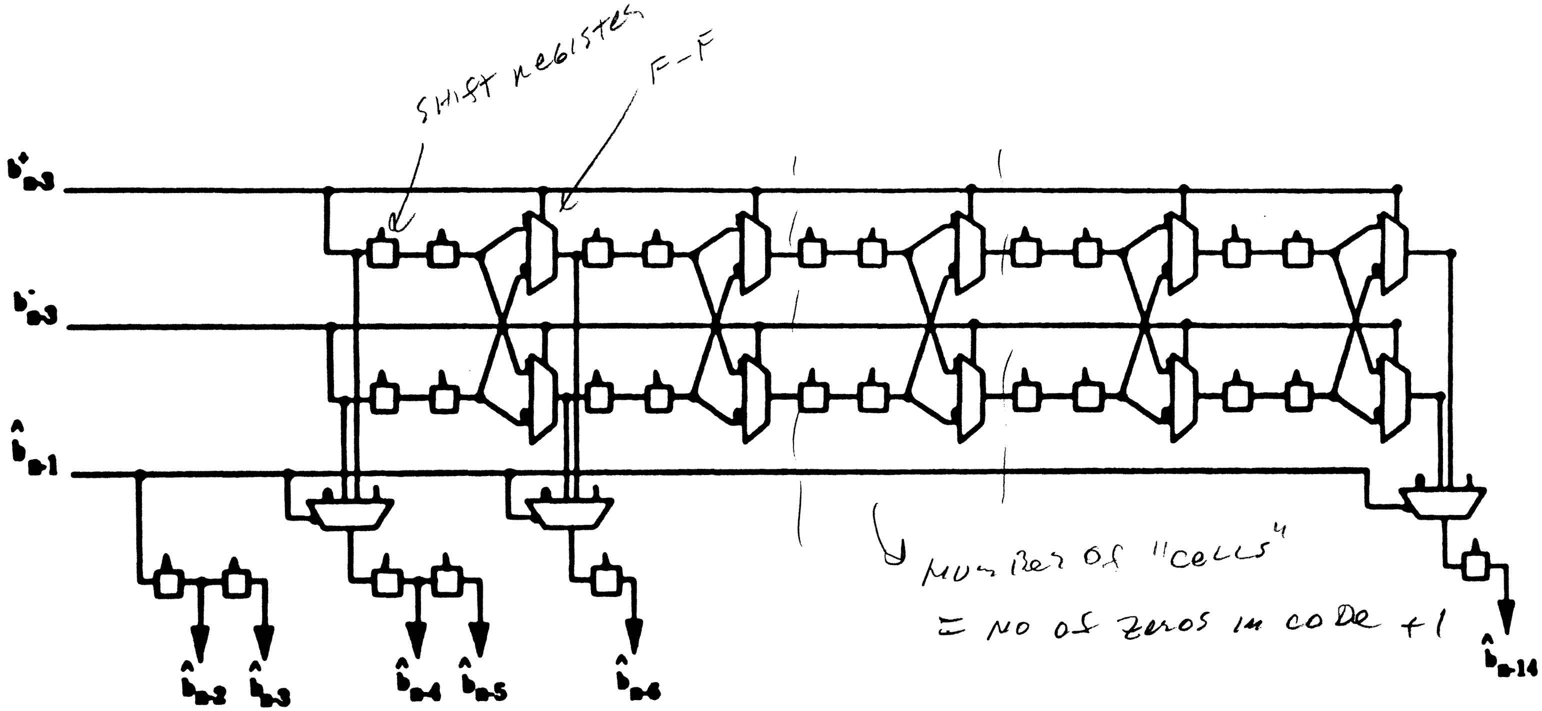
1 0 0 0 1 1 1 0

Viterbi Detector Metric Calculation



Two's complement representation is used.
Most significant bit (MSB) is at the top or left.

Path Memory


SHIFT REGISTERS
F-F
$\hat{b}_{n-1}$
$\hat{b}_{n-2}$
$\hat{b}_{n-3}$
$\hat{b}_{n-4}$
$\hat{b}_{n-5}$
$\hat{b}_{n-6}$
$\hat{b}_{n-14}$
NUMBER OF "CELLS"
= NO OF ZEROS IN CODE +1

Outline

1. Review of Peak Detection

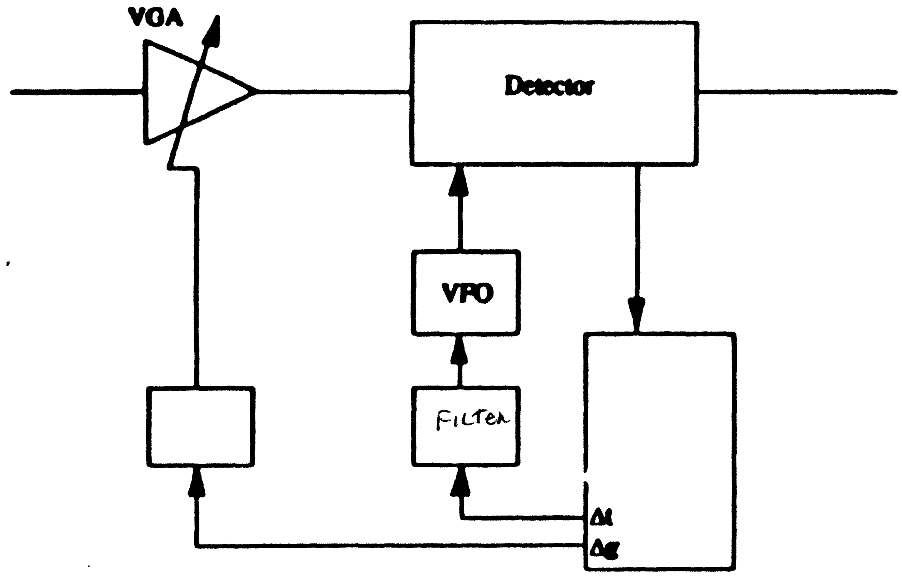
2. Sampling Detection

3. Timing and gain control

4. Equalization

5. Performance

Timing and Gain Control



Timing and Gain Control for PRML

$$\hat{y}_n = \hat{a}_n - \hat{a}_{n-2}$$

$$\hat{\dot{y}}_n = \hat{y}_{n+1} - \hat{y}_{n-1}$$

$$e_n = y_n - \hat{y}_n$$

$$\Delta g_n = e_n \hat{y}_n$$

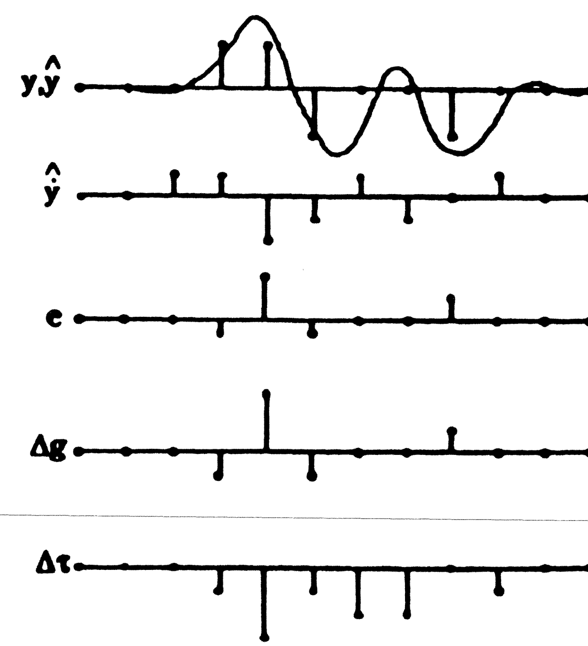
$$\Delta \tau_n = e_n \hat{\dot{y}}_n$$

$$\Delta T_{n+1} = \Delta T_n + \tau \Delta \tau_n$$

$$\tau_{n+1} = \tau_n - \beta \Delta \tau_n - \Delta T_n$$

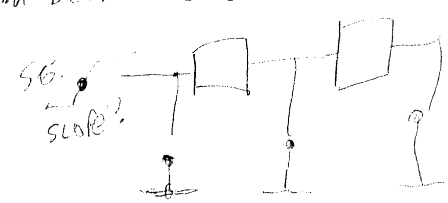
$$g_{n+1} = g_n - \gamma g \Delta g_n$$

Example:



Sample values are constant

Peak defines 2 delay line

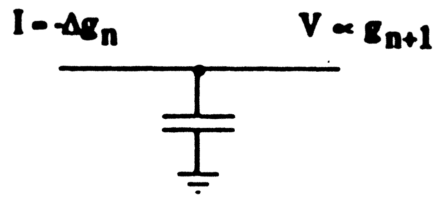


Filtering the Error Signals

CHARGE COUPLED
LOGIC implementation!

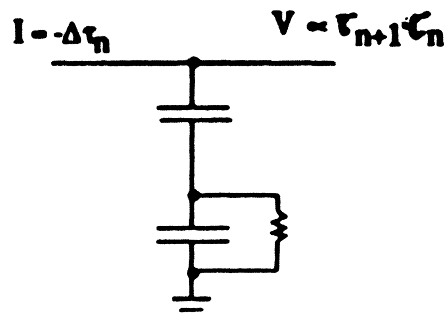
$$g_{n+1} = g_n - \gamma \Delta g_n$$

DIGITAL



ANALOG

$$\Delta T_{n+1} = \Delta T_n + \zeta \Delta \tau_n$$
$$\tau_{n+1} = \tau_n - \beta \Delta \tau_n - \Delta T_n$$



Outline

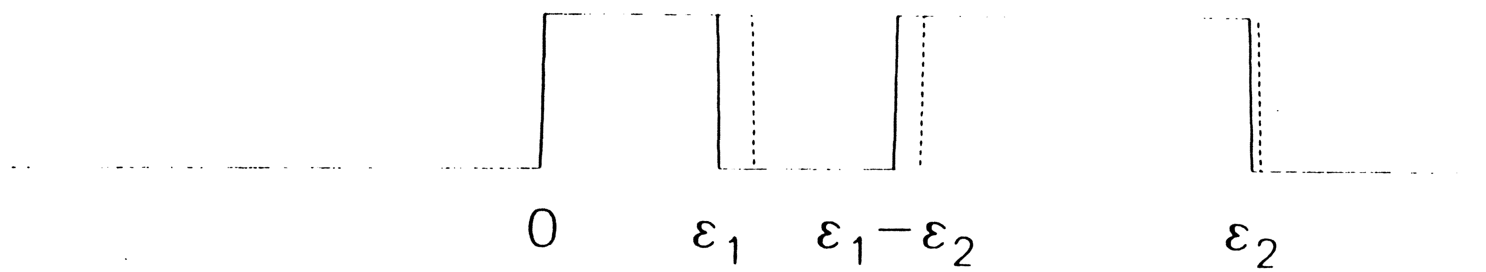
1. Review of Peak Detection

2. Sampling detection

3. Gain and timing control

4. Equalization

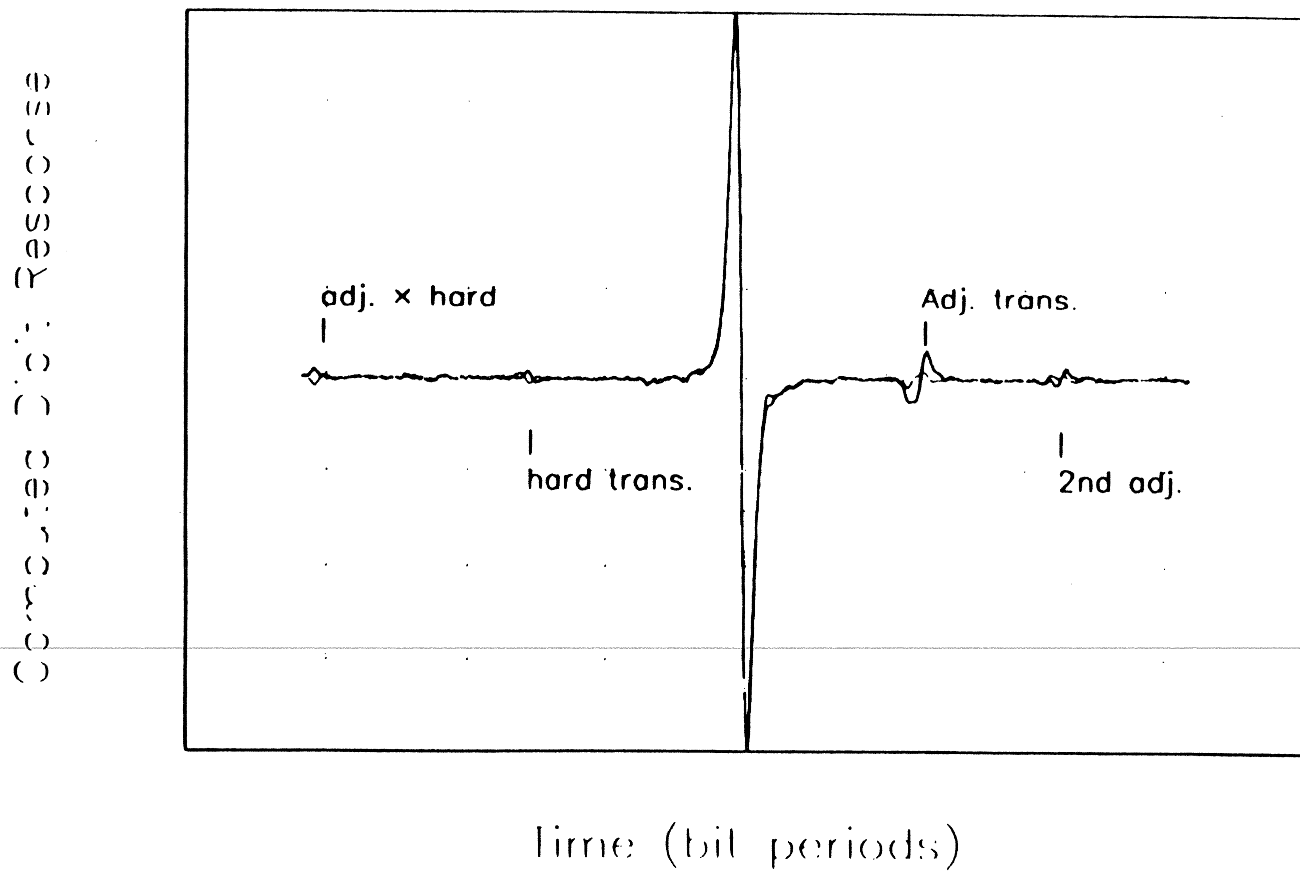
5. Performance



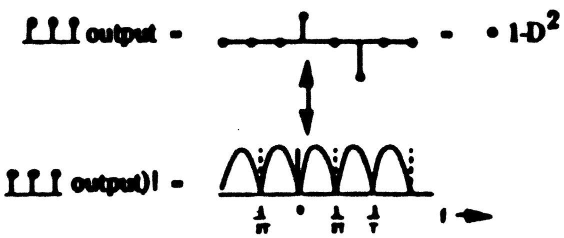
Nominal write current

Precompensated write current

HOWELL D EC126327 May 7, 1990 at 16:08:15 by GDFUGT (V-90.033)



Class IV (Modified Duobinary)



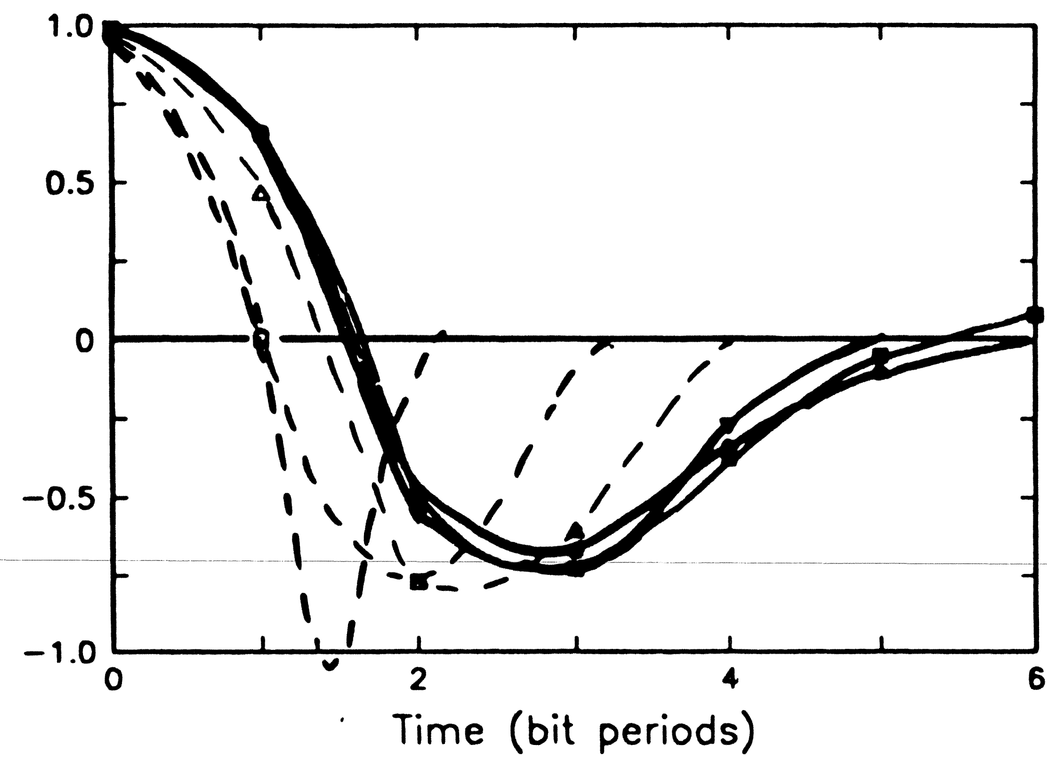
$$\mathcal{F}(\delta * 1\text{-}D^2) = 1 - e^{iw2T}$$
$$= e^{iwT}\ 2i \sin wT$$
$$= e^{i2\pi fT}\ 2i \sin 2\pi fT$$

DELAY FUNCTION

3-level output: $y_n = -2, 0, 2$

Sampled NRZ BIT Responses

1 - 6 Feedback Taps



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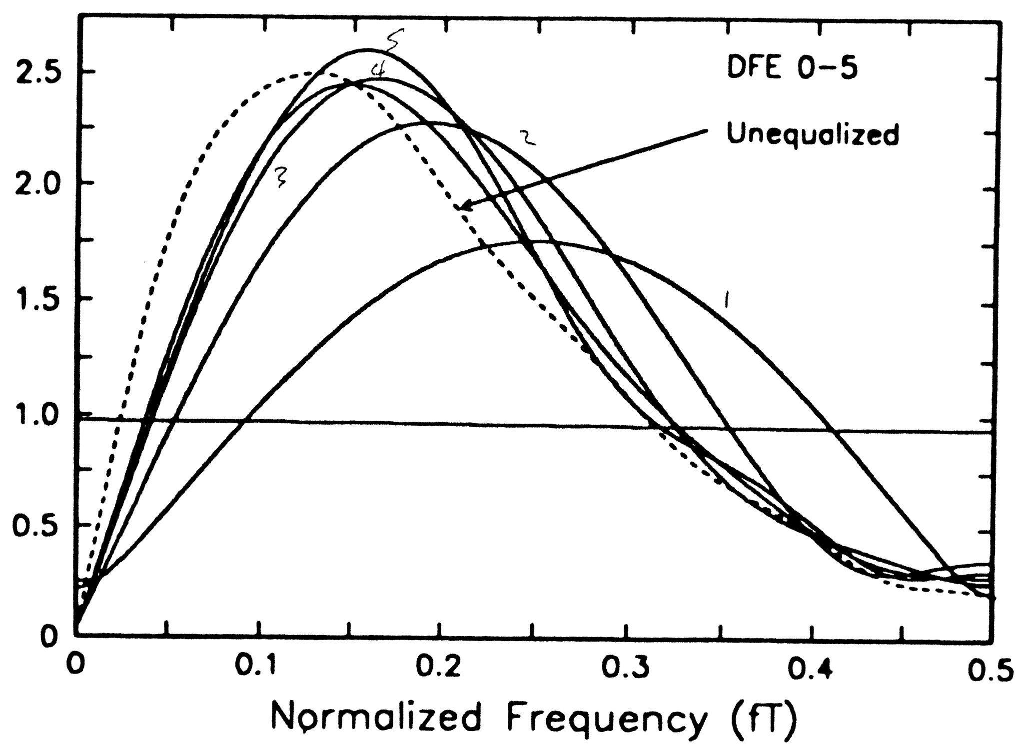
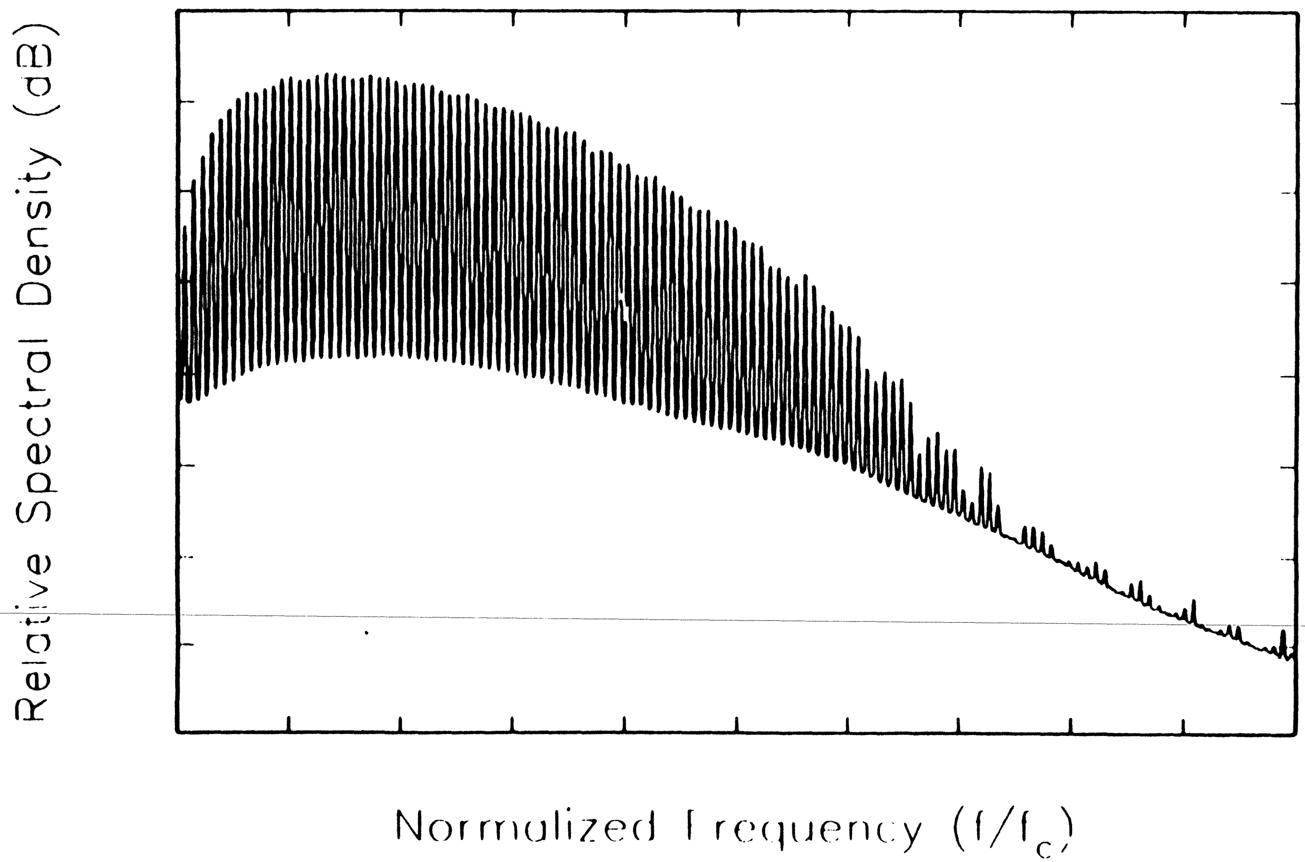
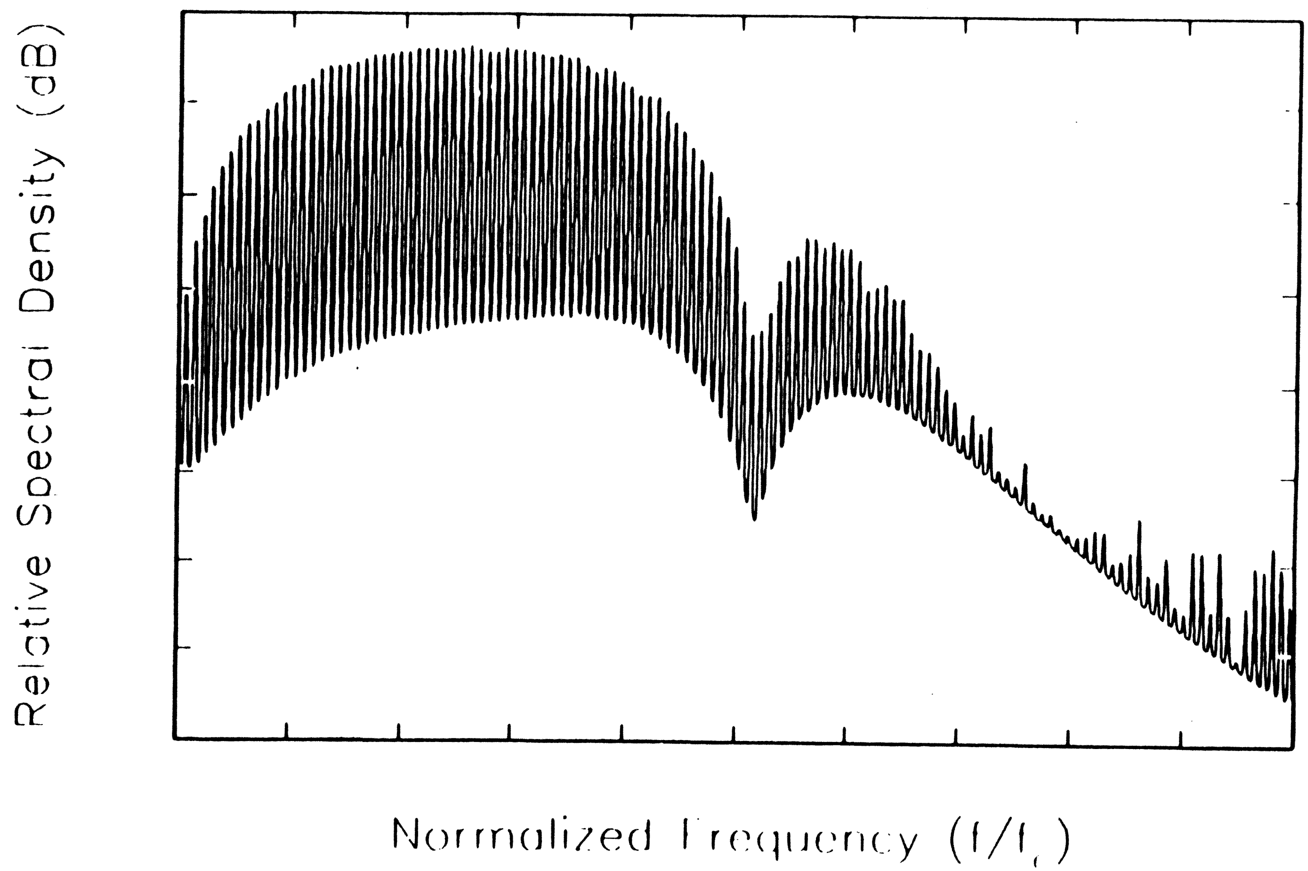

DFE 0-5
Unequalized
5
4
3
2
1
2.5
2.0
1.5
1.0
0.5
0
0
0.1
0.2
0.3
0.4
0.5
Normalized Frequency (fT)

HOWELL D UNEPRBS3 January 24, 1990 at 17:48:00 by GDFTRN (V-88.322)

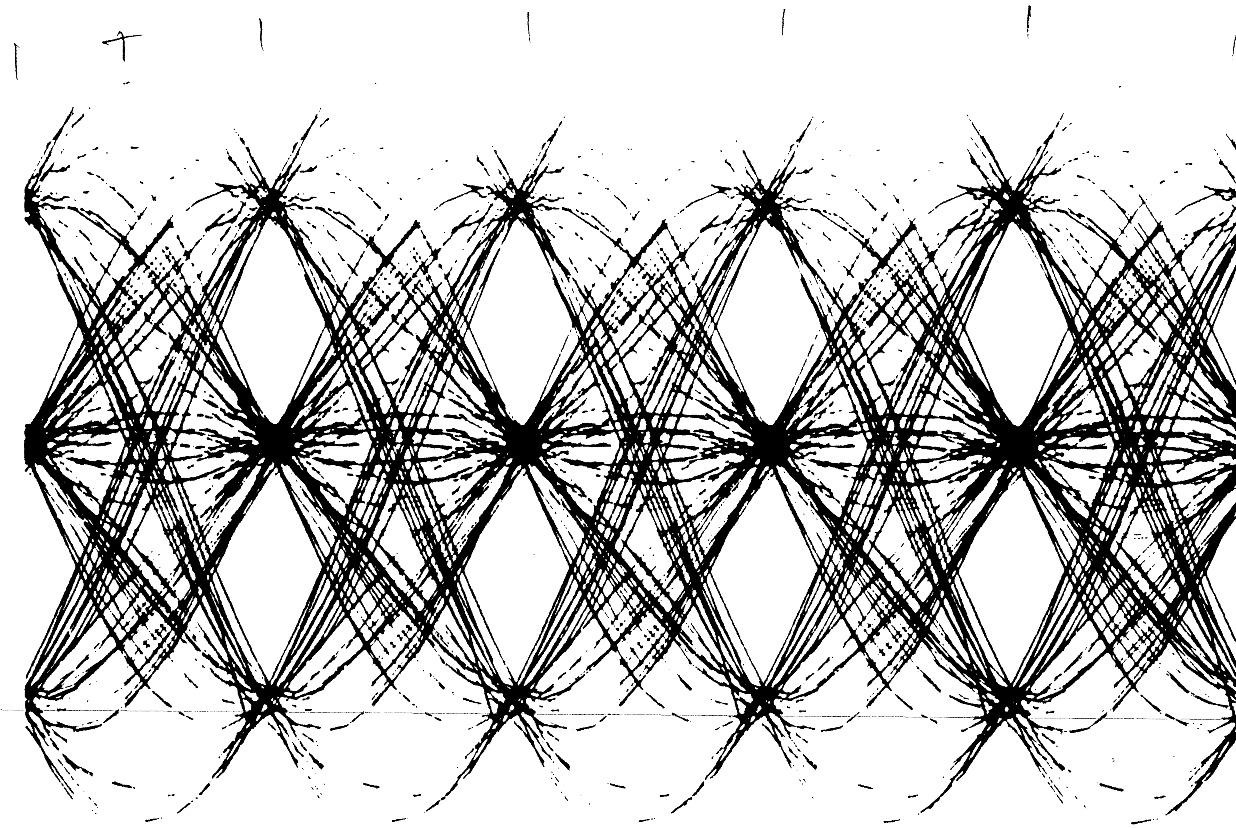


IIST 12/91

HOWELL D EQUPRBS3 January 24, 1990 at 17:48:16 by GDFTRN (V-88.322)



IIST 12/91



5T

6001) EQUALIZER RESPONSE
TO WIDE BAND. INPUT.

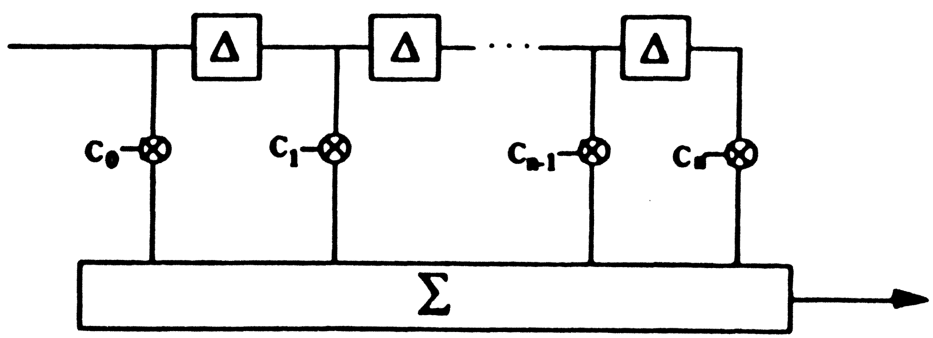
IIST 12/91

Implementation

1. R-L-C Network

$$H(w) = \frac{N(z)}{d(z)} = \frac{\pi(z-z_j)}{\pi(z-P_j)}\Bigg|_{z=iw}$$

2.



$$H(w) = f\left(\sum_k c_k \delta(t-k\Delta)\right)$$

Outline

1. Review of Peak Detection
2. Sampling Detection
3. Gain and timing control
4. Equalization
5. *Performance*

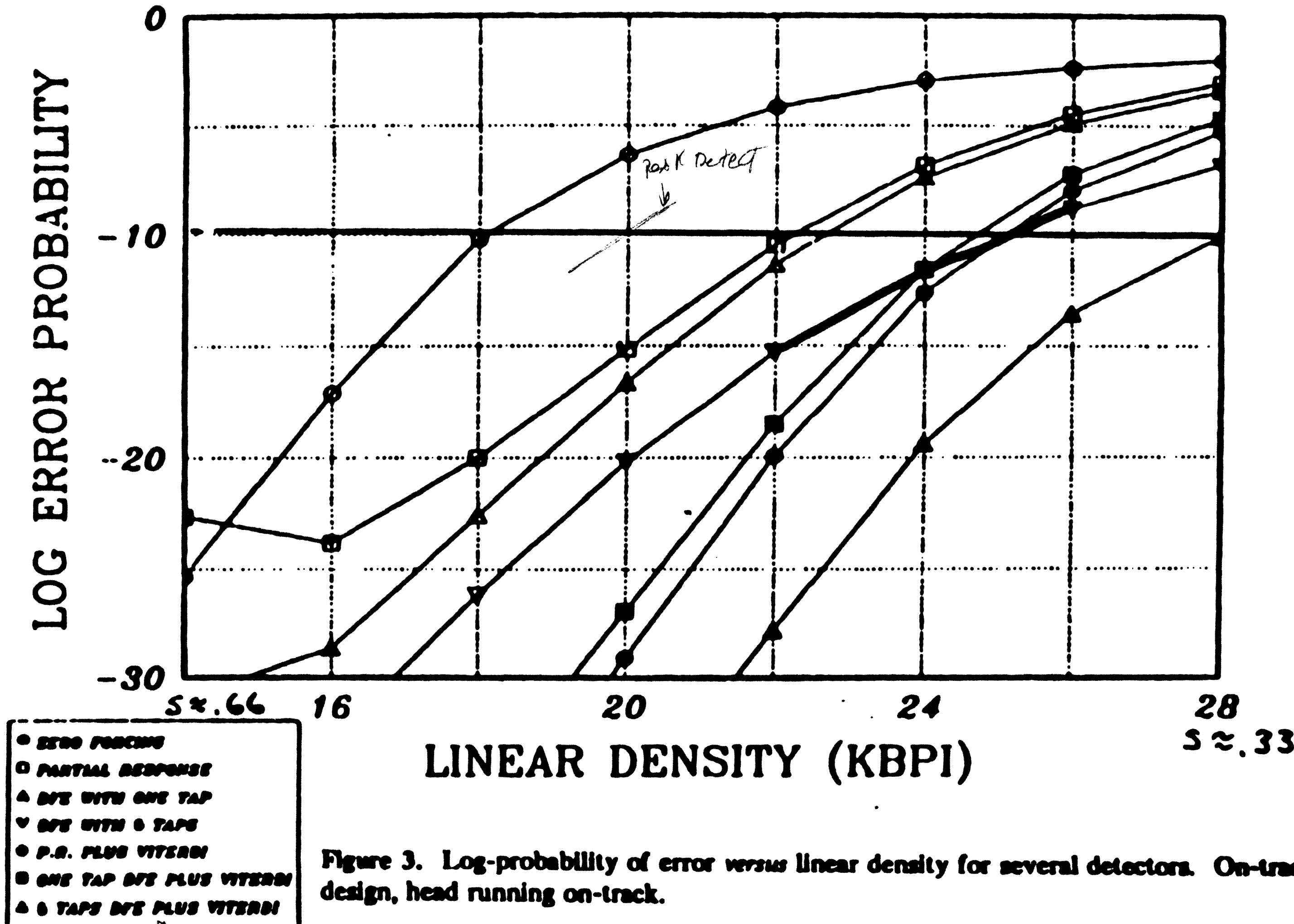
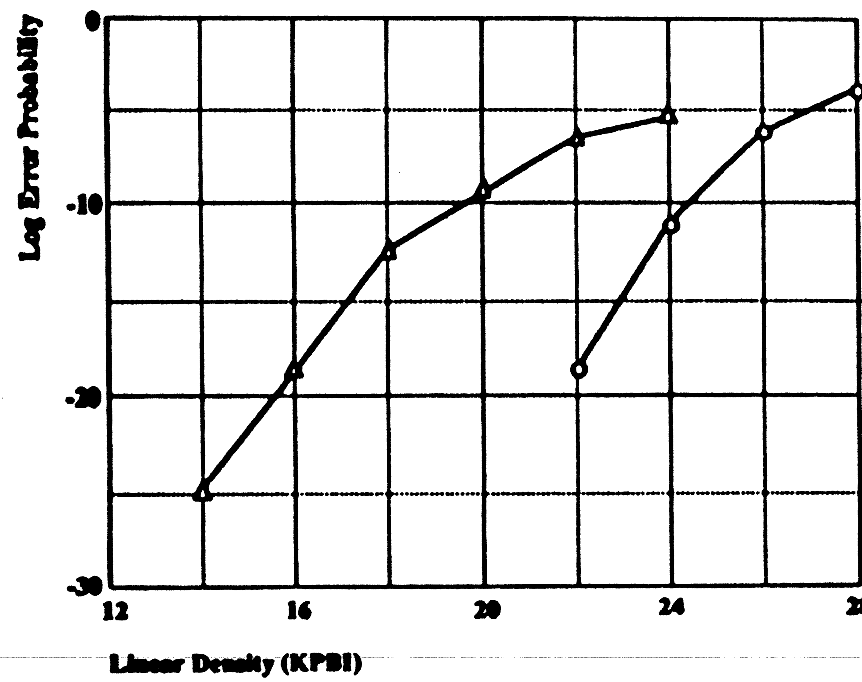


Figure 3. Log-probability of error *versus* linear density for several detectors. On-track design, head running on-track.

NOT PRACTICAL DUE TO CIRCUIT COMPLEXITY

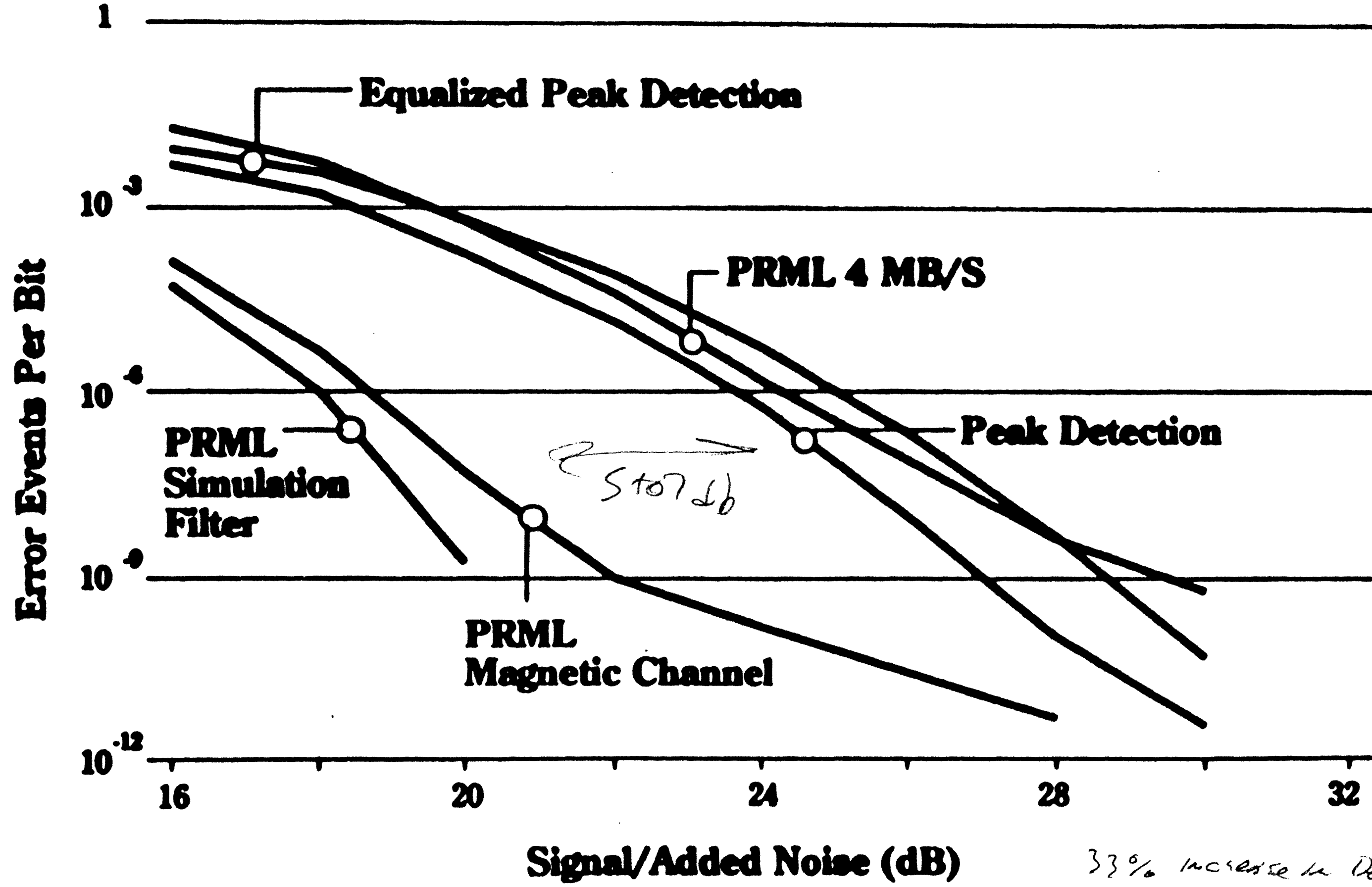
Performance of Channel Alternatives



▲ (1,7) Code Equalized

○ P. R. Max. Likelihood

Model Results On-Track



33% increase in Density
at same Error rate.

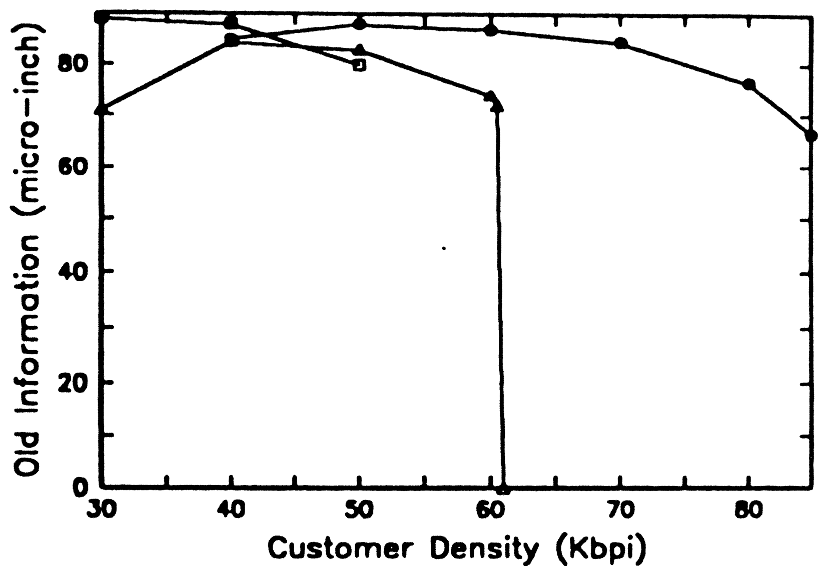


Figure 35. Old information versus linear density on MR head film disk. ○ = PRML, □ = (1,7) peak detection without equalization, Δ = (1,7) peak detection with equalization.

Conclusions

Best aternatives are PRML and DFE

Compared wtith the best peak detector, they offer:

- 25 - 40% linear density improvement at the same error rate and noise level or...
- 5 - 7 dB more noise tolerance at the same linear density and error rate or...
- Several orders of magnitude improvement in on-track error rate at given linear density and noise.

CODING FOR PARTIAL-RESPONSE CHANNELS

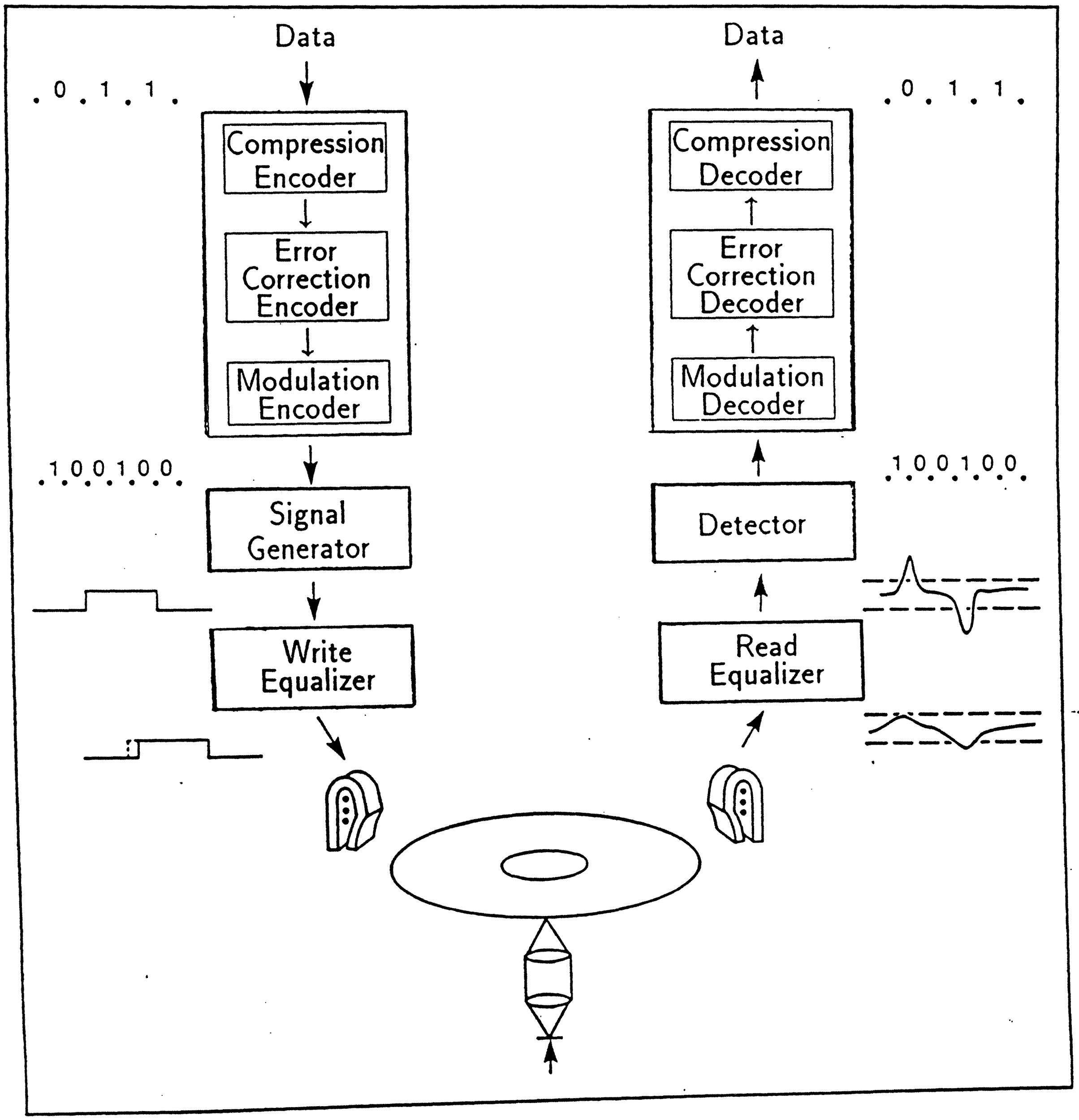
PAUL H. SIEGEL

IBM RESEARCH DIVISION
ALMADEN RESEARCH CENTER
SAN JOSE, CALIFORNIA

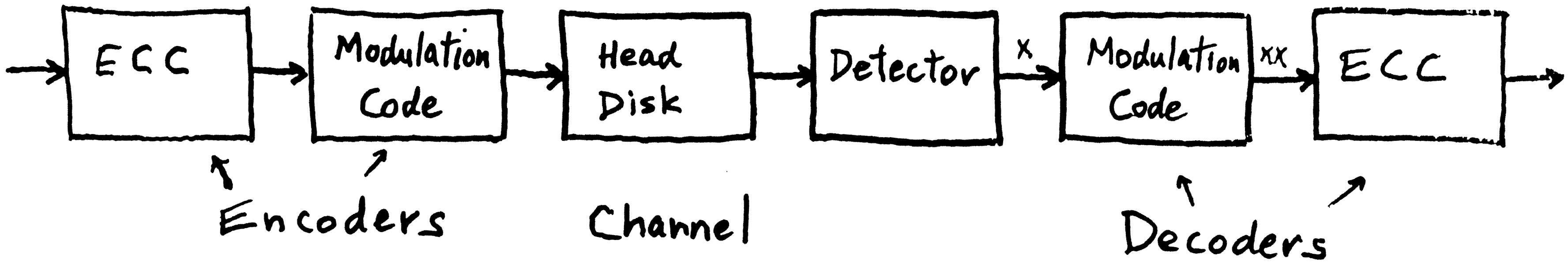
OUTLINE

- Digital recording channel
- Constrained codes for PRML
- Trellis codes for PRML

DIGITAL DATA RECORDING
(SCHEMATIC)



CONFIGURATION OF CODES



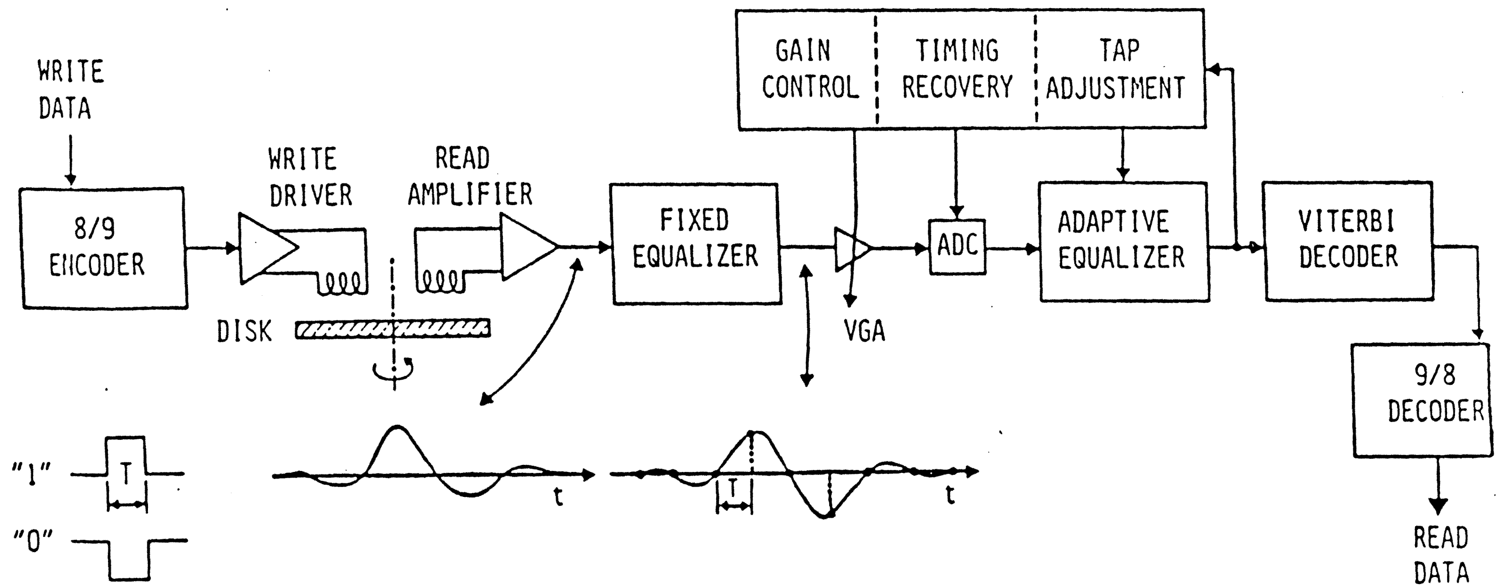
Modulation Code

Matches recording signal characteristics to channel bandwidth, detection method, read/write electronics, timing and tracking servo requirements

Error Correction Code

Detects and corrects data detection errors

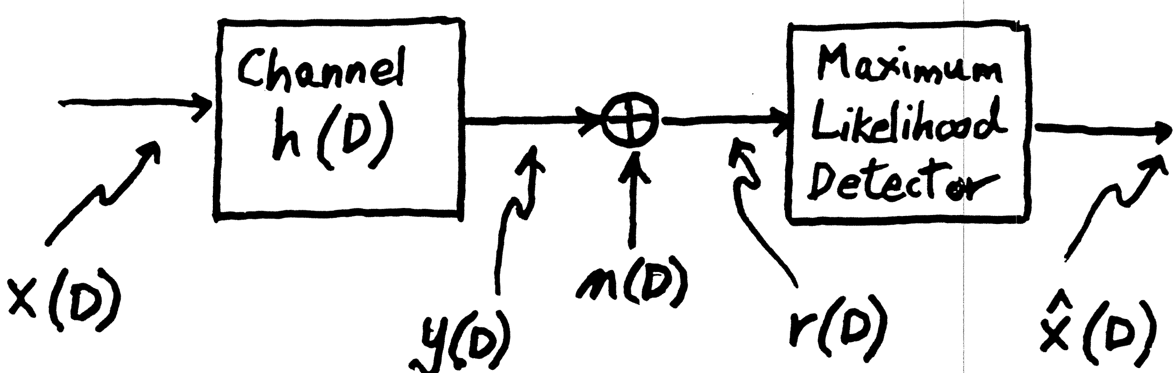
PRML Channel



PRML: PARTIAL-RESPONSE CLASS-IV SIGNALING
with MAXIMUM-LIKELIHOOD SEQUENCE DETECTION

- 30% linear density advantage over (2,7) peak detection

DIGITAL RECORDING CHANNEL



- Binary channel input

$$x(D) = \sum_{j=0}^{\infty} x_j D^j \quad ; \quad x_j \in \{0,1\}$$

- Channel linear filter model

$$h(D) = \sum_{j=0}^{N} h_j D^j \quad ; \quad \{h_j\}_0^N = \text{impulse response}$$

$$y(D) = x(D)\, h(D)$$

- Additive, i.i.d. Gaussian noise

$$n(D) = \sum_{j=0}^{\infty} n_j D^j \quad ; \quad n_j \sim N(0, \sigma^2)$$

PARTIAL-RESPONSE FILTER MODEL
FOR
RECORDING CHANNELS

- Magnetic recording

- Transfer polynomial

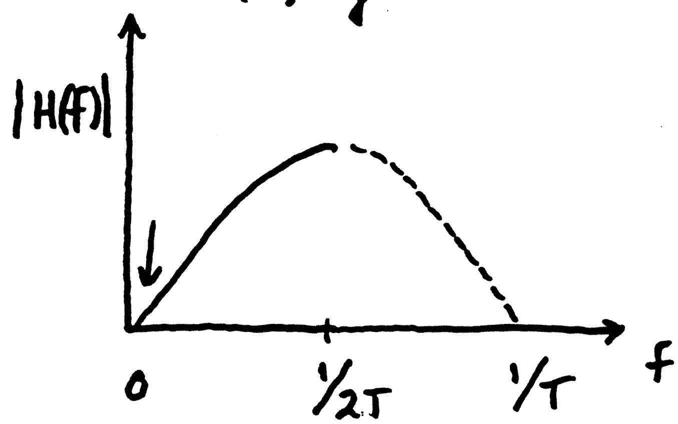
- $h(D) = 1 - D$

$(y_n = x_n - x_{n-1})$

"Dicode"

- Transfer function

$H(f) = j2T \sin \pi f T$

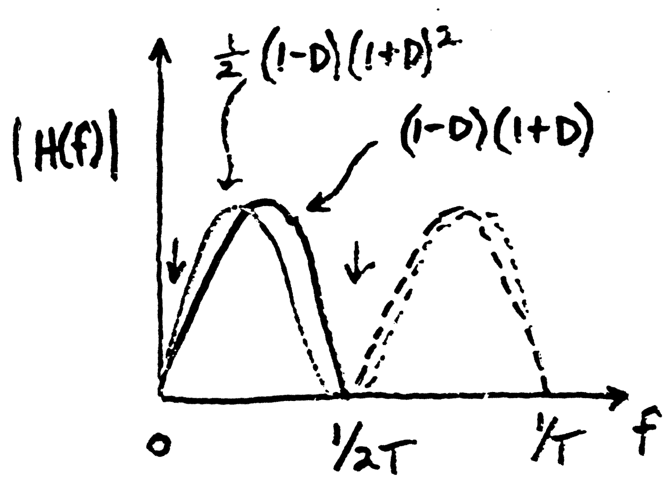


- $h(D) = \begin{cases} (1-D)(1+D) \\ (1-D)(1+D)^2 \end{cases}$

$y_n = \begin{cases} x_n - x_{n-2} \\ x_n + x_{n-1} - x_{n-2} - x_{n-3} \end{cases}$

{ "PR4"
{ "EPR4"

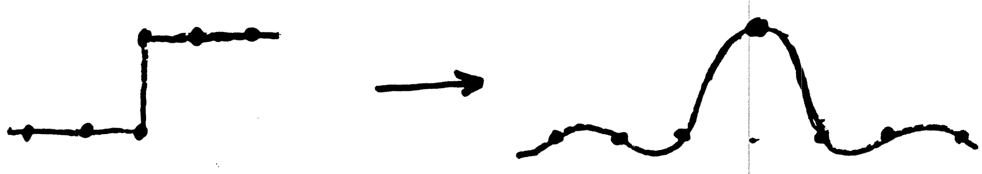
$H(f) = \begin{cases} j2T \sin 2\pi f T \\ j4T \cos \pi f T \sin 2\pi f \end{cases}$



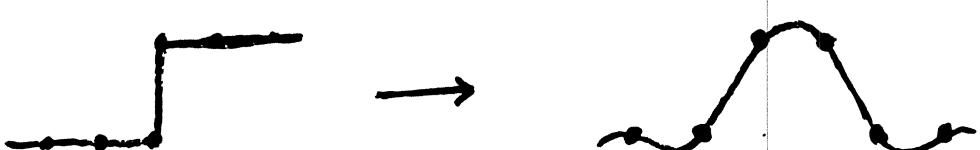
PR MODELS
(cont.)

- Magnetic recording – step responses

  - Dicode: $h(D) = 1 - D$



  - PR4: $h(D) = (1-D)(1+D) = 1 - D^2$



  - EPR4: $h(D) = (1-D)(1+D)^2 = 1 + D - D^2 - D^3$

PR Filter Models (cont.)

- Optical recording

- Transfer polynomial

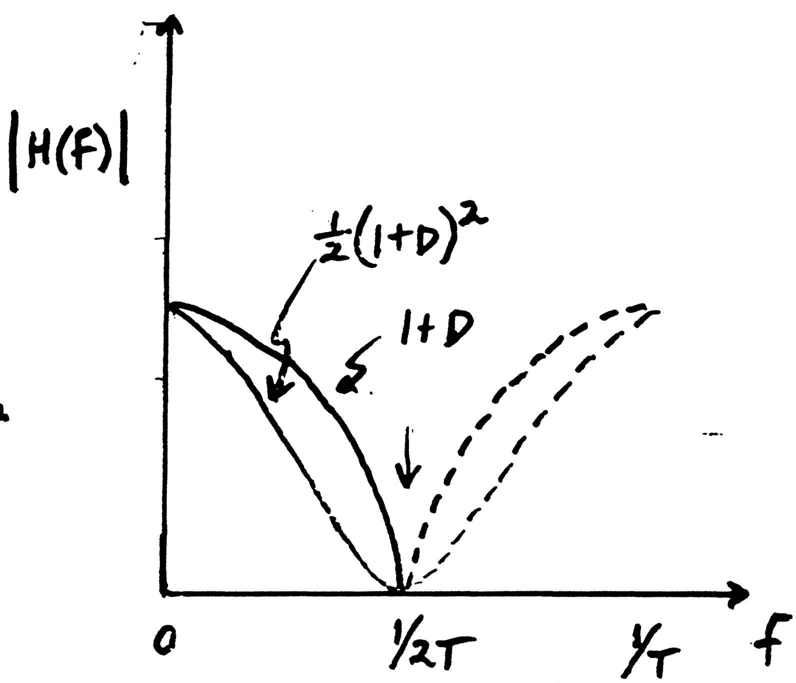
$$h(D) = \begin{cases} 1 + D \\ (1+D)^2 \end{cases}$$

$$y_n = \begin{cases} x_n + x_{n-1} \\ x_n + 2x_{n-1} + x_{n-2} \end{cases}$$

$$\begin{cases} \text{"PR1"} \\ \text{"PR2"} \end{cases}$$

- Transfer function

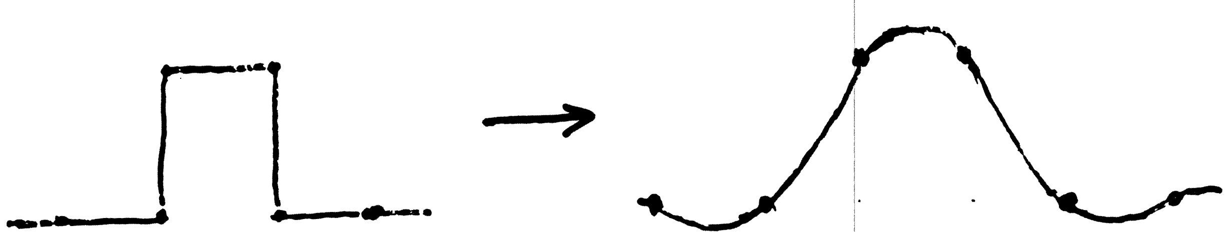
$$H(f) = \begin{cases} 2T \cos \pi f T \\ 4T \cos^2 \pi f T \end{cases}$$



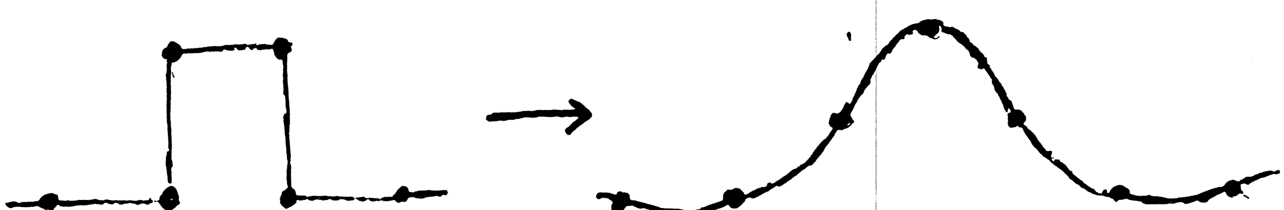
PR Models
(cont.)

- Optical recording - pulse responses

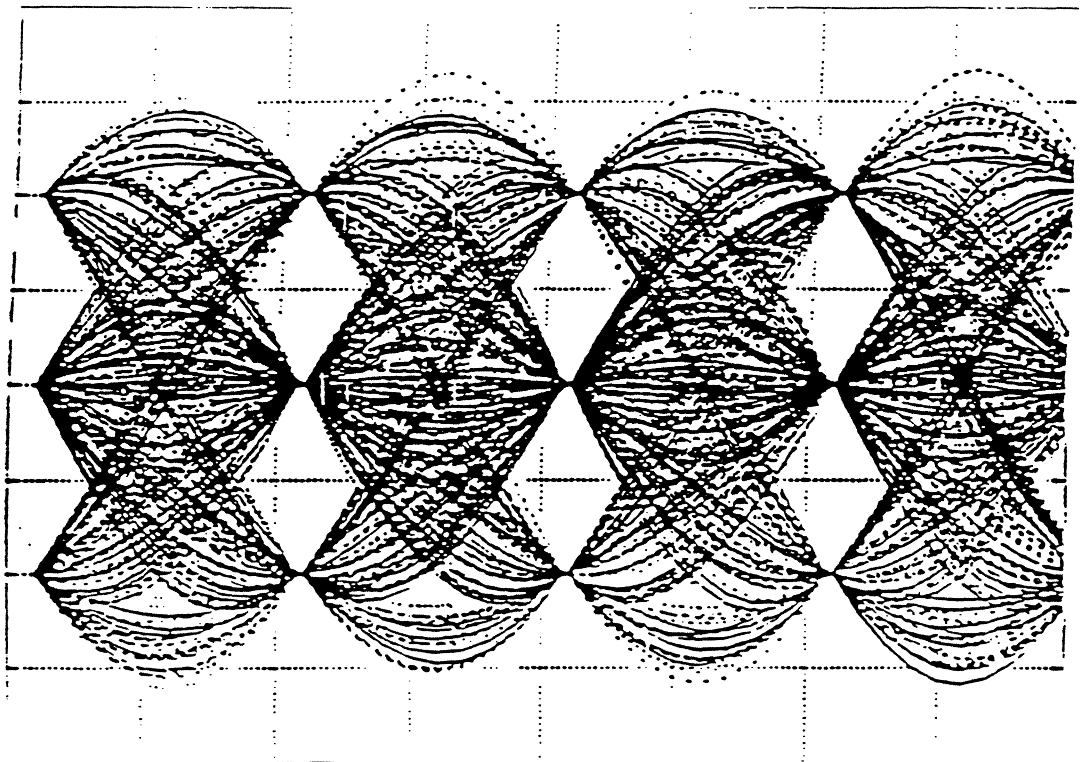
  - PR 1 (duobinary): $h(D) = 1+D$



  - PR 2 : $h(D) = (1+D)^2$

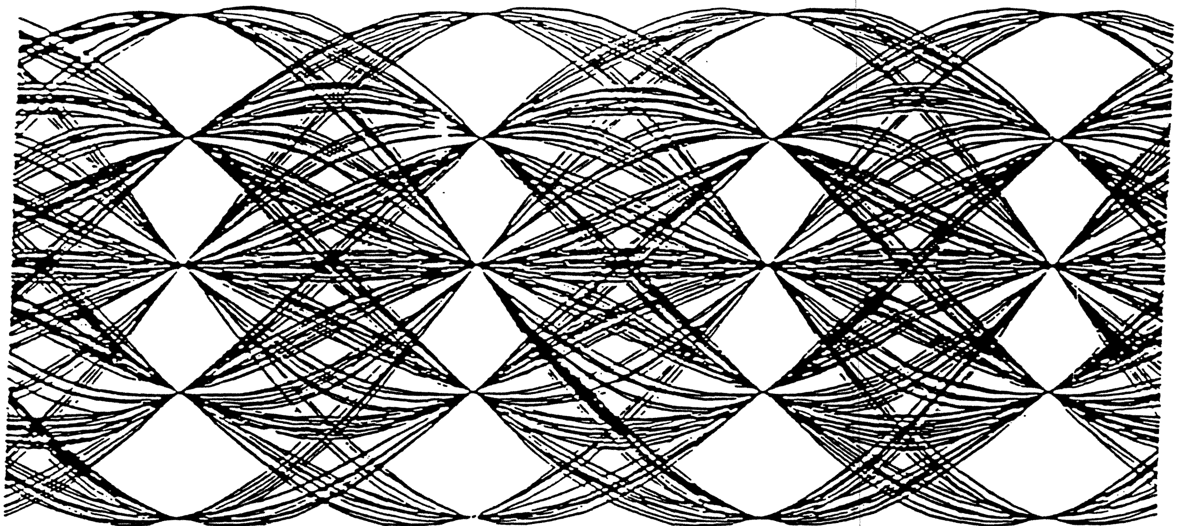


EYE DIAGRAM FOR PR4



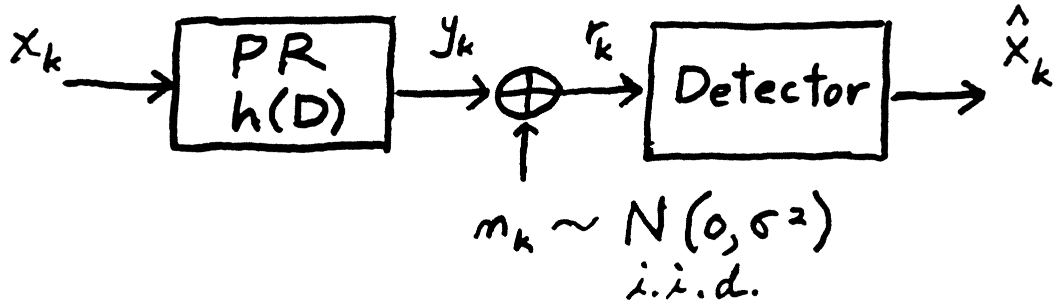
- 3 nominal sample values

EYE DIAGRAM FOR EPR4



- 5 nominal sample values

DETECTION



Received samples: $\quad r_k = y_k + n_k$

- Maximum Likelihood (ML) detector

$$\max_{\underline{x}} \; p(\underline{r} \,|\, \underline{x})$$

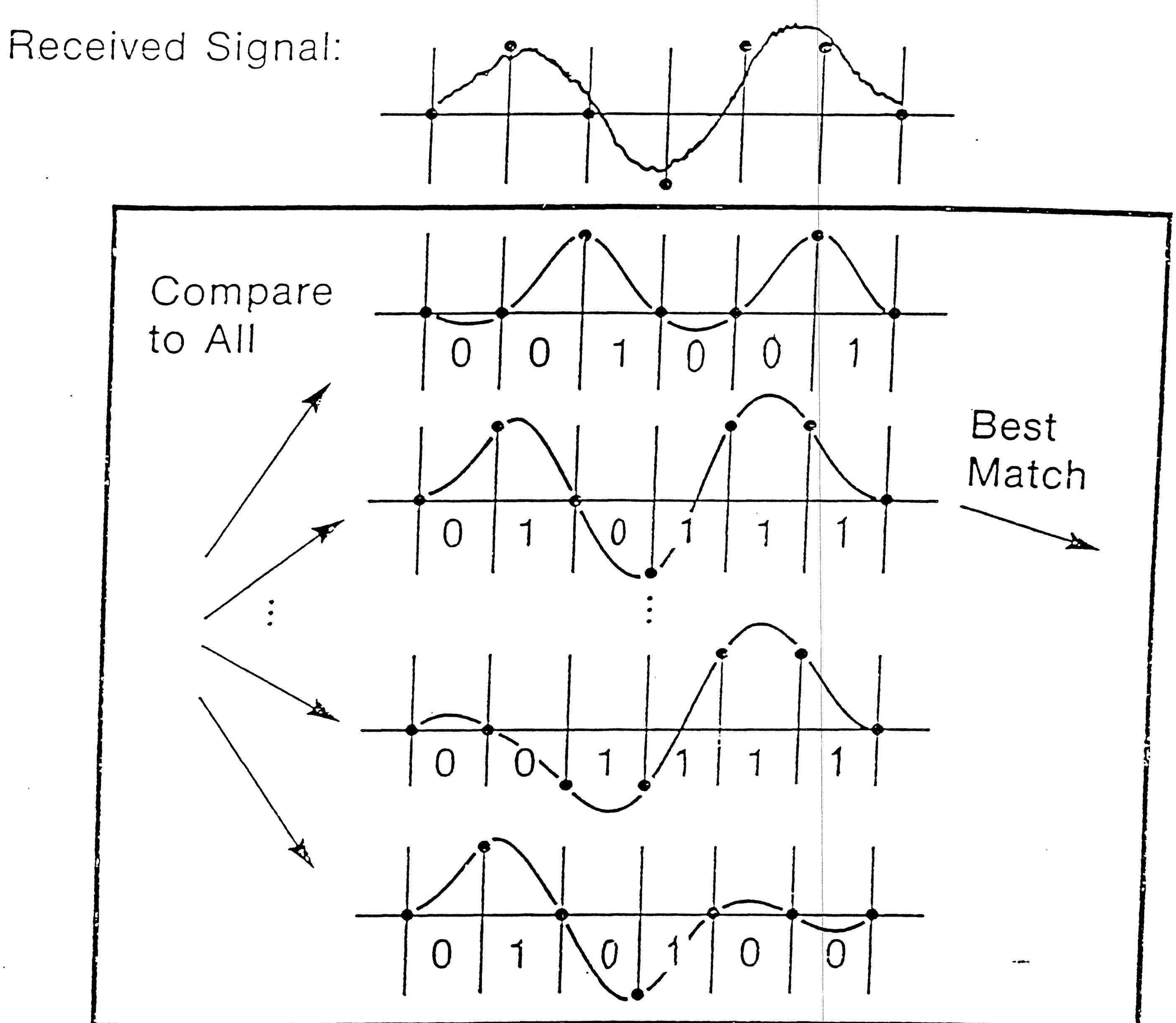
likelihood function

<u>ML is optimal detector</u>

- ML $\Longleftrightarrow$ Minimum-Distance decoding

$$\max_{\underline{x}} \; p(\underline{r} \,|\, \underline{x}) \iff \min_{\underline{x}} \sum_k (r_k - y_k)^2$$

MAXIMUM-LIKELIHOOD DETECTION
(SCHEMATIC)



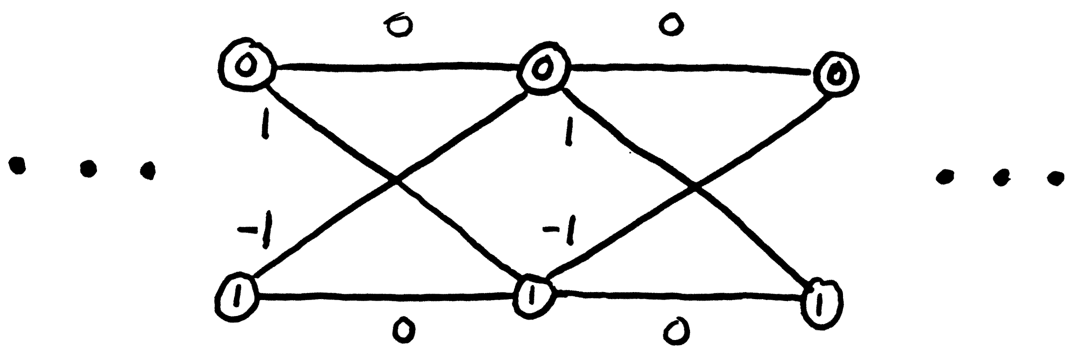
Most likely information sequence:

. . . 0 1 0 1 1 1 . . .

THE VITERBI ALGORITHM (VA)

- Recursive solution of ML detection (dynamic programming)

- Trellis representation of PR channel (Forney)



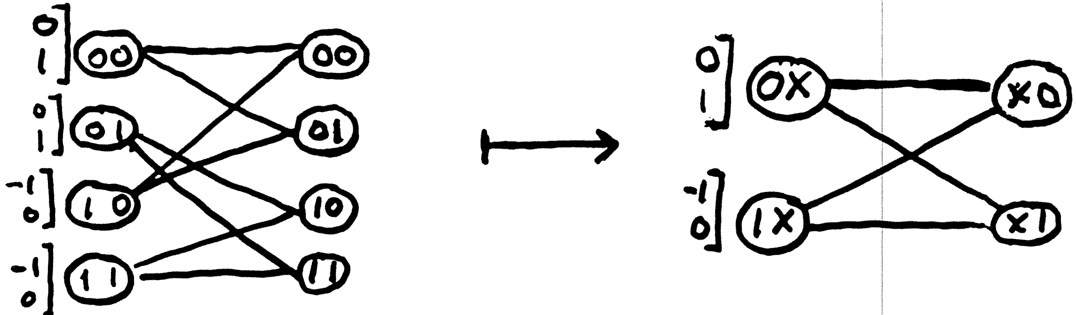
"Dicode" channel: $h(D) = 1 - D$

- Trellis-based architecture

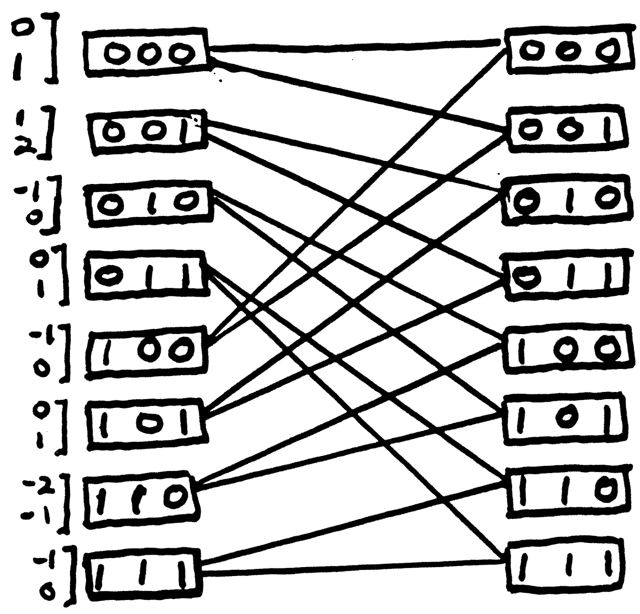
Trellis state $\longrightarrow$ <u>A</u>dd - <u>C</u>ompare - <u>S</u>elect processor (A C <u>S</u>)

PR TRELLISES

- PR4 (interleaved dicode)

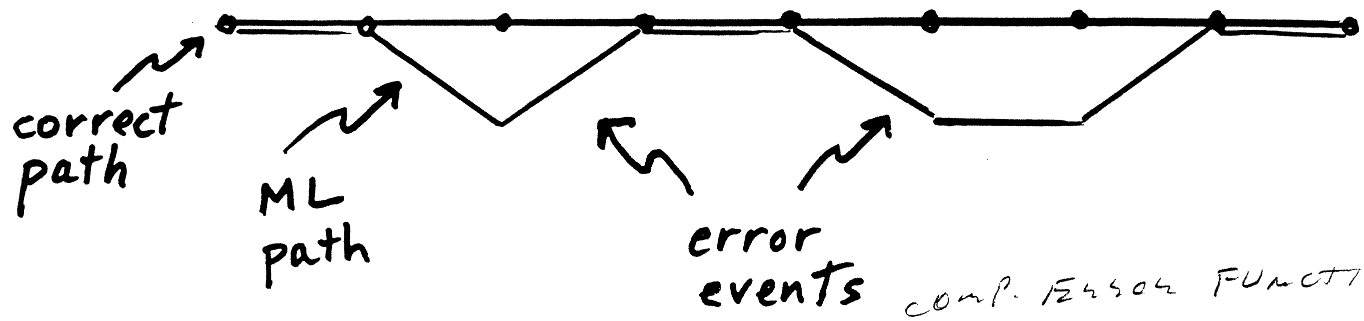


- EPR4



Improved PR model ⇒ larger detector complexity

VA PERFORMANCE



COMP. ERROR FUNCTION

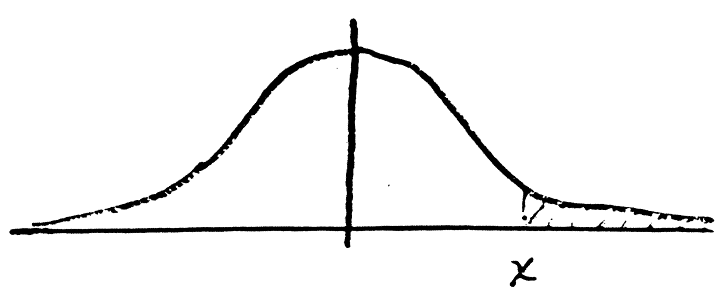
$$P_e \approx N \, Q\left(\frac{d_{free}}{2\sigma}\right)$$

where N = "error coefficient"

d^2_{free} = minimum distance between any two trellis sequences differing by 1 error event

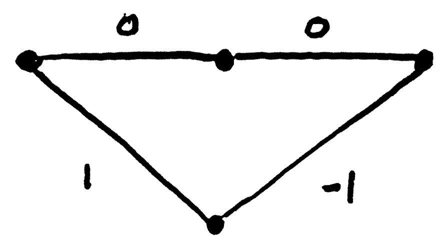
and

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-\frac{s^2}{2}} \, ds$$



VA PERFORMANCE
EXAMPLE

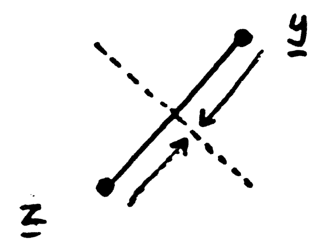
- $h(D) = (1-D)$



$$d^2_{free} = 2$$

$$N = 2$$

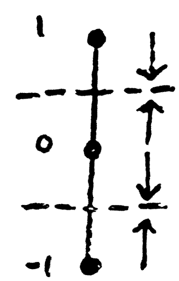
$$P_e^{VA} \approx 2\,Q\left(\frac{\sqrt{2}}{2\sigma}\right)$$



$$\frac{d_{free}}{2} = \frac{\sqrt{2}}{2}$$

- Compare to threshold detection (TD)

$$P_e^{TD} \approx \frac{3}{2}\,Q\left(\frac{1}{2\sigma}\right)$$

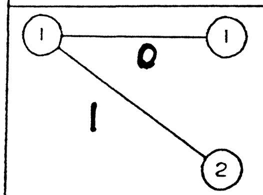
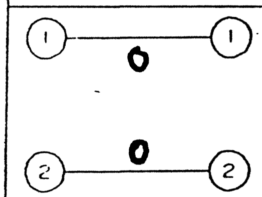
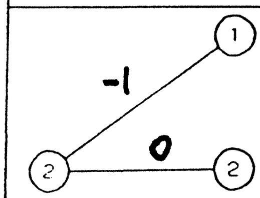


$$\frac{d}{2} = \frac{1}{2}$$

- VA is <u>3 dB</u> <u>better</u> than TD

VITERBI ALGORITHM

- Difference-metric formulation

Extension	*Condition*	*Update*
	$DM_k \leq 2y_{k+1} - 1$	$DM_{k+1} = 2y_{k+1} - 1$
	$2y_{k+1} - 1 < DM_k < 2y_{k+1} + 1$	$DM_{k+1} = DM_k$
	$2y_{k+1} + 1 \leq DM_k$	$DM_{k+1} = 2y_{k+1} + 1$

(0, G/I)
CONSTRAINED CODES
FOR
PRML

PRECODING CONVENTIONS
(peak detection)

- NRZI : $\left(\frac{1}{1 \oplus D}\right)$

  0 $\longrightarrow$ no transition

  1 $\longrightarrow$ $\pm$ transition

- (d,k) constraints

  $d \leq$ # consecutive 0's $\leq k$

  d reduces intersymbol-interference

  k provides timing/gain information

- $(1,7)$ example

  1 0 1 0 0 0 0 0 0 0 1 0 0 1 0 1 . . .

PRECODING CONVENTIONS
(PRML)

- Interleaved NRZI (INRZI): $\frac{1}{1 \oplus D^2}$

  $0 \longrightarrow 0$ sample

  $1 \longrightarrow \pm 1$ sample

- $(0, G/I)$ constraints

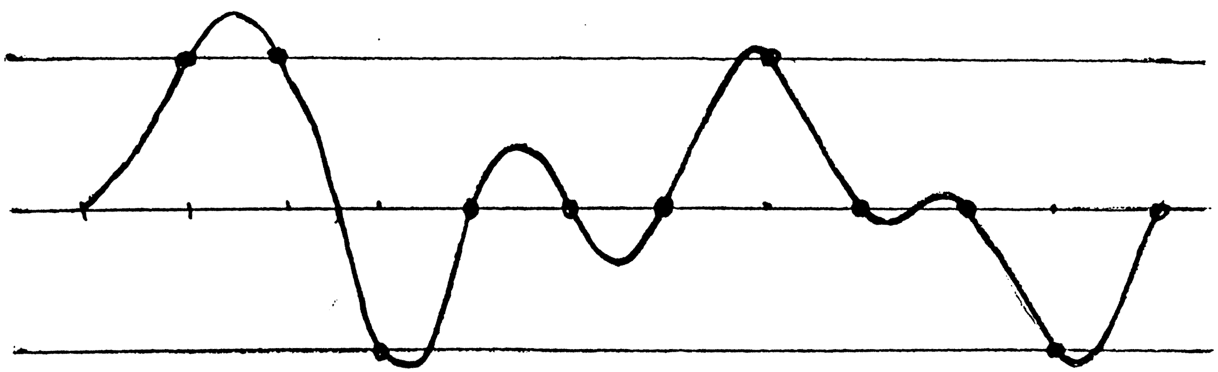
  $d = 0$ (no ISI problem)

  G = Global k constraint
  (timing/gain)

  I = Interleaved k constraint
  (Viterbi path memory)

(0,G/I) = (0,4/4)

0 1 1 1 0 0 0 1 0 0 1 0



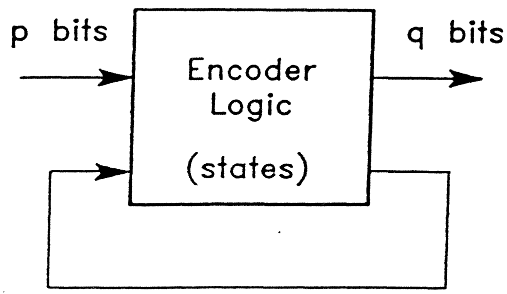
0 + + - 0 0 0 + 0 0 - 0

0 + 0 0 0 -

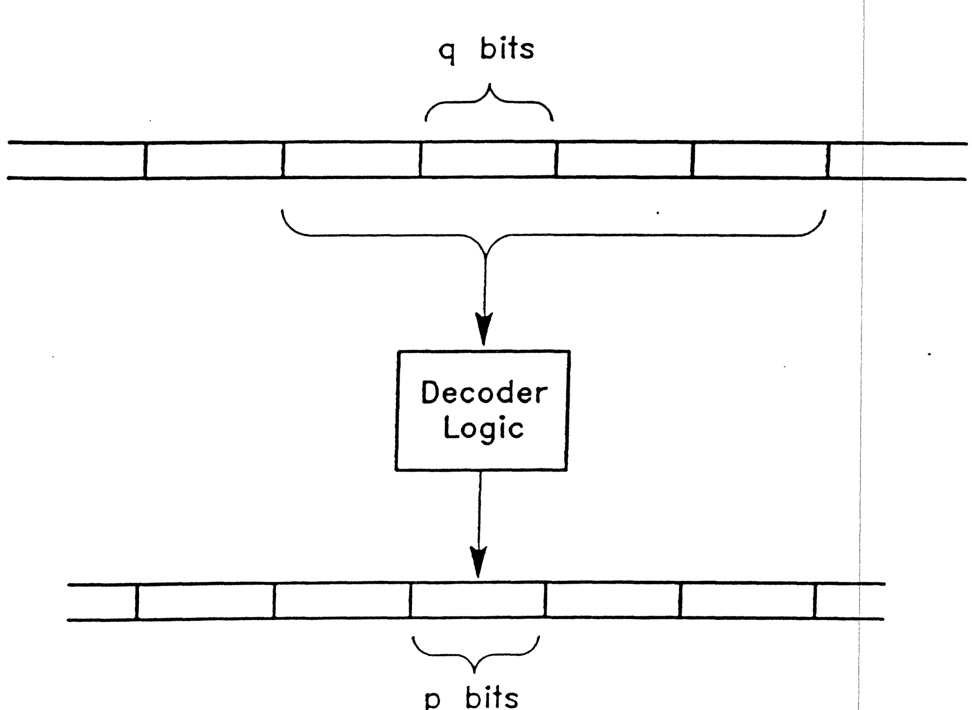
+ - 0 + 0 0

SLIDING-BLOCK CODES

- Finite-state encoder



- Sliding-block decoder



- Practical code construction methods

Sliding-Block (0,G/I) Codes

(0,G/I)	Capacity	Rate	Efficiency (%)	Encoder States	Decoder Window
(0,4/4)*	0.961	8/9	92.4	1	1
(0,4/3)	0.939	8/9	94.6	3	1
(0,3/6)*	0.944	8/9	94.1	1	1
(0,3/5)	0.941	8/9	94.4	2	1
(0,3/4)	0.934	8/9	95.1	3	2
(0,3/3)	0.915	8/9	97.0	4	2

×9 FOR # of BITS

* Originally found by J. Eggenberger

$(0, G/I) = (0, 4/4)$

- Optimal list of 279 9-bit words (in decimal)

73	116	183	225	268	310	361	402	438	479
75	117	185	227	269	311	363	403	439	481
76	118	186	228	270	313	364	406	441	483
77	119	187	229	271	314	365	407	442	484
78	121	188	230	281	315	366	409	443	485
79	122	189	231	282	316	367	410	444	486
89	123	190	233	283	317	369	411	445	487
90	124	191	235	284	318	370	412	446	489
91	125	195	236	285	319	371	413	447	491
92	126	198	237	286	329	372	414	451	492
93	127	199	238	287	331	373	415	454	493
94	146	201	239	289	332	374	417	455	494
95	147	203	241	291	333	375	419	457	495
97	150	204	242	292	334	377	420	459	497
99	151	205	243	293	335	378	421	460	498
100	153	206	244	294	345	379	422	461	499
101	154	207	245	295	346	380	423	462	500
102	155	210	246	297	347	381	425	463	501
103	156	211	247	299	348	382	427	466	502
105	157	214	249	300	349	383	428	467	503
107	158	215	250	301	350	390	429	470	505
108	159	217	251	302	351	391	430	471	506
109	177	218	252	303	353	393	431	473	507
110	178	219	253	305	355	395	433	474	508
111	179	220	254	306	356	396	434	475	509
113	180	221	255	307	357	397	435	476	510
114	181	222	265	308	358	398	436	477	511
115	182	223	267	309	359	399	437	478	

$G=4$: ≤ 2 0's at beginning/end

≤ 4 consecutive 0's inside

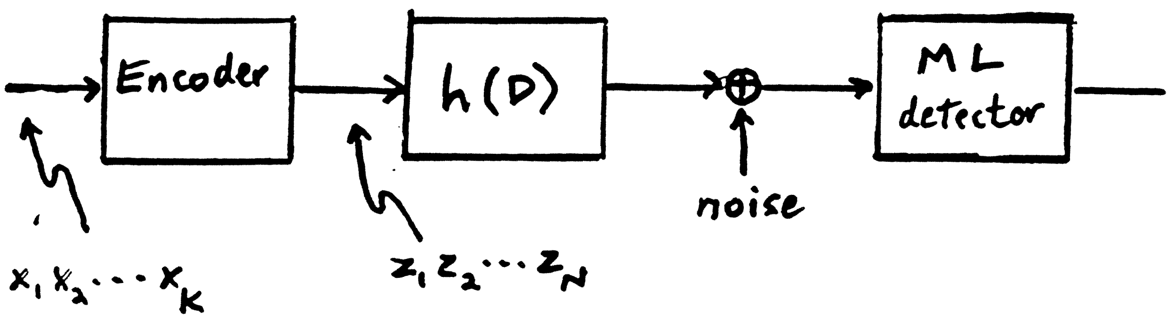
$I=4$: ≤ 2 0's at beginning/end in <u>each</u> interleave

≤ 4 consecutive 0's inside in <u>each</u> interleave

TRELLIS-CODED PRML

- Objectives and tradeoffs
- Example - Interleaved Biphase
- Design techniques
  - Precoded convolutional codes
  - Matched-spectral-null codes

TRELLIS CODING



Binary symbols $\Rightarrow N > K$

- Why use coding?
  - Reduce P_e
  - Tolerate larger σ
    - off-track capability
    - areal density
    - component yield
    - fly height relaxation
- Coding approach
  - Increase d_{free} with structured redundancy (trellis)
  - Enhance ML detector
- Costs
  - Code rate loss
  - Code/detector complexity

TRELLIS - CODED MODULATION

HISTORICAL BACKGROUND

- Shannon (1948): Use structured waveforms for efficient utilization of signal power and limited channel bandwidth.

- Elias, Massey, Viterbi, Forney, et al. (~1960's): Convolutional codes for binary, memoryless channel

- Ungerboeck (1981): Trellis-coded modulation (TCM) for multi-level, memoryless channel.

- Wolf - Ungerboeck (1986): TCM for binary, partial-response channels $h(D) = 1 \pm D^N$. using convolutional codes.

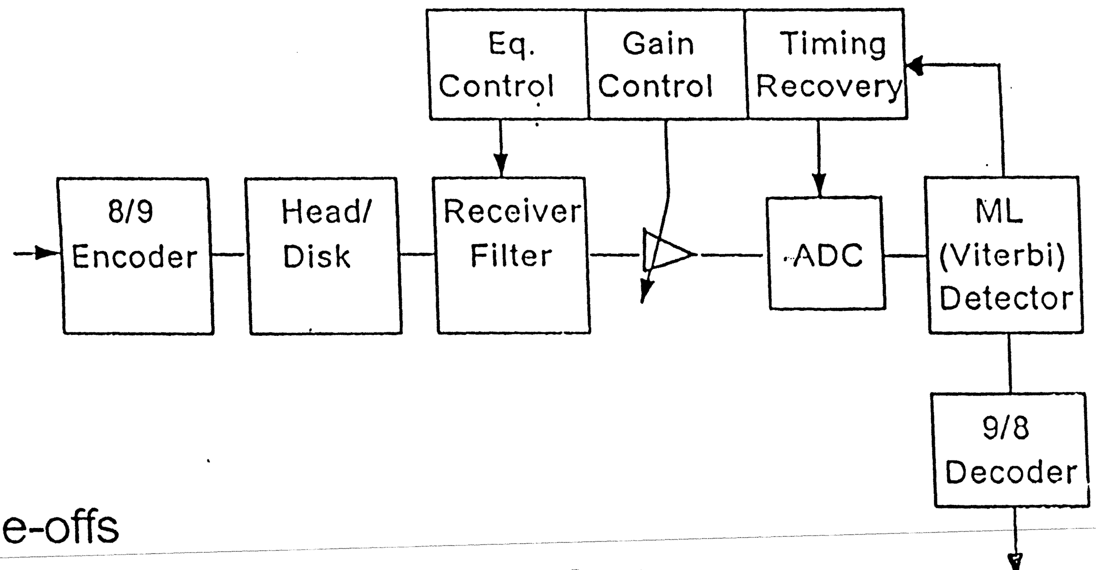
  [Also, Calderbank - Heegard - Lee (1986)]

- Karabed - Siegel (1988): New TCM for binary, PR channels
  - Convolutional codes + inner codes
  - Matched-Spectral-Null codes

- TCM for multi-level, PR channels ...

Trellis Code Design Problem

- Replace selected digital blocks in PRML channel



- Trade-offs

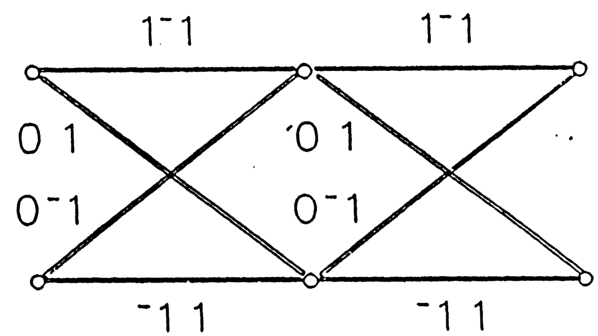
Coding gain (dB)	vs	Code rate
		Encoder/decoder complexity
		Viterbi detector complexity

Trellis Code Example

- Interleaved Biphase (IB) Code

  Rate: 1/2 (2:4)

  Encoder: $xy \rightarrow xy\bar{x}\bar{y}$

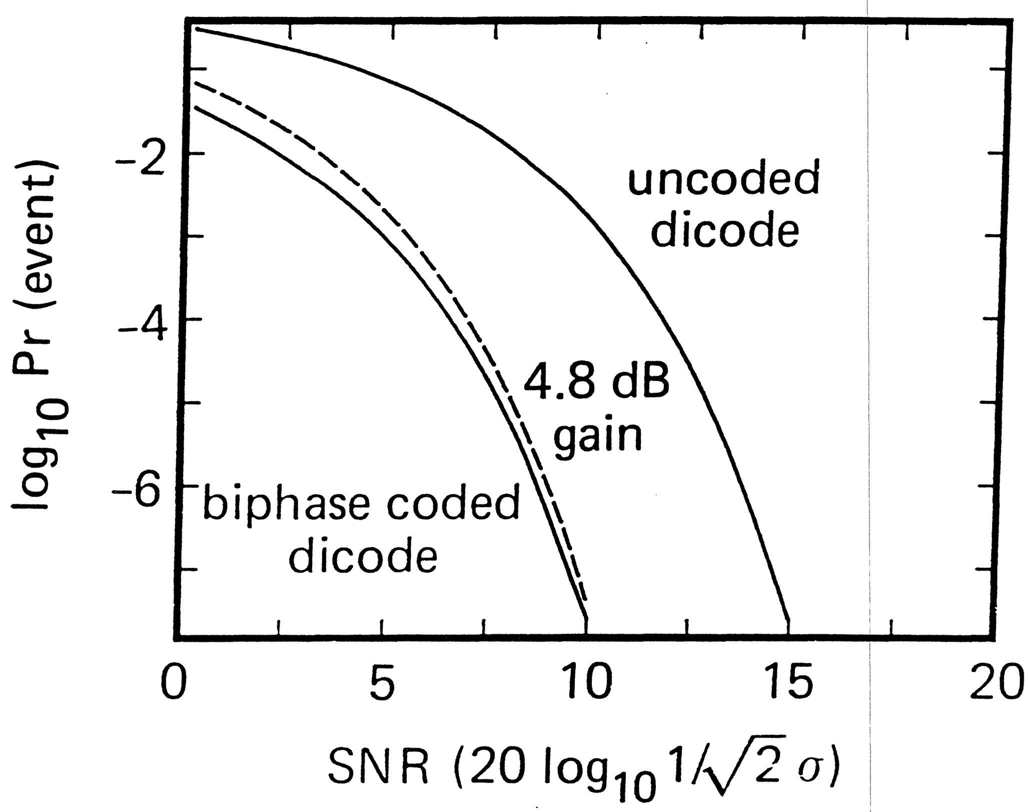


- Coding gain 4.8 dB

  $d^2_{free} = 6$ $\left(10 \log_{10} \frac{6}{2} = 4.8\right)$

- Complexity 4 $\left(\frac{\#\text{ edges}}{\text{stage}}\right)$

IB/DICODE PERFORMANCE
(simulated)



- Additive white gaussian noise

  $n_i \sim N(0, \sigma^2)$

Increasing Areal Density

W

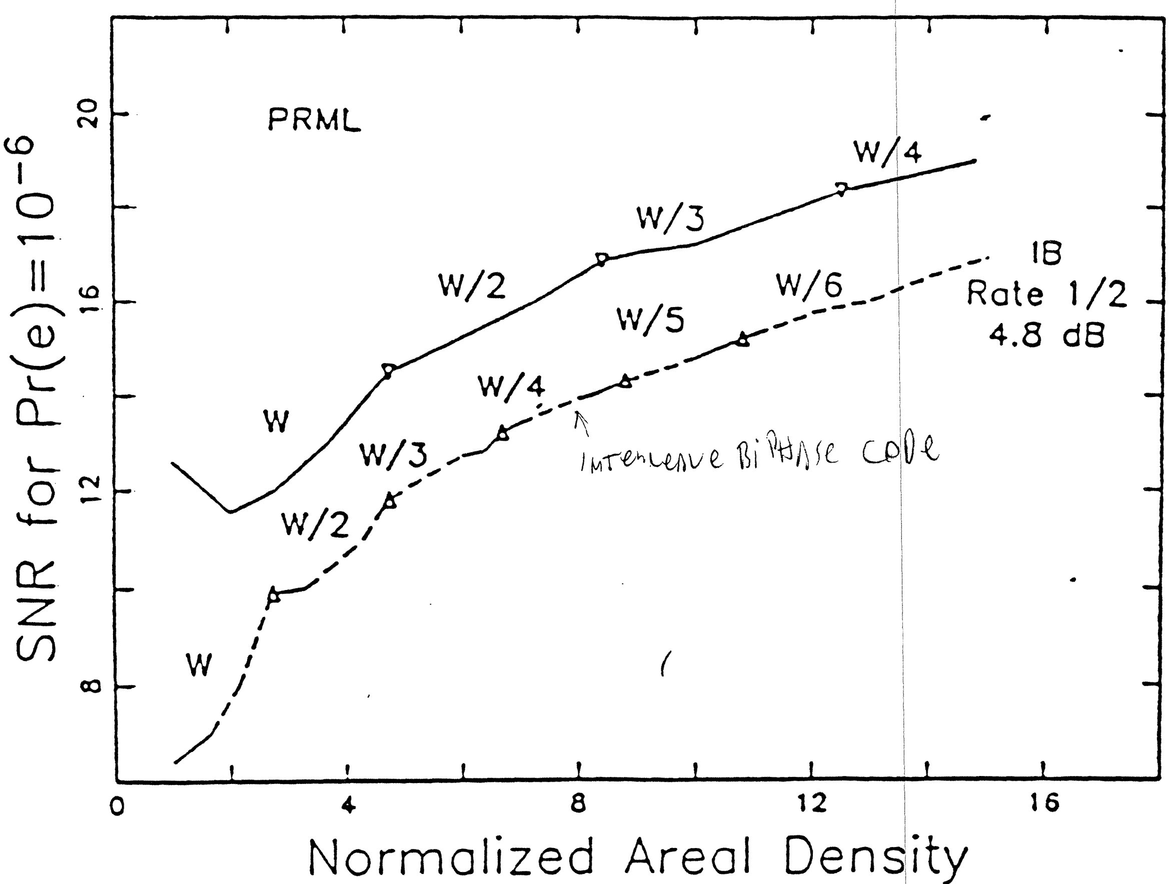
$W/3$

$W/3$

$W/3$

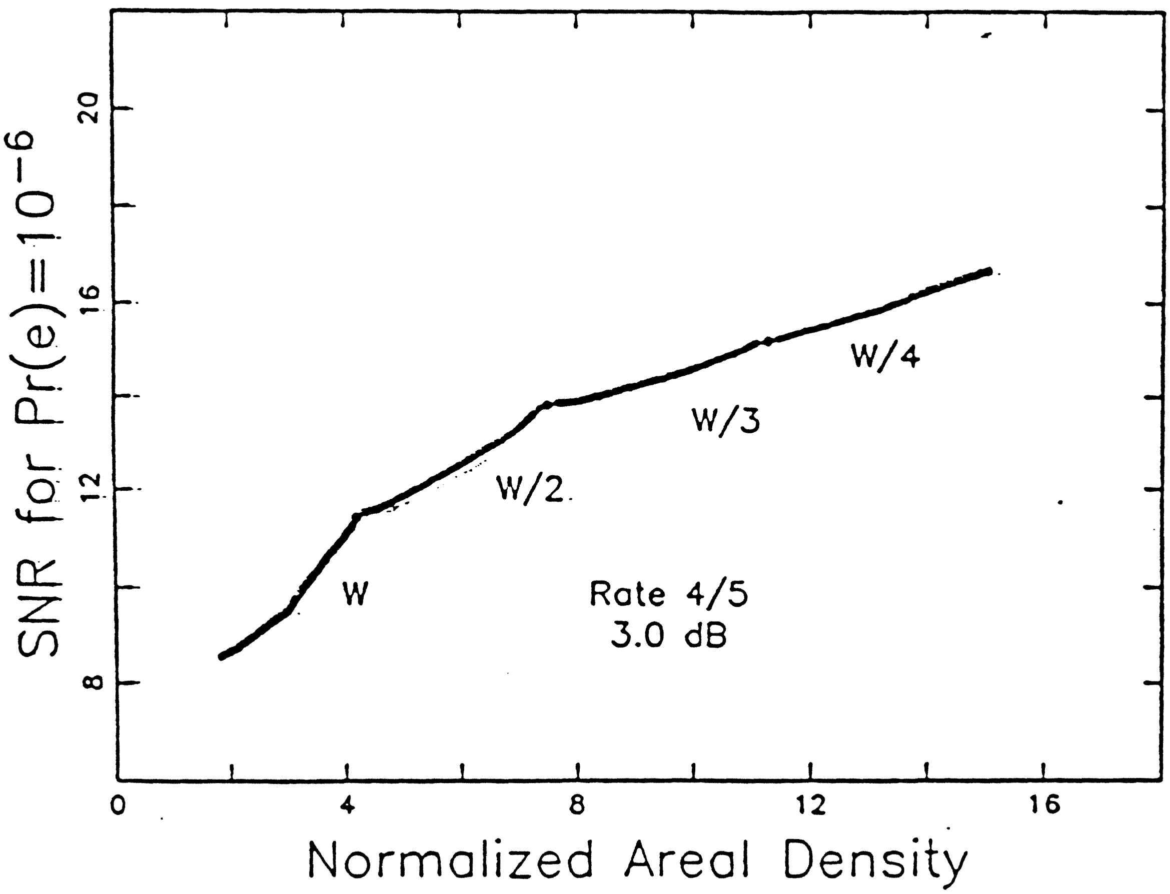
- Reduce trackwidth by 3: costs 4.8 dB
- Rate 1/2 IB code: gains 4.8 dB
- Net areal density: 1.7 (70% increase)
  $3 \times (1/2) \times (9/8) \simeq 1.7$
- Same P_e

TRACK CUTTING



- IB areal density gains > 70%
  - Low rate ⇒ very narrow tracks

TRACK CUTTING
(cont.)



- Rate 4/5, gain 3 dB
  - Same density gains
  - Wider tracks

WOLF-UNGERBOECK CODES

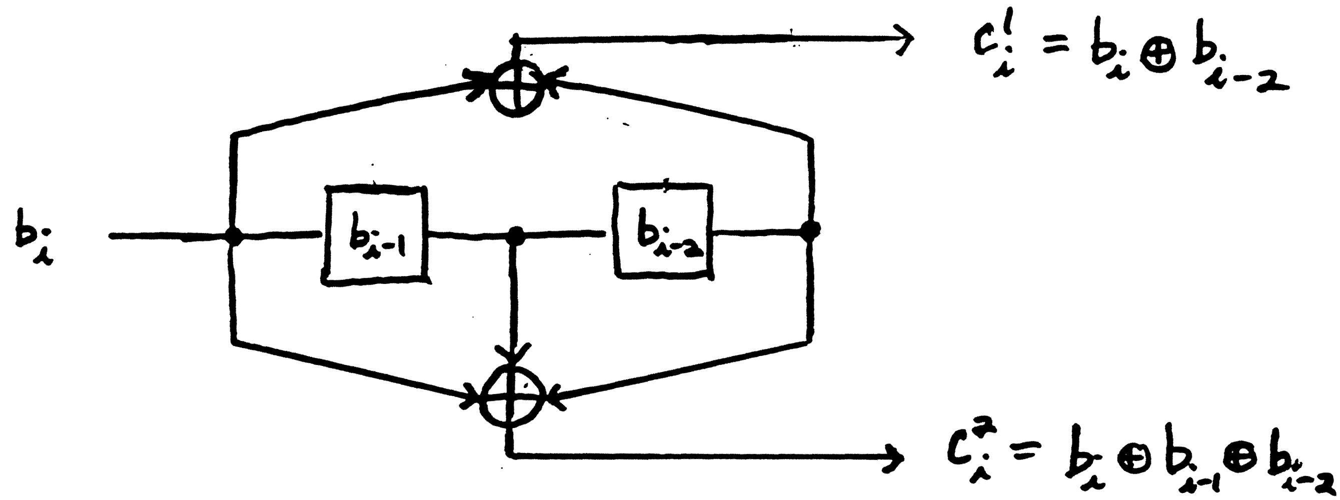
- Use known binary convolutional codes (designed for memoryless channel)

- Neutralize PR channel memory via precoding

- Add coset sequence to limit runs of zero samples

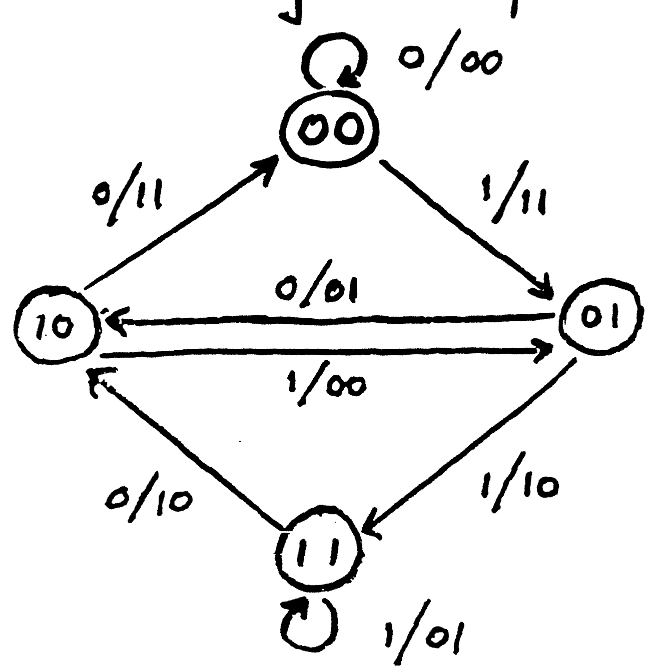
CONVOLUTIONAL CODES

- Linear Feed-Forward Shift Register Encoder



$$\left.\begin{array}{l} 0,0,0,0,0,0. \\ 0,0,1,0,0,0. \end{array}\right\} d^H = 1 \longrightarrow d^H = 5 \left\{\begin{array}{l} 00,00,00,00,00,00. \\ 00,00,11,01,11,00. \end{array}\right.$$

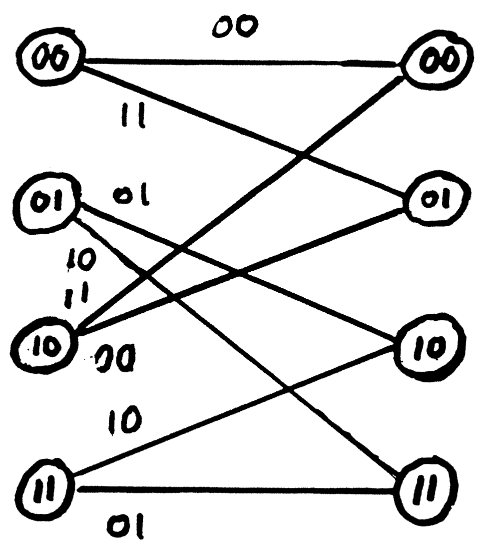
- State-diagram representation



$d^H_{free} = 5$

DECODING CONVOLUTIONAL CODES

- Trellis representation



- ML decoding via VA

- Optimal codes

  Maximize d^H_{free}
  for given rate $R = \frac{K}{N}$
  and complexity M (total encoder memory)

OPTIMAL CODE TABLES

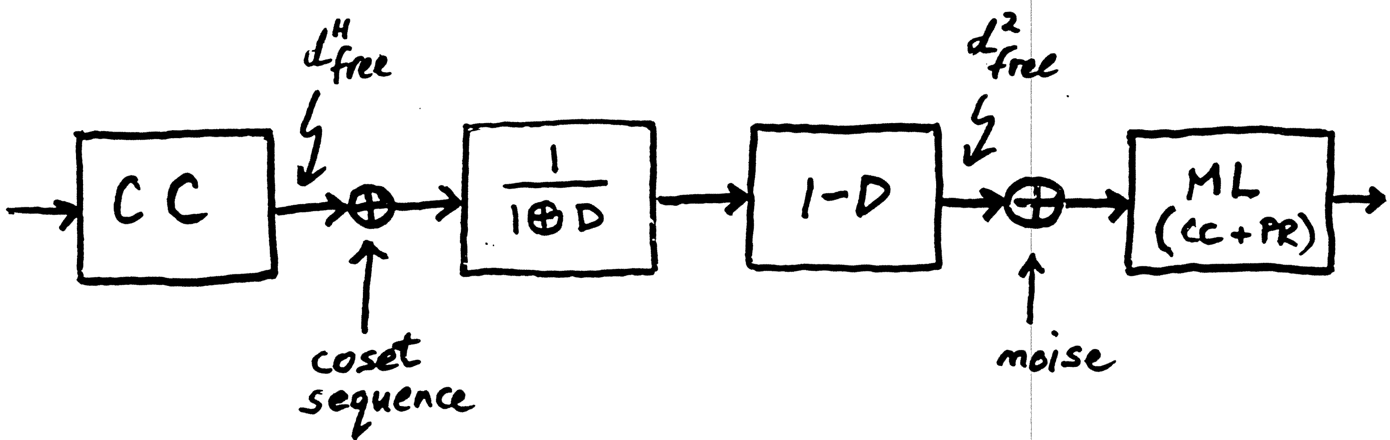
- Best codes found by computer search
- Examples [ref. Lin-Costello]

	M	States (2^M)	d^H_{free}
Rate $\frac{1}{2}$			
	2	4	5
	* 6	64	10
Rate $\frac{2}{3}$			
	4	16	5
	10	1024	10
Rate $\frac{3}{4}$			
	5	32	5
	6	64	6
Rate $\frac{4}{5}$ from [Daut, et. al.]	3	8	3

CONVOLUTIONAL CODES
FOR
PR $h(D) = (1 \pm D^N)$

- PR channel memory can destroy good d^H_{free} at channel input

- Solution (W-U): Use <u>precoder</u> to neutralize channel memory



- Precoder effect:

$$0 \longmapsto 0$$
$$1 \longmapsto \pm 1$$

$$d^2_{free} \geq \begin{cases} d^H_{free} & \text{if } d^H_{free} \text{ is even} \\ d^H_{free}+1 & \text{if } d^H_{free} \text{ is odd} \end{cases}$$

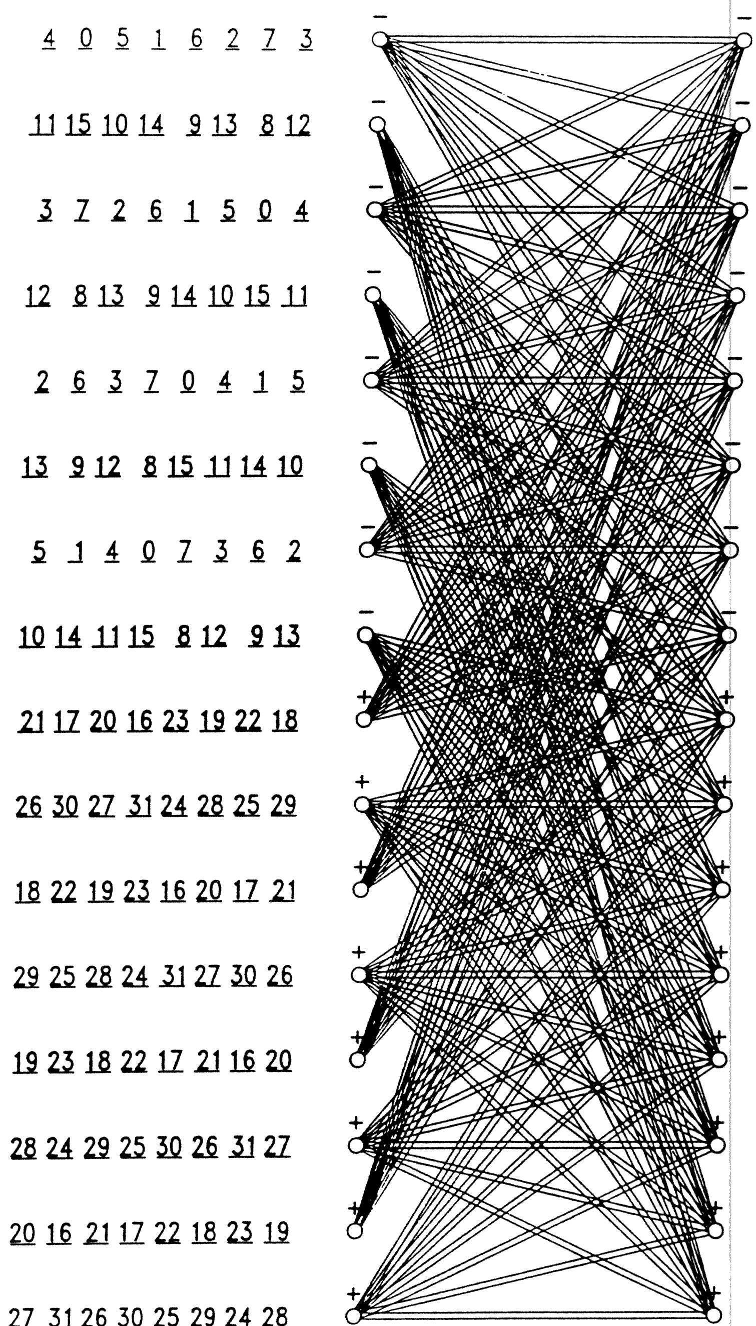
[see also C-H-L ; Hole]

PRECODED PR
(cont.)

- Coset sequence limits maximum run of zero outputs (timing/gain)
- ML decoder trellis has $\underline{2^{M+1}}$ states (usually - not always, e.g. see * in table)
- Gains smaller than in memoryless channel (for given rate and decoder complexity)

"Full response"	PR $(1 \pm D)$
$R = \frac{3}{4}$, $M = 6$, $d^H_{free} = 6$	$R = \frac{3}{4}$, $M+1 = 6$, $d^2_{free} = 6$
$\text{C.G.} = 10 \log_{10} \boxed{\dfrac{d^H_{free}}{1}}$	$\text{C.G.} = 10 \log_{10} \boxed{\dfrac{d^2_{free}}{2}}$
≈ 7.8 dB	≈ 4.8 dB
$\text{A.C.G.} = \text{C.G.} + 10 \log_{10} R$	$\text{A.C.G} = \text{C.G.} - 10 \log_{10} R$
≈ 6.5 dB	≈ 3.5 dB

W-U CODE EXAMPLE
(for 1-D channel)



- Rate 4/5, gain 3 dB
- $(0, G/I) = (0, 44/22)$ when interleaved

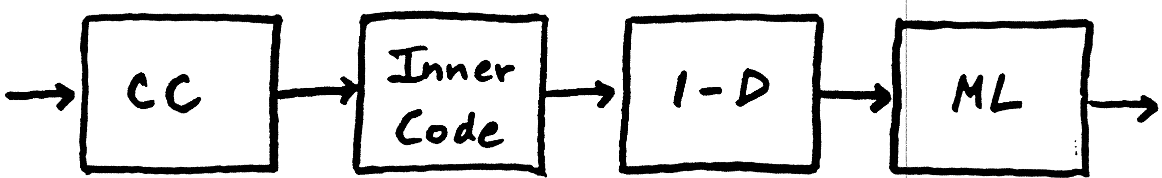
W-U CODE EXAMPLE (cont.)

- Detector edge labels

− to −	+ to −	− to +	+ to +
$\underline{0}\ \begin{cases}10\bar{1}00\\1\bar{1}01\bar{1}\end{cases}$	$\underline{16}\ \begin{cases}00\bar{1}00\\0\bar{1}01\bar{1}\end{cases}$	$\underline{8}\ \begin{cases}00100\\010\bar{1}1\end{cases}$	$\underline{24}\ \begin{cases}\bar{1}0100\\\bar{1}10\bar{1}1\end{cases}$
$\underline{1}\ \begin{cases}1\bar{1}1\bar{1}0\\1000\bar{1}\end{cases}$	$\underline{17}\ \begin{cases}0\bar{1}1\bar{1}0\\0000\bar{1}\end{cases}$	$\underline{9}\ \begin{cases}01\bar{1}10\\00001\end{cases}$	$\underline{25}\ \begin{cases}\bar{1}1\bar{1}10\\\bar{1}0001\end{cases}$
$\underline{2}\ \begin{cases}01\bar{1}00\\0001\bar{1}\end{cases}$	$\underline{18}\ \begin{cases}\bar{1}1\bar{1}00\\\bar{1}001\bar{1}\end{cases}$	$\underline{10}\ \begin{cases}1\bar{1}100\\100\bar{1}1\end{cases}$	$\underline{26}\ \begin{cases}0\bar{1}100\\000\bar{1}1\end{cases}$
$\underline{3}\ \begin{cases}001\bar{1}0\\0100\bar{1}\end{cases}$	$\underline{19}\ \begin{cases}\bar{1}01\bar{1}0\\\bar{1}100\bar{1}\end{cases}$	$\underline{11}\ \begin{cases}10\bar{1}10\\1\bar{1}001\end{cases}$	$\underline{27}\ \begin{cases}00\bar{1}10\\0\bar{1}001\end{cases}$
$\underline{4}\ \begin{cases}0010\bar{1}\\010\bar{1}0\end{cases}$	$\underline{20}\ \begin{cases}\bar{1}010\bar{1}\\\bar{1}10\bar{1}0\end{cases}$	$\underline{12}\ \begin{cases}10\bar{1}01\\1\bar{1}010\end{cases}$	$\underline{28}\ \begin{cases}00\bar{1}01\\0\bar{1}010\end{cases}$
$\underline{5}\ \begin{cases}01\bar{1}1\bar{1}\\00000\end{cases}$	$\underline{21}\ \begin{cases}\bar{1}1\bar{1}1\bar{1}\\\bar{1}0000\end{cases}$	$\underline{13}\ \begin{cases}1\bar{1}1\bar{1}1\\10000\end{cases}$	$\underline{29}\ \begin{cases}0\bar{1}1\bar{1}1\\00000\end{cases}$
$\underline{6}\ \begin{cases}1\bar{1}10\bar{1}\\100\bar{1}0\end{cases}$	$\underline{22}\ \begin{cases}0\bar{1}10\bar{1}\\000\bar{1}0\end{cases}$	$\underline{14}\ \begin{cases}01\bar{1}01\\00010\end{cases}$	$\underline{30}\ \begin{cases}\bar{1}1\bar{1}01\\\bar{1}0010\end{cases}$
$\underline{7}\ \begin{cases}10\bar{1}1\bar{1}\\1\bar{1}000\end{cases}$	$\underline{23}\ \begin{cases}00\bar{1}1\bar{1}\\0\bar{1}000\end{cases}$	$\underline{15}\ \begin{cases}001\bar{1}1\\01000\end{cases}$	$\underline{31}\ \begin{cases}\bar{1}01\bar{1}1\\\bar{1}1000\end{cases}$

INNER CODES

- Use simple inner code to exploit channel memory (Karabed-Siegel, Immink)



	Rate	Inner Code	Zero Runlength
(W-U)	$R=1$	$\frac{1}{1 \oplus D}$	CC dependent
(IC1)	$R=\frac{1}{2}$	$x \mapsto x\bar{x}$ (biphase)	1
(IC2)	$R=\frac{2}{3}$	$xy \mapsto xy\bar{y}$	2

- IC1 and IC2 give <u>robust</u> coding gain.

INNER CODES
(cont.)

- Gains from IC1 and IC2
  (for any convolutional code)

IC1:

$$d^2_{free} \geq 4\, d^H_{free} + 4$$

$$R_{cc/IC} = \frac{1}{2} R_{cc}$$

IC2:

$$d^2_{free} \geq 2\, d^H_{free}$$

$$R_{cc/IC} = \frac{2}{3} R_{cc}$$

- Example using IC2

$R_{cc} = \frac{3}{4}$, $M = 3$, $d^H_{free} = 5 \Rightarrow$

$R_{cc/IC} = \frac{3}{6}$, states = 16, $d^2_{free} = 10$

Compare to W-U: $R = \frac{1}{2}$, states = 64, $d^2_{free} = 10$

MATCHED-SPECTRAL-NULL CODES

- Code design method based on general theorem

  Significant coding gain results if:

$$\left\{\begin{array}{l}\text{null frequencies}\\ \text{in code power}\\ \text{spectrum}\end{array}\right\} = \left\{\begin{array}{l}\text{null frequencies}\\ \text{in channel frequency}\\ \text{response}\end{array}\right\}$$

- Sliding-block code design

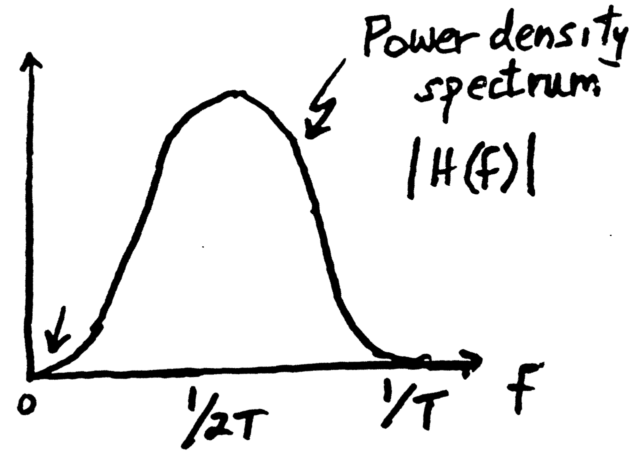
- Reduced-complexity detector trellis

MSN EXAMPLES

- Biphase code

$$h(D) = 1 - D$$

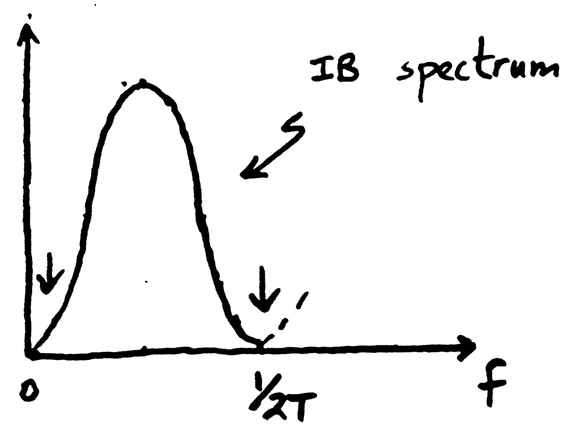
C.G. = $\underline{4.8\text{ dB}}$



- Interleaved Biphase

$$h(D) = \begin{cases} (1-D)(1+D) & (PR4) \\ (1-D)(1+D)^2 & (EPR4) \end{cases}$$

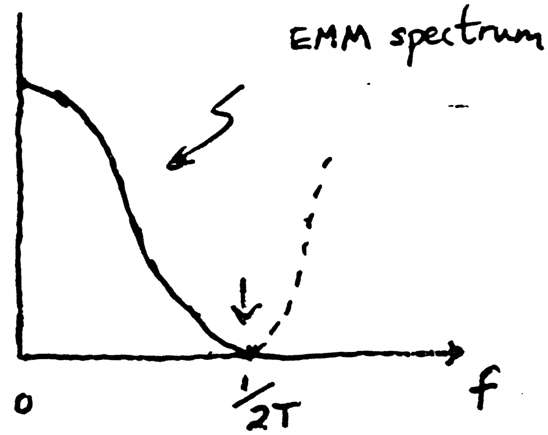
C.G. = $\underline{4.8\text{ dB}}$



- Even Mark Modulation

$$h(D) = \begin{cases} 1+D & (PR1) \\ (1+D)^2 & (PR2) \end{cases}$$

$$C.G. = \begin{cases} 3\text{ dB} \\ 4\text{ dB} \end{cases}$$



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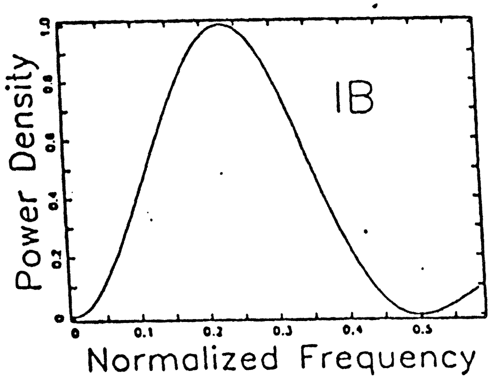
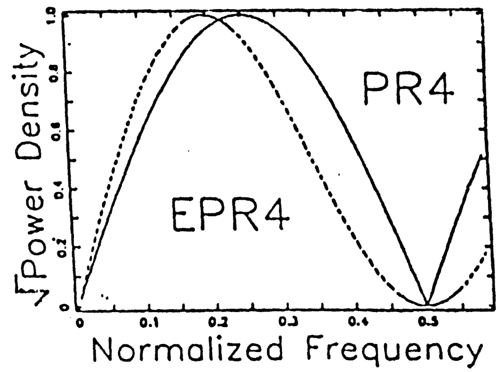
Matched Spectral Null Codes (cont.)

- Magnetic recording partial-responses

Interleaved Biphase

PR4: 4.8 dB
EPR4: 4.8 dB

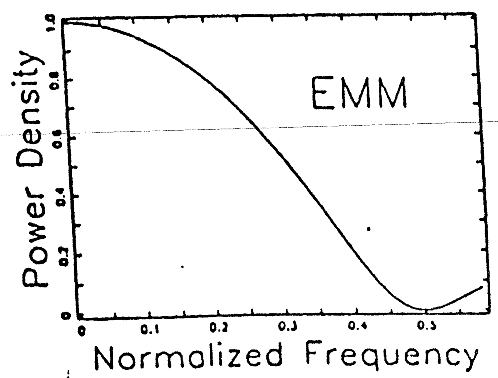


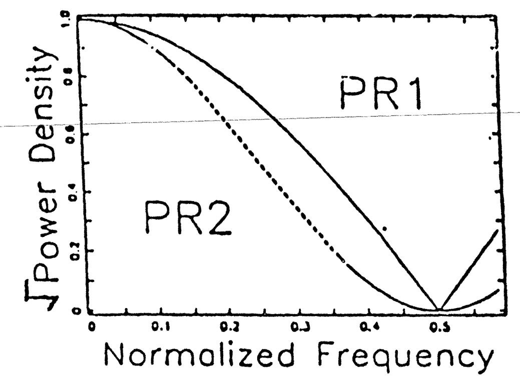


- Optical recording partial-responses

EMM

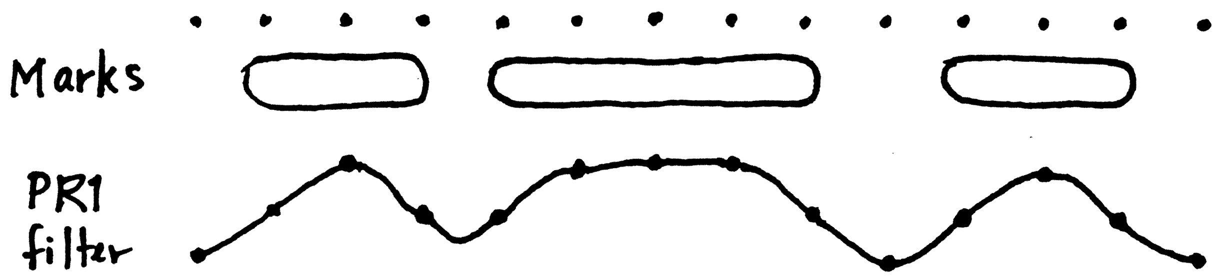
PR1: 3 dB
PR2: 4 dB



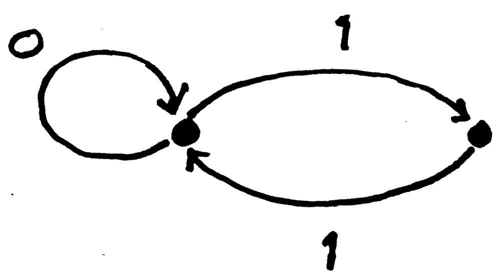


EVEN-MARK-MODULATION (EMM)

- Asymmetric RLL constraint for optical recording
- Marks must be <u>even</u> in length



- EMM constraint diagram



$$C = \log_2 \frac{1+\sqrt{5}}{2}$$
$$\approx .69$$

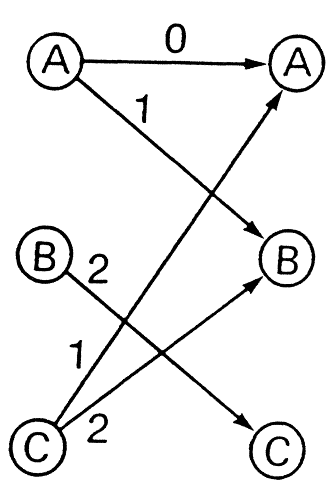
- Rate 2/3 code possible

EMM CODE

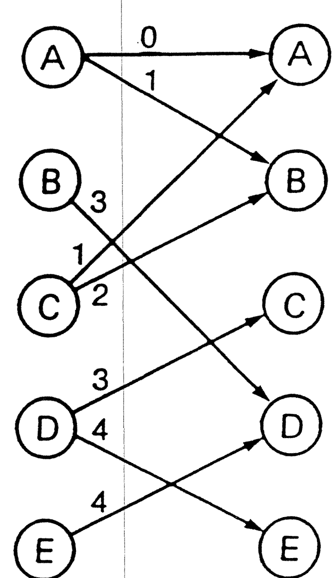
Data b_1/b_2 State $s_1s_2s_3$	00	01	10	11
000	011/000	011/001	110/000	110/001
001	001/100	001/101	110/010	011/110
010	000/000	000/011	111/100	111/101
011	001/100	001/101	111/100	111/101
100	100/000	100/001	101/100	101/101
101	111/000	111/001	100/010	111/111
110	000/000	000/001	111/100	111/101
111	000/000	000/001	111/100	000/010

Rate 2:3 encoder

Table entries = "codeword/next state"

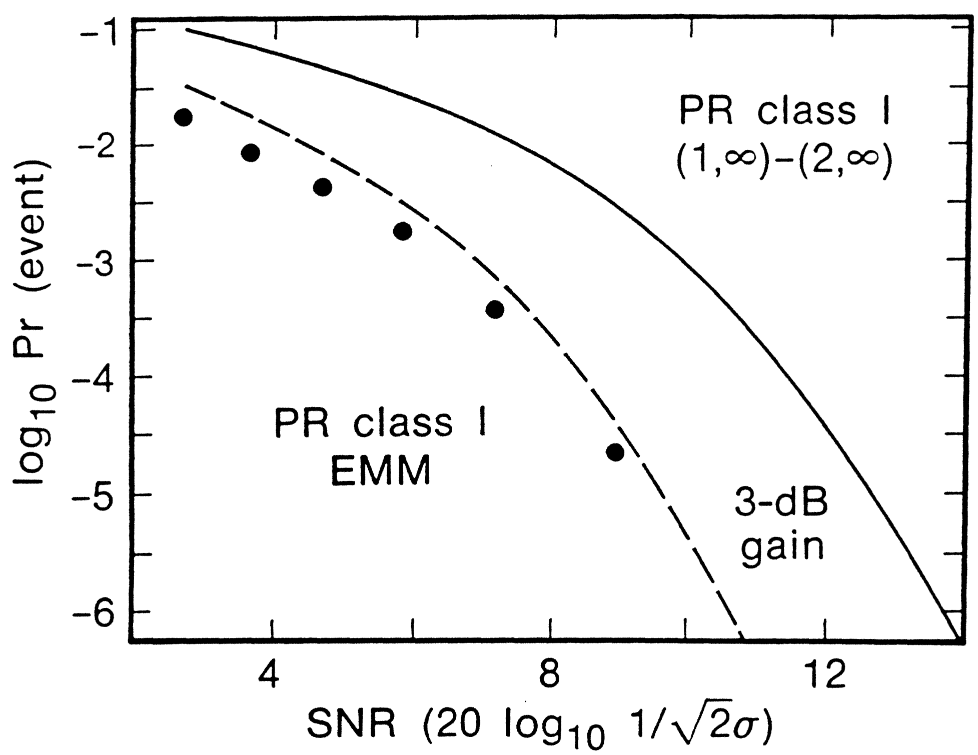


Detector trellis
EMM/PR1



Detector trellis
EMM/PR2

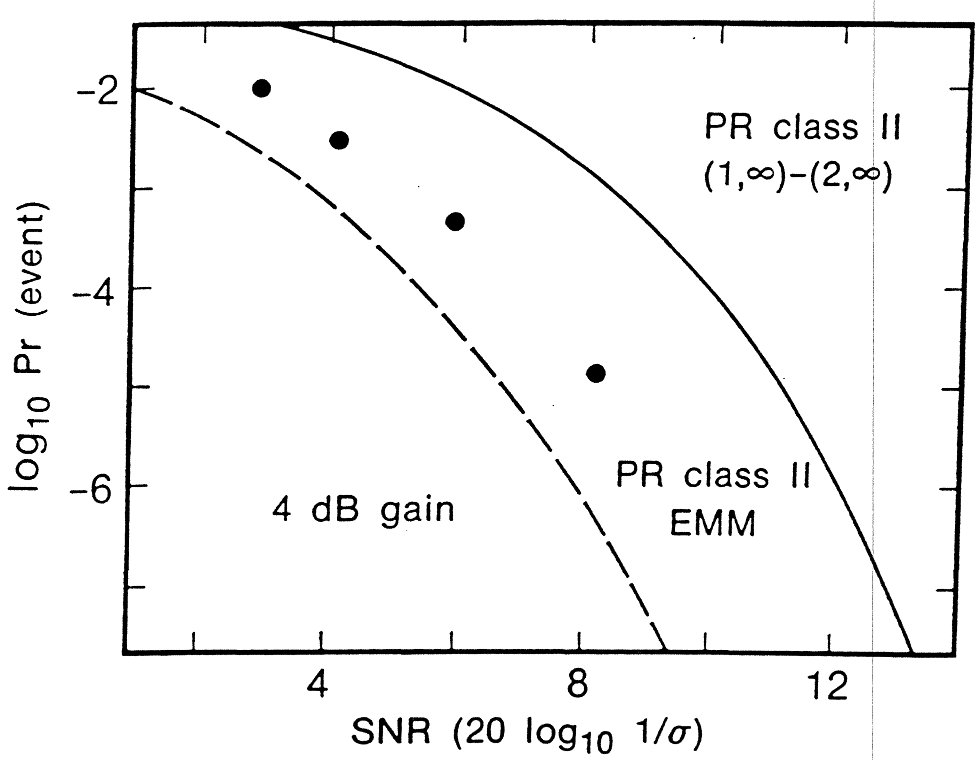
EMM/PR1 PERFORMANCE
(simulated)



- Additive white gaussian noise

$$n_i \sim N(0, \sigma^2)$$

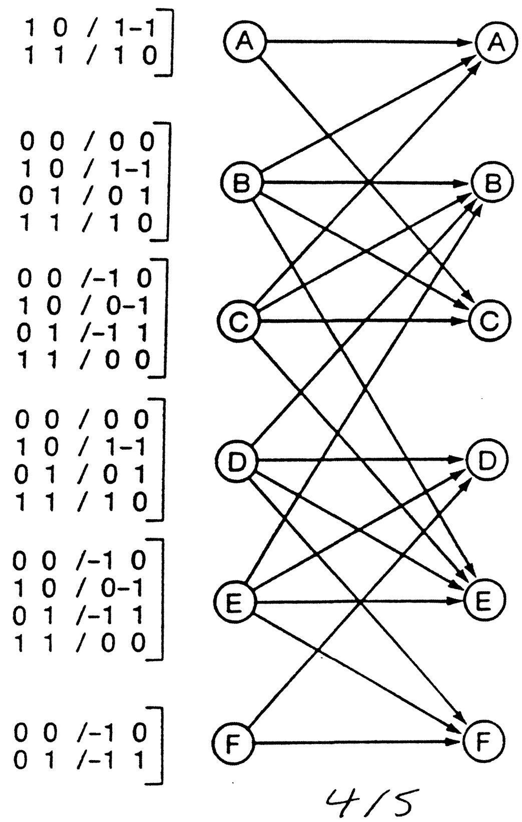
EMM/PR2 PERFORMANCE (simulated)



- Additive white gaussian noise

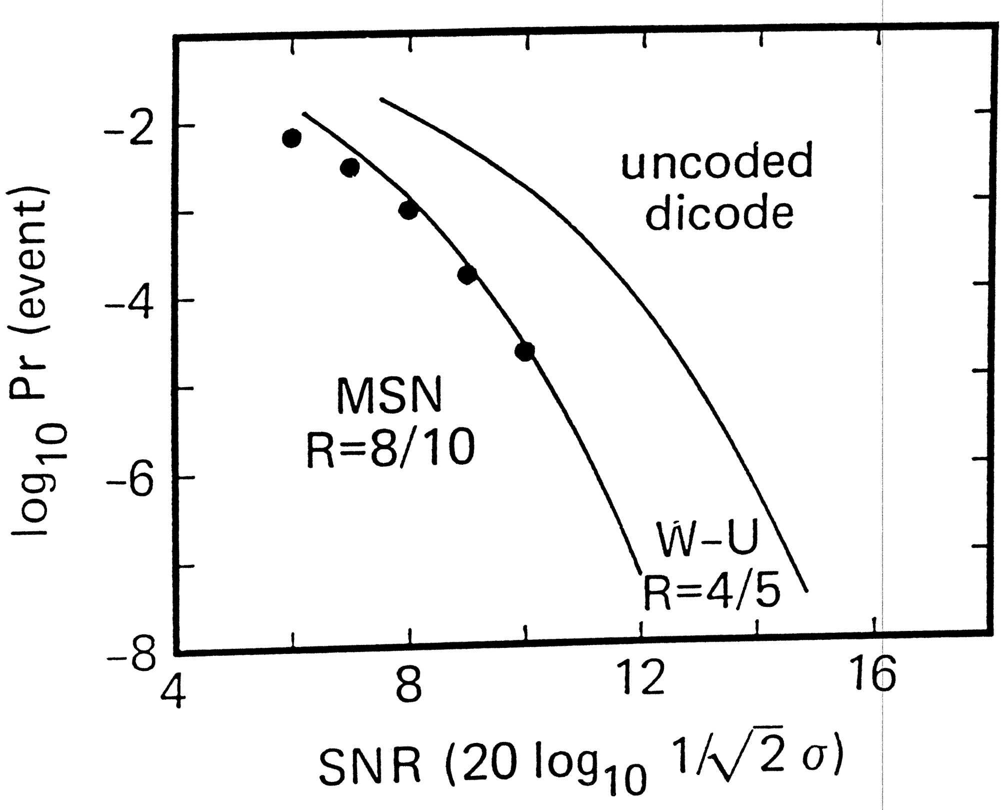
$$n_i \sim N(0, \sigma^2)$$

MSN CODE EXAMPLE
(for 1-D)



- Rate 8/10, gain 3dB
- (0, G/I) = (0, 10/5) when interleaved
- Reduced complexity trellis
- 2-state encoder, block decoder

TRELLIS CODE PERFORMANCE
(simulation)



- Confirms 3dB coding gain with AWGN

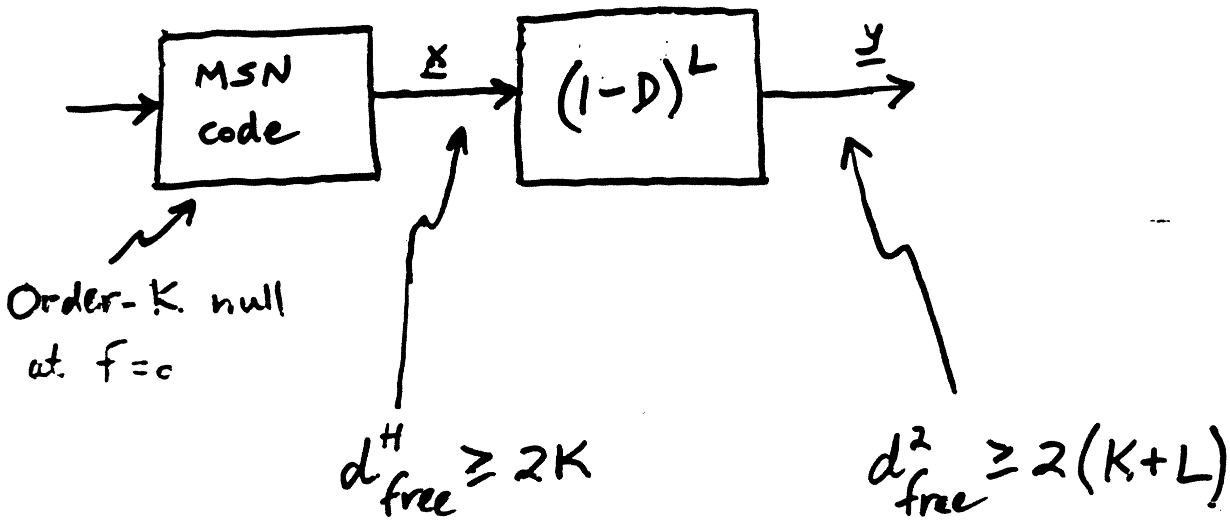
MSN CODING GAIN

- Order-K null at $f = \frac{k}{mT}$

$$S(f) = S^{(1)}(f) = \cdots = S^{(2K-1)}(f) = 0$$

power spectrum

- Theorem (sketch for $f=0$, binary code)

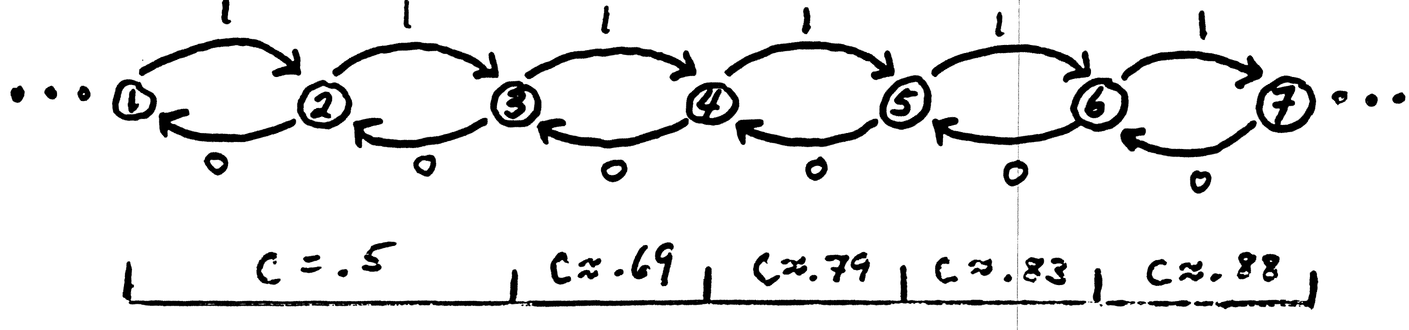


- Generalizes to multilevel codes

MSN CODE DESIGN

- "Canonical diagram" representation of sequences with order-K null(s).

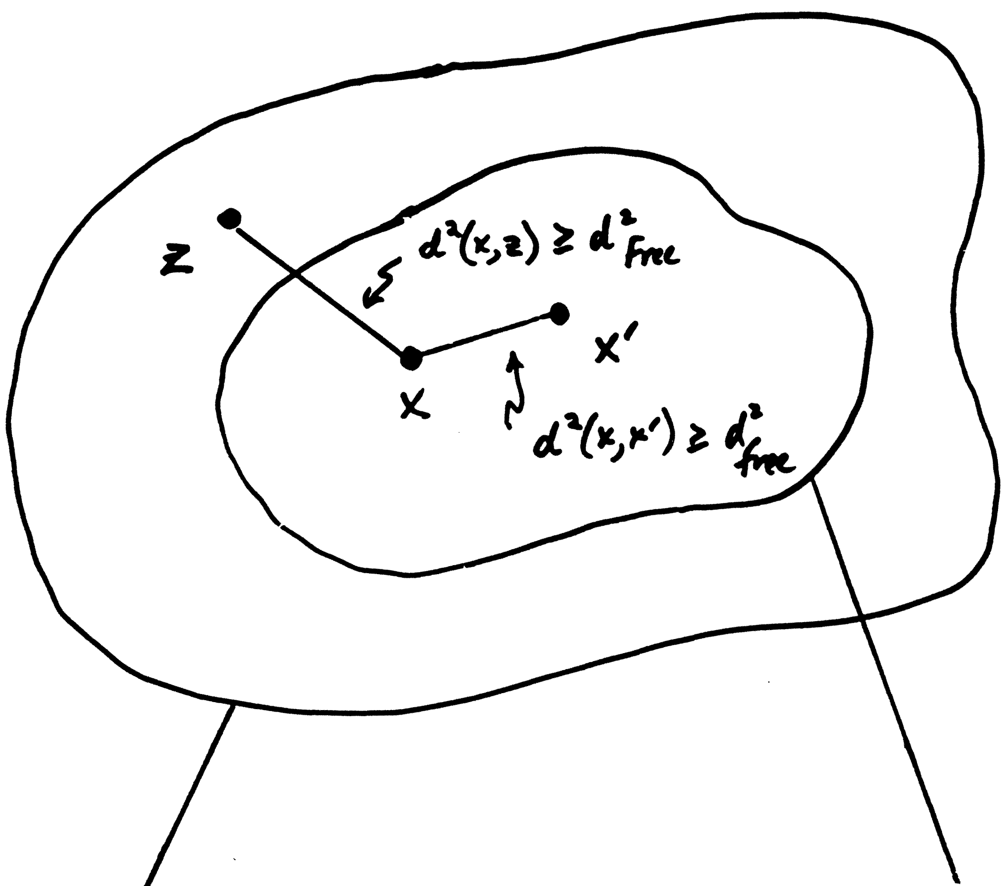
  $f=0 \;,\; K=1 \;\Rightarrow\; G_0'$



- Sliding block code construction
  - Choose desired rate R
  - Pick subdiagram $S \subset G_0'$ with $R < C_S$
  - Apply sliding block code algorithm
    [A-C-H, K-M]

REDUCED COMPLEXITY MSN DETECTOR TRELLIS

- Detector trellis derived from spectral null constraint, not from actual encoder.



spectral null sequences	MSN code sequences
6 states	4 states
20 edges	1024 edges
2 symbols/edge	10 symbols/edge

VLSI DESIGN
FOR
RATE 8/10 MSN CODE

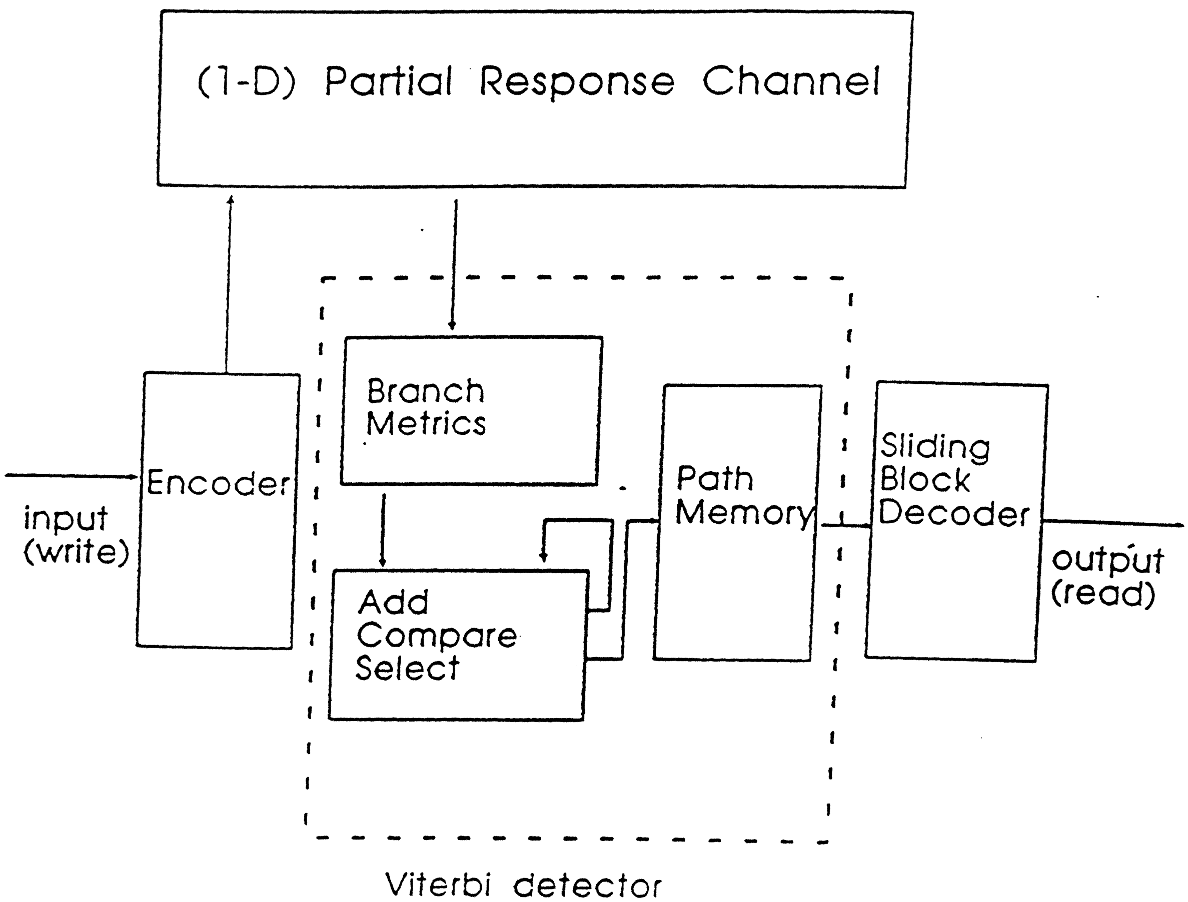
- ARCHITECTURE

- LAYOUT

- FUNCTIONAL EVALUATION

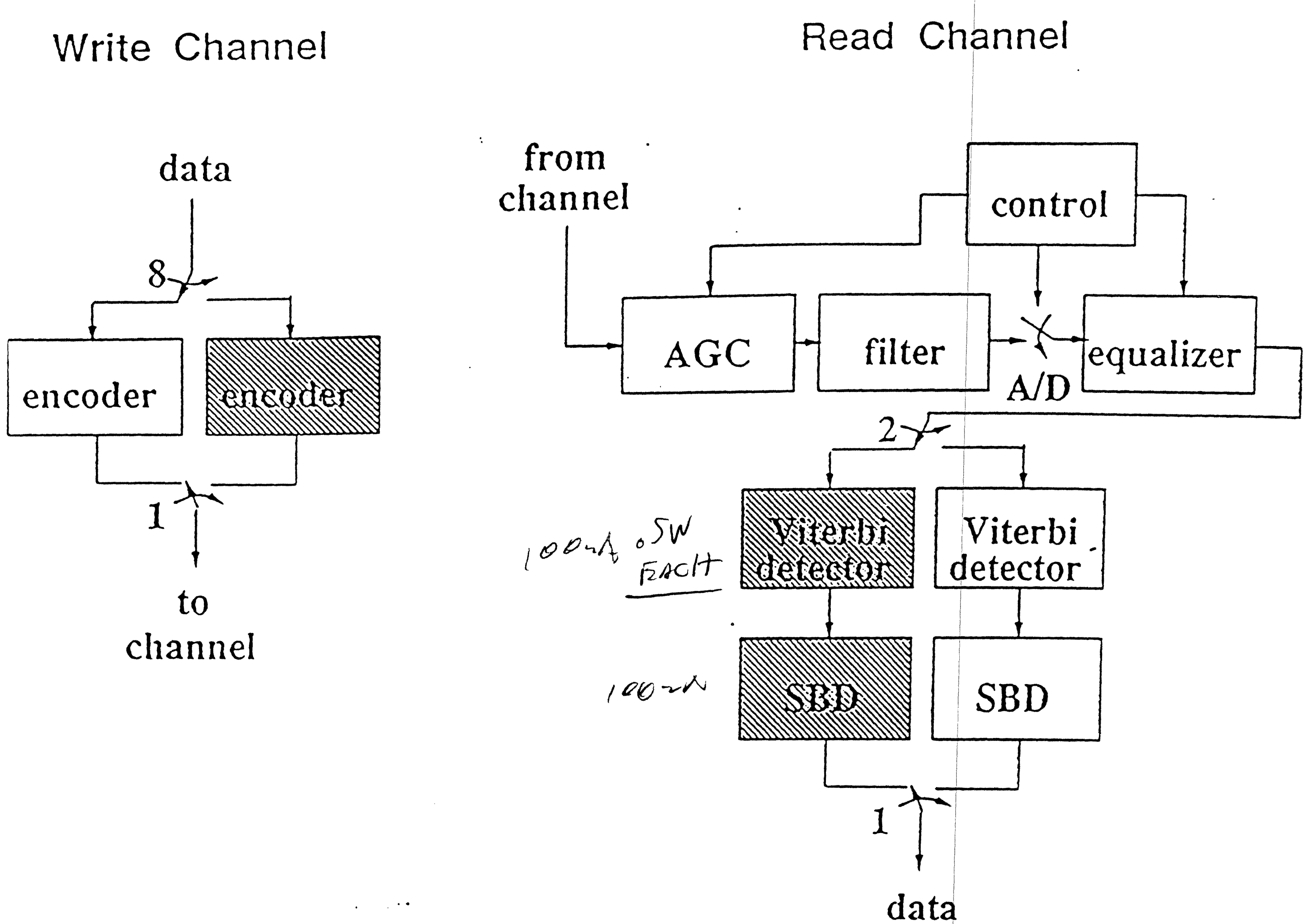
(Chip designer: Prof. C. B. Shung)

CHIP BLOCK DIAGRAM



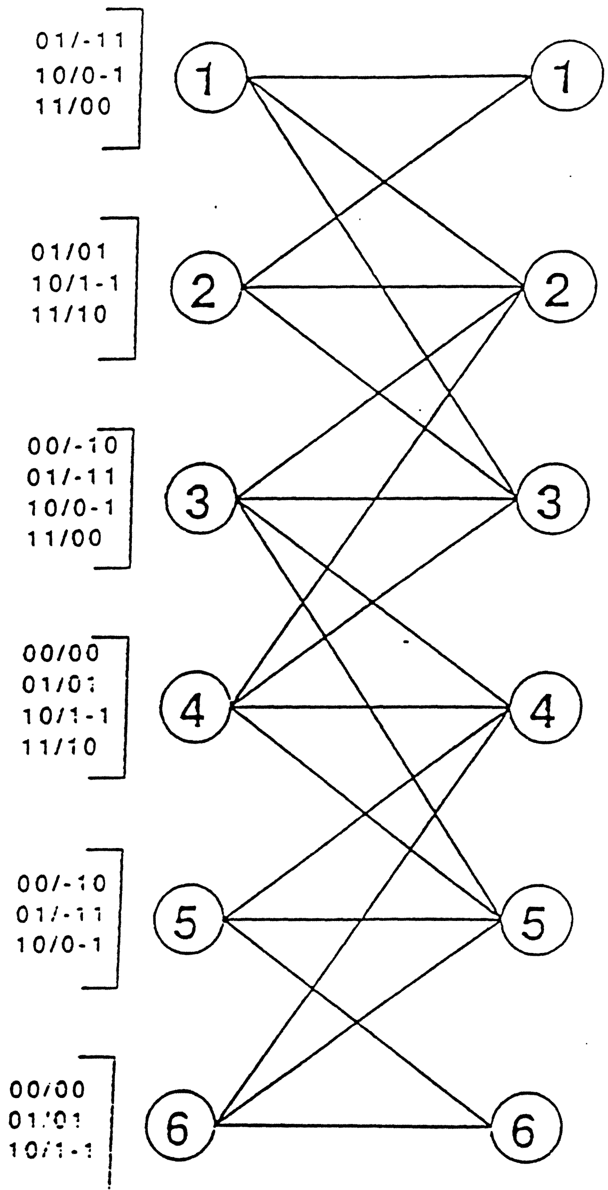
- Main architectural features
  - Modulo metric normalization
  - Pipelined ACS architecture

CHIP APPLICATION TO PRML



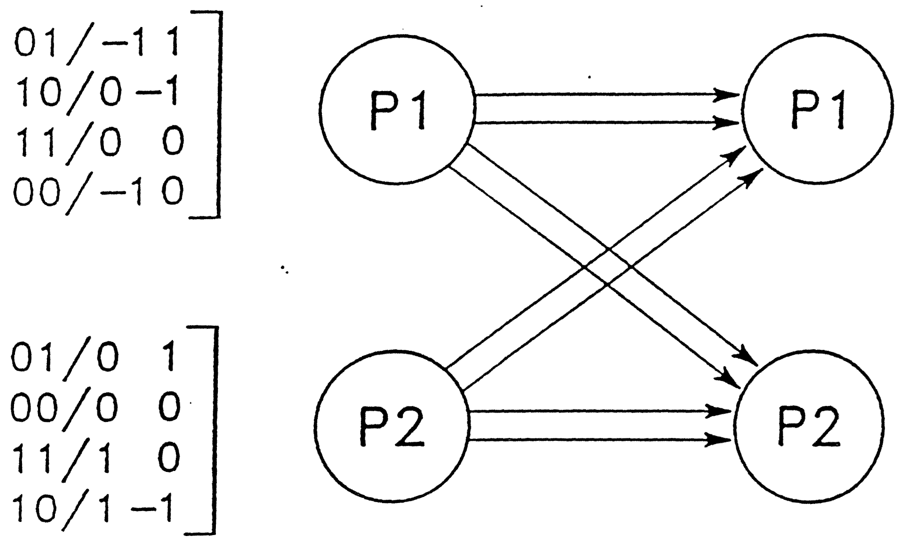
- 2 chips interleaved for PR4

MSN Trellis in Chip



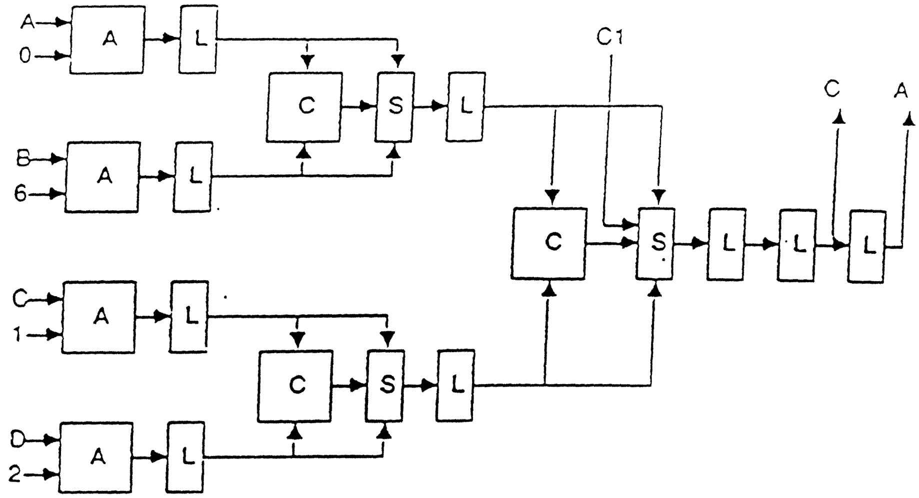
- Variation on trellis shown earlier

TRELLIS EMULATION VIA PIPELINING

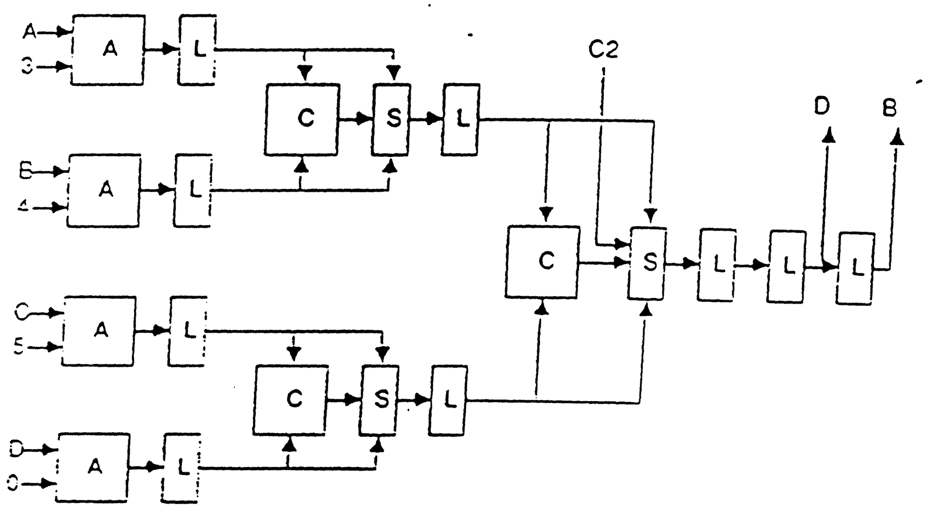


- 2-state trellis that emulates 6-state MSN trellis.

PIPELINED ACS CIRCUIT



ACS1



ACS2

- Legend

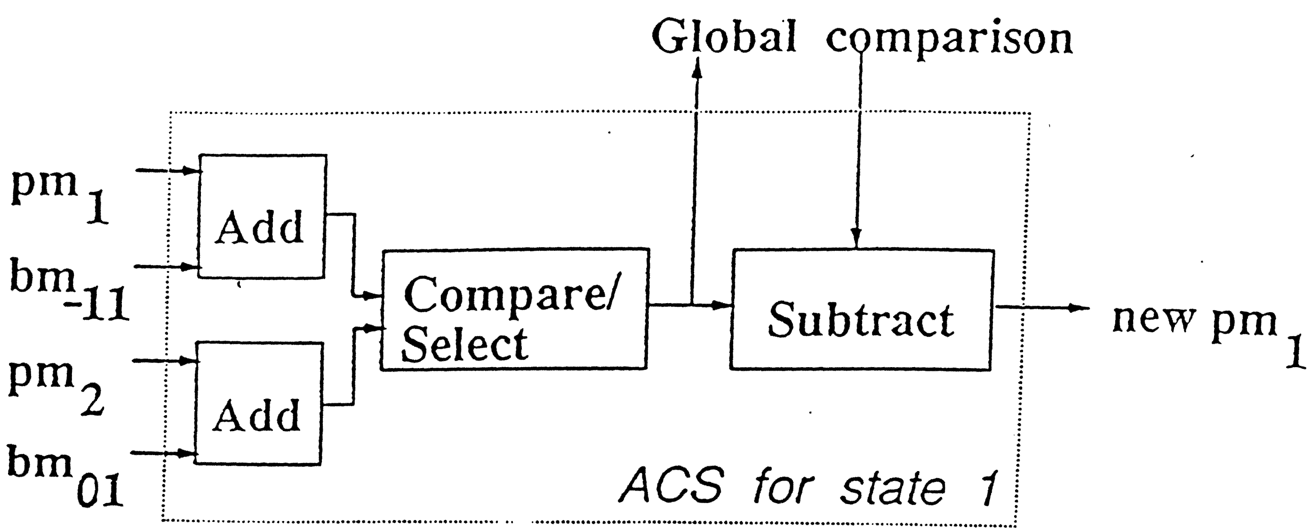
  A = adder
  C = comparator
  S = selector
  L = latch

Pipelined State Schedule

ACS Schedule

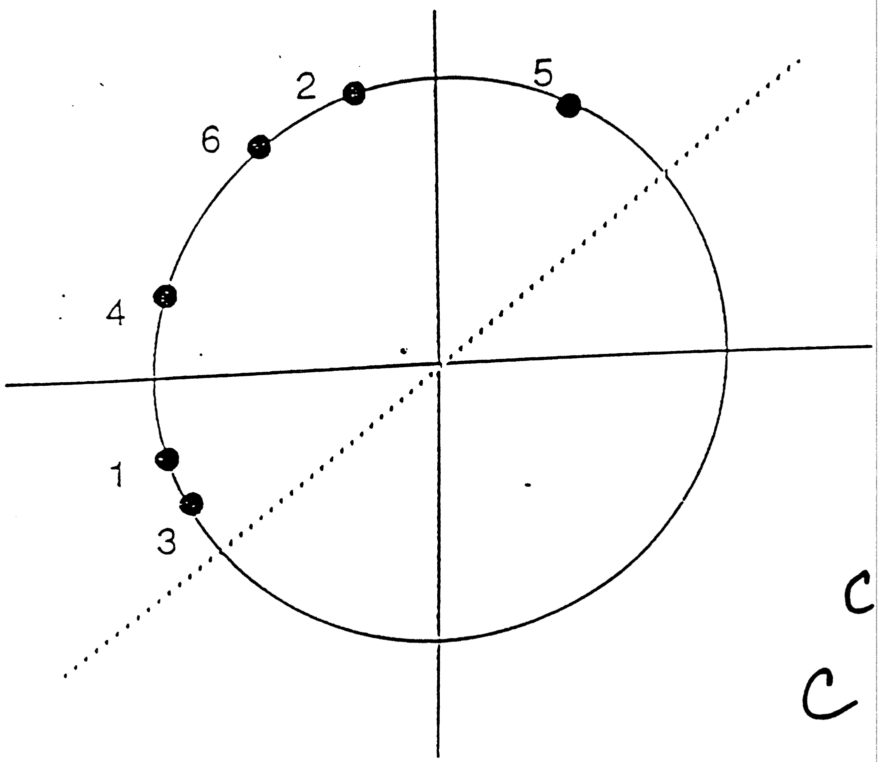
Stage T+1	Stage T	Stage T−1	
7 5 3 1	7 5 3 1	7 5 3 1	← P1
6 4 2 8	6 4 2 8	6 4 2 8	← P2

METRIC RENORMALIZATION
(CONVENTIONAL APPROACH)



MODULO NORMALIZATION

- Two's-complement arithmetic
- Uses bound Δ on path metric differences

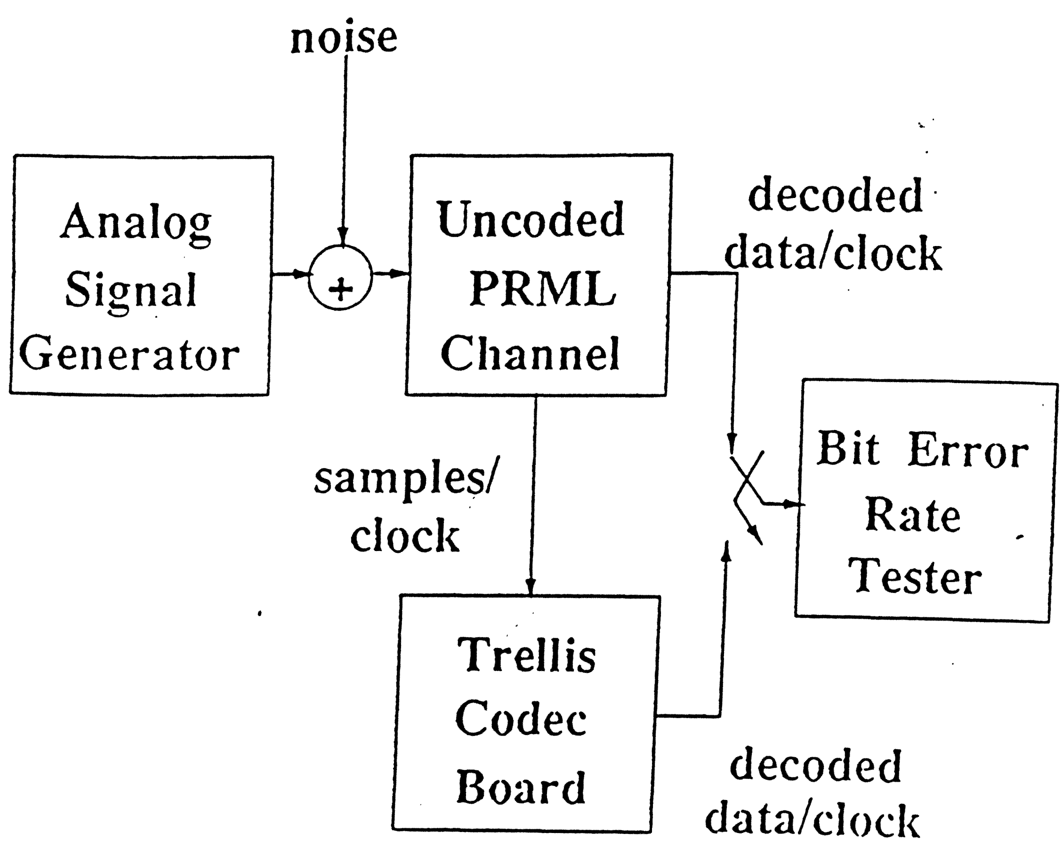


Circumference

$C = 2\Delta$

- Local and regular
- Compatible with pipelined ACS architecture

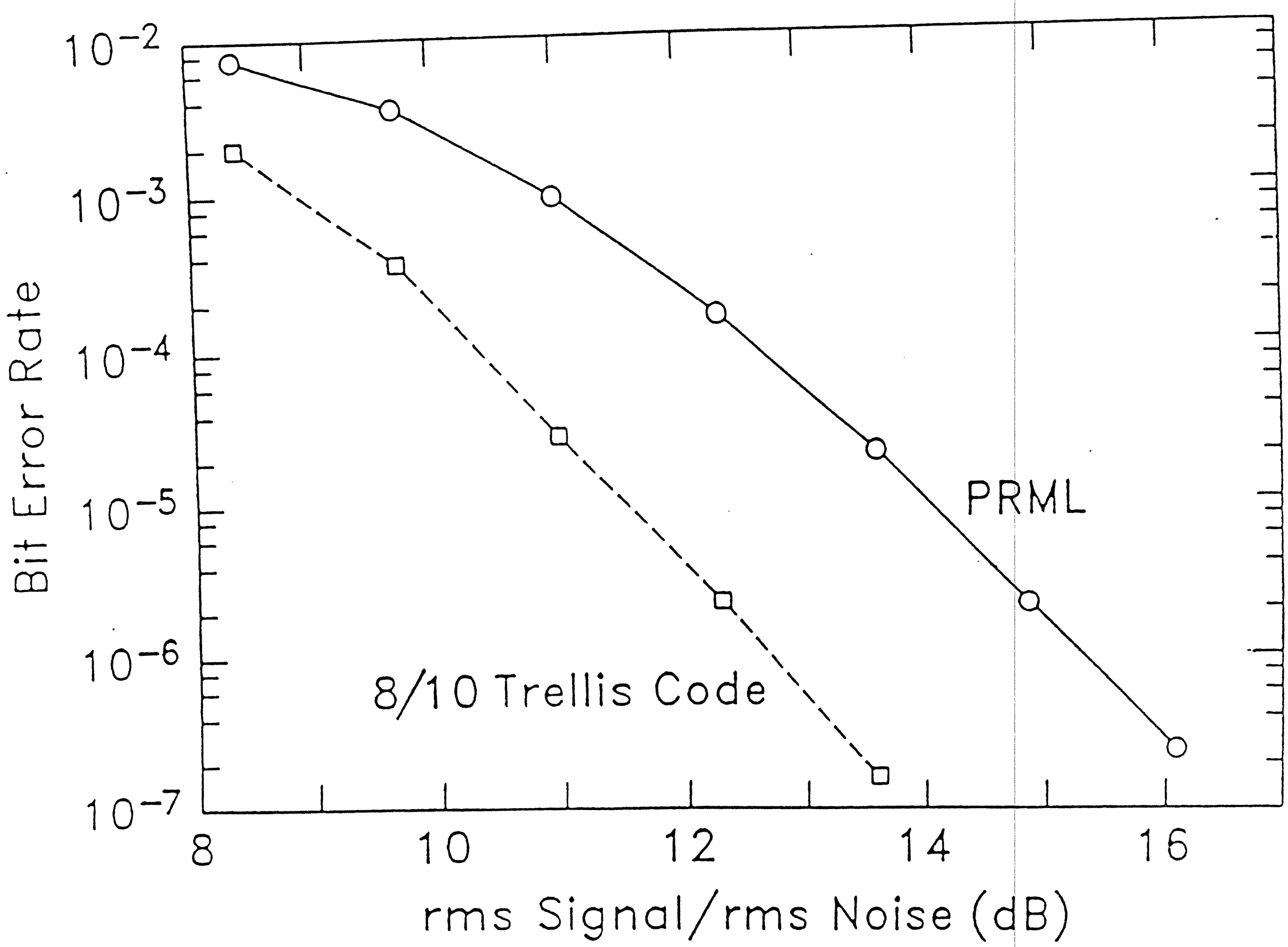
PERFORMANCE EVALUATION
(experimental set-up)



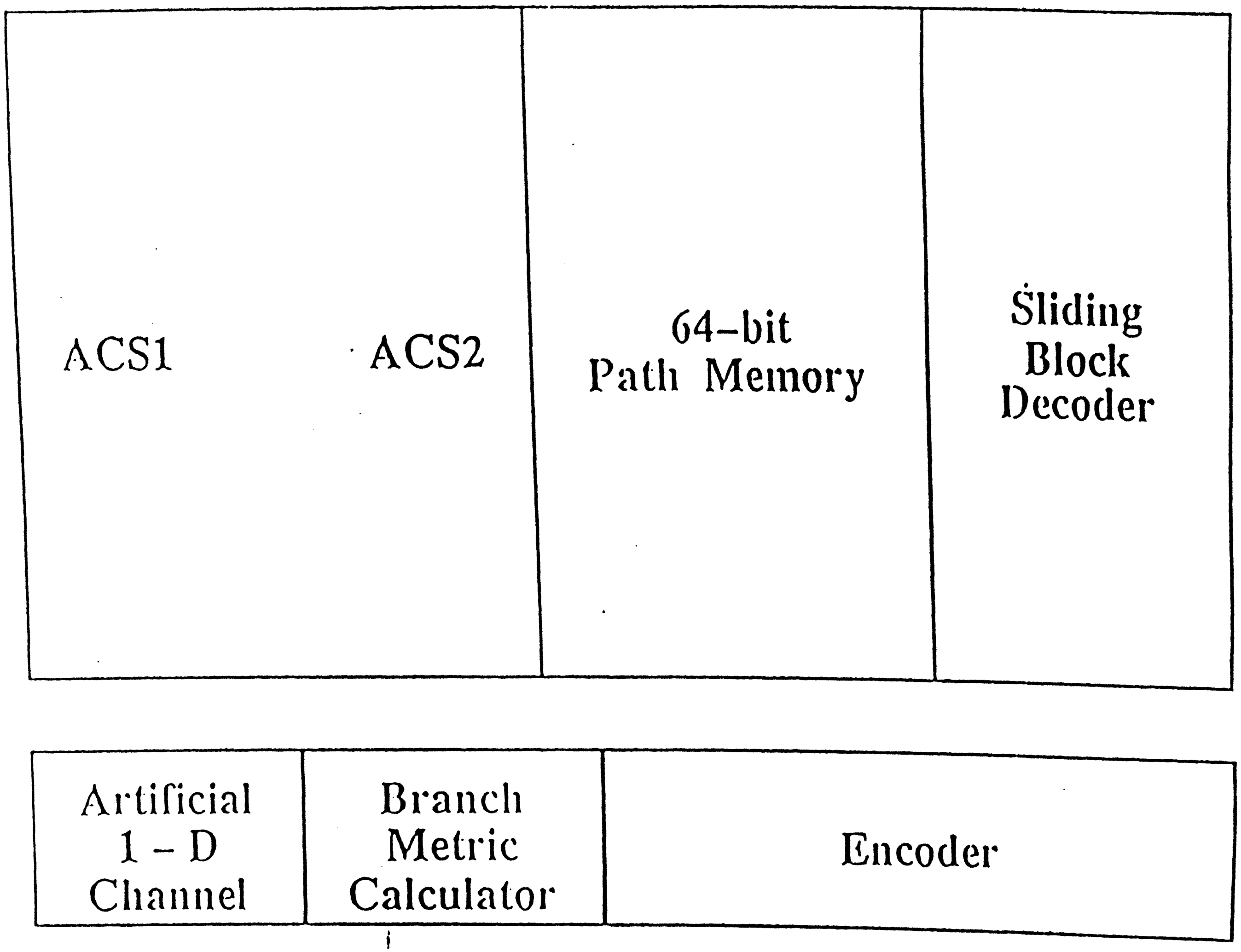
5 1W = 5 x .2004/A

MEASURED BENCH-TEST RESULTS

- MSN-coded PR vs. PRML
- Synthesized PR waveforms
- Injected AWGN

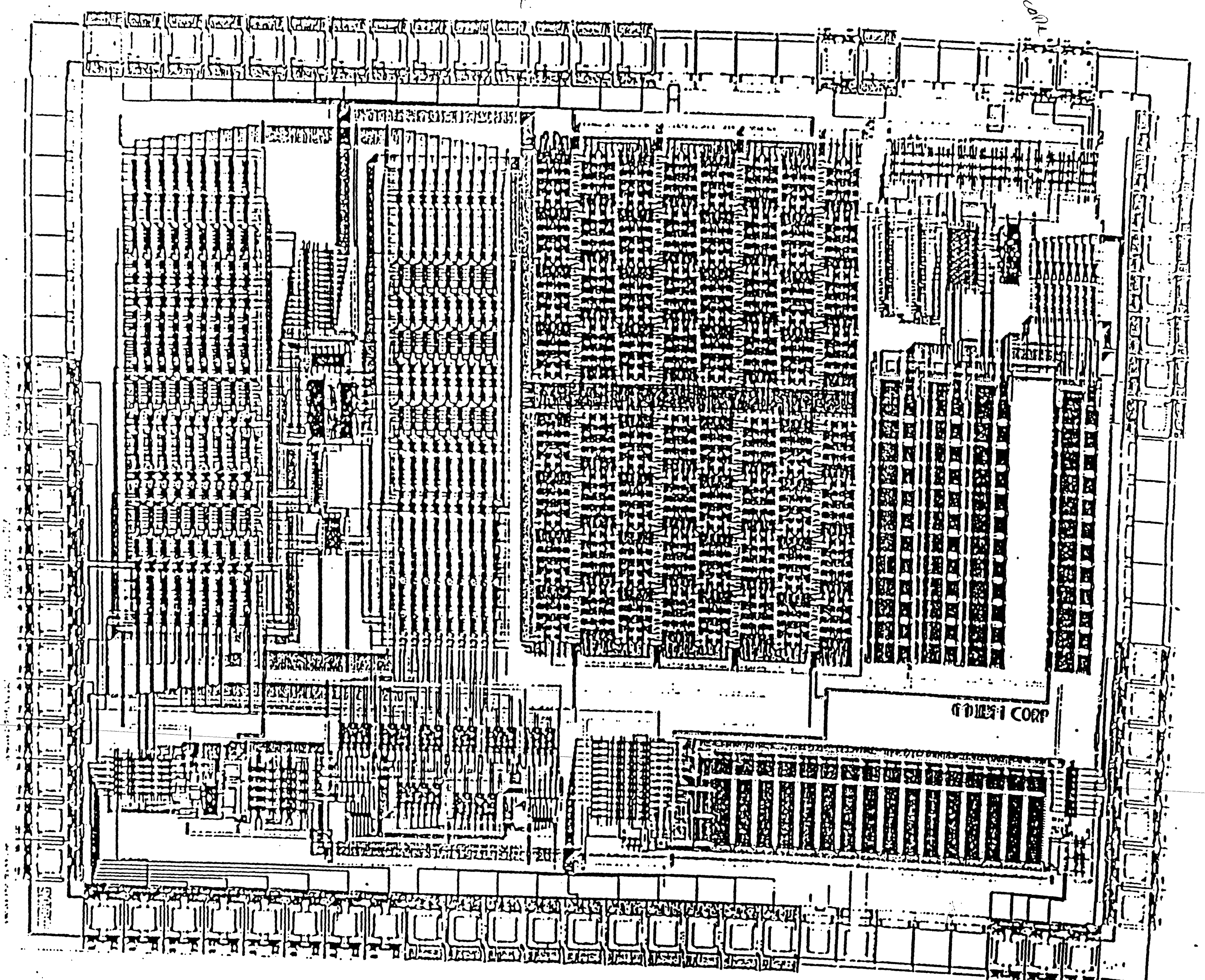


TRELLIS CODE CHIP FLOORPLAN



Trellis

Encoder



Decoder

TRELLIS CHIP MICROGRAPH

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CHARACTERIZATION OF DISK DRIVE COMPONENTS USING DSP TECHNIQUE

AVTAR SINGH

CAMBRIAN SYSTEMS, INC.

CONTENTS

1. INTRODUCTION

- Analog Signal Process (ASP) based ATE
    - Head tester
        - Parametric tester
        - Phase margin tester
        - Time interval analyzer
    - Disk Certifier
        - MP, EP, MOD tester
        - Window margin tester
    - Glide tester
    - Flying height tester
        - Digital
            - Average flying height measurement
            - Dynamic flying height measurement
        - Analog
    - et el
- Digital Signal Process (DSP) based ATE

2. PARAMETRIC TESTING

(A) TRACK AVERAGE AMPLITUDE

- ANALOG SIGNAL PROCESSING CAN PROVIDE AVERAGE TAA.

DSP APPROACH CAN PROVIDE

- AVERAGE TAA
- POSITIVE / NEGATIVE MODULATION
- CONTRIBUTION DUE TO MISREGISTRATION OF READ HEAD
- CONTRIBUTION DUE TO SPINDLE JITTER, AXIAL & RADIAL NON-REPEATABLE RUN OUT.

(B) O/W MEASUREMENT

- ASP TECHNIQUE USES BAND PASS FILTER OR SPECTRUM ANALYZER.

DSP APPROACH CAN PROVIDE

- DSP USE FFT ANALYSIS
- CONTRIBUTION DUE TO SPINDLE JITTER & RUN OUT
- CONTRIBUTION DUE TO MISREGISTRATION OF READ HEAD.

20MBIT/SEC TESTER CLOCK RATE
NEED MORE MEMORY IN DSP TEST
SYSTEM THAN ANALOG METHOD.

(C) NOISE MEASUREMENT

HEAD NOISE

- JOHNSON THERMAL NOISE
- BARKHAUSEN NOISE
- MAGNETIC DOMAIN INSTABILITY
  - AMPLITUDE MEASUREMENT
  - PULSE WIDTH MEASUREMENT PW25
  - HEAD BIAS TECHNIQUE BIAS CURRENT $\leq$ 3% OF I_w

UNSTABLE HEAD $\approx$ 2%

HIGH SPEED ADC AND DSP.

MEDIA NOISE

- SA TECHNIQUE
- TRUE-RMS VOLTMETER TECHNIQUE
- REVERSE DC ERASE TECHNIQUE
- MEDIA EDGE NOISE

(D) WAVE SHAPE ANALYSIS

- PULSE WIDTH
- UNDERSHOOT
- ASYMMETRY
- SPECTRUM
- RISE / FALL TIMING
- NON-LINEAR RESPONSE

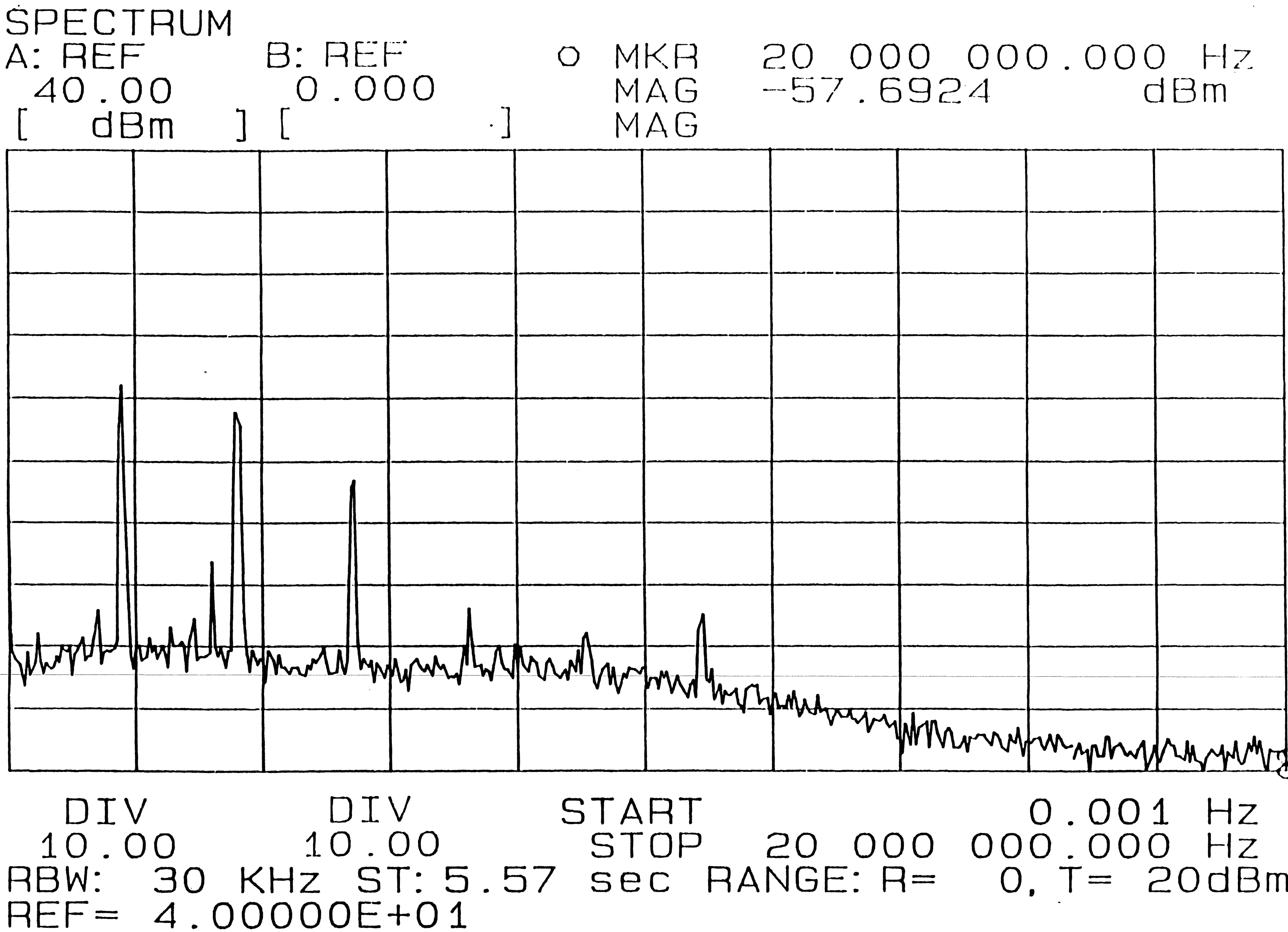


Fig. 1. TRANSITION NOISE OF MEDIUM.

3. TOTAL TIMING ERROR

I . HEAD / MEDIA / PREAMP NOISE

II. INTER SYMBOL INTERFERENCE

III. PEAK SHIFT DUE TO HARD TRANSITION EFFECT

IV INTER TRACK INTERFERENCE

V NON-LINEAR DISTORTION

I. HEAD / MEDIA / PREAMP NOISE

Peak Shift based on SNR

Simple approximation

$$Te = [\ Ts/4.2]\ \sqrt{-\log_{10}(4.2 * Pe)}\ /\ SNR$$

where

$$10^{-22} < Pe < 10^{-3}$$

Ts = Time period for highest frequency

Te = timing error

Pe = error probability per bit

SNR = signal to noise ratio (rms to rms)

Let us say SNR = 30

5MHz Freq

$T_e \approx 4.8 ns$

G.H.Hughes & R.K.Schmidt, " On noise in digital recording", IEEE Trans Mag, Vol. MAG-12, No.6 pp 752.

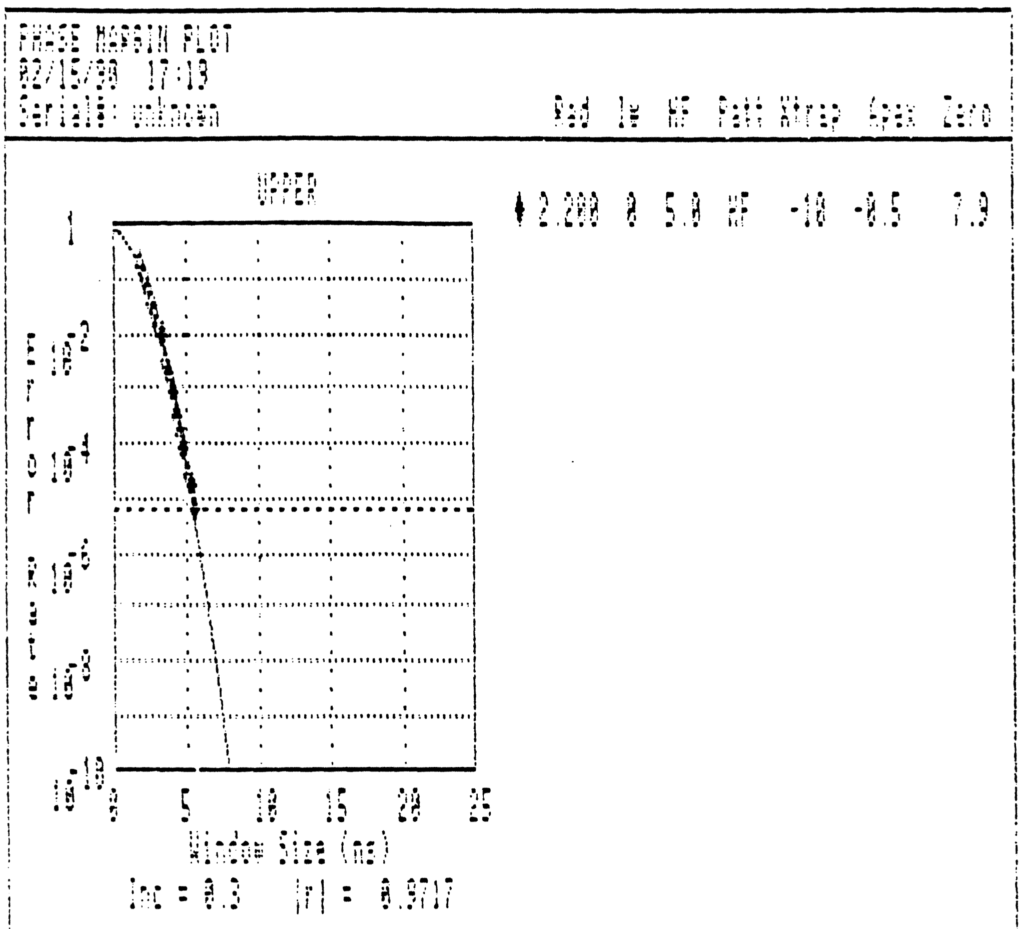


Fig 3 : Phase margin plot for (1,1) MFM pattern.

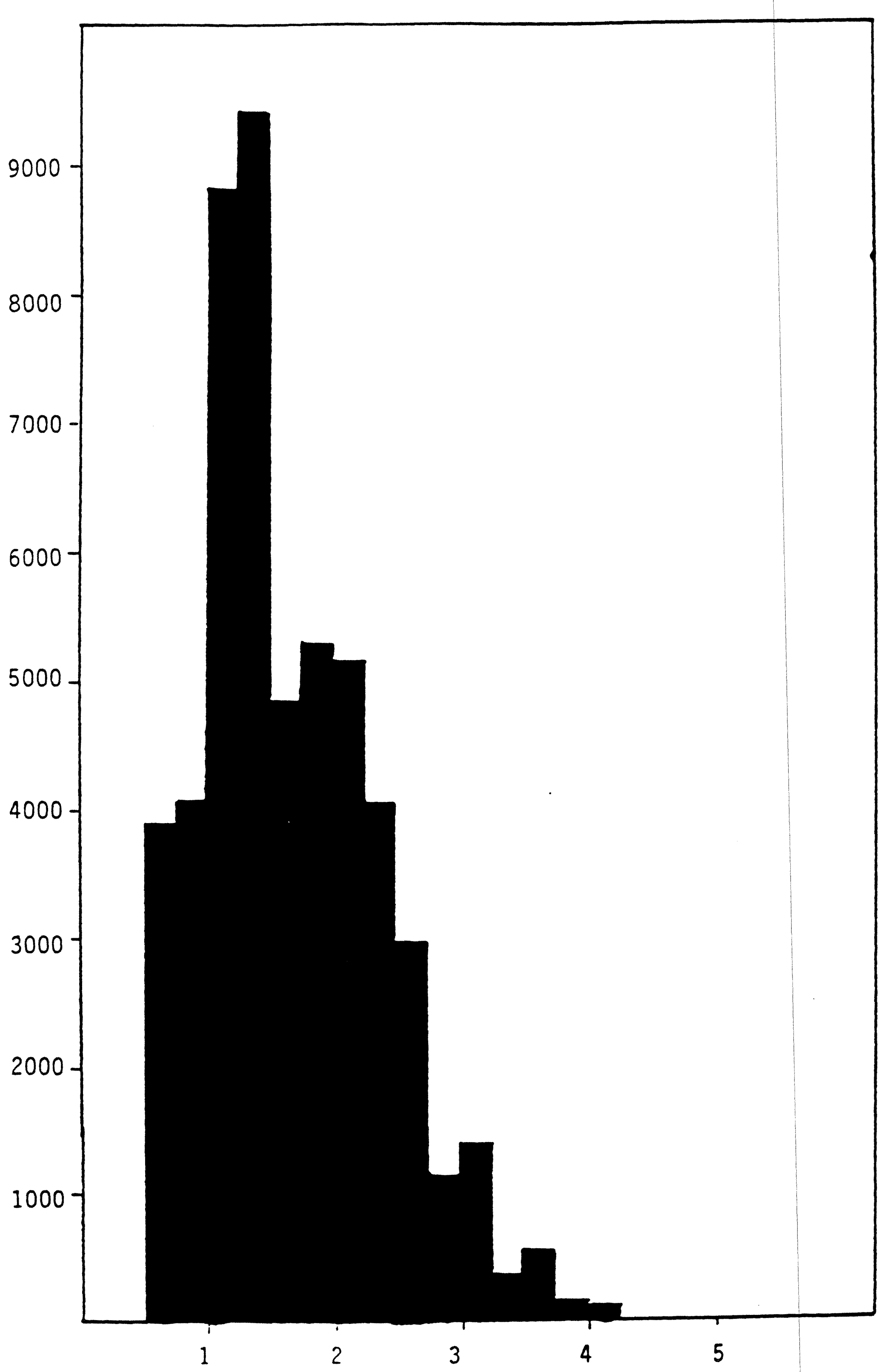


Fig 4 : Peak shift distribution for (1,1) MFM pattern.

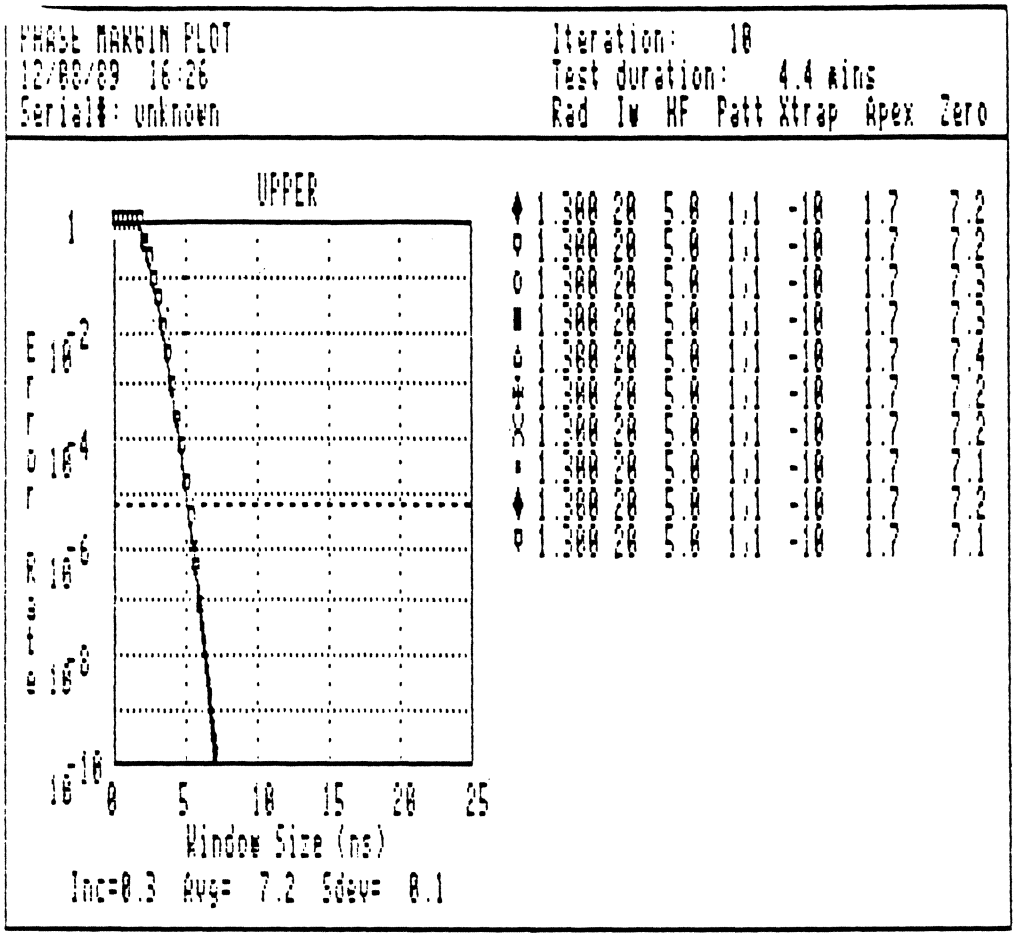


Fig 5: Phase margin plot for (1,1) pattern showing apex.

II. INTERSYMBOL INTERFERENCE

TFH PEAK SHIFT CALCULATIONS

$$V(K) = \frac{2\ V\ W\ Mr}{2} \cdot \frac{1 - e^{-Kt}}{Kt} \cdot \frac{e^{-K(d+a)}}{1} \cdot G(K) \quad \ldots (1)$$

$$K = \frac{2\ f}{V} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$$G(K) = \frac{SIN\ (gK)}{gK} - \frac{1}{2(1+C)} \left\{ \frac{A}{A-jK(g+p1)} + \frac{BC}{B-jK(g+p1)} \right\} e^{jK(g+p1)}$$

$$- \frac{1}{2(1+C)} \left\{ \frac{A}{A-jK(g+p2)} + \frac{BC}{B-jK(g+p2)} \right\} e^{jK(g+p2)} \quad \ldots\ldots (3)$$

$$a = \left(\frac{a1}{2r} - \frac{t}{4}\right) + \left[\left(\frac{a1}{2r} - \frac{t}{4}\right)^2 + \left(\frac{t}{2} + 2t\ \frac{Mr}{4Hc}\right) \frac{a1}{r} \right]^{1/2}$$

$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

$$V(X) = \frac{1}{T} \sum_{n=1}^{\infty} V(nK) \cdot \left\{ SIN\left(n.\frac{2\pi}{T}.x\right) - SIN\left(n.\ \frac{2\pi}{T}(x+T1)\right)\right.$$

$$\left. - SIN\left(n.\ \frac{2\pi}{T}(x+T2)\right)\right\} \cdot \left\{(1 - COS(n\pi)).(i)^{n-1} \right\} \quad \ldots\ldots (5)$$

Where T = time period for isolated pulse

T1 = time period between positive peaks.

T2 = time period between positive and negative peak.

A.Singh & P.G.Bischoff," Optimization of thin film heads for Resolution, Peak shift and overwrite", IEEE Trans Mag, Vol. MAG-21, No.5 pp 1572.

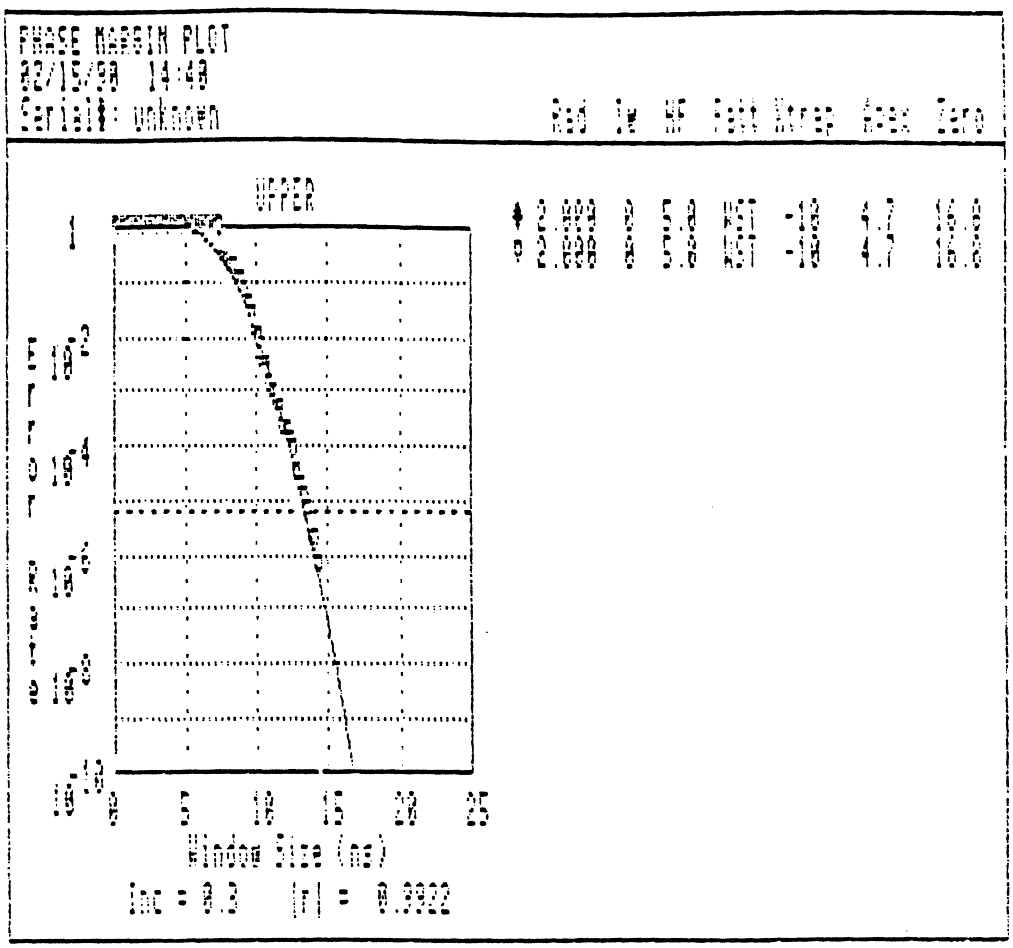


Fig 6: Phase margin plot for (1,3) MFM pattern.

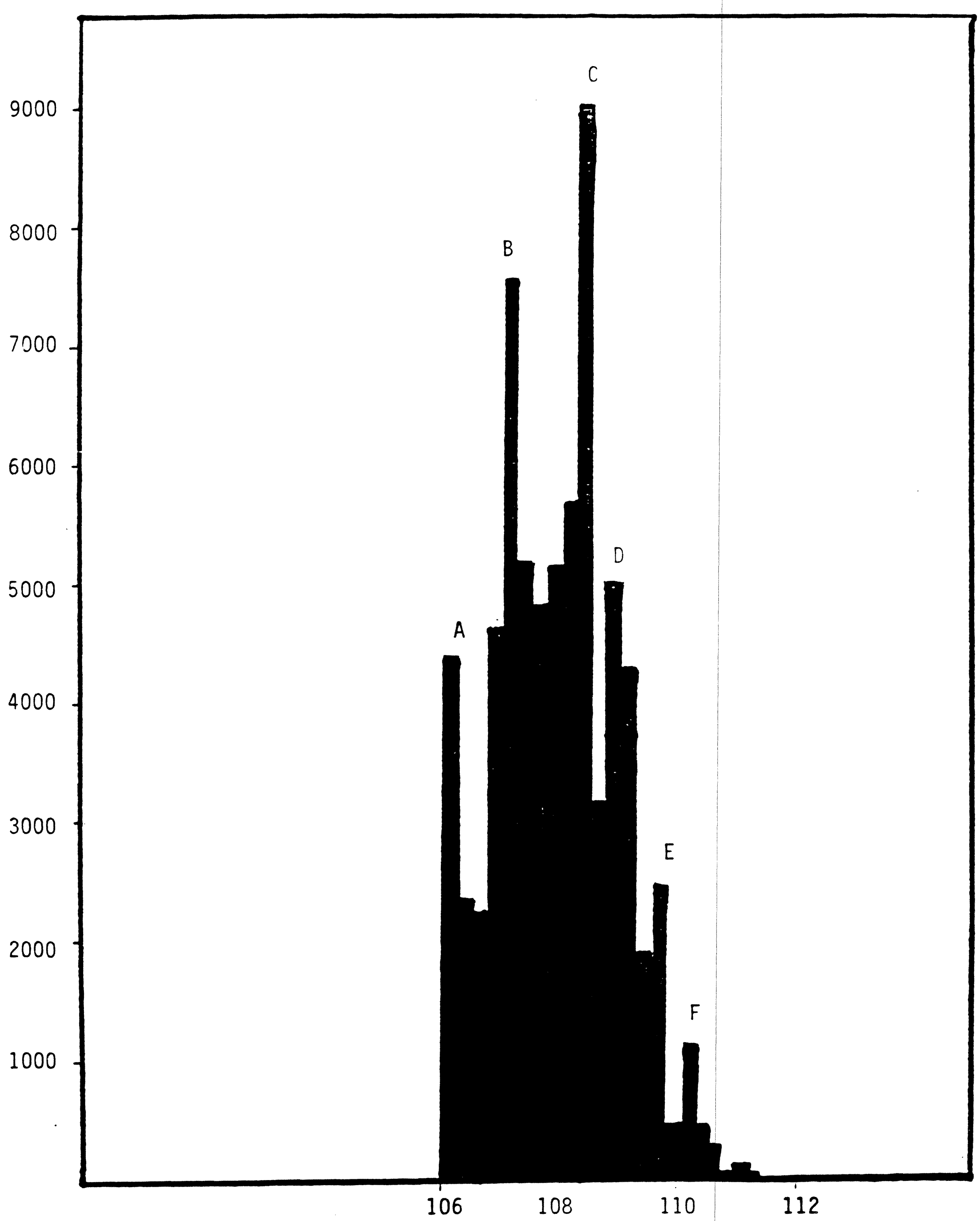


Fig 7: Peak shift distribution for (1,3) MFM pattern.

III - PEAK SHIFT DUE TO HARD TRANSITION EFFECT

$$\frac{P\left[2\cdot f_D - f_B\right]}{P\left[f_D\right]} = 2\cdot\left[2\cdot f_D - f_B\right]\cdot\left|\left[\frac{E\left[2\cdot f_D - f_B\right]}{E\left[f_D\right]}\right]\right| t$$

Where P(f) denotes the intensity of a spectral peak at frequency f .
E(f) denotes the amplitude of the Fourier Transform of the the easy transition waveform at frequency f and t is the hard transition peak shift in time.

$$t = OWO \left[\frac{500}{2f_D - f_B}\right]$$

over write

C. Tsang, Y. Tang, "An experimental study of hard transition peakshifts through the overwrite spectra.", IEEE Trans. Magn., MAG-24, 6 (1988).

PEAK SHIFT DUE TO HARD TRANSITION EFFECT

Algorithm:

1. Write low frequency Cw fb.

2. Then write high frequency fd.

3. Measure spectral peaks

Overwrite parameter OWP =

$$OWP := \frac{P\left[2 \cdot f_D - f_B\right]}{P\left[f_D\right]}$$

4. Measure spectral ratio RO

$$RO := \frac{E\left[2 \cdot f_D - f_B\right]}{E\left[f_D\right]}$$

$$\blacksquare := \frac{f_D}{\left[2 \cdot f_D - f_B\right]} \cdot \frac{V\left[2 \cdot f_D - f_B\right]}{V\left[f_D\right]}$$

5. Normalize OWP to remove effect of head disk resolution

$$OWQ := \frac{OWP}{RO}$$

6. Hard transition peak shift t

$$t := OWQ \cdot \left[\frac{500}{\left[2 \cdot f_D - f_B\right]}\right]$$

where t is in nanoseconds & fD and fB are in MHz.

C. Tsang, Y. Tang, "An experimental study of hard transition peakshifts through the overwrite spectra.", IEEE Trans. Magn., MAG-24, 6 (1988).

IV INTERTRACK INTERFERENCE

- ITI IS ONE OF THE MAIN CAUSES OF TIMING ERROR.

- ITI CONTRIBUTION TO TIMING ERROR IS EMBEDDED IN THE PHASE MARGIN PLOT.

- DSP TECHNIQUE CAN BE USED TO MEASURE TRACK MISREGISTRATION.

- TECHNIQUE CAN BE FURTHER MODIFIED TO PROVIDE TIMING ERROR DUE TO INTERTRACK INTERFERENCE.

T.J.Chainer et al," A technique for the measurement of track misregistration in disk file," paper presented at MMM- Intermag Conf. Pittsburg, Pennsylvania,1991.

4. PHASE MARGIN CIRCUIT DESIGN & ANALYSIS

(A) FILTER DESIGN

- NOISE MINIMIZATION
- PRESERVE WAVE SHAPE
- CONSTANT GROUP DELAY
- LINEAR PHASE
- CORRECT ERRORS INTRODUCED BY THE NON-IDEAL PHASE CHARACTERISTICS OF INPUT READ HEAD
- PROGRAMMABLE TRACKING FILTER
  (ONLY IF SNR BETTER THAN 60 DB)

DSP TO ANALYZE NON-IDEAL PHASE CHARACTERISTICS

- HIGH SPEED ADC
- DIGITAL SIGNAL PROCESSING
  -FFT, CONVOLUTION etc
- DIGITAL FILTER DESIGN FOR ANALYSIS

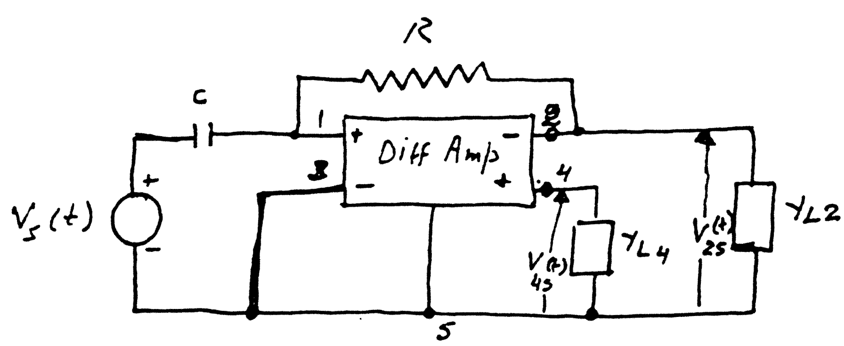
(B) DIFFERENTIATOR DESIGN

THE DIFFERENTIATOR OUTPUT CHANGES STATE WHEN THE INPUT PULSE CHANGES DIRECTION. NORMALLY THIS WILL BE AT THE PEAKS. BUT THE DIFFERENTIATOR CAN ALSO RESPOND TO NOISE NEAR THE BASELINE UNLESS THRESHOLD OR GATING CIRCUIT IS IMPLEMENTED.

(AMPLITUDE COMPARATOR CIRCUIT, ENABLING THE DIGITIZING COMPARATOR CAN BE USED AS GATING CIRCUIT.)

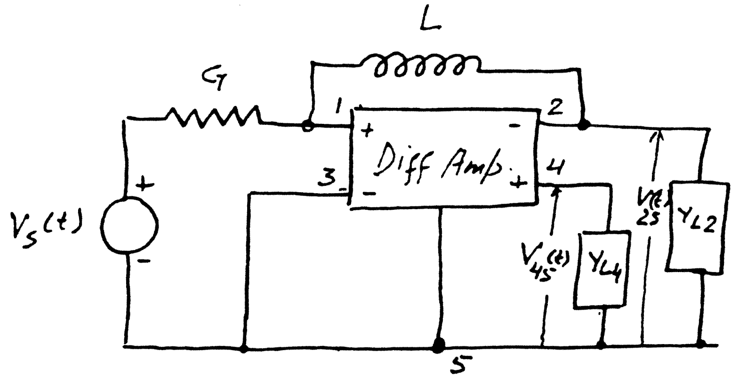
TYPES OF DIFFERENTIATOR

1. **RC DIFFERENTIATOR**
   - SIMPLE
   - PHASE DISTORTION
   - SNR DEGRADATION
2. **GL DIFFERENTIATOR**
   - SNR DEGRADATION
3. **DELAY LINE DEFFERENTIATOR**



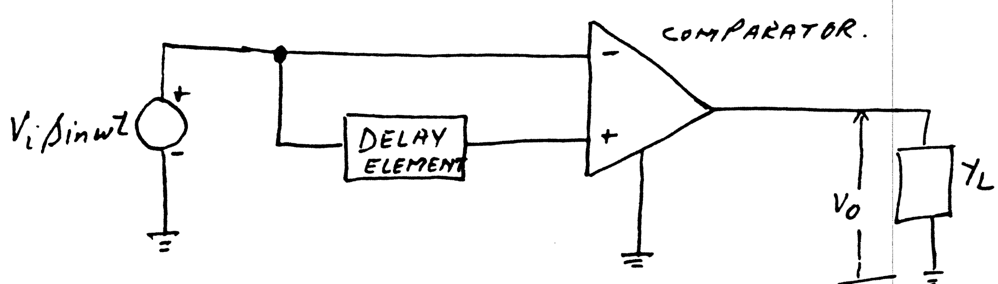
$$V_{25}(t) = -V_{45}(t) = -RC\frac{dV_s(t)}{dt}$$

Fig B-1 RC Differentiator.



$$V_{25}(t) = -V_{45}(t) = -LG\frac{dV_s(t)}{dt}$$

Fig B-2 GL Differentiator.



$$V_0 = K \cos w(t - \frac{t_d}{2})$$

Fig B-3 DELAY LINE Differentiator.

DELAY LINE DIFFERENTIATOR

$$Vo := A \cdot Vi \cdot \sin(w \cdot (t + td)) - A \cdot Vi \cdot \sin(w \cdot t)$$

$$VO := 2 \cdot A \cdot Vi \cdot \sin\left[w \cdot \frac{td}{2}\right] \cdot \cos\left[w \cdot \left[t - \frac{td}{2}\right]\right]$$

$$VO := K \cdot \cos\left[w \cdot \left[t - \frac{td}{2}\right]\right]$$

Where $K := 2 \cdot A \cdot Vi \cdot \sin\left[w \cdot \frac{td}{2}\right]$

K will have the peak value when

$$w := \frac{p}{td}$$

or

$$f := \frac{0.5}{td}$$

Where Vi = input voltage
Vo = output voltage
A = Gain
td = delay
f = cut off frequency of the differentiator

Code = (2, 7) HF = 5Mhz				
Ptrn = FF	Delay Line = 60nS			
Tap	#1	#2	#3	#4
Run #1	8.8	6.9	5.8	5.8
Run #2	8.6	7.0	5.8	5.8
Run #3	8.8	7.0	6.0	5.8
Run #4	8.6	6.9	6.0	5.9
Delay (nS)	18.0	30.0	48.0	60.0
Average	**8.7**	**7.0**	**5.9**	**5.8**
Stdev	**0.1**	**0.1**	**0.1**	**0.1**
Ptrn = (2,7)	Delay Line = 60nS			
Tap	**#1**	**#2**	**#3**	**#4**
Run #1	11.6	11.6	13.1	14.8
Run #2	11.8	11.9	13.1	14.9
Run #3	12.0	11.7	13.2	15.0
Run #4	11.9	11.6	13.3	14.9
Delay (nS)	18.0	30.0	48.0	60.0
Average	**11.8**	**11.7**	**13.2**	**14.9**
Stdev	**0.2**	**0.1**	**0.1**	**0.1**

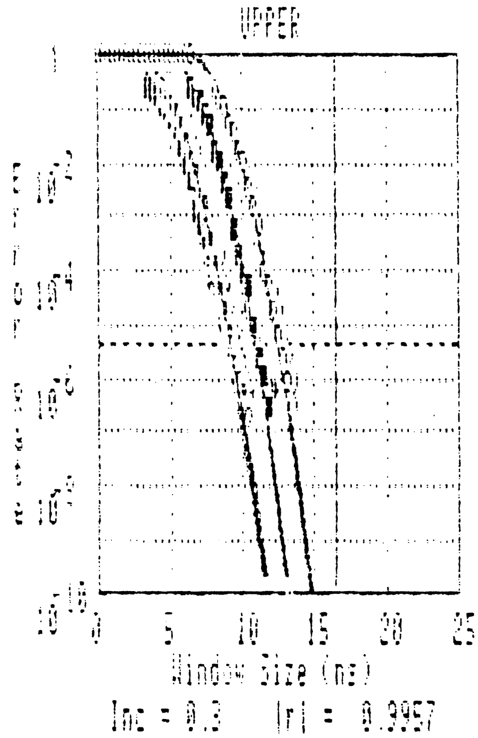
Code = (2, 7) HF = 5Mhz				
Ptrn = FF	Delay Line = 100nS			
Tap	#1	#2	#3	#4
Run #1	7.1	6.6	5.2	5.5
Run #2	7.3	6.7	5.3	5.3
Run #3	7.3	6.8	5.3	5.5
Run #4	7.3	6.6	5.4	5.3
Delay (nS)	30.0	50.0	80.0	100.0
Average	**7.3**	**6.7**	**5.3**	**5.4**
Stdev	**0.1**	**0.1**	**0.1**	**0.1**
Ptrn = (2,7)	Delay Line = 100nS			
Tap	**#1**	**#2**	**#3**	**#4**
Run #1	11.9	13.8		
Run #2	11.9	13.9		
Run #3	12.2	14.2		
Run #4	12.4	14.1		
Delay (nS)	30.0	50.0	80.0	100.0
Average	**12.1**	**14.0**	**####**	**####**
Stdev	**0.2**	**0.2**	**####**	**####**

Ptrn = FF		
Delay (nS)		Δ p.s
18	8.7	3.1
30	7.1	4.8
48	5.9	7.3
50	6.7	7.3
60	5.8	9.1
80	5.3	
100	5.4	

Ptrn = (2,7)	
Delay (nS)	
18	11.8
30	11.9
48	13.2
50	14.0
60	14.9
80	
100	

PHASE MARGIN PLOT Iteration: 4
11/30/89 15:28 ▪ 2.100 20 5.0 HST -10 6.3 14.8
Serial#: unknown

DELAY LINE = 60ns
PM. FILTER = 15MHz



Rad	Iw	HF	Patt	Xtrap	Apex	Zero	
2.100	20	5.0	HST	-10	1.5	11.6	TAP #1
2.100	20	5.0	HST	-10	1.4	11.8	
2.100	20	5.0	HST	-10	1.3	12.0	
2.100	20	5.0	HST	-10	1.5	11.9	
2.100	20	5.0	HST	-10	2.6	11.6	TAP #2
2.100	20	5.0	HST	-10	2.4	11.9	
2.100	20	5.0	HST	-10	2.6	11.7	
2.100	20	5.0	HST	-10	2.6	11.6	
2.100	20	5.0	HST	-10	4.8	13.1	TAP #3
2.100	20	5.0	HST	-10	4.8	13.1	
2.100	20	5.0	HST	-10	4.7	13.2	
2.100	20	5.0	HST	-10	4.6	13.3	
2.100	20	5.0	HST	-10	6.2	14.0	TAP #4
2.100	20	5.0	HST	-10	6.1	14.5	
2.100	20	5.0	HST	-10	6.0	15.2	
2.100	20	5.0	HST	-10	6.3	14.8	
2.100	20	5.0	HST	-10	6.2	14.8	

(C) PHASE LOCK LOOP DESIGN

DESIGN PARAMETERS

1. VCO Gain (Ko)

For MC1648 at VCO center frequency 128 MHz

$Ko = 16$ MHz / Volt

$= 2\pi * 16E6$ Rad / Sec / V

2. Phase Detector Gain (Kd)

For MC12040 Phase Detector

$Kd = 1/2\pi * A * (Voh - Vol)$ Volts / Rad

where A = Signal attenuation

$Voh = -1.8$ V

$Vol = -0.9$ V

PROGRAMMABLE GAIN CONTROL IS MOST SUITABLE FOR TEST EQUIPMENT.

3. Loop Gain (K)

$K = Ko * Kd / N$ / Sec

where N is frequency division ratio.

4. PLL Bandwidth (BW) & Damping Factor (ξ)

For linear continuous second order system

Bandwidth $BW = fo = 2 \xi f$

$= 2 \xi Wn / 2$

where

fo = Open loop unity gain cross over frequency.

fn = Close loop Natural frequency

ξ = Closed loop Damping Factor

Notes: 1. Normally high frequency operation is more critical and difficult to optimize. Optimize the system for high and verify at low frequency.

2. For Test equipment design low PLL jitter or noise is more important rather than quick response. Hence Damping Factor should be fairly large approx equal to 3.

3. Good approximation for BW = 50 KHz

5. PLL Transfer Function

$$G(S) = K * F(S) / S$$

where $F(S)$ = Transfer function of loop filter.

$1 / S$ = VCO act as integrator

Normally pole frequency should be much higher than BW or fo. Loop filter can be active or passive, but **IT IS BETTER TO HAVE SELECTABLE LOOP FILTERS.**

6. FREQUENCY CONTROL LOOP

Contribution of VCO jitter to PLL noise is more than any other components. A pretune DAC is used to tune the VCO to the required frequency with enough resolution for PLL to acquire lock easily. To reduce the VCO phase noise one or more frequency control loops can be placed around the VCO.

5. SAMPLE VS PHASE MARGIN TESTING

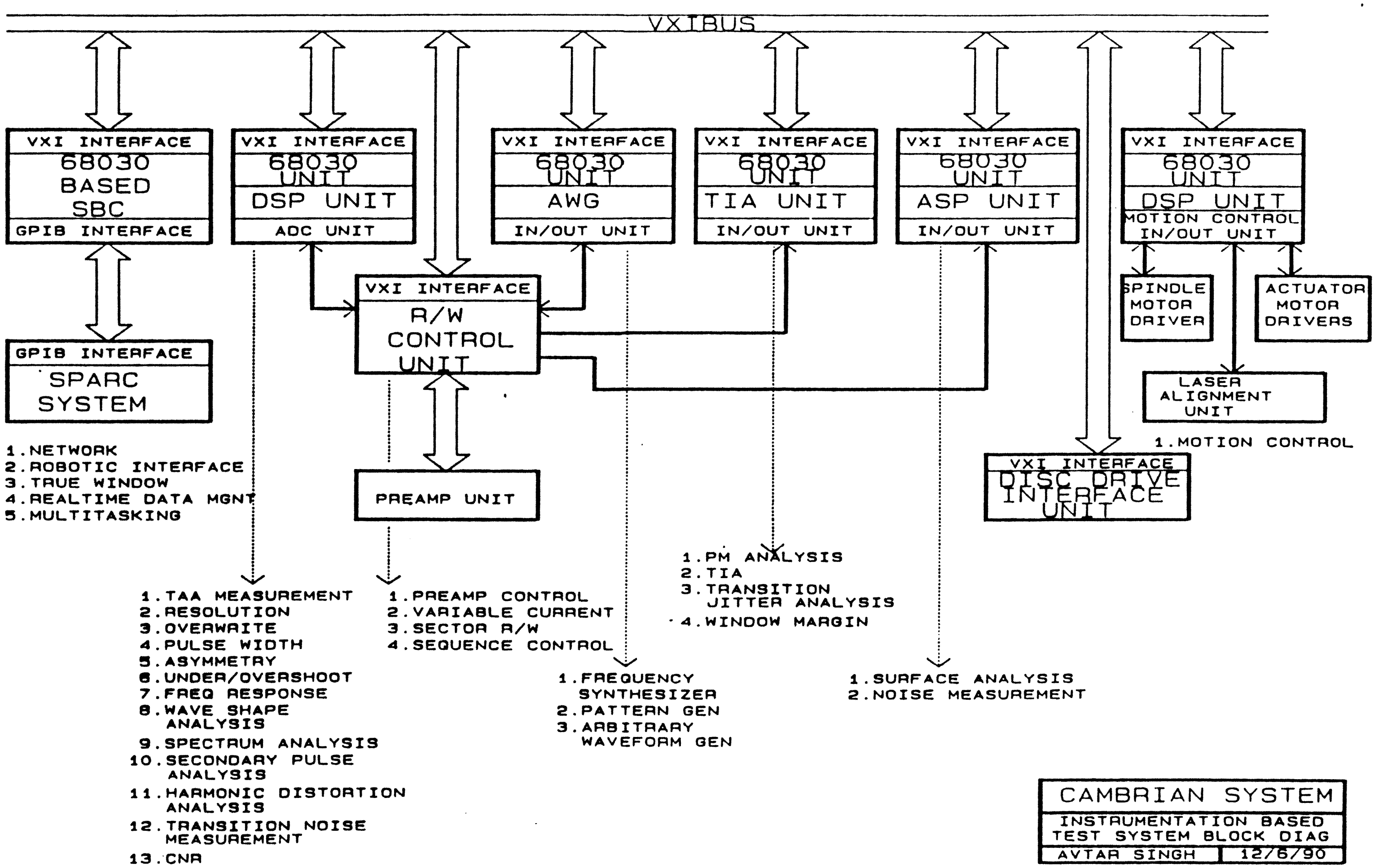
- Sample Margin Test Technique (SMTT) is logical extention to DSP technique.

- High speed ADC with DSP processor will supplement SMTT.

- SMTT with DSP can produce
  - Bar Graph
  - Gaussian curve

- SMTT more suitable for higher frequency and easier to implement.

INSTRUMENTATION BASED TEST SYSTEM



ELECTRONIC FUNCTION INTEGRATION

Steve Dines

Cirrus Logic

CIRRUS LOGIC

AGENDA

- Integration environment
- Why does DSP impact integration
- Packaging & Test issues
- Integration Scenarios

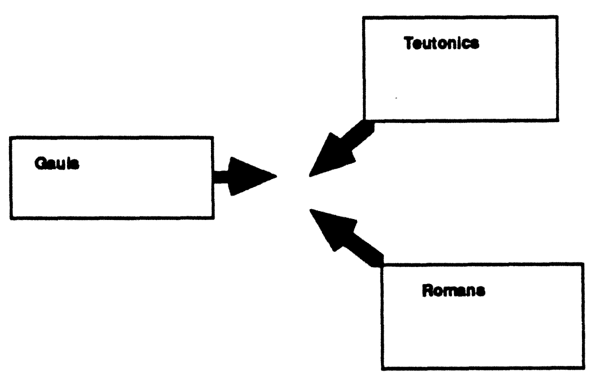
CIRRUS LOGIC

INTEGRATION ENVIRONMENT

- *Everybody* claims to be able to integrate *everything*

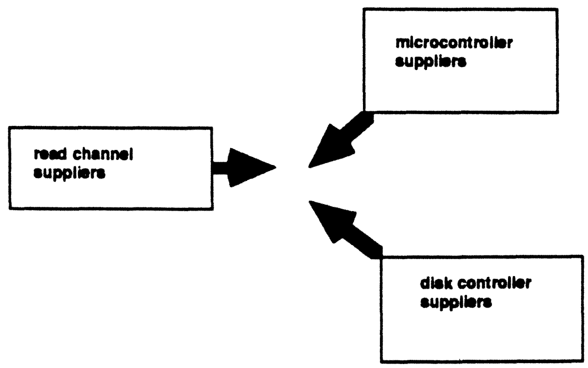
CIRRUS LOGIC

EUROPE 100 B.C.



CIRRUS LOGIC

DISK ELECTRONICS SUPPLIERS TODAY



- Buyer beware!

WHY DOES DSP IMPACT INTEGRATION?

- Channel
- Servo
- Flexibility
- Power management
- Pin-out

SYNCHRONOUS CHANNELS AND INTEGRATION

- highly tuned analog --> analog front end + digital algorithms => CMOS
- Force to CMOS paves the way for integration with other logic elements
- Scalability of digital vs analog
- Flexibility gains ensure customer value added

Bipolar
to
CMOS 50%
to
100%
reduction
of
power

DSP to

CIRRUS LOGIC

SYNCHRONOUS CHANNEL INTEGRATION BENEFITS

- Space reduction
- Power deduction
- Pin-out reduction

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DIGITAL SERVO AND INTEGRATION

- Servo becomes logic element plus analog periphery (A to D and D to A)
- Easier to integrate

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DIGITAL SERVO INTEGRATION BENEFITS

- Integrated servo is an areal capacity argument

  Integrated header - avoid repeating track
  info in data fields and servo fields
  5% benefit (linear only)

- Eases pseudo-sector mark generation
- More integrated power management
- Servo is becoming more hardware path - fits better with data channel
- Totally concurrent servo processing
  - no interdependence between micro and servo engine
- Preserves commodity micro benefits
- Removes major complexity from ASIC

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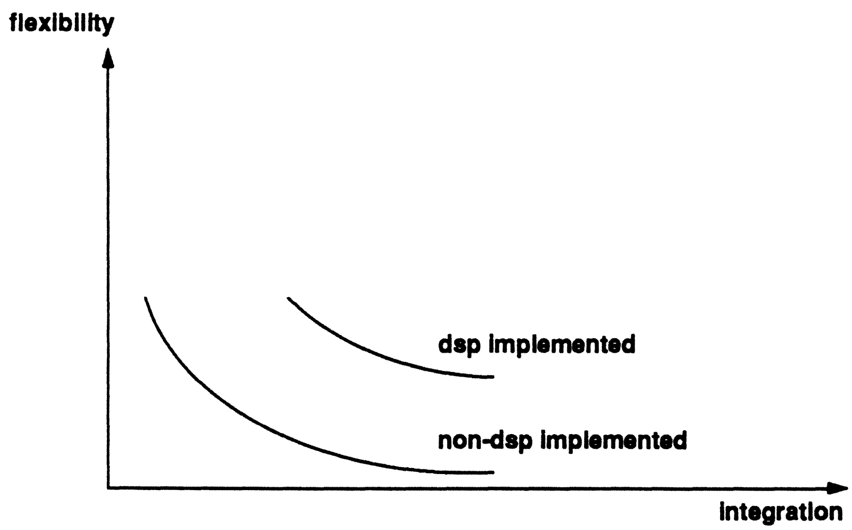
OPTIMIZED SERVO PROCESSING

- Servo engine targeted at magnetic disk head control
- Key hardware modules added
- Reduces code
  - space
  - time
  - engineering effort
- Overkill avoidance - eg sub 100ns multiplies not needed for typical sample rates

FLEXIBILITY

- How do electronics suppliers ensure customer flexibility in the face of ever increasing integration
- Synchronous channels provide digital flexibility
- Digitally based servo allows user to implement his servo approach

DSP IMPROVES FLEXIBILITY



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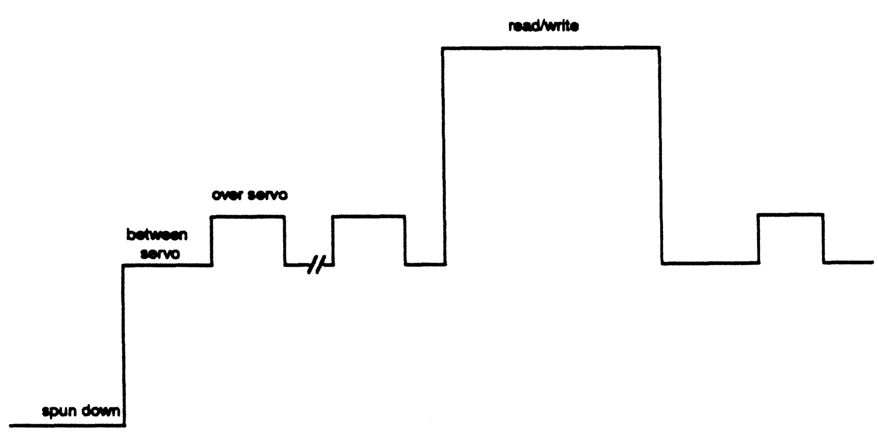
DSP IMPROVES POWER MANAGEMENT



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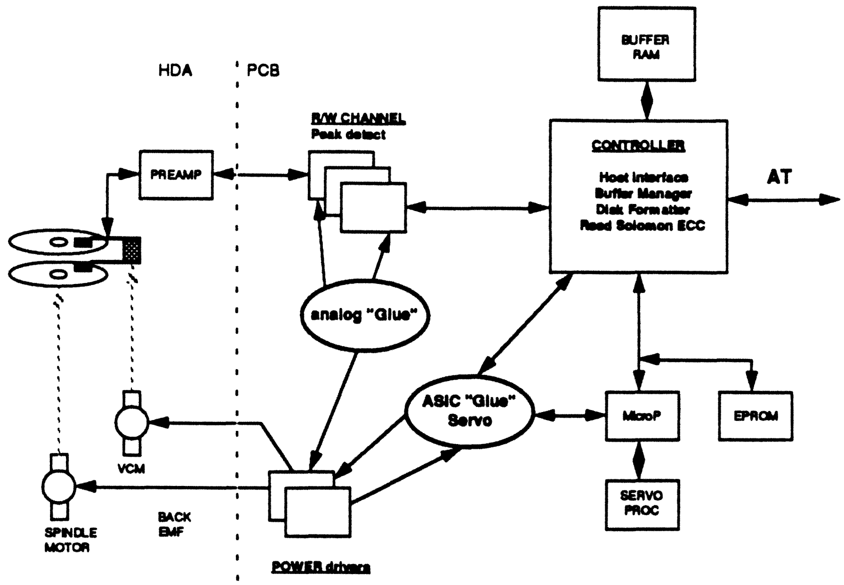
TODAY'S DISK DRIVE SUBSYSTEM



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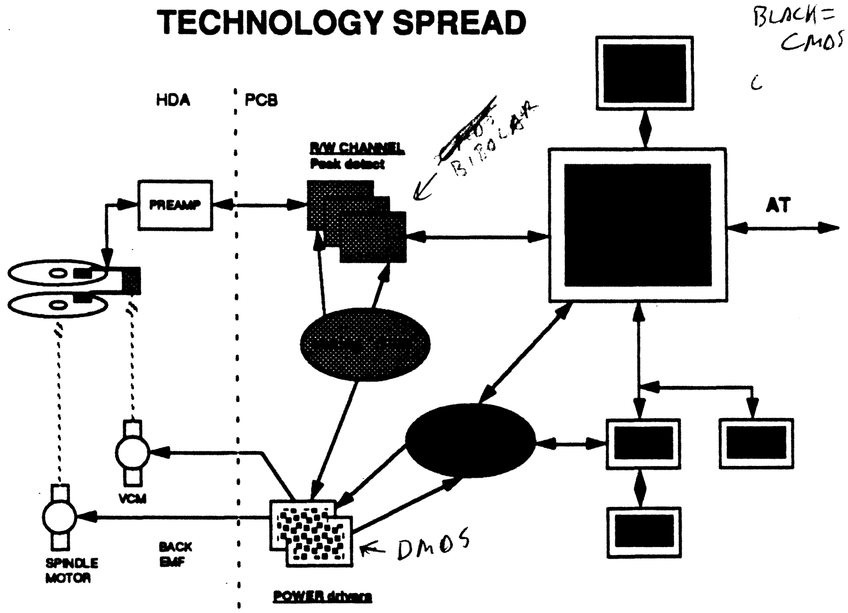
BST SD 12/16/91 15/

TECHNOLOGY SPREAD

BLACK = CMOS

C



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BST SD 12/16/91 16/

PACKAGING & TEST ISSUES

- Integration should match packaging
- Relationship to form factor
- Die considerations

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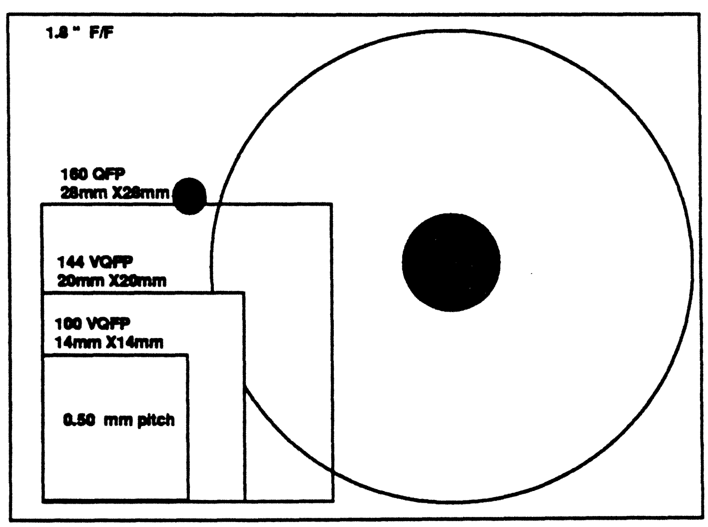
1.8 " AND QFP



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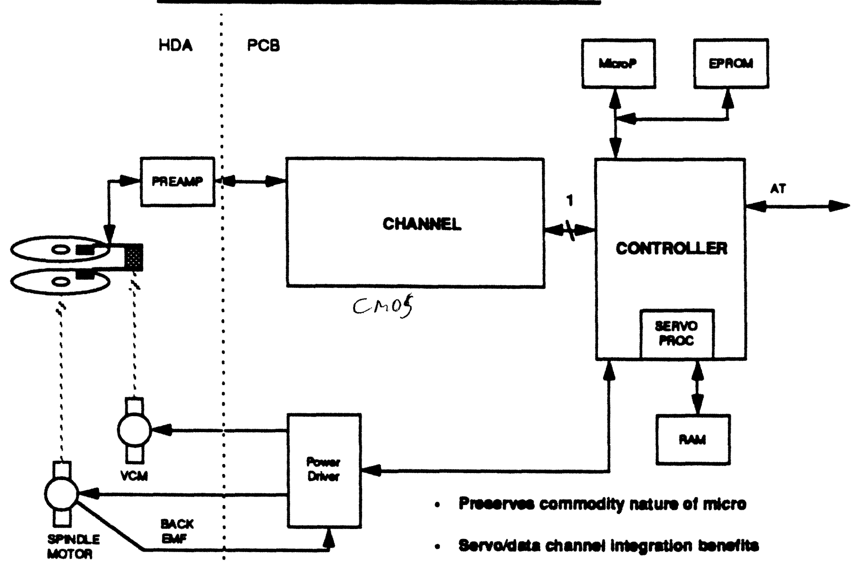
INTEGRATION SCENARIO #1



- Preserves commodity nature of micro
- Servo/data channel integration benefits
- CMOS or BiCMOS channel ?

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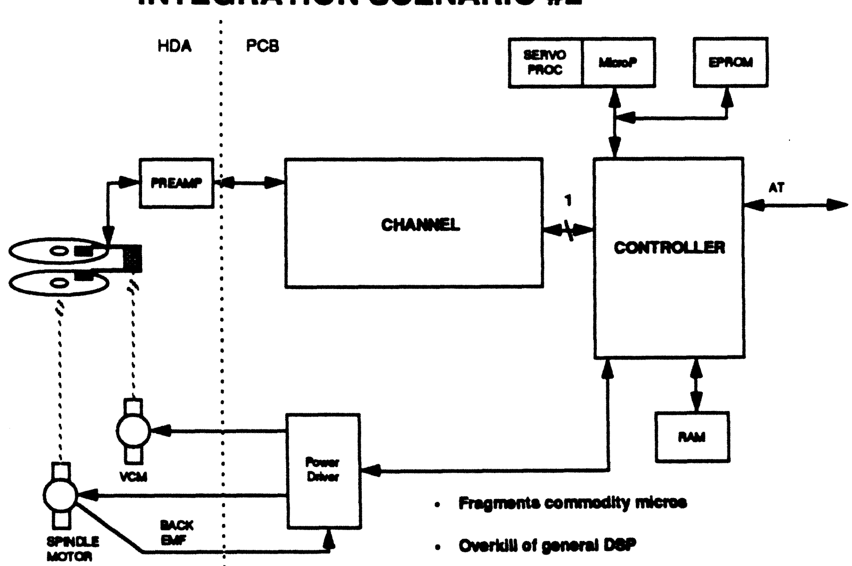
MST SD 12/16/91 19/

INTEGRATION SCENARIO #2



- Fragments commodity micros
- Overkill of general DSP

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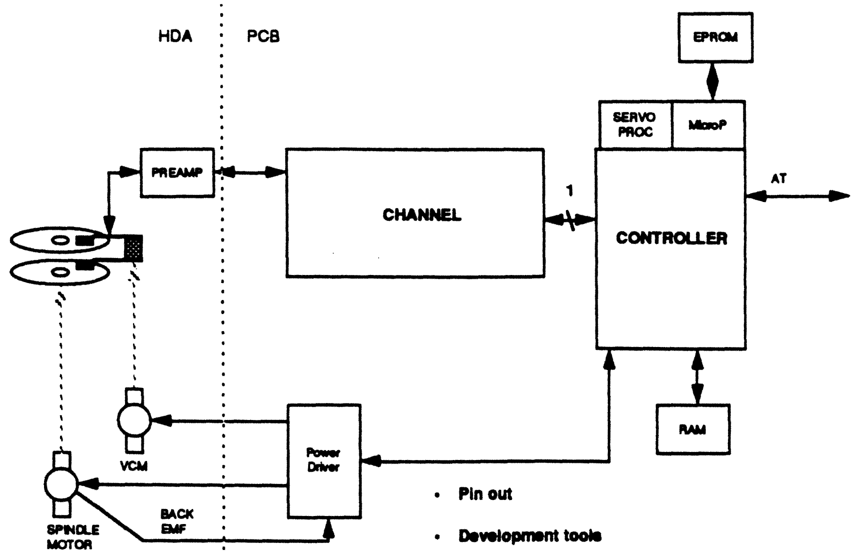
MST SD 12/16/91 20/

INTEGRATION SCENARIO #3



- Pin out
- Development tools
- fragmented product line

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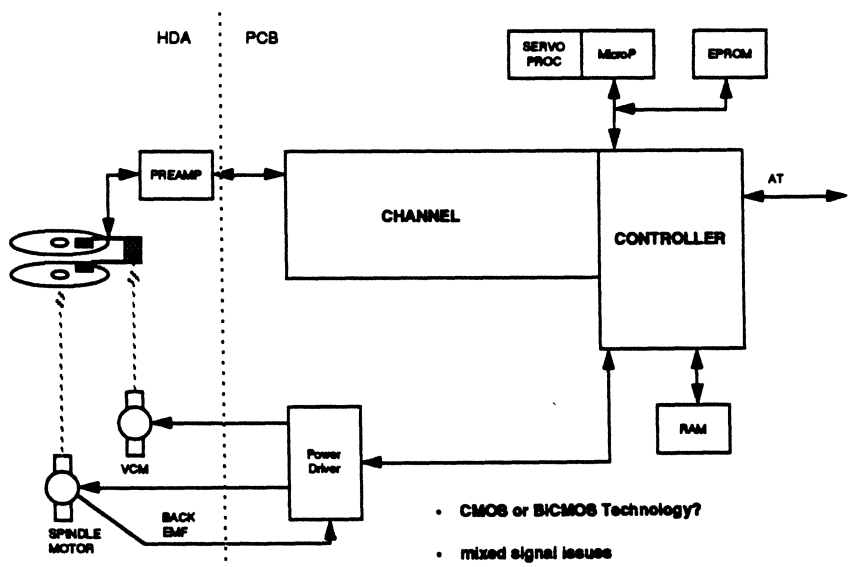
INTEGRATION SCENARIO #4



- CMOS or BiCMOS Technology?
- mixed signal issues

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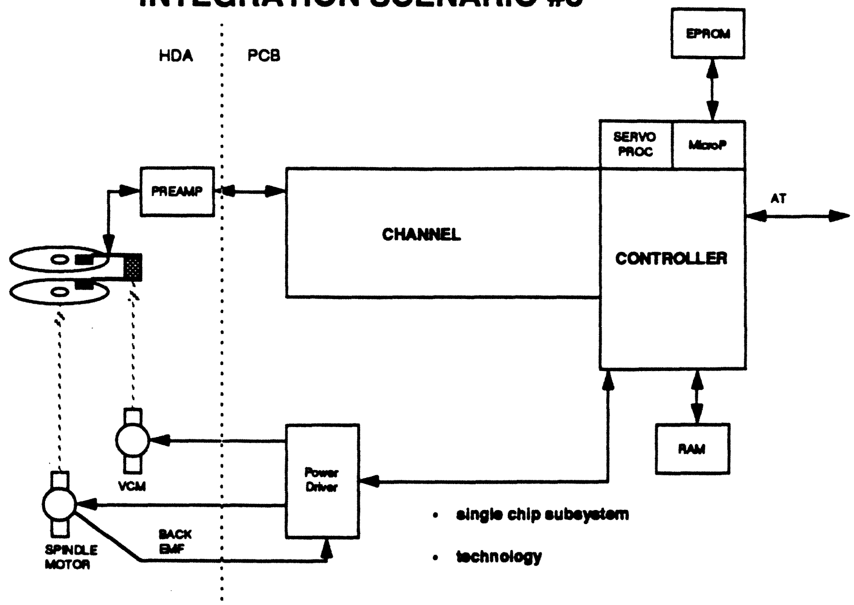
INTEGRATION SCENARIO #5



- single chip subsystem
- technology

SUMMARY

- Buyer must beware
- Most cost efficient vehicle for transistor delivery
- Understand your commodity benefits
- Exploit the digital drive!

DRIVE SELF TESTING AND DIAGNOSTICS

Jonathan D. Coker

For IIST's "The Impact of DSP on Future Generation HDDs"
December 17-19, 1991

IBM Storage Systems Products Division, Rochester, MN

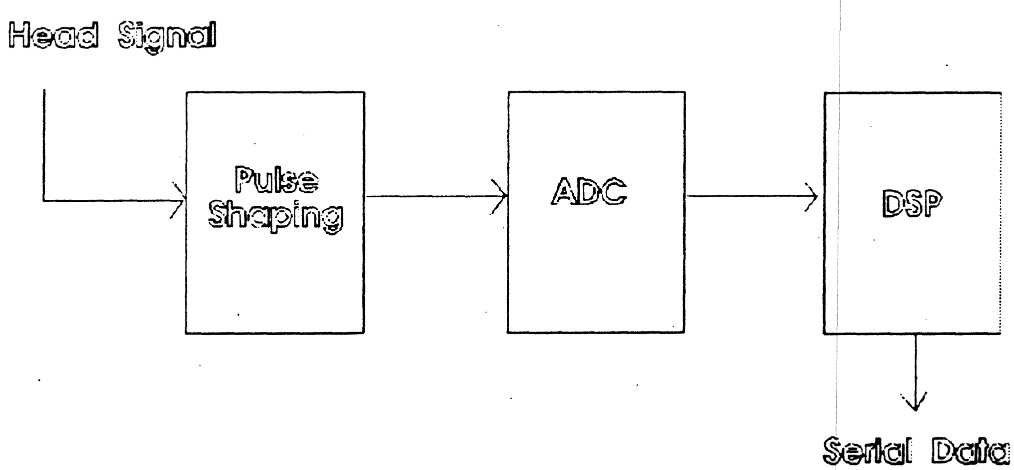
Redwing 5.25" DSP Drive

3.50" DSP Drive - JUST ANNOUNCED

Overview

- PRML channel primer
- Error rate performance estimation
- Flying height change detection
- Disk surface analysis

Signal Flow in a PRML Channel



Partial Response IV Conventions

$$y_k \equiv a_k - a_{k-2}$$ - output rule

$$a_k \in \{\pm 1\}$$ - input rule

$$\Rightarrow \quad y_k \in \{0, \pm 2\}$$

Partial Response IV Tidbits

- Interleaves are independent
- Output "2"s must alternate polarity within an interleave

Output Sequence Examples

NOT LEGAL

-2 -2 0 0 2 2 0 0 $\boxed{-1}$ 0 2

-2 2 0 -2 0 0 2 0 -2 2 0 0 2

-2 2 0 -2 0 0 $\boxed{2}$ 0 $\boxed{2}$ -2 0 0 2

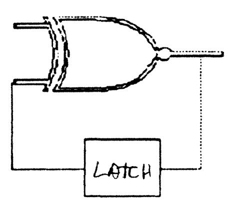
NOT LEGAL

Precoding

Peak Detection:

Input

... 01001000101 ...



Output

... 10001111001 ...

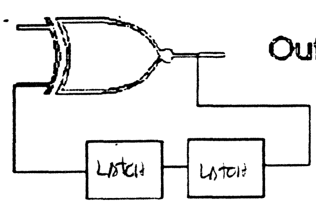
OR

...01110000110...

Partial Response IV:

Input

... 01001000101 ...

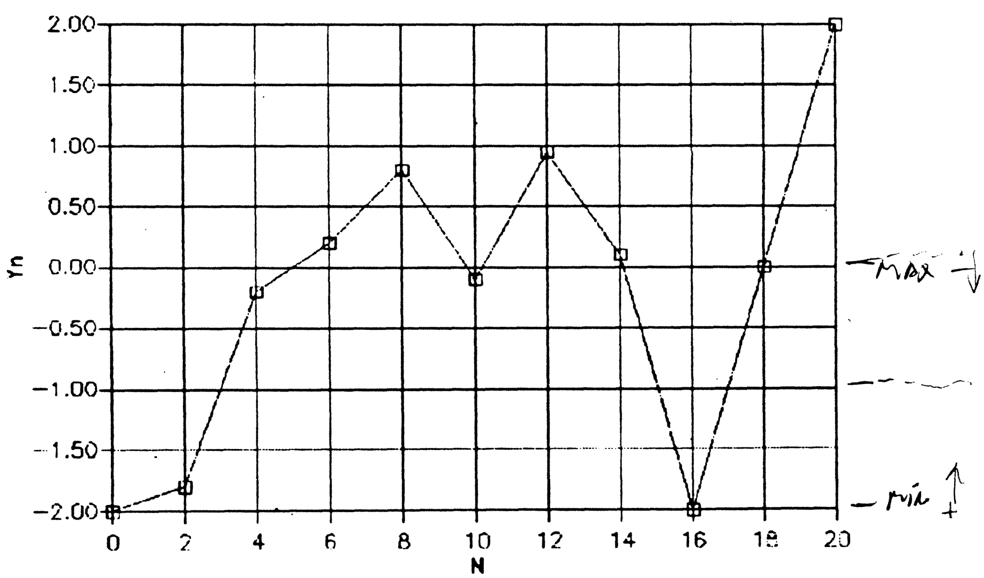


Output

... 01011111011 ...

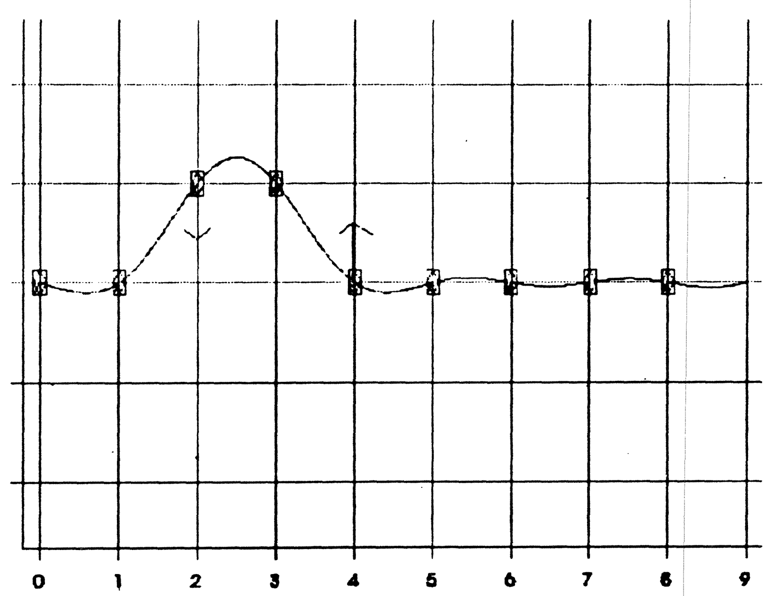
Precoding guarantees a non-zero output if~~f~~ the input is 1.

Noisy Readback Sequence



With PR-IV, Viterbi detection consists of a minimum/maximum finder with a polarity latch.

PRML Error - Example 1

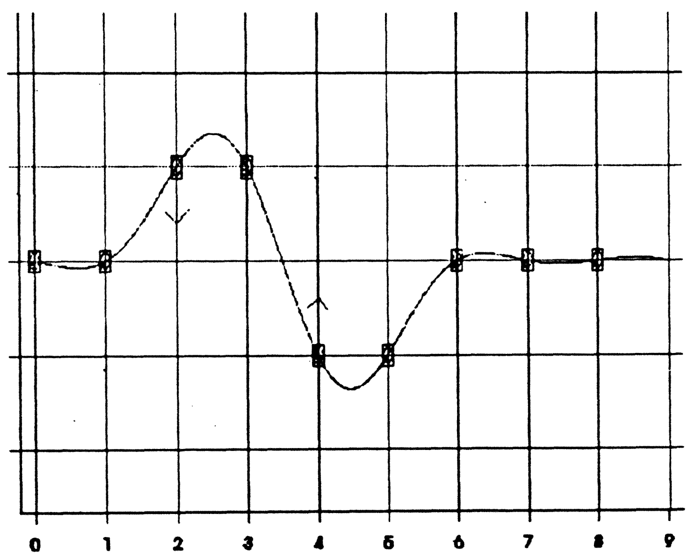


0 0 +1 +1 -1 -1 -1

Condition for error: EX 1

$n1 + n2 > 2$

PRML Error - Example 2



Condition for error: EX2

$$n1 + n2 > 2$$

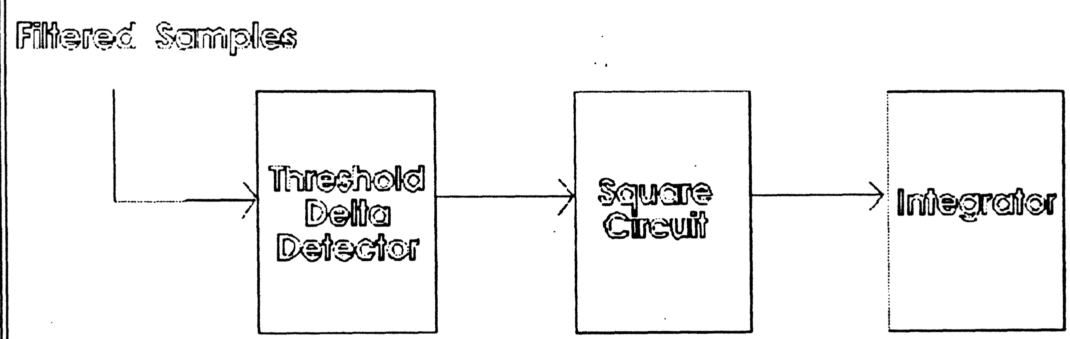
Error Rate Performance Estimation

- Error rate performance may be estimated by measurement of noise statistics in fraction of time necessary for a true error rate test
- Simplest case assumption of white Gaussian noise allows compact implementation

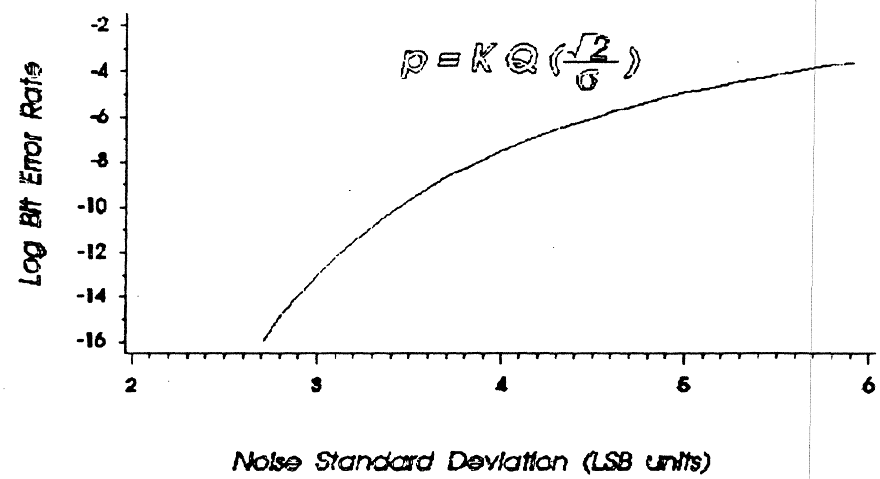
Possible Uses

- *quick performance indicators during the manufacture of the drive*
- *early detection of error rate changes in the field*
- *field diagnostics*

Mean-Square-Error Circuit



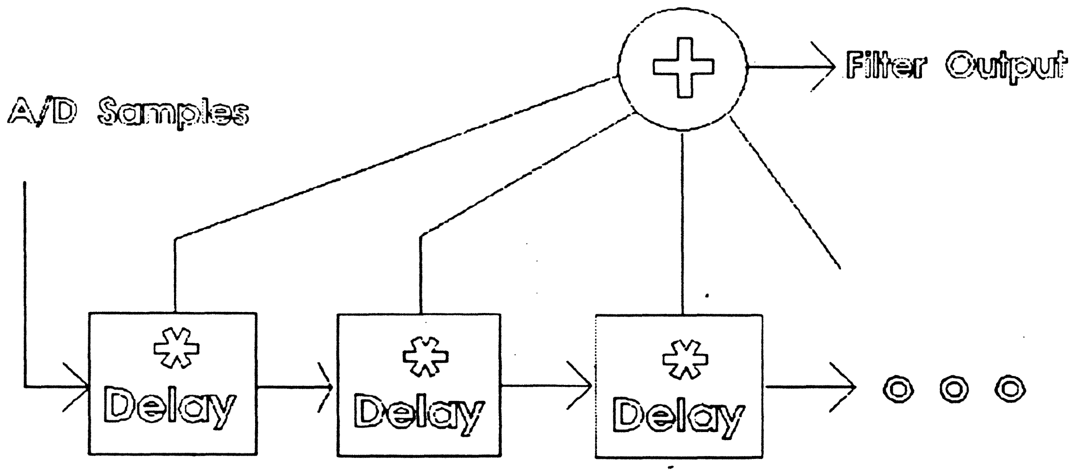
Error Probability with WGN



WGN is typically a bad presumption.

Equalization typically introduces significant noise correlation effects.

Correlation Effects in a Digital Tap Delay Line



PRML "cares" about the following quantities:

$$Y(n) - Y(n+2)$$
$$Y(n) - Y(n+4)$$
$$Y(n) - Y(n+6)$$

o o o

Noise Multipliers

These quantities are zero-mean
Gaussian variables whose standard deviations
are related to the input by the following factors:

$$M^2(n) = \left(\sum t^2(i) - \sum t(i)t(i+n) \right)$$

Noise multipliers are functions of time spacing.

Noise Multipliers - Example

$$\sum t^2(i) = 1.2^2$$

M(2) = 1.3

M(4) = 1.5

M(6) = 1.3

M(8) = 1.2

M(10) = 1.2

...

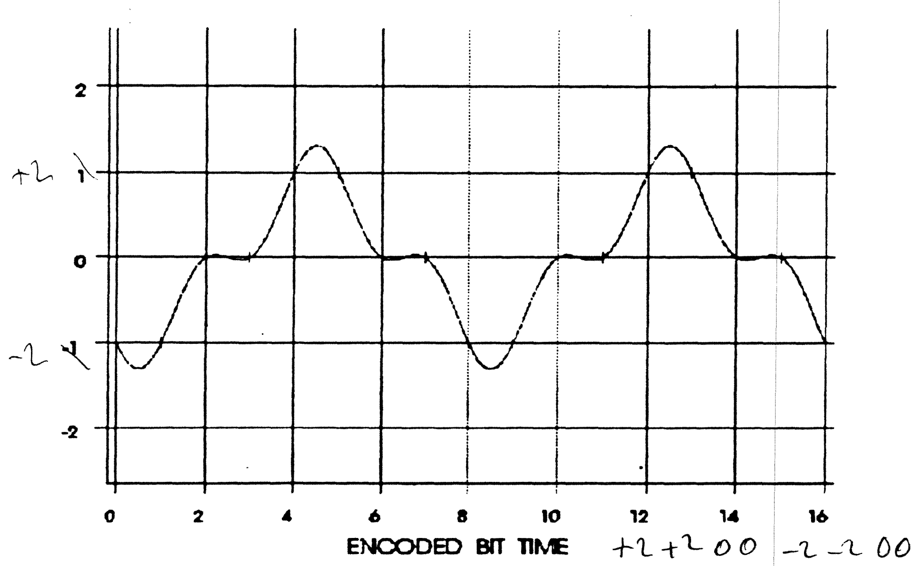
When noise correlation is significant, the overall error rate can be dominated by a single most-likely error length.

Flying Height Change Measurement

- Technique uses frequency response changes to detect flying height differences

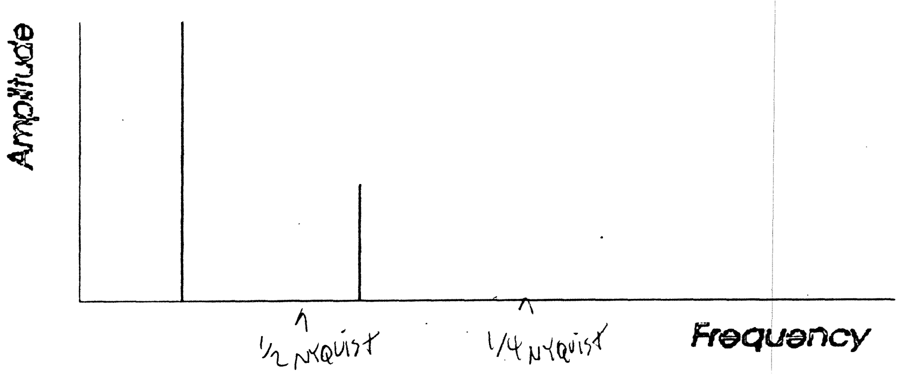
- Frequency response changes described by the Wallace equation

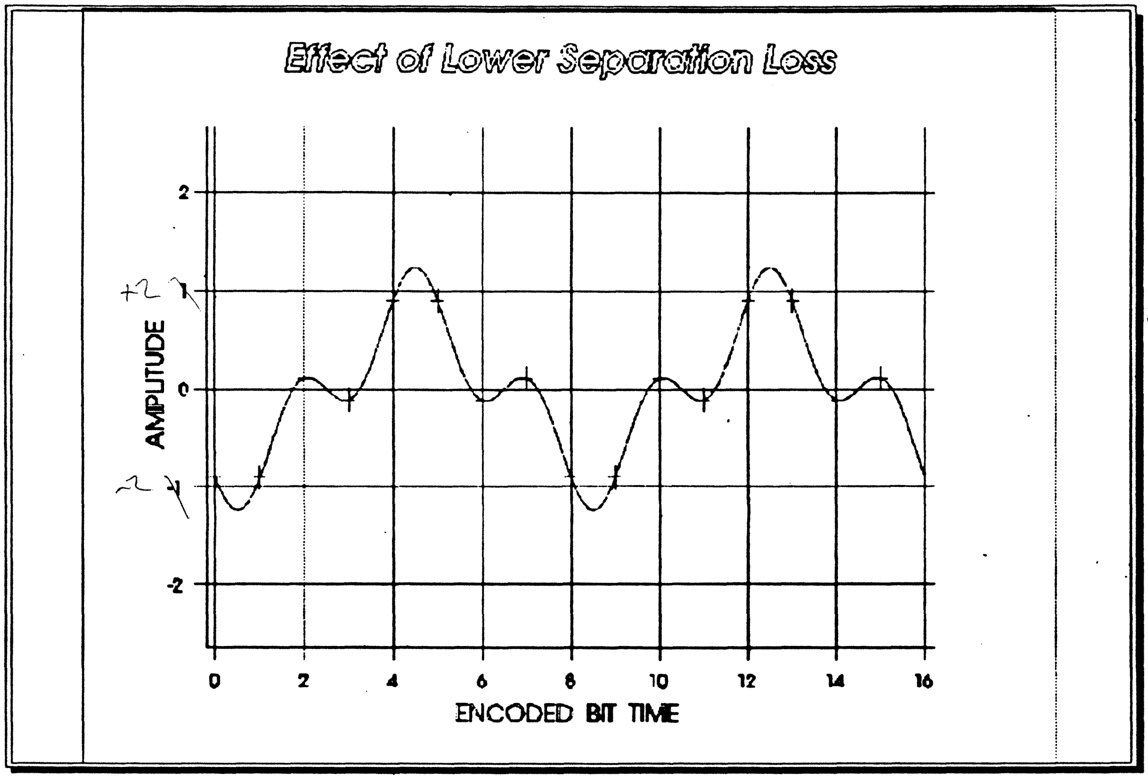
Test Pattern

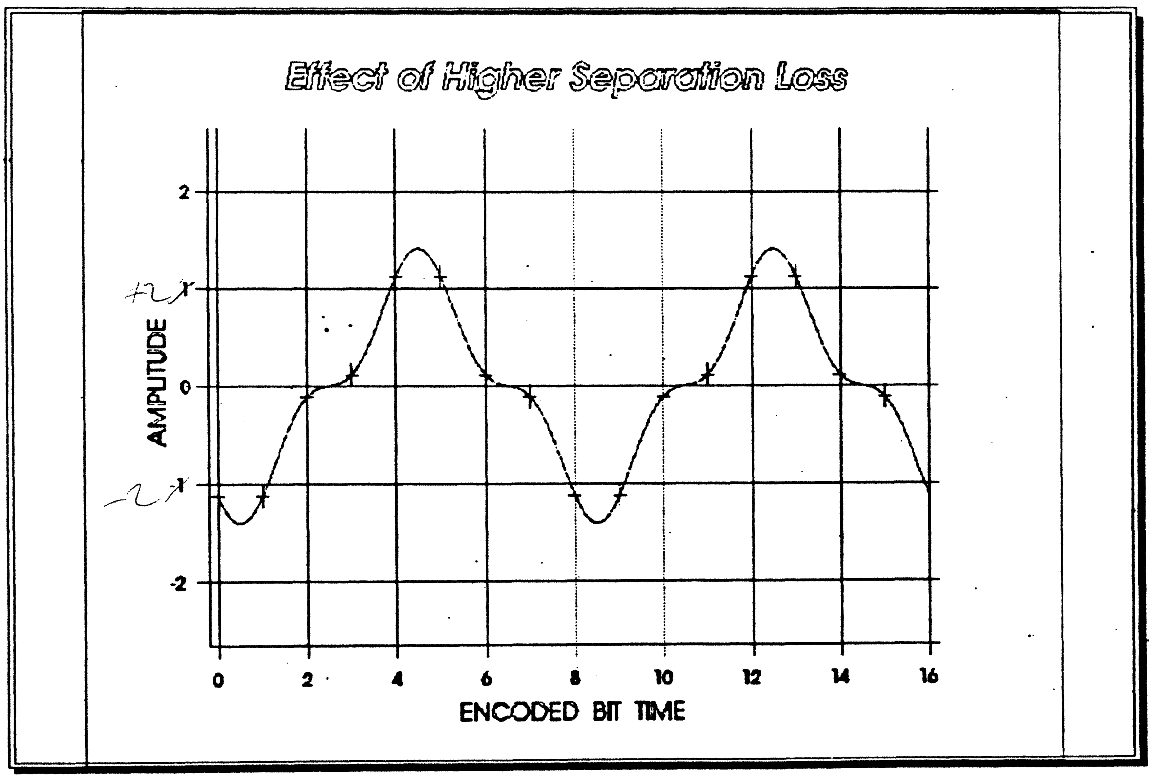


Description of Test Pattern

$$f(t) = (1 + \sqrt{2}) \cos\left(\frac{\pi}{4} t\right) + \cos\left(\frac{3\pi}{4} t\right)$$




Effect of Lower Separation Loss
2
+2
1
0
-1
-2
AMPLITUDE
0
2
4
6
8
10
12
14
16
ENCODED BIT TIME


Effect of Higher Separation Loss
2
+2
1
0
-1
-2
AMPLITUDE
0
2
4
6
8
10
12
14
16
ENCODED BIT TIME

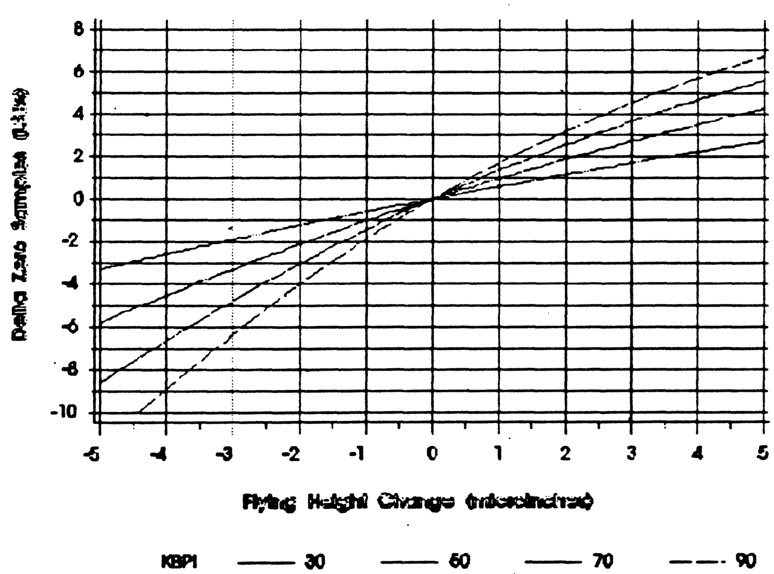
Wallace Equation Application

$$f(t) = (1+\sqrt{2})\, e^{-k\frac{\pi}{4}} \cos\left(\frac{\pi}{4} t\right) + e^{-3k\frac{\pi}{4}} \cos\left(\frac{3\pi}{4} t\right)$$

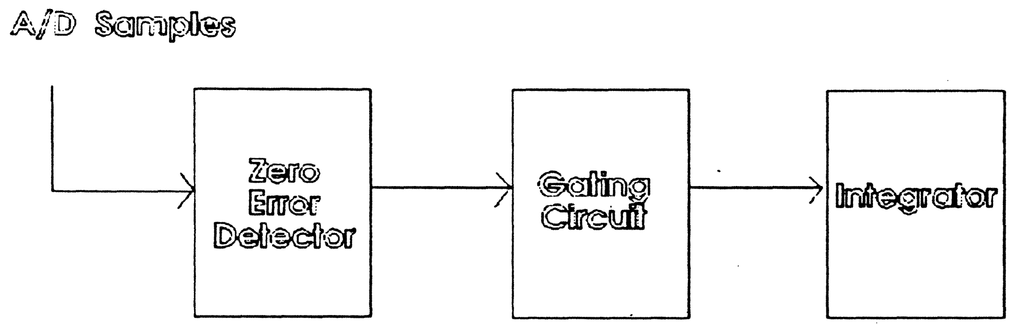
$$f(-0.5) + f(0.5) = 4$$

$$\Longrightarrow \delta(k) = \frac{2\left(1 - e^{-k\frac{\pi}{2}}\right)}{\cot\left(\frac{\pi}{8}\right) + \tan\left(\frac{\pi}{8}\right) e^{-k\frac{\pi}{2}}}$$

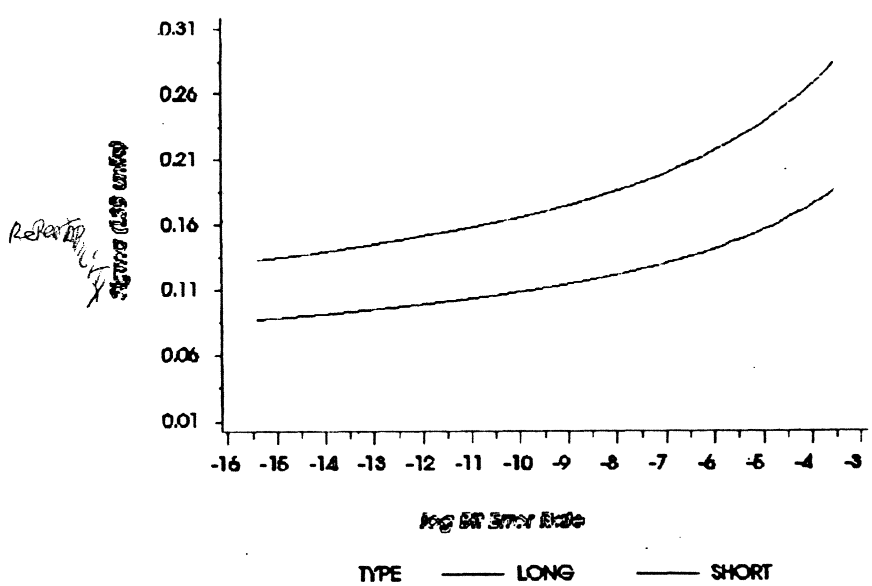
Delta versus Separation for Various Linear Densities



Fly Height Change Detector Circuit



Measurement Error Analysis



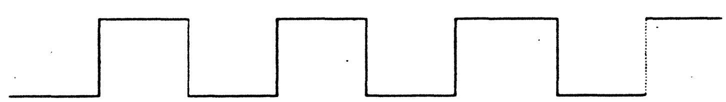
Disk Surface Analysis

==> Purpose: to mark and deallocate magnetic imperfections on the disk surface

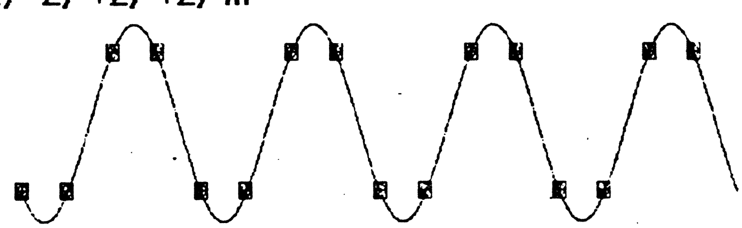
==> typically performed during the manufacture of the drive

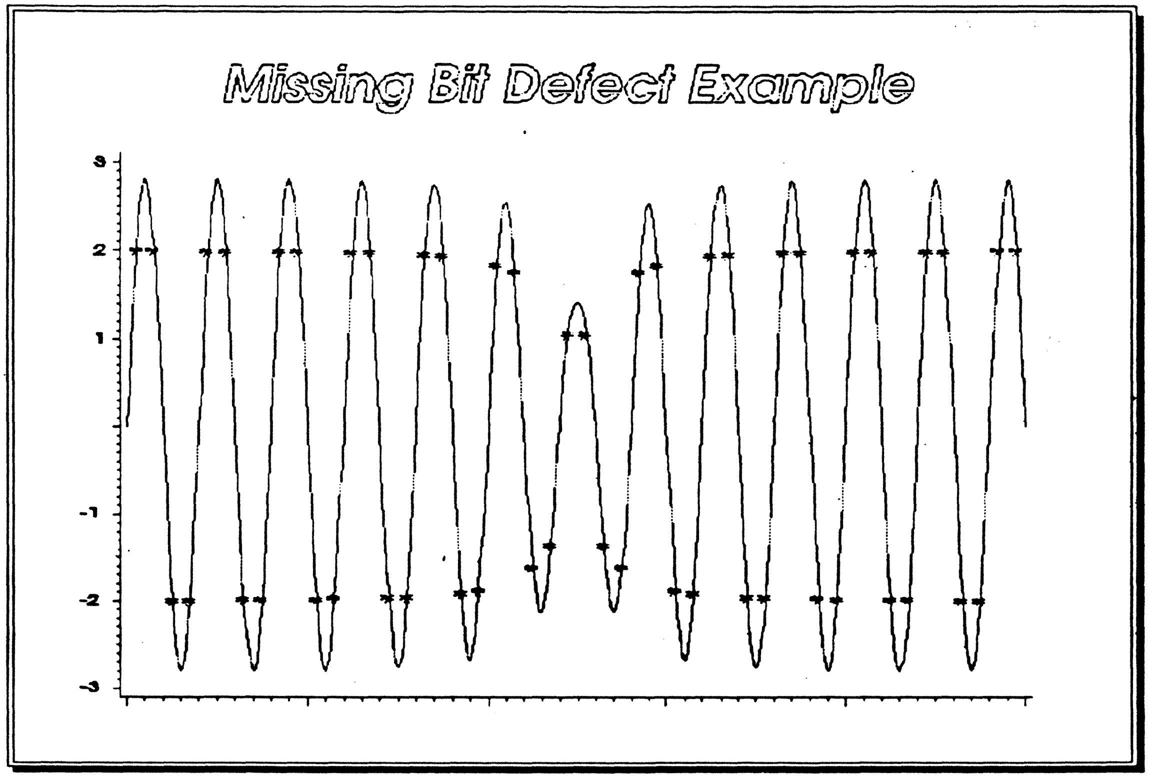
Surface Analysis Test Pattern

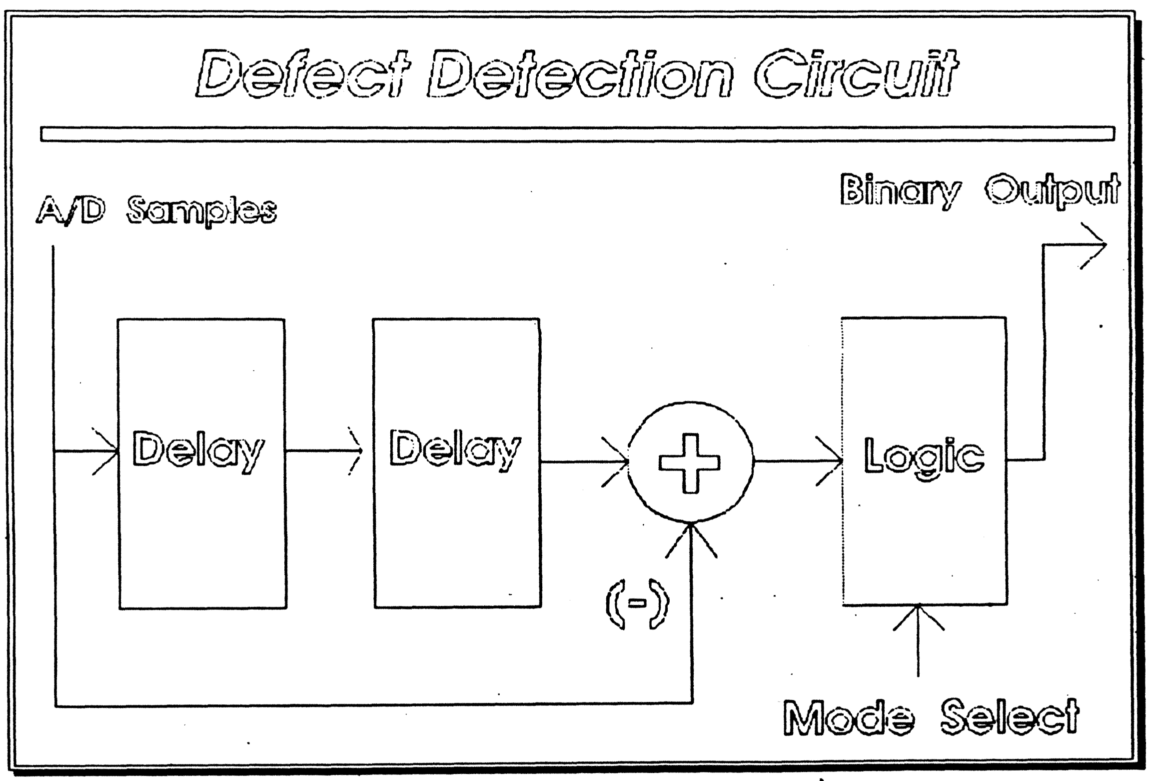
a_k : -1, -1, +1, +1, ...

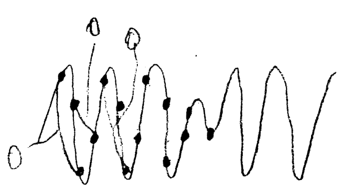


y_k : -2, -2, +2, +2, ...

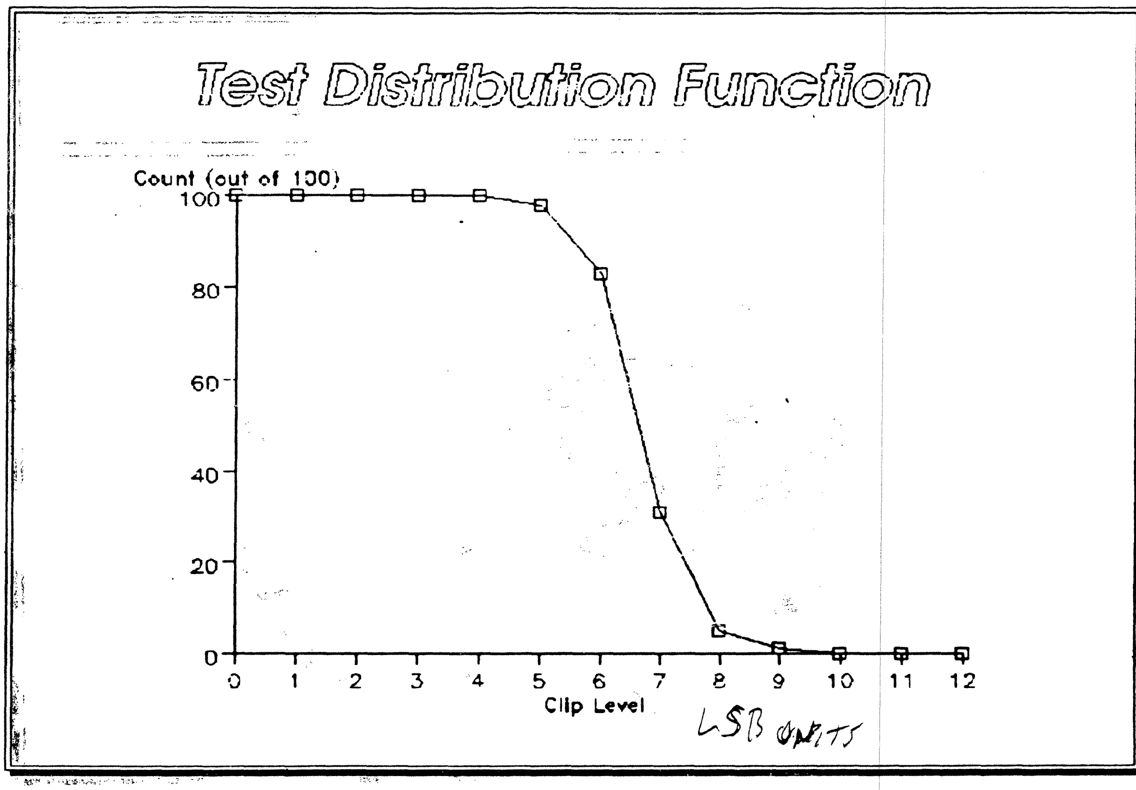


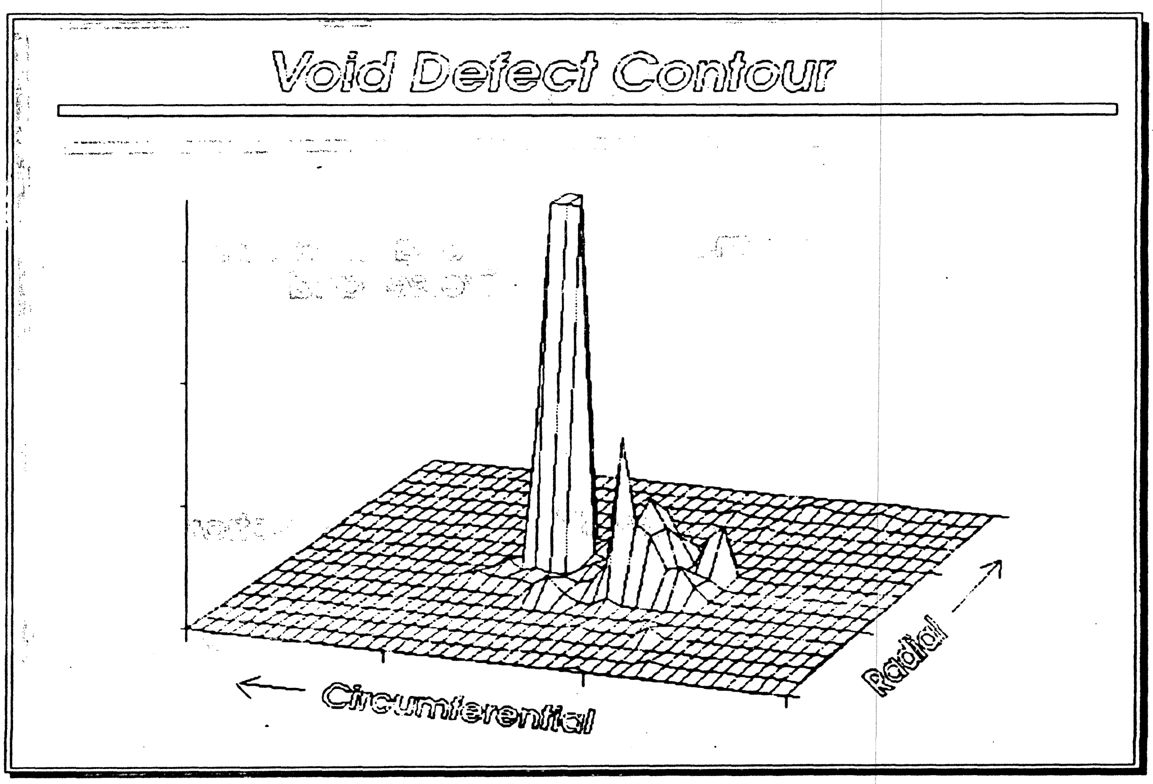




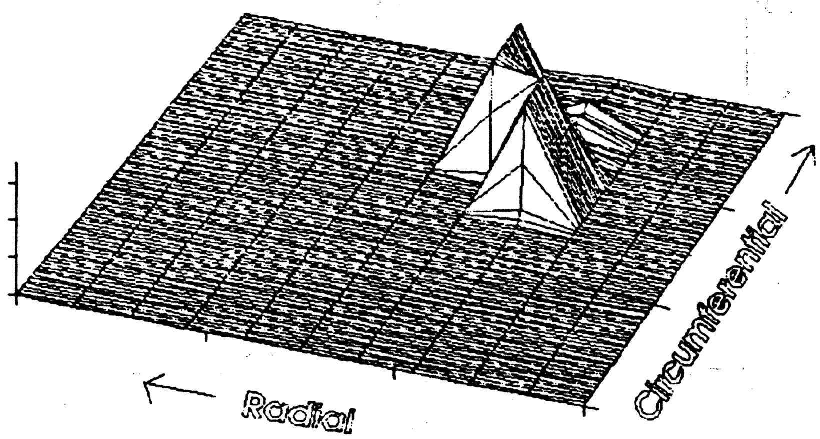


WILL REPORT A LONG ERROR
AS ~~AND~~ SHORT ERRORS
SEPARATED BY SPACE EQUAL
TO ERROR LENGTH.


Test Distribution Function
Count (out of 100)
100
80
60
40
20
0
0 1 2 3 4 5 6 7 8 9 10 11 12
Clip Level
LSB UNITS


Void Defect Contour
Circumferential
Radial

Scratch Defect Contour



Summary

Incremental modifications to a standard PRML channel provide diverse and powerful applications:

- Disk surface analysis
- Flying height change detection
- Error rate performance estimation