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COMPUTER MEMORIES
A Survey of the State of the Art

by

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ABSTRACT

Computer memory developments of the last decade, the present state, and efforts for improvements are surveyed. The following topics are included. Principles of storage and selection of random access memories. Principle and engineering considerations of current-coincident driven core memories. Magnetic decoding and load sharing switches. Word organized one-core and two-core per bit memories. Fast and impulse switching. Transfluxor memories. Non-destructive read-out memories. Ferrite apertured plates. Twistors. Fixed read-only memories. Thin magnetic film memories: dots, sheets, coated wires and rods. Present operational memories typically with capacities of 10^5 to 10^6 bits and read-write cycles of 2 to 15 μsec. Likelihood of order of 100 ns read-write cycle times attainable with ferrite and thin film memories. Consideration relating to large capacities. Ferroelectric memory attempts. Cryoelectric superconductive memories: principle, superconductive films, Crowe cells, continuous sheets, systems, and the outlook for large capacities. Tunnel diode memories which promise a read-write cycle of the order of 10 ns. Outlook for content addressable memories.

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I. INTRODUCTION

Computing, or more generally, processing of information, consists of causing some parts of it to interact with others in order to produce new information and, in general, of compounding such steps by causing interactions between parts of the new information. Since these steps are successive and in general all input information is not available simultaneously, provisions must be made for storing information. The basic idea of modern digital computers consists of extending the necessary storing of the information to be processed to storing also the program describing the process to be performed. It is not surprising therefore that the art of storing information is central to the whole art of digital computers.

In general the storing and processing functions are separate. There is a central memory to which and from which all data is routed and a processor which receives from the memory data to be processed and the description of the prescribed process and which delivers back to the memory the resulting new information.

The routing to and from the memory can be obtained, in principle, by the sequential flow of data and programming information provided this information is properly preordered. Such serial access has been investigated extensively because it matches well the physical motion of tapes or drums, the natural propagation of disturbances in delay lines, the flow of signals from a continuously scanned electrostatic storage tube, etc. It has been

found that the required preordering of information is often more onerous than the execution of the desired processing. But more detrimental yet is the fact that the necessity of advance ordering prevents (or at least greatly restricts) the use of a key programming tool, namely the possibility of conditional addressing. This is the possibility of making the choice of data to be taken at any time to be dependent on the results of the process in progress. Clearly, what is needed is free access to any information at any time, independent of previous accesses. Selectively addressably electronic memories, or "random" access memories, so called to emphasize the freedom of accessability, have been conceived for this purpose and mark the real advent of modern high speed computers.

A random access memory is a store of information words or groups having a fixed number of bits which are codes for numbers, characters, orders, etc. Each m-bit word is associated with an identifying label, or address, which itself consists of a fixed number n, of bits. To insert information into the store, i.e., to write or "read-in" into it, the m bits identifying the word, the n bits identifying the address and a signal commanding write-in are given. This causes the particular m-bit word to be stored. To read-out any word, its n-bit address and a signal commanding read-out are given. This causes an m-bit output from the memory corresponding to the selected stored word.

The storage capacity of the memory is $m2^n$ bits or 2^n words of m-bits, if all possible n-bit addresses are permissible, as is commonly the case. The time required for access is in general different for read-out and write-in. The operation of most present day memories requires that both steps be taken for every access so that the significant time is the cycle time required to both read-out and write-in at a certain address and leave the memory available for the next access. Unless otherwise stated we shall call this the access time.

This paper surveys random access memories with a capacity in the range of one hundred to millions of words of one to hundreds of bits each with an access time ranging from a fraction of a microsecond to tens of microseconds. This is the range of present, and presently sought for, high speed electronic memories. The paper does not include memories with a capacity of one or a few words which are usually called registers and which should be grouped with logic circuitry with which they are usually intimately associated. Nor does it include the important class of electromechanical memories such as discs, drums or fast-stop-go tapes, with which a degree of random access and large capacities have been achieved but which have relatively long access times ranging from a few tenths of a second to tens of minutes.

II. General Considerations

A few general considerations on possible methods of making random access memories may be useful, to put into perspective

present solutions and the search for better ones. For every bit, there must be a discrete physival storage cell capable of being set into one of the two distinct states. The cell must remain in the set state indefinitely, or until it is changed to the other state. The selection of a particular cell, for establishing or ascertaining its state, must be determined uniquely by the presence of the n signals defining its address. There are thus two basic aspects to memory: storage and selection.

1. Storage

The two distinct states of the storage cell can be natural states which require no external energy to be maintained. This is the case for ferromagnetic, ferroelectric, and superconductive cells all of which have a hysteretic characteristic, i.e., the following property. The quantity defining the state (magnetic induction, electric polarization, or induced supercurrent) has remanent states corresponding to no energization. The sign of this quantity can be changed by an excursion of the energizing force (magnetizing force, electric field, or primary inducing current) from zero to a sufficiently positive or negative value at which it remains for a sufficiently long time and then back to zero. The required absolute value of the excursion and its timing depend on the amount of stored energy (magnetic, electric, or magnetic respectively) and the details of the mechanism of energy loss during the transitions. In all three cases the amount of required energy is controllable by existing

electronic elements, and the time can be in the microsecond range. These possibilities, and the fact that the non-linear response to energization facilities the selection of the element, as will be explained, have made the ferromagnetic, ferroelectric and superconductive elements prime contenders for storage cells of random access memories.

Storage elements requiring external energization to maintain the stored state have been the basis of important developments and some types are running contenders, particularly for ultra high speed memories. The external energization can be used to create artificially two stable states. For example, an electrically floating target subjected to constant electron bombardment will assume one of two stable potentials under conditions insuring the proper secondary emission mechanism. This has been exploited in the selective electrostatic storage tube with matrix grid selection as well as in deflected beam barrier grid tubes. In a more recent proposal, tunnel diodes are maintained by a dc source at one of two stable potentials existing by virture of the negative resistance of the device. In the above examples the stable states are static and maintained by dc power. Dynamically stable elements maintained by ac power are possible also, as for example parametrically excited oscillators which can be made to oscillate in one of two opposite phases at a frequency one half that of the energizing source. External energization can be used also to hold information in elements which have no stable states, such as condensers. Two distinct ranges of stored energy can be

maintained, despite unavoidable energy losses, through the artifice of periodic rechanging of every element in the memory. This is the principle of the diode condenser memory[7,8] and Williams'[9] storage tube.

2. Selection

The selection of one out of 2^n words (typically 256 to 16,384) according to its n bit coded address (n = 8 to 14) is a decoding function basic to random access memories and has been one of its main problems. In the mid-forties when the first high speed memories were being actively developed electronics was still chiefly vacuum tube electronics. A natural solution to the problem was the use of an electron beam which could be deflected to select electrostatic storage elements on a target in the manner so successfully employed in television pick-up tubes. The required amplitude of deflection is obtained through digital-to-analog conversions,[3,9] a process which turns out to be a difficult circuit task. Purely digital selection through the use of an array of beams switched by combinatorially connected control electrodes, avoids the conversion difficulty but leads to rather complex tube structures.[1] The early fifties saw the advent of the first core memories[10,11] in which selection by a reasonable number of tube drivers was made possible by utilizing the non-linear property of the storage cores. This is also the start of the era of solid state electronics through the practical appearance of the transistor which was soon applied to core memories. Transistor driven

core memories have become, and are today, the classic form of random access memories. In attempting a unified survey of present and possible future memories, it is convenient to consider the selection problem from a general point of view without regard to its historic evolution.

Conceptually the simplest organization of a random access memory consists of separating completely the address selection function from the storing function. Such memories are variously known as "word organized" "switch driven" or having "linear" or "end-on" selection. The memory elements are in a rectangular array with each row line corresponding to a word and each column line to a bit. (Fig. 1). The 2^n word lines are driven by a decoder switch which selects one of the lines uniquely from its n-bit coded address. To write in the bit lines are energized according to the m bit of the word to be stored. To read-out any word, the appropriate word line is selected, and the signals of the bits corresponding to the stored word appear on the bit lines.

Great economy in decoder switching is obtained if the storing cells are made to participate in the address selection function. Consider, for example, that the cell can respond to two simultaneous address selecting signals, instead of one. It is then possible to energize the 2^n words by $2^{n/2}$ sets of selecting lines x and y. (Fig. 2). The economy of the required decoder is evident as the single n to 2^n decoder (e.g., n = 12 to 2^n = 4096) has now been replaced by two much smaller decoders of n/2 to $2^{n/2}$

(e.g., $\frac{n}{2} = 6$ to $2^{n/2} = 64$) capacity. The logic at the cell level is more complicated as two address signals instead of one must be coped with. Greater participation to the switching function by the storing cell could be obtained by having 3 or 4 or 5 up to n selection signals on the cell and providing the appropriate local logic. It is found that two signals are sufficient to bring the decoder problem to within practical proportions, and the complication resulting from the use of additional signals is generally not warranted. Memories organized with such partial cell participation in the selection are variously called "bit organized" "current coincident", or "coincident".

The practical attainment of large memory capacities, e.g., hundreds of thousands to tens of millions of bits, requires obviously the possibility of making very simple and inexpensive storing cells. Hysteretic elements provide a simple means to obtain storage and the required logic at each element. This is achieved as follows. Let there be two periods to every access, a read and a write period. To read, let the single or a linear combination of two or more word selecting signals energize the hysteretic device in a given polarity, so as to exceed the switching threshold. (Fig. 3). This will cause the switching of those elements of the selected word and those elements only, which were initially in the remanent state previously brought about by energizations of the opposite polarity and will leave unaffected all others. The switching of a hysteristic element can create a

transient signal, (e.g., an induced voltage) in an appropriate circuit. In general these signals occur on m common circuits each linearly coupling the 2^n elements belonging to a given bit of all words and thus constitute the m required read-out signals. In the second, or write step, the address signal or signals are of opposite polarity of those in the read step, and are linearly combined with the bit write-in signal. The amplitudes of all signals are chosen so that the combined signals on unselected words never reach the threshold of switching except on those bits of the selected words which have the proper bit write-in signals. These m bit write-in signals can have the same or opposite polarity from the address write signals depending upon the particular system design. The written-in word can be the word just read-out in the previous read period and can thereby restore the information momentarily lost in the so-called destructive method of read-out of hysteretic devices just described. It can also be a new word to be inserted in the memory, in which case the read-out signals of the first period are ignored.

The two period read-write access system is naturally suited to hysteretic devices. The first period in which all elements are brought to a standard cleared state serves for read-out as well as one polarity write-in, so that in the second write-in step only the elements to be brought to the opposite state need be switched.

Hysteretic elements furnish all storage and logic functions required of an element of a random access memory provided that the threshold for the onset of switching is distinct enough so that the desired linear combination of driving signals produces switching while no switching occurs even with a single dissident contributing signal. It is also necessary that whatever transients occur on unselected elements due to partial excitations should not unduly add up in the sensing circuits to avoid masking the read-out signals which are also transients. These conditions require in general a so-called rectangular hysteresis loop and uniformity of properties from element to element. How much deviation from ideal properties can be tolerated depends on the precise nature of the memory system. This important question is considered in the following specific memory descriptions.

III. MAGNETIC MEMORIES

1. Current Coincident Core Memories

a. Principle

Arrays of individual cores operated in current coincidence were the first type of hysteretic memory introduced about a decade ago.[10,11] First experiments and models were with ribbon wound molybdenum permalloy cores.[10,11,12] Bit organized ferrite core arrays are today the most widely used type of high speed memory.

The cores corresponding to each bit of the word are arranged in a plane in rows and columns, i.e., $2^{n/2}$ rows and $2^{n/2}$ columns for 2^n words. There are m planes corresponding to the m bits of the word. Each core is linked by four windings. Two of the windings are connected in series by rows and columns and the two others, the bit-write and the bit-sense or read-out windings, are common windings linking all cores in series. "Single-turn" windings consisting of straight conductors are generally used (Fig. 4). All cores are magnetized to one or the other of two remanent inductions represented by the points P and N on the idealized hysteresis loop of the figure. In this state the array is holding information previously written-in.

To read out, equal pulses of current are applied simultaneously to row and column windings in each array corresponding to the selected word. The amplitude of these currents is so adjusted that their doubling effects produce sufficient magnetomotive force to exceed the knee of the loop for the selected cores in each array at the intersections of these lines, but insufficient to exceed the knee for the other cores on the selected lines where they act singly. Consequently, the selected cores will be magnetized in a standard direction, for example towards P, while all other cores will remain unaffected. It follows, therefore, that the existence of an induced voltage in each of the m read-out array windings, which can be caused in each array only from the switching of the selected core, will indicate that core was switched from N to P, while absence of such voltage indicates

that it was originally in state P. The read out is ascertained by the pattern of voltages on the m read-out windings. The interrogation may change the stored information in the so-called "destructive" read-out mode and must be rewritten to be retained in the memory as was mentioned previously.

To write, pulses of current are applied simultaneously to the selected rows and columns windings of all arrays as well as to the individual bit write windings of certain arrays. The amplitudes of these pulses are equal and equal to those of the read-out pulses and therefore too small to singly change the state of any core. The row and column pulses tend to drive the cores toward N and the bit write pulses toward P. Consequently only those selected cores subject to row and column pulses in arrays where the inhibiting action of the bit write pulses are absent will be driven to N, all others will remain in P. The inhibit pulses will not affect any cores on unselected addresses.

This memory system depends on the discrimination, due to a two-to-one ratio of excitations on the selected cores to that on the most energized nonselected cores and yet the selection is according to three signals: two addressing and one write signal. This is possible because the hysteresis loop has in fact two thresholds, one on the positive and one on the negative range of magneto-motive driving forces. The operation of the system is shown by the schematic of one element, Fig. 5-A.

b. Disturb Voltages

Departure from ideal rectangularity of the hysteresis loop of available materials was an important limitation in the development of the core memories. Only moderate rectangularity is sufficient to prevent cumulative demagnetization due to repetitive half demagnetizing steps, so that loss of stored information has never been a serious problem. On the other hand, the voltages induced in the read-out winding by the half-excited cores on the selected lines did present a problem, as these "disturb" voltages are additive and may mask out the desired read-out signal, particularly in large arrays. Direct pick-up from the exciting windings adds also to the disturbs. Common practice is to use a reading winding in which the directions of cores' linkage are opposite on the two halves of every line, as in a "checkerboard" pattern, so that the disturb voltages tend to cancel each other. (Fig. 4). The cancellation depends on the uniformity of core properties. Great efforts have been devoted to methods of fabrication and of testing of cores. Very good results have been obtained in recent years. However, cancellation is in general not a sufficient remedy to the problem of the disturb voltages, even with the most uniform cores.

The reason for this is that the reversible flux change due to partial excitation of a given polarity is in general somewhat different for the two states of remanence of the core, so that the degree of cancellation depends on the pattern of remanent states established by the particular stored information. The

difference between these two flux changes is commonly referred to as "delta-flux". This difficulty can be alleviated by using, after writing, a routine to "post-disturb" or "pre-disturb" the core with a demagnetizing half excitation, a procedure which tends to equalize the reversible flux changes for the two remanent states during subsequent half excitations and thereby improve the cancellation of disturb voltages.

The most widely used artifice to discriminate against the disturb voltages consists of time strobing the output voltage, and is based on the fact that the unwanted reversible flux changes on the half-excited unselected cores occur much faster than the wanted irreversible flux change on the selected core. Another method[13] consists of integrating the read-out signal, preferably over a reading cycle with two periods, to effectively discriminate between reversible and irreversible flux changes. Still other schemes have been proposed. For example, the row and column can be energized one after the other so that only the half-excited cores on the column contribute to the disturb read-out voltage.[14] This system favors the use of a rectangular array with long rows and short columns. From all methods to deal with the disturb problem, strobing is the most commonly used, as it is very effective and does not lengthen the time required for access to the memory.

The problem of the disturb voltages was brought sufficiently under control in the early fifties so that arrays of 16 x 16 = 256 cores were being operated in computers, and arrays of 10,000 cores were being developed in the laboratory.[13] The rectangularity and uniformity of present day ferrite cores is such that arrays of 64 x 64 = 4,096 cores up to 256 x 128 = 32,768 are in use. In large arrays, the problem of disturb voltages is solved by the simple expedient of splitting the read-out winding and using a separate sense amplifier or preamplifier in each part. A particularly advantageous way to split the winding is by grouping together square subdivisions of the plane along diagonals, as then there are disturb contributions only from the cores on the selected lines continued within the subsquare including the selected core.[15,16]

c. Cores

In most present day ferrite core memories, the mechanism of switching of the square loop cores is primarily through domain wall motions, for the case in which switch-over occurs in times longer than 10^{-7} second. The switching time, T, is related to the magnetizing force, H, by the relation

$$T(H - H_c) = S_w, \qquad (1)$$

where H_c is the coercive field, and S_w a constant, the switching constant.[17]

In the current coincidence mode of operation, the total magnetizing force due to the addition of row and column current drives cannot exceed $2H_c$, since the magnetizing force due to the row or column drive alone cannot exceed H_c. In practice it is generally found that an optimum discrimination between full and half excitations is obtained when $H = 1.5H_c$. It is seen, therefore, that the switching time is proportional to the switching constant and inversely proportional to the coercive force.

The commonly used cores are made of manganese magnesium ferrite. By varying the composition and heat treatment it is possible to obtain a fairly wide range of coercivity. However, it was found possible to exert only a small influence on the switching constant, S_w, which is of the order of 10^{-6} oersted-second for a wide variety of ferrite materials. Consequently, the present practice consists in making so-called fast materials with relatively high coercive force, and so-called slow materials with relatively low coercive force, but among the various compromises between speed and required driving current the essential figure of merit, S_w, remains nearly constant. This is also true for cores made from thin metal ribbon, such as were used in early memories.

In any case, relatively large ampere-turns are required to obtain the requisite magnetomotive forces. The use of single turn windings is dictated primarily by simplicity of construction, but is also necessary to avoid excessive back voltages and delays in large memories. Since the magnetomotive force is inversely

proportional to the flux path length, ring-spaced cores are universally made of as small a radius as technologically possible, so as to minimize the required driving current. Some of the early experiments[13] were with .034" I.D. .050" O.D., but most of the first memories used .050"-.080" cores which considered the smallest practical to make and wire. Present improved manufacturing is mostly with the smaller .030"-.050" cores. Typical characteristics of commercially available cores are listed in Table I.

TABLE I. TYPICAL CHARACTERISTICS OF FERRITE MEMORY CORES

Outside Diameter	mils	.050	.050	.080	.080	.040
Inside Diameter	mils	.030	.030	.050	.050	.025
Height	mils	.015	.015	.025	.025	.012
Switching Time	microsec	.15	1.3	1.2	2.7	0.35
Drive	mA	1100	350	740	360	800

d. Addressing and Digit Write-Read Circuits

The functions required of the addressing circuits are the following. (Fig. 6). The n bit address, stored in a register, must be decoded. In the current coincident memory two decoders for n/2 bits each are required. The two sets of $2^{n/2}$ outputs of the decoders are used to drive the row and columns of the core arrays. Positive and negative pulses are required for the read and write cycles respectively.

The advent of relatively high current transistors has brought about an all diode-transistor solution to addressing circuits which is in common use today. Diode or transistor decoders of the combinatorial type are often made in two steps[15] each $n/4$ to $2^{n/4}$. The outputs of the decoders are amplified by high current output transistors which drive the memory. A read-write gate determines the polarity of the drive. Various ways of obtaining the two polarities are used. In some cases the output transistors can provide both polarities directly.[15] In others, a transformer couples the memory lines to two single polarity driving transistors.[18] In some earlier hybrid circuits the output transistors "steered" the current from a tube-drive.[19]

The m bits of information to be stored in or to be read from the memory are generally stored in a register which serves not only for the input and output but also as a buffer necessary in the process of rewriting the information momentarily lost from the arrays in the destructive read-out process. Transistor amplifiers, similar to those used for addressing, are used to supply the digit write inhibit pulses and are triggered, on command to write, according to the bits stored in the register. The m read out signals, after suitable amplification and strobing, set the register on command to read.

The transistor sensing circuits are complicated by the pick-up on the read winding resulting from the excitation of the write winding of the preceding write-in operation. Without

adequate measures, this unwanted pick-up would be many times larger than the desired signal and would paralyze the relatively sensitive amplifiers for a time which could well be longer than the total time required to read, write, and decode. It is customary to wind the digit write and digit sense windings on the core arrays so as to minimize both magnetic and capacitive pick-ups. This is achieved by a pattern of alternate core orientations and right angle crossings of write and sense winding wires. (Fig. 4). A further artifice consists of using carefully balanced sense amplifiers transformer coupled to the sense windings.

A typical transistor-diode driven current-coincident core memory of 4096 words of 40 bits each may require about a thousand transistors and several hundred diodes.

2. Magnetic Switching

The relatively large numbers of transistors and diodes and the considerable power required may be reduced by using magnetic switches. These were first conceived in the pre-transistor era to reduce the number of high current tube drivers and to simplify decoding. Magnetic switches for decoding and load-sharing are still useful with the advent of transistors and are in common use.

Consider an array of switch cores linked by row u and column v windings.[13] (Fig. 7). All cores are biased by a direct current. The excitation of u or v line alone is just sufficient to cancel the bias and therefore does not switch any core. The

simultaneous excitation of u and v switches the selected core. At the termination of the u and v drives the dc bias restores the selected core to its initial state. Each core of the u X v array is provided with an output winding which is coupled to a row x of the memory array. Another u X v array is used to energize column y of the memory. The switches accomplish several functions: (1) they provide part of the address decoding, (2) they provide both polarities of output with single polarity inputs, thus simplifying the driving problem as well as the winding of the memory array, (3) they allow convenient means for impedance transformation, and matching to tubes or transistors, as it is relatively easy to provide several turns on the switch cores which are larger and less numerous than the memory cores.

There are other modes of operating the switch which do not require a dc bias. For example, in the switch array the selected line v can be driven in the switching direction while all lines u except the selected one can be driven in the inhibiting direction.[20] Alternatively by the proper connection of outputs in shunted groups it is possible to operate the switch in a so-called "set-a-line" mode in which the selected line u is driving and the selected line v is inhibiting.[21] It is also possible to use combinatorial magnetic switches.[11] Among all of these decoder type switches the dc bias type is the most widely used.

Alternatively to a primary decoding function magnetic switches can be used for channeling the power of several sources to a single load. Such "load sharing switches"[22,23,24] permit the use of relatively low current transistors to provide the relatively large current for memory arrays. The energization of a number of inputs can be made to drive a generally smaller number of cores in such a way that one selected core receives the total excitation from all the sources while the other cores receive zero excitation. Fig. 8 illustrates the wiring arrangement for the case of eight inputs and outputs. The signs + and - refer to the direction of linkage through the core of each of the eight input windings linking the cores in series. The currents from the source are assumed to be + or - one unit of current. It is clear from inspection that if the input circuits are excited according to the pattern of polarities corresponding to any one of the eight patterns of winding polarities of the cores, the selected core will have eight units of excitation while other cores will have precisely no excitation. In such a switch the combinations of windings are exploited for load-sharing purposes rather than to gain a combinational advantage in coding or decoding. In general, the inputs to such a switch must be decoded by some other means. It should be mentioned that there are no particularly severe requirements on the nonlinearity of the cores, as the saturation characteristics are useful only to attenuate the effects of whatever inequalities of amplitude there may be between inputs. Load-sharing switches are in use with large capacity memories.[20]

It is also possible to combine decoding with load-sharing functions,[11,24] if some excitation on non-selected cores is tolerated. For such switches cores with pronounced non-linearity are necessary to minimize outputs on partially energized non-selected cores.

3. Word Organized Core Memories

a. One Core Per Bit

Consider an array of cores with row and column windings (Fig. 9). Let each row correspond to a word and each column to a bit of the words. Assume that all cores are in states P or N and are storing information previously written in.

To read-out a given word, the desired row is energized with an amplitude large enough to switch the cores of the row to one of the two states, e.g., N. Voltages are induced simultaneously on all the columns wherein the cores of the row being interrogated were previously in state P, and only on these columns. These are the read-out signals. The read-out step is truly by external word addressing and involves no current coincidence. This has two important implications. In the first place, the read-out signals are free from any disturb signals from cores of other words, as these cores are not energized at all. The only undesired signals on the read-out column are due to "elastic" flux excursions of the cores on the selected row in state N being driven further into saturation. The wanted flux change from state P toward the saturated state N is always easily distinguishable

from these elastic flux excursions. Consequently, considerable deviation from ideal rectangularity of the hysteresis loop is tolerable. In the second place, the read-out current is not limited in amplitude by the selection mode to produce a magneto-motive force equal to 1.5 or $2H_c$, but can be as large as desired, many times larger than the coercive force, H_c. Consequently, it is possible in principle to make the switching time during read-out arbitrarily short simply by making the selecting current sufficiently large (see Relation (1)). The speed is limited by the practical difficulty of obtaining an adequate external switch.

To write or rewrite, the current in the selected row is reversed, i.e., it tends to drive the cores to P. Simultaneously digit write currents are applied to certain or all columns. The amplitude of the write current and the amplitude and polarity of the digit currents must be so chosen that the desired cores on the selected row be switched to P, while cores on unselected rows are not switched at all. This can be obtained in different ways. For example the selected row and the column currents could be of the same polarity and both equal to half the nominal switching current, the column currents being present only in columns where the selected core is to be in P. Conversely the selected row current could be the full switching current and the digit currents on the complementary columns of inhibiting direction and half amplitude. In both cases the ratio of excitations between the selected core and the most energized non-selected core is 2:1. This ratio can be increased to 3:1, by using 2/3 of the nominal drive on the

selected row and 1/3 of the drive on all columns, the polarity of the column drive being plus or minus depending on the polarity to which it is desired to magnetize the cores. Shorter write time is possible with the greater ratio. Even so, the write-in step is not determined by external means but depends on the drive current amplitudes. Therefore the currents and the resulting speed of writing are limited. The schematic of one-core-per-bit word organized memory is shown on Fig. 5b.

The advantages of word addressed memories are obtained at the expense of an external driving switch. Transistor switches driven by diode or transistor decoding switches can be used. To obtain both polarities of drive a single transistor per word can suffice as it is well suited to deliver very large currents of one polarity for read-out and a relatively small current of the opposite polarity for write-in.[15] Memories so driven with read out times less than one microsecond and write-in times of several microseconds have been reported. It is also possible to use magnetic switches of various types.

Depending on the stored word these can be any number from 0 to m of cores switching when a word line is energized. To keep the word current constant despite this variable load large resistances in series with the word line are generally resorted to. This is wasteful of power and is particularly objectionable when magnetic switches are used.

b. Two Core Per Bit

The driving switch can be simplified[21] by the use of two cores per bit instead of one as the voltage induced on the selected row can be made independent of the stored information, i.e., the same for every access. The use of two cores per bit has also fundamental advantages for high speed as is explained later. The two cores store one bit of information by being either in states PN or states NP. (Fig. 5c). On read-out, a large current is applied to the selected row and brings all cores on the row to state N. This induces a voltage on one or the other column winding of the pair belonging to each digit. By connecting the two column windings in series opposition a positive or negative read-out voltage is obtained depending on the stored bit. This arrangement automatically neutralizes the effect of the elastic excursions of flux of the cores driven further into saturation. To write-in or rewrite, the current on the selected row is reversed and simultaneously positive or negative currents are sent through the series connected column pair depending on the nature of the bit to be written in.

Word addressing by a magnetic switch has a number of advantages. Fig. 10 shows a dc biased core switch, each core driving a word of the memory. Fig. 11 shows a switch core and its memory load in the case of a word with a single bit. There are three identical cores, the switch core and the two memory cores. Assume the resistance of the coupling electric loop to be negligible. Let us assume that initially the switch core is in state N and the

memory cores are either in states NP or PN. When the selecting currents on the rows and columns of the switch overpower the dc bias and reverse the switch core from N to P, whichever memory core was in state P is switched to state N. This occurs because the total amount of flux linked by a zero resistance loop must remain constant. The identity of the memory core being switched determined the polarity of the read-out signal on the digit winding. When the selecting currents driving the switch terminate, the dc bias restores the switch core from P to N. This tends to switch both memory cores to P. If there were no current in the digit winding at that time, the two identical memory cores would be switched half way, absorbing equally the flux change of the switch core. A subsequent read-out, due to a new switching of the switch core from N to P, would switch the two memory cores equally, and consequently no read-out voltage would be obtained. However, if during the return of the switch core from P to N, a current is sent through the digit winding which favors one core and hinders the other, the flux change in one core will be greater than that in the other. Consequently, on a subsequent read-out, a voltage is obtained as both memory cores are brought to the standard N condition. The read-out voltage depends on the amplitude and polarity of the write-in current in accordance with a typical characteristic curve, as shown in Fig. 12.

The system, described for simplicity for a one bit word, is adaptable to many-bit words. A single switch for the whole memory is made up of cores each with sufficient large flux capacity

to supply the flux changes of the m bit memory cores pairs which it drives.

The system described above depends on transferring a limited amount of flux from the switch core to the memory cores. This principle has several interesting consequences[21,25]. The read-out step can be arbitrarily fast as in other types of externally addressed memories. The write-in step is still dependent on current selection but the two disadvantages of that selection system — limitation in speed and small tolerances in the amplitude of drive — are largely overcome. The pair of memory cores really stores analog information, i.e., gives a read-out output voltage which is a function of the digit write amplitude according to the characteristic of Fig. 12. For digital storage, only the polarity of the output is ascertained, so that the digit write current can have any value between a minimum which insures no false indications due to unavoidable inequalities between the cores or to noise, and a maximum which insures that the state of storage of non-selected cores is not altered. The ratio of maximum to minimum permissible amplitude of the write digit pulse was a practical range of 3 to 1 when the durations of that pulse and the address-selecting pulses are of the length dictated by the conventional current-coincident operation. Actually, it is possible to use very intense address drive producing very fast switch-overs not only for the read-out step, but also for the write-in, as some unbalancing of flux distribution between the two memory cores will occur in principle for any value of digit write current. However,

it is preferable to use the greatest permissible value of digit write current in order to obtain as large a read-out signal as possible. For very short pulses, this maximum value is several times greater than it is for pulses of duration compatible with conventional current operation. Therefore there is essentially no significant limit to the maximum permissible drive in the whole read-write cycle, so that two cores per bit magnetically switch driven memories have the possibility of being very fast.

c. Fast and Impulse Switching of Ferrite Cores

The possibility of using extremely high current pulses both for the read and the write cycles in a two-core per bit word organized memory driven by a magnetic switch is dependent on the fact that the total flux changed in the memory cores is necessarily limited to the flux in the switch core. Since the flux is transmitted through an electrical linkage loop, the flux limitation must result in a limitation of the duration of the induced current in the loop. This demonstrates that it ought to be possible to obtain any desired change of flux in a core in a very short time provided sufficiently intense current impulses are used. Extensive studies of impulse switching of ferrites in the last few years confirm this expectation.[25-34]

Let us consider a core brought to a standard level of saturation, as for example the zero state resulting from a large read pulse. When a pulse I producing a field exceeding the coercive force is applied to the core, the core will switch completely provided the pulse is longer than a minimum time T. The

relation between I and 1/T is made up of two or three straight line segments corresponding to different values of S_w presumably resulting from different switching mechanisms.[33] When the pulse duration t is shorter than T, only part of the flux is reversed as was found in fast transfluxor setting characteristics.[28,29] Later extensive experiments[30,31] with impulse switching of cores revealed a number of interesting properties. For example an amplitude (e.g., 600 mA) of a short pulse (e.g., 150 nsec) can be chosen to produce practically no flux change while a relatively small increase (e.g., 200 mA) can produce a substantial change. This non-linear behavior was applied to a word organized memory[34] in which the word write cuttent supplies the larger part of the reversing current and the digit or exciter current the smaller part is insufficient to disturb non-selected cores. The memory has 1024 words of 80 bits each and is operated sequentially with addressing times of less than one microsecond. It is believed that comparable cycle times are possible also with random access operation.

When the duration t of the pulse is sufficiently reduced there is no irreversible flux change, even partial. However the amount of reversible flux change depends strongly on the remanent state of the core and can be used for non-destructive read-out.[26,30,35] These effects were first observed[26] with molybdenum permalloy cores with pulses of about 100 ns duration, and were attributed to domain wall viscosity effects.

d. Transfluxors and Multi-Aperture Cores

The drive of a memory by a magnetic switch was shown to be based on transfer of flux from the switch core to the memory cores by means of electrical linkages. This concept can be generalized to direct geometrical transfer of flux between branches of cores having multiple flux paths.[21] The principle of the transfluxor and multiple aperture cores called by other names depends on such transfer of flux. These devices have broad utility for many switching and storing functions all of which will not be surveyed here. Only their applications to memories will be considered.

A three apertured transfluxor can be used instead of the switch core and the two memory cores of a one bit word memory.[28,29] (Fig. 12). Here the dc links leg 1, and the selecting currents X and Y link the central aperture; i.e., both legs 1 and 2. When the sum of energizations of the windings X and Y exceeds that of the dc bias by an amount sufficient to produce switchover between leg 1 and legs 3 and 4, the latter will be brought to saturation. If they have been previously left in unequal states of remanence, this will produce an output voltage on the digit winding linking legs 3 and 4. When the selecting currents X and Y terminate, the dc tends to transfer the total flux of leg 1 through legs 3 and 4. Assuming for a moment that the path lengths 1 to 3 and 1 to 4 are equal, this would produce equal amounts of flux (equal to half that contained in leg 1) through legs 3 and 4. If, during this time, a digit current is sent through the digit winding, unequal

amounts of flux will be transferred, because that current will favor transfer of flux to one leg and hinder it to the other. Consequently, the relation between the read-out voltage and write-in current will be similar to what it was for the three cores. (Fig. 12). It is interesting to note that the total amount of flux through legs 1, 2, 3, and 4 must not only be constant in this case, but identically zero. For this reason it is necessary to have an additional leg, leg No. 2, which is really a dummy and serves merely to make up for the balance of flux.

If the lengths of path 1 to 3 and path 1 to 4 are not equal, as is true in the case of the core having the geometry shown in Fig. 11, there will be unequal division of flux between legs 3 and 4 even when the digit current is zero. Various geometries are possible to make these flux paths equal. One geometry consists of properly shaping the center aperture in the shape of a "U". Another consists of locating legs 3 and 4 on either side of leg 1 and splitting dummy leg No. 2 in two halves. Also a right angle aperture can be used.

In another three aperture core arrangement,[36] a dc bias and X and Y windings through the central aperture are used also. The sense winding is on leg 4 only. The direction of magnetization of that leg stores the bit. To read, the X and Y windings are energized and overpower the effect on the dc in the windings in legs 1 and 2. This causes the flux to be clockwise (Fig. 13) on the whole core and may reverse leg 4 if it was magnetized upwards from a preceding write. At the termination of the X and Y pulses

the dc causes flux changes in legs 1 and 3 only. To write "one" the X and Y currents are applied in the opposite direction causing the whole core to be magnetized counterclockwise, i.e., causing leg 4 to be magnetized upward. In a m bit arrangement the bias winding has a pulse component in a direction and amplitude to inhibit the action of the X and Y windings on the digits which it is desired to keep in the "zero" condition established in the read period.

The three hole cores of the above two systems act simultaneously as the storage cell and as the access switch. Because the operation is dependent on geometry of the core there is considerably less dependence on the existence of a well defined threshold of switching, and a greater latitude to deviate from ideal loop rectangularity. This allows a greater permissible range of operating temperatures. The dc bias system allows as large drives as desired and therefore the speed of operation is not intrinsically limited.

The same advantages of speed and tolerances exist in a three hold memory core operated in an inhibited flux mode for a word organized memory.[37] The word line links the central hole, the bit write line links leg 1 and the sense line leg 4. (Fig. 14). To read, a current pulse is applied to the word line of sufficient amplitude to magnetize the whole core in a given direction, e.g., clockwise. This produces a read out signal if leg 4 had previously been magnetized upwards and stored a "one". To write, the word current is reversed, and simultaneously bit

write currents are applied to windings in leg 1 on the bit location where it is desired to write "zero". These bit currents inhibit switching of leg 1 and therefore cause flux to switch only around the central aperture in legs 2 and 3, leaving leg 4 in the "zero" state established by the read pulse. The bit current on unselected cores causes switching between legs 1 and 2 without disturbing leg 4. In experiments with single cores having .015" holes switching times of about a microsecond were reported.

A thousand word memory made with three hole cores was described[38] in which the inhibit flux mode was obtained slightly differently. The word winding threads both the central aperture and the aperture between legs 1 and 2. The bit location in which the bit currents are applied corresponds to writing a "one" instead of a "zero" as in the previous arrangement and this results in a polarity of bit current which disturbs "zero's" rather than "one's" on unselected word locations.

4. Non-Destructive Read Out Memories

The transfluxor's main property is the possibility of ascertaining the state to which it was set without altering that state. This non-destructive read-out property can be used for memories in which read-out need not be followed by a rewrite.

In a two-apertured transfluxor having three legs,[39,40] the amount of remanent flux in leg 1, which is equal to the negative algebraic sum of fluxes in legs 2 and 3, determines how much transfer of flux between legs 2 and 3 is possible. (Fig. 15).

There can be an indefinitely long back-and-forth exchange of flux between these two legs, the amount of which is determined by the flux initially set in. The transfluxor is blocked when legs 2 and 3 are saturated in the same direction as one or the other leg denies flux flow. The amount of setting determines the amount of flux that can be changed in one of the legs 2 or 3 before it is saturated. That same amount will necessarily appear in the other leg. The device can be used to store analog as well as digital information. Only its digital applications are of interest here.

An array of two hole transfluxors can be linked with one set of column and row windings through the large input apertures, and another set through the small output apertures.[40] (Fig. 16). Current coincident setting of the transfluxors is possible because there is a threshold of current required to produce setting around the larger aperture, and similarly, coincident read-out can be obtained because there is a threshold of current required to switch the flux around the smaller read-out aperture. A non-destructive current coincident m bit random access memory can be made, by providing digit write and digit sense windings through the large and small aperture respectively. (Fig. 16). In such a transfluxor memory the read-out can be faster than with core memories with destructive read-out.

Additional read-out holes can be provided in the transfluxor so that it is possible to read-out information simultaneously to several destinations. This is the principle of a multiload transfluxor memory.[41] It is also possible to combine the

non-destructive properties of the transfluxor with the various methods of fast setting described above.[28,29]

The non-destructive read-out of the transfluxor depends on switching back and forth the non-elastic flux set successively in legs 3 and 4. Such action is possible also with cores having two holes at right angles to each other.[40,42] Alternatively non-destructive read-out can be obtained in a number of ways by switching elastic reversible flux in simple ring cores or in multiaperture cores. An early proposal is based on the difference of polarity of the curvature of the hysteresis loop at the two remanent states which can be determined by the phase of the beat resulting from applying two small amplitude ac voltages of different frequencies to the X and Y windings.[43] Recent work with impulse switching mentioned above consists of observing the amplitude of reversible flux resulting from the application of large amplitude pulses so short as to produce no irreversible changes[26,30,35] It is also possible to ascertain the sense of remanent flux flow by the polarity of its change as it is momentarily diminished through the application of an orthogonal field. This can be achieved in a bobbin coil by sending a current through its ribbon.[43] In ferrite ring cores, the orthogonal field can be obtained by a solonoid wrapped around the core[44] or else, as in a recent proposal,[45] by a solonoid wrapped diametrically around the core. In ferrite cores having non-intersecting orthogonal holes in various forms, non-destructive mechanisms have been proposed on the basis of the rotation of the magnetization in the legs of the core common to the

main remanent flux path and an orthogonal interrogating reversible path.[42,43] It is also possible to use an interrogating hole parallel to the writing hole, or hole cluster, and applying an interrogating small amplitude current to one of its legs and obtain thereby more or less flux change depending on the direction of remanence of the leg.[46]

In general non-destructive read-out memories are particularly useful when frequent and rapid read-out is necessary and relatively slow write-in can be tolerated. This is the case in a number of applications ranging from data processors in which the ratio of read-outs to write-in may be typically 4 or 5 to application where there is essentially read only. This is the case for example for an airborne memory to be set on the ground and frequently read-out in flight. Non-destructive read-out can give also added insurance that information in the memory is not lost due to a malfunction in the read-rewrite circuitry of destructive memory, but proper engineering is required to take advantage of this possibility. In general the non-destructive memory is more complicated as separate addressing circuits for write-in and read-out are necessary and for this reason the simpler destructive read-out memories are used more commonly. Common addressing circuits are possible in certain forms of word organized memories driven by fast impulses, which are thus particularly advantageous for non-destructive read-out.[26,30,35]

5. Ferrite Apertured Plate Memories

Arrays of individual ferrite cores have become a classical solution to selective access high speed memories. The techniques of making and wiring individual cores can be improved upon by using an integrated method by which a large number of elements are made and wired in one step, as in the case with ferrite aperture plates.

A plate with a regular array of holes is molded from square-hysteresis-loop ferrite material. The direction of remanent magnetization around each aperture stores one bit of information. There is no interference between magnetizations around adjacent apertures because for a given current through an aperture, the magnetizing force diminishes gradually with radial distance and, at a well-defined distance chosen to be less than half the width of the leg between adjacent apertures, becomes smaller than the threshold of switch-over. The plate thus constitutes a unit conveniently fabricated as a whole in a single step and is equivalent to a number of cores. Furthermore, the ferrite being an insulator it is possible to "print" windings directly on the plate and thereby eliminate the need for some of the manual threading. This is particularly suitable for making a winding which links all the holes in series.

Plates with an array of 16 x 16 = 256 holes have been developed and are finding increasing use. (Fig. 17). The holes are .025 inch in diameter and are spaced .050 inch center-to-center.

The plate is less than an inch square. Squareness of the hysteresis loop and switching characteristics are comparable to that of individual cores made of the same material. Very uniform properties from hole to hole and plate to plate have been obtained. About 300 milliampere-turns are required to switch over the magnetization around an aperture in 1.5 microseconds.

The plates, stacked with all the holes in register are threaded in a single operation which does not need to be repeated separately for each plane as is necessary for memory core planes. Plate memories can be used in current coincidence or external word selection.

For current coincidence operation the holes of the stack of plates are threaded back and forth by row X and column Y windings. With this wiring pattern the direction of coupling of the selecting lines is the same as that of the printed winding and, therefore, during read-out the disturb voltages would add up rather than tend to cancel each other. This difficulty can be overcome by various wiring arrangements. For example four plates can be used in a module.[49,53] The plates are arranged in a square and are connected in series diagonally in pairs. The two diagonal pairs are connected in series opposition and the midpoint is grounded. A stack of quartets of plates is wired as a whole by X and Y selecting windings. In the reading step, the polarity of the difference voltage between the two non-grounded terminals of the diagonally connected plates is sensed by a difference amplifier and is indicative of the identity of the stored bit. The

disturb signals tend to cancel each other. For writing or rewriting, the inhibit signal is sent into both branches of the common winding, in one polarity in one and the other polarity in the other. Extremely good discrimination is obtained with this arrangement. This is due in part to the high uniformity of the plates and in part due to the lack of any appreciable air coupling. Planes of that type including as many as 16 plates yield satisfactory discrimination ratios. It is also possible to print patterns of windings with three or four terminals to obtain similar operation. This is done in a recent development of a 4 x 32 rectangular plate.[50]

The apertured plates are particularly suitable for external word addressing as the switch can be made of plates identical to those used for the memory. The memory stack and the switch stack can be wired as a whole with a bundle of wires going through all the holes. The switch stack is wired in addition with X and Y selecting windings. The switch can be operated in a number of ways such as set-a-line system,[21,51] and the dc bias system. The latter seems to be the most advantageous. Bias current can be conveniently supplied through the printed winding. The memories with a dc bias switch and a pair of plates for each digit were made according to the system explained previously in connection with core memories.[52] In this case, the operation is not strictly flux limited, since the amount of flux available from a plate hole increases monotonically with the drive. It turns out, however, that very fast operation and larger tolerances in current are possible with the plates than with cores.[52]

Apertured plates are fundamentally more economical to fabricate and test than are the corresponding number of individual cores. Also their assembly and wiring into memories is considerably simpler. Furthermore, a smaller driving energy is necessary as it is possible to use a much smaller amount of material to store one bit than is necessary with individual cores which become unmanageable when very small.

A 4096 word with 16 bits per word memory operating in current coincidence with a cycle time of about 4 μsec was reported recently.[48] This memory utilizes 16 x 16 ferrite "sheets" similar to the "plates" described above.

6. The Twistor

A way to utilize a magnetic wire for the elements of a random-access memory has been reported in 1957.[54] Consider a magnetic wire or ribbon wrapped around an insulated non-magnetic wire (e.g., enameled copper) in the form of a helix making an angle of 45° with respect to the axis. Let there be in addition a solenoid around the wire (Fig. 18). This constitutes the "barber pole type" form of twistor. The combined effect of a current I_s through the solenoid and of a current I_w through the wire produces a magnetizing force parallel to the helical wire. The lines of flux will follow the easy path along the helical wire and return from the ends of the wire through the space surrounding element. The hysteresis loop is very rectangular due to the anisotropy of the wire created by its longitudinal tension.

The air return path has no serious shearing effect on the loop as long as the ratio of length-to-diameter of the element (enhanced by the helical path) is sufficiently large to insure that the demagnetizing field is smaller than the coercive force.

Originally, a form of twistor which consisted simply of a twisted magnetic wire was reported. The twist causes lines of strain at 45° with respect to the axis. The resulting anisotropy produces an easy direction of magnetization and permits twistor action by the combination of a current through the magnetic wire itself and through a solenoid wrapped around it. As the operation is dependent on the amount of twist, this seemingly simpler type of twistor is not as convenient to use in large memories as the barber-pole type.

The twistor can be operated in a bit or in a word organized mode. A word organized memory system driven by a ferrite core dc biased switch has been described.[55] The barber-pole twistor wires correspond to the digits of the word. The words are selected by one turn solenoid coils which link the twistors by lines and which produce axial magnetic fields. (Fig. 19). Read-out is obtained by sending through the selected word line, a current I_s intense enough to switchover the twistors which it links. The twistors which were previously magnetized in the opposite direction, switchover and produce a read-out signal on the corresponding twistor central wires. These signals are relatively intense, because the magnetic wire wraps around many times the "single turn" central wire. This gain in voltage is a unique

property of the twistor. The twistors which were previously magnetized in the direction of the read-out drive undergo small reversible flux charges. The write-in is obtained by a current coincidence mode, as the effects of the currents I_s in the word solenoids and of the current I_n in the central wires add algebraically.

The barber-pole twistors are made by wrapping on .003-inch insulated copper wire a .001-inch permalloy wire flattened to .0003 inch. These wires are embedded in parallel lines spaced ten to the inch between two sheets of polystrip plastic. Similar polystrips with embedded ribbons of copper wire are placed on either side of the twistor sheets to provide the words selecting coils.

Some developments of twistor memories include a random access memory of 500 words of 100 bits each within a cycle time of 6.4 μsec.[56] Also reported is a twistor buffer store.[57] A new form of twistor, the counter-wrapped twistor has been reported recently.[58]

7. Fixed Memories for Read-Only

The twistor memory has been adapted for the storage of semipermanent information.[39] This is a type of fixed memory with random access "read only" capability. The information is stored by the pattern of small permanent magnets superimposed on the array of twistor elements. The field of the permanent bar magnet is along the direction of the twistor central wire, and opposite

to the field created by the word solenoid. It is sufficiently intense to prevent switch over of the twistor element over which it happens to lie. The selected word solenoid is energized positively and then negatively and this causes a back and forth switching of the twistors not paralyzed by the magnets. The resulting induced voltages are sensed on the central wires. The pattern of magnets is made by etching sheets of Vicalloy bonded to plastic cards. The cards are inserted between layers of twistor arrays in arrangements which provide for proper registry. A 512 word, 26 bit per word, store operating in a cycle time of 5 microseconds has been reported.[59] This card changeable nondestructive read-out twistor store is fully transistorized and uses 50 watts of power.

The twistor permanent memory is really a large code converter with a semi-permanent pattern of conversion. Other forms of such fixed memories are related to core memories or to the switching concepts used in the electrically accessible memories and are thus a natural parenthetical subject in this paper.

Fixed memories can be obtained simply by omitting cores at selected locations of conventional arrays and permanently writing a one in all locations having cores. The vacancies can be created in the original wiring or by breaking selected cores of an initially full array. Shorting selected cores to paralyze their operation is possible also. It has been proposed[60] also to thread each word line through selected cores of a single row of cores.

Switching arrays comprising N inputs and M outputs such that the excitation of one input causes a given pattern of excitation among the M outputs, (as in the word organized twistor memory) has been accomplished[61] twenty years ago by a pattern of resistances coupling selected intersections between two groups of M and N parallel intersecting conductors. In a recent development[62] ferrite slugs are positioned at selected intersections of N parallel elongated coils with M such coils places at right angles. Reported also is a development depending on capacity couplings at the selected positions.[63] In these switches, the resistive, capacitive or inductive couplings are linear and operate only if the M necessary sensing output devices have nonlinearity, preferably a sharp threshold of response.

Permanent memories are useful in computers to store subroutines for microprogramming and for storing arithmetic or other tables. It is often possible to use access circuitry in common with the inner high speed memory proper. Interest in permanent memories is increasing as they can substitute in certain cases for parts of the regular memories and provide faster access and larger capacity at lower cost. Permanent memories have a number of other applications in data processing and data transmission as well as in telephone switching.

8. Thin Film Memories

About five years ago it was suggested[64] that memory elements made of thin Permalloy films could have high switching speeds inherent to a rotational mechanism of flux reversal and could be fabricated conveniently by evaporation techniques. Since then, the physics of the film behavior and various memory systems and fabrication techniques have been studied extensively,[67] and initial successes with experimental memories have been reported. The subject has been surveyed recently with some detail.[65]

The magnetic alloy of zero magnetostriction consisting of 81.5% nickel and 18.5% iron is deposited on a smooth substrate through evaporation in vacuum or through electroplating. Uniaxial anisotropy is established in the films by an orienting film during the formation of the element or in a subsequent anneal. Anisotropy can also be established through evaporation at an oblique angle.[68] The material acquires an easy direction of magnetization along which the hysteresis loop is square and a hard direction at right angles to the easy direction along which there is a straight characteristic and practically no hysteresis. The film is characterized by a coercive force H_c along the easy or longitudinal direction and an anisotropy field H_k along the hard or transverse direction. (Fig. 20a). At remanance, the film is magnetized longitudinally in one direction or the other. Magnetization reversal can occur either by domain wall motion or by rotation or by both depending on the nature and geometry of the film and the nature of the drive. The switching threshold and the switching

time depend on both the value of the longitudinal field H_L and the transverse field H_T. Typical dependence is illustrated on Fig. 20b. In general, the switching coefficient S_W has different values for different strengths of H_L and H_T, generally a relatively high value of the order of one oersted microsecond for low drive when switching is mostly by wall motion and values lower by an order or even two orders of magnitude for high drives when switching is mostly by rotation.

Memories can be made by evaporating a regular array of circular spots on a glass substrate. The circular shape is chosen to eliminate anisotropy effects during rotation of the magnetization. In order to keep down the demagnetization effect of the free poles at the edges of the film, the ratio of radius-to-thickness is made very large, typically about 2×10^4.

An early experimental memory[71] had 4 mm diameter dots 2000 Å thick. The conductors were flat strips placed in close proximity to the glass. At the element position, the row, the column, the inhibit, and the sense conductors were made to run parallel to each other and made a small angle with respect to the hard direction of magnetization of the elements. The application of the drive currents, in conventional current coincident operation, produced a main component of field in the longitudinal direction and a smaller transverse component which enhanced switching. Difficulties were encountered with uniformity of spots.

In a more recent memory[72] combinatorial advantage is taken of the possibility of controlling separately the longitudinal and the transverse field components. The memory is word organized with the attendant greater tolerances on film characteristics particularly with respect to uniformity. The word line provides the transverse field and the bit line the longitudional write field. The application of the selected word line current rotates the element to the hard direction. This induces a voltage on the sense winding of a polarity corresponding to the previously stored remanent state in the easy direction. There is a dc current through all bit lines and an opposing greater current is applied to all lines on which it is desired to write a one. At the termination of the word current the magnetization, momentarily in a naturally unstable state of hard magnetization between two stable states, rotates to the easy direction corresponding to the longitudinal field in the direction of the dc bias or the write current. The sense winding is made of two balanced halves to reduce coupling to the write winding. The simple straight windings required were made by winding a few turns around the glass substrate. A 32 word, ten bit per word, memory using 1.5 mm spots 600 A thick was operated so as to demonstrate the feasibility of a cycle time of .5 or even possibly of .2 microsecond. (Fig. 21).

A very recently described memory[73] utilizes a continuous film evaporated on an aluminum substrate instead of a dot array on glass. The film, made of an alloy called gyralloy, is about 1000 A thick. The memory is word organized and uses also transverse

field word and longitudinal field bit drives. However the biasing to favor the zero direction is obtained by inclining the two windings slightly with respect to the anisotropy axis of the films, instead of dc currents in the bit lines. The conductors are flat strips obtained by evaporating copper directly on the suitably insulated film or by laying thin films of plastic carrying the strips. Because the conductors are in close proximity to the film, the induced magnetic fields are very localized and the film switches right under the conductors and only a small distance away. The reversal stops abruptly at a point where the field is insufficient for switching. In a sense, the storing elements are created by the magnetic field instead of having to be fabricated. This simplifies the construction and eliminates exacting requirements of dot-to-winding alignments. A more fundamental advantage is the greater ease of obtaining uniform elements through the elimination of spot edges whose erratic nature was found to be an important cause of variability of switching properties. Also, there are several advantages to the use of a metal substrate. The sense line whose return is through the grounded substrate is very close to it, being separated only by the magnetic film and a thin insulation, so that it offers very little effective area for coupling to the write winding. The magnetic field at the film due to the drive is increased by the eddy currents in the plate. The inductance of the drive winding is kept at a minimum. A prototype memory with 50 words of 50 bit each was built. It has lines spaced about 3 mm apart on aluminum plates of 3 x 7 inches. Word currents of 1.2 amp and digit current of .5 amp yield signals of 3 millivolts for word pulses rising in 40 nanoseconds. (Fig. 22).

Another proposed form[74] of thin film memory having continuous elements in one direction, consists of using electrodeposited nickel-iron films on a copper wire in which a circumferential easy direction is obtained by the presence of a current through the wire during plating. The plating is a continuous operation obtained by pulling a wire through the electrolyte. As with twistors, the plated wire can be used in a word organized memory in an arrangement of as many parallel lengths of wire as there are bits and surrounding the bundle by a number of solonoids, one for each word. The axial field due to the word solonoid can produce non-destructive read-out by rotations of the field of less than 90^{o}. The sense voltages appear on the wire. Because there are no demagnetizing effects in the closed flux path in the easy direction, films as thick as 12,000 A can be used, yielding correspondingly stronger signals. Typically, 50 mv from 1.5 mm length of .005" wire are obtained in .15 microsecond. Write-in is by coincidence of currents through the solonoids and through the wires.

A form of memory similar in geometrical concept and mode of operation to the wire memory consists of using a set of parallel cylindrical glass rods on which thin films have been evaporated.[75,76] An experimental model of another cylindrical film memory was reported.[77] The model with 256 bits has yielded a cycle time of less than a microsecond.

9. State of the Art of Magnetic Random Access Memories

The present state of the art in computer magnetic random access memories can be summarized as follows.

The most widely used type are memories made of ferrite cores (50-80 or 30-50) which are transistor driven. Storage capacities vary between 10^4 and 10^6 bits and cycle access time is of the order of 10 microseconds. Some of the later memories have access times of about 2 microseconds.

Ferrite plate and twistor memories are in use also with capacities of about 10^5 bits and cycle times of the order of 3 to 5 microseconds.

Typical memories are listed in Table II.

TABLE II. TYPICAL MEMORY SYSTEMS

Type	Words	Bits/W	Cycle Time μs	Remarks	Year
TX-2 S Memory	65,536	37	6.5	Core current coincident	57
TX-2 X Memory	64	19	4.10	Word organized two cores per bit	57
Transac S-1000	4,096	38	20.0	Core current coincident	57
IBM704 - 738 Memory	32,768	36	12.0	Core current coincident load sharing	57
RCA 501	16,384	28	15.0	Core current coincident	58
Lark	10,000	60	4.0	Core current coincident	58
Bell Gamma 60	32,768	6	10	Core current coincident	59
Siemens 2002	1000 to 10,000	49	14	Core current coincident	59
BTL Twistor Memory	500	100	6.4	Twistor memory elements. Word organized.	59
Stretch 7302	16,384	74	2.18	Core current coincident oil cooled load sharing switch	60
Telemeter LQ	512-8192	4-100	1.5	Core word organized	60
BTL Sheet Memory	4,096	16	4.0	Ferrite sheets or plates. Current coincident	60

10. Considerations on Speed and Capacity of Magnetic Memories

a. Speed

A few general considerations apply to the present efforts to speed up memories with thin films or ferrites. These are: the inherent switching speed of the element for driving current attainable with the best semiconductor drivers, its ability not to overheat at high repetition rates, the transmission time along driving and sensing lines which is mostly determined by the physical size of the element, the strength of the read-out signal, the importance of masking signals inherent in the operation, and the ease of obtaining sufficiently uniform elements.

Thin film elements cannot be arbitrarily small because of the demagnetizing effects resulting from the open magnetic path. Smallest practical spacing with dot arrays and continuous film appears to be about 10 to the inch. With this size and the best materials, currents of a few hundred milliamperes available from the latest transistors can switch the film in tens of nanoseconds. Transmission delay per bit is about .02 nanosecond assuming a propagation speed of 10 cm/ns or a third of the speed of light. The signal output is of the order of one millivolt. To be amplified to usable levels amplifiers with delays of the order of ten nanoseconds are required. Masking signals in the sensing circuit induced from the addressing and digit write windings are very large due to the required high currents. Using neutralizing winding geometries and closely spaced grounding planes it has been possible

to reduce the peak of masking signal to be two orders of magnitude greater than the read-out signal, a reduction still short of ideal. Thin films present no overheating problems. Great difficulties have been encountered in obtaining uniform films. Intensive studies of basic reasons for observed variations is likely to overcome this difficulty.

Ferrite memory elements can be switched by currents whose amplitude is not restricted by the operational mode. This is possible either through the use of short pulses or by using a multiaperture geometry. Favorable to fast switching is also the decrease of the switching constant with the intensity of the drive. Cores can be made arbitrarily small with no fundamental limit due to demagnetizing fields since the flux paths are closed. Diminution of size reduces the current requirements, the transmission time per bit, and the effects of heating at high repetition rates. Miniaturization is a question of technique. With present molding practice multiaperture cores have been made with .015 inch holes which switch in tens of nanoseconds with currents of hundreds of milliamperes, available from the best of present transistors. Element spacings of twenty per inch seem feasible leading to a transmission delay of .01 ns/bit. Signal output voltages are in the order of one volt with present core size, leading to a simple amplifier with a short delay. While the masking effects of the pick-up in the sensing loop are relatively less important it is still difficult to cope with the large pick-up due to digit writing. Uniformity problems have been largely overcome by the

extensive strides of the ferrite technology.

At present, small capacity film and ferrite memories have been operated with a fractional microsecond access time. It is likely that memories of a capacity of a few hundred short words can, and probably will, be made in the near future with both techniques to achieve a hundred nanosecond write-read cycle and corresponding ten megacycle repetition rates. Capacities of thousands of words with cycle time of about a microsecond have been already achieved with ferrites and are very likely to be obtained with films. The question of obtaining the larger capacities at the higher speed awaits further engineering with either technique.

b. Storage Capacity

The question of obtaining large storage capacities, at any electronic speed, is mostly one of economy in the fabrication. Present cost per bit is an appreciable fraction of a dollar. Capacities of billions of bits are thus economically unthinkable even if technically realizable. The magnitude of the problem can be illustrated by the consideration that a third of a century would be required for an automatic cell fabricating machine yielding a bit per second to produce a billion elements. Obviously integrated means to fabricate many elements in a single step are indispensable. The apertured ferrite plate and the twistor are examples of such integrated techniques with which a modest progress has been achieved.

Major innovations in the concepts of construction are still required to obtain electronically addressable random access memories with billion bit capacities. Because such memories would have crucial practical importance in a number of applications, one can optimistically assume that such concepts will be found. In the meantime, electromechanical random access memories with capacities of millions of bits and access times of about a second will be utilized.

IV. FERROELECTRIC MEMORIES

In ferroelectric materials internal polarization effects produce a hysteretic relation between the electric induction D and an applied electric field E. The D-E loops are similar to the B-H loops of ferromagnetic materials. Some materials such as barium titanate, exhibit square hysteresis loops. (Fig. 23).

When a varying electric field is applied to a ferroelectric condenser, the integrated current that flows through it can be thought as being a trapped charge Q. A hysteresis relation exists thus between the measurable quantities Q and applied voltage V. With square loop materials, practically no current flows when the condenser is driven from remanance further into saturation, but a large current flows momentarily when the condenser is reversed from one remanent state to the other. The time of reversal is inversely proportional to the excess of the applied electric field with respect to a constant field (the coercive field). A relation similar to relation (1) can be written.

Proposed memory systems[78,79] utilize an x-y array of ferroelectric condensers in which each condenser is connected between a row conductor X and a column conductor Y. (Fig. 23). The application of voltages to one column and one row conductor produces a voltage difference on the element at the intersection which is greater than that which appears on the other elements of the selected lines. Consequently, if the hysteresis loop is reasonably rectangular, voltage coincident systems similar to the current coincident systems of magnetic memories can be used. Because no third electrode is available on the condenser, the read-out cannot be obtained from an ad hoc circuit as is possible in magnetic memories. One must resort to measuring the current which flows in the selected lines at the instant of selection and sense, whether or not it has an increment due to the reversal of the selected element. Because of lack of perfect loop squareness, the total current flowing through the unselected elements on the selected line may be much larger than this increment. This makes it very difficult to operate the memory in voltage coincidence, as was found in various reported attempts.[78,79,80] In a word organized memory sensing could become a manageable problem.

Most work was with barium titanate.[78,79] Arrays of 16 x 16 elements were made on single crystals of less than a square centimeter area by painting two perpendicular sets of parallel strips on the two sides of the crystal.[78] Also arrays of single units were used.[79] Difficulties were encountered with element uniformity, with creeping of the remanence due to repeated partial

depolarizing voltages, and with loosening of the electrodes caused by piezoelectric effects. With more recent materials such as Gash, Thiouera, and Triglycine Sulfate these difficulties would not be as severe.

The ferroelectric approach has not come out of the experimental stage and it is questionable whether it ever will be able to compete with its magnetic counterpart. Apart from practical difficulties encountered thus far, there are inherent reasons for this. (1) The ferroelectric condenser is a two terminal device which makes sensing difficult as mentioned above, and precludes also any signal cancellation circuit arrangements. (2) There is no topological necessity to provide for the geometrically more complex linkage of windings through holes as in the closed flux path magnetic approach. However it turns out that this topological necessity of magnetics is not as severe as first believed. On the other hand, the problem of making electrodes with sufficiently intricate and stable contacts is more difficult than first suspected. This is because the slightest interface layer between the dielectric and the electrodes introduces a series impedance much greater than the impedance of the ferroelectric at the instant of switching. (3) In ferroelectric materials the stored energy per unit volume is much higher than it is in magnetic materials with which extreme miniaturization is already necessary to bring drive requirements down to a reasonable level. (4) At present, ferroelectric materials are not as fast as magnetic materials.

V. CRYOELECTRIC MEMORIES

1. Superconductive Memories

a. Principle

About five years ago D. A. Buck reported[81] on his pioneer demonstrations of the utility of superconductive phenomena for computer elements. Since then, intensive work in this field has established superconductive, and more generally cryoelectric, techniques as main contenders for computer logic and memory realizations. Logic gating by cryotrons is based on the control exercised by a magnetic field in the transition of the superconductive to the normal state. Memory cells, realizable by cryotrons, are obtained more elegantly through the use of superconductive persistent currents or trapped flux. The operation of such cells is as follows.

Consider a closed loop of superconductive metal and in close proximity to it another, driving loop. (Fig. 24). Let us suppose, that a superconductive current flows in the closed loop in a given direction as a result of a previous write-in. Let the current in the driving loop rise and the polarity be such that the induced e.m.f. in the loop will tend to increase the supercurrent. The loop current I will increase until it reaches a critical value I_c at which time the loop becomes normal and the current starts to decay as a result of the non-zero resistance. If the drive current is maintained, the loop current will decay to zero. This occurs due to Joule heating of the loop by its

current I which raises the temperature sufficiently to decrease the critical current I_c and keeps it lower than the current I so that the loop does not become superconductive until the current I has decayed to zero. Now, if the driving current is turned off, a supercurrent of opposite polarity will be induced which will not reach the critical value since there is no previously induced additive current. In this way the supercurrent of the loop is switched.

The operation is similar to that of an element possessing hysteresis. There are two distinct remenant states corresponding to the two directions of flow of the supercurrent. These states persist indefinitely without any external holding energy. To switch from one state to the other the drive must exceed a certain threshold in the direction establishing the desired state and it must remain at the high value for a sufficiently long time. In the case of the superconductive cells, this time is necessary to dissipate the stored magnetic energy in the resistance of the loop and is determined solely by the thermal and L/R time constants of the element. It does not depend on the strength of the drive as is the case with ferromagnetic and ferroelectric cells. The operational similarity of the superconductive cell to hysteretic cells allows it to be used in similar memory systems.

To obtain a low L/R time constant, the resistance R of the material when it becomes normal should be as high as possible and the magnetic flux created by the supercurrent should be as small as possible. This can be achieved by using thin film

superconductive elements made by evaporating in high vacuum suitable metals and separating insulating layers. Films about 2000 Å thick are found to have appreciable resistance in the short lengths of interest. The magnetic flux around a superconductor is kept small by confining it to occupy a very small volume, by means of sandwiching superconductive ground films which are perfect magnetic shields. The limit of this confinement is the ability of making adequate thin insulating films. Furthermore, with this flat construction of the cells the ratio of heat dissipating surface to heat storing volume is high so that the thermal time constants can be very short. Indicative of the short L/R and thermal time constants obtainable by the thin film techniques are elements which have been switched to a few nanoseconds.[82] The film fabrication techniques provide also a convenient means to make in an integrated manner whole arrays of elements with all the necessary interconnections. For these reasons all current research is with thin film devices in contrast to the earlier work with wire wound devices.

b. The Crowe Cell

A storage cell can be made[83] by using a film with a hole crossed by a narrow diametrical strip bar. (Fig. 25). The persistent current flows in a figure eight pattern with a heavy concentration in the strip which is the active part of the cell. The drive and sense lines are placed on either side of the cross bar and are separated from it by proper insulation. When the drive exceeds a threshold value the cell switches, i.e., the direction

of the persistent supercurrent in the cross bar reverses. At that instant the flux linkage around the cross bar and the sense winding reverses and a voltage is induced in the sense winding.

An extremely important property of the Crowe cell is the complete lack of spurious coupling between the drive lines and the sensing lines separated by perfect superconductive shields. The coupling appears only at the desired location when the selected cross bar becomes momentarily normal. Consequently the ratio of wanted to unwanted signals is determined only by spurious pick-ups in the leads. This pick-up can be compensated for with high accuracy because there are no "delta" noise effects.

c. Continuous Sheet Superconductive Memory

The main difficulties experienced with Crowe cells are the variation of the currents required for their switching. The lack of uniformity may preclude their use in current coincident systems. These variations are due chiefly to the strong dependence of critical field on the nature of the edges of the bridge.[84]

There is a good promise[85] that these difficulties can be eliminated by using a continuous sheet of superconductor without any fabricated holes in them. Two perpendicular sets of parallel suitably insulated lead strips are evaporated on top of a continuous film of tin. When an X and a Y strip carry a current I, the magnetic field pattern at their intersection is at 45° with respect to the strips. (Fig. 26). The intensity of the field is maximum at the intersection, and diminishes gradually with

distance. Consequently there is a region limited by a definite boundary within which the supercurrents induced by the change of the field exceed the critical value and outside of which it does not. In this way a superconductive elemental region is created without the necessity of any holes in the film. It is found that these regions are stable.

In all other respects the continuous sheet element operates as the original Crowe cell. The sense winding is located on the opposite side of the film with respect to the drive lines and picks up a voltage only at the instant and location at which a selected element is switched.

d. Other Types of Cells

Another type of cryoelectric memory element is the persistor[86] and the closely related persistatron.[87] In the persistor memory element, a superconducting inductor is in parallel with a switch element that is normally superconducting, but which becomes resistive when the current exceeds a critical value. When a suitable current pulse is applied to a persistor memory element, a persistent circulating current is stored. A second pulse in the same direction as the first makes no change, but a pulse in the opposite direction reverses the circulating current and produces a voltage across the element. By mutual inductance coupling to two or more driving circuits, these memory elements can be made to operate in matrices. Memory elements of this type have been operated with 15 millimicrosecond pulses at a 15 mc repetition

rate. The great advantage of complete shielding of the sense line from the drive lines afforded by the memory planes in the Crowe type memories is not obtained in persistor memories and thus arrays of only limited size can be made.

e. Memory Systems

The circuits for addressing and sensing superconductive memory array can consist of cryotrons. These devices can be fabricated by similar thin film techniques making it possible to make the whole memory by an integral construction. This has the advantage that only a few leads, — for the n address bits, the m information bits and for controls and power supplies — need to be brought into the cold chamber. Cryotron trees and cryotron sensing amplifiers can be used. The speed of the memory would depend mostly on the speed of the cryotrons. Although low gain can be tolerated in this application, it is unlikely that cycle times of less than one microsecond could be obtained with any reasonable storage capacity.

It is possible also to use transistor or tunnel diode circuits at room temperature in conjunction with superconductive memory arrays. Higher speeds of operation could be obtained in such a hybrid arrangement which do not seem to present insurmountable matching problems. Cycle times of tens of nanoseconds are conceivable.

f. Outlook

Superconductive techniques for memory have a number of inherent advantages: persistent current flow is a natural form of storage, there are sharp switching thresholds, there are perfect shields against undesired signals, switching times can be of the order of a few nanoseconds, and the stored energy per bit can be very low. Furthermore, elements small enough to allow packing of at least 100/cm seem possible yielding a transmission delay of only 10^{-12} sec/bit. There is also promise in vacuum evaporation for a good integrated technique of memory fabrication.

The necessity of maintaining the memory at the temperature of boiling liquid helium is an inconvenience at present. Special experimental techniques are required. Liquid helium although reasonable in price is not always readily available, it is wasted. However, closed cycle refrigerators are being developed[88] with sufficient cooling capability for a reasonable computer, typically capable of maintaining an electric load dissipating as much as 3 watts and occupying a cubic foot at a temperature of 3.3°k. When these become an economic reality, cryoelectric elements may prove no less practical than conventional components requiring air conditioning or cooling systems.

Results of efforts to implement these great potentialities have been reported in three areas: (1) greater understanding of the superconductive phenomena particularly with regard to the transition between superconductive and normal states,

(2) experiments with single and a few memory cells demonstrating that all required properties for memory systems can be obtained and that the switching times can be very short, and (3) suggestions on methods to make memory systems. No fundamental difficulties have been found. The problem seems to be chiefly one of technology.

It is reasonable to expect that superconductive memories with thousands of words and cycle times in the microsecond range will become a reality in the near future.

2. Cryosar Memory Applications

A high speed semiconductor cryoelectric element, the Cryosar, reported recently,[93] may be used for making ransom access or fixed memories or for driving superconductive memories. The Cryosar is a two terminal device made of doped germanium. There are two forms.

In one, the impurities such as indium are not compensated. The element exhibits a very high resistivity up to a certain critical field after which the current increases by orders of magnitude. There are thus two distinct regions: one of high and one of low resistance. Such diodes can be used for making fixed memories or function tables.[93] It has also been proposed to use these monostable diodes for drivers of superconductor memories.[94] Such drivers could probably switch more current in less time than cryotrons. Devices of this kind have been proposed for making fast amplifiers.[95]

To obtain the read-out signal several solutions are possible despite the difficulty presented by the use of two terminal devices already mentioned in connection with ferroelectricity. The signal can be obtained by direct pick-up from a common circuit resistively or capacitively coupled to all elements corresponding to a bit of a word. This attenuates the signal in proportion to the number of words and thereby brings about an unavoidable delay due to necessary high amplification. Several methods to couple through induction or radiation have been suggested also.[90,5]

Drivers of tunnel diode arrays must be able to supply pulses of relatively large power. The current is large because many elements are driven in parallel, and the voltage is high because the voltage of the series current regulating resistances must be several times greater than the voltage swing of the tunnel diode. Typically, hundreds of milliamperes and several volts must be provided. The best promise for a switch of this power handling capability operating in nanoseconds is the tunnel diode itself. Sufficient voltage can be obtained by connecting a number of tunnel diodes in series, and adequate current simply by using sufficiently high current units.

Physically small storing elements are possible. The active region of a tunnel diode is typically about a square mil so that very close spacing is possible with adequate integrated technology. Presently available individually packaged units have been reduced to a capsule 1.2 mm in diameter and .7 mm high.

These units and their associated resistances can be packed at about 5 per cm. The delay per bit is thus about .02 na/bit. A tolerable 5 ns transmission delay permits the use of 250 elements per line. Center-tapping of the lines and other artifices permit one therefore to contemplate memories of about a thousand words.

It appears thus that tunnel diode memories may achieve cycle times of the order of ten nanoseconds: the diodes themselves are fast enough, there does not seem to be insurmountable sensing or driving problems, and the physical size of the storing elements is sufficiently small. Their use entails the requirements of dc holding power not necessary with hysteretic devices. Also the cell structure of a tunnel diode element is relatively more complicated than that of magnetic storing elements. Despite these disadvantages with respect to the more elegant hysteretic types, the tunnel diode offers at the present time the best and possibly the only solution to ten nanosecond random access memories.

VII. CONCLUSION

About 15 years ago the central importance of a high speed electronic memory for computers was recognized. The first types depended on serial access. These were soon followed by the development of electrostatic storage tubes with which it was possible to obtain far more versatile random access addressing. About eight years ago random access magnetic memories started to displace tubes and are now the dominant type in use. Ferrite core memories with capacities of hundreds of thousands to a million

bits and access cycle times of 2 to 15 microseconds are common.

Present efforts with impulse switching of single and multiple apertured ferrite cores as well as the work with thin magnetic films are likely to lead to memories with an access time of 100 nanoseconds. The advent of the tunnel diode two years ago opens the possibility of memories with an order of magnitude shorter access time.

Ferrite aperture plates, three years ago, and the twistor two years ago, were significant steps to provide the integrated fabrication methods necessary to obtain large storage capacities. Ferroelectric memory experiments for the same purpose did not show promise. On the other hand, superconductive elements which have a history of only five years, offer great promise. These cryoelectric elements can be fabricated through vacuum evaporation by methods which may provide the required integrated technique.

Selective addressing by coded addresses known as random access is a great improvement with respect to serial time addressing. This is chiefly because of the freedom of organizing successive processing steps in any desired order, and in particular in an order depending on the progress of the processing itself. A still greater versatility of addressing would be obtained if it were possible to address the memory directly by its stored contents instead of indirectly by the labelling addresses. This would allow, for example, to answer the question as to whether or not a given word is stored in the memory without scanning through all

the words. Also it would be possible to find a complete stored word upon giving a few of its digits. Such content addressable memories must have logic circuits associated with all storage elements. Some experiments with content addressable memories or "catalog" memories were reported four years ago[91] and utilized wire wound cryotrons for storage and logic. More recent work is with evaporated cryotrons.[92]

Progress of computer memories in the last fifteen years has been tremendous and its rate steadily increasing. This trend is likely to continue because the memory is the central part of all data processors and any improvements in it have a determining influence on the performance of the whole system. We can look forward to faster, larger, cheaper, and more versatile memories.

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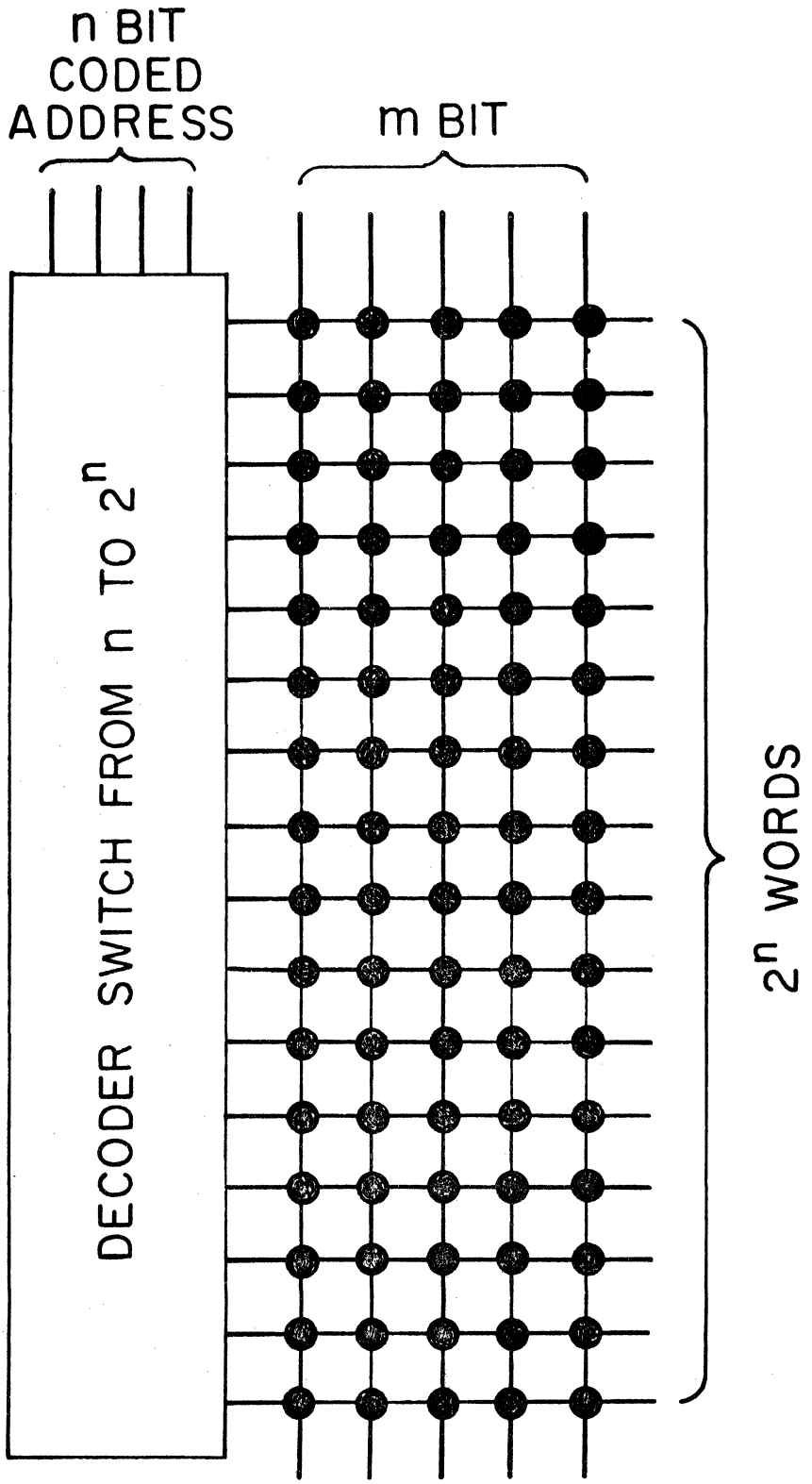


Fig. 1. Word-Organized Memory

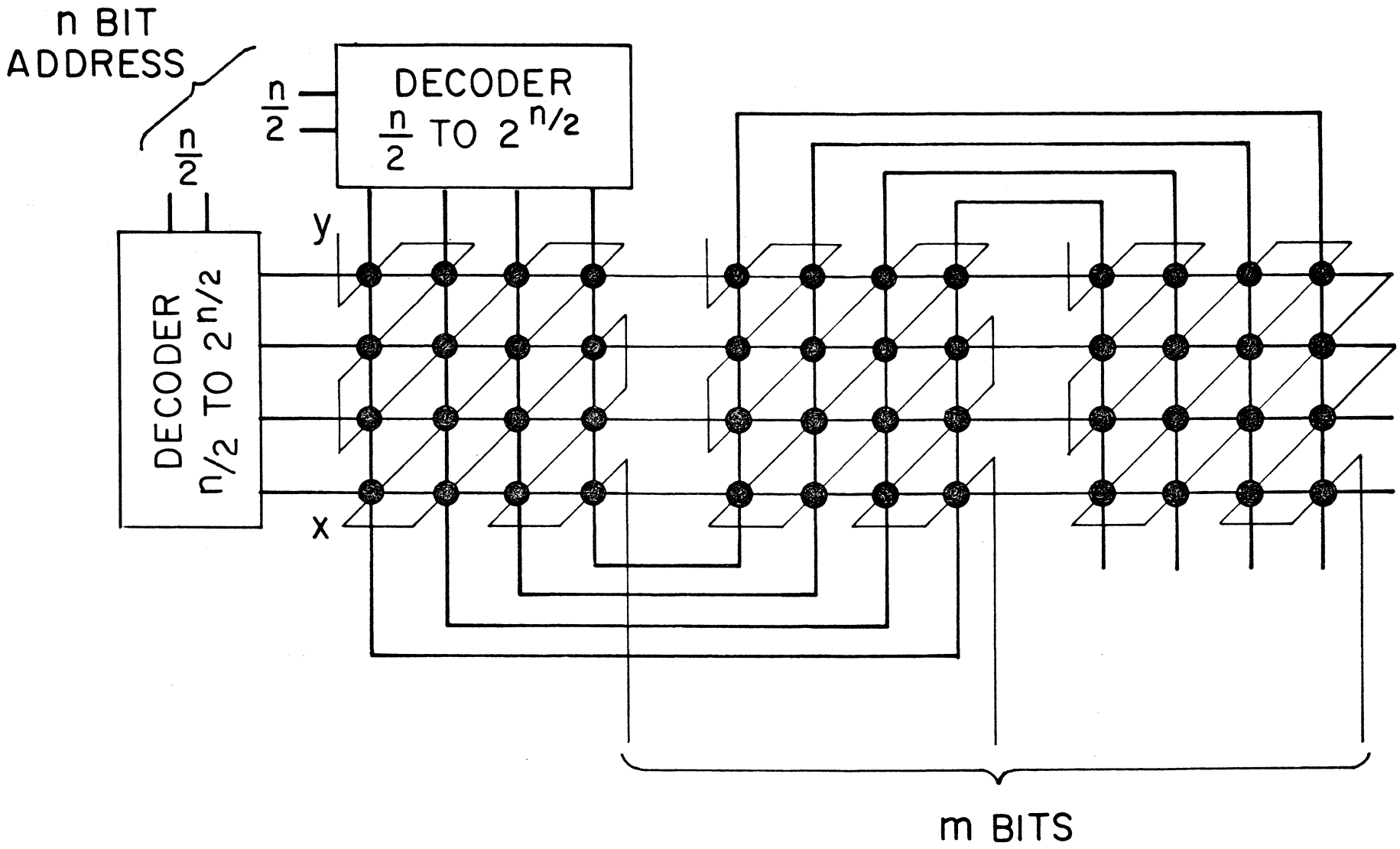
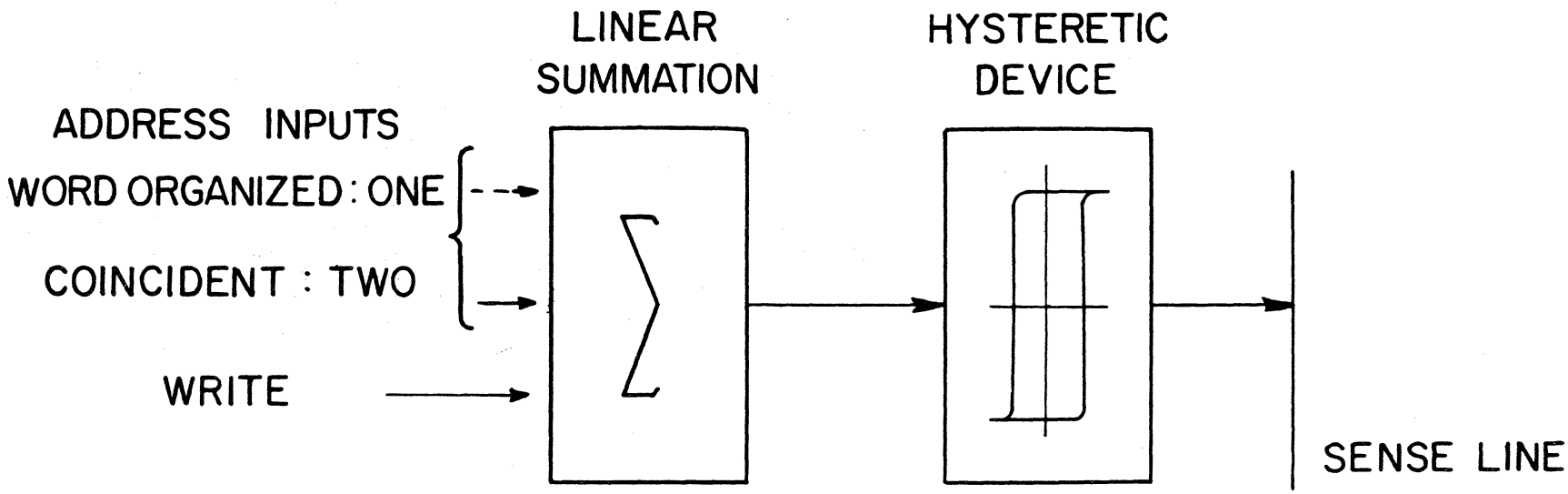
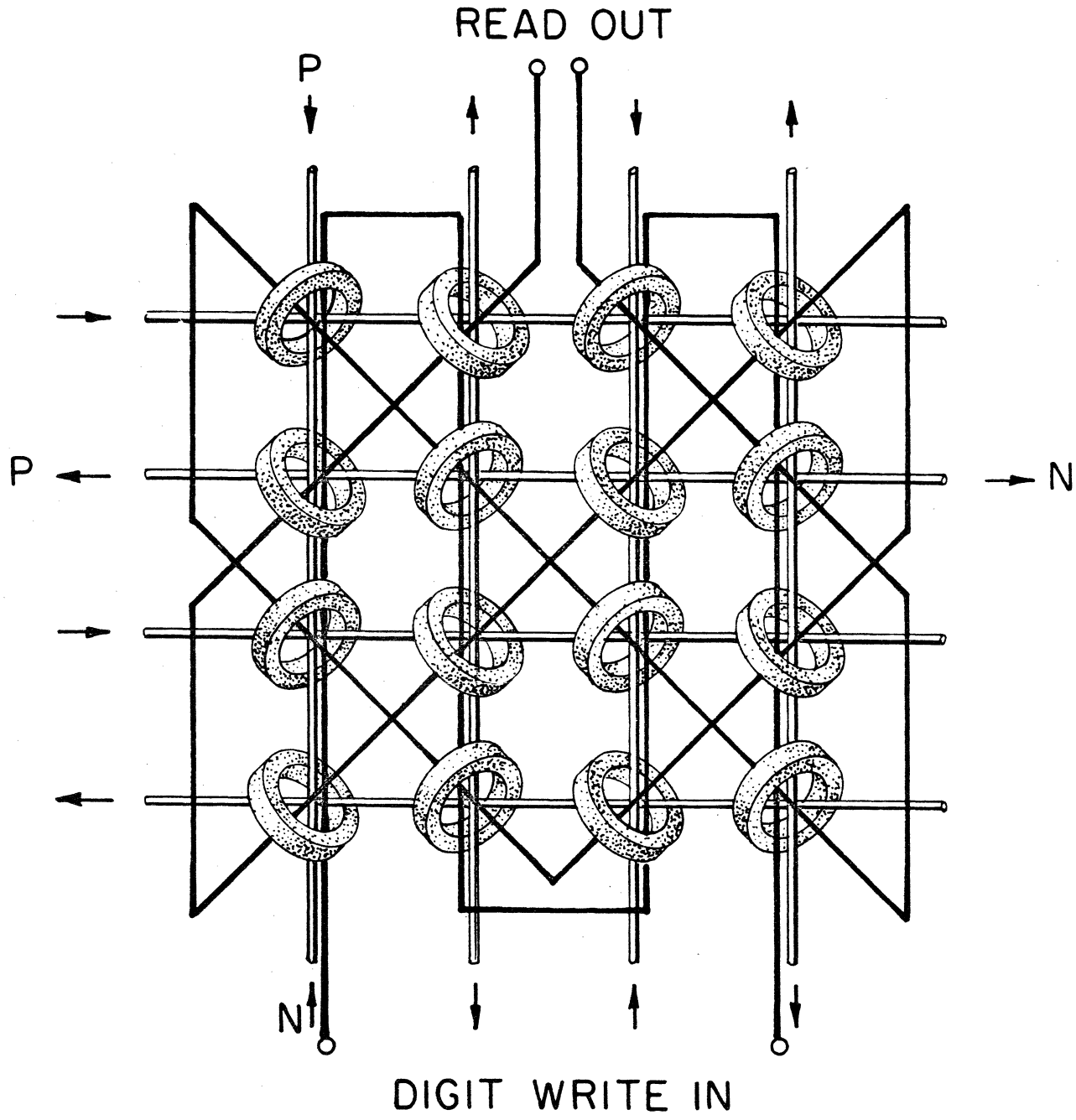


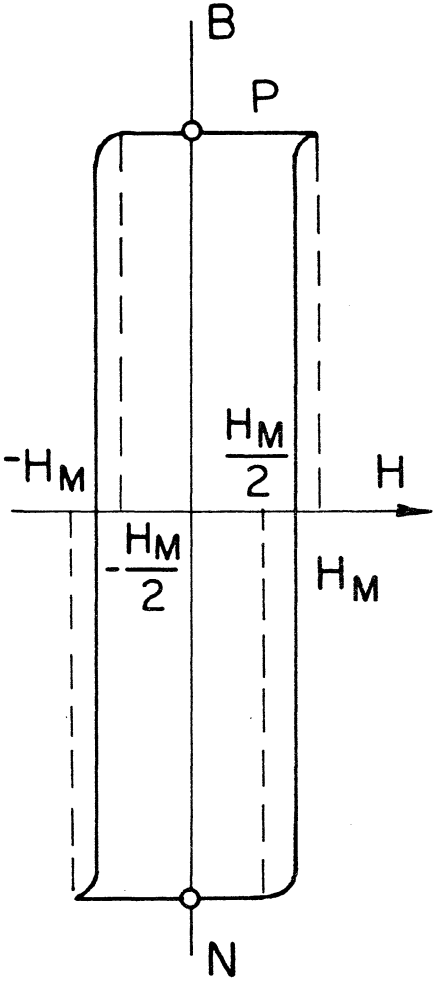
Fig. 2. Coincident or Bit Organized Memory



	READ PERIOD	WRITE PERIOD
ADDRESS	+	−
DIGIT SENSE	SENSE	
DIGIT WRITE		+OR −

Fig. 3. Schematic of Hysteretic Memory Cell


READ OUT
P
P
N
N
DIGIT WRITE IN


B
P
H_M
$-H_M$
H
$\frac{H_M}{2}$
$-\frac{H_M}{2}$
H_M
N

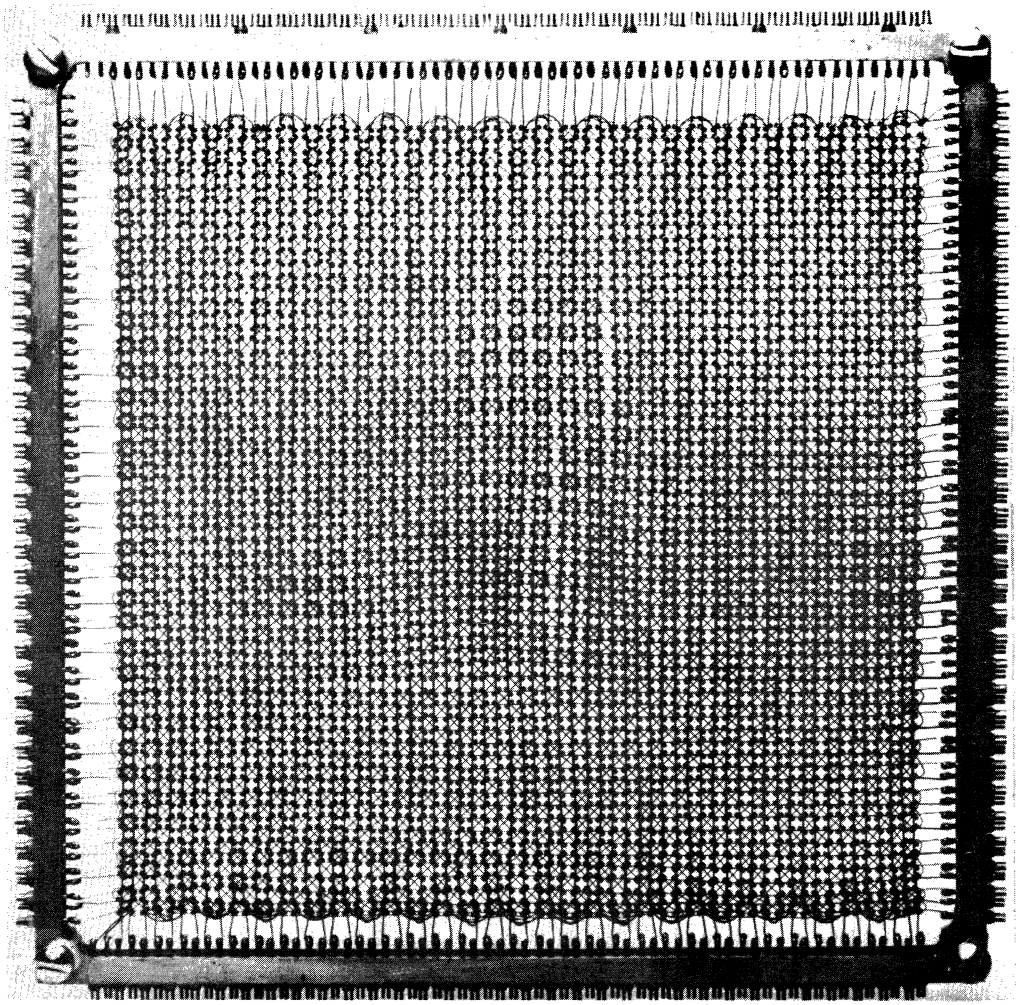
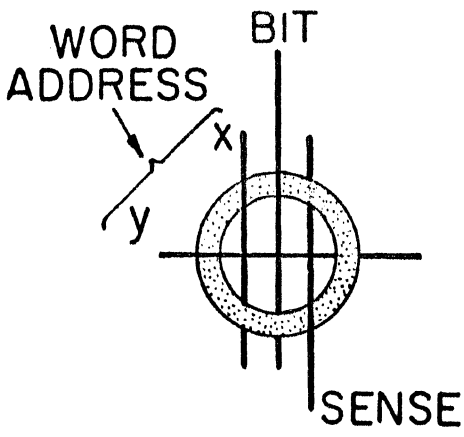


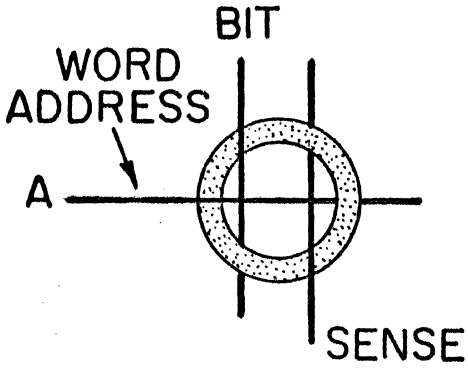
Fig. 4b. Typical Core Plane



CURRENT COINCIDENT

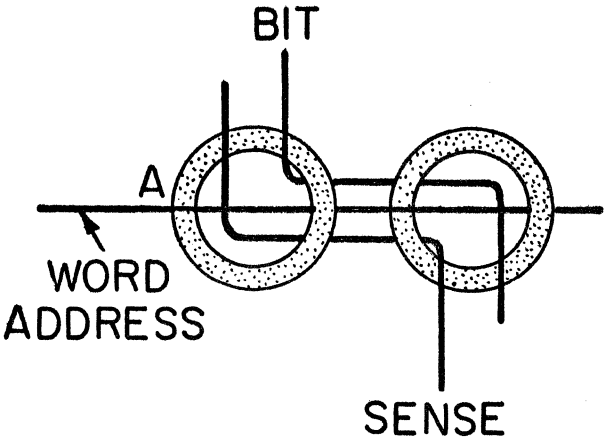
	READ	WRITE
X	$+\frac{1}{2}$	$-\frac{1}{2}$
Y	$+\frac{1}{2}$	$-\frac{1}{2}$
B		0 OR $+\frac{1}{2}$
S	V OR 0	

WORD ORGANIZED



ONE CORE PER BIT

	READ	WRITE	
		MODE I	MODE II
A	+1	-1	$-\frac{2}{3}$
B		0 OR $\frac{1}{2}$	$+\frac{1}{3}$ OR $-\frac{1}{3}$
S	V OR 0		



TWO CORES PER BIT

	READ	WRITE
A	+1	-1
B		+b OR -b
S	+ OR -	+

Fig. 5. Storing Element and Energizations for (a) Current Coincident Memory (b) Word Organized One-Core-Per-Bit (c) Word Organized Two-Cores-Per-Bit

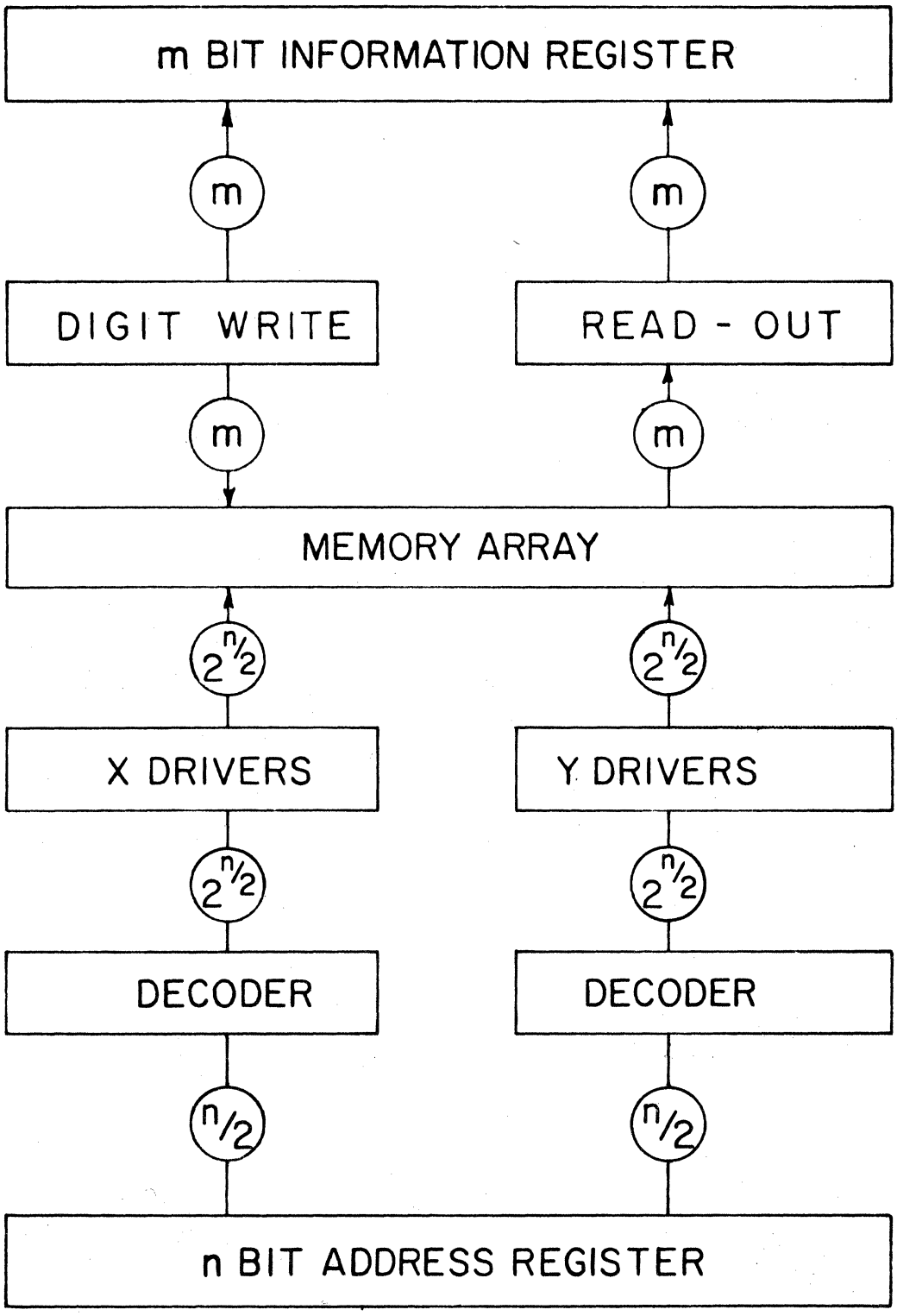


Fig. 6. Schematic of Typical Current Coincident Memory System

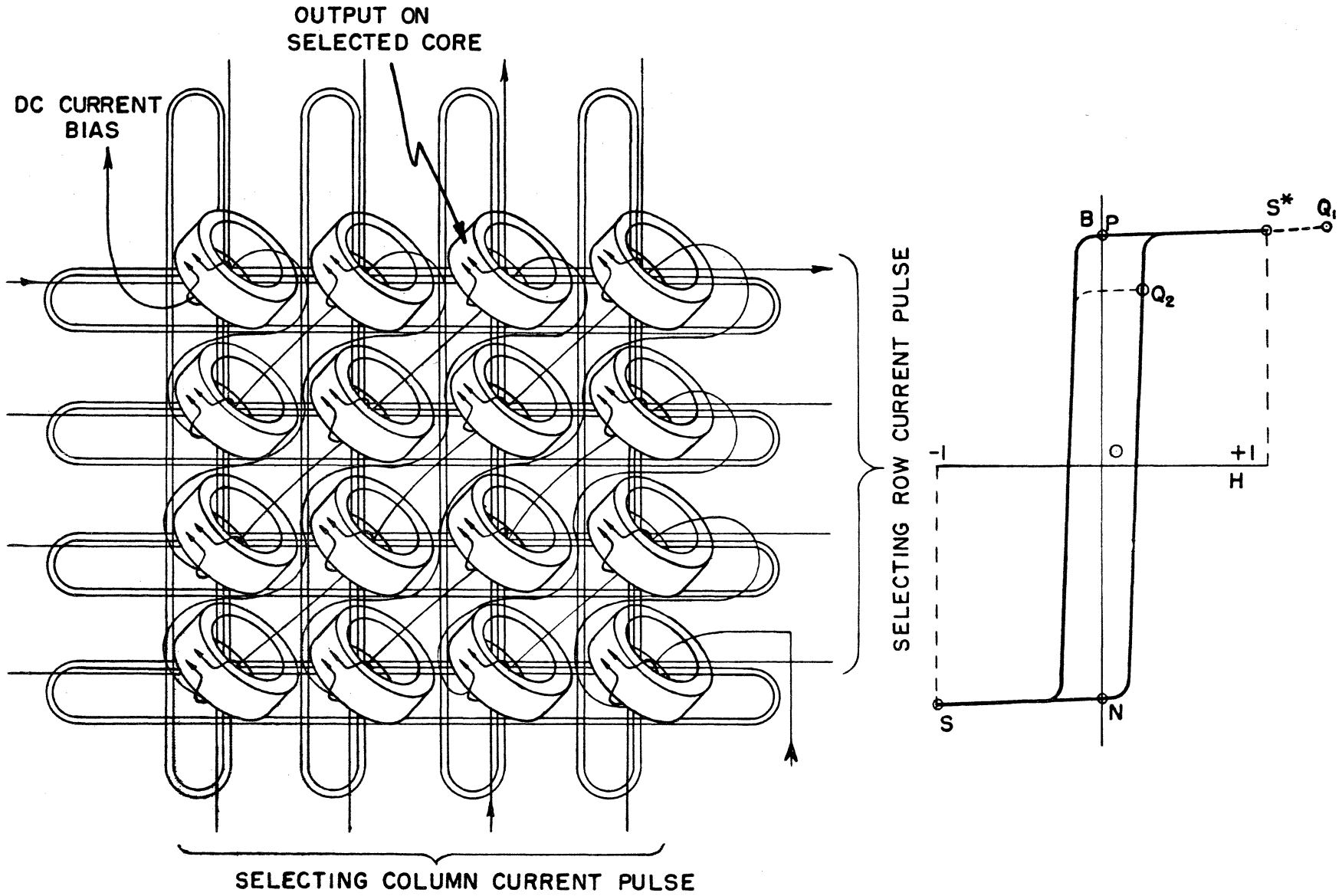


Fig. 7. DC-Biased Magnetic Switch

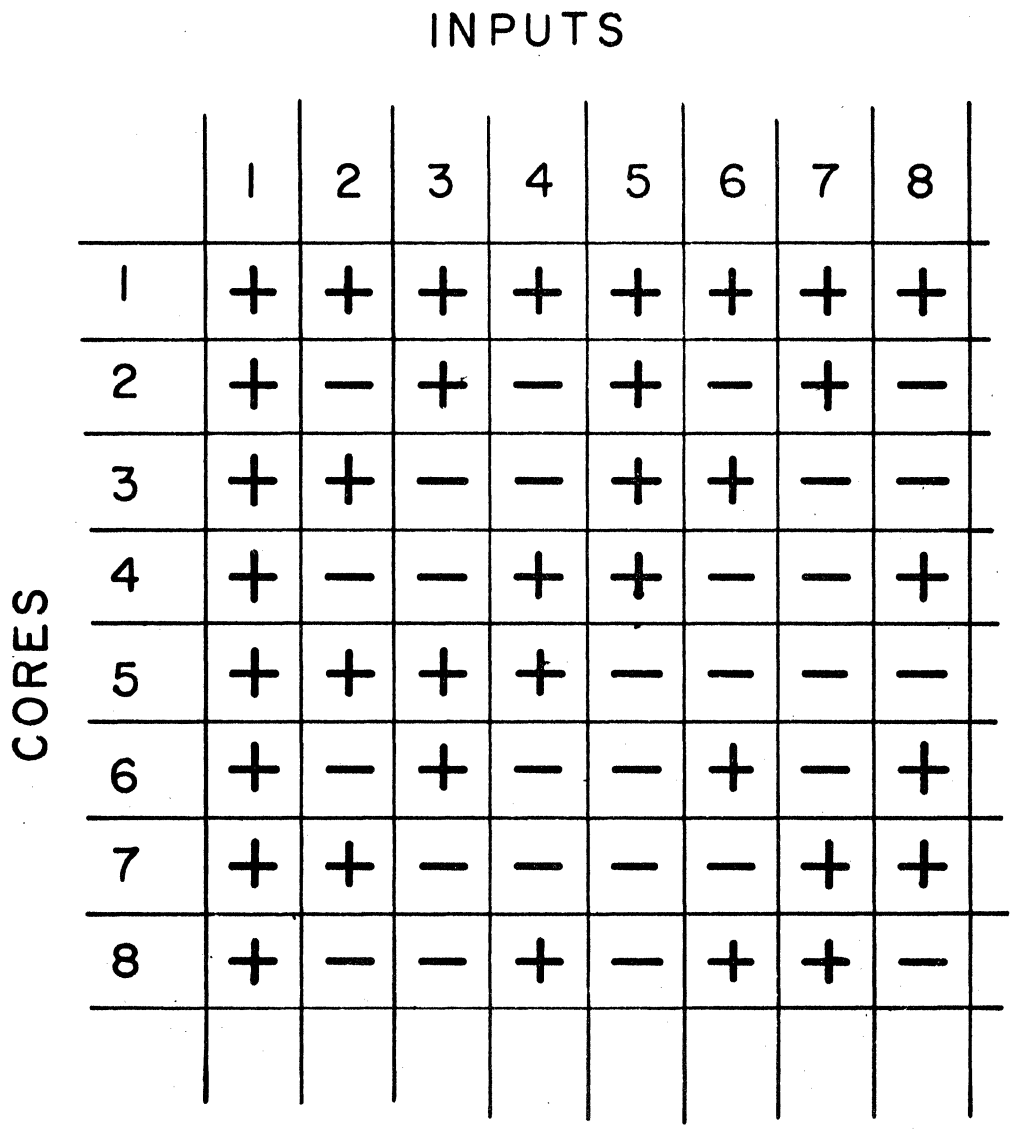


Fig. 8. Pattern of Windings for a Load-Sharing Switch

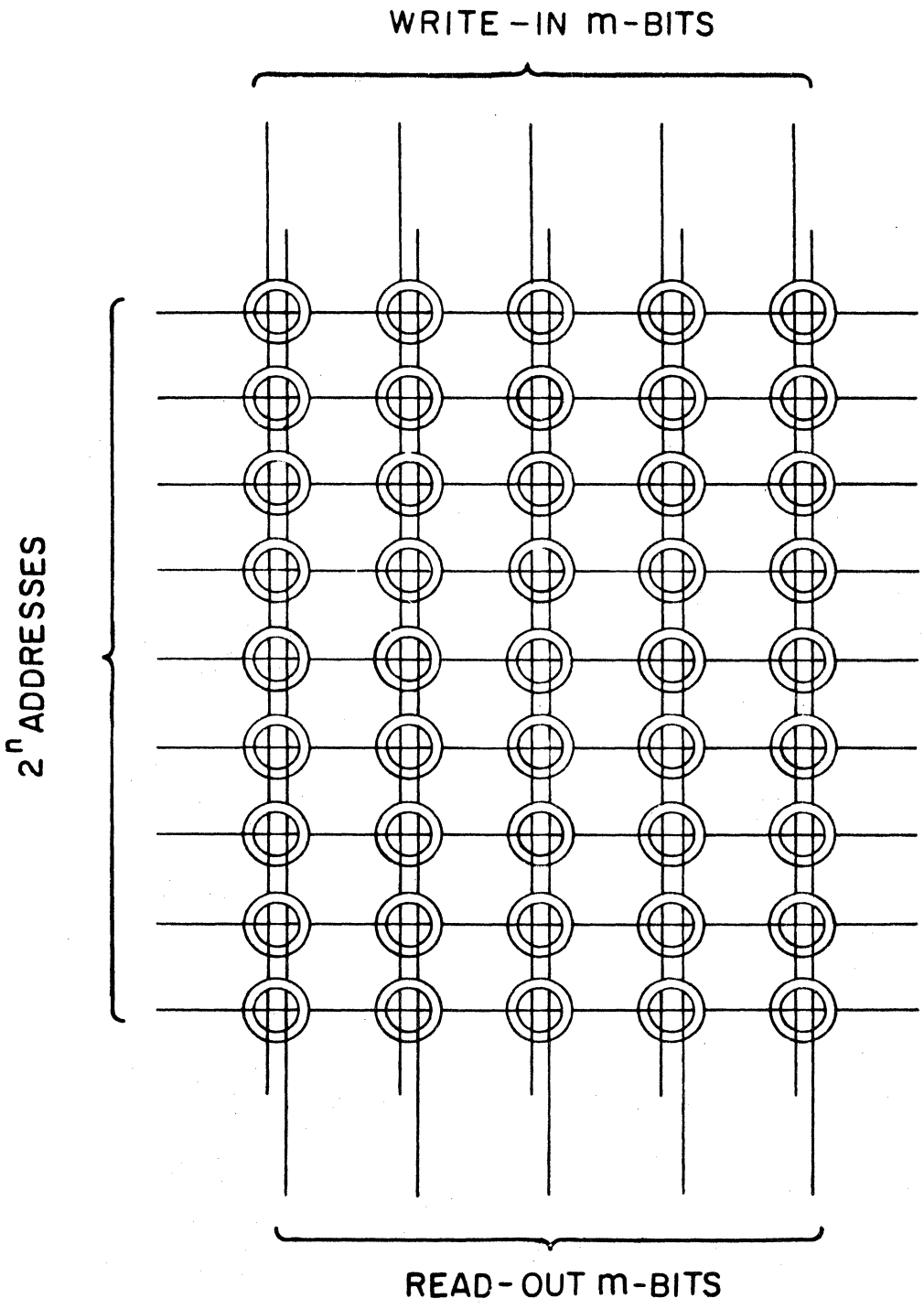
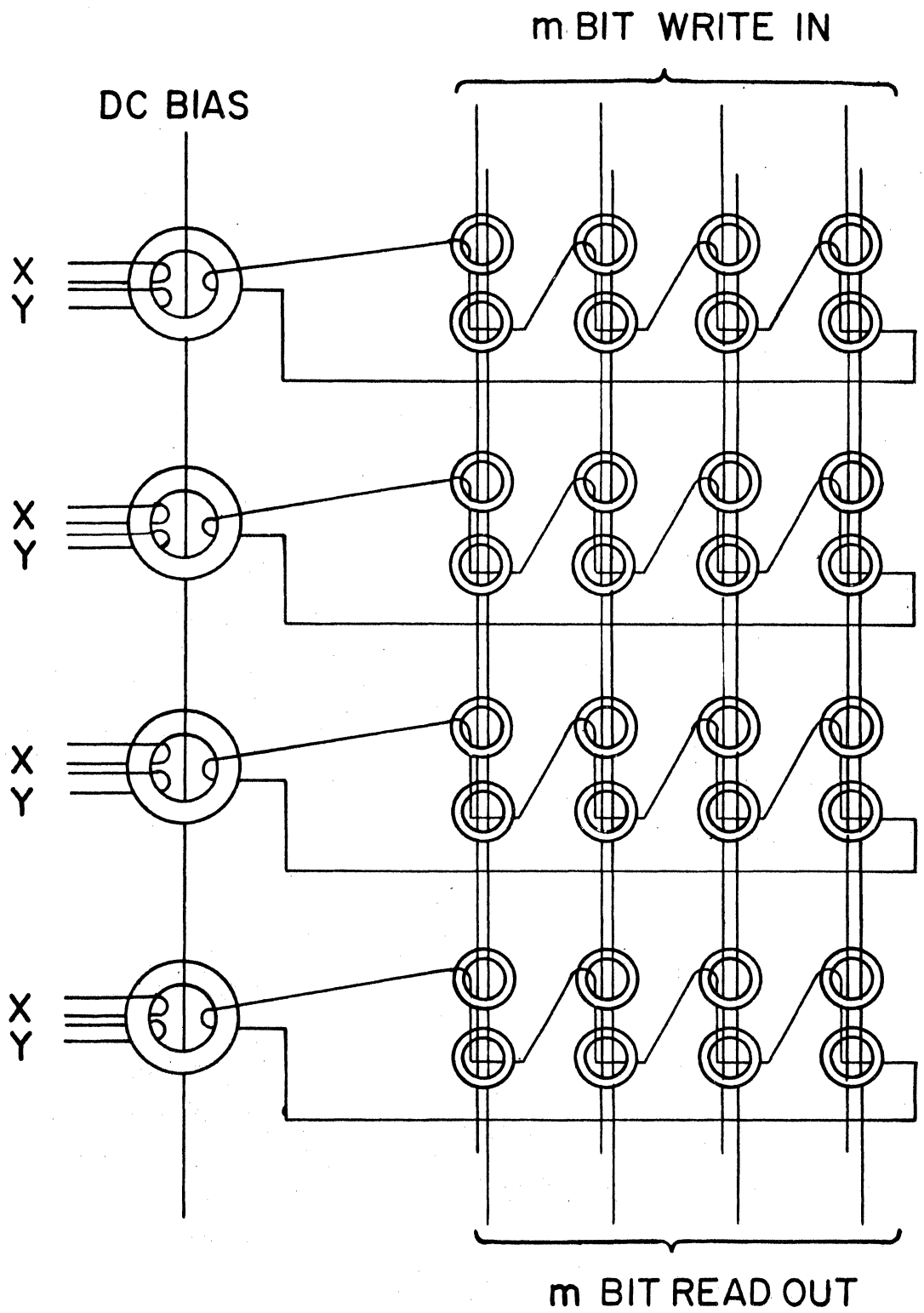


Fig. 9. Word-Organized Core Memory



10. Magnetic Switch Driven Word Organized Memory

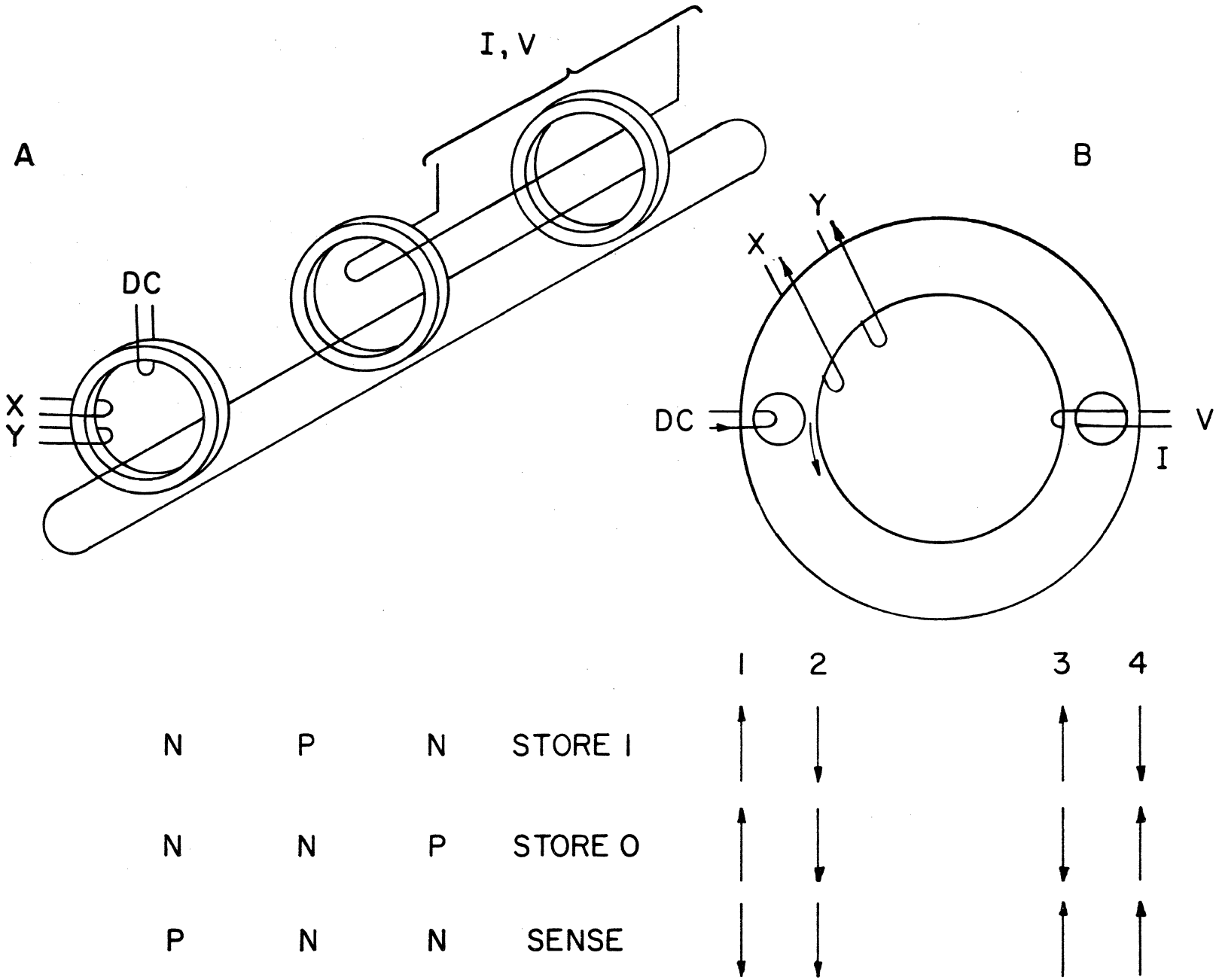


Fig. 11. Switch Drive of a Two-Core-Per-Bit Memory. Transfluxor Memory Element

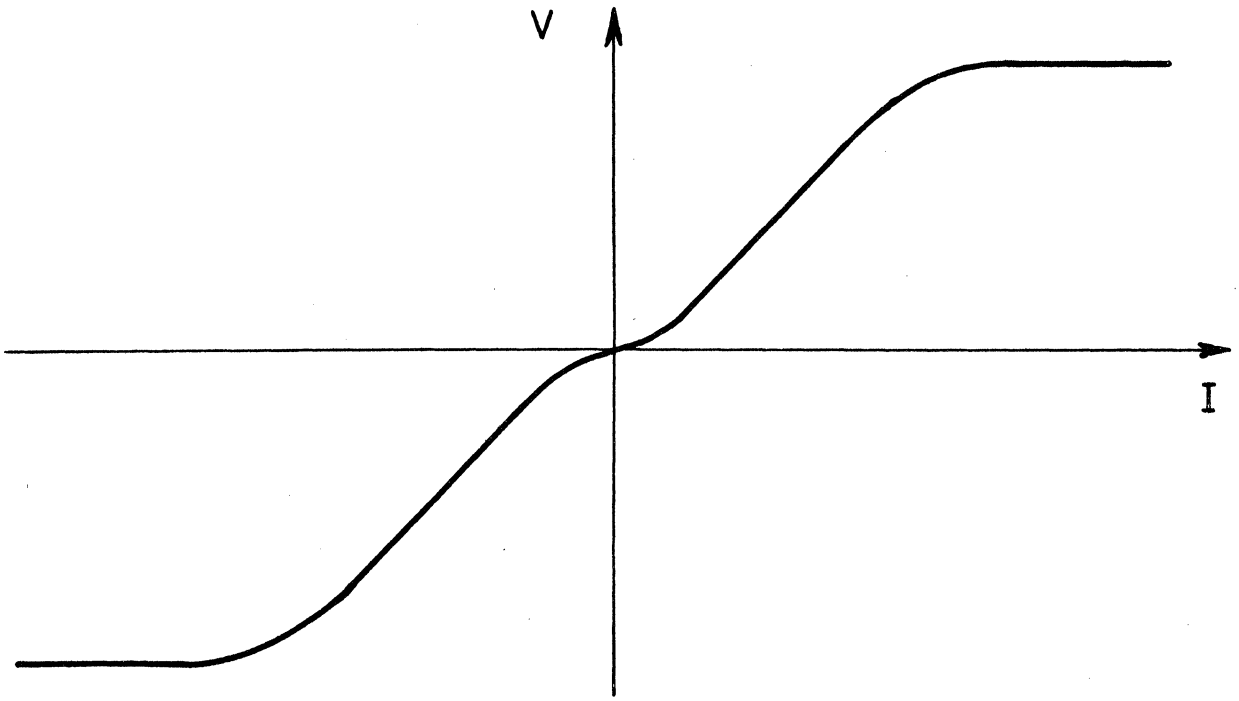


Fig. 12. Read-Out Voltage vs Digit Write Current for Two-Core-Per-Bit Memory Cell and Transfluxor Memory Element

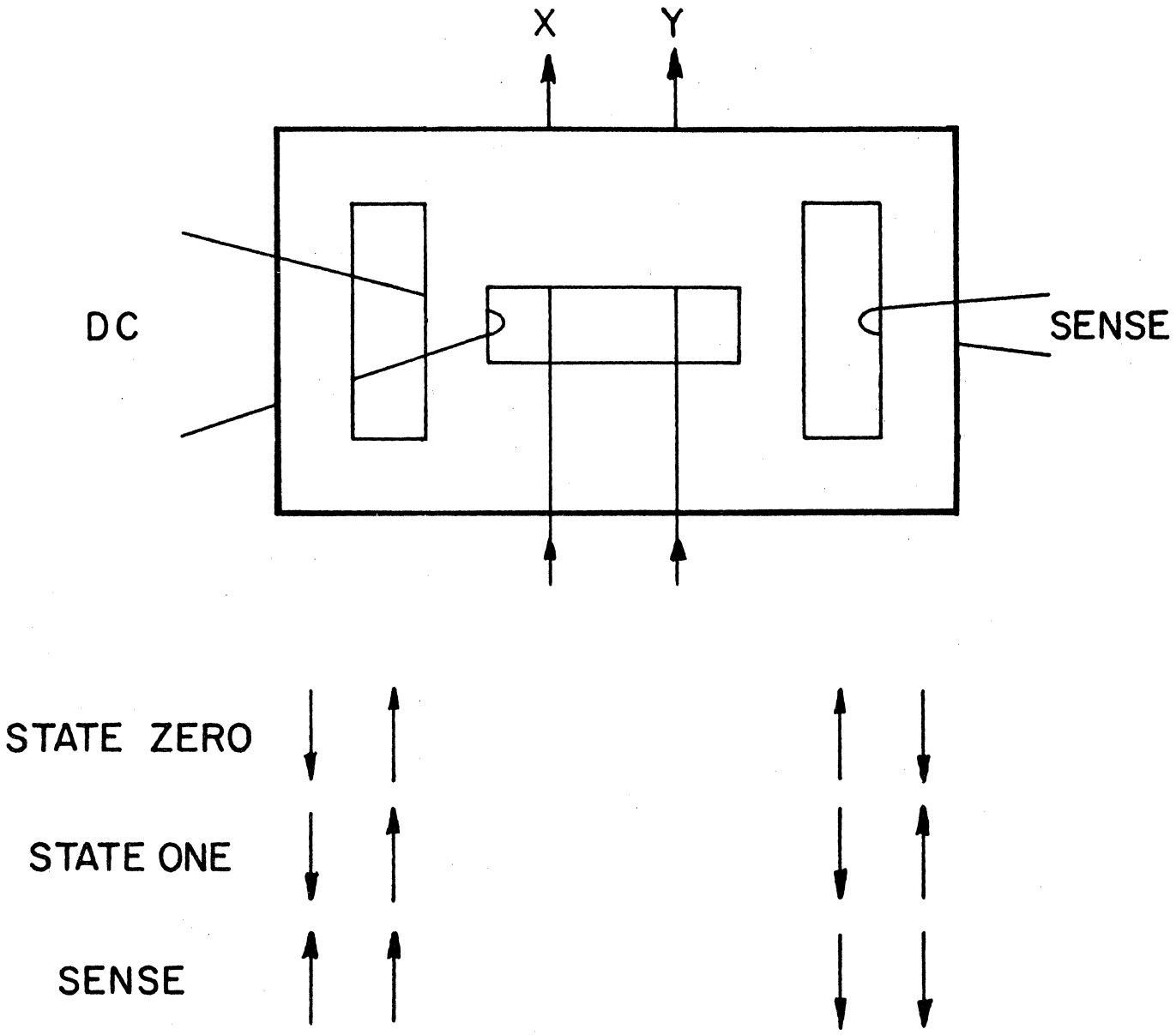
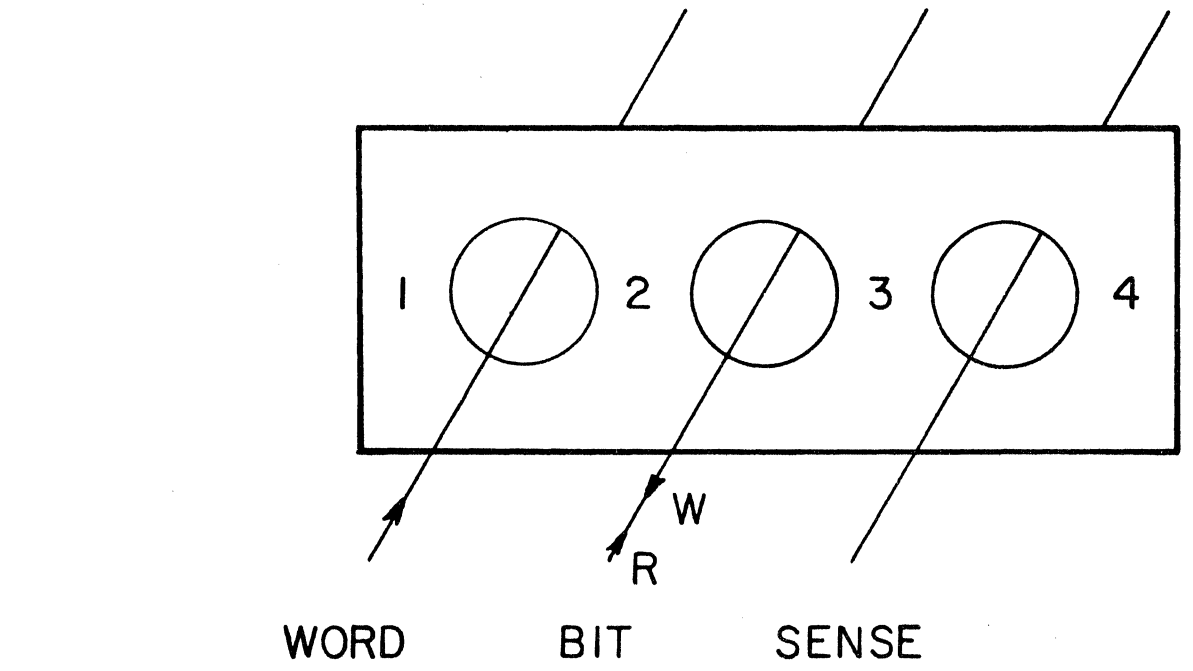


Fig. 13. Multipath Memory Core



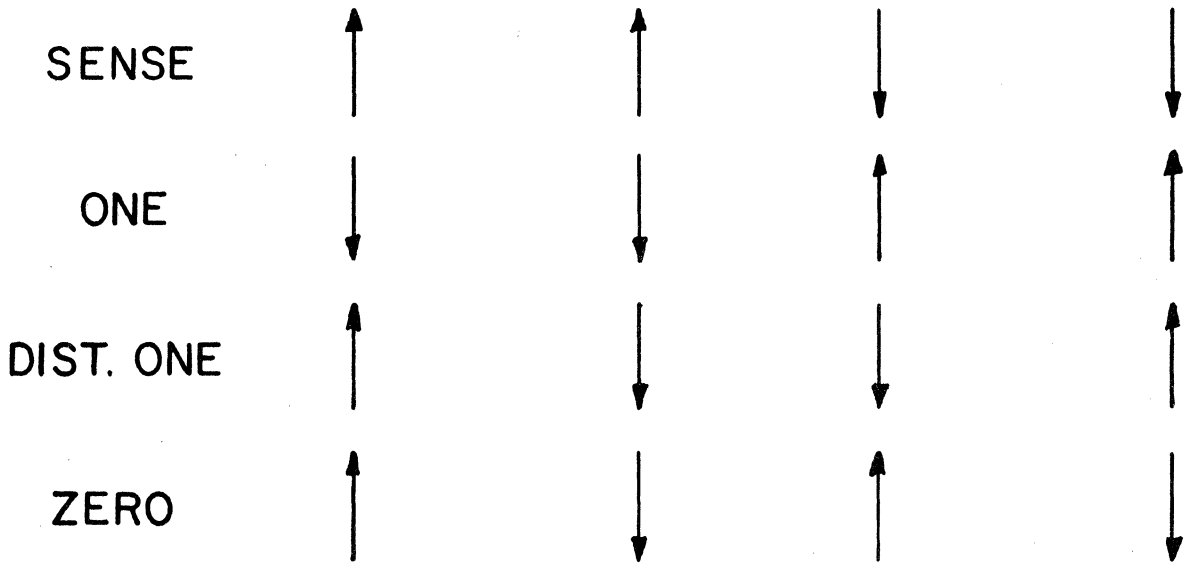


Fig. 14. Inhibit Flux Drive of Three Hole Memory Cell

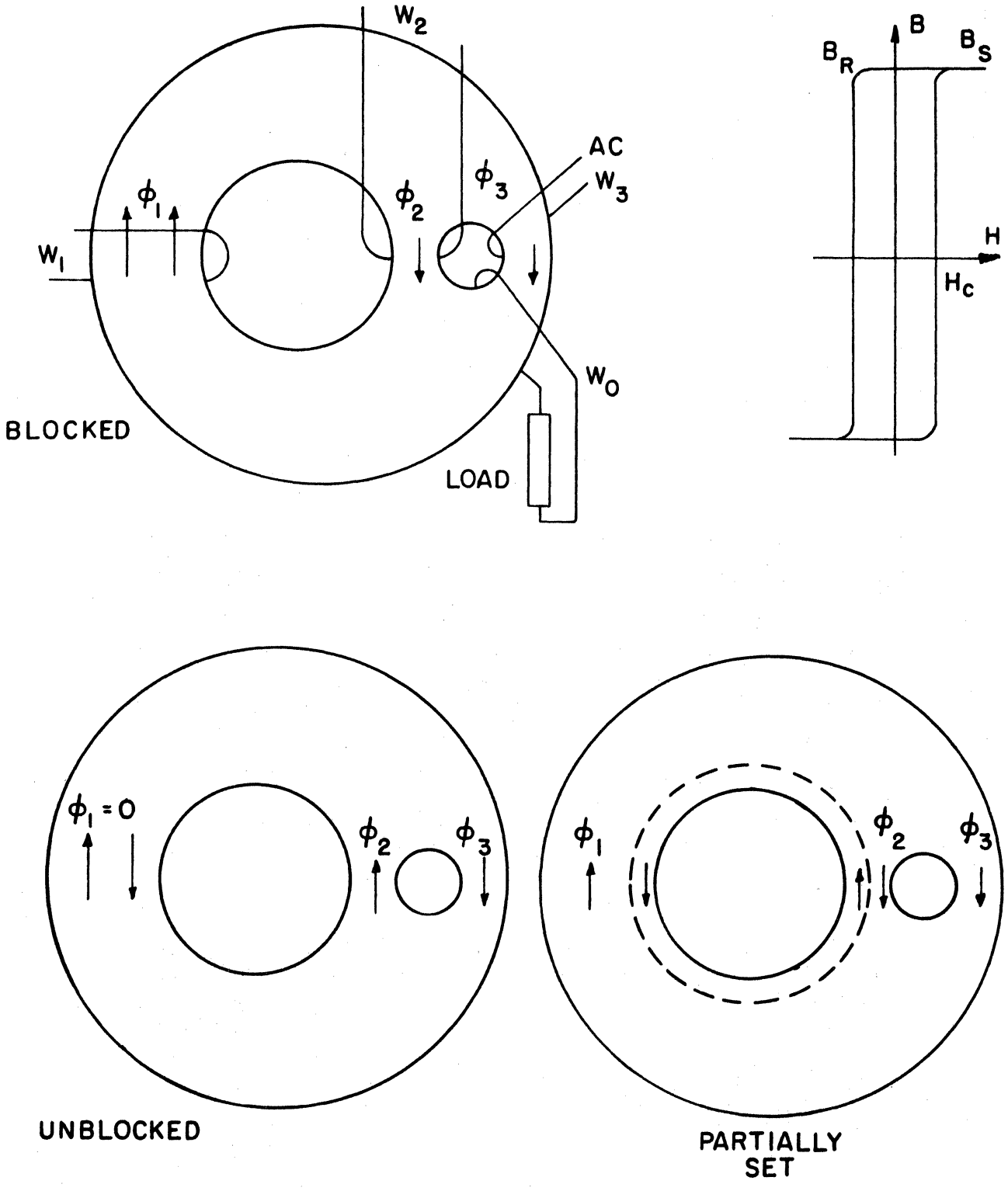


Fig. 15. Principle of Transfluxor

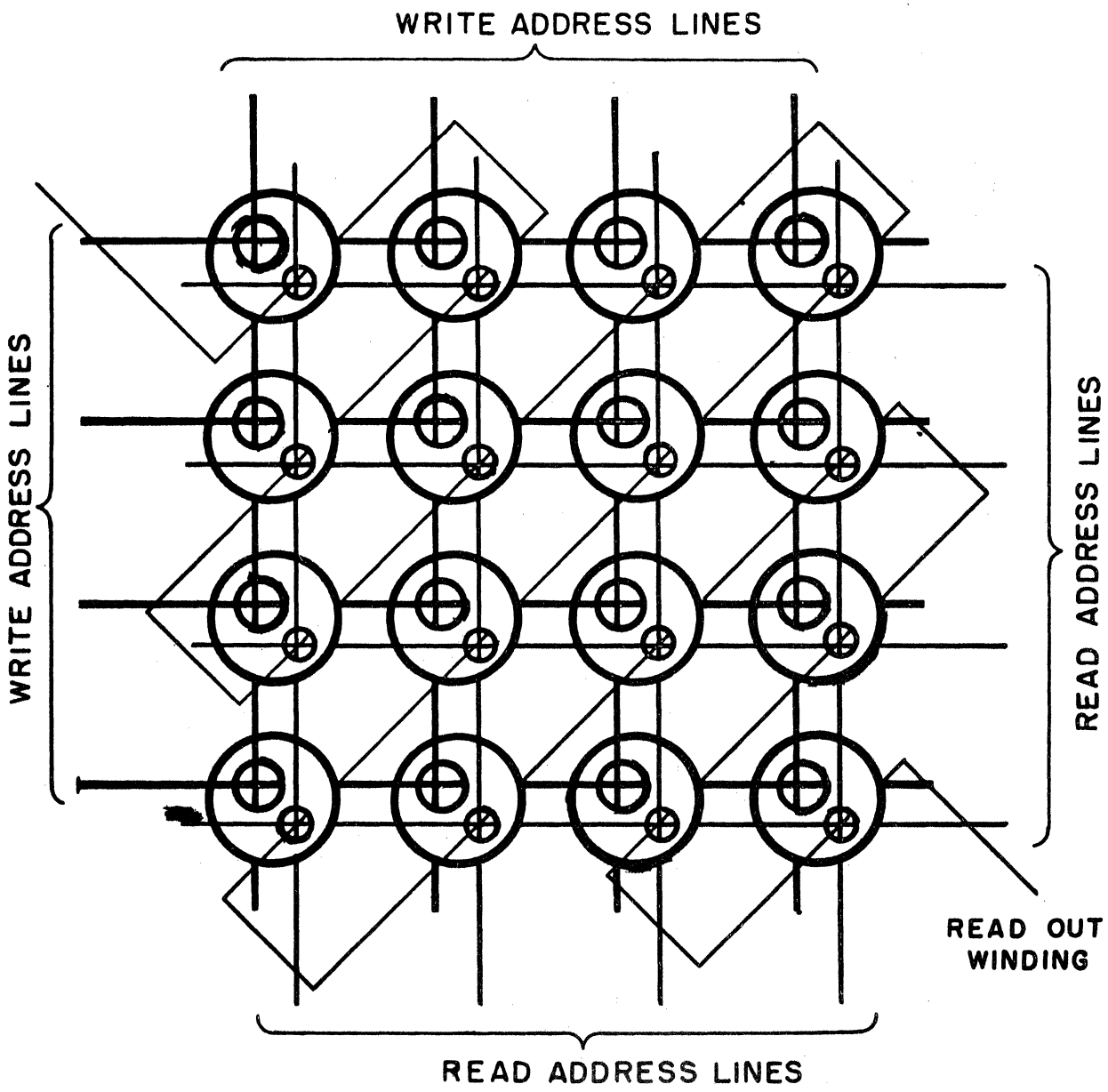


Fig. 16. Non-Destructive Read-Out Transfluxor Memory

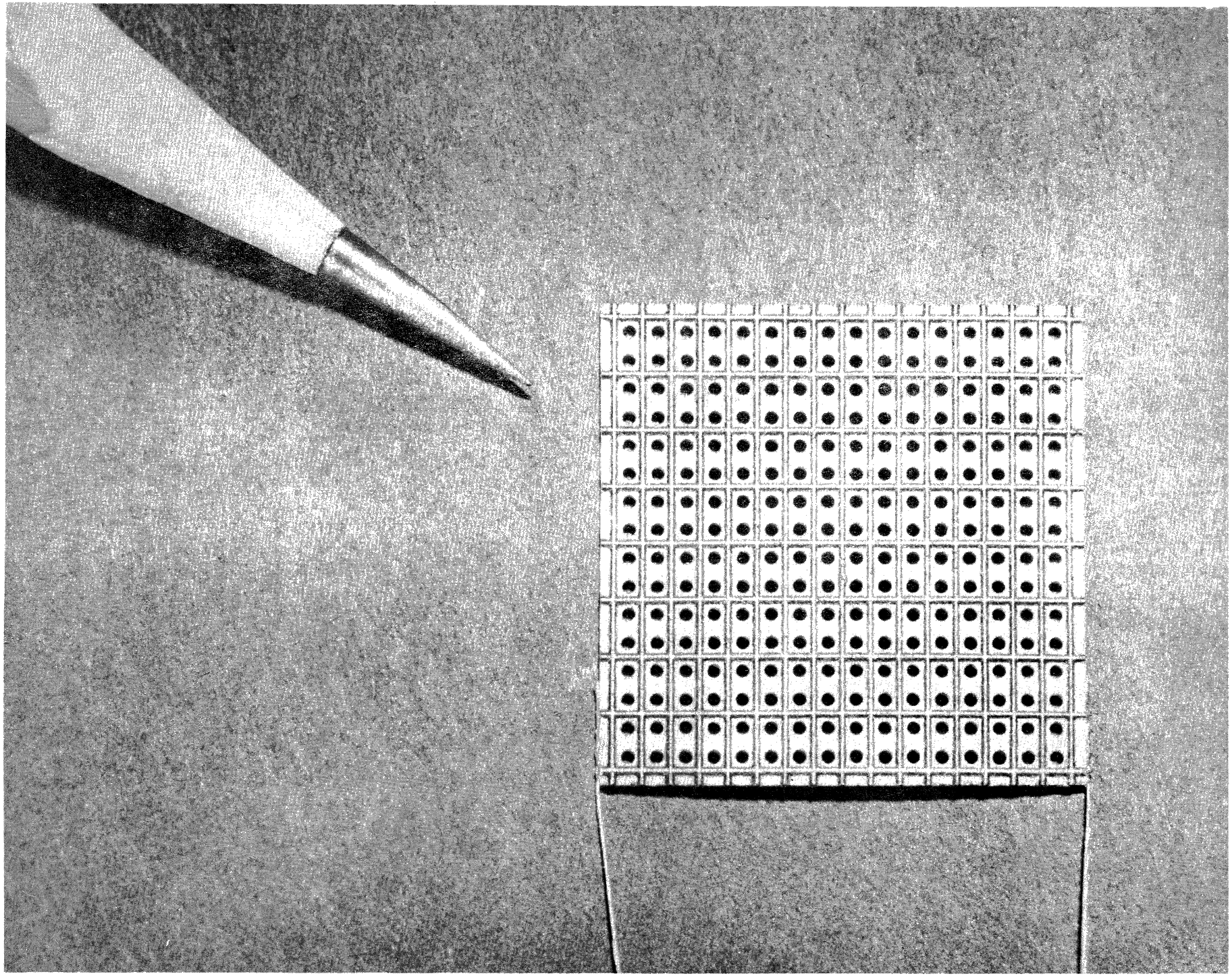


Fig. 17. Ferrite Apertured Plate

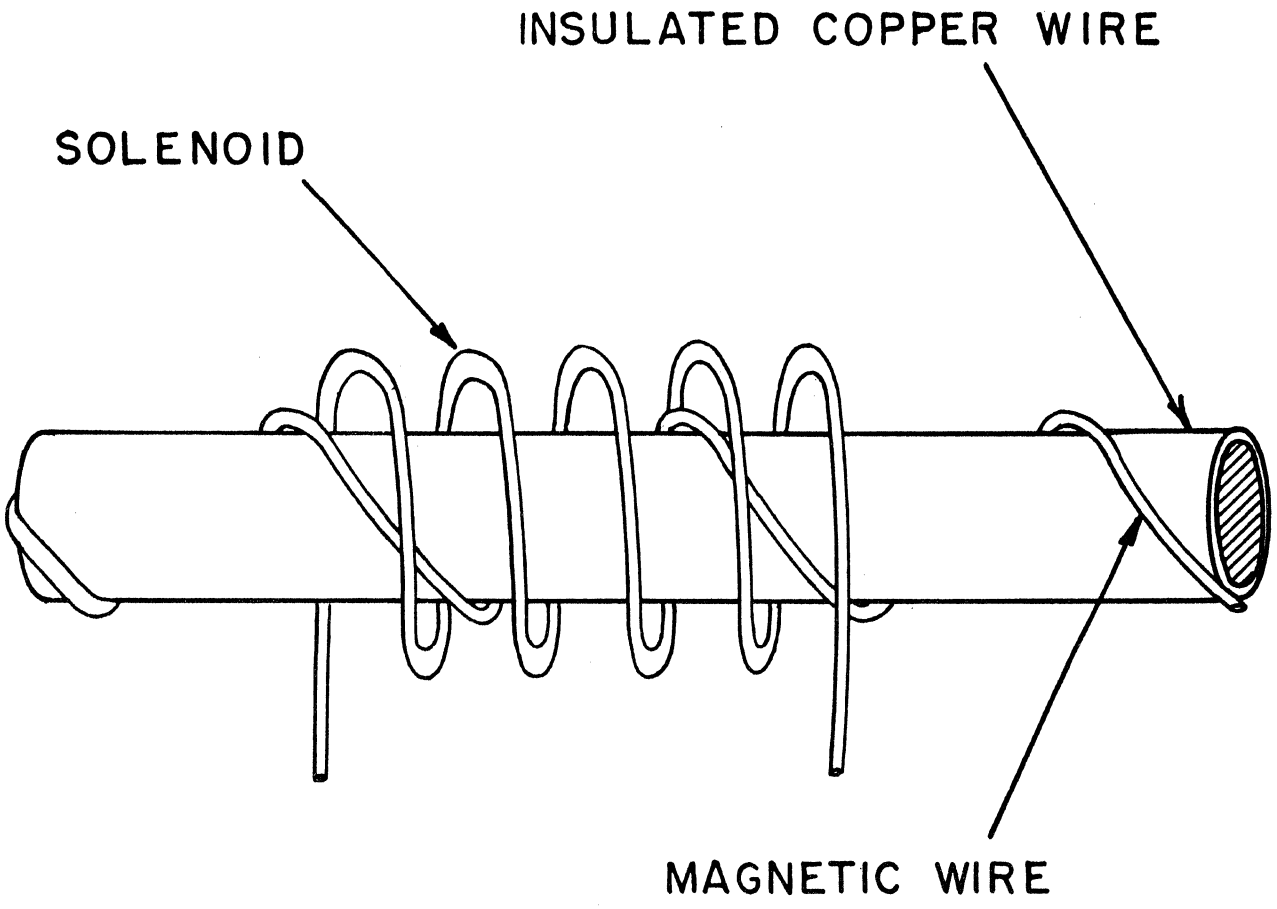


Fig. 18. Twistor

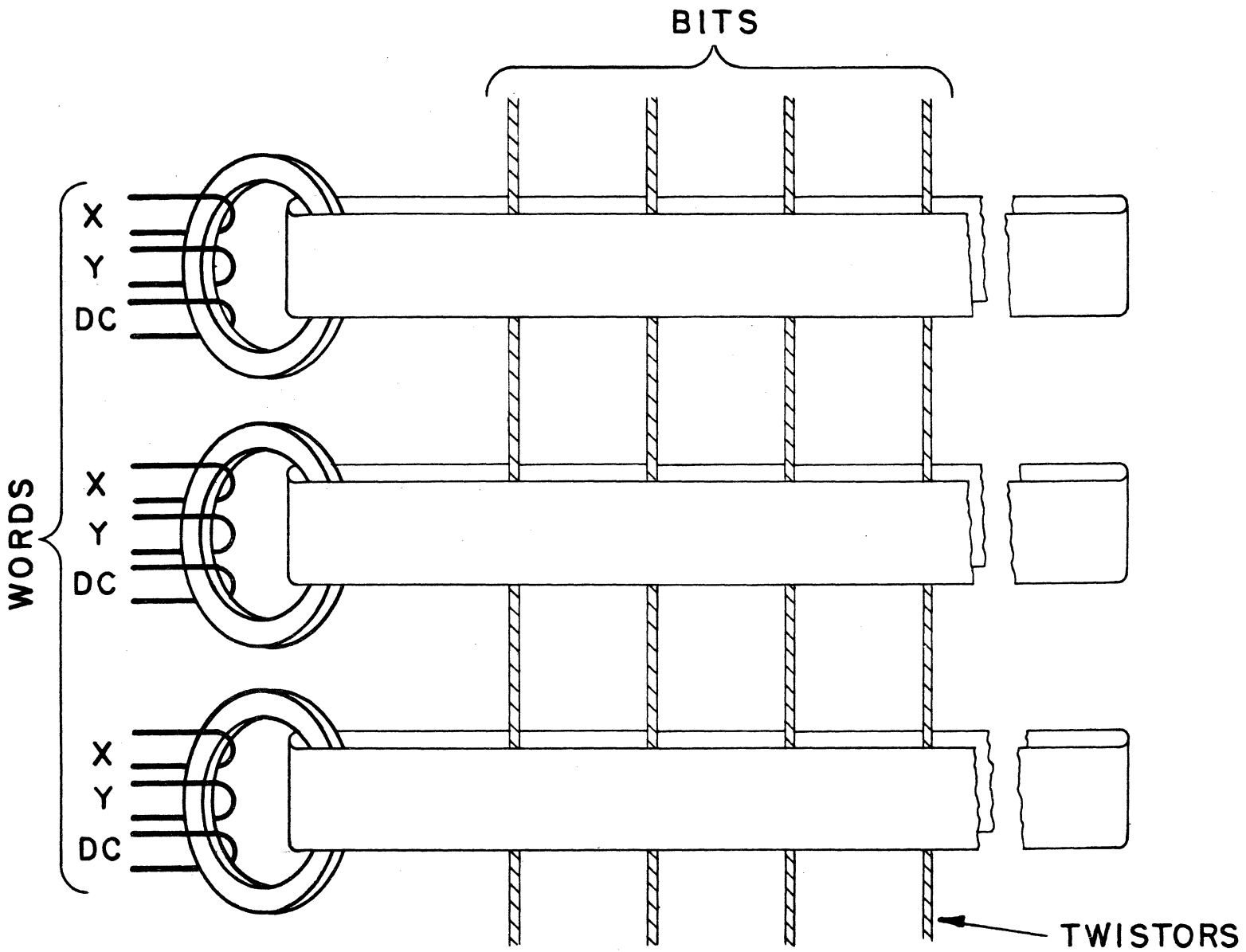


Fig. 19. Twistor Memory

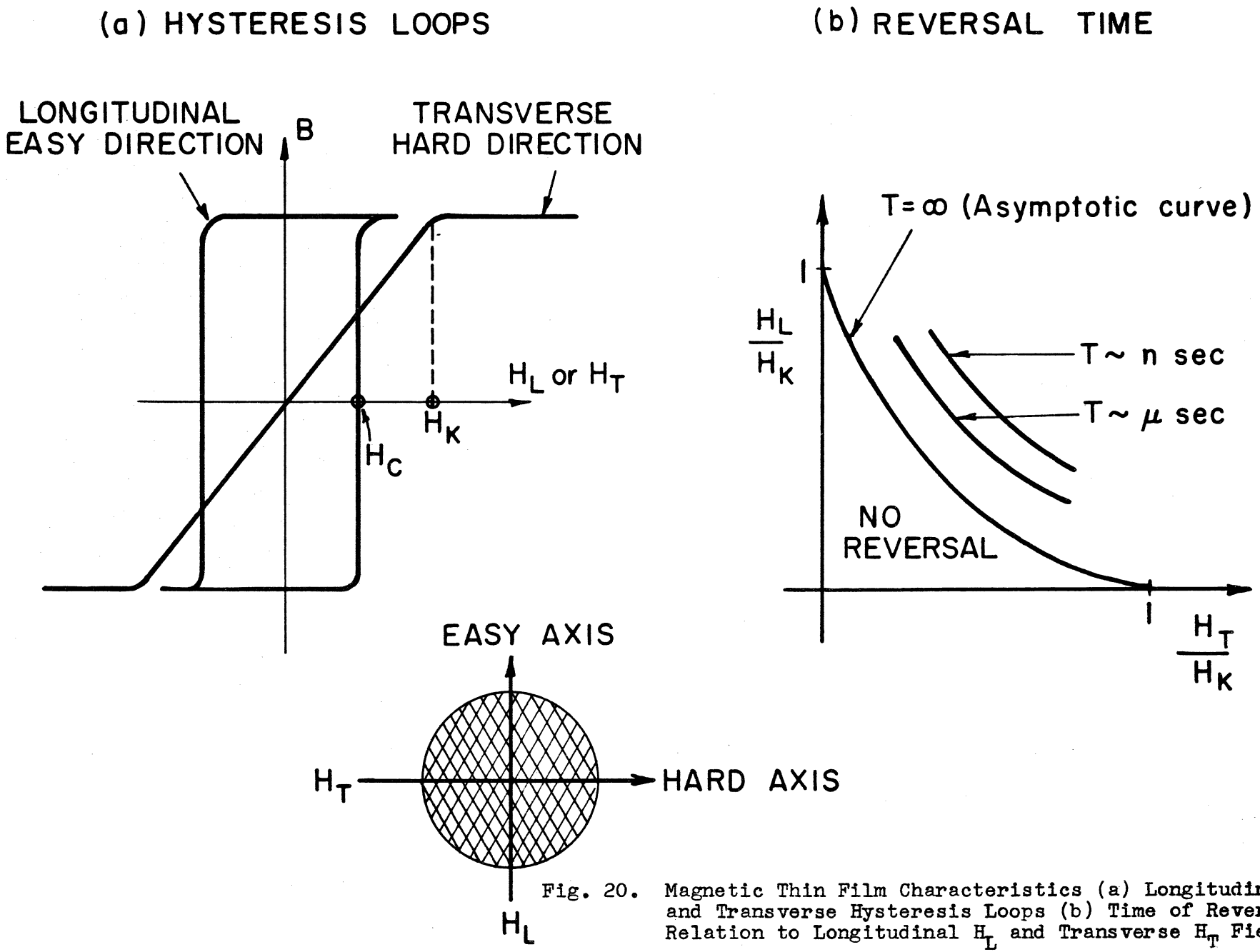


Fig. 20. Magnetic Thin Film Characteristics (a) Longitudinal and Transverse Hysteresis Loops (b) Time of Reversal Relation to Longitudinal H_L and Transverse H_T Fields

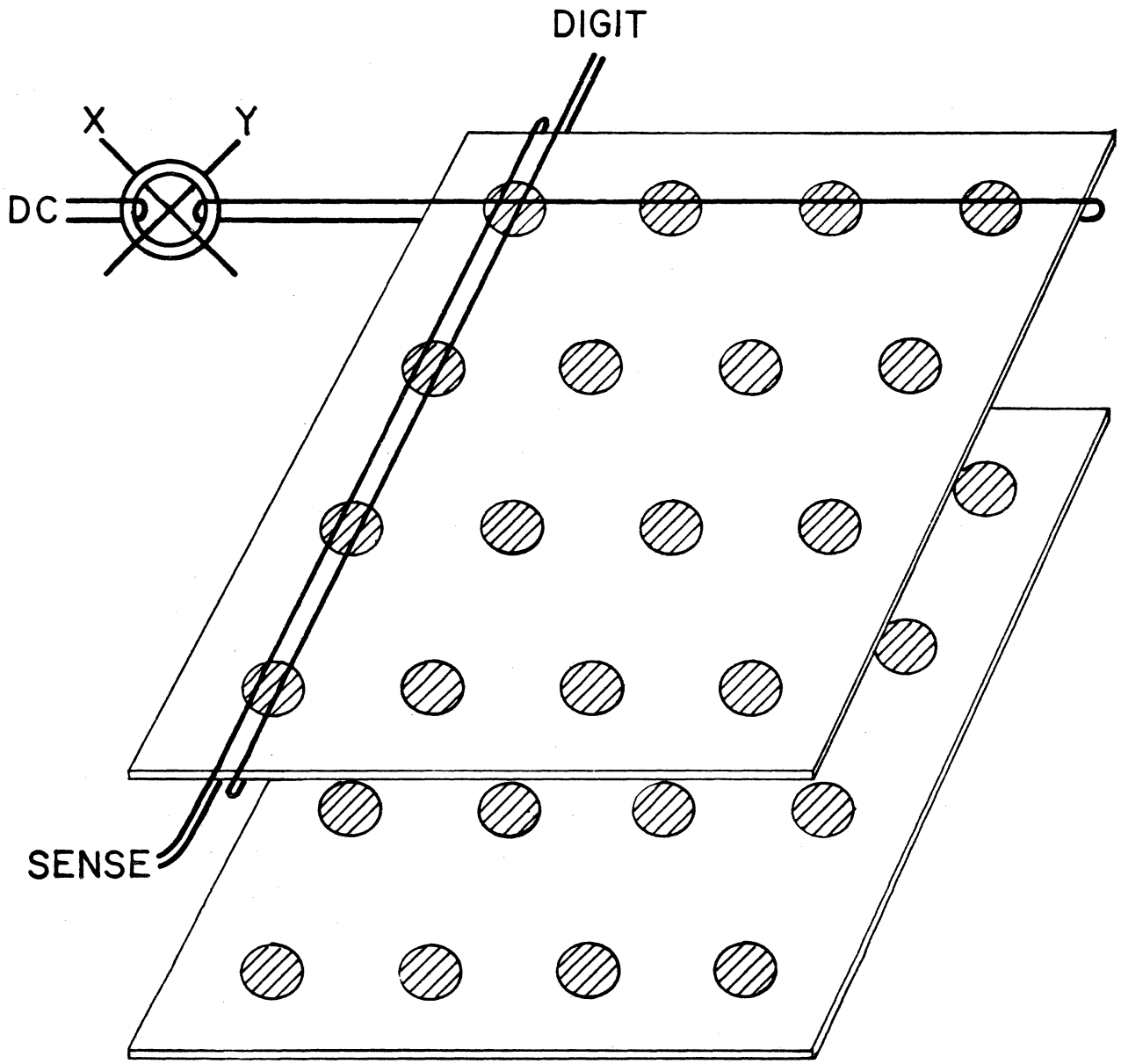


Fig. 21. Thin Film Dot Array Memory

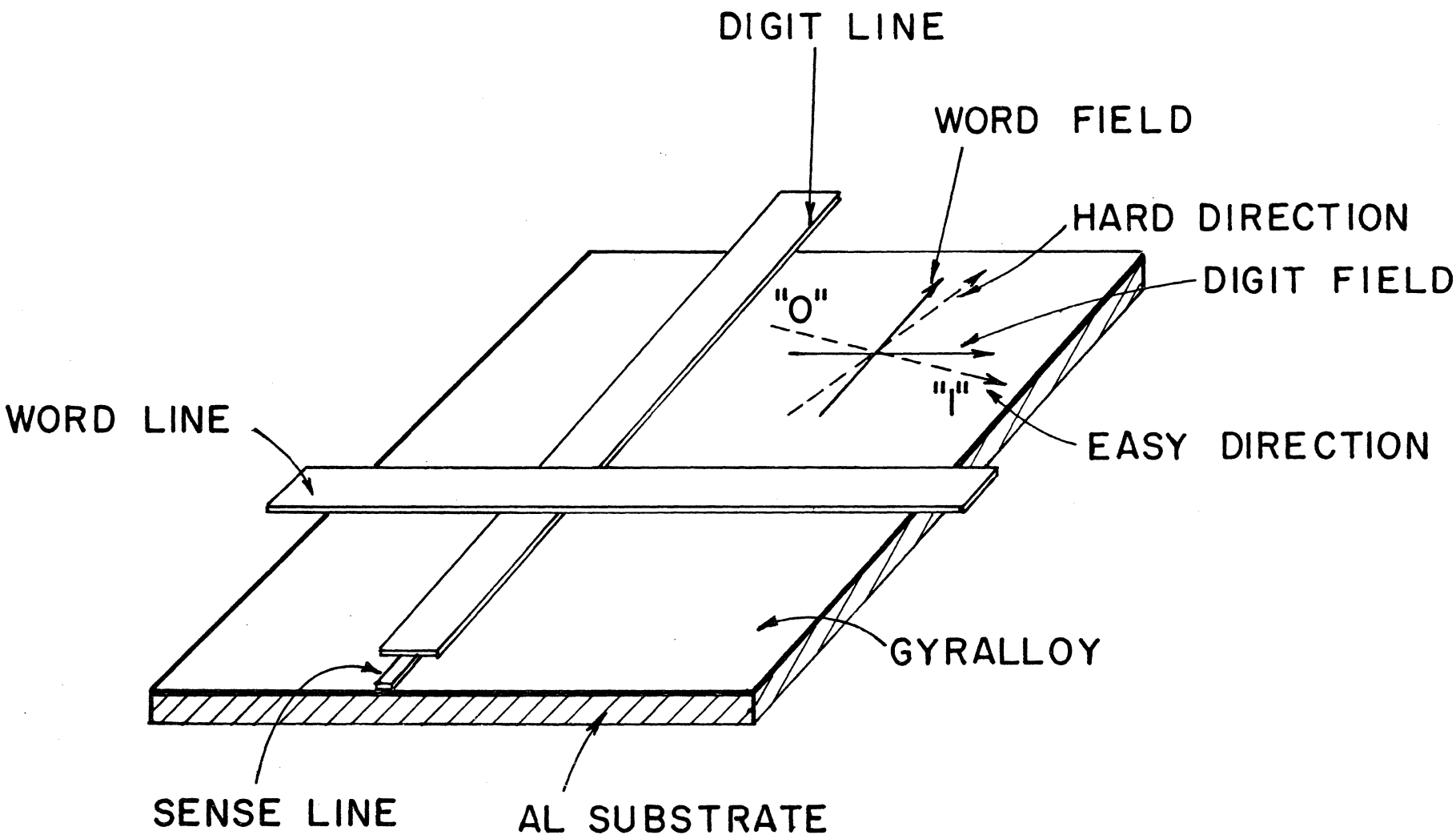


Fig. 22. Continuous Sheet Thin Film Magnetic Memory

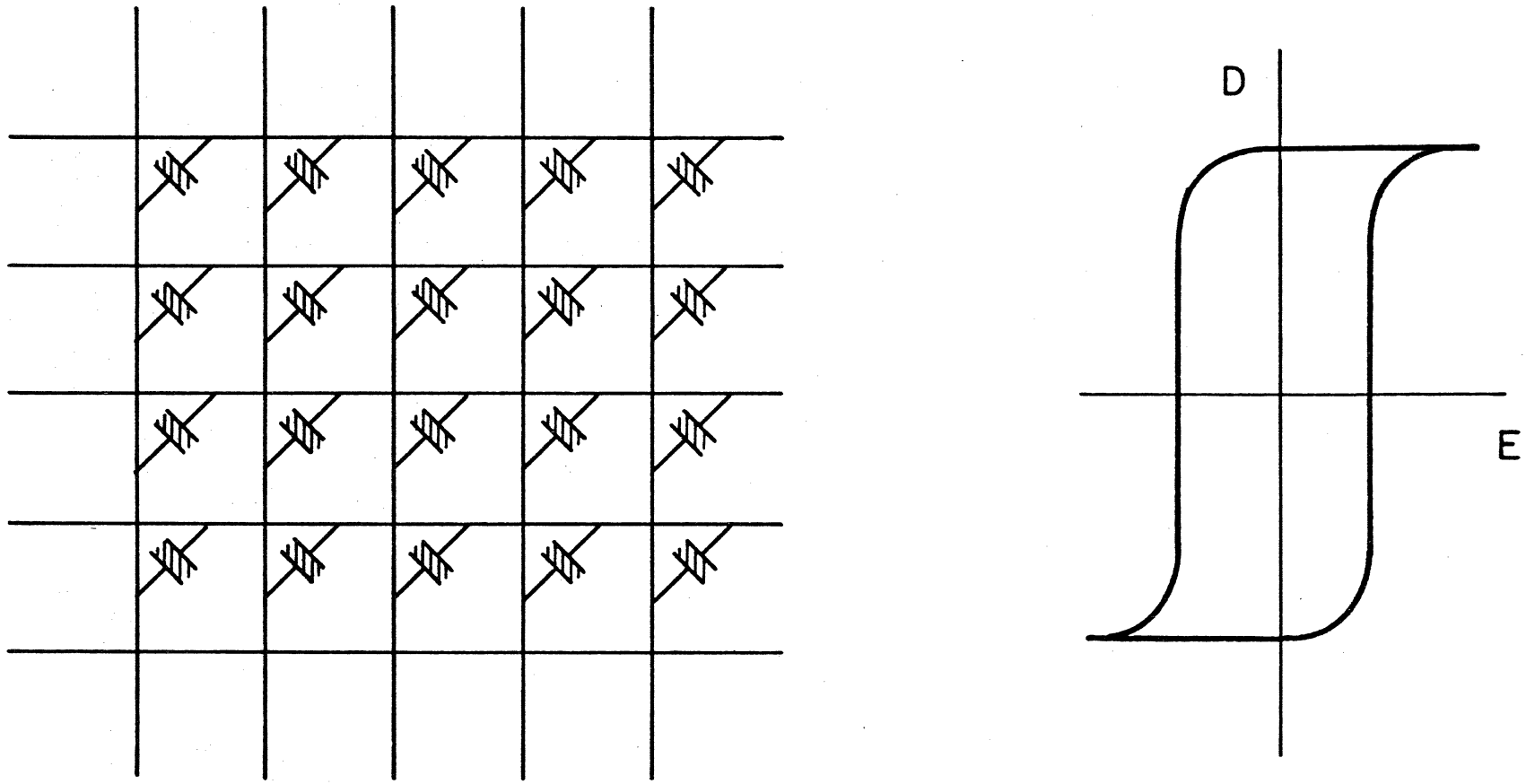


Fig. 23. Ferroelectric Memory Array and Hysteresis Loop

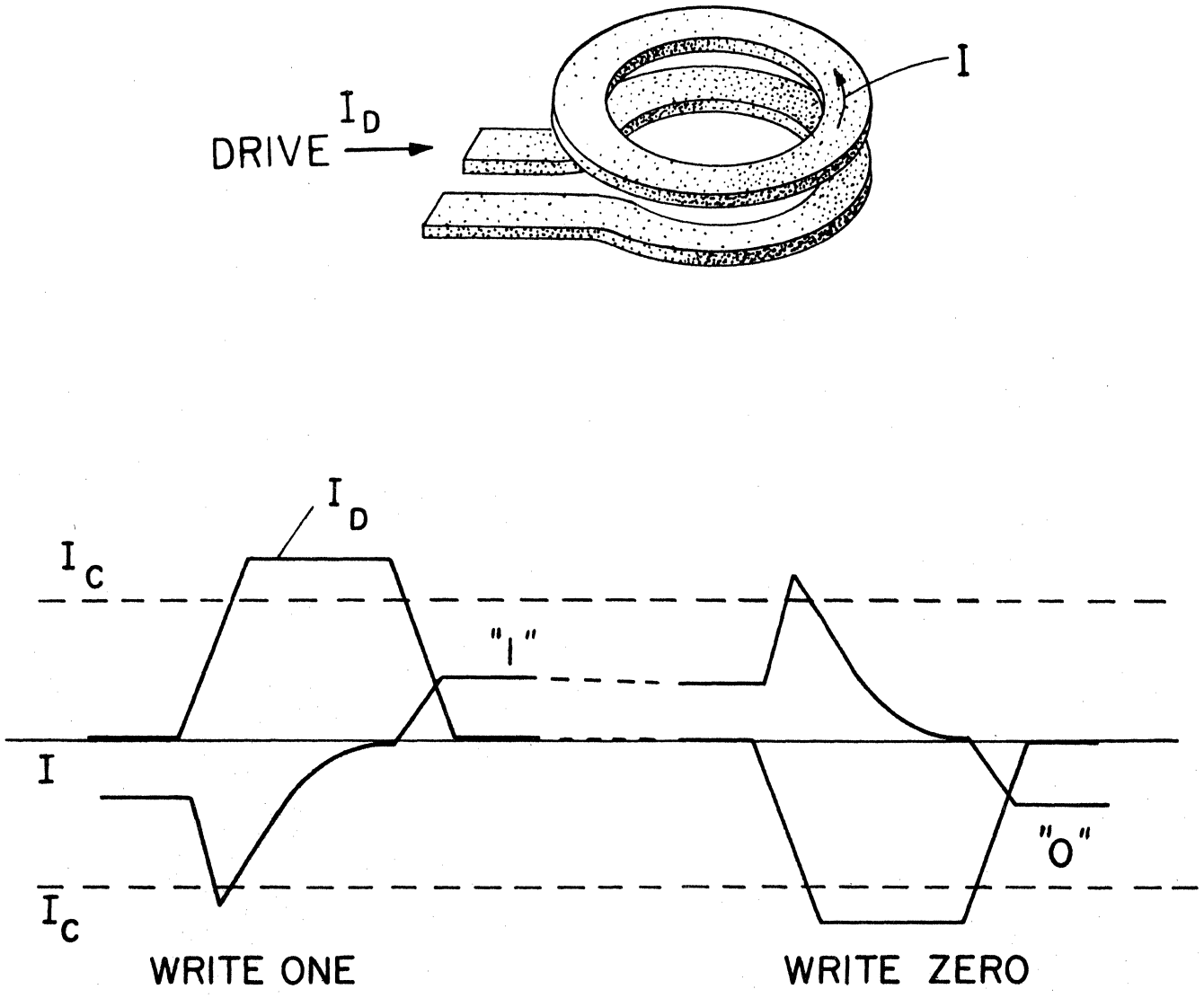


Fig. 24. Principle of Superconductive Persistent Current Storage Cell

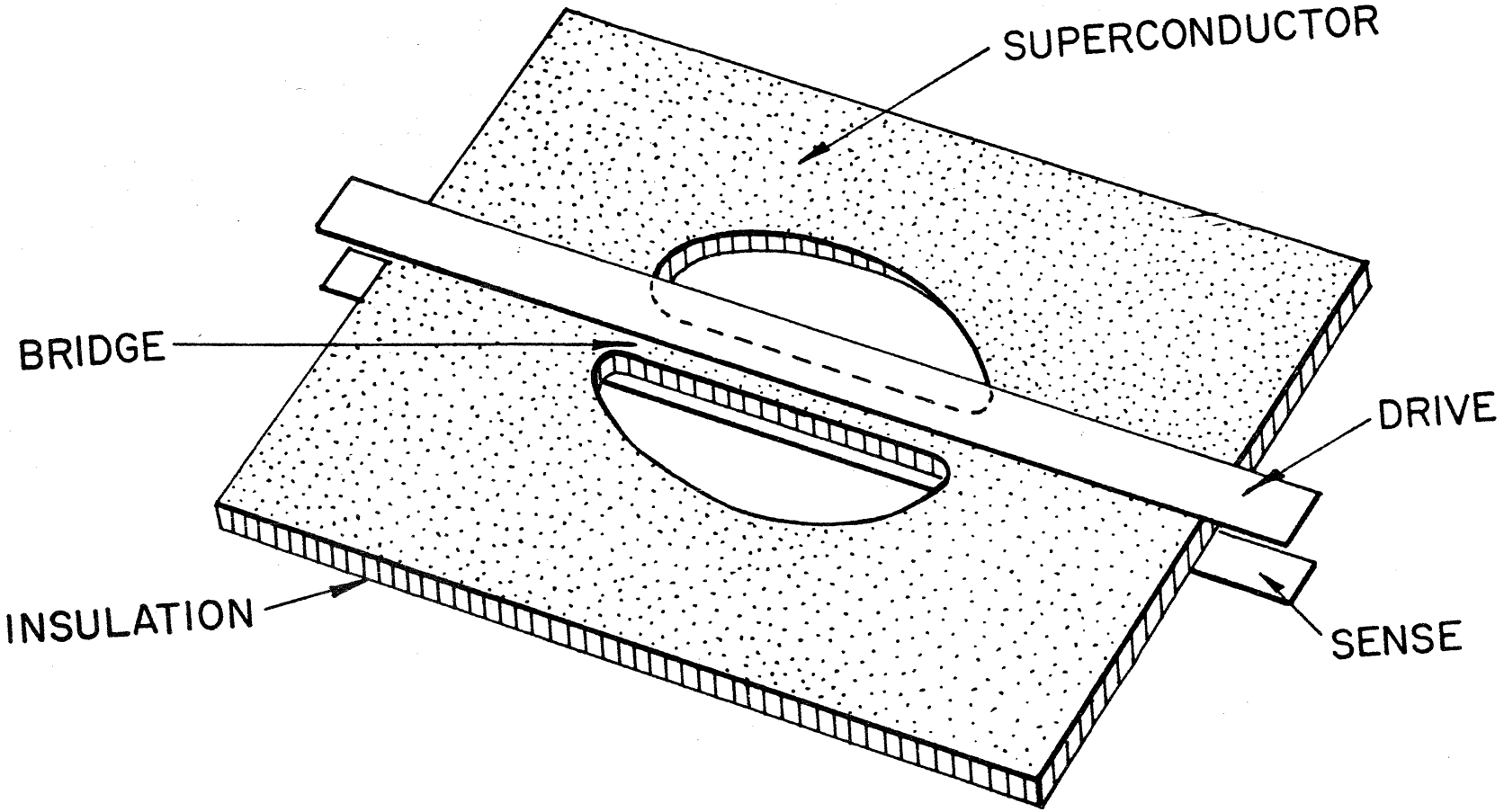


Fig. 25. Crowe Cell

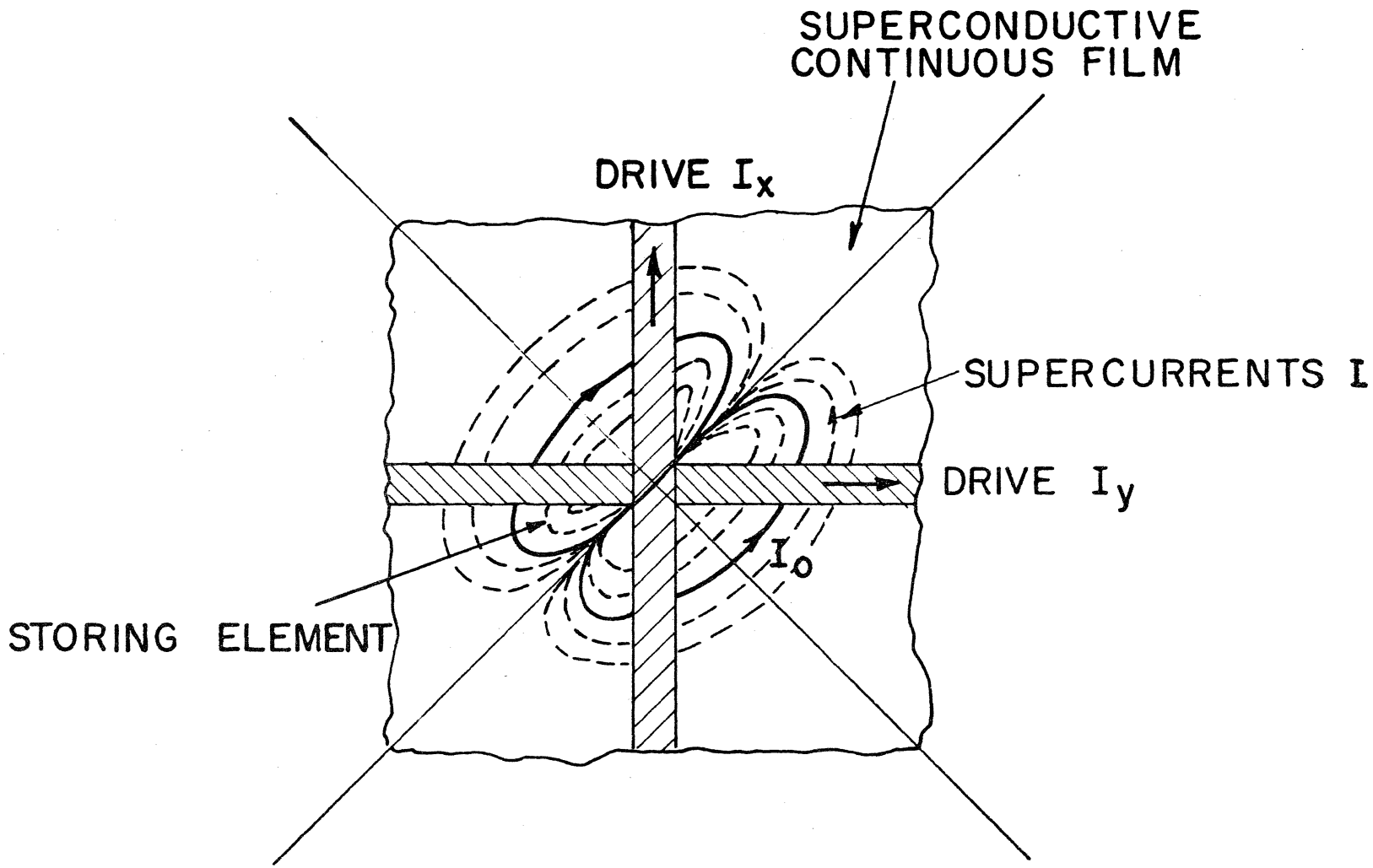


Fig. 26. Persistent Current Storage in Discrete Region of a Continuous Superconductive

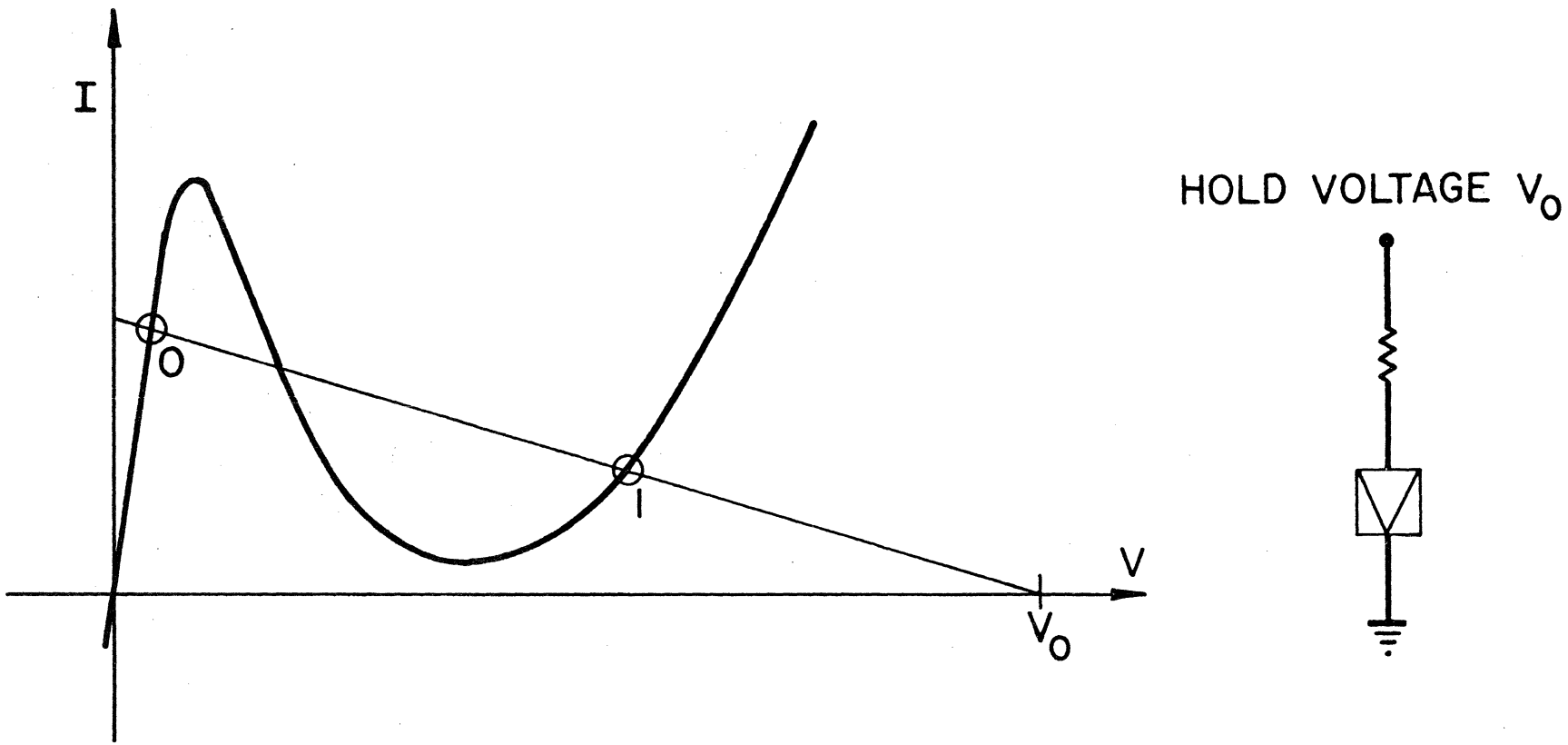


Fig. 27. Tunnel Diode Characteristic and Storage Element

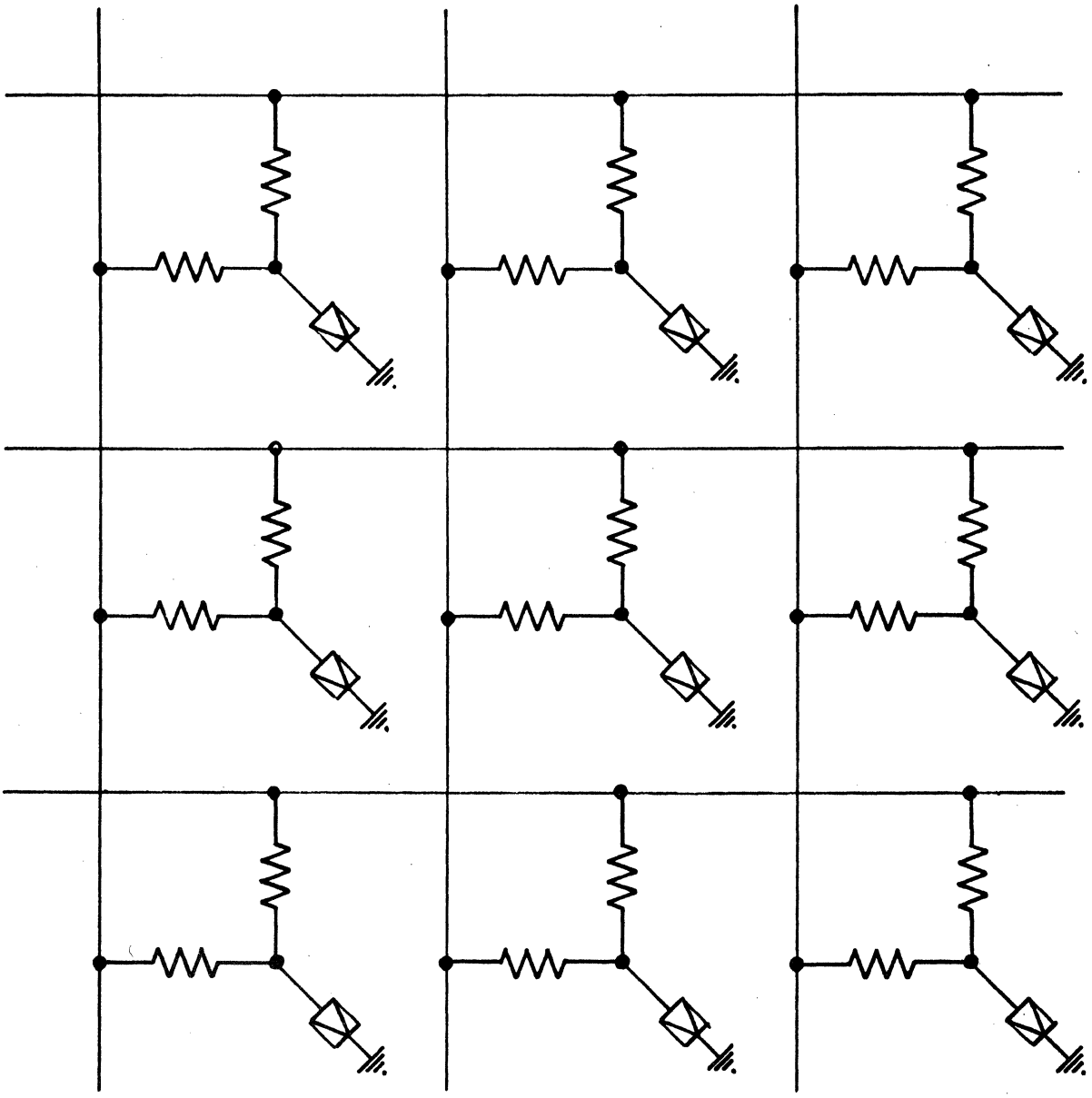


Fig. 28. Tunnel Diode Memory Array