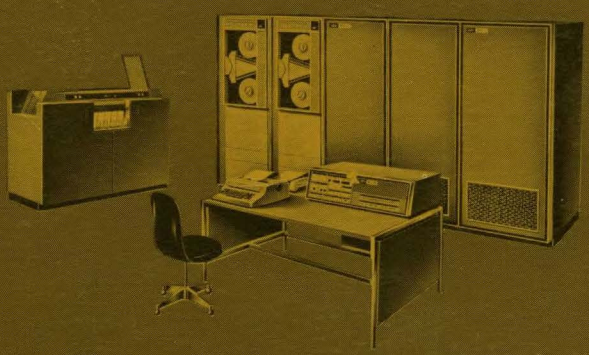
RAYTHEON 520 SYSTEM



RAYTHEON COMPUTER

RAYTHEON

RAYTHEON 520 SYSTEM

the new price-performance leader in scientific, engineering and data systems computing.

The Raytheon 520 System is an integrated, highly automated combination of modern high-speed hardware and state-of-the-art software. It is modular, and Raytheon Computer can design a system to fit your need and budget by selecting the appropriate standard units.

Raytheon has recognized that the day of the "stand-alone" computer is passing, and that customers must have a processor which can be the central element of an expandable automatic data collection and computing system. Sophisticated, high-speed internal operation, and expandable, high-throughput input-output are both essential to good system performance. A wide range of peripherals providing for use of all input-output media and for disk pack mass storage, as well as magnetic tape, are available as system building blocks.

Unusual skill in realtime system engineering is a Raytheon plus. Broad experience and capability in communications, radar, sonar, laser, and photographic data transmission and processing is brought to bear on commercial systems.

Data system implementation and cost are reduced by hardware oriented toward interface of the 520 System with analog computers, satellite telemetry, automatic test and checkout, teletypewriter networks and other data sources.

Software is the key to 520 System superiority. Programming ease and economy, use of an existing program library, speed of processing, and automation of system operation are all planned for your benefit. You may use advanced 520 FORTRAN or FLEXTRAN, Raytheon's advanced compiler-assembler. The use of existing program libraries with the 1620 Simulator or FORTRAN is possible with the Raytheon 520 System. Maximum system productivity and maximum use of programmer or operator labor can be realized when BOSS, the 520 System operating system, is used to control job processing and routine functions.

Raytheon invites you to learn more about its 520 System and to take advantage of the problem solving capability and support that Raytheon Computer will provide.

SUMMARY OF 520 SYSTEM CHARACTERISTICS

- Fully Parallel Machine Organization
- Twenty-four Data Bits plus One Parity Bit per Word
- 4096 Word Core Memory Modules — Each with Read/Write Electronics
- Two-Microsecond effective Memory Cycle Time
- Direct Addressing to 32,768 Words
- Optional 200 Nanosecond access NDRO BIAX Memory in Modules of 256 or 512 Words
- High-Speed Arithmetic Operation — e.g. One Microsecond ADD and Three Microsecond 10 x 24 MULTIPLY
- 45 One Microsecond Commands
- Two Instructions per Word — Allows Efficient Utilization of Memory
- Seven Addressable Hardware Registers
- Efficient Register-to-Register Instructions — Reduces Time Consuming Memory References
- Most Shifting and Branching Capability in Price Class
- Register Layout Optimized for Floating Point Operations — Allows Intermixed Use of 16, 24 or 39-bit Mantissa Formats
- Sixty-four wired-in Commands, each with many Variations
- Advanced Four-Level Interrupt System included in Basic Processor
- True I/O Bus Structure
- Directly Address up to 512 I/O Devices
- Four 24-bit I/O Channels
- Each I/O Channel may be Time-Multiplexed among many Devices
- I/O Devices Individually Buffered for Simultaneous I/O and Compute
- Wide Range of Peripheral Equipment available
- Direct Memory Access from I/O Devices
- Low-cost Real-Time Data System Interface — Allows Easy System Expansion or Modification
- Advanced Software

  BOSS, the 520 Operating System
  FLEXTRAN Compiler-Assembler
  520 FORTRAN II and IV
  1620 Simulator

520 APPLICATIONS

- Aerial survey data reductions
- Antenna and telescope control (tracking)
- Automatic checkout systems
- Circuit analysis
- Command and control (DOD)
- Communication switching systems
- Component test
- Civil engineering calculation
- Data acquisition systems
- Data reduction
- Digital simulation
- Flight test data processing
- Hybrid computing
- Inventory control
- Lab and process instrumentation
- Launch control and ground guidance
- Map making
- Medical monitoring (hospital)
- Medical research
- Meteorology
- Missile design and analysis
- Mission control
- Nuclear Reaction (monitoring and control)
- Nuclear research
- Oceanography
- Photogrammetry
- Physics (experimental data reduction)
- Radar data reduction
- Reactor design and simulation
- Satellite checkout
- Seismic data reduction
- Statistical analysis
- Structural data reduction (vibration, stress/strain)
- Telemetry (Command and Control)
- Telemetry (flight test, data gathering and reduction)
- Trajectory computations
- Typesetting
- Wind tunnel vibration data analysis reduction

RAYTHEON 520 SYSTEM — THE CENTRAL PROCESSOR

The Raytheon 520 System offers a series of exclusive individual features which provide the user with computing and programming capabilities generally found only in systems costing many times the price of the 520.

The Raytheon 520 System is a parallel digital computer, using a data word of 24-bits plus a parity bit. Forty-five of its 64 basic instructions execute in one microsecond. Effective main memory cycle time is 2 microseconds and a Raytheon-manufactured non-destructive readout memory (BIAX) with an access time of 200 nanoseconds is available as an option.

Basic main memory storage capacity is 4096 words, expandable to 32,768 words. The optional NDRO BIAX memory can be employed in modules of 256 or 512 words.

Use of advanced circuitry, e.g., high speed adder with 5 nanosecond per bit transfer times, allows ultrafast, variable length multiply and divide. Simple multiply executes in 0.5 microsecond plus 0.25 microsecond per bit or eight, twelve and 24 bits in 2.5, 3.5 and 6.5 microseconds, respectively. Full word divide executes in 12.5 microseconds.

SEVEN PROGRAMMABLE REGISTERS

Seven hardware arithmetic registers and an appropriate complement of efficient register-to-register commands are available to the programmer. Since the Raytheon 520 System register-to-register instructions execute in a fraction of the time required for typical computer memory load and store times, the use of multiple registers results in faster throughput rates. For instance, many types of problems require temporary holding of intermediate results. If held in a register, these intermediate answers require no memory access time. Each register may serve as an accumulator or as an index register. As a result, the implementation of exceptionally fast subroutines and highly efficient interpretive and compiler languages may readily be achieved.

RAYTHEON 520 REGISTERS

	Register Name	Use	
Programmable Registers	A	Arithmetic Register	24 bit
	B	Arithmetic Register	
	C	Arithmetic Register	
	D	Arithmetic Register and Command Interpretation Register	
	L	Command Location Counter, General Address Register or Index Register	15 bit
	P	Instruction Location Counter	
	N	Repeat Count Register or Exponent Register	8 bit
	Q	Phantom Register (source of zeros or ones)	
	E	Instruction-Pair Register (not addressable)	
	Carry Toggles	Indicate carry from bit positions 0, 1, & 9	
	Program Flags	6 1-bit registers	
	Parity Toggle	Indicates parity of the last memory access operation	

CONVENIENT DATA DISPLAY

The contents of any arithmetic register or core memory cell may be displayed or changed without disturbing the processing unit. An automatic address halt mode causes the computer to stop when a specified memory location is addressed. Marginal checking voltages are supplied on each power supply. These features provide powerful program debugging and maintenance aids. Six addressable program flags (one-bit registers) and six sense switches are provided for convenience.

ADVANCED MULTI-LEVEL INTERRUPT

An advanced four-level interrupt system is included in the basic system, and is based on a free-running scanner (similar to large scale computer systems). The scanner sequentially tests each channel at a one-megacycle rate. When an interrupt signal is found, the scanner is locked on the requesting channel and the program transferred to one of four fixed positions in memory. Three modes of operation are available and under program control:

(1) Automatic interrupt with program assignable priority levels,
(2) Automatic interrupt with all channels having equal priority levels or
(3) Programmed interrupt.

Programmed interrupt is obtained by manipulating a mask register to inhibit the automatic mode on one or more channels. Input levels to the mask register may be directly tested under program control. The scanner is released under program control to restart from any desired channel, e.g., from channel one in the automatic priority interrupt mode. Automatic and programmed interrupt modes may be intermixed.

The basic interrupt system may be expanded in increments of four levels to sixty-four levels of automatic priority interrupt with an optional system which develops a unique 15-bit address for each priority level. In addition, automatic program jumps for I/O faults allow unique direct servicing for each I/O device. The interrupt features allow exceptionally efficient management of a complex system.

SUPERIOR DATA TESTING AND CONTROL CAPABILITY

More data testing and control capability is provided in the Raytheon 520 System than is offered on any other commercially available computer. This capability includes direct testing for zero *or* non-zero on: (1) the sign, exponent, fraction, magnitude, or logical (entire word) fields in any register; (2) bits 0, 1, 6, 7, 8, 9, 10, 11, or 23 in any applicable register; (3) any one of the six program flags; (4) any one of the six sense switches; (5) any one or all three carry toggles at the same time; (6) any one of the four interrupt mask bits; and (7) any one of four interrupt lines when not in the automatic interrupt mode. In addition, bits 6, 7 and 8 may be tested simultaneously for any 3-bit pattern. *Each of the above testing operations requires only one microsecond.*

UNIQUE DATA SHIFTING PROVISIONS

The Raytheon 520 has shifting capabilities which are unique in the industry. Shifting is applicable to all seven arithmetic registers at speeds up to 500 nanoseconds/bit. There are 84 shifting combinations. Any register may be shifted left or right, open or closed or logical or magnitude fields. Other combinations include a normalizing shift for sign, exponent, fraction or any combination of these, and a shift right double length floating mantissa fields. In addition, the 520 can shift left six bits from any register into any other register in one microsecond.

OPTIONAL NON-DESTRUCTIVE READOUT MEMORY

An optional fast memory may be employed in the 520 System. This memory is of the NDRO (Non-Destructive Readout) type, does not require a rewrite cycle after each read cycle, has an access time of less than 200 nanoseconds, and allows any register to be loaded in only one microsecond. Fast memory is particularly useful for storing frequently used subroutines and substantially improves the throughput of the system. For instance, fast memory reduces the average time for a 24-bit mantissa floating add, not including the calling sequence, from 32 to 17 microseconds. This fast memory, known as BIAX for its multi-aperture ferrite storage element, is manufactured by Raytheon Computer.

RAYTHEON 520 SYSTEM PERFORMANCE

FLOATING POINT OPERATIONS

In general, computer floating point operations may be implemented with either software subroutines or special purpose hardware. Because of its speed and optimized register layout, the 520 System can execute programmed floating point operations at speeds competitive with expensive hardware options for other machines. These highspeed operations can be executed in any one of three floating point formats.

Utilizing 8-bit exponents, mantissa lengths of 16, 24, or 39 bits, including sign, are available. The 24-bit times are fastest, since this format requires less manipulation. The unusual 16-bit format is efficient, since exponent and mantissa are packed into one word. A 16-bit mantissa is adequate for many system applications where 12-bit data is typical. Note that the 16-bit and 39-bit formats are identical, except for mantissa length. This allows efficient intermixing of the short and long formats within one program.

THE RAYTHEON 520 SYSTEM OUT-PERFORMS COMPETITIVE MACHINES

Compared to other computers in its price class, the Raytheon 520 System displays a substantial speed advantage in scientific, engineering and data systems applications. Some of the specific operations in which the 520 demonstrates this advantage are detailed in the table on page 7.

Almost every computer programmer approaches and solves a problem in a different manner. Timing of the operations chosen to illustrate the 520 System's performance superiority are undoubtedly subject to such variations in approach and methods. To minimize the effect of these variables and to ensure overall accuracy, all times for performance of the listed operations on competitive computers were derived from detailed study and application of published programming and reference manuals by professional programmers who, in many cases, were able to draw on actual experience with the machines being compared.

FORTRAN Benchmark tests of 520 System speed will effectively demonstrate overall system superiority.

FLOATING POINT OPERATION TIMES (In Microseconds)*

OPERATION	Subroutine In NDRO Memory			Subroutine In Core Memory		
	Mantissa			Mantissa		
	16-Bit	24-Bit	39-Bit	16-Bit	24-Bit	39-Bit
ADD**	25-42	21-36	34-45	31-57	29-52	47-64
SUBTRACT**	27-44	23-38	36-47	34-60	32-55	50-67
MULTIPLY	37-39	25-28	74-76	48-51	34-38	95-98
DIVIDE	42-44	48-53	112-129	56-59	65-73	135-157

*Includes subroutine calling sequence of eight microseconds in core memory.
**Assumes an average of two bits of shifting to scale mantissa.

DERIVED TIMES IN MICROSECONDS INCLUDING MEMORY CYCLE

OPERATION	RAYTHEON 520 with NDRO Memory	RAYTHEON 520 w/o NDRO Memory	SDS 930	CDC 3100	IBM 360/40
SCIENTIFIC/ENGINEERING FUNCTIONS					
Floating Point Add (24-Bit Mantissa)	21-36*	29-52	81	NA	43**
Floating Point Add (39-Bit Mantissa)	34-45*	47-64	NA	210†	NA
Floating Point Multiply (24-Bit Mantissa)	25-28*	34-38	59	NA	105**
Floating Point Multiply (39-Bit Mantissa)	74-76*	95-98	NA	340†	NA
REAL-TIME DATA SYSTEMS FUNCTIONS					
Add Register-to-Register	1	1	NA	1.8	7.5
Convert to Eng. Units (12-Bit Data) (ax + b)	10.5	15.5	19.25	21.5	81.26
Normalization $\left(\frac{x-z}{f}\right) \rightarrow y$	14.5	20.5	31.5	22	216.26
Convert any 6-Bit Code to any other code	1	2	8.75	5.25	17.5+6.25/CH.
Binary to BCD Conversion (4 Six-Bit Char.)	24.5	32.5	112	77.5	<50
BCD to Binary Conversion	18	28	80.5	72	<45
Data Quality Check (Match 24-Bit Word Against Reference Word and Count Unmatched Bits)	16	23	69	49.4	108
Limit Check Two 12-Bit Data Words for Upper and Lower Limits	12	20	28	15.2	100.5

*Times for subroutines in fast memory and calling sequence in main memory.
**Short format (24-Bit Mantissa and 7-Bit hexadecimal exponent) with floating point option.
†36-Bit Mantissa

SOFTWARE

- BOSS, the 520 Operating System
- FLEXTRAN Compiler-Assembler
- 520 FORTRAN II and IV
- 1620 Simulator

These 520 System software packages are designed to ease the programmers' efforts in writing and debugging, and to maximize management's return on investment by automating the processing of jobs and utilizing existing program libraries. The following software packages are among those available:

BOSS, THE 520 OPERATING SYSTEM

Raytheon brings to the 520 System user automated operation and productivity previously reserved for scientific computers of larger classes. The 520 Operating System provides several important benefits — automatic assignment and control of input-output, control and batch processing of jobs, time accounting and other housekeeping operations. The 520 Operating System is used when on-line debugging is not taking place, and when high production per dollar invested is desired by the operating management. It supplies control of those processors and routines which provide the capabilities of compilation, assembly, loading, program execution and continuous system operation. Inter-mixing of job types and the compile/ execute and assembly/execute modes are provided. Scheduling jobs is the responsibility of facility personnel.

Dynamic core dumps during program execution and post mortem dumping are accomplished under control of BOSS.

An editor routine provides the capability of modifying, adding, deleting, or replacing system routines and programs stored in the library.

FLEXTRAN COMPILER-ASSEMBLER

FLEXTRAN is an automatic programming system of the compiler-assembler type. It provides the programmer with many capabilities to ease the writing and testing of programs. In addition to mnemonics for each machine instruction, a standard set of macro instructions is incorporated.

FLEXTRAN allows the addition of new macro instructions either temporarily or permanently as the user requires. Thus macro instructions oriented toward particular applications are possible; for example, one may create macros that facilitate the translation of programs for other computers to 520 machine language.

FLEXTRAN is capable of producing efficient object programs suitable for computer based data systems where realtime throughput must be maximized. It was created with applications such as data acquisition, telemetry processing, and hybrid computing in mind.

Macro instructions which provide control of realtime input-output devices such as multiplexers, A/D and D/A Converters, magnetic tapes and disks, etc., are incorporated. Instructions designed for bit manipulation applications, including PCM data quality checking, will ease the system programmer's job.

FLEXTRAN generates relocatable object code. Separately assembled programs can be linked regardless of the sequence in which the segments or instructions are assembled. This means that several programmers can work on separate sections of a program simultaneously. Input-output devices may be assigned at object time. Object code may be in-line machine code or it may employ subroutines.

RAYTHEON 520 FORTRAN II & IV

Both the language and the processor that make up Raytheon 520 FORTRAN II have been expanded beyond basic FORTRAN to provide the user with a rich procedure-oriented programming system unexcelled in its class.

Major advantages include removal of most of the redundancies and logically unnecessary restrictions of earlier versions of the language. In addition, the meanings of some of the other features of FORTRAN have been generalized so that they apply to more situations than formerly. The result is that Raytheon 520 FORTRAN II language is easier to learn, easier to use without making minor errors, and is more powerful than earlier versions of FORTRAN.

The Raytheon 520 FORTRAN IV System has for its basis the language that is the standard FORTRAN advanced by the American Standards Association. This language has been enhanced by facilities that enable the rapid and efficient development and testing of programs written in FORTRAN. In addition, the language has been enriched to permit exploitation of such machine features as the hardware interrupt facilities, thus providing the basis for real-time capability. The processor also allows programs written in FLEXTRAN to be incorporated in FORTRAN programs.

The Raytheon 520 FORTRAN IV processor is treated simply as another system program that is called and executed under control of the operating system monitor, BOSS. For this reason, the processor is easy to use, providing optimum throughput in both the batch-compile and compile-and-execute modes. Moreover, as an intrinsic part of the programming support package, FORTRAN IV shares with FLEXTRAN the subroutine library commonly structured to satisfy the needs of both.

THE 1620 SIMULATOR

The IBM 1620 Computer was oriented toward "stand-alone" scientific applications. There are approximately 1,500 of these units reported to be in use. For many of these users who wish to move up to a modern, high-speed, system oriented processor, Raytheon provides a 1620 Simulator. It allows use of the thousands of existing machine language programs and can extend the amortization of a large programming investment. Its most important benefit is to provide low-cost, smooth transition to the Raytheon 520 System without the expensive, disruptive process which normally accompanies change over.

The 520 System user who has not replaced a 1620 benefits also. He may utilize the many application programs for the 1620 as they enter the 520 Programming Library. He may also exchange programs with the 1620 computers in his or associated organizations.

All basic and optional 1620-I and II instructions are simulated to allow direct execution of machine language programs. The Raytheon 520, because of its efficient simulation capability, executes 1620 programs at least three times faster than the 1620 Mod I. Programs written in the 1620 FORTRAN source language would, of course, be compiled and executed at much higher speed via 520 FORTRAN, without use of the 1620 Simulator.

The 1620 Simulator provides data processing serially by digit or variable length decimal fields.

IBM 1402 Card Reader/Punch and a Disk Pack are available with the 520 System. Where these peripherals are already available at a 1620 site, Raytheon will interface to them and provide further use of an existing user investment.

THE RAYTHEON 520 INPUT/OUTPUT SYSTEM

The Raytheon 520 provides the most powerful and useful input/output capability available in machines of its class. Input, output and computing can occur simultaneously. Basic input-output character rate is 560KC; word rate is 140KC.

The 520's Input/Output System features the use of a true dual-bus structure (input and output) to which peripheral devices may be added at any time. Direct addressing for up to 512 devices is provided.

Devices are connected to the I/O bus via a controller interface which is unique for each type of device. Each controller has buffer storage appropriate to the device, e.g., 6-bit buffers for paper tape and typewriter I/O and dual 24-bit buffers for magnetic tape. Since there is an individual buffer for each device, it is not necessary to time-share one buffer among many devices. Each of the four I/O channels may be time-multiplexed among many devices, giving the 520 the ability to input, output, and compute simultaneously.

All I/O devices are physically connected to the I/O bus at all times. Under program control, a device may be electronically connected to ("selected") or disconnected from ("deselected") any one of the four 24-bit I/O channels. Each channel is provided with an interrupt line.

PERIPHERAL EQUIPMENT

Typewriter	15 cps
Paper Tape	110 cps punch 300 cps read with rewind, read reverse, and spoolers
Punched Cards	100 cpm reader, 100 cpm punch 800/250 cpm reader punch
Magnetic Tape	45 ips, 75 ips 200 bpi, 556 bpi, 800 bpi 9KC — 120KC
Line Printers	300 lpm, 600 lpm, 1250 lpm 80, 120, 132 or 160 columns
Disk Pack Memory	2 million 6-bit characters per drive, IBM 1311 - compatible (disk file memory also available)
Multidevice Controller	Generalized data system interface allows simple, low-cost expansion by the user with standard sub-assemblies and digital modules
Direct Memory Option	Provides high speed block transfer capability between I/O device and memory with simultaneous computation

MAGNETIC TAPE CONTROLLER

The magnetic tape controller provides two 24-bit buffer registers; one buffer transfers 24-bit parallel words to/from the I/O bus, the other acts an an assembly/disassembly register and transfers 6-bit characters to/from the magnetic tape read/write electronics. The use of dual buffering allows the computer program a maximum of one word time rather than the usual one character time to respond to an interrupt and hence allows more computing during tape operations.

The Raytheon 520 System's programmed magnetic tape format control capability allows maximum flexibility, system efficiency, and computation during tape operation.

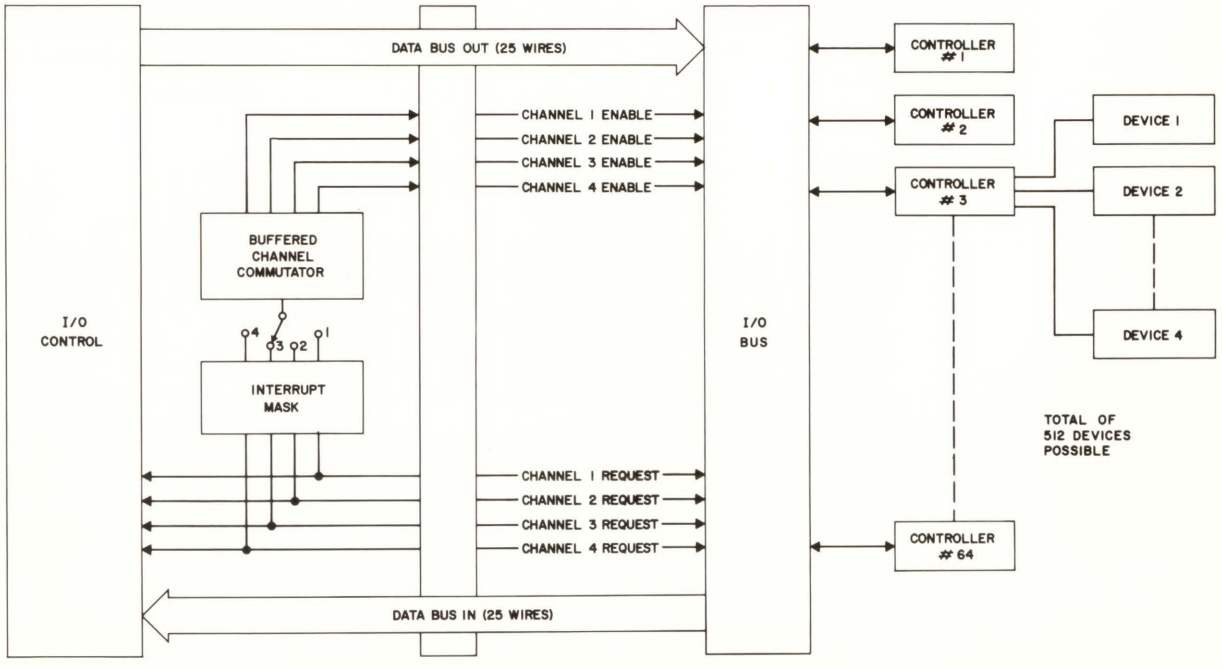
Since input-output format of the tape controller is under program control, the programmer may designate each computer word to contain 1, 2, 3, or 4 characters. This technique avoids the necessity of packing, under program control, four characters per word before an output operation or unpacking during input.

The exceptionally fast code translation and radix conversion capability of the Raytheon 520 System allows efficient communication with a variety of on-line devices without the need for expensive external translation circuitry. This capability is important in working with communication terminals, laboratory instruments, displays and other external data systems devices.

DIRECT MEMORY INPUT/OUTPUT OPTION

High speed data transfers may be handled independently of the central processor by exchanging data directly between the I/O device and memory. This option allows data transfer rates of up to 400,000 words per second.

The address of the starting position in memory and the block length in words are loaded via the central processor into hardware registers contained in the I/O adapter unit. After starting, no further attention from the central pro-



cessor is required until the block transfer has been completed. At this time, at the programmer's option, the central processor may or may not be signaled via the interrupt system. In this manner, for example, data may be entering one area of memory from a disk pack or file while a second area of memory is being unloaded onto magnetic tape and the central processor is computing on unrelated data.

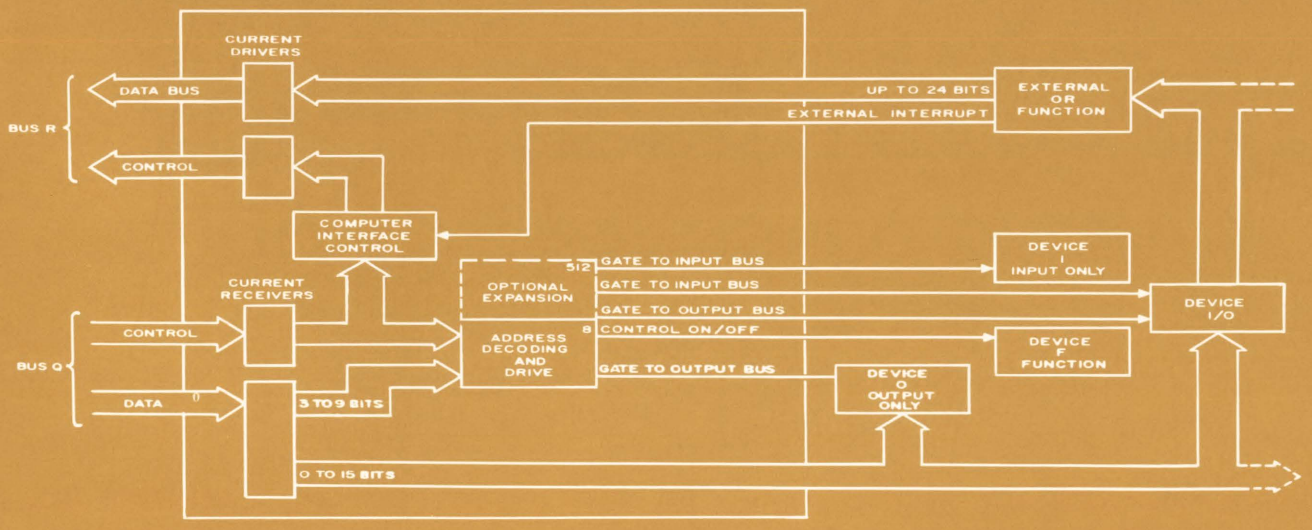
RAYTHEON 520 SYSTEM MULTIDEVICE CONTROLLER (MDC)

Almost all data system requirements are easily and efficiently implemented with the 520's Multidevice Controller. This unit serves as an interface between the 520's I/O bus and up to 512 external data systems devices.

The MDC provides a 24-bit input data bus, a 15-bit output data bus, and a 9-bit address bus. Address and output data bus information are output simultaneously as one 24-bit word. External device identity and data are transmitted in a single I/O operation. This takes advantage of the 520's register format and results in more efficient use of memory, computer time and I/O time.

An optional priority interrupt system may be added to the MDC. This features the direct development of a 15-bit address unique for each interrupt level, logic for gating out lower levels so that a given level may be interrupted by a higher level, a mask register that allows each unique level to be enabled or disabled without affecting the other levels.

Many other options are available for the MDC. These include: standard pre-wired module cases to expand the basic unit up to 512 decoded device selection lines; input assembly registers or output disassembly registers that allow packing one 24-bit, two 12-bit, three 8-bit or four 6-bit data words into one computer word; interval timers of 15 or 24 bits with programmable input frequencies; BCD time-of-day digital clock; analog timing subsystem; output control registers; sense switch input control registers, and digital counters.



RAYTHEON 520 SYSTEM APPLICATIONS

GENERAL PURPOSE SCIENTIFIC PROBLEM SOLVING

The Raytheon 520 System has been designed for this application and provides hardware and software capabilities for many configurations. Open shop problem solving on smaller configurations using FLEXTRAN or the 1620 Simulator are appropriate. For a typical small configuration, the 520 processor could be equipped with an 8192 word core memory. For expanded requirements, a system could include a processor with 12K of main memory, a 512 word fast memory, disk pack, magnetic tape, line printer, etc. A typical system is diagramed below. Maximum productivity of a system this size can be achieved by use of the BOSS operating system. An 8192 word core memory with or without the 200 nanosecond fast memory may be employed with typewriter and card or paper tape input-output. The system may be expanded to include disk pack, magnetic tape, line printer, etc., as appropriate.

The 520 System may be interfaced to realtime data acquisition sources or teletypewriter, and can output results for closed loop control or hybrid computation when the user need expands to include these requirements.

DATA ACQUISITION

Raytheon will provide complete data acquisition and data processing systems for applications such as medical experiments, rocket engine tests, meteorological sensors, nuclear experiments, seismic surveys, wind tunnels, oceanographic mapping, or process monitoring.

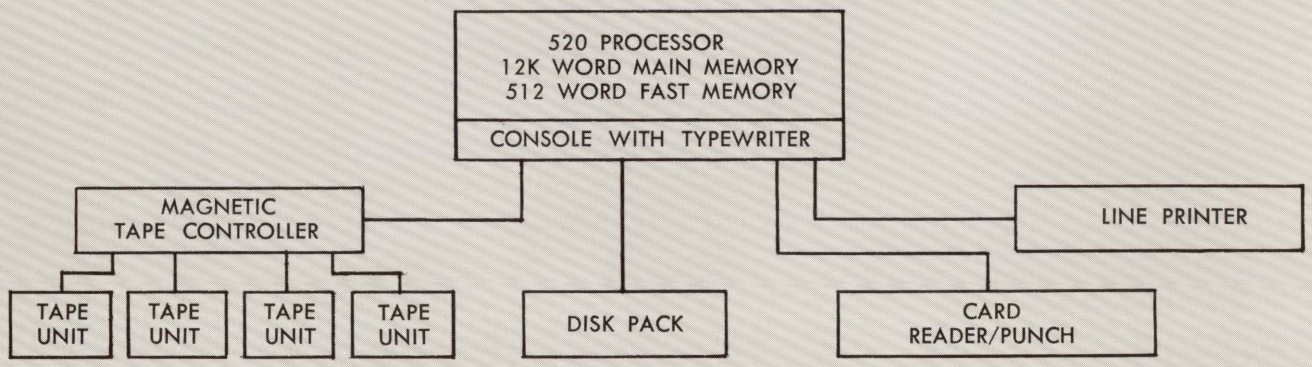
Unique analog instrumentation products and engineering skills assure the customer of a reliable, high performance data system. The Multiverter®, a standard product available only from Raytheon, provides: a 1000 megohm input, 0.01% integrated circuit Multiplexer capable of 250 KC switching; a 50 nanosecond, 0.01% Sample and Hold Amplifier; and anyone of several 0.01% high-speed A/D Converters. These functions, and up to 96 channels of Multiplexer, may be housed in a single self-powered 5¼" high drawer for rack mounting. This data acquisition front end is typically supplied with 15-bit (14-bits plus sign), 30 KC throughput, or 12-bit (11-bit plus sign), 50 KC throughput.

Other data system products, including high-speed 0.01% D/A Converters, are available from Raytheon.

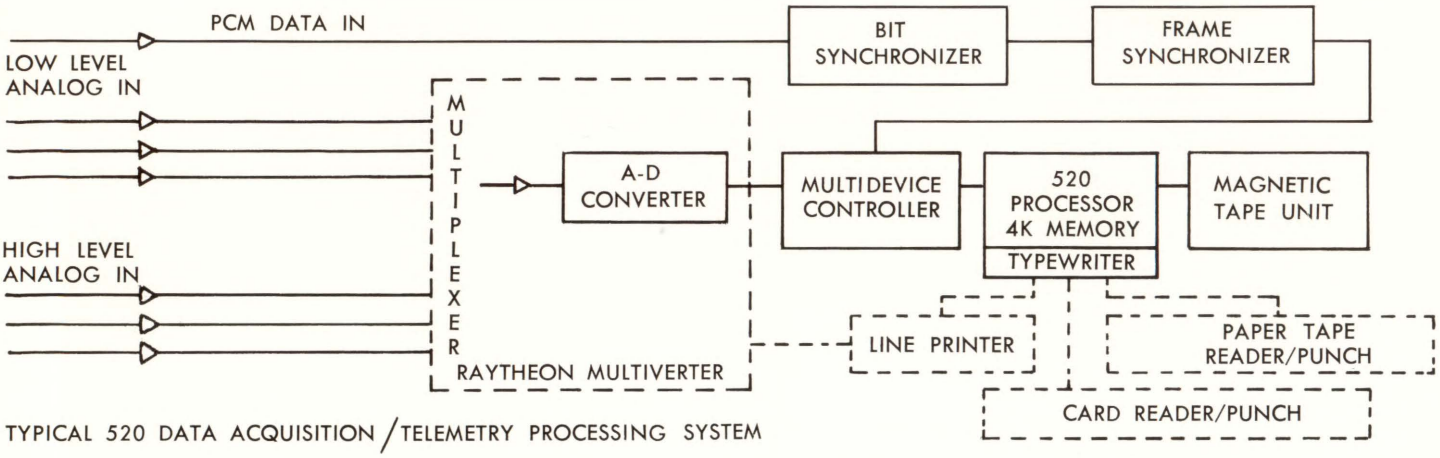
For those situations where 6 or 8-bit A/D conversion is appropriate, Raytheon provides a 5 or 1 MC converter.

The Raytheon 520 System includes the Multidevice Controller for realtime I/O interface to the processor as described elsewhere in this brochure.

A typical Raytheon 520 System application to data acquisition is shown on the next page.



RAYTHEON 520 SYSTEM TYPICAL SCIENTIFIC CONFIGURATION



TYPICAL 520 DATA ACQUISITION / TELEMETRY PROCESSING SYSTEM

TELEMETRY DATA REDUCTION

Telemetry data acquisition and reduction is another current application in the real-time data systems area where the Raytheon 520 System demonstrates advantages in data throughput rate and flexibility of data manipulation.

A typical system consists of a 520 System plus the peripheral equipment required to accept and process PCM, PAM, and PDM telemetry data, high-level analog inputs and additional serial and parallel digital data.

The capabilities of a Raytheon 520 System in such an application would include:

1) Handling continuous PCM data input, gapped magnetic tape output at 120KC — over 650,000 bits per second with a 40 percent computer duty cycle.
2) Handling continuous digital tape input at 90 KC, output gapped tape at a 120 KC character rate — less than 30 percent computer duty cycle.
3) Providing computer addressing of an optional analog multiplexer and analog-to-digital converter, sampling, conversion (11 bits plus sign), formatting, and writing gapped IBM-compatible tape — 40,000 samples per second.
4) Providing computer addressing of an optional analog multiplexer and analog-to-digital converter, sampling, conversion (11 bits plus sign), formatting, linearizing, and writing gapped IBM-compatible tape — 20,000 samples per second.
5) Performing PCM data decommutation and distribution to digital and analog displays by computer stored program, limit tests, linearization and magnetic tape recording at rates in excess of 250,000 bits/sec.

A similar system is now operational for the Air Force Systems Command at Eglin Air Force Base. Details will be furnished on request.

THE 520 AS A "BLACK BOX"

System engineering organizations will want to consider the 520 for use in custom systems requiring high-speed digital computation, data formatting, communications switching, or digital simulation. Its ultra fast internal speed, including 45 one-microsecond instructions and register-to-register operations, makes it a powerful system component. Two hundred nanosecond memory with register load every microsecond is a unique capability for function generation, table look-up, executive control, data output, etc. 520 I/O is in keeping with high-speed system demands.

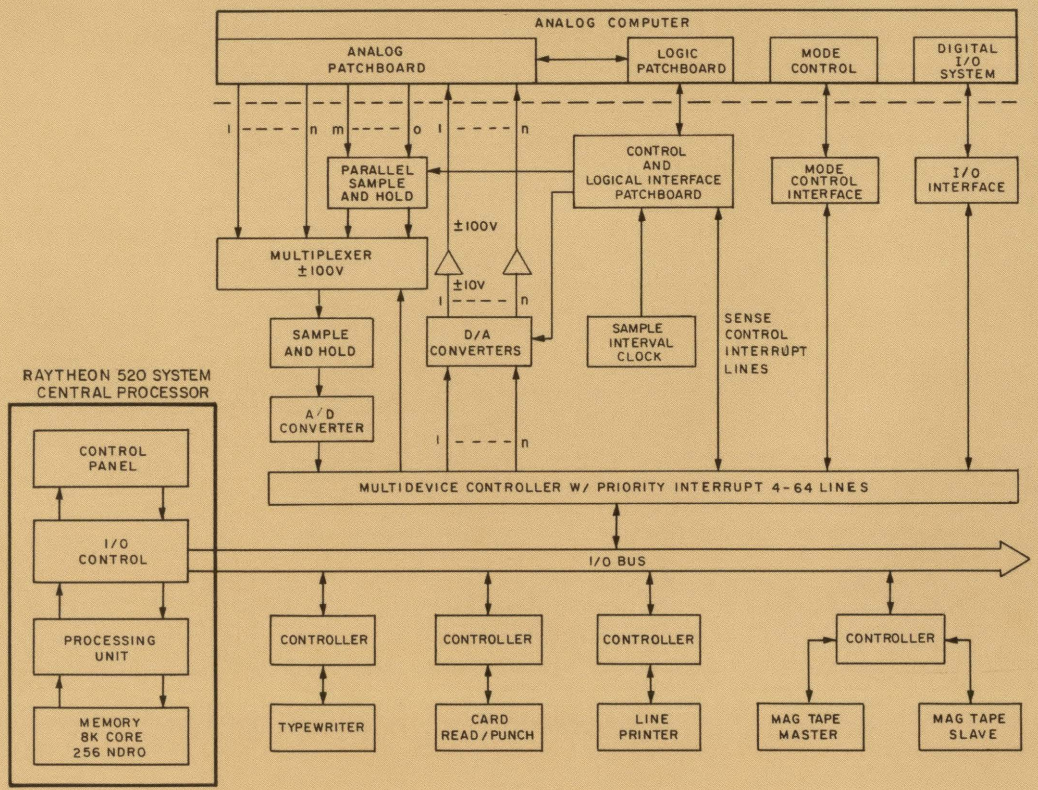
THE RAYTHEON 520 SYSTEM FOR HYBRID COMPUTING – HYCOMP 520

Raytheon Computer has had broad experience in supplying digital computers or linkage subsystems for hybrid analog-digital computing systems. This experience is based on capability in the design, and manufacture and application of digital computers themselves, as well as the analog-to-digital converters, digital-to-analog converters and other equipment and software required for efficient and accurate communication between the two major elements of the system.

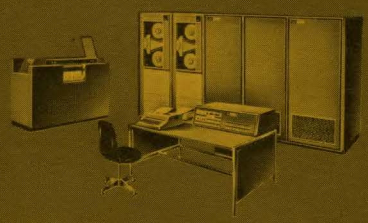
The new Raytheon 520 System's high internal processing speeds, especially its high-speed multiply operation, its 1 microsecond register-to-register add and its ability to input/output up to 280,000 12-bit words per second make it well suited for hybrid computing applications. The 520's 200-nanosecond memory allows ultrafast table look-up, function generation and floating point arithmetic operations.

Raytheon is also applying the latest technology to the computer linkage system. A new development—the Multiverter®—introduces integrated circuits to the Raytheon equipment line and makes possible the packaging of 96 channels of 0.01% multiplexing, a 50 nanosecond, 0.01% sample-and-hold amplifier and any one of Raytheon Computer's standard line of high-speed, 0.01% accurate analog-to-digital converters in a single drawer 19 inches wide by 5¼ inches high. This "data system in a box" provides a throughput rate of up to 50KC, significant for hybrid computing applications.

Subroutines which can be called by FORTRAN CALL Statements for system control permit simplified programming of the 520 for hybrid applications.



RAYTHEON 520 HYBRID COMPUTER SYSTEM



SALES OFFICES

Alabama

RAYTHEON COMPUTER
Holiday Office Center, Suite 47
Huntsville, Alabama
Phone (205) 881-2844
TWX 510 579-2113

California

RAYTHEON COMPUTER
2700 South Fairview Street
Santa Ana, California 92704
Phone (714) 546-7160
(From Los Angeles 625 7645)
TWX 714 546-0444

Massachusetts

RAYTHEON COMPANY
Bedford Laboratory
P. O. Box 508
Bedford, Mass. 01730
Phone: (617) 274-7100, Ext. 643 and 644
TWX 617 274-6487

Texas

RAYTHEON COMPUTER
204 East Main
Arlington, Texas
Phone (817) CR 5-5361
TWX 817 274-3917
Houston, Texas
Phone (713) WA 3-1144

Washington, D. C.
Eastern Regional Office

RAYTHEON COMPUTER
4217 Wheeler Avenue
Alexandria, Va. 22334
Phone (703) 836-7616
TWX 703 931-4247

RAYTHEON

RAYTHEON COMPUTER

2700 SOUTH FAIRVIEW ST., SANTA ANA, CALIFORNIA 92704

LITHO U.S.A.