
QUANTUM

**PRODUCT
DESCRIPTION**
TECHNICAL REFERENCE MANUAL

Q2080
8" Media Fixed Disk Drive

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Q2080 DISK DRIVE

Technical Reference Manual

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PREFACE

Document Objective

The Quantum *Q2080 Disk Drive Technical Reference Manual* describes the principles of operation, major circuits, component parts, maintenance, and applications of the Q2080 drive.

Intended Audience

This manual is for experienced Design Engineers, Applications Engineers, Software Programmers, and Repair Technicians using the Q2080 drive for OEM applications.

Document Structure

- Section 1 describes the principles of operation of the drive mechanics and electronics.
- Section 2 shows schematics of the Q2080 circuits.
- Section 3 describes errors and media defects, self diagnostics, and track format applications.
- Section 4 summarizes maintenance procedures.
- Section 5 shows illustrated parts diagrams for all major assemblies including bills of material.

Associated Documents

Additional information on the Q2080 drive, including general specifications and installation procedures, is contained in the *Q2080 Product Description OEM Manual*.

SECTION I

PRINCIPLES OF OPERATION

1.1 MODEL Q2080 BLOCK DIAGRAM

The block diagram shown in Figure 1-1 represents the Model Q2080 disk drive. The spindle drive motor may be powered by either 110 VAC, 220 VAC or 24 VDC. The motor drives the spindle by a belt and pulley arrangement. There is a different belt/pulley set for 50 HZ and 60 HZ AC. The DC motor uses the 60 HZ belt/pulley set. These interchangeable belt/pulley sets allow the spindle to rotate the disks at 3,000 RPM for either frequency.

The head stack assembly is mounted to the rotor of the proprietary rotor positioner assembly. The positioner motor is driven from circuitry on the control PCB via power drivers on the heat sink. Track crossing and coarse position feedback signals are obtained from an optical encoder and scale assembly via the encoder PCB. A dedicated servo surface provides fine track position. This servo data is written on the bottom surface of the lowest platter. Read/write signals are obtained from or written to seven disk surfaces via the heads, head switching matrix, and preamplifier encoder. The drive control PCB contains electronics for reading and writing, as well as the microprocessor that controls actuator positioning and servo position decoding.

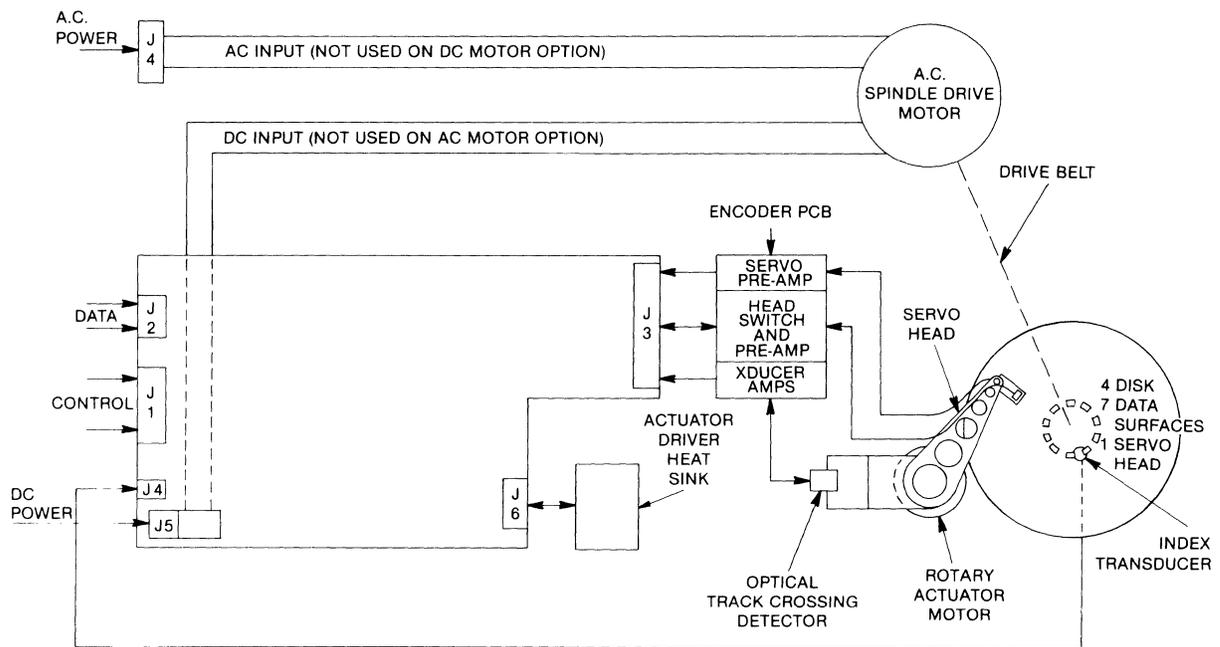


FIGURE 1-1
MODEL Q2080 BLOCK DIAGRAM

1.2 MODEL Q2080 DRIVE MECHANISM

The drive mechanism consists of the mechanical drive sub-assemblies in a sealed enclosure. **None of these sub-assemblies requires adjustment nor are they field repairable.**

1.2.1 DRIVE MECHANISM BLOCK DIAGRAM

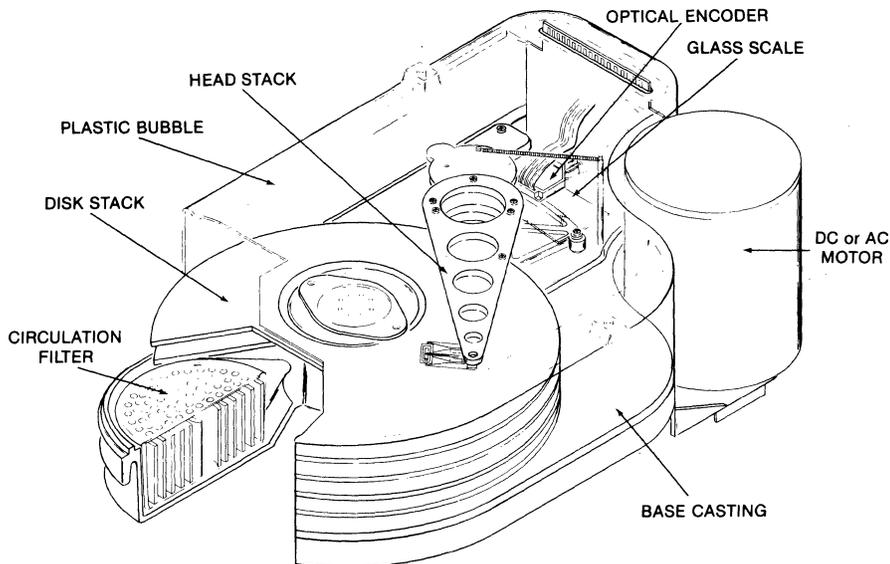


FIGURE 1-2
MODEL Q2080 MECHANICAL LAYOUT

1.2.2 OPTICAL ENCODER

The optical encoder is mounted on a shaft that is pressed and bonded into the base casting. The assembly consists of a housing, an infrared light emitting diode, an optical reticle, and a multi-cell photo diode matrix.

The infrared LED is mounted in the lower half of the housing. This allows the optical scale near the lower arm of the head stack to move between the infrared LED and the upper half of the housing that contains the reticle and photo cells. The reticle masks five photo cells so that each cell only receives light through a specific portion of the moveable scale. Both the clearance and angular position of reticle and scale are precision adjustments that are made when the drive is manufactured.

1.2.3 ROTARY POSITIONER ASSEMBLY

The positioner used in the Model Q2080 (a design proprietary to Quantum) consists of upper and lower magnet plates, rotary single phase coil, head stack mounting hub, two magnet rings, and bearing shaft. The magnets are composed of alternating poles bonded to the magnet plates that, in turn, are bolted to the base casting. The rotor and hub are bonded together and the bearings and shaft are bonded into the hub. This entire bearing shaft assembly is bonded into the base casting. The shaft/casting bond provides both mounting rigidity and an air-tight seal between the shaft and mounting bore. The bearing to shaft bond and bearing to hub bond are also rigid and air-tight. This design allows the mass center of the head stack to be placed at the hub so that bearing wear and friction are minimized and gravity forces cannot apply torques to the head stack that would have to be countered by rotor current. This enables the drive to operate in any orientation. The crash stops, which prevent the heads from being driven into the spindle or off the disk surface, are mounted to the upper magnet plate.

1.2.4 HEAD STACK ASSEMBLY

The head stack assembly consists of the heads, head arms, and counter balances. In addition, the optical scale is bonded to the lower counter balance. The counter balances are castings whose shape and weight are designed to insure that the mass center of the entire stack is at the center of the mounting hub. The lower counter balance is slightly different than the others as it holds the rubber crash stop bumper and optical scale. The heads are Winchester slider type mounted to spring steel flexures that are staked to the head arm. The head conductors are routed in plastic guides and tacked in place with an adhesive. All head stack assemblies consist of an upper head arm assembly, a lower head arm assembly, and three dual head arm assemblies.

1.2.5 DISK STACK ASSEMBLY

The disk stack assembly consists of the spindle bearing assembly, disk mounting hub, disks, disk spacers, disk clamp, drive pulley, spindle grounding system, and ferrous exclusion seal. The bearing assembly is bonded in place and a ferrofluid magnetic seal is applied at the top of the assembly. This seal prevents outside air from entering the drive through the bearing bore or along the bearing shaft. A sector ring, which provides index pulses to the user and servo timing to the microprocessor, is mounted on the disk hub. A drive pulley mounted on the bottom of the spindle bearing assembly couples the spindle to the motor pulley through a flat belt. The spindle grounding system consists of a carbon button bonded to the spindle screw and a spring contact on the belt guard. Four disks and three spacers are clamped on the hub. These disks are an aluminum alloy with a magnetic oxide coating that is polished and lubricated. The lubrication prevents head and media wear when the heads are in contact with the disk surface, which only occurs outside the data area when the disks are not rotating.

1.2.6 BASE CASTING ASSEMBLY

The base casting is a single piece cast aluminum alloy that provides a mounting surface for the rest of the drive mechanism. It has two machined holes used to mount the positioner assembly and optical encoder. The outside top edge is flat to ensure an air-tight seal with the bubble cover. Surfaces are provided for mounting the transducer PCB, and the upper and lower magnet plates for the positioner motor. Mounting holes are also provided, outside the bubble area, for the drive motor and belt guard spindle-ground assembly.

1.2.7 AC DRIVE MOTOR

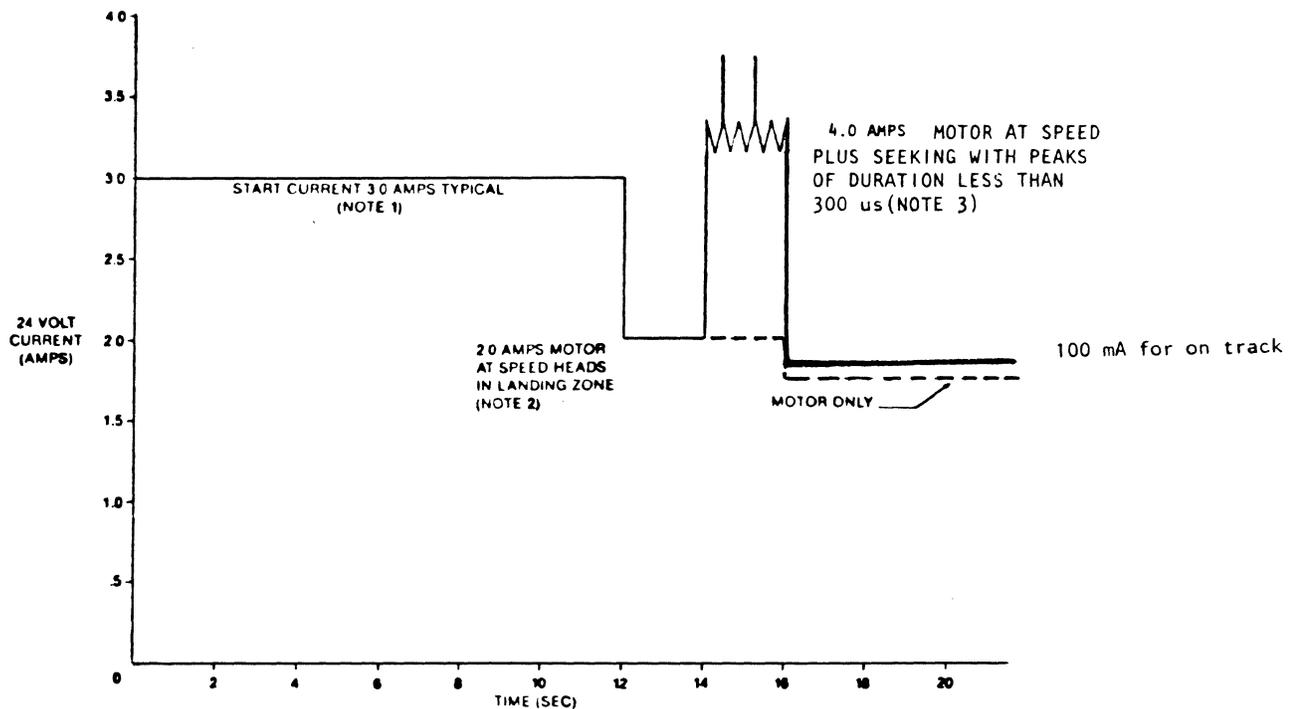
The Q2080 spindle is driven by an induction AC motor and belt/pulley combination. Two motors are available, one for 110 VAC operation and another for 220 VAC operation. Both motors will operate at either 50 or 60 HZ. However, since the 50 HZ input will result in a slower motor rotational speed than the 60 HZ input, different size pulleys and belts are used to set the spindle rotational speed at 3,000 RPM regardless of input frequency. Changing the Q2080 from one frequency or voltage to the other is described in section 4.4.1 of this manual.

The motor capacitor and AC input connector are both part of the AC motor assembly. The capacitor is used to provide the necessary phase shift to get the motor to start and run in the correct direction. The motor is mounted on the base casting with three studs and is isolated from direct contact with the base casting with plastic washers. The washers provide AC ground isolation and prevent excessive motor vibrations from being mechanically coupled into the drive base. The drive pulley is mounted to the motor shaft. Pulley size is dependent on AC line frequency. (The 50 HZ pulley is larger than the 60 HZ pulley.)

1.2.8 DC DRIVE MOTOR

The Q2080 is available with an optional DC spindle drive motor assembled by Quantum, which directly replaces the standard AC motor. The motor is microprocessor controlled using an Intel 8048 single chip microprocessor. Three Hall effect devices provide position and velocity feedback to the microprocessor that controls, using pulse width modulation, three Darlington transistors. The Darlington transistors, by having their collectors connected to motor coils, control the current driving the motor coils. The currents from emitters of the three Darlington transistors pass through one current sense resistor. The current sense resistor, in conjunction with the microprocessor, regulates the startup and running current of the motor.

Figure 1.3 displays a typical current profile of a DC motor on the Q2080 drive.



**FIGURE 1-3
DC DRIVE MOTOR CURRENT PROFILE**

The start sequence for the Q2080 with the DC motor option has four steps. Each step uses a different amount of 24 volt current.

1. During start up, the motor takes 3.0 amps and the actuator is disabled so that the entire 24 volt current is used in the motor. This state lasts until the microprocessor senses that the motor is 90% of full speed, typically twelve to sixteen seconds.

2. After the motor reaches 90% of full speed the microprocessor limits the motor to 2.0 amps. There is a period of one to two seconds when the motor is in the lower current limit and actuation is disabled.

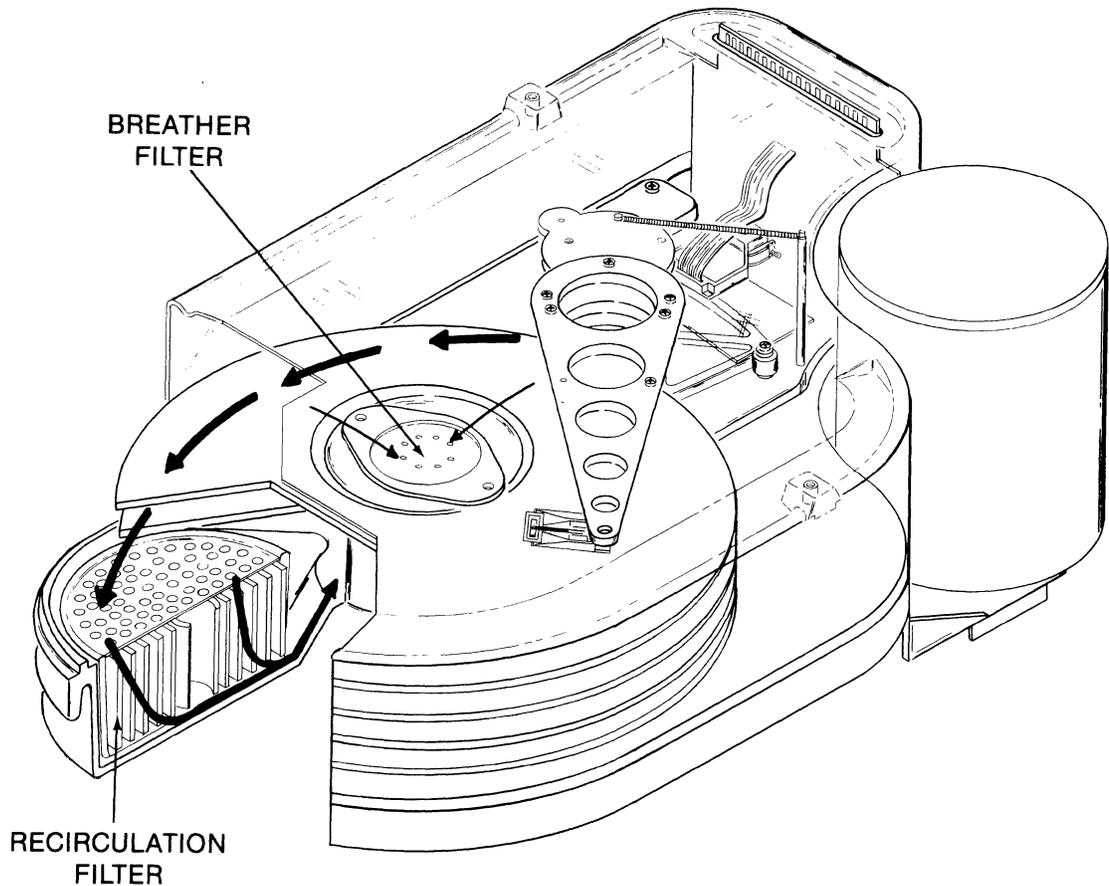
3. When the drive reaches 92% of regulated speed, the actuator begins its recalibration sequence. The motor continues to draw 2.0 amps and the actuator draws 2.0 amps. At the end of each buffered seek, this 4.0 amp level is topped by a spike of less than 4.0 amps and less than 300 us duration. The recalibration current level is repeated during normal seeking.

4. After recalibration and the motor has reached full speed, the actuator remains on track using 100 mA of 24 volt current and motor current drops to 1.75 amps. The total motor and actuator current is then 1.85 amps. This is the nominal drive current during the read/write and quiescent states.

1.2.9 AIR FILTRATION

The Model Q2080 is a Winchester type drive, and as such, the heads fly very close to the media surface. The nominal flying height is eighteen micro inches or roughly 1,600 times smaller than the period at the end of this sentence.

It is absolutely essential that the air circulating within the drive is kept clean of particles. Sealing the drive in a bubble and using the rotating disks as an air pump to force the air through a filter ensures clean circulating air. Figure 1-4 shows the air flow in the enclosed area of the drive. The lowest pressure area within the drive is located at the top in the center of the spindle. A 0.3 micron breather filter is bonded in this area of the bubble. This filter allows outside air into the bubble enclosure to equalize internal and external pressures. The highest pressure area within the drive is located at the inner surface of the bubble. Bonded in the base casting at this location is another 0.3 micron filter called the circulation filter. Air constantly pumped into the top of this filter exits from the bottom into a channel cut in the base casting. This channel extends from the filter to a location close to the spindle where pressure is lower than at the top of the filter. This ensures a continuous flow of filtered air as soon as the disks start to rotate. Due to the stringent requirements for cleanliness, the bubble and/or seals should not be tampered.



**FIGURE 1-4
AIR FILTRATION SYSTEM**

1.2.10 AUTOMATIC ACTUATOR LOCK

The Q2080 uses a dedicated landing zone inside track 1171 to prevent damage to the media data area during shipping or handling.

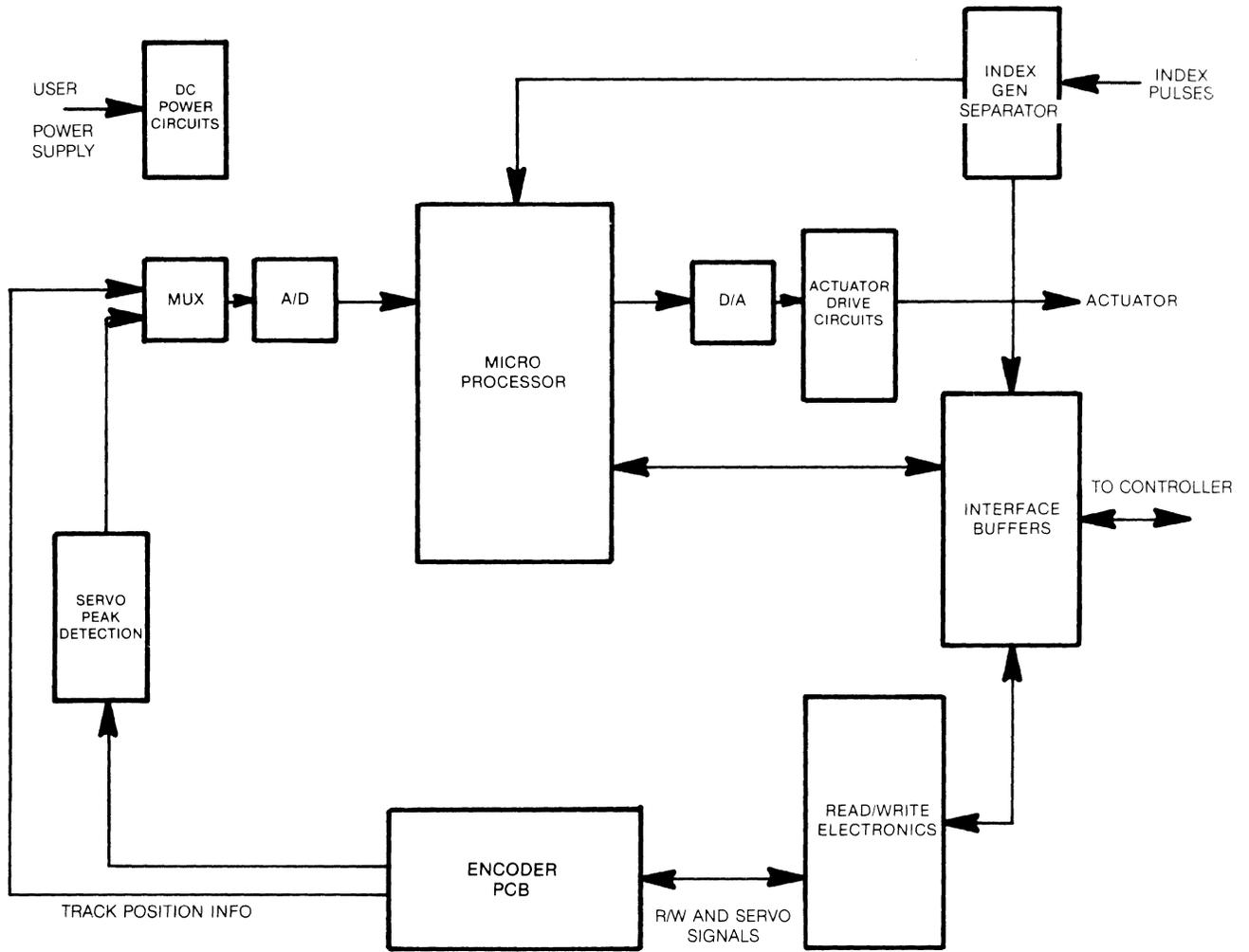
The AIRLOCK™ used in the Model Q2080 (a design proprietary to Quantum) is an entirely mechanical means of locking the heads in the landing zone. The AIRLOCK™ consists of an airvane mounted close to the edge of the disk stack with an arm that holds the head stack in the landing zone when the disks are not rotating. As power is applied to the motor and the disk stack starts rotating, an airflow is generated around the disk. As airflow increases, the airvane and its arm rotate, allowing the arm stack to move freely out of the landing zone.

1.3 MODEL Q2080 DRIVE ELECTRONICS

1.3.1 GENERAL FEATURES

This section describes the functions performed by the Model Q2080 drive electronics. Figure 1-5 is a functional block diagram of the Model Q2080 drive electronics. The drive electronics consist of the following circuitry:

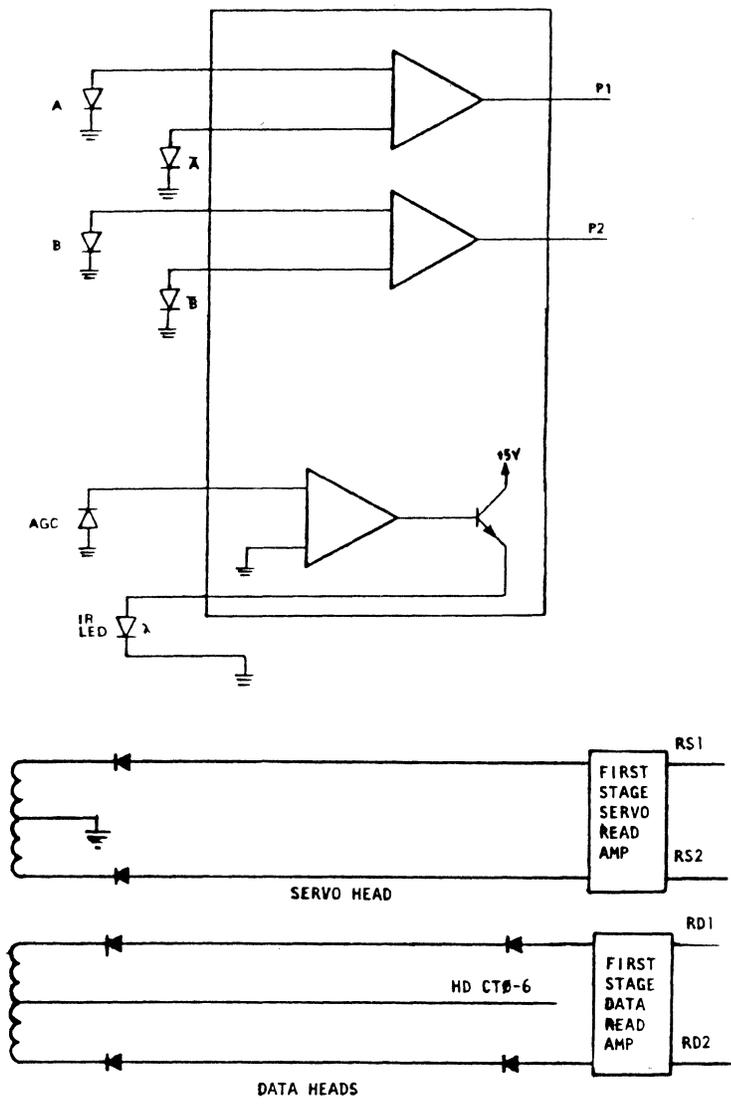
- **Interface Buffers** — These drivers and receivers buffer the control and data signals between the drive and the drive controller.
- **DC Power Circuits** — This circuitry provides decoupling and regulation as well as the power up reset signal.
- **Index Generator** — Using the mechanical sector ring as a reference, input time slots for reading the servo data are generated and an index pulse is provided to the user interface.
- **Read/Write Electronics** — This circuitry provides the write current to record data and the circuits to detect recorded data.
- **Encoder PCB** — This PCB contains the head switching matrix, the servo and data read preamplifier, and the circuits used to generate track signals provided by the scale and optical encoder.
- **Servo Peak Detection** — By using the signals from the factory-recorded servo, this circuitry, in conjunction with the microprocessor, controls fine position correction while on track.
- **Actuator Drive Circuits** — This circuitry provides the power to drive the actuator.
- **Microprocessor** — This single chip processor controls the drive during its various modes of operation. Primarily, it controls the actuator, either by processing servo information when the actuator is on track or by monitoring track crossings to provide velocity feedback when the actuator is moving.



**FIGURE 1-5
DRIVE ELECTRONICS BLOCK DIAGRAM**

1.3.2 ENCODER BOARD

Figure 1-6 is a functional block diagram of the encoder PCB. The board contains the diodes used for head switching, a through bubble connector (for the head signals, actuator drive signals, and actuator position signals), the amplifiers and comparators used to detect the encoder photo cell outputs, and the AGC amplifier used to control the infrared LED drive current.



**FIGURE 1-6
ENCODER PCB BLOCK DIAGRAM**

1.3.3 DRIVE CONTROL BOARD

Figure 1-7 is a functional block diagram of the drive control board. The board is mounted to the top of the drive and connects on one end to the through bubble connector of the transducer PCB. The opposite end of the board provides connectors for the controller data and control signals and DC power. Two additional connectors are provided for the index transducer and the actuator power driver.

Applying AC power to the drive starts the AC motor that rotates the disks. This results in the heads lifting off the disk surface and flying above the landing zone. Applying DC power generates a power on reset by the POR circuit, which resets the microprocessor and all drive logic. Until the rotational speed of the disks exceeds 2,000 RPM, the RESET ONE SHOT keeps the microprocessor reset. Then, the microprocessor waits until the speed reaches approximately 3,000 RPM via the -INDEX line, at which point it waits two seconds for the heads to contact the landing zone. Next, the microprocessor calibrates the P1 and P2 signals by computing center values.

The heads then perform 100 five track seeks and continue to servo on the last seeked track for greater than one second to compute the Null Current Value. The Null Current Value is the current required to keep the actuator motionless. Following this, the heads single step out to Track 0, then the microprocessor sets READY and SEEK COMPLETE. The heads continue to servo on Track 0 until interrupted by a command from the controller.

When DRIVE SELECT "X" is driven true and matches the drive select jumper, the drive select logic enables the interface logic to gate control and data signals to and from the drive. The drive will read or write data on the selected head at the present track depending on the state of the WRITE GATE line. The read/write circuits transfer the MFM data as required.

The drive may be commanded to move the heads by receiving step pulses. The pulses can be sent in one of two modes:

1. Normal mode, in which the step pulses are sent slower than every 1.5 msec.
2. Buffered mode, in which the step pulses are sent faster than every 200 μ sec.

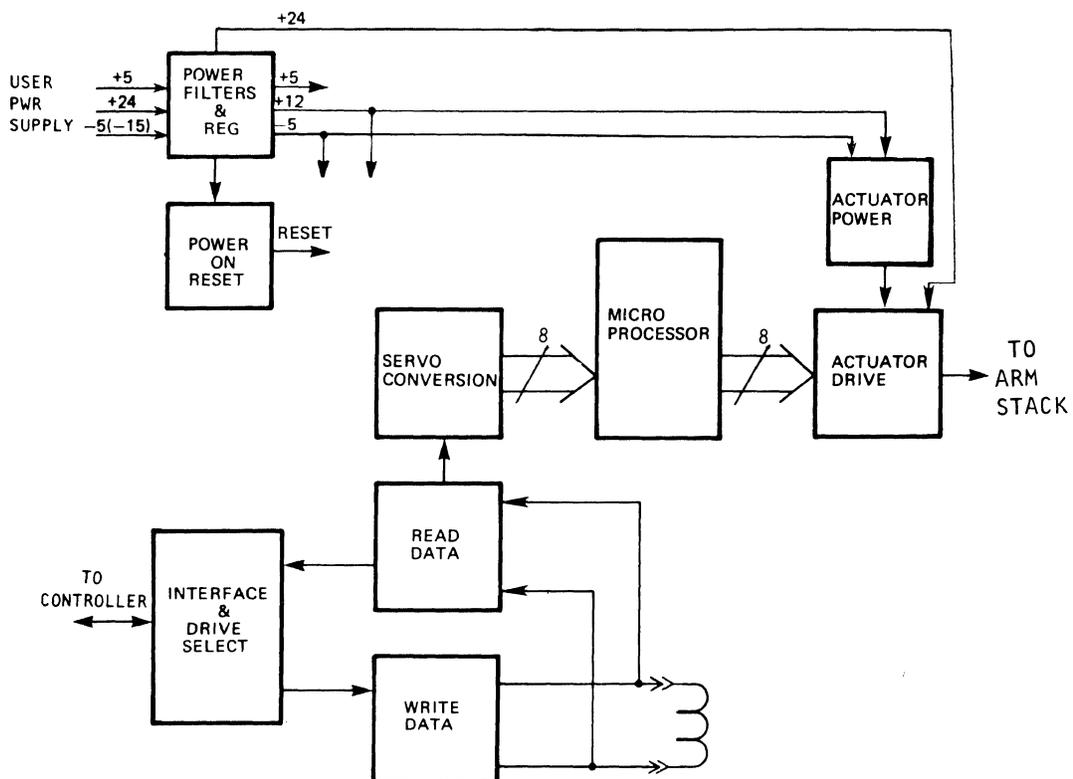


FIGURE 1-7
DRIVE CONTROL PCBA BLOCK DIAGRAM

1.3.4 AGC CIRCUIT

Paragraph 1.2.2 describes the mechanical operation of the transducer scale reticle and photo cell. The AGC window in the reticle provides its photo cell with a large view of the scale in order to sense an average of the amount of light striking any of the other cells. Figure 1-8 is a simplified schematic of the AGC circuit.

Amplifier U1 drives the base of Q1 that provides the current for the infrared LED. R1 is adjusted at the factory to provide the proper signal amplitude out of the track position amplifiers. Once R1 is adjusted, the amount of light produced by the LED depends on the amount of light seen by the AGC photo diode. If the photo diode output decreases (less light seen) amplifier U1 output increases and Q1 conducts harder, passing more current to the LED which outputs more light until the circuit stabilizes again. In this way, the signal amplitude of the other photo diodes remains constant over the entire scale, compensating for aging and variations in temperature and voltage.

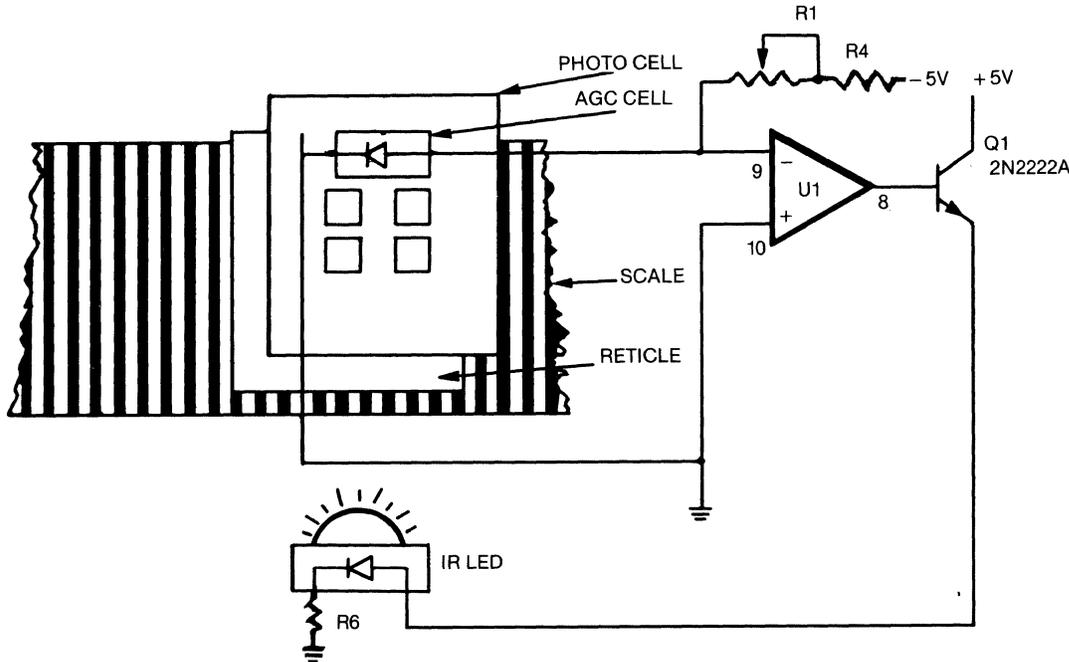
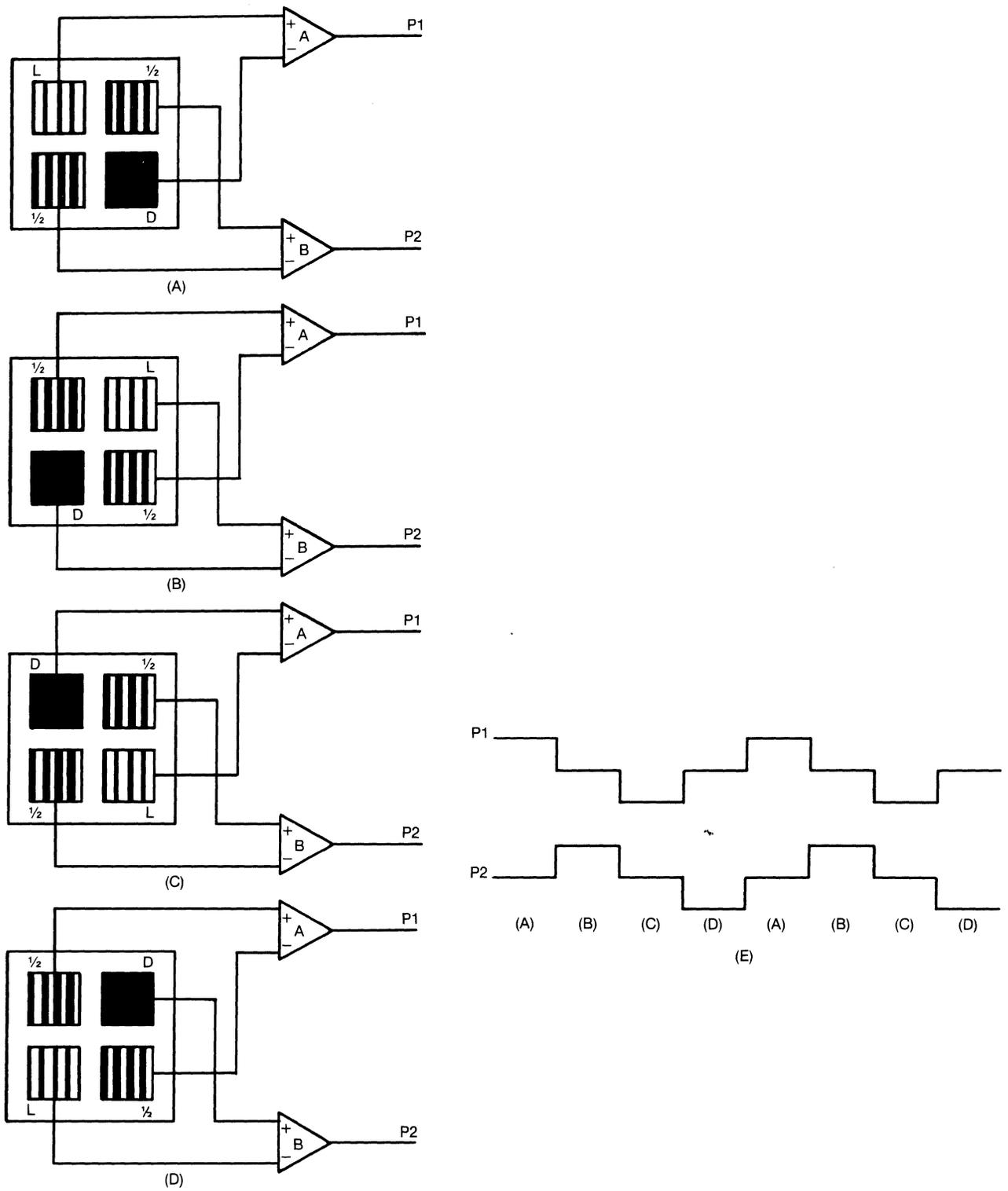


FIGURE 1-8
SIMPLIFIED AGC CIRCUIT

1.3.5 P1 AND P2 GENERATION

The P1 and P2 signals are used to determine coarse track position and track crossing. As seen on the simplified schematic in Figure 1-9A, one pair of photo cells (connected to comparator A) are in opposite states. The cell with no light results in minimum voltage to the inverting input and the cell with maximum light results in maximum voltage to the non-inverting input. With these inputs comparator A outputs maximum positive voltage at P1. On the other hand, the cells connected to comparator B see equal light and therefore result in equal voltages to both inputs of comparator B. This results in a zero voltage output at P2. Moving the scale to the next state gives the conditions shown in 1-9B. Here comparator A has equal inputs, hence, zero output at P1. Comparator B has maximum voltage on the non-inverting input and zero voltage on the inverting input, resulting in a maximum positive output at P2. Moving the scale again gives the condition shown in 1-9C. Once again, comparator B sees equal inputs and P2 is zero volts. Comparator A has different inputs, but they are in the opposite state from 1-9A; here there is maximum voltage at the inverting input and minimum voltage at the non-inverting input. This results in a maximum negative output from comparator A at P1. Figure 1-9D shows the last of the four possible conditions. Here we have no output at P1 and maximum negative output at P2. The waveforms in Figure 1-9E illustrate the outputs from P1 and P2 that would occur with the scale constantly moving in one direction. The scale and reticle are etched in such a way that the zero voltage point of the P1 or P2 waveform indicates a track center. Therefore, the disk contains four tracks in the space between the beginning of one scale line and the beginning of the next scale line.

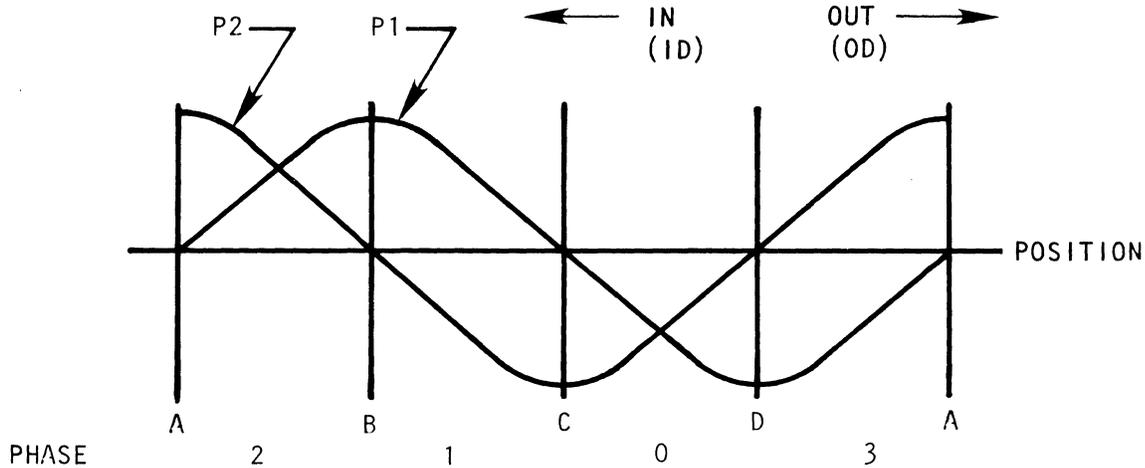


**FIGURE 1-9
P1 AND P2 GENERATION**

1.3.6 COARSE SEEK POSITIONING

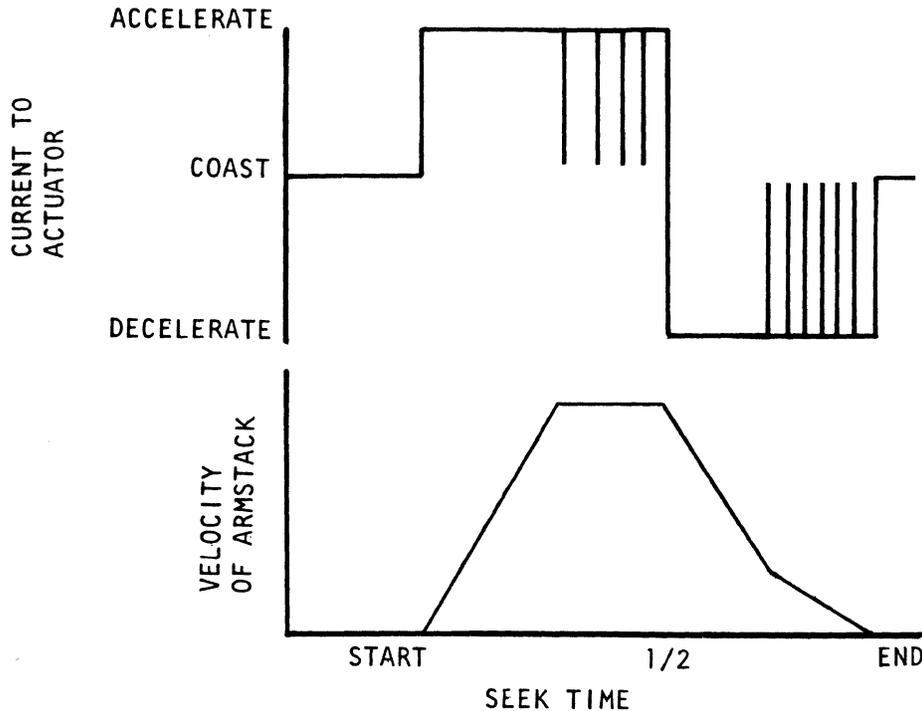
The microprocessor of the Q2080 uses the P1 and P2 signals for track crossings and coarse position settling during seeks. Following coarse positioning, the Q2080 reads servo bursts for fine positioning. The drive performs coarse seeks in two modes: slow mode seeks (seeks of more than six tracks), a single step mode seeks (1-6 step bursts with step rate less than $200\mu\text{sec}$ or single STEP pulse of greater than 1.5 msec).

The last STEP pulse, when STEP pulses are sent in slow mode, results in a full current pulse to the actuator for the direction set by the direction bit. During the start of the seek, the microprocessor looks at zero crossings of P1 and P2 to compute track crossings (see Figure 1-10 at points A, B, C, and D). During longer seeks, once the arm stack gains speed, the microprocessor only looks at zero crossings for P1 or P2. This results in detection of track crossings every two tracks.



**FIGURE 1-10
P1 AND P2 SIGNALS VS. POSITION**

To decelerate the arm stack during slow mode seeks, the microprocessor sends the actuator full current in the opposite direction once approximately half of the seek has been completed (See Figure 1-11).



**FIGURE 1-11
ACTUATOR CURRENT DURING SEEK**

When the velocity of the arm stack drops during deceleration, the microprocessor returns to single track zero crossing detection. Then, when the seek is within three tracks of completion, the microprocessor switches to an angle mode of seek (see Figure 1-12). The microprocessor controls positioning by monitoring the angle ($\arctan \frac{P1}{P2}$) until reaching the reference angle. Finally, the microprocessor switches to AB servo positioning for fine settling.

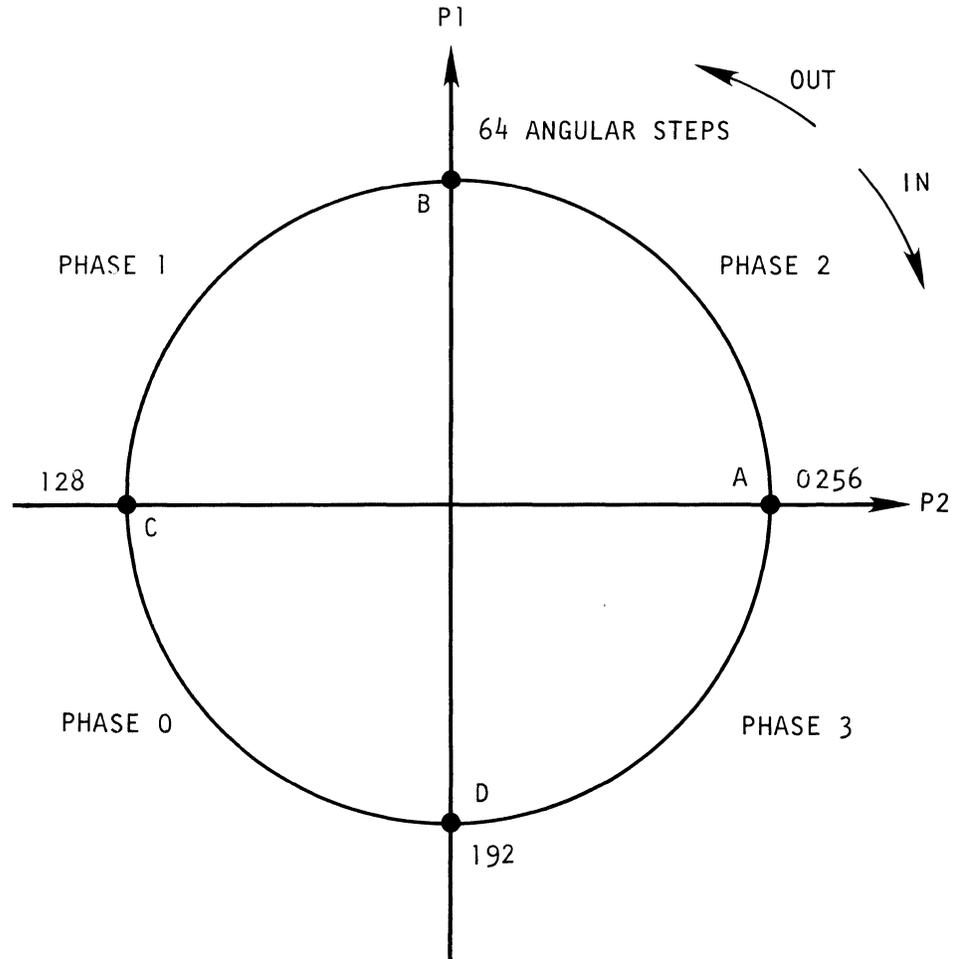


FIGURE 1-12
ANGULAR POSITIONING: P1 VS. P2

During single step mode seeks, the microprocessor reads the present angular position, adds 64 angular steps in the direction needed (64 angular steps = 90°), and calls that position the new reference angle. The microprocessor then sends current to the actuator to drive towards the point where the actual angle minus the reference angle equals zero. This point completes a single step. The microprocessor repeats this procedure until completing all single steps and then switches to AB servo positioning for fine settling.

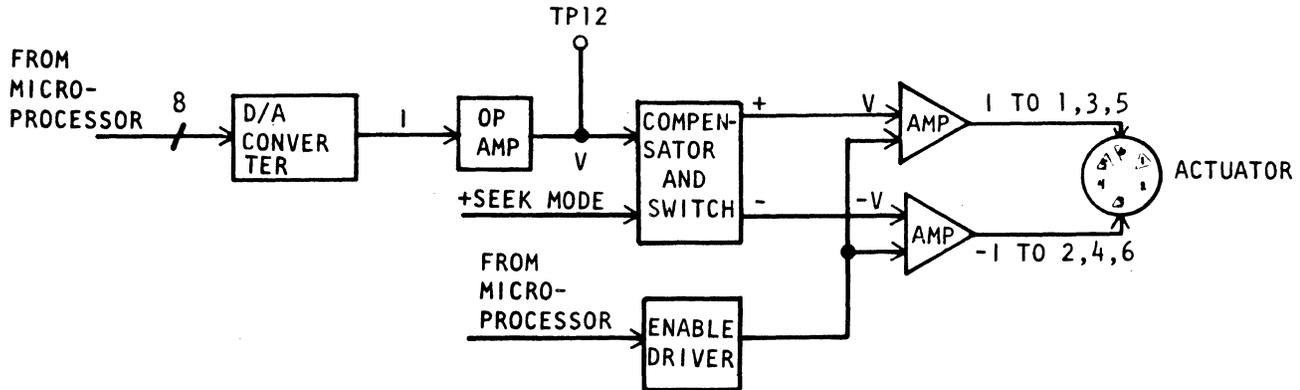
1.3.7 ACTUATOR DRIVE CIRCUITS

The block diagram in Figure 1-13 summarizes the actuator drive circuits. The microprocessor enables power to the amplifiers at power up via the enable driver. Additionally, the microprocessor generates a series of 8 digital line signals that correspond to specific currents to the actuator, as shown in Table 1-1.

**TABLE 1-1
D/A ACTUATOR SIGNALS**

DIGITAL	CURRENT
11111111	FULL OUTWARD CURRENT
10000000	ZERO CURRENT
00000000	FULL INWARD CURRENT

A D/A converter transforms the eight digital lines to a current that an op amp converts to voltage (TP 12). The voltage goes into a lead-lag compensator to stabilize the loop. Finally, the compensator output passes through voltage to current amplifiers that sent current to the actuator.



**FIGURE 1-13
ACTUATOR DRIVE BLOCK DIAGRAM**

Figure 1-14 illustrates the actuator enable driver circuit. This circuit prevents the heads from moving during power sequencing.

When the +5V line is greater than 3.5V and the +12V line is on, transistor QA12 turns on, drawing current through R98. This turns on transistor Q11 supplying +12V to U9D, U7D, and the Zener CR12, which regulates to +6V to provide V_{REF} . When the -5V and +5V lines are on, R106 receives sufficient current to turn on transistor Q13, supplying negative voltage to U9D and U7D.

When the ENABLE DRIVER line is LO, V_i equals 0V, which turns off transistors Q11, Q12, and Q13. This disables power to U9D and U7D. When the ENABLE DRIVER line is HI, the 7407 (U4B) becomes an open collector and is taken out of the circuit, allowing V_i to rise to the voltage required to turn on transistors Q11, Q12, and Q13. This enables power to U9D and U7D.

The circuits for the actuator compensator are shown in Figure 1-15. The compensator operates when SEEK MODE is off. Switches S1, S2, and S3 switch compensation in and out. When compensation is switched in, the TP12 voltage is unity gain amplified through OA1 (U9D pins 12, 13, 14) which can function as a summing block to measure loop gain. Next, the signal is low pass filtered at OA2 to lower mechanical resonance. Finally, the signal passes through OA3, getting a phase lead to provide phase margin for the loop response.

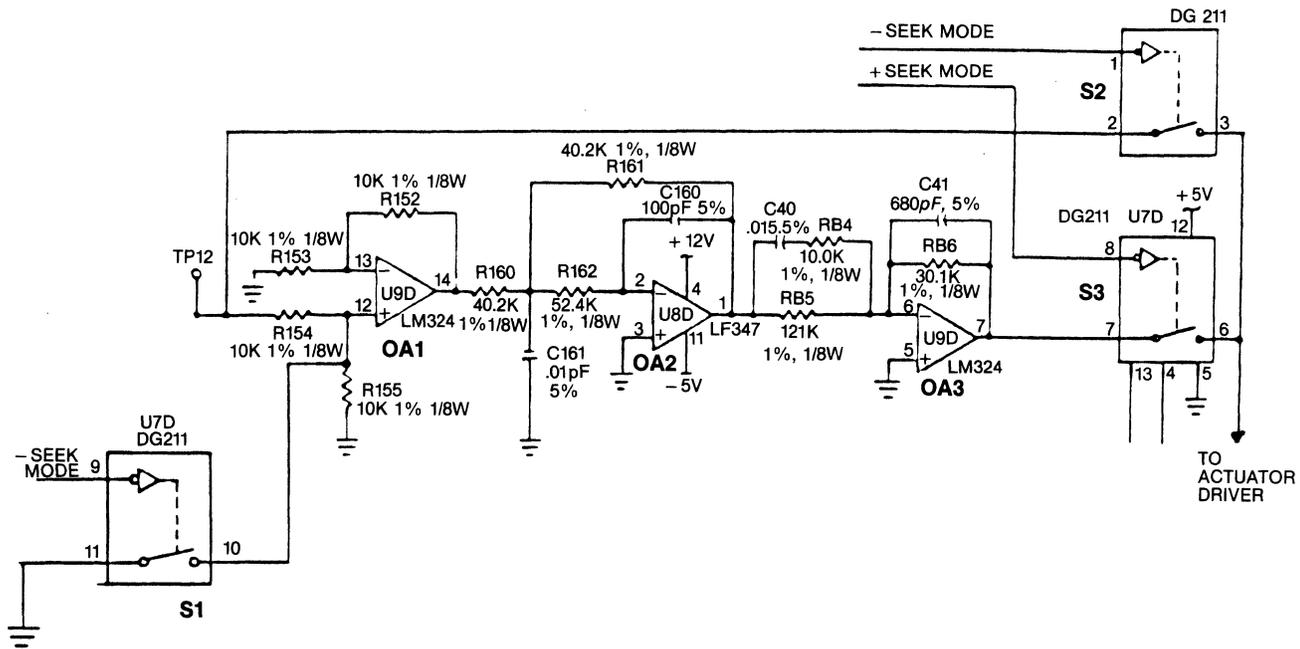


FIGURE 1-15
ACTUATOR COMPENSATOR

Figure 1-16 illustrates the actuator drive circuits. The actuator driver receives V_i input from the compensator. The voltage converts to current I_o according to $I_o = -2V_i$. V_{REF} equals +6V, which goes to the + input of the TDA2030 power op amp. Because of the high gain the input of the TDA2030 also equals +6V.

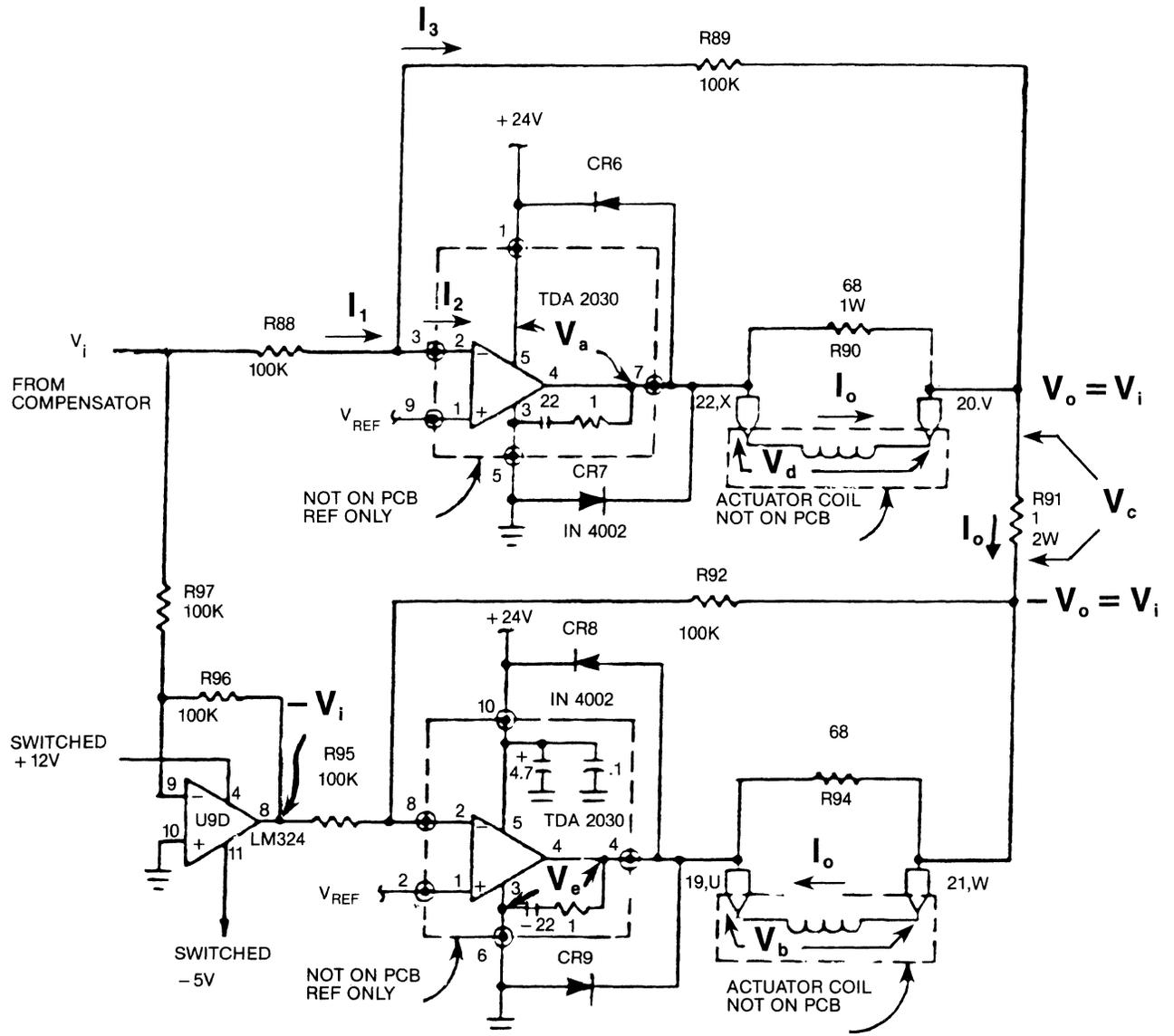


FIGURE 1-16
ACTUATOR DRIVE CIRCUITS

The following summarizes the voltage and current relationships in this circuit:

$$I_2 = 0, \text{ therefore } I_1 = I_3$$

$$I_1 = \frac{V_i - 6V}{R88} = I_3 = \frac{6V - v_o}{R89}$$

$$\text{Since } R88 = R89, \text{ then } V_o = 12V - V_i$$

A similar analysis shows that the voltage at the other side of R91 is $V_o = 12V + V_i$.

$$\text{Therefore, } I_o = \frac{(12V - V_i) - (12V + V_i)}{1\sim} = \frac{-2V_i}{1\sim} = -2V_i$$

In summary, for any voltage V_i , a current of $-2V_i$ runs through the actuator coils to generate a torque. For example,

$$V_i = .5V$$

$$I_o = -1 \text{ amp (produces an outward torque)}$$

I_o flows from V_e ground end to V_d then V_c , V_b , and V_a back to 24V.

When $V_i = -1.5V$, pin 4 of TDA2030 goes to $24V - V_a$ (V_a is a saturated transistor).

$$\text{From Figure 1-16, } V_a + V_b + V_c + V_d + V_e = 24V$$

$$\text{When saturated } \frac{V_a}{I_o} \approx \frac{V_e}{I_o} \approx 1\sim \text{ (saturated output transistor of TDA2030)}$$

$$\frac{V_b}{I_o} \approx \frac{V_d}{I_o} \approx 5\sim @ 25^\circ C$$

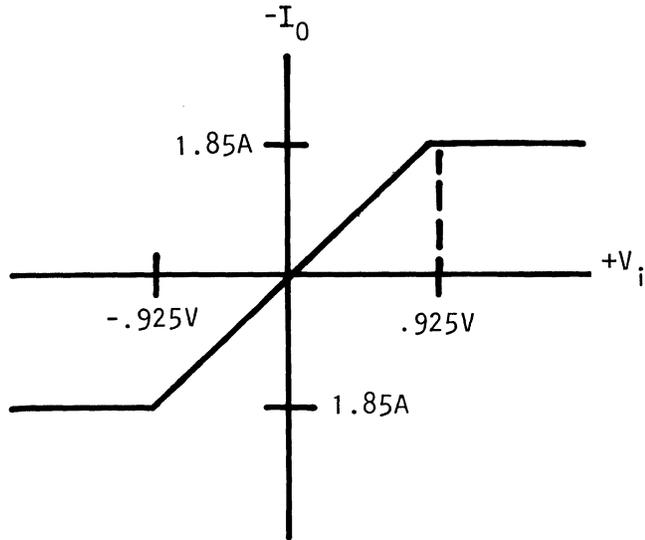
$$\frac{V_c}{I_o} = 1\sim (R91)$$

$$\frac{V_a}{I_o} + \frac{V_b}{I_o} + \frac{V_c}{I_o} + \frac{V_d}{I_o} + \frac{V_e}{I_o} = \frac{24V}{I_o}$$

$$13 = \frac{24}{I_o} \quad I_o \approx 1.85A @ 25^\circ C \text{ (produces an inward torque)}$$

In summary, a positive V_i produces an outward motion (toward TK0) and a negative V_i produces an inward motion (toward TK1171).

The transfer function of the actuator drive circuit is shown in Figure 1-17. In this circuit when V_i is greater than approximately .925V (at $25^\circ C$), I_o does not increase further because the voltage source is limited to 24V.



APPROX. @ 25°C
 DECREASES WITH RISING TEMPERATURE
 BECAUSE OF ROTOR RESISTANCE

**FIGURE 1-17
 ACTUATOR DRIVE CIRCUIT
 VOLTAGE/CURRENT RELATIONSHIP**

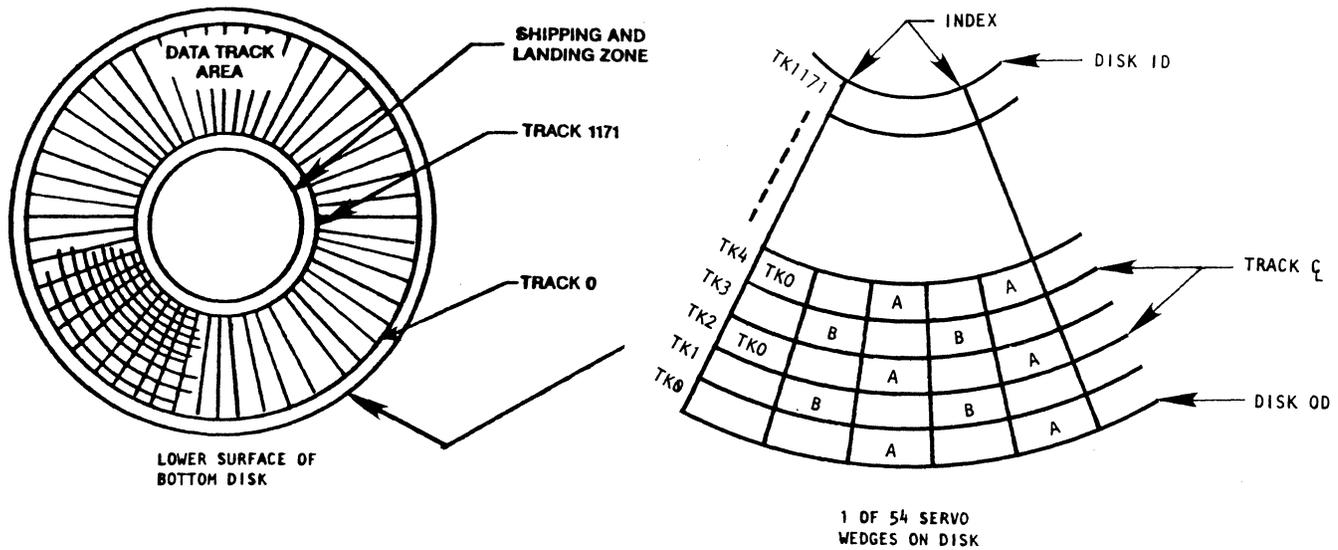
1.3.8 SERVO READ AND CONVERSION CIRCUITS

The lower surface of the bottom disk stores servo bursts that reference all fine positioning moves. The disk is divided into 54 wedges, as shown in Figure 1-18. Each of the 1172 tracks in a wedge repeats the pattern of servo bursts shown in Table 1-2.

**TABLE 1-2
 SERVO BURSTS**

Burst	Duration
A burst	72 μ sec
B burst	72 μ sec
A burst	72 μ sec
B burst	72 μ sec
TK0 burst*	(index-to-index time) - (4) (72 μ sec)
	$\frac{20.38 \text{ msec}^{**}}{54} - (4) (72 \mu\text{sec}) = 89 \mu\text{sec}$

*all tracks except Track 0
 **nominal disk speed



**FIGURE 1-18
SERVO WEDGES**

The servo read and conversion circuits detect the servo bursts and convert this analog information into digital values that are used by the microprocessor to position the heads on the track center. Figure 1-19 shows a functional block diagram of the servo circuits. The actual circuitry is found in Figure 2-6.

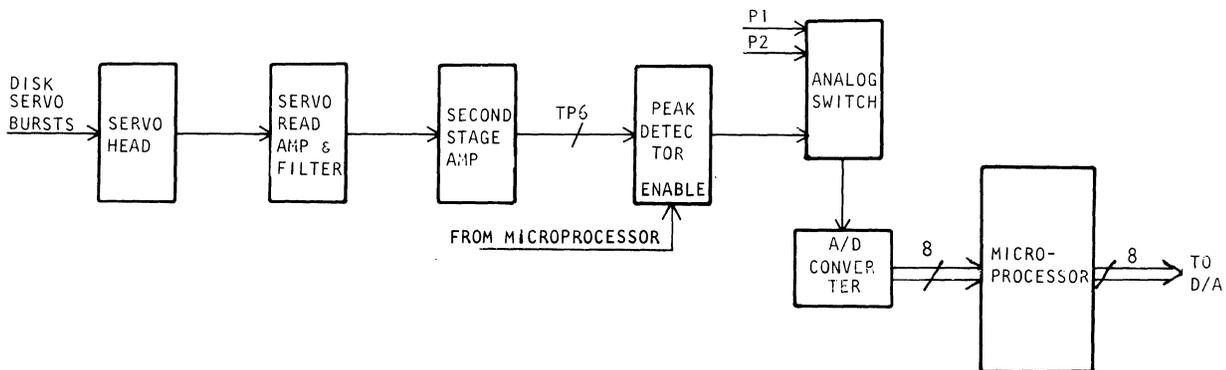
Consult the block diagram to reference the following summary of the servo circuitry. The servo head reads servo bursts and sends the signal through an amplifier on the encoder board. Next, a filter attenuates the high frequency noise, which then passes through a second stage amplifier on the main board. The filtered and amplified signal is peak detected with timing controlled by the microprocessor. Finally, an A/D converter transforms the AB peak detected bursts from an analog signal to an 8 line digital signal that goes to the microprocessor.

The microprocessor reads the A burst and compares it to the last B burst using the formula:

$$\frac{32 (A-B)}{A + B} \text{ if on an odd track}$$

$$\frac{32 (B-A)}{A + B} \text{ if on an even track}$$

The microprocessor outputs digital values to the D/A converter, which converts them to an analog voltage. Finally, the actuator driver converts the analog voltage signal to a current to move the actuator.



**FIGURE 1-19
SERVO CIRCUITRY BLOCK DIAGRAM**

The circuits for the servo read amp and filter are shown in Figure 1-20. In this circuit U3(NE592) amplifies the servo read signal, which then passes through a differential filter to eliminate data write crosstalk at frequencies greater than 542 KHz. Next, the signal is AC coupled by C12, C13, R37, and R38, and further amplified by UIC (NE592). Finally, C14 and R39 AC couple at approximately 80 KHz and R41 and C15 roll off at about 1.0 MHz to band pass the signal.

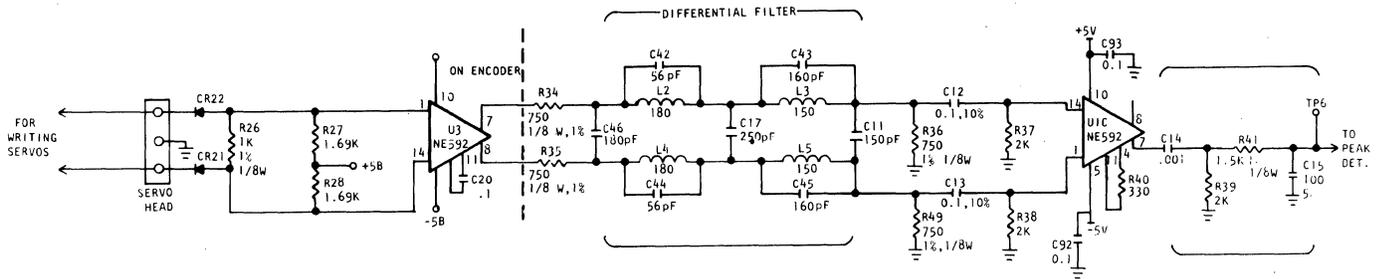


FIGURE 1-20
SERVO READ AMP AND FILTER CIRCUITS

The Servo Peak Detector (Figure 1-21) takes a 540 KHz sine wave input and finds the greatest positive voltage. The peak voltage is amplified (3X) and held in capacitor C16. The Reset Peak Detector Gate U1J (7406) receives input from the microprocessor and resets C-16.

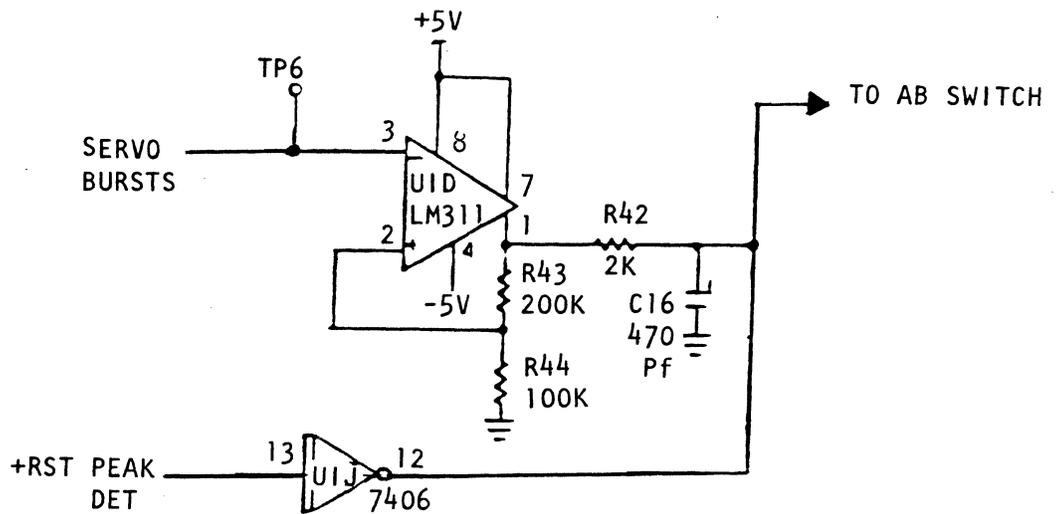


FIGURE 1-21
SERVO PEAK DETECTOR

Figure 1-22 illustrates the servo A/D conversion circuits. The A/D circuit consists of an AM2502 successive approximation register (SAR), a DAC0800 D/A converter, a LM311 comparator, a 74LS540 octal tri-state inverter, and a LM336 2.5V reference. The SAR analyzes the analog signal in a series of 8 successive approximations to convert the analog signal to an 8 line digital signal.

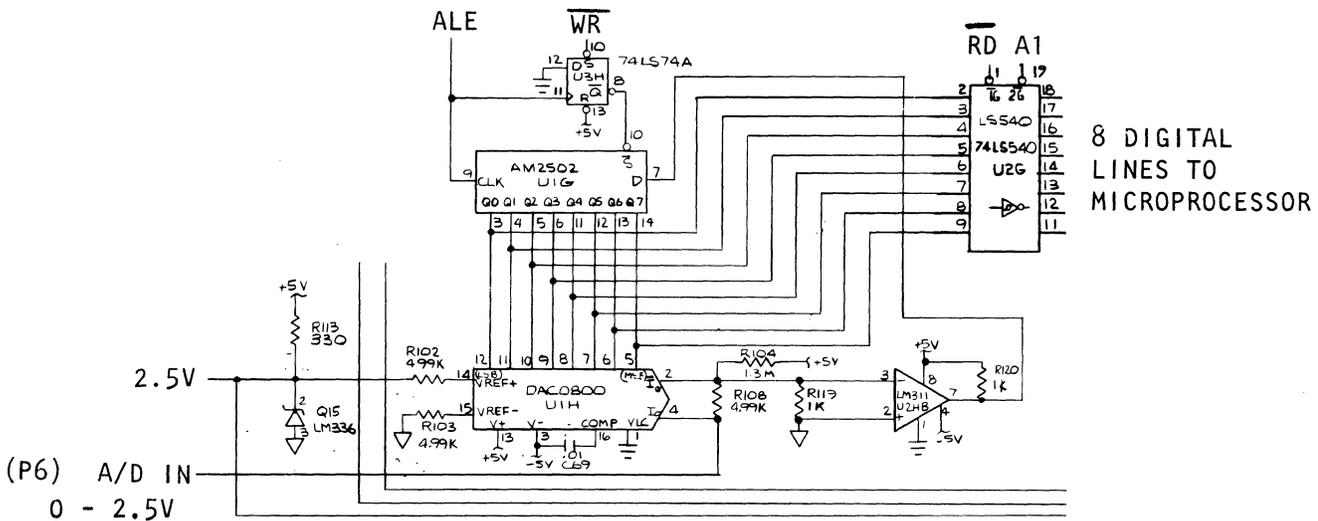


FIGURE 1-22
SERVO A/D CONVERSION

The A/D conversion starts when \bar{S} (START NOT) goes LO. This occurs every time the microprocessor issues a WRITE command as shown in Figure 1-23.

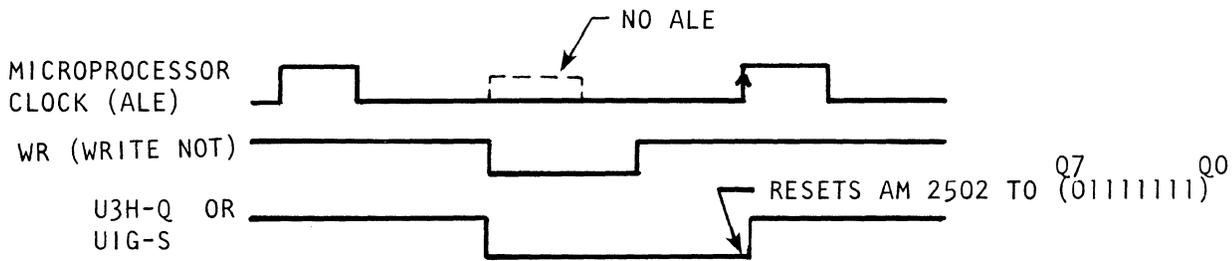


FIGURE 1-23
A/D RESET

Following the reset, the AM2502 issues a digital word corresponding to half full-scale $^{Q7}_{(01111111)}^{Q0}$. The D/A converter transforms the half full-scale digital signal into a half full-scale analog voltage ($\frac{2.5V}{2}$) which equals $I_0 R108$. Next, the LM311 comparator examines the voltage at pin 3 ($\approx V_1 - I_0 R108$). If the voltage is positive, then V_1 is greater than $\bar{I}_0 R108$ and the D line to the SAR is LO, indicating that voltage in is greater than half full-scale. The SAR saves the Q7 LO signal and inverts the signal through the 74LS540, which sends the microprocessor a HI (>half full-scale) signal. This process repeats for the next 7 bits (through Q0) of the digital signal.

1.3.9 DATA INTERFACE

The function of each of the five (5) data signals is described below:

- **MFM WRITE DATA** — Provided there is a LO level on the WRITE GATE control line the transition of the + MFM WRITE DATA line more positive than the -MFM WRITE DATA line will cause a flux reversal to be written on the disk. During read operations the + MFM WRITE DATA line must be held more negative than the -MFM WRITE DATA line. Figure 1-24 shows the write data timing.

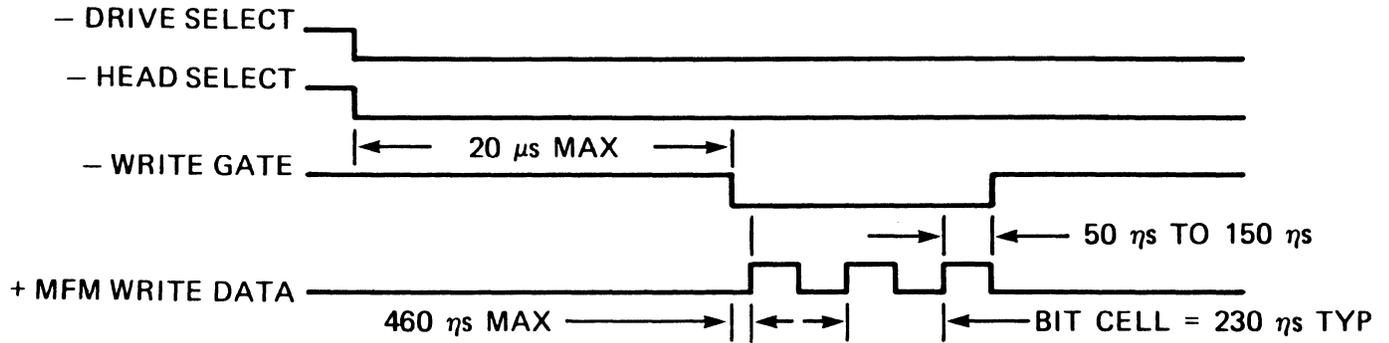


FIGURE 1-24
MFM WRITE DATA TIMING

- **MFM READ DATA** — Provided there is a HI level on the WRITE GATE control line, the transition of the + MFM READ DATA line more positive than the -MFM READ DATA line indicates a flux reversal was detected on the track. Figure 1-25 shows the read data timing.

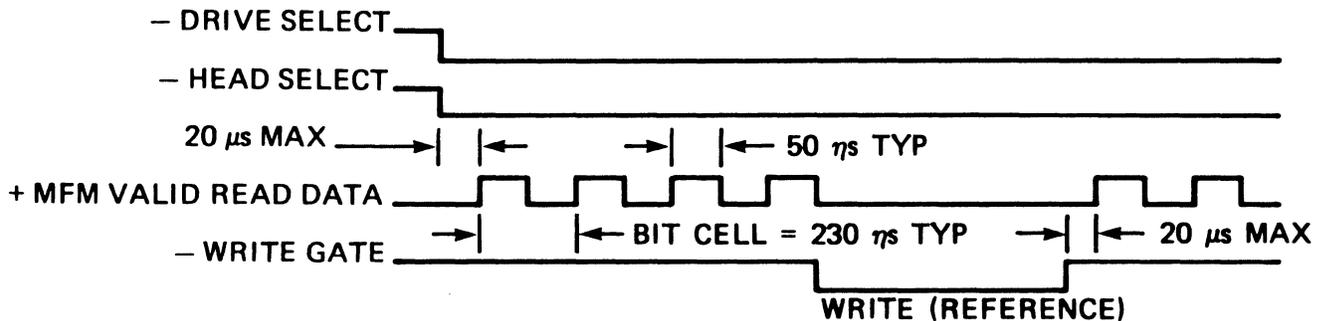


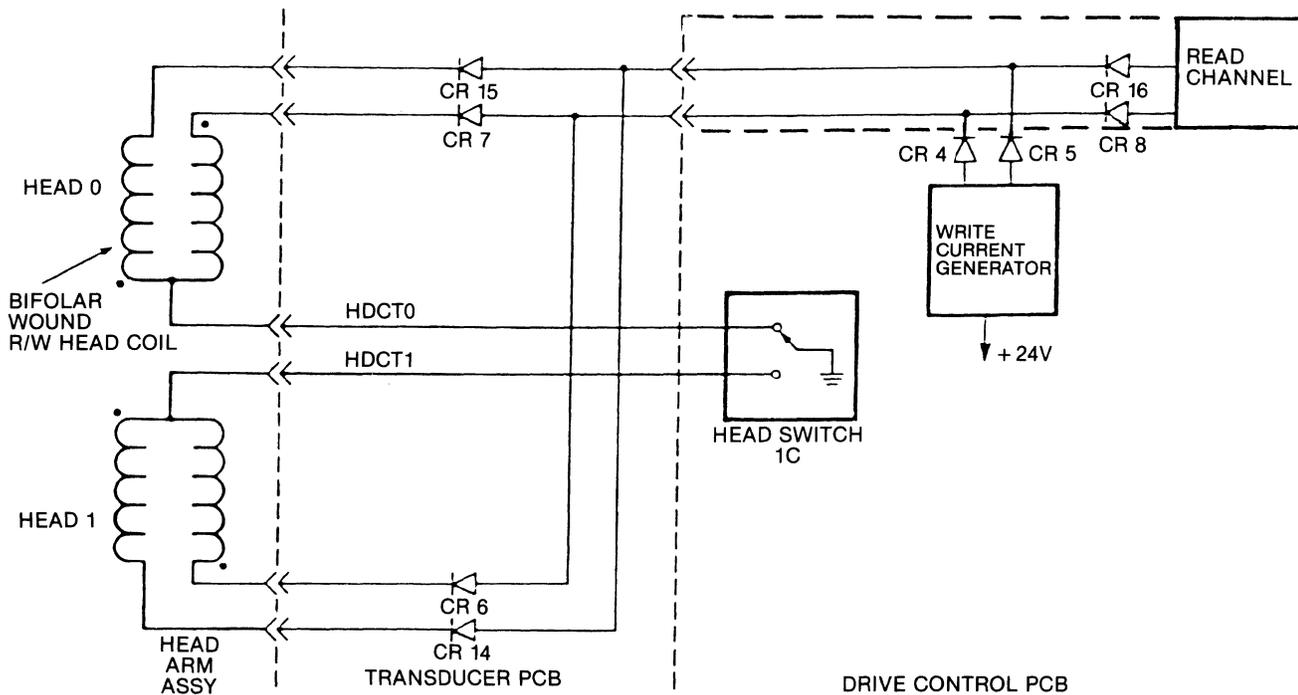
FIGURE 1-25
MFM READ DATA TIMING

- **DRIVE SELECTED** — This open collector line will go to a LO level when this drive is selected by the appropriate drive select line.
- **RADIAL SEEK COMPLETE** — Select this output by installing Jumper D at PCB location J1. When selected, a LO level on this line indicates the R/W heads have settled at a cylinder and a read, write or another seek may take place. This signal is not gated with drive select.
- **RADIAL INDEX** — Select this output by installing Jumper H at PCB location J1. When selected, a LO pulse of 10 μsec duration on this line indicates the beginning of a track. This signal is not gated with drive select.

1.3.10 HEAD SWITCHING MATRIX

Figure 1-26 is a simplified schematic of the head switching diode matrix for two heads. Refer to Figure 2-2 for the actual matrix used.

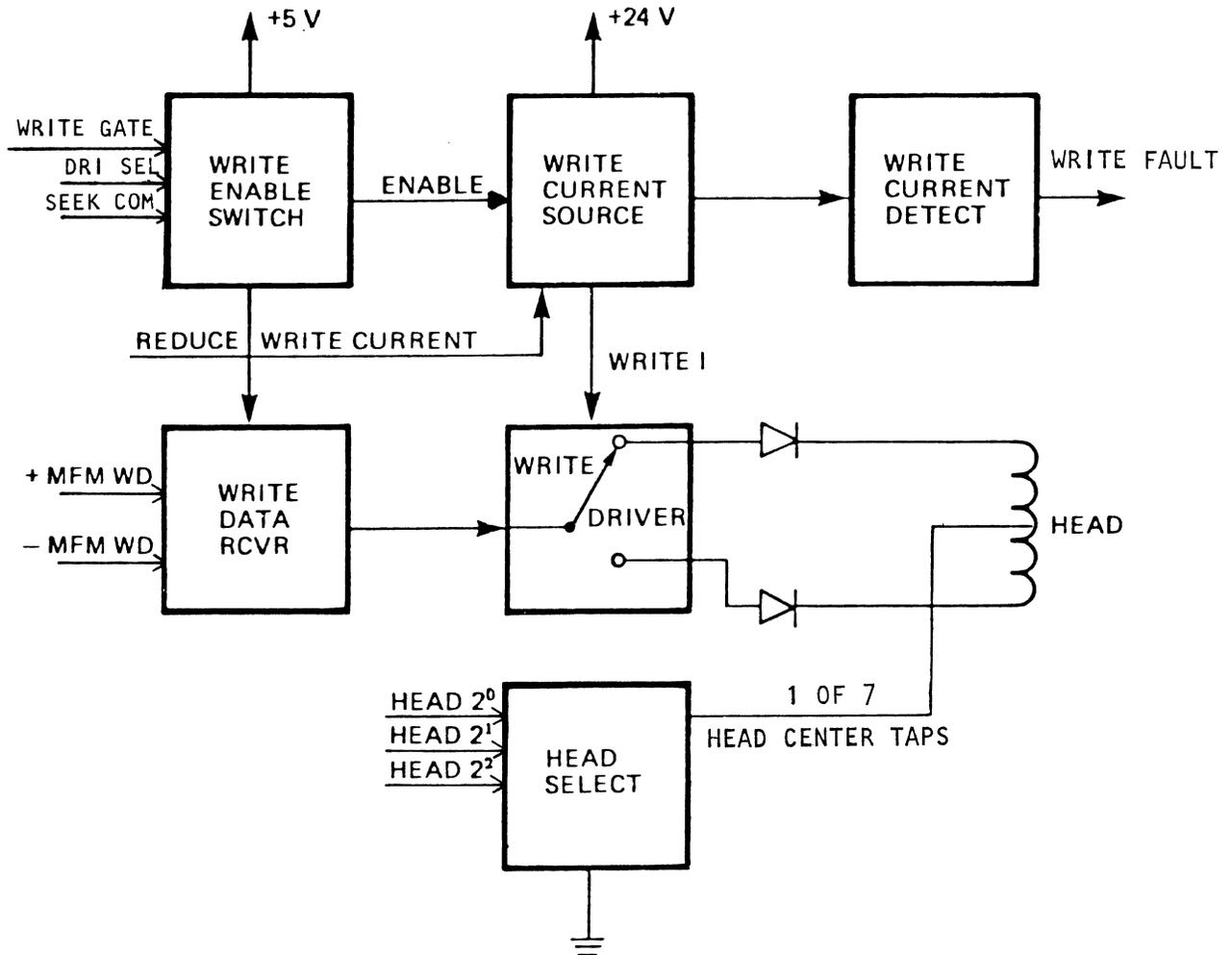
Diodes CR7, CR6, CR14 and CR 15 are part of the head switch matrix. When the head switch IC grounds the head centertap (HDCT0-6) the selected head is connected to the Read/Write circuits via one of the diode pairs. None of the other diode pairs is forward biased, therefore, the other heads are isolated from the selected head. Diodes CR5 and CR4 through CR16 and CR8 are part of the Read/Write circuits and are used to isolate the Read and Write circuits from each other. See paragraphs 1.3.8 and 12.



**FIGURE 1-26
HEAD SWITCHING MATRIX**

1.3.11 WRITE DATA CIRCUITS

Figure 1-27 is a functional block diagram of the write circuits found in the Q2080. The write enable circuit ensures that the +5V logic voltage is present; that the drive is selected, on track, and READY; and that the WRITE GATE is active. When these conditions are met the write enable switch turns on the write current source.



**FIGURE 1-27
WRITE CKT BLOCK DIAGRAM**

This constant current source provides the write driver with 18 mA of write current. The circuit also provides a current-on signal that is used by the write current detector to set the write fault flip-flop. The write driver receives its switching input from the write data receiver. The write driver switches the write current into one end or the other end of the head coil whose center tap has been grounded by the head select switch. The head select switch then grounds the selected head center tap.

Figure 1-28 is a simplified schematic of the write enable switch which is shown in greater detail on Figure 2-2, location A and B, 5 through 8. The logic to generate +WRITE is found on Figure 2-2, location A and B, 1 through 8. Transistor Q3 is the current enable switch that will turn on when current flows through R9, causing Q3's base to be less positive than its emitter. In order for current flow in R9 transistor Q4 must conduct. Q4 conducts when the +5V is greater than 3.5V due to the action of R13, the base emitter junction of Q4, and CR12 (3.0V zener diode); and the +WRITE signal is true. The +WRITE signal will only be true if all of the following conditions are met:

1. The drive is selected (U4F-4HI)
2. WRITE GATE is true (U4F-5HI)
3. SEEK COMPLETE is true (U4D-2HI)

When these conditions are met, current is supplied to the constant current source Q2 via the current setting resistor R15. Diodes CR3 and CR16 set a reference voltage across R15 and Q2 to maintain a constant current flow through Q2 during voltage fluctuations of the +24V supply. Resistors R17 and R20 provide a current path for the write driver to shut off when Q3 is turned off. The write driver switches the write current between the windings of the selected head.

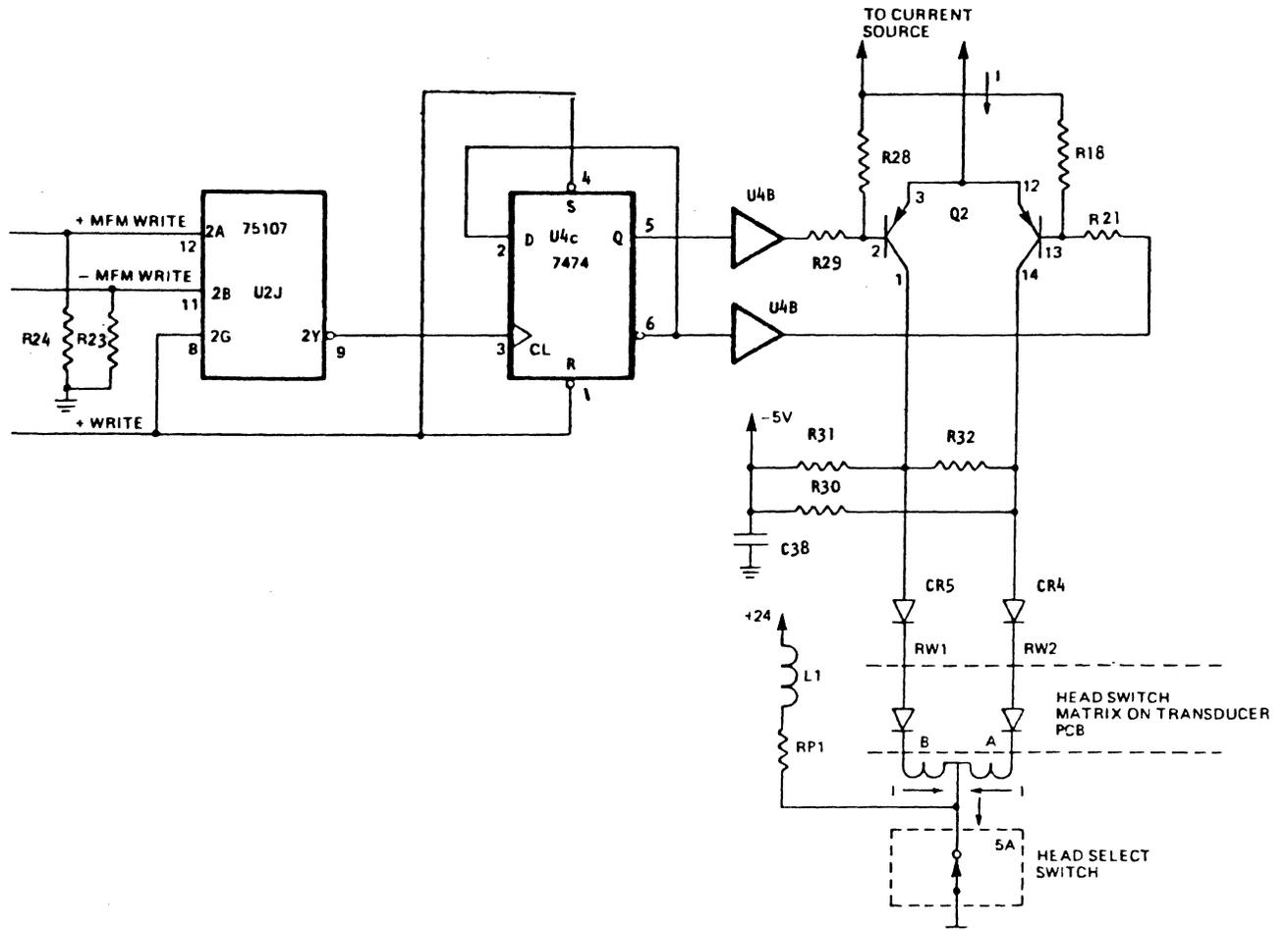


FIGURE 1-29
WRITE DATA RECEIVER AND SWITCH

Figure 1-30 illustrates the write circuit detector used to trigger the write fault flip-flop U4C. The circuit is at 2B on Figure 2-2. Transistor Q2 (8,9, and 10) remains in the off state until current flows through R9. The positive to negative drop across R9 causes Q2 to turn on, allowing current to flow through R11 and R16 to ground. This will clock the write fault flip-flop U4C, which is set if the WRITE GATE signal is not true (HI) and the drive is selected.

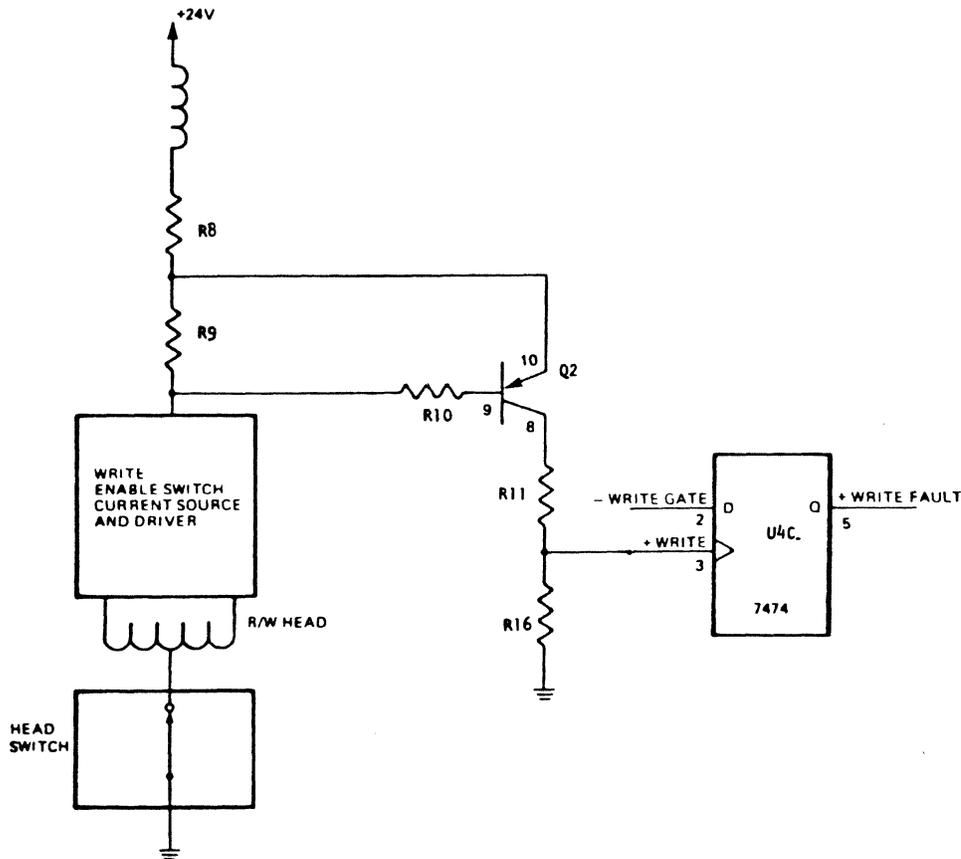
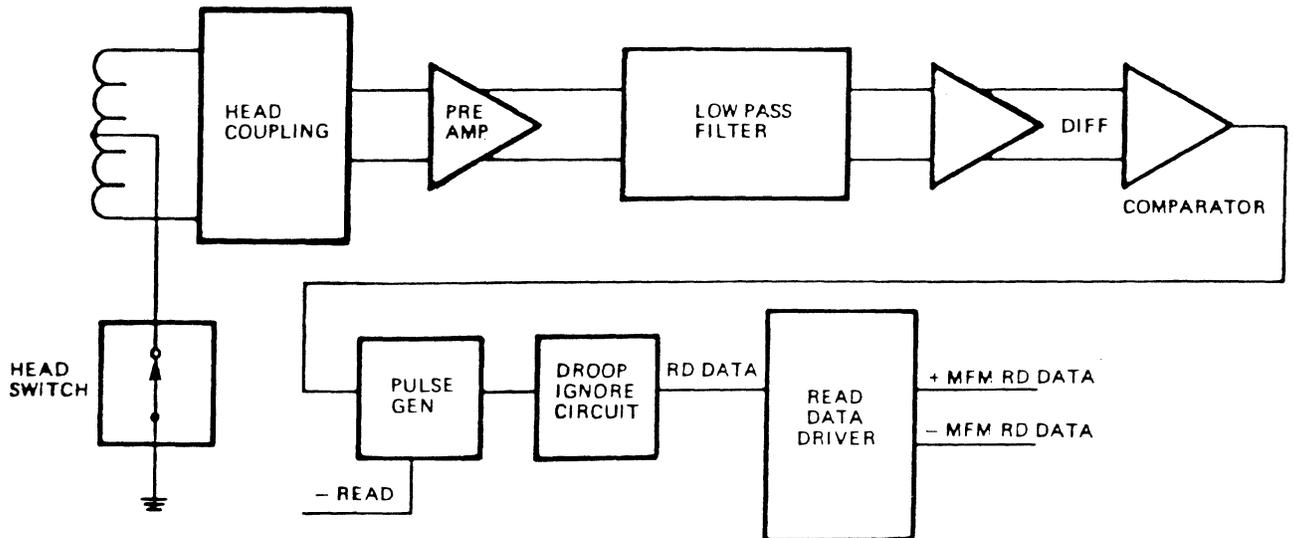


FIGURE 1-30
WRITE CURRENT DETECTOR

1.3.12 READ DATA CIRCUITS

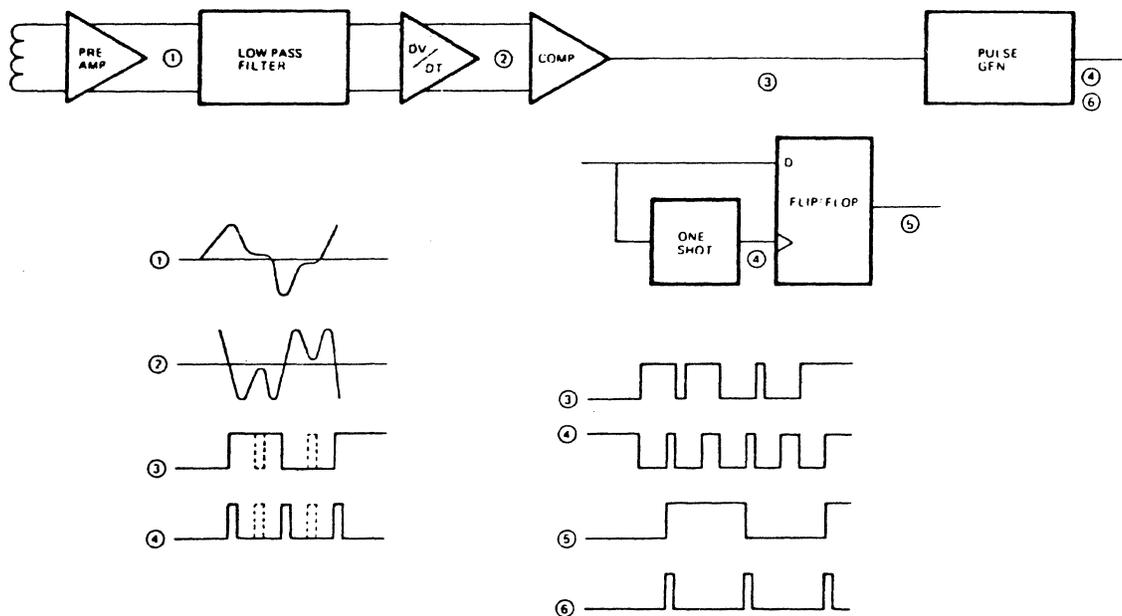
The block diagram in Figure 1-31 illustrates the functional areas of the Q2080 read channel. When the head select switch connects the center tap of the selected head to ground, the diodes in the head coupling network become forward biased. Magnetic flux changes then pass by the head coil inducing current into the coil. This current is coupled through the head coupling diodes and appears as small differential voltage changes at the input of the pre-amplifier. The pre-amplifier boosts these changes, which then travel through a low pass filter to eliminate unwanted high frequency noise. The signal is again amplified and filtered before being input to the differentiator, which converts the voltage peaks of the signal to zero voltage crossings. These zero voltage crossings represent the flux changes read from the disk. They are input to a comparator which converts the sinusoidal signal to a square wave to drive a pulse generator. This pulse generator is enabled whenever the drive is not writing and will output a pulse each time its input switches. A droop ignore circuit filters the pulse train and sends it to a differential line driver. The outputs of the line driver is the \pm MFM READ DATA sent to the controller via the 20 conductor data cable.



**FIGURE 1-31
READ CHANNEL BLOCK DIAGRAM**

The droop ignore circuit eliminates false data pulses from the pulse train. These false pulses may be generated when the differentiated signal droops toward zero volts while reading low frequency data patterns and noise causes the signal to cross zero between legitimate bits. Figure 1-32 illustrates the effect and the function of the droop ignore circuit.

Signal 1 shows an amplified IF pattern, which after filtering and differentiating looks similar to 2. Where signal 1 had a slow rate of change (between flux changes) the differentiated signal droops toward zero volts. The output of the comparator should be as shown by the solid line in signal 3. However, noise in the read channel could cause the droops in signal 2 to cross zero volts, giving the extra pulses shown by the dashed lines in 3. The result would be extra bits in the output signal 4. Adding a one-shot and the flip-flop (droop ignore) between the comparator and the pulse generator prevents the extra pulses from triggering the pulse generator. Signal 5 is now the pulse generator input and the resulting output is signal 6 with no extra bits.



**FIGURE 1-32
READ DROOP AND DROOP IGNORE**

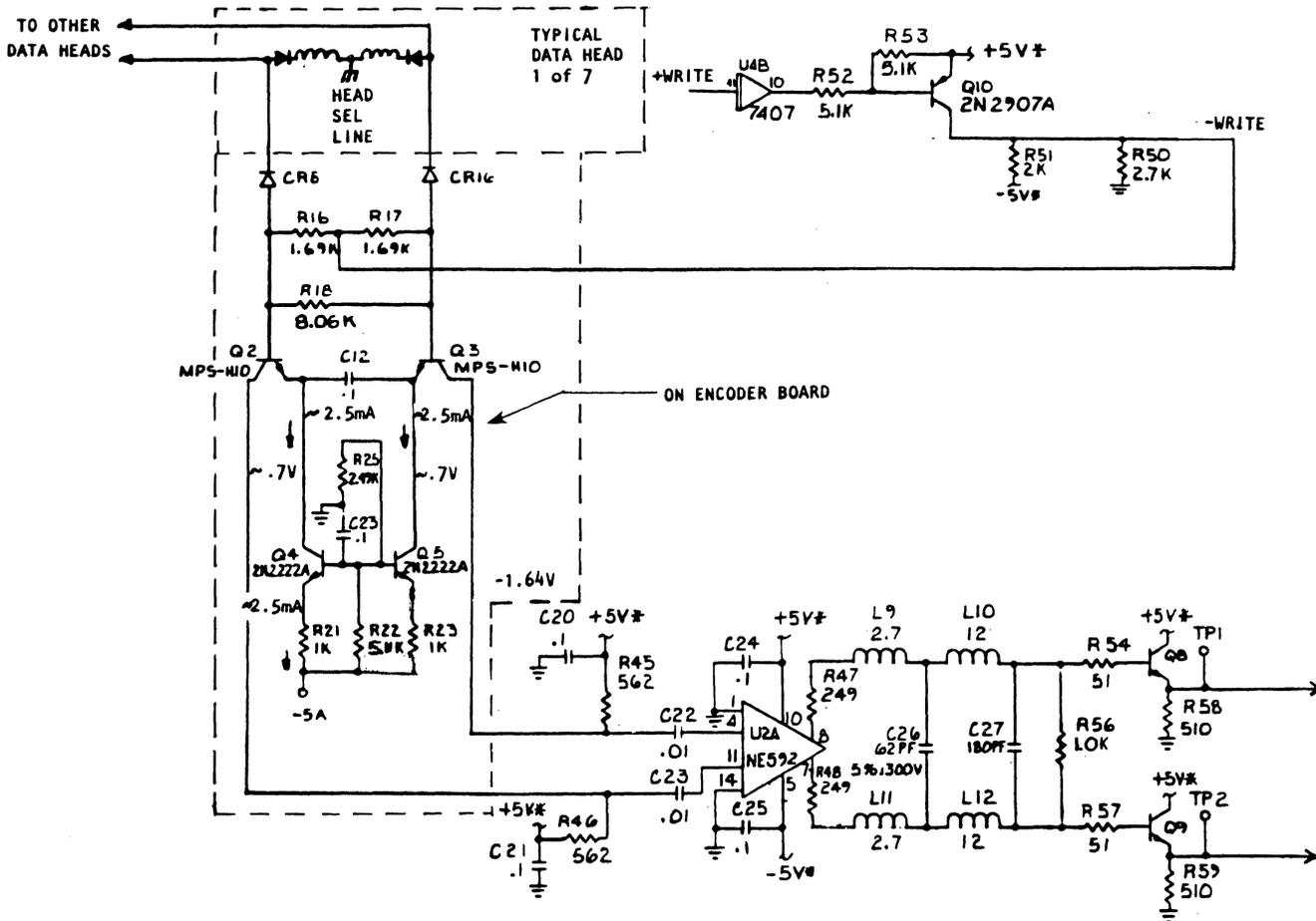
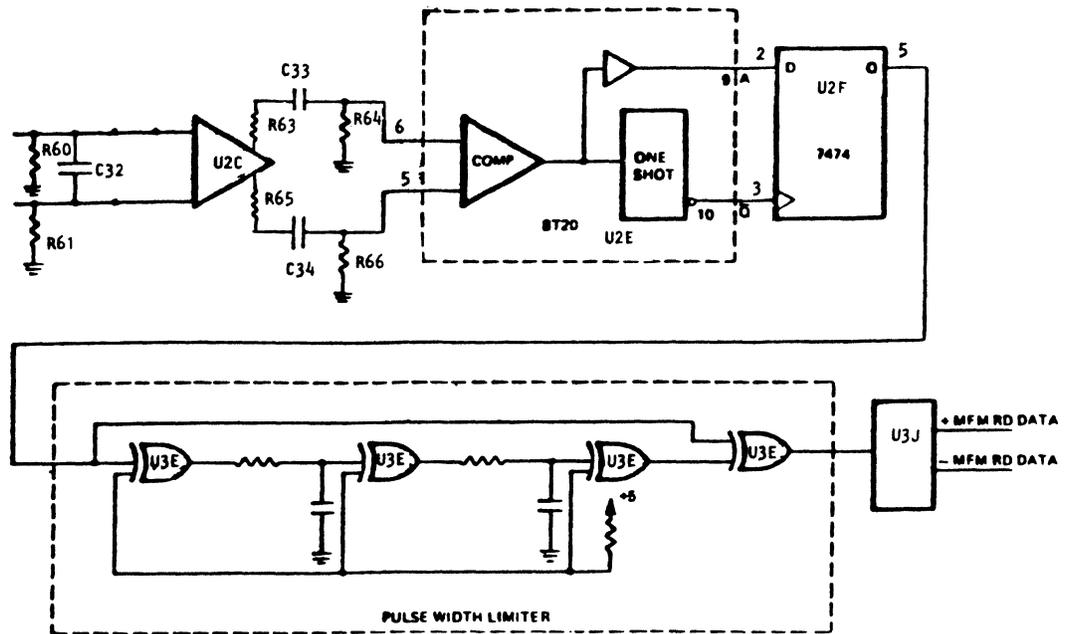


FIGURE 1-33
READ CHANNEL FRONT END

Figure 1-33 illustrates the read channel up to the differentiator input. When +WRITE is HI, -WRITE is -3V. This reverse biases CR8 and CR16 and blocks the AC signal from the data heads at Q2 and Q3. When +WRITE is LO, -WRITE is +5V, which forward biases CR8 and CR16 (and the head diodes). The READ signal then flows differentially to QA2 and Q3, which have Q4 and Q5 as current sources. The current source provides DC bias for Q2 and Q3. U2A (NE592) is set up CASCODE (common emitter, common base amp) with Q2 and Q3. The NE592, a high frequency differential amp, amplifies the READ signal (gain approximately 400). Then the amplified differential output flows through a low pass filter. Differential processing of the READ signals up to the comparator reduces common mode noise. The low pass filter is comprised of R47, R48, L9, L11, C26, L10, L12, C27, R56, R54, and R57. The filtered signal is coupled to another filter by emitter followers Q8 and Q9.

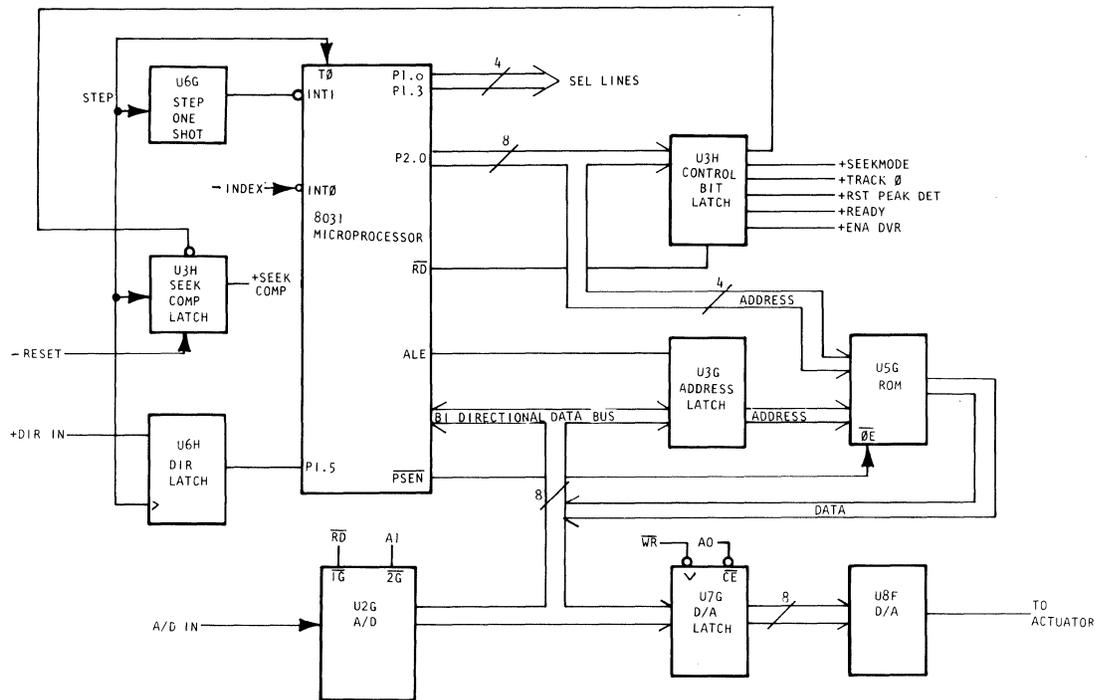


**FIGURE 1-34
READ DATA PULSE GENERATION**

Up to this point, flux changes on the media that have been detected, amplified, and filtered are in the form of voltage peaks. Since the precise bit timing required by the data separator is not easily achievable by peak detection, the data is differentiated to accurately convert the peaks into zero voltage crossings. Figure 1-34 illustrates the remainder of the read channel. Amplifier U2C is configured as a differentiator with the differentiated outputs appearing at the input to the comparator. The zero crossings are detected by the comparator, whose output is the D input of flip-flop U2F, part of the droop ignore circuit. The zero crossings also trigger a one-shot whose period is set shorter than the expected bit time. When the one-shot times out, the flip-flop latches the state of the comparator. The one-shot time is long enough that any change in the comparator output due to noise in the differentiated signal will be filtered by the flip-flop and will not be detected as data bits. The output of the droop ignore flip-flop then passes through a pulse width limiter comprised of a series of gates with added delays. The resulting narrow positive pulses represent the detection of flux reversals in the media. These pulses are input to a differential line driver and are output as \pm MFM READ DATA to the controller via the 20 conductor data cable.

1.3.13 MICROPROCESSOR CIRCUITS

The Q2080 uses an 8031 microprocessor to control the drive during operation. The microprocessor interfaces are shown in Figure 1-35.



**FIGURE 1-35
MICROPROCESSOR CIRCUITS BLOCK DIAGRAM**

The STEP ONE-SHOT (U6G) separates STEP pulses slower than a nominal $535 \mu\text{s}$ and interrupts (INT1) the microprocessor every time STEP pulses go slower than $535 \mu\text{s}$. U6G is a retriggerable one shot with timing equal to $.45 (R111) (C50) = 535 \mu\text{s}$.

The SEEK COMPLETE LATCH (U3H) clocks in SEEK NOT COMPLETE when STEP pulses begin. The microprocessor sets SEEK COMPLETE when the seek is finished. U3H is a D-type flip-flop.

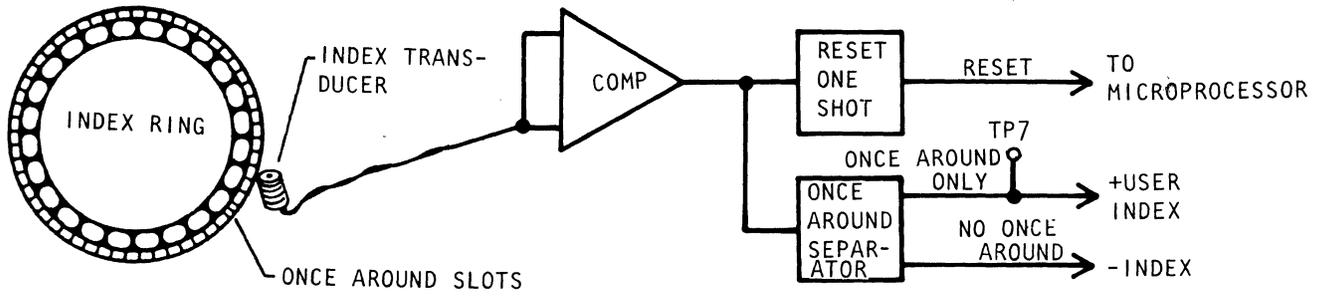
The DIRECTION LATCH (U6H) clocks the direction bit into the microprocessor. It is a D-type flip-flop.

In order to read the main program stored in EPROM U5G-2732 4K x 8, the microprocessor sends ADDRESS via P0 (data bus) and P2 (lower 4 bits). U3G latches the ADDRESS during ALE (address latch enable). The 2732 puts the data to 00 to 07 and $\overline{\text{PSEN}}$ (program store enable) goes LO enabling 00 to 07 onto the data bus.

The CONTROL BIT LATCH (U5H) holds the control bits until the microprocessor issues a READ command. This latch is required because the microprocessor uses P2 for both ADDRESS lines and control bits. -RESET starts the control bits in the right state. U5H is a 74LS 273 octal latch.

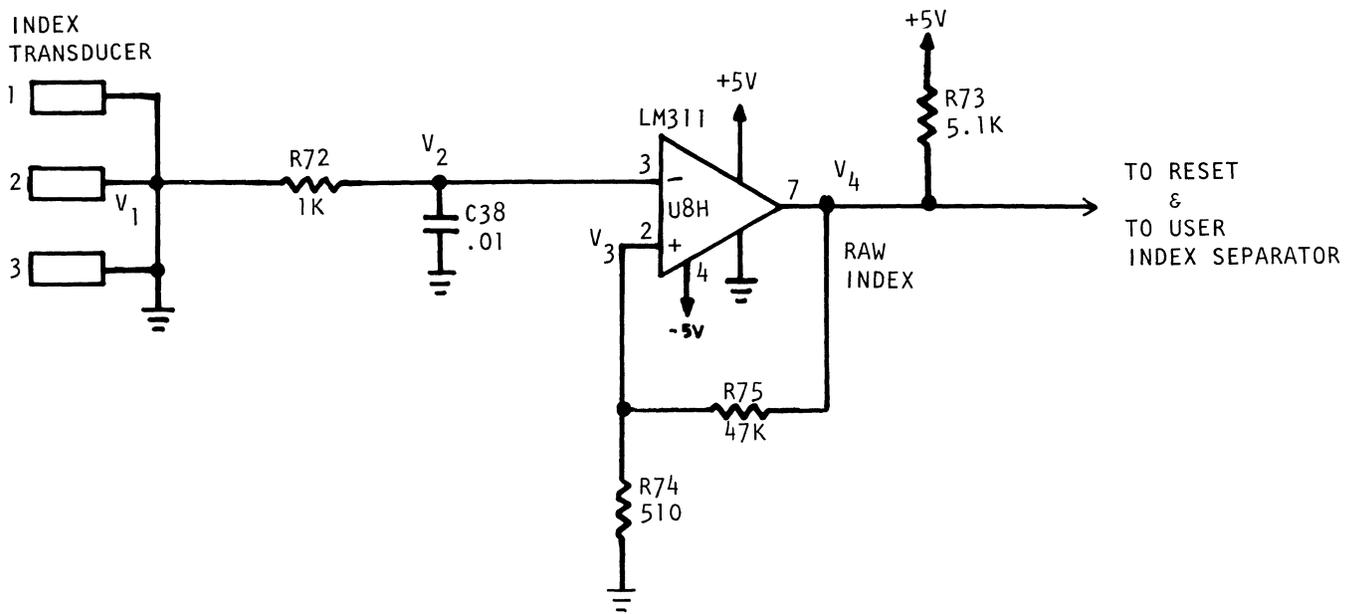
1.3.14 INDEX GENERATION

The Q2080 uses a metal index ring on the disk mounting hub below the bottom disk to generate index signals. The ring has 55 index slots and one of the slots has an extra rib dividing it into two smaller slots. The two smaller slots signal the once-around index. A magnetic transducer picks up signals as the slots rotate past and sends these signals to the index comparator (LM311) that squares the waves at the zero crossings. The signal then goes to the RESET one-shot, which resets the microprocessor when disk speed is less than 2000 RPM. The index comparator also sends a signal to the once-around separator, which separates the extra once-around pulse from the 54 INDEX pulses. The block diagram in Figure 1-36 illustrates the index generation circuit.



**FIGURE 1-36
INDEX GENERATION**

The circuit for the index comparator is shown in Figure 1-37. R72 and C38 make a low pass filter to eliminate high frequency noise. R74 and R75 provide hysteresis according to $V_4 \left(\frac{R74}{R74 + R75} \right) = V_3$.



**FIGURE 1-37
INDEX COMPARATOR**

Figure 1-38 demonstrates the index separator circuit. In this circuit, the -INDEX LO time is determined by $0.7(R117)(C51) = 273\mu s$. V_1 goes HI if the RAW INDEX clocks in when -INDEX is LO (or Q of U8G is HI). This only happens during the extra pulse of RAW INDEX at the once-around point. When V_1 goes HI, the +USER INDEX goes HI for approximately $12\mu s$. Figure 1-39 summarizes the timing relationships between the index signals.

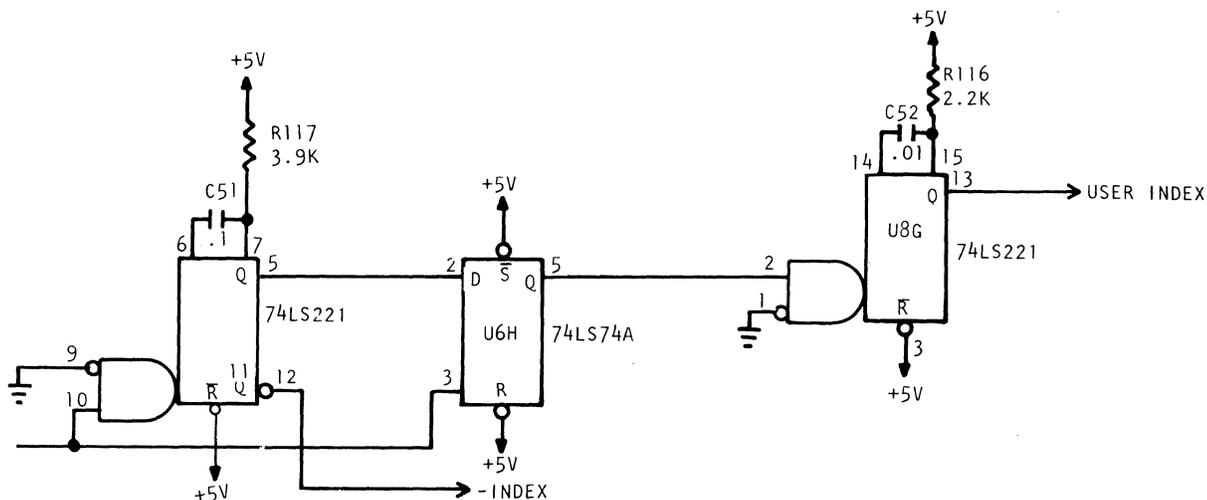


FIGURE 1-38
INDEX SEPARATOR

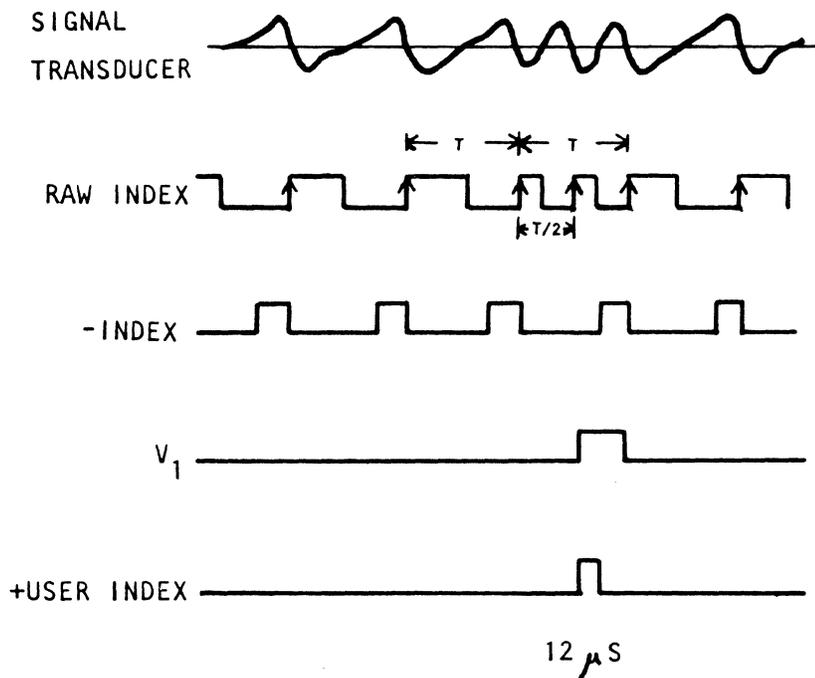
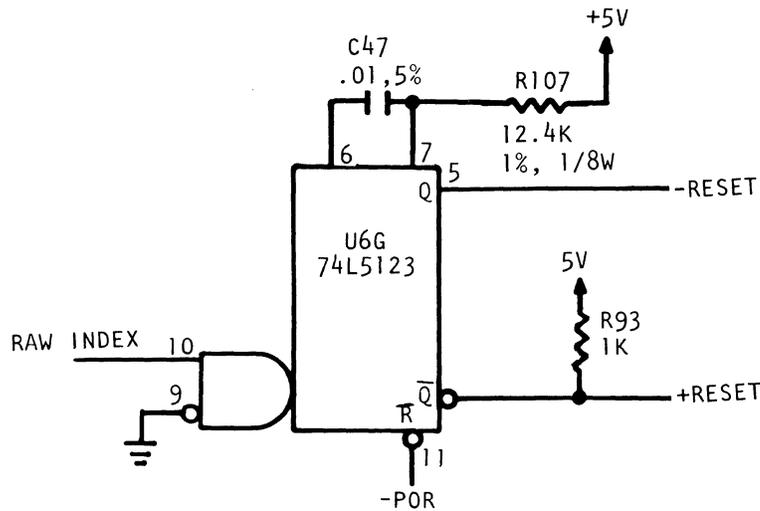


FIGURE 1-39
TIMING RELATIONSHIPS BETWEEN INDEX SIGNALS

When the RAW INDEX is slower than $558\mu s$ ($= 0.45 R107 C47$), (disk speed $= \frac{1}{(54)(558\mu s)} = 33\text{ Hz}$ or 2000 RPM) the RESET one-shot does not always retrigger and the RESET lines keep sending a RESET signal. When the RAW INDEX is faster than $558\mu s$, the RAW INDEX gives a constant retrigger which stops the RESET signal. Figure 1-40 shows the RESET one-shot circuit.



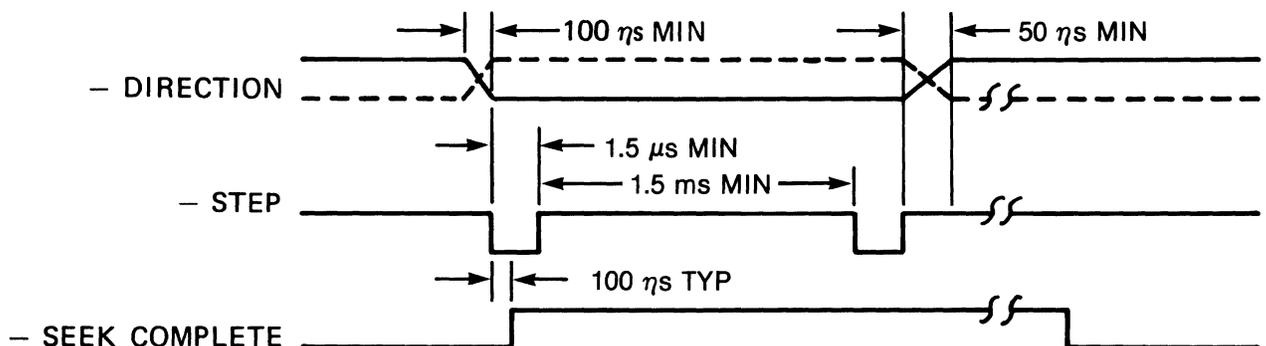
**FIGURE 1-40
RESET ONE-SHOT**

1.3.15 CONTROL SIGNAL INTERFACE

Unless stated otherwise, all control signals are enabled/gated with drive select. The function of each of the thirteen (13) control signals is described below:

INPUT SIGNALS

- **DRIVE SELECT 1, 2, 3, or 4** — A LO level on this line logically connects the drive to the control lines. Only one drive select line may be active at a time and it selects the drive that has the matching drive select jumper installed.
- **DIRECTION IN** — A LO level on this line defines the R/W head motion as in or toward the center of the disk (away from track 000). Motion occurs with receipt of a STEP pulse. A HI level on this line defines the R/W head motion as out or toward the edge of the disk (toward track 000).
- **STEP** — A LO pulse of at least $1.5 \mu\text{s}$ duration on this line will cause the R/W head to move in the direction defined by the DIRECTION IN line. If STEP pulses occur at a rate equal to or greater than 1.5 ms between pulses, the heads will move at the rate of the incoming steps (normal step mode). If the incoming step pulse rate is equal to or less than $200 \mu\text{sec}$ between pulses, the pulses are buffered into a counter and motion occurs after the last step pulse is received (burst mode). See Figures 1-41 and 1-42 for Step Timing.



**FIGURE 1-41
NORMAL STEP MODE TIMING**

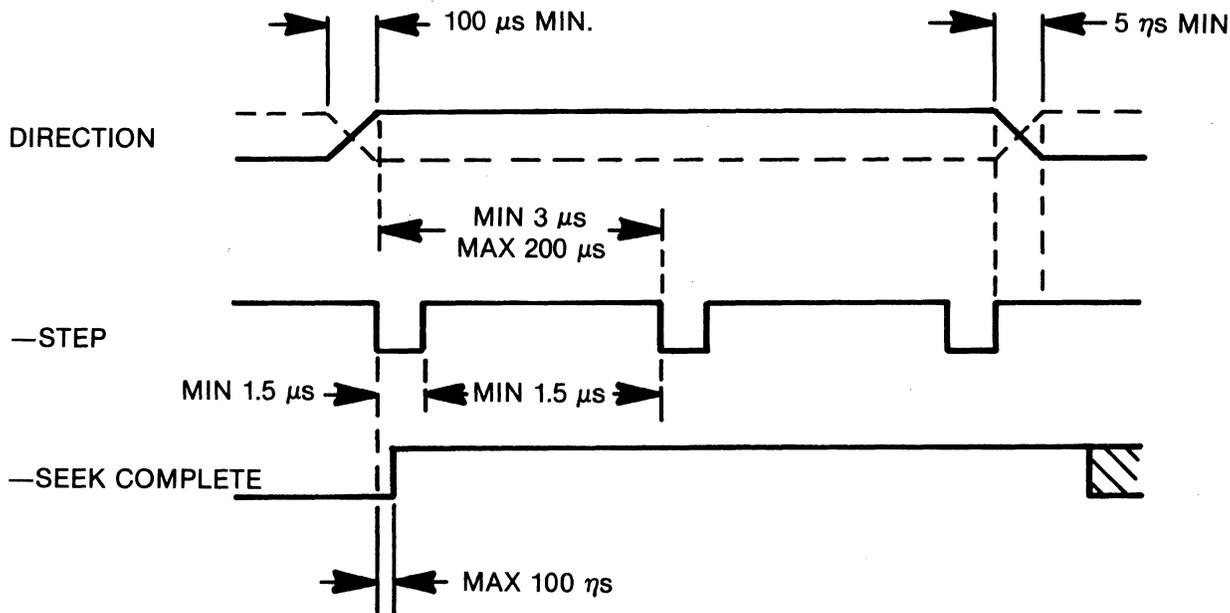


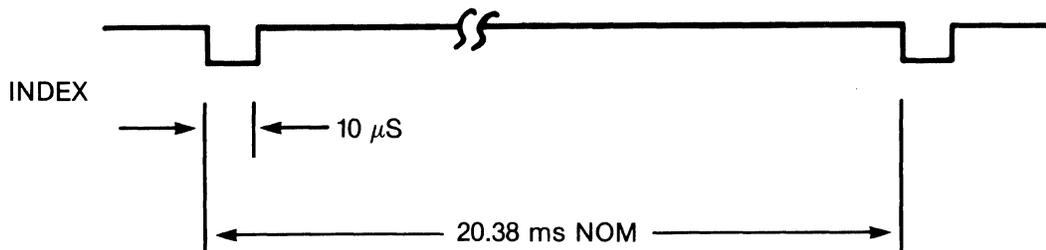
FIGURE 1-42
BURST STEP MODE TIMING

- **HEAD SELECT 2^0 , 2^1 , and 2^2** — These three lines provide a binary code to select one of the heads. 2^0 is the least significant bit and the heads are numbered 0 through 6. When head select 2^1 and 2^2 are LO and 2^0 is HI, head 6 is selected. Conversely, if all lines are HI, head 0 is selected.
- **WRITE GATE** — A LO level enables write data to be written on the disk.
- **REDUCE WRITE CURRENT** — A LO level on this line selects a lower level of write current to be used when writing. It is recommended that the lower level be used when writing on levels 586 through 1171.
- **RE-ZERO** — When this feature is enabled by installing jumper “C” on the control PCB and LO pulse of at least $50\ \mu\text{s}$ duration occurs on this line, the drive resets the microprocessor and recalibrates to cylinder 000.

OUTPUT SIGNALS

- **TRACK 000** — A LO level on this line indicated the R/W heads are positioned at cylinder 000 (the outermost cylinder).
- **INDEX** — A LO pulse of $10\ \mu\text{s}$ duration on this line indicates the beginning of a track. The leading edge of this pulse must be used for all timing requirements. The pulse occurs once each revolution or every 20.38 msec. Figure 1-43 illustrates INDEX timing.

INDEX normally is output on cable J2 only if DRIVE SELECT is true. If it is desired to output index continually, trace G1 must be cut and a wire jumper installed at U1. Both G1 and U1 are located at PCB location J6.

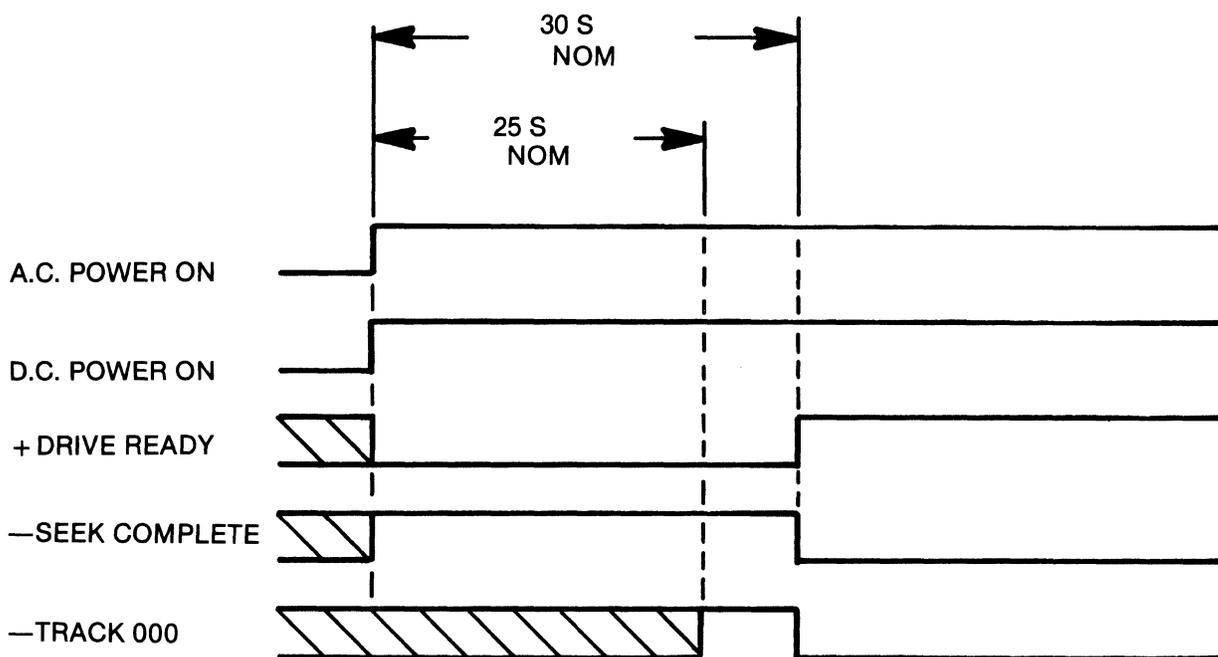


**FIGURE 1-43
INDEX TIMING**

- **READY** — A LO Level on this line indicates the drive is up to speed and the interface signals are valid. When **READY** and **SEEK COMPLETE** are true, the drive is ready to read, write or seek.
- **WRITE FAULT** — A LO level on this line indicates write current is flowing in the selected head and **WRITE GATE** is not true (HI). Write Fault may be reset by: deselecting the drive, driving the Re-zero line, or cycling the DC power off then on.
- **SEEK COMPLETE** — A LO level on this line indicates the R/W heads have settled on a cylinder and a read, write or another seek may take place.
- **M3** — When this output is selected by installing Jumper M3 on the control PCB, a LO level indicates that the drive selected is a Model Q2080. Make sure that this line is not already used at J1-46.

Figure 1-44 shows the general timing relationships between some of the control signals found in the Model Q2080.

NOTE: The air actuated actuator lock (AIRLOCK™) will take 30s (MAX) to lock the actuator after power is removed.



**FIGURE 1-44
GENERAL CONTROL TIMING REQUIREMENTS**

1.3.16 INTERFACE AND DRIVE SELECT LOGIC

This logic performs three functions in the Q2080:

1. Provides cable drivers and receivers for the interface signals.
2. Allows for gating these signals with the DRIVE SELECT line.
3. Provides for interface cable termination on the last drive on the cable.

Refer to Figure 2-1. At the top of this figure are the cable receivers for the REDUCED WRITE CURRENT, HEAD SELECT, DIRECTION IN, STEP, and WRITE GATE control signals. The REDUCED WRITE CURRENT line is received by buffer U4B, a 7407, at pin 9. The other signals are received by the hex Schmitt trigger inverter, a 7414, at U3E. All of these signals may be terminated at this drive by installing a 220/330 ohm resistor pack at U5J. The RE-ZERO line may be enabled by placing a jumper across point C.

At page location 7C is the DRIVE SELECT jumper block and the DRIVE SELECT terminator R2 and R3. Placing a jumper across point A results in the drive being continuously selected and is normally used for test purposes. When a LO signal on a DRIVE SELECT line matches with a jumper, gate 7H is enabled to receive the optional RE-ZERO command. +DR SEL (U4F -2) will enable reception of STEP (U4F-1) and WRITE GATE (U4F-5). +DR SEL also provides the -DRIVE SELECTED signal via U7J-4 over the data cable (J2-1) to indicate to the controller that the drive has been selected. The signal +DR SEL also enables the differential line driver 2J to output \pm MFM RD DATA to the controller. The WRITE FAULT F/F U4C is also enabled to latch a fault condition in the event write current is detected and there is no WRITE GATE present. If this error is detected and latched, it is necessary to raise the DRIVE SELECT line to reset the error (U4C-13). +DR SEL also enables the -TR000, -RDY, and -SK COMPLETE control signals at gate U6J.

1.3.17 POWER ON RESET

The purpose of the power on reset circuitry is two-fold. First, the reset will hold the processor and other circuits in a known condition (reset) until the logic power is up and stable. Second, it provides a reset when the logic power falls below an acceptable level. The circuitry is located at C4 on Figure 2-1. As the +5V rises, C2 charges via R5. Once this charge exceeds the high level input voltage of OR gate U7H, (nominally 1.4V) the gate outputs a LO at pin 4. This is -POR and is distributed throughout the PCB to reset the logic.

1.3.18 DC POWER FILTER AND REGULATORS

Refer to Figure 2-1, location B6 and 7. The three required DC voltages connect to the drive via connector J5. +24 VDC enters on pin 1 where L18 and C3 form a decoupling network. Voltage regulator VR1 uses +24 VDC as an input and outputs +12 VDC used by some of the operational amplifiers in the drive. The +24 VDC is used by both the write current drivers and the actuator drivers. The +24 VDC return line is J5 pin 2.

+5 VDC enters on pin 5 and is decoupled by L19, C4 and C70-72 before being supplied to the logic on the PCB. +5 VDC is further filtered by L6, C89 and C18 to be used by the read channel amplifiers as +5V* as shown in Figure 2-3. The +5VDC return line is J5 pin 6.

The minus voltage supplied to the drive may be either -5 VDC or -7 VDC to -16 VDC and enters at J5 pin 4, where it is decoupled by L20, C5 and C7. The regulator output is selected by placing the W1 jumper in the -15 VDC position (all drives are shipped from Quantum with the jumper in the -15 VDC position). If the minus voltage is more negative than -5 VDC, then regulator VR2 regulates the input voltage to -5 VDC.

NOTE

Damage to the drive can occur if minus voltages greater than -5 VDC are applied to the drive when the jumper is in the -5 VDC position.

The -5VDC is further filtered by C8, L7 C90, and C97 to be used by the read channel as -5V*. The minus voltage return line is J5 pin 5.

SECTION 2

LOGIC CONVENTIONS AND CIRCUIT DIAGRAMS

2.1 GENERAL DISCUSSION

Quantum's logic diagrams emphasize the functions performed by the logic elements rather than the kinds of devices used. For example, a NAND gate may appear on a Quantum diagram as either a positive logic AND function with the output inverted (NAND), or as a negative logic OR function with the inputs inverted (NOR). This practice runs contrary to some logic drawing standards that require the use of the NAND symbol for both functions, but aids field service personnel in troubleshooting and system design engineers in understanding the principles of operation of the design.

This functional approach to logic symbology is basic to the logic documentation conventions employed by Quantum. The conventions that govern logic symbology, signal nomenclature, and other drawing standards that may help the reader interpret Quantum logic diagrams, are discussed in the following paragraphs.

2.2 LOGIC SYMBOLOGY

The logic function symbols that Quantum uses in logic diagrams conform closely to those set forth in MIL-STD-806 or ANSI Y32.14-1973. Small scale integration (SSI) circuits are represented by their function symbol. Medium scale (MSI) and large scale (LSI) integration devices, such as shift registers, RAMs, ROMs, etc., are represented by rectangles with function labels. Since both positive and negative logic conventions can appear in a single diagram, the unfilled-circle negation symbol specified by MIL-STD-806 or ANSI Y32.14-1973 is used to distinguish between LO true and HI true signals.

Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Some device symbols, such as flip-flops, show inputs and other external connections on the top and bottom of the symbol for clarity. Also, the drawings themselves usually show major signal flows from left to right, top to bottom. However, drawing layout restrictions occasionally require the reverse of this, and that some symbols be drawn with a vertical orientation.

2.3 COMPONENT LOCATIONS

Quantum uses two component location systems. One, shown on the perimeter of the diagram, is useful in locating a portion of a circuit or a particular component on the diagram itself, and has no other meaning. The other involves the component identifiers, such as OR gate 4J. The identifier is a "grid coordinate" code for locating that component on its printed circuit board. Further, a textual reference to a device, such as a flip-flop, will usually further identify the device by its major output terminal. In the case of flip-flops, the "Q" output is usually used, i.e. FF 6H-9.

2.4 CIRCUIT DIAGRAMS

The schematic diagrams which follow the integrated circuit illustrations represent the latest version of each circuit board in current production at the time of preparation of this manual.

There are two important part numbers associated with each circuit board in the Q2080.

1) The PCB Assembly part number identifies the complete circuit board with components installed. This number is etched onto the top (component) side of the PCBA. The revision letter of the board assembly generally is marked on this side of the PCBA also.

2) The PCB part number (fabrication number) is the part number of the blank PCB with components. This number is etched on the bottom (solder) side of the PCB. The revision letter of the fabrication is also etched on this side.

This section contains circuit diagrams for the followings:

Figure 2-1 Power Interface Circuits

Figure 2-2 Write Data Circuits

Figure 2-3 Read Data Circuits

Figure 2-4 Actuator Driver Circuits

Figure 2-5 Microprocessor Circuits

Figure 2-6 Servo Burst and Index Circuits

Figure 2-7 Encoder PCB Circuits

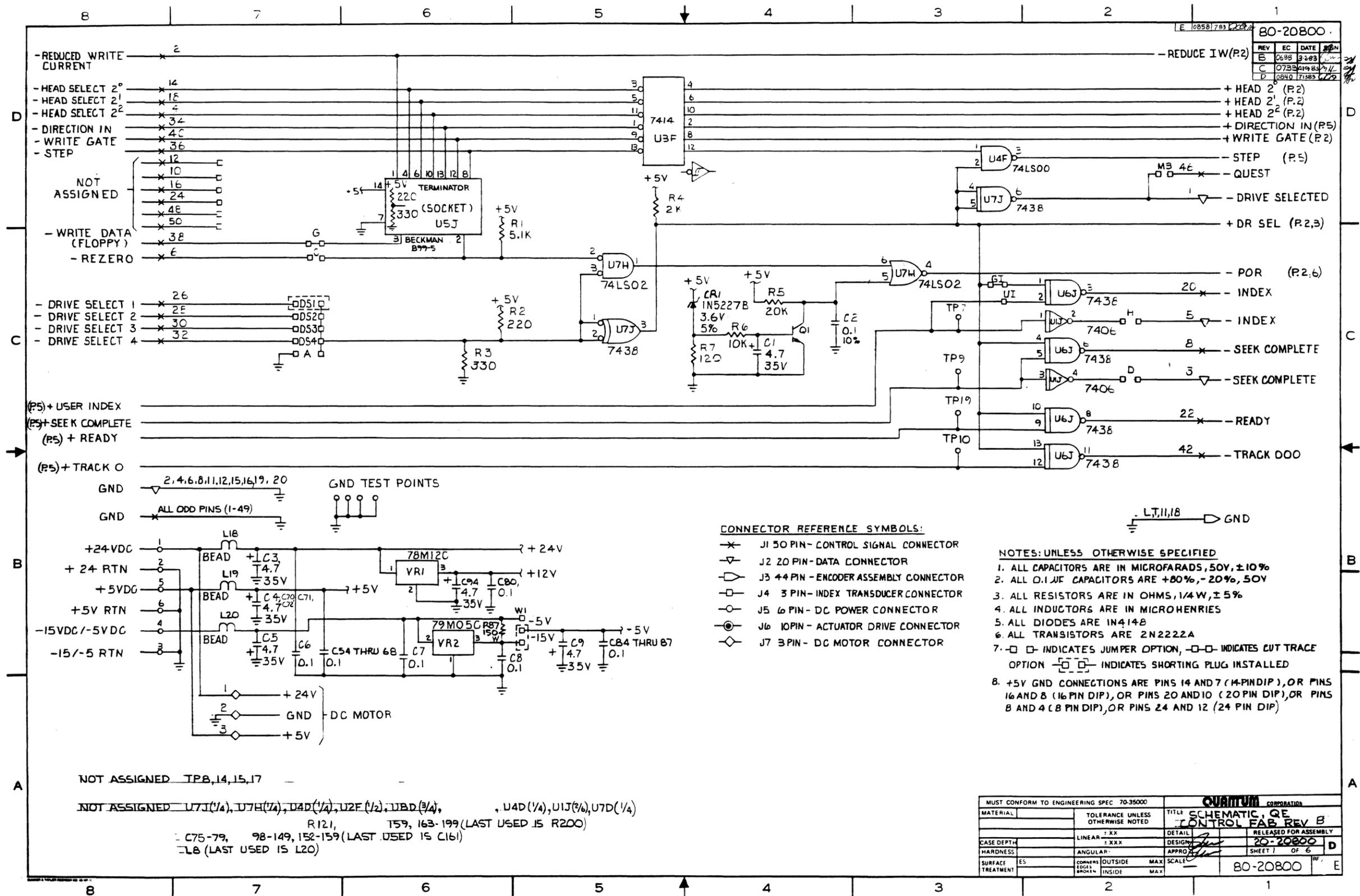
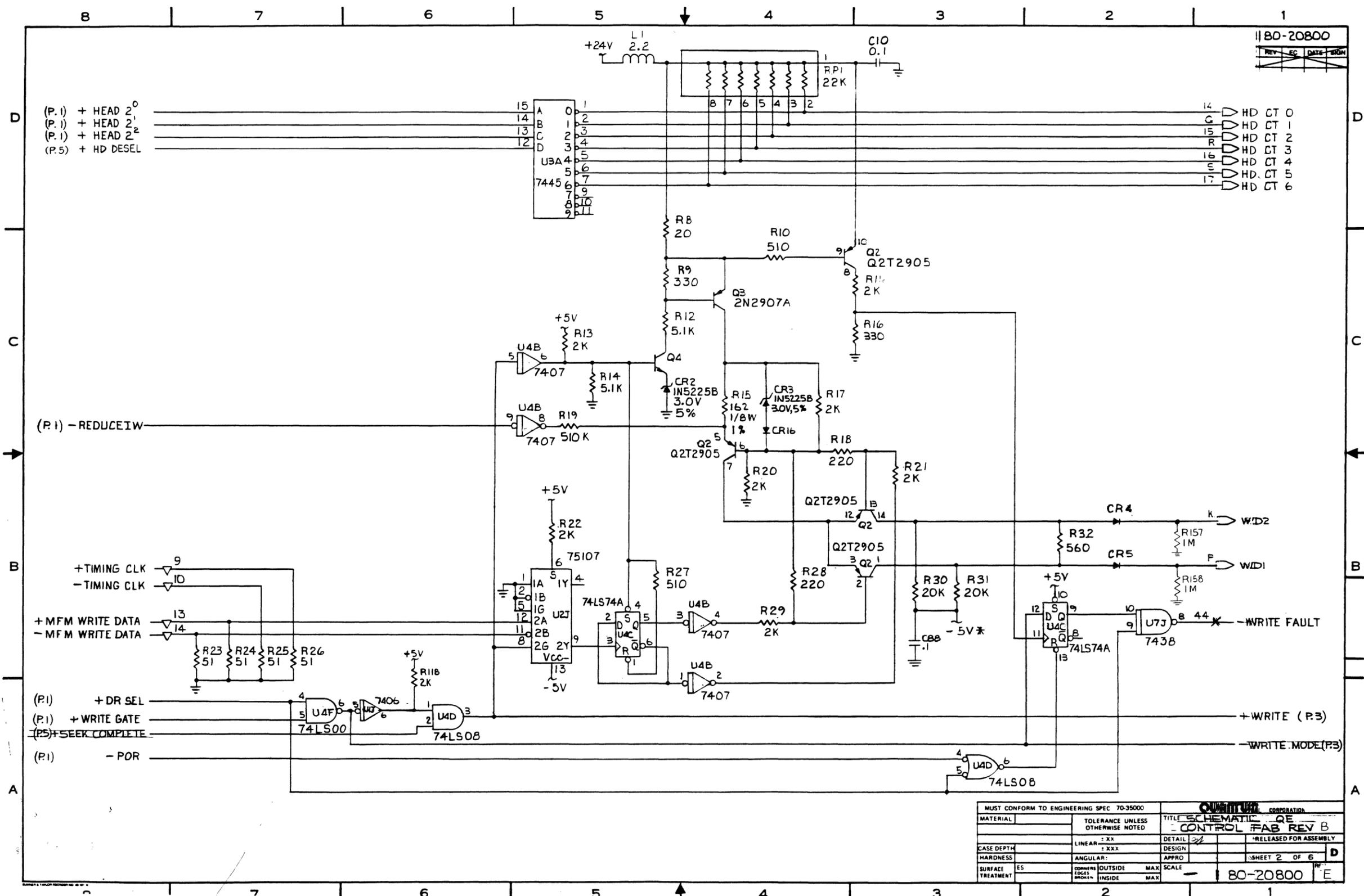


Figure 2-1
Power Interface Circuits



BD-20800			
REV	EC	DATE	BY

Figure 2-2
Write Data Circuits

MUST CONFORM TO ENGINEERING SPEC 70-35000			
MATERIAL		TOLERANCE UNLESS OTHERWISE NOTED	
CASE DEPTH		LINEAR : .XXX	
HARDNESS		ANGULAR : .XXX	
SURFACE TREATMENT		CONFORM TO OUTSIDE MAX EDGES INSIDE MAX	
		TITLE: SCHEMATIC QE CONTROL FAB REV B	
		DETAIL: [initials]	
		DESIGN: [initials]	
		APPRO: [initials]	
		SCALE: [initials]	
		SHEET 2 OF 6	
		80-20800 E	

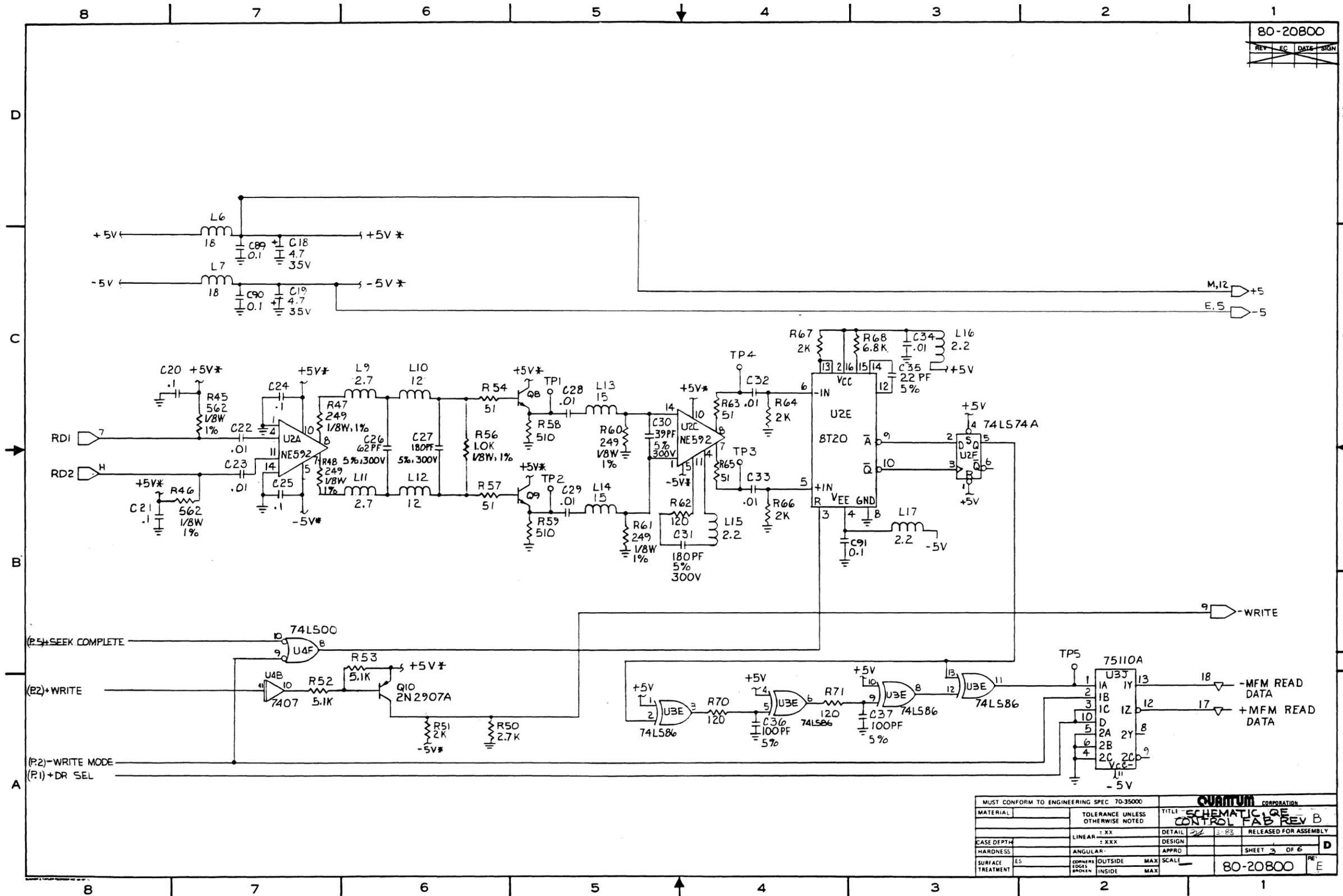
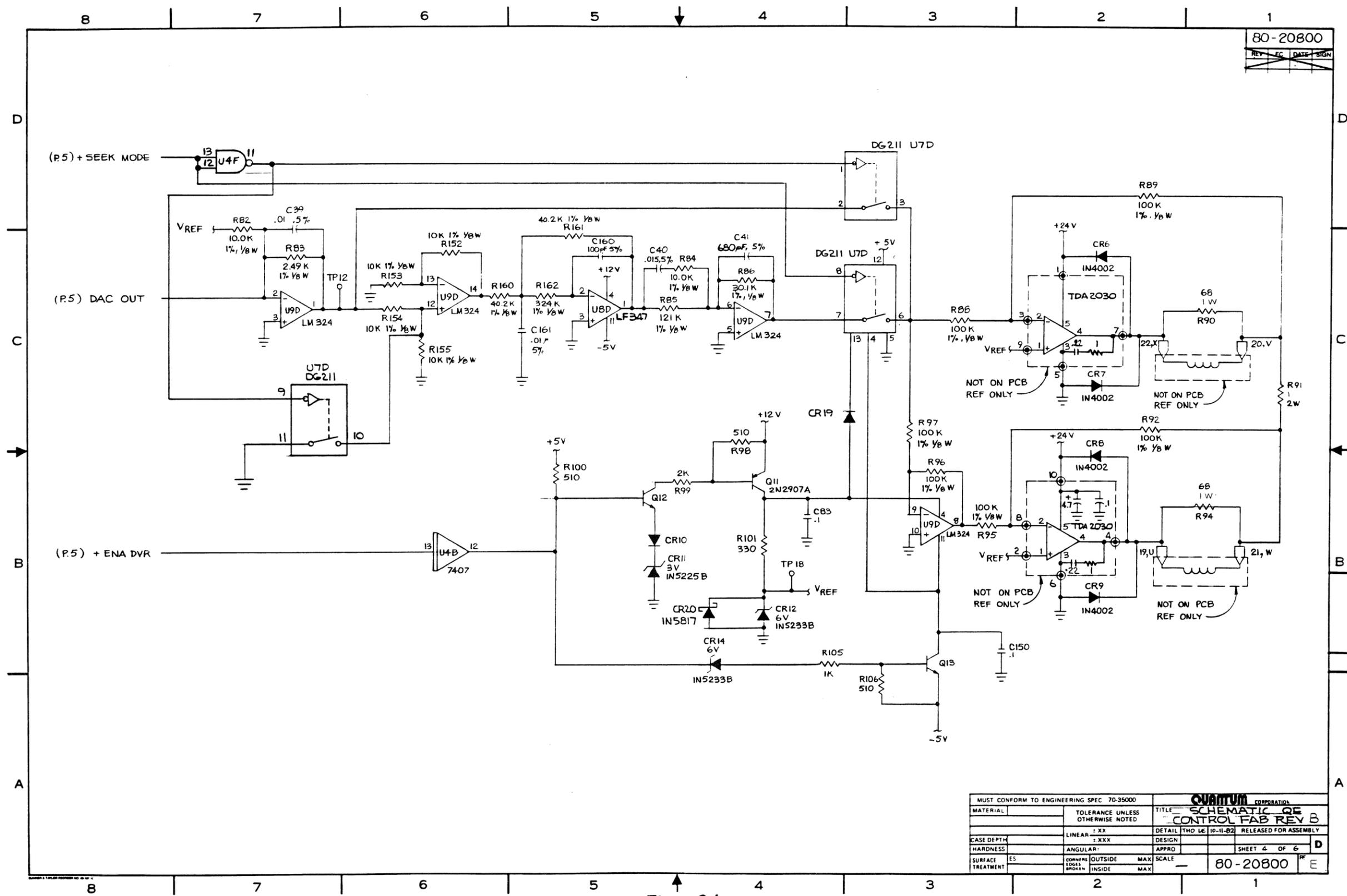


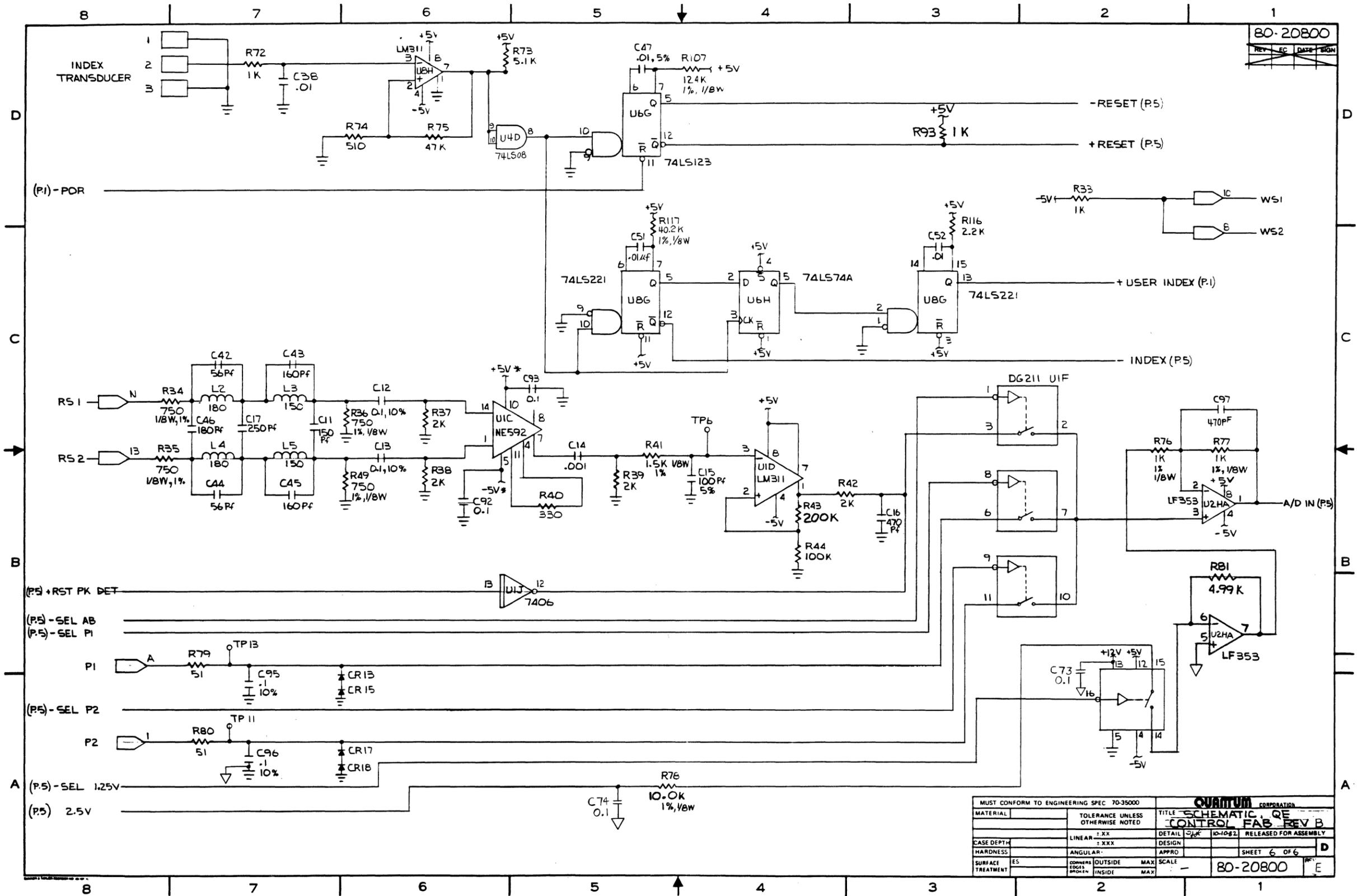
Figure 2-3
Read Data Circuits



80-20800
REV EC DATE SIGN

MUST CONFORM TO ENGINEERING SPEC 70-35000		QUANTUM CORPORATION	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC OF CONTROL FAB REV B	
CASE DEPTH	LINEAR : XX	DETAIL THO LE 10-11-82	RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR : XXX	DESIGN	
SURFACE TREATMENT	ES	APPRO	SHEET 4 OF 6
	CORNERS OUTSIDE MAX SCALE		80-20800
	EDGES INSIDE MAX		E

Figure 2-4
Actuator Driver Circuits



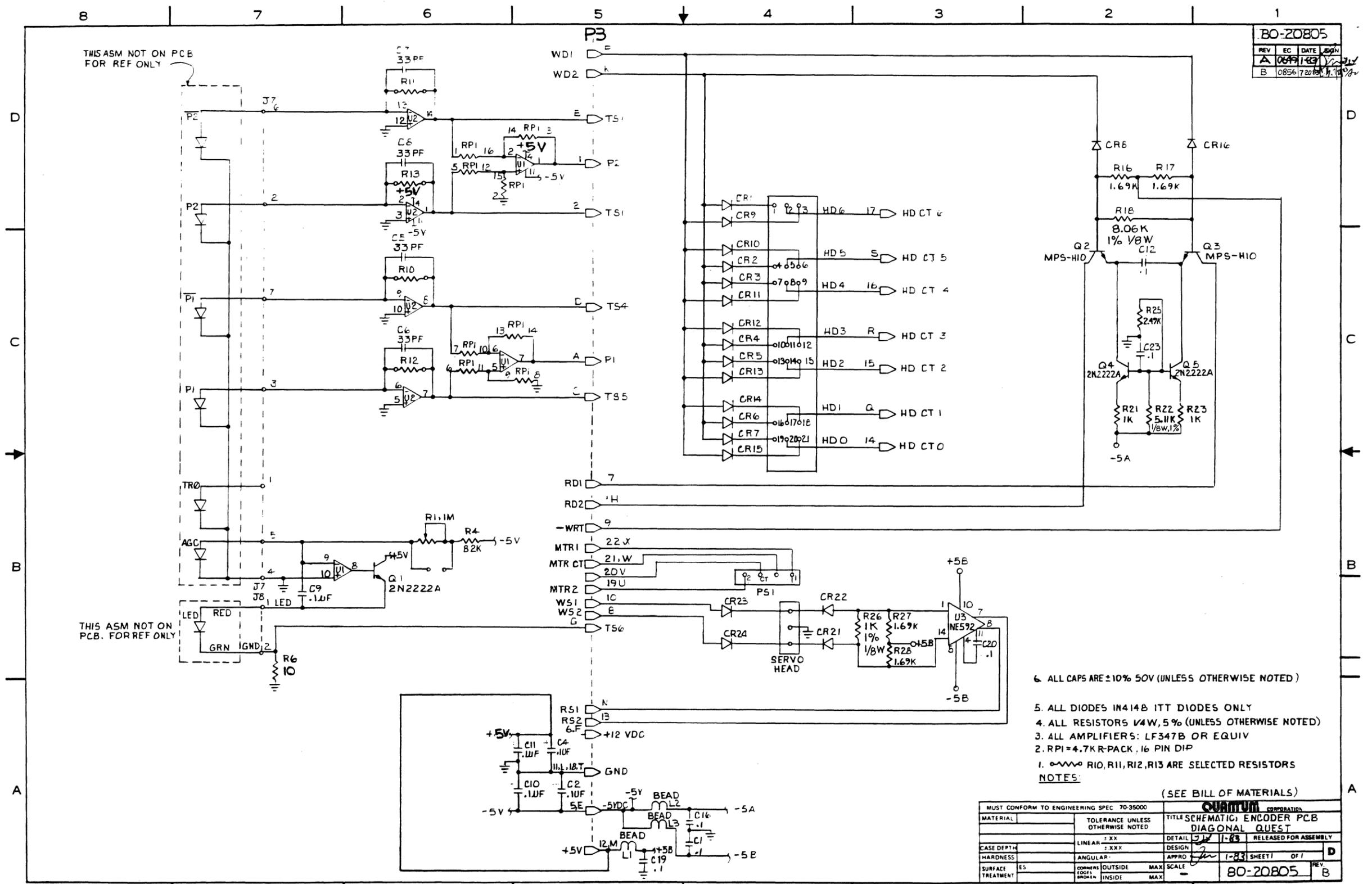


Figure 2-7
Encoder PCB Circuits

SECTION 3 APPLICATIONS

3.1 INTRODUCTION

The Q2080 drive will be incorporated into a number of different systems. Each of these applications will vary depending on system design, software, drive controller, cabinet design, etc. Quantum intends to assist engineers working with the Q2080 by supplying accurate technical data on the drive. This section of the Q2080 Technical Manual provides information on those aspects of the Q2080 that influence the integration of the drive into a system. Specific topics include the interface, errors and media defects, self diagnostics, and track formats.

3.2 POWER ON RECALIBRATION SEQUENCE

The following summarizes the recalibration procedure that the Q2080 performs when power to the drive is turned on.

1. Initialize all registers.
2. Check index time.
3. Delay 2 seconds.
4. Calibrate P1 and P2 ("circle" size.)
 - a) Find P1 and P2 maximum and minimum.
 - b) Compute P1 and P2 center value.
5. Servos.
6. Generate rough calculations of "NULL 1" value (to negate stiffness of wires on the head stack).
7. Do 100-5 track seeks to the center of the disk track area (5 track seeks equal single step mode.)
8. Wait 1 second to calculate a new "NULL 1" value.
9. Find track 0 (uses single step seeks).
10. Settle and look at track 0 bursts. (If fifth servo burst equals zero amplitude, then track 0 has been detected.)
11. Compare servo burst values for average amplitude.
12. Compare results (track 0 detect) to the track counter.
13. If error, drop actuator power and try again.

3.3 INTERFACE

The Q2080 uses a SA1000 compatible drive interface with a 4.34 Mbit/sec transfer rate. General interface timing specifications can be found in the *Q2080 Product Description OEM Manual*. Also, refer to section 1.3.9 and 1.3.15 of this manual for additional interface information.

When the drive receives more STEP pulses than there are cylinders on the disk and the direction of seek is out (toward disk OD), the heads will seek to track 0. Then the drive sends SEEK COMPLETE and asserts READY.

3.4 ERRORS AND MEDIA DEFECTS

3.4.1 ERRORS

Any discrepancy between recorded data and recovered data is defined as an error. High density digital recording systems require an error detection and correction scheme to enhance the operational performance and increase the reliability of the system. Disk storage systems record data in a precisely timed bit stream. Data recovery is accomplished with a data separator that uses this precise bit positioning to detect encoded data bits.

In these systems three types of errors occur, drop outs, drop ins, and phase shifts, with the most predominant error pattern being a burst of errors occurring in one or more data tracks.

A drop in is when the system sees a bit when it was not expecting to see one. This is caused by a media flow causing a rise in signal amplitude. A drop out is a bit that has shifted from its nominal position further than the data separator can tolerate due to signal amplitude decrease. Phase shift detects are small shifts in the data signal that the data separator cannot tolerate but have little or no effect on the signal amplitude.

The errors can be either “soft,” those that are not readily repeatable, or “hard”, those that are repeatable with high probability. Soft errors are generally related to the signal to noise ratio of the system. They represent marginal conditions of the media, heads, read/write circuitry, and the controller and data separator circuits. Hard errors are most often due to defects, pits, scratches, or thin spots in the media. These defective media areas can be detected and identified by the track and position. Having this position information allows a user to skip these bad areas when recording data.

3.4.2 DEFECT DETECTION AND REPORTING

Quantum uses a unique analog media test system that measures both the amplitude and phase distortion of each bit that can be recorded on all tracks of all surfaces. The test system provides a defect map that is shipped with each drive. The defect location is identified on the map by cylinder number, head number, number of (8 bit) bytes from index, and number of bits in length. The numbers are given in both decimal and hexadecimal notation for user convenience.

3.4.3 MEDIA QUALITY CRITERIA

Each drive that Quantum ships will meet or exceed the following standards of media quality:

1. Cylinder zero (0) will be free of defect areas.
2. No drive will have more than 84 total defect areas.
3. No surface will have more than 4 tracks with multiple defect areas.

Quantum defines a defect area as an area equal to or less than 16 bits in length. For example, a defect area 17 bits in length counts as 2 defect areas and a defect area of 16 bits in length counts as 1 defect area.

3.5 SELF DIAGNOSTICS

The Model Q2080 provides an internal seek diagnostic that will exercise all drive functions except data transfer. The diagnostic is initiated by installing jumper E4 at PCB location F5. When the jumper is installed the drive ignores any signals at the interface connectors and implements a seek algorithm that performs seeks and checks for track 0. The repeating butterfly seek pattern is: 586→585→587→584→588→583 If an error is detected, the drive drops READY and drops power to the actuator. Dropping actuator power causes the heads to move over the landing zone. The drive will remain in this state until DC power is cycled or jumper E4 is removed.

3.6 TRACK FORMATTING

3.6.1 INTRODUCTION

With the high transfer rates and large capacities of disk drives, data are normally stored in small, easily managed blocks. As the data are stored in a serial bit stream on a circular track, these blocks can be thought of as segmenting the track. These segments are called sectors.

The method used to define sector boundaries classifies drives as being hard or soft sectored. Hard sectored drives define sector boundaries by some fixed mechanical method. Soft sectored drives define sector boundaries by an ID field that is written on the track by the user. With either sectoring method, data bits cannot occupy all of the available bit positions on the track. Gaps must be placed between sectors to compensate for spindle speed and write oscillator tolerances and also to mask head switching time, write to read recovery time, and the write update splice.

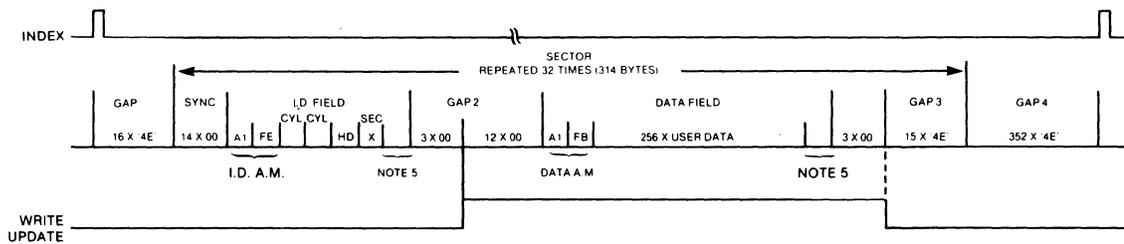
3.6.2 TRACK FORMAT

The position and length of sector boundaries around a track is called a format. Formatting a drive is the process of writing this format on all tracks and surfaces of a drive.

The Q2080 is a soft-sectored drive and as such can use whatever format the use desires. When choosing or designing a format for the Q2080 the following drive specifications must be considered:

- | | |
|---|--|
| 1. Head switching time | 20 microseconds maximum |
| 2. Write to read recovery time | 20 microseconds maximum |
| 3. Spindle speed tolerances | 19.75-21.00 milliseconds (rotational time) |
| 4. Head, media and read write channel characteristics — | These items are selected and optimized for MFM coding at a transfer rate of 4.34MBITS/sec. |

The soft sector format shown in Figure 3-1 is a slightly modified version of the IBM System 34 double density format commonly used on 8 inch floppy disk drives. Data are encoded using the modified frequency modulation (MFM) code.



**FIGURE 3-1
SAMPLE TRACK FORMAT**

Each track is divided into 32 sectors with each sector containing a data field of 256 bytes.

The beginnings of the sector ID field and the data field are defined by a unique field called an address mark. This two byte field always has hexadecimal A1 as the first byte. This byte is followed by hexadecimal FE in ID address marks or hexadecimal FB in data address marks. To insure the recorded pattern of the address marks is unique from all other data patterns, the A1 byte is recorded with a missing clock bit. This encoding violates one of the rules of the MFM code, while maintaining normal bit intervals used in MFM.

Each ID and data field is followed by a data verification field. This may be either a cyclic redundancy check (CRC) field of 16 bits (2 bytes) or an error correction code (ECC) field of 24 or 32 bits (3 or 4 bytes). Various gap and sync fields separate the ID and data fields.

The sync fields provide the data separator with periods of specific length in which bits are recorded in a known and constant position. This allows the data separator to lock onto the present data rate and separate known clock and data bits from the bit stream. The sync field length is determined by data separator performance characteristics.

Each of the four gaps are inserted to mask and/or compensate for various drive characteristics. Gap 1 provides a period that masks the head switching time when formatting a track. When formatting, the controller starts writing at index and continues until the next index is received, at which time the controller switches heads to the next track. This allows one complete track to be formatted on each revolution of the disk. Gap 1 should be at least 11 bytes long to allow for a head switching time of 20 microseconds. Gap 1 is immediately followed by the sync field for the sector ID field of the first sector.

Gap 2 follows the sector ID field and separates it from the data ID field. This gap provides a period that masks the write update splice and provides a sync field for the data ID field. The splice occurs when data is written into the data field, because the new data may not be written exactly in phase with the old data. The length of Gap 2 is determined by: write oscillator tolerance which generates the write splice, data separator lock up performance which requires a specific sync period, and drive spindle speed tolerance which determines where physically the splice may occur.

Gap 3 follows the data field and provides extra time in the sector to allow for spindle speed variations, write oscillator tolerance and to mask the write to read recovery time. For example a track could be formatted with the spindle running faster than nominal the thus occupy less disk space. The track may then be write updated with the spindle running slow and require more disk space for the same number of data bytes.

Gap 4 follows the last Gap 3 on the track and provides extra time in the track to allow for spindle speed and write oscillator tolerances. Gap 4 must be long enough to prevent the format operation from overflowing the track capacity when the write oscillator is running slow and the spindle is rotating 3% faster than normal.

3.6.3 WRITE PRE-COMPENSATION

Recording data at high bit densities creates a phenomenon known as intersymbol interference. This occurs when two bits must be recorded closer to each other than to neighboring bits. When these two bits are read back, intersymbol interference causes the bits to appear shifted away from each other. This is the major cause of bit shift in data recording systems. Other factors such as head/media resolution, speed variations, write current level and random circuit noise contribute to bit shift to a lesser degree. When bit shift is great enough, read errors occur.

Bit shift is density related and therefore, more apparent on the shorter innermost cylinders. There are two methods that the Q2080 user may employ to reduce bit shift: reduce write current, and write pre-compensate. Both methods should be used when writing above cylinder 586. The Q2080 provides an input that when driven will reduce write current by approximately 10%. Write pre-compensation is a technique whereby the bit patterns that cause the greatest inter-symbol interference are detected and those bits that are predicted to be read early or late are correspondingly written late or early. A practical amount of pre-compensation for the Q2080 is 12 nanoseconds for both early and late written bits.

Table 3-1 shows those bit patterns that require pre-compensation, the shift direction expected, the precompensation direction and the type (clock or data) pulse to write for MFM encoding.

**TABLE 3-1
WRITE PRE-COMPENSATION**

Data Pattern				Expected Shift Direction For Data in Cell 3	Pre-compensate Direction	Type of Pulse To Write
1	2	3	4			
0	0	0	0	None	On Time	Clock
0	0	0	1	Late	Early	Clock
0	0	1	0	None	On Time	Data
0	0	1	1	Early	Late	Data
0	1	0	0	None	No Clock or Data Written	
0	1	0	1	None	No Clock or Data Written	
0	1	1	0	Late	Early	Data
0	1	1	1	None	On Time	Data
1	0	0	0	Early	Late	Clock
1	0	0	1	None	On Time	Clock
1	0	1	0	None	On Time	Date
1	0	1	1	Early	Late	Data
1	1	0	0	None	No Clock or Data Written	
1	1	0	1	None	No Clock or Data Written	
1	1	1	0	Late	Early	Data
1	1	1	1	None	On Time	Data

Data is encoded in the sequence 1,2,3,4 and written from Cell 3. Clock pulses are written positioned at the beginning of a cell time and data pulses are written in the center of a cell time.

3.7 EMI INDUCED SOFT READ ERRORS

The higher data densities used by the Q2080 make it more susceptible to EMI than Q2000 series drives. We have identified at least two mechanisms by which EMI can cause soft read errors. This section describes these two mechanisms so that customers can know what to avoid in their system designs.

An EMI problem occurs when a signal is coupled by some means into the read channel. It shows up as an excessive soft data error rate. A higher error rate occurs at the inner (higher numbered) tracks because the signal levels are smaller in that area of the disk. A good test for an EMI problem is to remove the drive from the system and extend the power and data cable to it. If the problem is EMI, the soft data errors should go away. If the soft data errors do not disappear, EMI may still be causing them through a grounding problem.

3.7.1 MAGNETIC COUPLING

One of the coupling methods the drive is sensitive to is magnetic. The sensitive area of the drive is the read pre-amp on the Encoder PCB. Because of Faraday's Law,

$$V = \frac{d\theta}{dt}$$

Where V = voltage/turn induced

θ = flux through the turn

only rapidly changing magnetic fields (high $d\theta/dt$) induce EMI errors. This means you should avoid rapidly changing currents in the neighborhood of the encoder PCB. For example, a 1 Amp 60 HZ current near the encoder will not create EMI errors since the current is slowly varying. However, a 50mA square wave of current has been observed to cause data errors. See Figure 3-2.

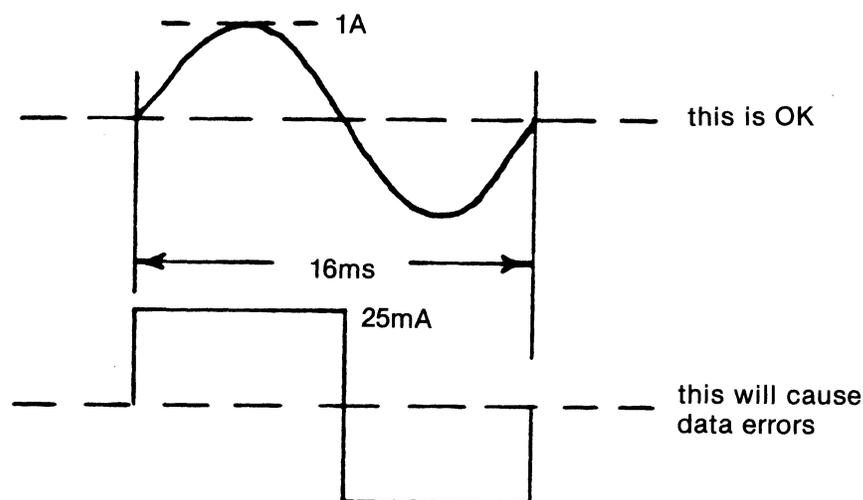
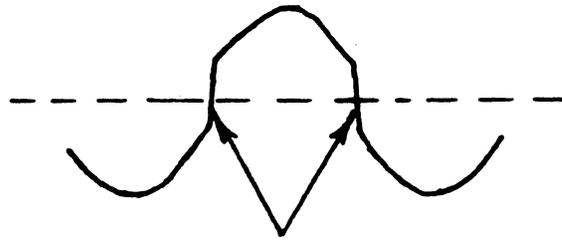


FIGURE 3-2
MAGNETIC INDUCED EMI ERROR

The current causing the problem was observed flowing *through the chassis* in close proximity to the encoder PCB. The current, caused by a switching power supply, is shown in Figure 3-3.



note the rapid
changes in current

FIGURE 3-3
CURRENT FLOW THROUGH CHASSIS

The best way to prevent magnetic coupling is to re-route the current. If this cannot be done, shield changing magnetic fields with sheets of conductor such as copper or aluminum.

3.7.2 GROUND CURRENT COUPLING

The second coupling method we have observed is through ground currents. The Q2080 has 3 possible grounding points: the DC ground at the DC power connector, the AC ground at the AC power connector, and ground to the base casting through the bubble clamps and cabinet. If currents run through the drive from one ground to another, they can induce voltages in the front end of the read channel and cause data errors. See Figure 3-4.

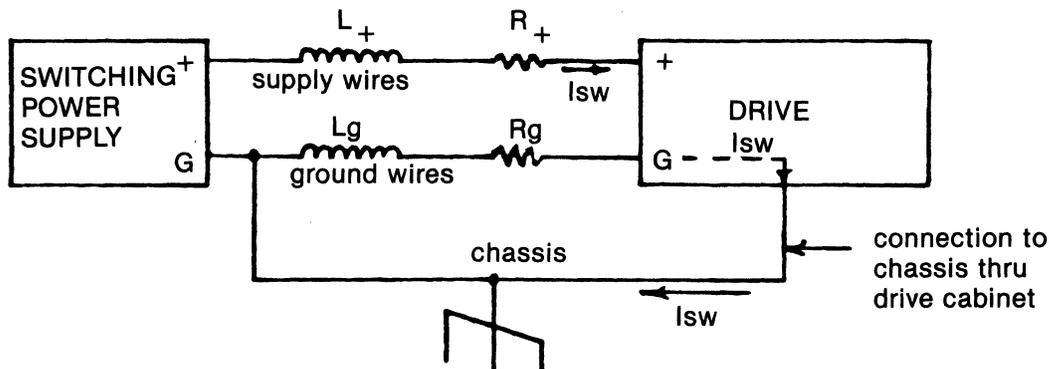


FIGURE 3-4
GROUND INDUCED EMI ERROR

Any noise spikes the switcher generates will be dropped across Z_+ (R_+ and L_+) and Z_G ($R_G + L_G$). If the impedance from the drive to the power supply is lower through the chassis than the impedance of the ground wire, the switching currents will flow from the DC connector through the drive to the chassis/cabinet connection. Currents from one ground to another traveling through the drive will induce data errors.

To solve a ground current EMI problem, prevent the noise currents from flowing through the drive. This can be done in three ways: (1) remove the source driving the current, (2) open one of the grounds, or (3) shunt the current around the drive. In the example, the designer could remove the driving source by using a power supply with lower output spikes or the driving source could also be removed by reducing the ground line impedance to stop 'pushing' the current through the chassis. Also, the path could be opened by insulating the drive cabinet from the chassis. Finally, current could be shunted by connecting the drive DC ground to the chassis. See Figure 3-5.

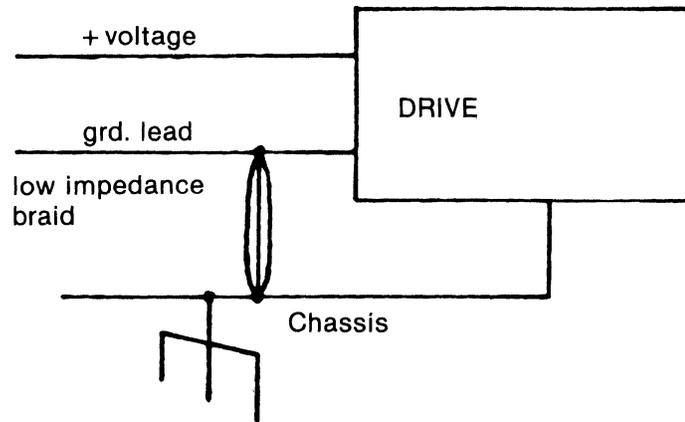


FIGURE 3-5
CONNECTING DRIVE GROUND TO CHASSIS

This last solution forces the currents to flow from DC ground to chassis ground *outside* the drive and eliminates the problem. The key to reducing ground current problems is to eliminate current flow from one ground to another.

SECTION 4 MAINTENANCE

4.1 GENERAL INFORMATION

A high degree of reliability has been achieved in the Model Q2080 through the simplicity of its mechanical design and the extensive use of microelectronics. The Model Q2080 is designed for fast, easy sub-assembly replacement with no adjustments. This greatly reduces the amount of downtime for unscheduled repairs.

4.2 MAINTENANCE PRECAUTIONS

To avoid damage to the Model Q2080 and personal injury to the service technician, observe the following precautions during service activity:

1. Avoid harsh shocks to the drive.
2. Do NOT open or remove the plastic bubble or its seals unless the drive is in a Class 100 clean environment.
3. Do not lift the drive by the face plate or the PCBA.
4. Do not move the drive for 30 seconds after power is removed to insure that the actuator is automatically locked.
5. Potentially hazardous AC voltage is present on the underside of the drive for the AC spindle drive motor.
6. Exercise caution when operating the drive with the cabinet and drive belt shield removed. Stay clear of the belt motor and spindle pulley.

4.3 PREVENTIVE MAINTENANCE

The Model Q2080 does not require any preventive maintenance.

4.4 MAINTENANCE PROCEDURES

Corrective maintenance on the Model Q2080 requires certain minimum levels of technical expertise and facilities. Capabilities in this area will vary greatly from user to user. Maintenance procedures for the Model Q2080 are categorized into two levels. The first level involves on-site exchange of sub-assemblies or the drive itself. The second level involves service center and/or factory repair or refurbishment of assemblies and the printed circuit board.

4.4.1 LEVEL 1 MAINTENANCE

Level 1 maintenance consists of circuit board exchange, external sub-assembly replacement, drive belt replacement, frequency and voltage conversions, and unit replacement.

Tools

The following tools are required for Level 1 maintenance procedures:

1. An assortment of hand tools adequate for electronic/mechanical repair
2. Two torque driver handles (preset to 14 and 22 in.-lbs) with a #8 Allen tip, a #2 Phillips tip, and a 3/32 hex socket tip.

Spare Parts

The following spare parts should be on hand when performing Level 1 maintenance procedures:

1. Drive control PCBA (Quantum Part No. 20-20800)
2. AC and/or DC drive motor
3. Drive power transistor assembly (Quantum Part No. 79-49075)

Frequency Conversion

The AC drive motor used in the Model Q2080 is able to operate on either 50 or 60 HZ at its rated voltage. The rotational speed of the motor is dependent on its input frequency and is slower at 50 HZ. To keep the spindle speed constant with the different motor speeds, two sizes of drive motor pulleys are used. Along with these two pulley sizes there are two different drive belt sizes. Table 4-1 lists the Part Numbers of these parts.

**TABLE 4-1
VOLTAGE AND FREQUENCY PARTS**

Voltage	POWER		PART NUMBERS		
	Frequency	Motor	Pulley	Belt	Motor/Pulley Assy.
110 VAC	60 HZ	73-40109	40-40015	50-40000	73-40226
110 VAC	50 HZ	73-40109	40-40032	50-40001	73-40227
220 VAC	60 HZ	73-40111	40-40015	50-40000	73-40228
220 VAC	50 HZ	73-40032	40-40001	50-40001	73-40111

To convert the drive for a change in the operating frequency, use the following procedure:

1. Select the pulley and belt for the desired frequency from Table 4-1.
2. Remove all power and interface cables from the drive and place the drive on the work surface.
3. Remove the cabinet assembly by removing the three Phillips head screws on the bottom of the cabinet that hold the assembly to the shock mounts.
4. Remove the capacitor clamp.
5. Remove the old drive belt.
6. Remove the old pulley by loosening the two Allen drive set screws using a #8 Allen wrench.
7. Install the new pulley. Ensure that one of the set screws will match the flat side on the shaft and the pulley is seated down so that there is .030 inches clearance between the top of the motor and the pulley.

NOTE

The 50 HZ pulley is larger than the 60 HZ. A 50 HZ belt can be identified by the white square on one side.

8. Tighten the set screws to 14 in.-lbs.
9. Install the new belt.
10. Reinstall the capacitor clamp.
11. Reinstall the cabinet assembly.
12. Reinstall the drive and test as required.

Voltage Conversion

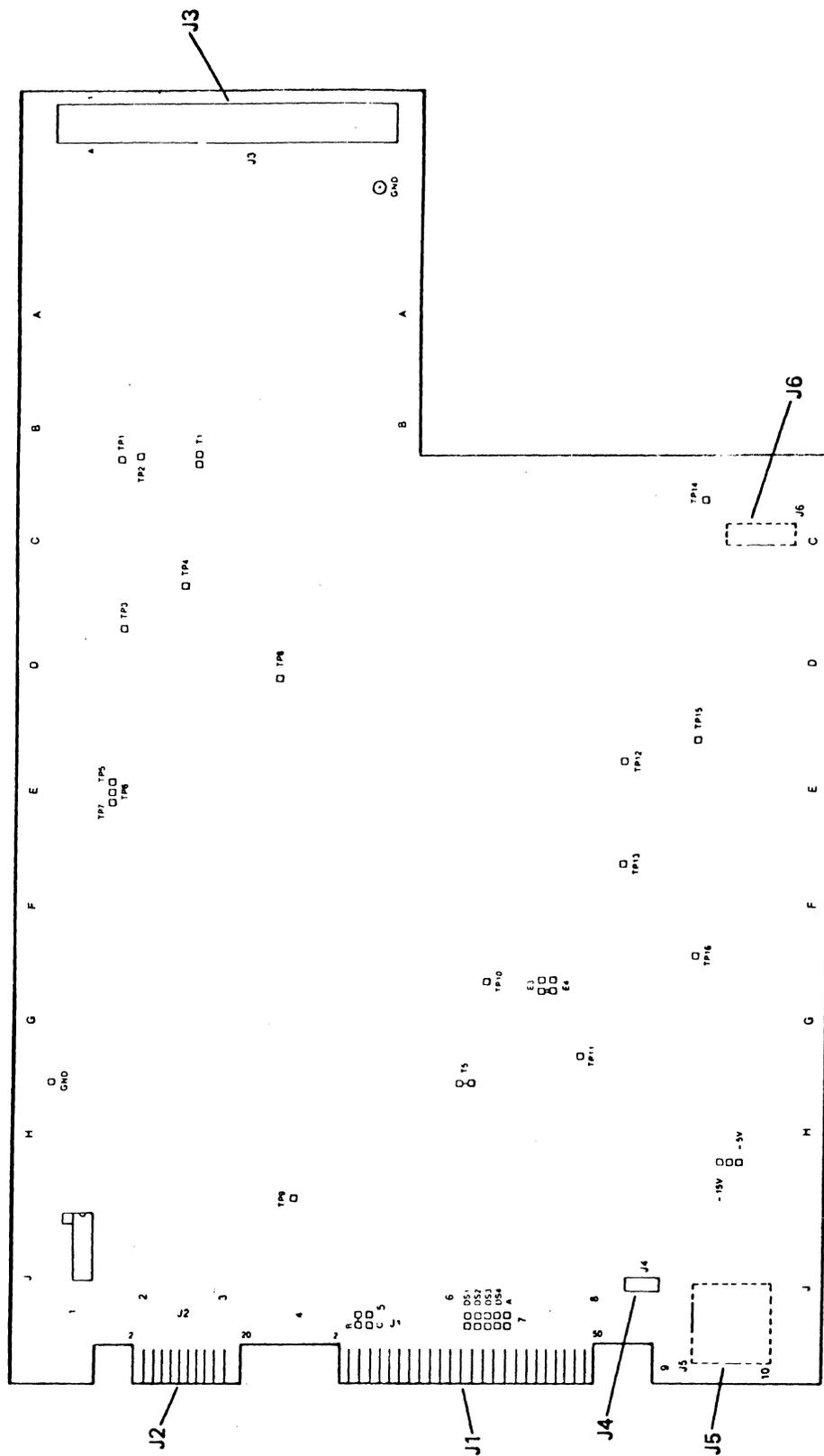
The Model Q2080 AC drive operates within two voltage ranges. The voltage ranges are 90 to 127 VAC, and 180 to 253 VAC. To convert from one range to the other it is necessary to exchange the motor for one operating in the desired voltage range. Table 4-1 lists the Part Numbers of the two motor assemblies. To change motors proceed as follows:

1. Select the required motor assembly from Table 4-1.
2. Remove all power and interface cables from the drive and place the drive on the work surface.
3. Remove the cabinet assembly from the drive by loosening the three Phillips head screws on the cabinet.
4. Remove the belt guard by loosening the two Phillips head screws.
5. Remove the drive belt.
6. Remove the AC input connector J4 from its bracket.

7. Disconnect the AC ground wire from the chassis. The wire runs from the AC Motor to the bottom side of the base casting where it is secured by a Phillips screw.
8. Remove the motor leads from the tywrap hold downs by cutting the tywraps. Be careful not to damage the wires.
9. Remove the motor by loosening and removing the 3/32 inch mounting nuts.
10. Installation of the new motor is the reverse of the foregoing steps.
11. Torque the mounting nuts to 22 in.-lbs.

Replacement of Drive Control PCB

1. Remove the interface and DC power cables, the drive transistor cable and the index cable. See Figure 4-1 for the connector locations.
2. Remove the four Phillips head screws holding the PCB to the drive.
3. Gently lift the PCB off the transducer connector at the narrow end of the PCB.
4. Install the new PCB in the reverse order of the foregoing steps.
5. Torque the hold down screws to 14 in.-lbs.



**FIGURE 4-1
CONNECTOR LOCATIONS**

Replacement of the Drive Power Transistor Assembly

1. Remove all power and interface cables from the drive and place the drive on the work surface.
2. Remove the cabinet assembly from the drive.
3. Gently remove the drive transistor cable connector from the control PCB.
4. Remove the belt guard and drive belt from the drive.
5. Remove the drive transistor leads from the tywrap hold downs.
6. Remove the AC connector J4 from the drive transistor mounting bracket.
7. Detach the drive transistor assembly by loosening the hold down screw. Refer to Figure 4-1 for screw location.
8. Install the new power transistor assembly in the reverse order of the foregoing.
9. Torque the hold down screws to 22 in.-lbs.

4.4.2 LEVEL 2 MAINTENANCE

Level 2 maintenance involves major disassembly and refurbishment of the drive and repair of the circuit boards.

If the ability to do Level 2 repairs is required, please contact Quantum for information.

NOTE

The user's service activity should be limited to only Level 1 procedures. The Quantum warranty is null and void when any Level 2 procedure has been attempted. In addition, no sub-bubble repairs are authorized. All time and material required to restore the drive to working order after unauthorized Level 2 procedures have been attempted will be billed at prevailing rates.

SECTION 5

ILLUSTRATED PARTS BREAKDOWN

5.1 GENERAL DISCUSSION

This section illustrates the various sub-assemblies and component parts of the Q2080. Quantum part numbers are listed by call out numbers on the exploded drawings. Both Quantum and commercial part numbers are given for those electronic parts where appropriate.

5.2 MAJOR ASSEMBLIES

Figure 5-1 is an exploded view of the drive showing

1. Cabinet assembly
2. Drive control PCBA
3. Drive assembly

5.3 SUB-ASSEMBLIES

Figure 5-2 shows an exploded view of the Drive Assembly showing all replaceable parts of the drive; bubble, head arms, disks, AC motor, etc.

Figure 5-3 shows an exploded view of the Drive Power Op Amp Assembly.

Figure 5-4 shows an exploded view of the Actuator Sub-Assembly.

Figure 5-5 shows an exploded view of the Spindle and Disk Sub-Assembly.

Figure 5-6 shows an exploded view of the Head Arm Sub-Assembly.

Figure 5-7 shows an exploded view of the Cabinet Sub-Assembly.

Figure 5-8 shows an exploded view of the AC Drive Motor Assembly.

Figure 5-9 shows an exploded view of the DC Drive Motor Assembly.

Figure 5-10 shows an exploded view of the Bubble Sub-Assembly.

5.4 PRINTED CIRCUIT BOARDS

5.4.1 ENCODER PCB

Figure 5-11 shows the component layout of the Encoder PCB Assembly.

5.4.2 DRIVE CONTROL PCB

Figure 5-12 shows the component layout of the Drive Control PCB Assembly.

Throughout this section notes are used to indicate parts that are not field replaceable, e.g., bottom motor plate, rotor, spindle, etc. All under bubble parts are only available to Quantum qualified repair centers.

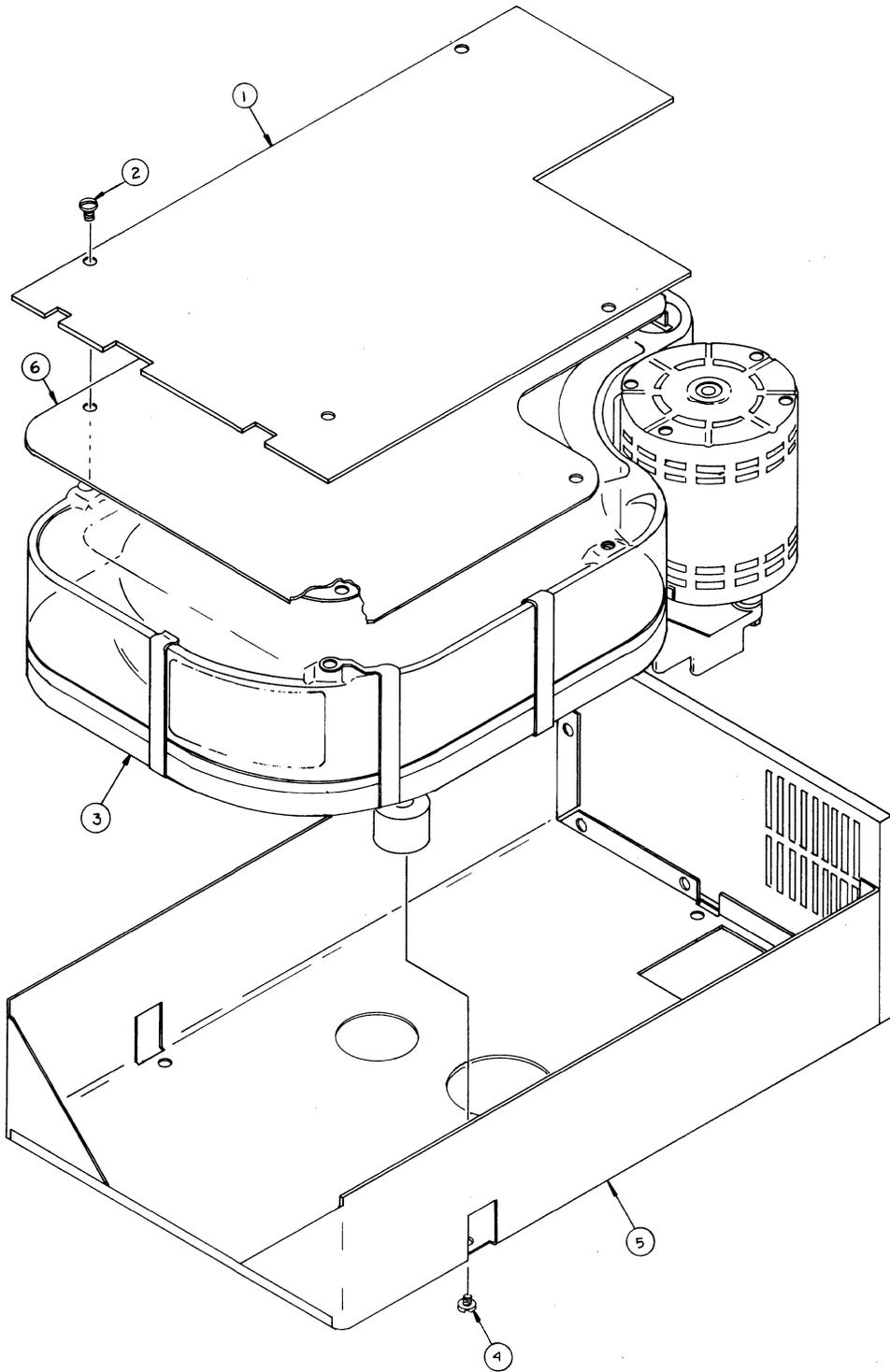


FIGURE 5-1
MAJOR ASSEMBLIES

Q2080 MAJOR ASSEMBLIES

Item	Part Number	Description
1.	20-20800	Drive Control PCB (See Figure 5-12)
2.	54-10104	Screw, 8-32 X .38 (3)
3.	NA	Drive Assembly (See Figure 5-2)
4.	54-10226	Screw, Flat head, 8-32 X .25 (3)
5.	75-40190	Cabinet Sub-Assembly (See Figure 5-7)
6.	50-49182	Shield, Bubble QE

DRIVE ASSEMBLY

Item	Part Number	Description
1.	75-49120	Belt Guard Assembly QE
2.	20-20816	Power Op Amp Assembly (See Figure 5-3)
3.	36-4019	Shock Mounts (3)
4.	NA	Spindle and Disk Assembly (See Figure 5-5)
5.	75-40200	Bubble Assembly (See Figure 5-10)
6.	38-40003	Filter, Circulation
7.	NA	Head Arm Assembly (See Figure 5-6)
8.	75-49084	Encoder Assembly
9.	73-49074	Index Assembly
10.	NA	Motor Capacitor (See Figure 5-8)
11.	NA	Actuator Sub-Assembly (See Figure 5-4)
12.	NA	AC Motor Assembly (See Figure 5-8)

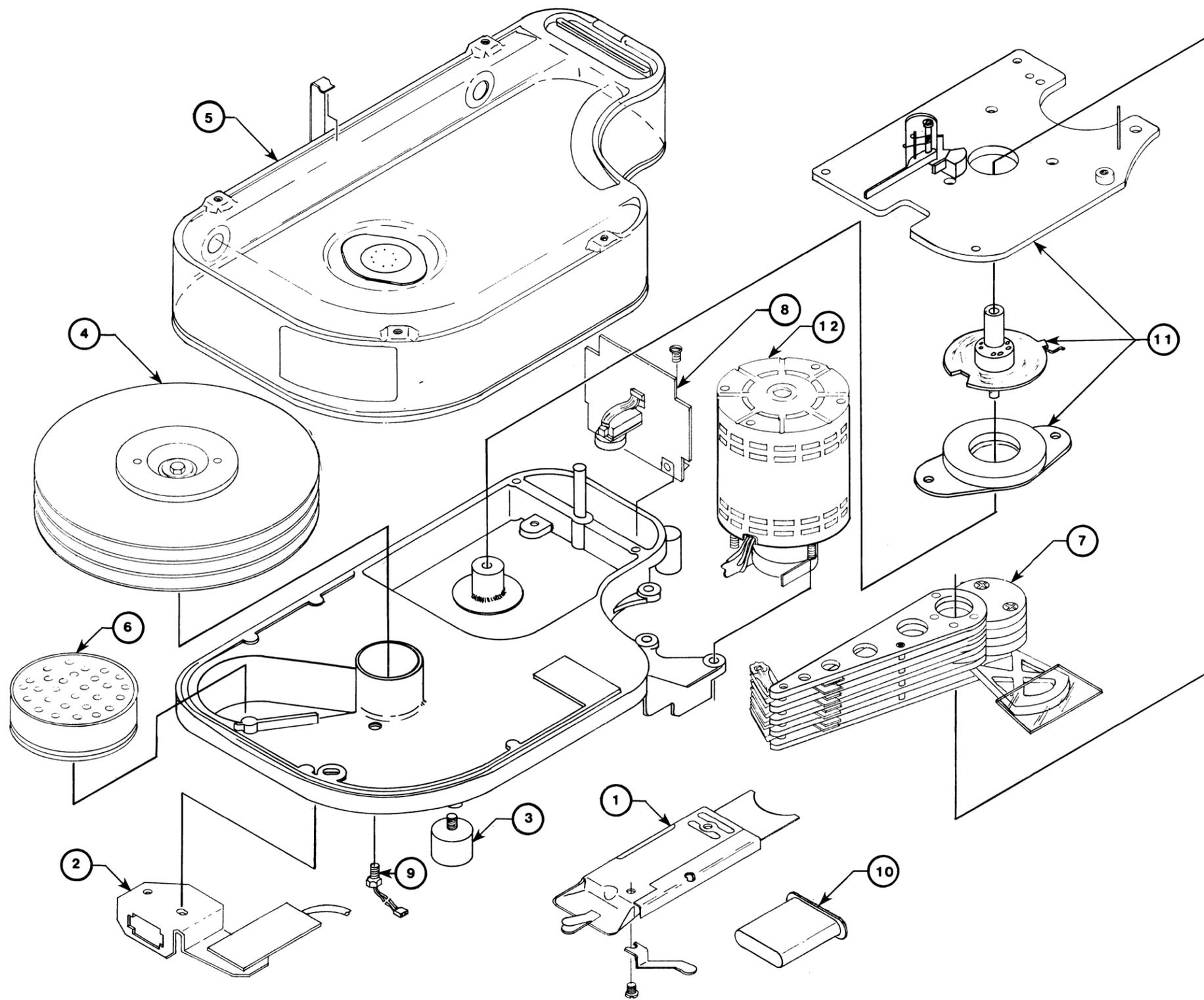


Figure 5-2
Exploded Drive Assembly

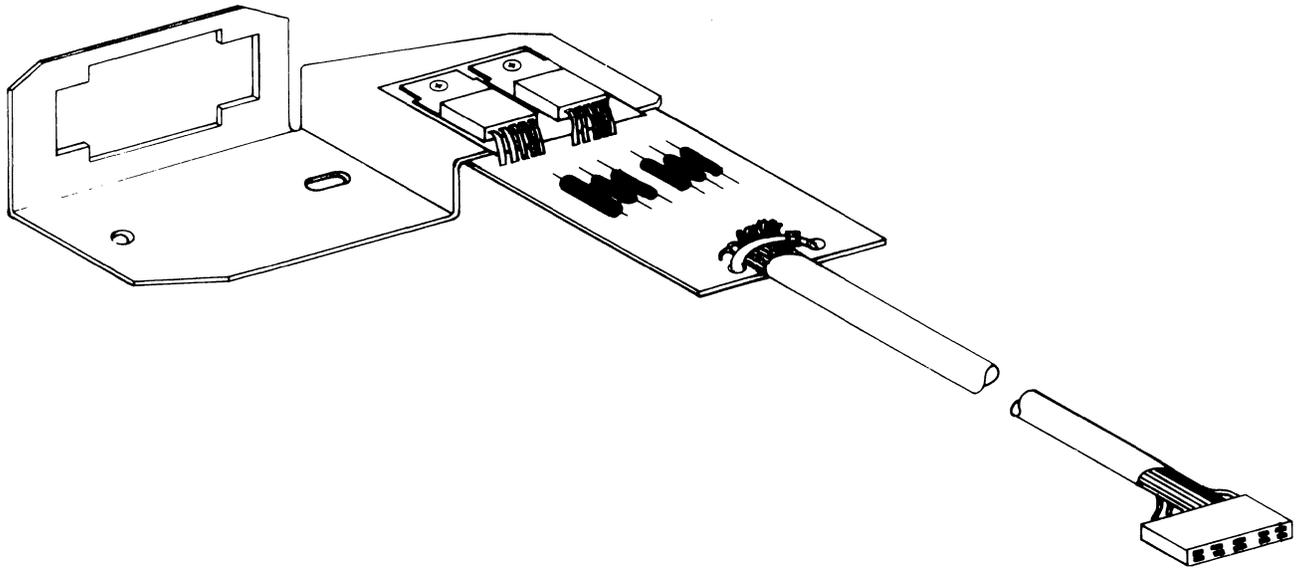


FIGURE 5-3
POWER OP AMP ASSEMBLY
PART NUMBER 20-20816

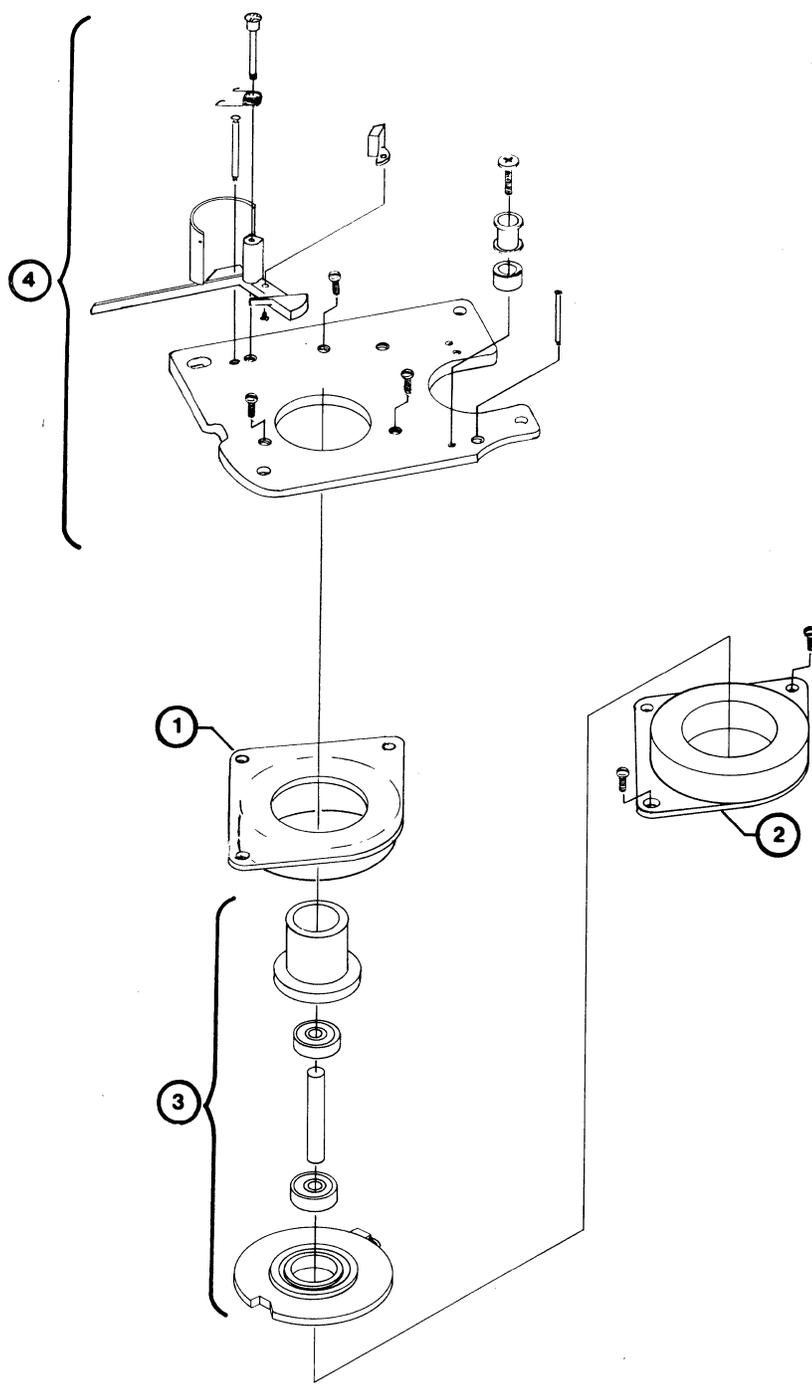
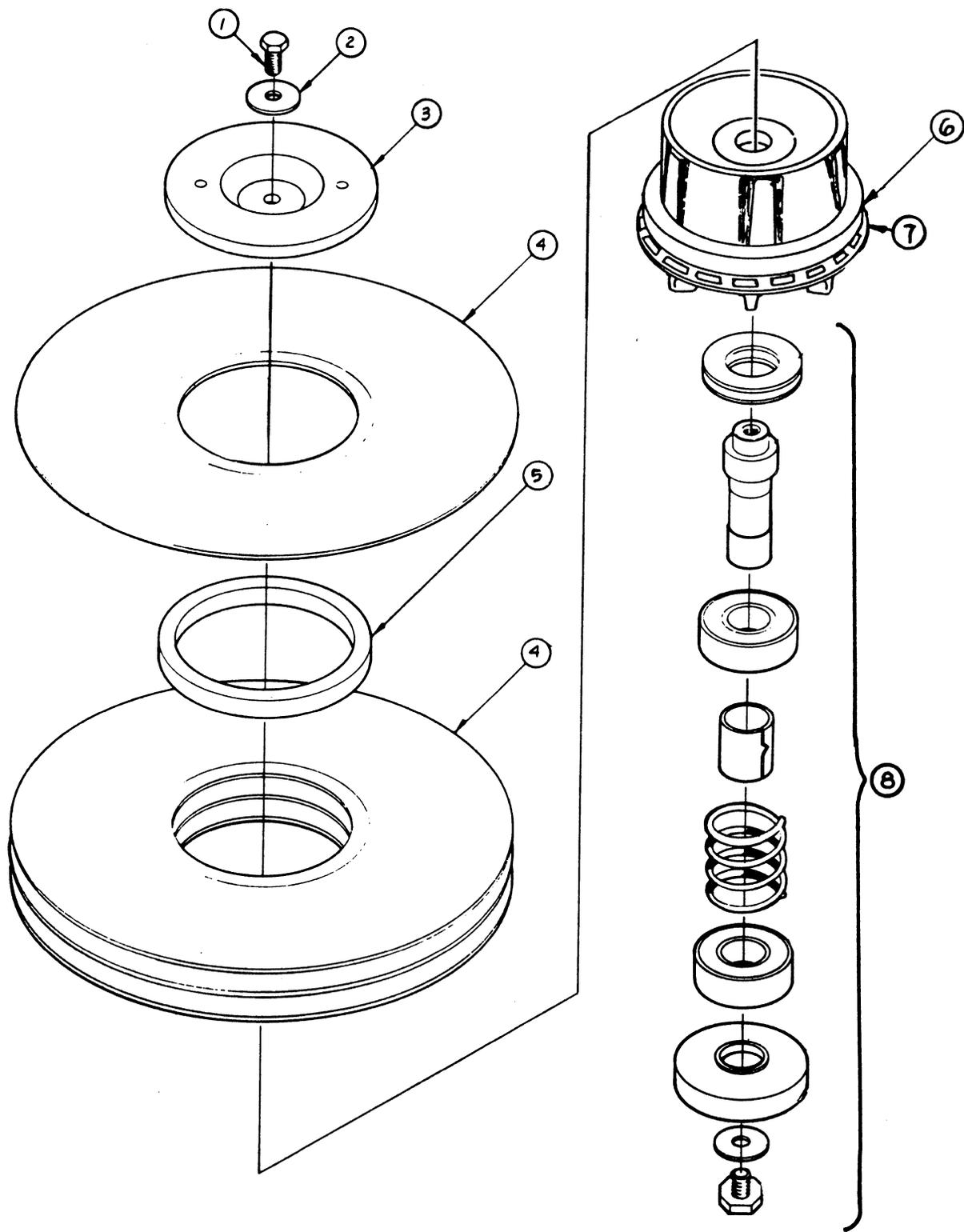


FIGURE 5-4
ACTUATOR SUB-ASSEMBLY

ACTUATOR SUB-ASSEMBLY

Item	Part Number	Description
1.	75-49078	Lower Magnet Plate
2.	75-49083	Upper Magnet Plate
3.	75-49087	Armature, QE
4.	75-49141	Airlock Assembly, QE



**FIGURE 5-5
SPINDLE AND DISK SUB-ASSEMBLY**

SPINDLE AND DISK SUB-ASSEMBLY

Item	Part Number	Description
1.	54-10213	Screw, .25-20 x .62
2.	57-10090	Washer, Spindle Flat
3.	40-40033	Clamp, Disk
4.	61-49004	Disk, 200 mm QE (4)
5.	40-40025	Spacer, Common Disk (3)
6.	40-49132	Hub, Spindle QE
7.	40-49108	Index Ring QE
8.	75-40095	Shaft Assembly, Spindle

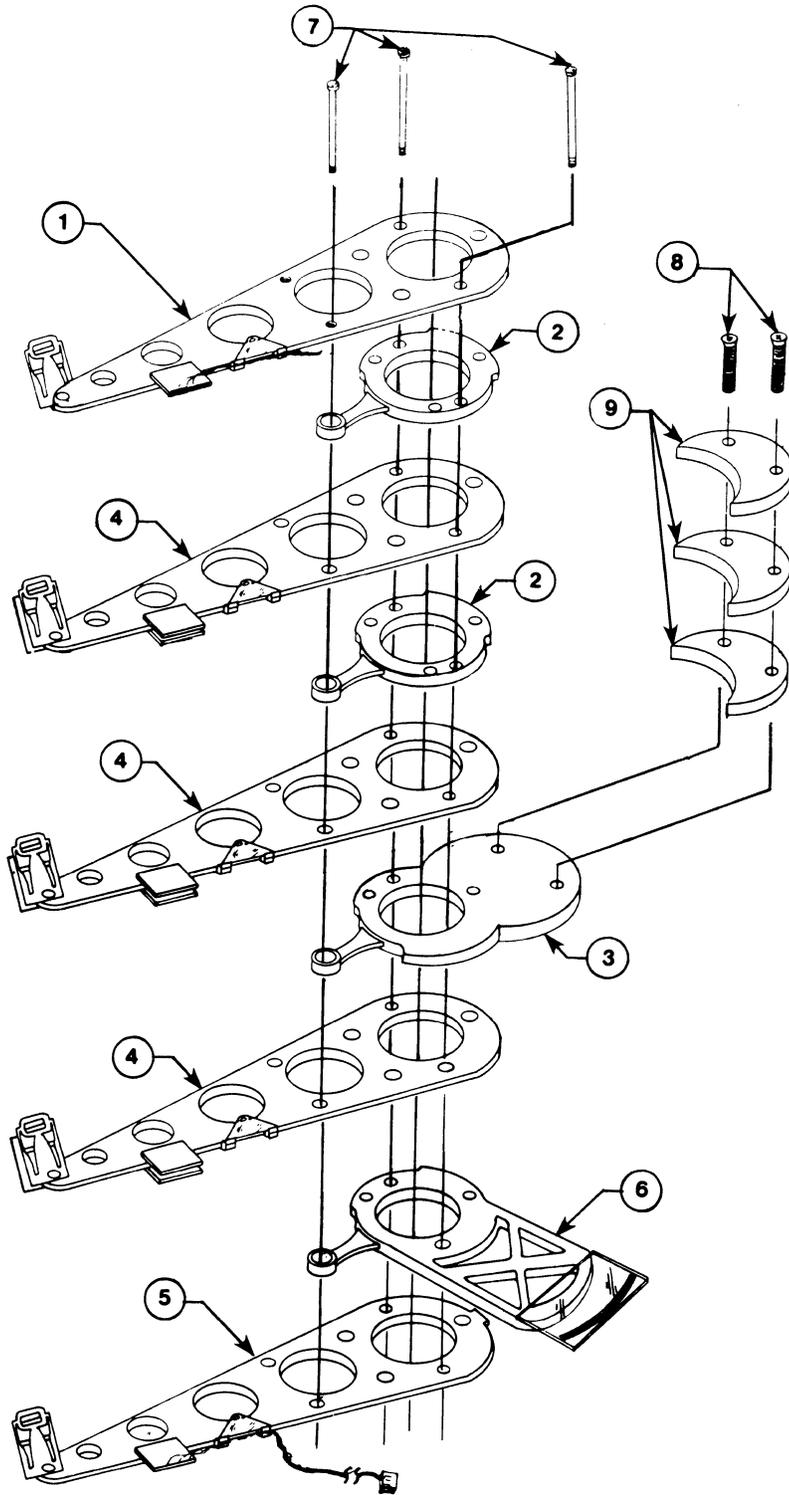


FIGURE 5-6
HEAD ARM SUB-ASSEMBLY

HEAD ARM SUB-ASSEMBLY

Item	Part Number	Description
1.	75-49017	Arm Assembly, Upper Head
2.	40-49174	Spacer, Arm (2)
3.	40-49176	Spacer, Guitar
4.	75-49023	Arm Assembly, Dual Head (3)
5.	75-49097	Arm Assembly, Lower Head
6.	75-49106	Scale Mount Assembly
7.	54-10176	Screw, Hex Head, 4-40 x 1.62 (3)
8.	54-10229	Screw, Phillips Flat Head, 8-32 1.0 (2)
9.	40-49178	Counterbalance (3)

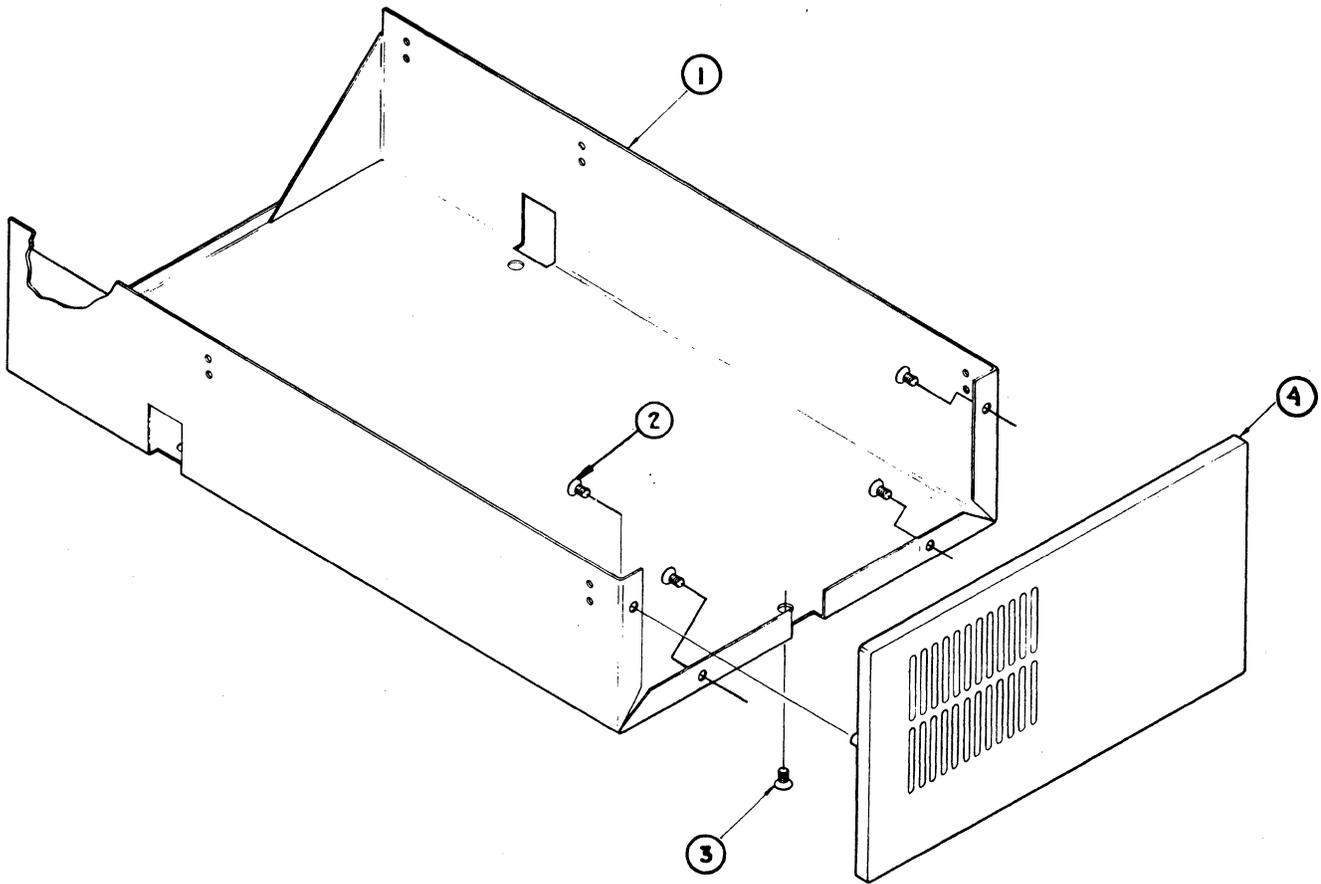
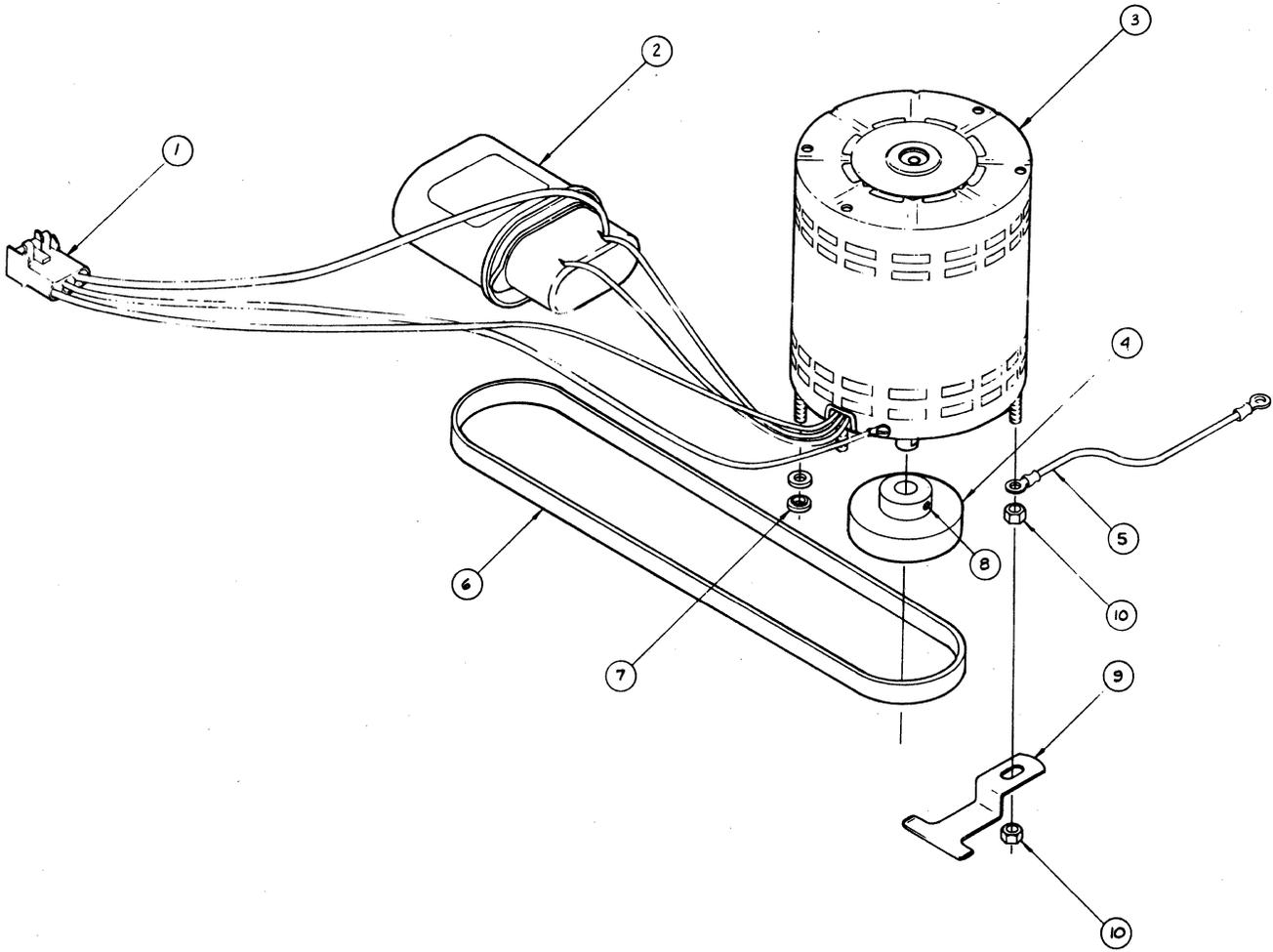


FIGURE 5-7
CABINET SUB-ASSEMBLY

CABINET SUB-ASSEMBLY 75-40190

Item	Part Number	Description
1.	59-40045	Cabinet
2.	54-10112	Screw, Phillips Head, 6-32 x .19 (4)
3.	54-10226	Screw, Flat Head, 8-32 x .25 (3)
4.	48-40253	Plate, Molded Face



**FIGURE 5-8
AC DRIVE MOTOR**

AC DRIVE MOTOR

Item	Part Number	Description
1.	22-10003	Housing, AC Connector
	22-10006	Pin, AC Ground
	22-10004	Pin, AC (2)
	31-10050	Wire, 18GA Yellow/Green (AC Ground)
	31-10051	Wire, 18GA White (AC)
2.	03-10088	Capacitor 110 VAC
	03-10089	Capacitor, 220 VAC
3.	26-40006	Motor, Drive 110 VAC
	26-40007	Motor, Drive 220 VAC
4.	40-40015	Pulley, Motor 60 HZ
	40-40032	Pulley, Motor 50 HZ
5.	74-40180	Strap, AC Motor Ground
6.	50-40000	Belt, Drive 60 HZ
	50-40001	Belt, Drive 50 HZ
7.	57-40039	Washer, Motor Insulating (6)
8.	54-10205	Setscrew, Cup Point 8-32 X .19 (2)
9.	43-40035	Clamp, Pulley Shipping
10.	56-10304	Nut 8-32 X (5)

Note 1 Motor Assembly with pulley, capacitor, and connector for:

110 VAC 60HZ 73-40226

110 VAC 50HZ 73-40227

220 VAC 60HZ 73-40228

220 VAC 50HZ 73-40229

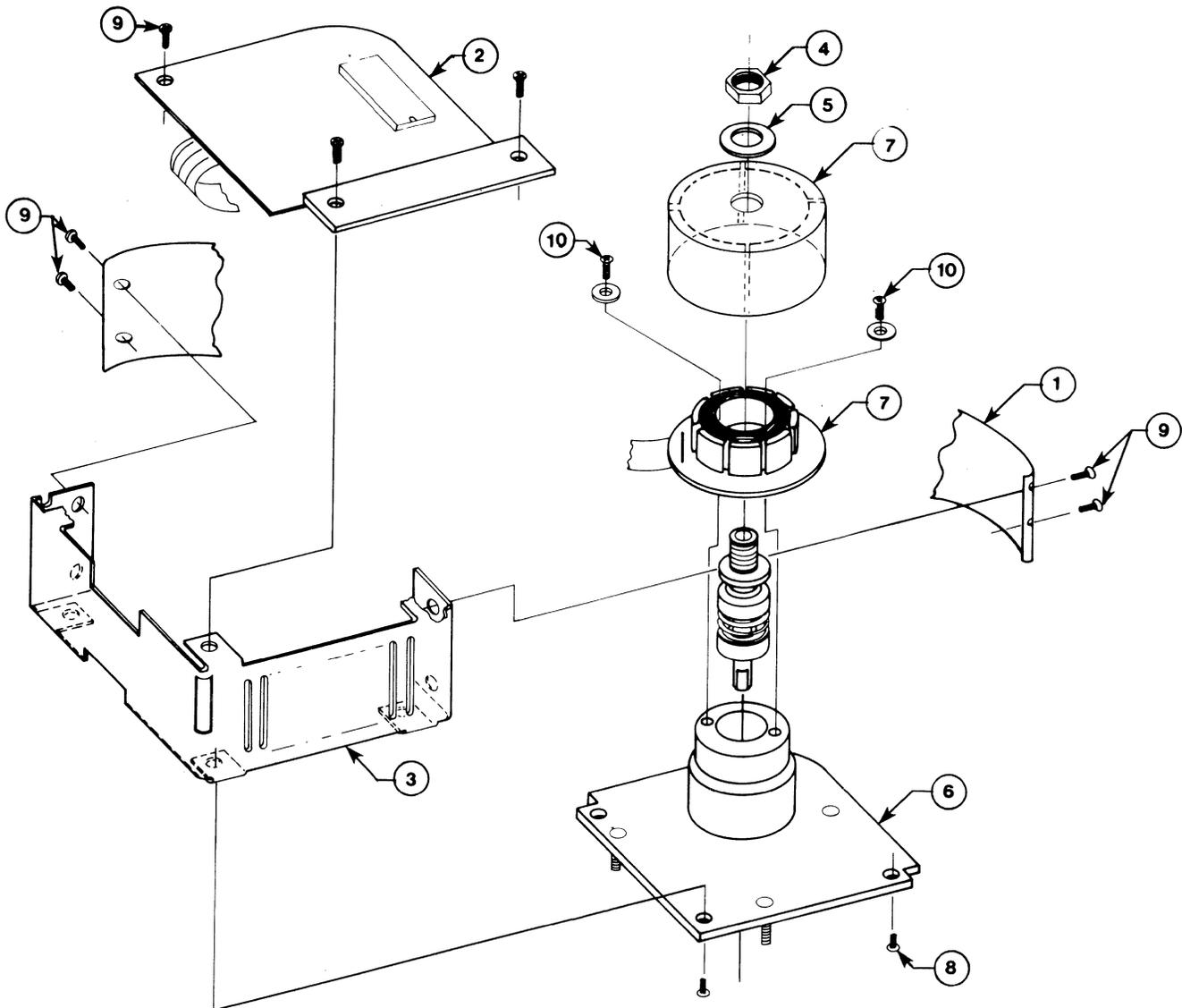


FIGURE 5-9
DC DRIVE MOTOR ASSEMBLY

DC DRIVE MOTOR ASSEMBLY (See Note 1)

Item	Part Number	Description
1.	59-40371	Shield, DC Motor
2.	20-20025	PCB, DC Motor, Control
3.	43-40344	Bracket, PCB Sinking
4.	56-10311	Nut, Jam, ½-20
5.	57-10456	Lockwasher, IT, ½
6.	75-40354	Spindle/Housing Assembly
7.	27-40366	Rotor/Stator Assembly
8.	54-10228	Screw, Flat Head, 8-32 x .38 (3)
9.	54-10104	Screw, Phillips, 8-32 x .38 (7)
10.	54-10143	Screw, Phillips, 4-40 x .25 (2)

Note 1: DC Motor Assembly with pulley and connector is 73-40355.

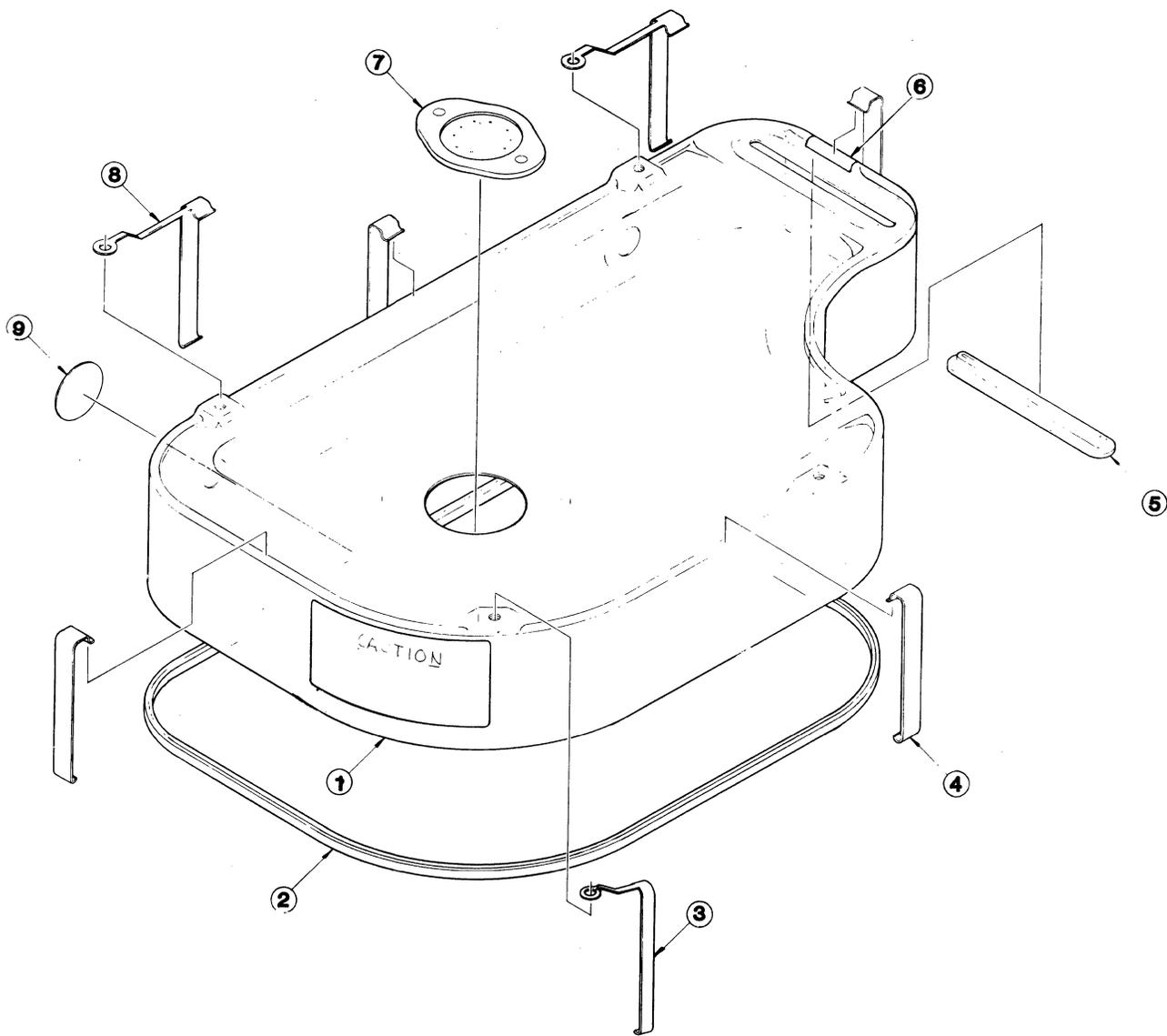
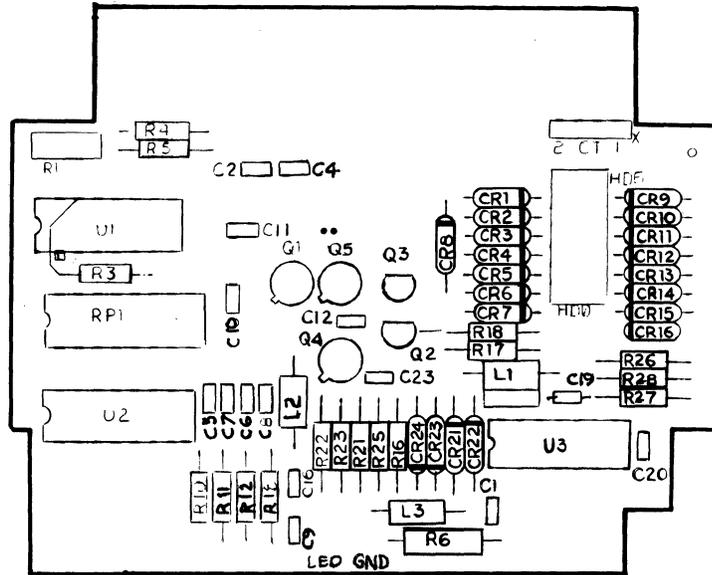


FIGURE 5-10
BUBBLE SUB-ASSEMBLY

BUBBLE SUB-ASSEMBLY

Item	Part Number	Description
1.	48-40207	Bubble, Injected
2.	75-40034	Gasket Assembly Bubble Seal
3.	43-40154	Clamp, Bubble, Short Ground
4.	43-40058	Clamp, Bubble (4)
5.	46-40046	Seal, Actuator
6.	51-40163	Label, Shield
7.	38-40002	Filter, Breather
8.	43-40155	Clamp, Bubble, Long Ground (2)
9.	51-40085	Label, Seal



**FIGURE 5-11
ENCODER PCB ASSEMBLY**

ENCODER PCB ASSEMBLY

Ref.	Part Number	Description	Ref	Part Number	Description
RESISTORS					
R1	06-12314	1M,20	R18	01-12215	8.06K, 1/8w 1%
R4	01-12031	82K, 1/4w 5%	R21, 23,26	01-12202	1K, 1/8w 1%
R6	01-20100	10, 1/4w 5%	R22	01-12206	5.11K, 1/8w 1%
R16,17, 27, 28	01-12203	1.69K, 1/8w 1%	R25	01-12204	2.49K, 1/8w 1%
CAPACITORS					
C2,4,9 10,11,12, 16,19,23, 20,1	03-00104	.1UF ± 10%	C5-8	03-16009	33PF ± 10%
INDUCTORS					
L1,2,3	04-16506	FERRITE BEAD			
TRANSISTORS					
Q1,4,5	16-14001	2N2222A	Q2,3	16-00000	MPS-H10
DIODES					
CR1-16, 21-24	16-14012	IN4148 (ITT DIODES ONLY)			
INTEGRATED CIRCUITS					
U1,2	13-18233	QUAD OP AMP	U3	13-18204	NE592 14 PIN DIP
MISCELLANEOUS					
P5	22-10395	HDR, 4 POS., SRT (TIN)	---	10-20805	ENCDR, DIAG. PCB FAB
P6	22-10466	HDR, 7 POS., STR (GOLD)	---	40-10396	RVT, 1/8" DIA by 3/6"
---	22-10467	HDR, 3 POS. (GOLD)	---	22-10404	SOCKET, PIN
RPI	02-12309	RES. PK, 4.7K, 16 PIN DIP	---	58-40065	LIP TRNSDCR PCB

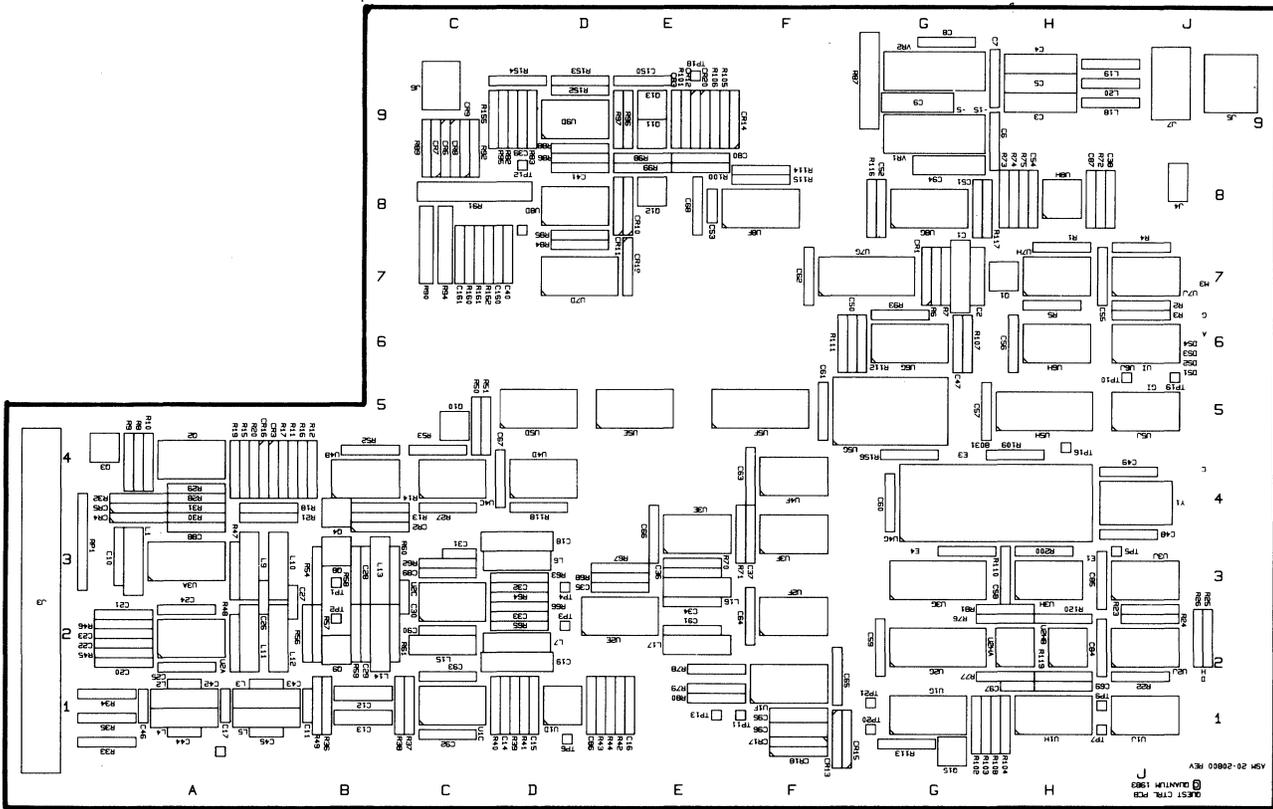


FIGURE 5-12
DRIVE CONTROL PCB ASSEMBLY

DRIVE CONTROL PCB ASSEMBLY

Ref.	Part Number	Description	Ref.	Part Number	Description
RESISTORS					
R1	01-12015	5.1K, 1/4w, 5%	R40	01-12005	330, 1/4w, 5%
R2	01-12004	220, 1/4w 5%	R41	01-12207	1.50K, 1/8w, 1%
R3	01-12005	330, 1/4w 5%	R42	01-12012	2K, 1/4w, 5%
R4	01-12012	2K, 1/4w 5%	R43	01-12024	200K, 1/4w, 5%
R5	01-12018	20K, 1/4w, 5%	R44	01-12048	100K, 1/4w, 5%
R6	01-12016	10K,1/4w, 5%	R45-46	01-05620	562,1/8w, 1%
R7	01-12003	120,1/4w, 5%	R47-48	01-12201	249,1/8w, 1%
R8	01-12001	20, 1/4w, 5%	R49	01-07500	750, 1/8w, 1%
R9	01-12005	330, 1/4w, 5%	R50	01-12047	2.7K, 1/4w, 5%
R10	01-12006	510, 1/4w, 5%	R51	01-12012	2K, 1/4w, 5%
R11	01-12012	2K, 1/4w, 5%	R52-53	01-12015	5.1K, 1/4w, 5%
R12	01-12015	5.1K, 1/4w, 5%	R54	01-12002	51, 1/4w, 5%
R13	01-12012	2K, 1/4w, 5%	R56	01-12202	1.0K, 1/8w, 1%
R14	01-12015	5.1K, 1/4w, 5%	R57	01-12002	51, 1/4w, 5%
R15	01-01620	162, 1/8w, 1%	R58-59	01-12006	510, 1/4w, 5%
R16	01-12005	330, 1/4w, 5%	R60-61	01-12201	249, 1/8w, 1%
R17	01-12012	2K, 1/4w, 5%	R62	01-12003	120, 1/4w, 5%
R18	01-12004	220, 1/4w, 5%	R63	01-12002	51, 1/4w, 5%
R19	01-12049	510K, 1/4w, 5%	R64	01-12012	2K, 1/4w, 5%
R20-22	01-12912	2K, 1/4w, 5%	R65	01-12002	51,1/4w, 5%
R23-26	01-12002	51,1/4w, 5%	R66-67	01-12012	2K, 1/4w, 5%
R27	01-12006	510, 1/4w, 5%	R68	01-12014	6.8K, 1/4w, 5%
R28	01-12004	220, 1/4w, 5%	R70-71	01-12003	120, 1/4w, 5%
R29	01-12012	2K, 1/4, 5%	R72	01-12008	1K, 1/4w, 5%
R30-31	01-12018	20K, 1/4w, 5%	R73	01-12015	5.1K, 1/4w, 5%
R32	01-12007	560, 1/5w, 5%	R74	01-12006	510, 1/4w, 5%
R33	01-12008	1K, 1/4w, 5%	R75	01-20473	47K, 1/4w, 5%
R34-36	01-07500	750, 1/8w, 1%	R76-77	01-12202	1.0K, 1/8w, 1%
R37-39	01-12012	2K, 1/4w, 5%	R78	01-01002	10.0K, 1/8, 1%

DRIVE CONTROL PCB ASSEMBLY

Ref.	Part Number	Description	Ref.	Part Number	Description
RESISTORS (con't)					
R79-80	01-12002	51, 1/4w, 5%	R105	01-12008	1K 1/4w, 5%
R81	01-04991	4.99K, 1/8w 1%	R106	01-12006	510, 1/4w, 5%
R82	01-01002	10.0K, 1/8w 1%	R107	01-12254	124K, 1/8w, 1%
R83	01-12204	2.49K, 1/8w 1%	R108	01-04991	4.99K, 1/8w, 1%
R84	01-01002	10.0K, 1/8w, 1%	R109	01-12008	1K, 1/4w, 5%
R85	01-12253	121K, 1/8w, 1%	R110	01-12012	2K, 1/4, 5%
R86	01-03012	30.1K, 1/8w, 1%	R111	01-12020	36K, 1/4w, 5%
R87	01-30002	150, 2w, 5%	R112	01-12012	2K, 1/4w, 5%
R88-89	01-12245	100K, 1/8w, 1%	R113	01-12005	330, 1/4w
R90	01-30003	G8, 1w, 5%	R114-115	01-04991	4.99K, 1/8w, 1%
R91	01-12300	1, 2w, 5%	R116	01-20222	2.2K, 1/4w, 5%
R92	01-12245	100K, 1/8w, 1%	R117	01-04022	40.2K, 1/8w, 1%
R93	01-12008	1K, 1/4w, 5%	R118	01-12012	2K, 1/4w, 5%
R94	01-30003	68, 1w, 5%	R119-20	01-12008	1K, 1/4w, 5%
R95-97	01-12245	100K, 1/8w, 1%	R151	01-12012	2K, 1/4w, 5%
R98	01-12006	510, 1/4w, 5%	R152-155	01-01002	10.0K, 1/8w, 1%
R99	01-12012	2K, 1/4w, 5%	R156	01-12012	2K, 1/4w, 5%
R100	01-12006	510, 1/4w, 5%	R157-58	01-12026	1M, 1/4w, 5%
R101	01-12005	330, 1/4w, 5%	R160-161	01-04022	40.2K, 1/8w, 1%
R102-103	01-14991	4.99K, 1/8w, 1%	R162	01-03243	324K, 1/8w, 1%
R104	01-20135	1.3M, 1/4w, 5%	R200	01-12012	2K, 1/4w, 5%

CAPACITORS

C1	03-16201	4.7uF ± 10%, 35V	C10	03-02104	0.1uF ± 80%-20%, 50V
C2	03-00104	0.1uF ± 10%, X7R Cer.	C11	03-30151	150pF ± 5% MICA
C3-5	03-16201	4.7uF ± 10%, 35V	C12-13	03-00104	0.1uF ± 10%, X7R Cer.
C6-8	03-02104	0.1uF ± 80%-20%, 50V	C14	03-00102	.001uF ± 10%, X7R Cer.
C9	03-16201	4.7uF ± 10%, 35V	C15	03-01101	100pF ± 5%, NPO Cer.

DRIVE CONTROL PCB ASSEMBLY

Ref.	Part Number	Description	Ref.	Part Number	Description
CAPACITORS (con't)					
C16	03-30471	470pF \pm 5% MICA	C43	03-30161	160pF \pm 5% MICA
C17	03-30251	250pF \pm 5% MICA	C44	03-30560	56pF \pm 5% MICA
C18-19	03-16201	4.7uF \pm 10%, 35V	C45	03-30161	160pF \pm 5% MICA
C20-21	03-02104	0.1uF \pm 80%-20%, 50V	C46	03-16203	180pF \pm 5% MICA
C22-23	03-00103	.01uF \pm 10%, X7R Cer.	C47	03-16010	.01uF \pm 5% NPO Cer.
C24-25	03-02104	0.1uF \pm 80%-20%, 50V	C48-49	03-01220	22pF \pm 5% NPO Cer,
C26	03-16202	62pF \pm 50% MICA	C51-52	03-00103	.01uF \pm 10% X7R Cer.
C27	03-16203	180pF \pm 5% MICA	C53	03-16211	75pF \pm 5% MICA
C28-29	03-00103	.01uF \pm 10%, X7R Cer.	C54-68	03.02104	.01uF \pm 80%-20%, 50V
C30	03-16208	39pF \pm 5% MICA	C69	03-00103	.01uF \pm 80%, X7R Cer.
C32-33	00103	.01uF \pm 10%, X7R Cer.	C70-72	03-16201	4.7uF \pm 10%, 35V
C35	03-01220	22pF \pm 5%, NPO Cer.	C73-74,	03-02104	0.1uF \pm 80%-20%,
C36-37	03-01101	00pF \pm 5%, NPO Cer.	80,83-93		50V
C38	03-00103	.01uF \pm 10% X7R Cer.	C94	03-16201	4.7uF \pm 10%, 35V
C39	03-16010	.01uF \pm 5%	C95-96	03-00104	0.1uF \pm 10%, X7R Cer.
C40	03-16011	.015uF \pm 5%	C97	03-30471	470pF \pm 5% MICA
C41	03-30681	680pF \pm 5% MICA	C150	03-02104	0.1uF \pm 80%-20%, 50V
C42	03-30560	56pF \pm 5% MICA	C160	03-01101	100pF \pm 5%, NPO Cer.
			C161	03-16010	.01uF \pm 5%

INDUCTORS

L1	04-16500	2.2uH	L11	04-16501	2.7uH
L2	04-00181	180uH Shielded	L12	04-16502	12uH
L3	04-16504	150uH Shielded	L13-14	04-16507	15uH
L4	04-00181	180uH Shielded	L15-17	04-16500	2.2uH
L5	04-16504	150uH Shielded	L18-20	04-165-6	Bead
L6-7	04-16503	18uH Shielded			
L9	04-16501	2.7uH			
L10	04-16502	12uH			

DRIVE CONTROL PCB ASSEMBLY

Ref.	Part Number	Description	Ref.	Part Number	Description
TRANSISTORS					
Q1	16-14001	2N2222A	Q8-9	16-14001	2N2222A
Q2	13-18203	Q2T2905 or FPQ2907 Transistor Array	Q10-11	16-14002	2N2907A
Q3	16-14002	2N2907A	Q12-13	2N2222A	
Q4	16-14001	2N2222A	Q15	13-90001	LM336 2.5V Ref.
DIODES					
CR1	16-30027	IN5227B 3.6V Zener	CR12	16-30033	IN5233B 6.0V Zener
CR2-3	16-14005	IN5225B 3.0V Zener	CR13	16-14012	In4148 (ITT only)
CR4-5	16-14012	IN4148 (ITT only)	CR14	16-30033	IN5233B 6.0V Zener
CR6-9	16-14018	IN4002	CR15-19	16-14012	IN4148 (ITT only)
CR10	16-14012	IN4148 (ITT only)	CR20	16-20003	II DQ03, Schottky
CR11	16-14005	IN5225B 3.0V Zener			
INTEGRATED CIRCUITS					
U1C	13-18204	NE592 (Video Amp)	U4D	13-18005	74LS08
U1D	13-18211	LM311 N(P)(8 PIN)	U4F	13-18000	74LS00 QUAD NAND 14P
U1F	13-90002	DG211 (Analog Switch)	U4G	15-18252	8031
U1G	13-90004	AM2502 SAR	U4G	22-10473	IC 40 PIN
U1H	13-60200	DAC0800	U5G	14-49195	Q2080 MAIN PCB
U1J	13-18003	7406 HEX BUFF INV 14P	U5G	22-10373	IC 24 Pin
U2A	13-18204	NE592 (Video Amp)	U5H	13-18044	74LS273 OCT D-FF 20P
U2C	13-18204	NE592 (Video Amp)	U5J	02-12302	14 Pin dip, 220/330
U2E	13-18205	8T20	U5J	22-10085	14 Pin I.C.
U2F	13-18009	74LS74A DUAL FF 14P	U6G	13-18016	74LS123 DUAL

DRIVE CONTROL PCB ASSEMBLY

Ref.	Part Number	Description	Ref.	Part Number	Description
INTEGRATED CIRCUITS (con't)					
U2G	13-02540	74 504	U6H	13-18009	ONE-SHOT 16P 74LS74A DUAL FF 14P
U2HA	13-30100	LF353 or TL072 (DUAL) OP AMP	U6J	13-18007	7438 QUAD NAND BUFF 14P
U2HB	13-18211	LM311 N(P)(8 PIN)	U7D	13-90002	DG211 (Analog Switch)
U2J	13-18207	75107	U7G	13-18041	74LS377 OCT D-FF 20 P
U3A	13-18008	7445 BCD-DEC DECODER 16P	U7H	13-18001	74LS02 QUAD NOR 14 P
U3E	13-18011	74LS86 QUAD XOR 14P	U7J	13-18007	7438 QUAD NAND BUFF 14 P
U3F	13-18006	7414 HEX INV SCHMITI 14 P	U8D	13-18233	LF 347 QUAD OP AMP 14 P
U3G	13-18040	74LS373 (octal latch)	U8F	13-18208	MC 1408L8 DAC 16P
U3H	13-18009	74LS74A DUAL FF 14P	U8G	13-18043	74LS221
U3J	13-18206	74110A DUAL LINE DUR 14P	U8H	13-18211	LM311 N(P)(8PIN)
U4B	13-18004	7407 HEX BUFF 14P	U9D	13-18243	LM324
U4C	13-18009	74LS74A DUAL FF 14P			
MISCELLANEOUS					
RPI	02-12303	Res.Pk, 10 pin dip, 22K	VR2	16-18216	Reg, I.C. Volt., -5V 79MO5C
Y1	11-10458	Crystal, 12MHz	VR1,2	54-10111	Screw, Ph.Pan.Hd., 4-40 x .25
VR1	16-18217	Reg., IC.. Volt., ± 12V 78M 12C	VR1,2	56-10322	Nut, Kept 4-40
J1 Pin	22-10411	Pin, Test Point	DS1, -15V 22-10036		Plug, Shorting
50			TP1-7, 9-13,16,		
J3	22-10034	Conn, Dual 22, 125 ctrs., Bottom Mount	18-21, GND (S), DS1-4 (2 ea),		
J4	22-10033	Hdr., Rt. Angle, 3 pos.	4(2), A(2), C(2),		
J	22-10032	Conn., PCB Mt., 6 Pos. Bottom Mount	D(2), H(2), M3(2), -15-5(3), 8031(2),		
J6	22-10459	Conn., PCB Mt., 10 Pos. Rt. Angle	E1(2), E3(2)	22-10411	Pin, Test Pt.
J7	22-10460	Conn., PCB Mt., 3 Pos. Btm. Mt.			

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