PM-DLV11J

SERIAL LINE INTERFACE

MANUAL

Plessey
Peripheral
Systems

PM-DLV11J

SERIAL LINE INTERFACE

MANUAL

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Section 1
General Information

1.1 INTRODUCTION

This manual provides the necessary information to install and operate the PM-DLV11J serial line interface manufactured by Plessey Peripheral Systems, Irvine, California 92714.

The material is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a breif general description of the PM-DLV11J and the specifications for the interface.

Section 2 - INSTALLATION AND OPERATION. This section explains the procedures for equipment installation.

Section 3 - FUNCTIONAL DESCRIPTION. This section contains a detailed functional description of the PM-DLV11J including address selection, register data bit functions, baud rate selection and interfacing information.

Section 4 - THEORY OF OPERATION. This section contains a circuit logic description of the PM-DLV11J.

MAINTENANCE DRAWING PACKAGE. The maintenance drawing package MD 703330 contains the parts list, logic diagrams, and assembly drawing required for this unit.

1.2 GENERAL DESCRIPTION

The PM-DLV11J is a 4 channel asynchronous serial line interface between the LSI-11 bus and a standard I/O device. The device receives parallel data from the LSI-11 bus, converts it to a serial word and transmits it to the peripheral device. The PM-DLV11J also receives a serial data word and converts it to parallel data to be output to the LSI-11 bus.

There are two contorl status registers per channel: a receiver CSR (RSCR) and a transmitter CSR (XCSR). The CSRs maintain information on the status of the operation and contain bits which control the mode of operation. There are two data buffer registers per channel: a receiver (RBUF) and a transmitter (XBUF). The buffer registers hold the data receivered from or transmitted to an external device.

*DEC, LSI-11, Unibus and Q-bus are registered trademarks of Digital Equipment Corporation.

The module has the ability to act as a polled or interrupting peripheral dictated by processor (software) commands. Channel 4 can be configured as a dedicated console device interface.

The PM-DLV11J can respond to any address in the upper 4K peripheral page (160000_8 to 177776_8). It operates in sixteen contiguous registers unless Channel 4 is configured as the console device. In that case, twelve contiguous addresses are required, and Channel 4 operates at 177560_8 thru 177566_8.

All standard baud rates are supported. Each channel has independent baud rate jumper selects.

The serial line can be jumper selected for compatibility with EIA RS232, RS422 or RS423.

The PM-DLV11J is hardware and software equivalent to four PM-DLV11s. It can be used to replace the DEC DLV11J. If not otherwise specified, the PM-DLV11J will shipped in the configuration shown in Table 1-1.

Channel	ADDRESS	REGISTER	VECTOR
1	176500	RCSR1	300
	176502	RBUF1	
	176504	XCSR1	304
	176506	XBUF1	
2	176510	RCSR2	310
	176512	RBUF2	
	176514	XCSR2	314
	176516	XBUF2	
3	176520	RCSR3	320
	176522	RBUF3	
	176524	XCSR3	324
	176526	XBUF3	
4*	177560	RCSR4	60
	177562	RBUF4	
	177564	XCSR4	64
	177566	XBUF4	
Baud Rate:	Channel 1 through 3		9600
	Channel 4		300
Break Response:	Halt		
UART Operation:	8 Data bits; no parity; one stop bit		
Serial Interface:	EIA RS232C		
*Channel 4 used as console device interface.			

TABLE 1-1: FACTORY CONFIGURATION

1.3 SPECIFICATIONS

1.3.1 Physical Specifications

The PM-DLV11J is contained on a single dual-wide printed circuit board.

- Width 5.2 inches (13.2 cm)
- Height 8.9 inches (22.8 cm)

The circuit board is a multi-layer etch board with internal power and ground planes, and logic traces on component and solder sides.

1.3.2 Power Requirement

+5VDC	1.55A
+12VDC	0.20A

1.3.3 Environmental Specifications

- Temperature — Operating 0°C to 50°C
Nonoperating -40°C to 85°C
- Relative Humidity — 10% to 90% without condensation

Section 2

Installation and Operation

2.1 UNPACKING AND INSPECTION

The PM-DLV11J is shipped in a special packing carton designed to keep the board from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

To unpack the PM-DLV11J remove any packing materials and visually inspect for physical damage.

2.2 INSTALLATION

Refer to Figure 2-1 for switch and jumper locations.

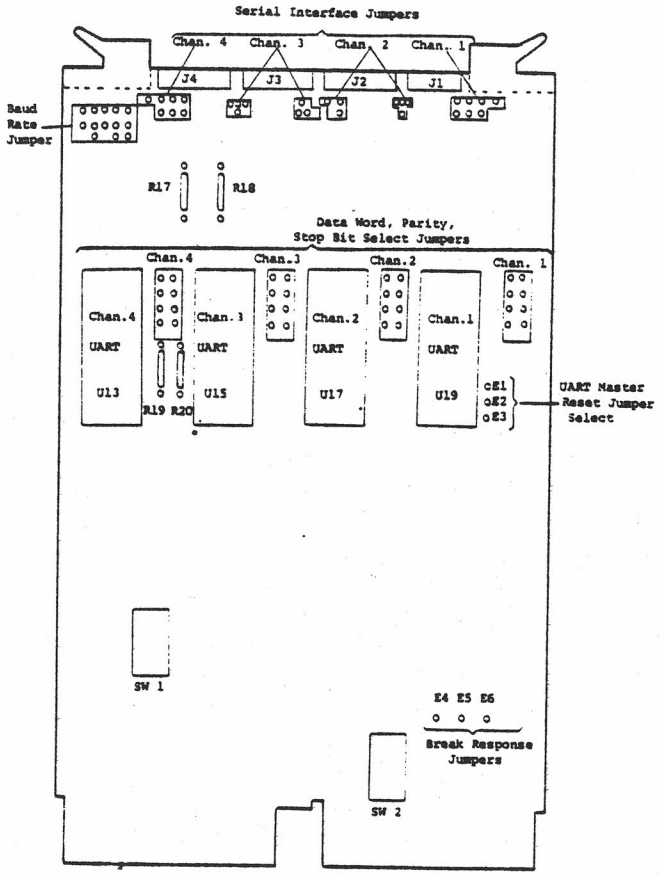
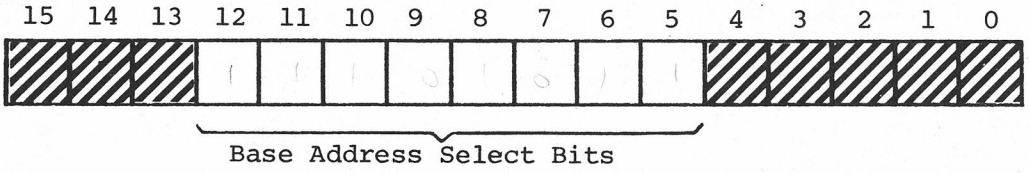


FIGURE 2-1: SWITCH AND JUMPER LOCATIONS

2.2.1 Address Select Switches

The base interrupt vector for the PM-DLV11J is selected through switch S2. Refer to Table 2-1.



ADDRESS BIT	SWITCH
5	S2-1
6	S2-2
7	S2-3
8	S2-4
9	S2-5
10	S2-6
11	S2-7
12	S2-8

TABLE 2-1: ADDRESS SELECT BIT SWITCHES

A switch set to the ON position corresponds to an inactive signal on the bus. For example, the switch settings for base address 176500 thru 176536 (factory configuration) are shown in Table 2-2.

S2-	SETTING	ADDRESS BIT
1	ON	5
2	OFF	6
3	ON	7
4	OFF	8
5	ON	9
6	OFF	10
7	OFF	11
8	OFF	12

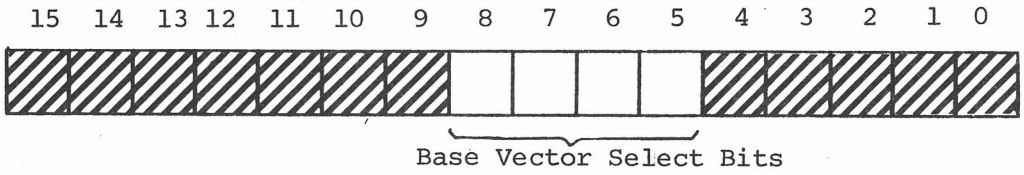
* S2-10 is unused.
If channel 4 is used as the console device, S2-9 and S1-4 should be ON.

TABLE 2-2: SWITCH SETTING FOR BASE ADDRESS 176500 THRU 176536

For more detailed information, refer to Section 3.1.

2.2.2 Vector Select Switches

The base interrupt vector for the PM-DLV11J is selected through switch S1 . Refer to Table 2-3.



ADDRESS BIT	SWITCH
5	S1-8
6	S1-7
7	S1-6
8	S1-5

TABLE 2-3: VECTOR SELECT BIT SWITCH

A switch set to ON corresponds to an INACTIVE signal on the bus. For example, the switch settings for base vector 300 thru 334 (factory configuration) are shown in Table 2-4.

S1-	SETTING	VECTOR ADDRESS BIT
5	ON	8
6	OFF	7
7	OFF	6
8	ON	5
S1-1 and S1-2 are unused.		

TABLE 2-4: SWITCH SETTING FOR BASE VECTOR 300

NOTE

If channel 4 is used as the console device, S1-3 should be ON.

For more detailed vector information see Section 3.2.

2.2.3 Use of Channel 4 as Console Device Interface

If Channel 4 is used as a dedicated console device interface, the following switches must be set correctly.

- S2-9 ON
- S1-4 ON

} Enable Selection of Addresses 17560-17566

- S1-3 ON — Enables Selection of Vector 60 and 64

When the BREAK key on the console is pressed, the UART detects a framing error. The processor response to the error detection is jumper selectable as shown in Table 2-5. See Figure 2-1 for jumper locations.

BREAK RESPONSE	JUMPER
Halt	E5 to E4
Re-Boot	E5 to E6
No Response	No Jumper

TABLE 2-5: BREAK RESPONSE JUMPER

NOTE

If channel 4 is not used as the console device interface, remove the jumper, or a framing error on Channel 4 will cause the processor to halt or re-boot.

2.2.4 Baud Rate Selection

Baud rates for each of the four channels on the PM-DLV11J are set independently by jumper selection. The wire wrap pins labeled CLK 1 through CLK 4 control the baud rate for the corresponding channel. Refer to Table 2-6 and Figure 2-2 for the jumper information.

BAUD RATE	WIRE-WRAP PIN
150	B
300	G
600	C
1200	A
2400	D
4800	E
9600	F
19.2K	J
38.4K	H

TABLE 2-6: BAUD RATE JUMPER PINS

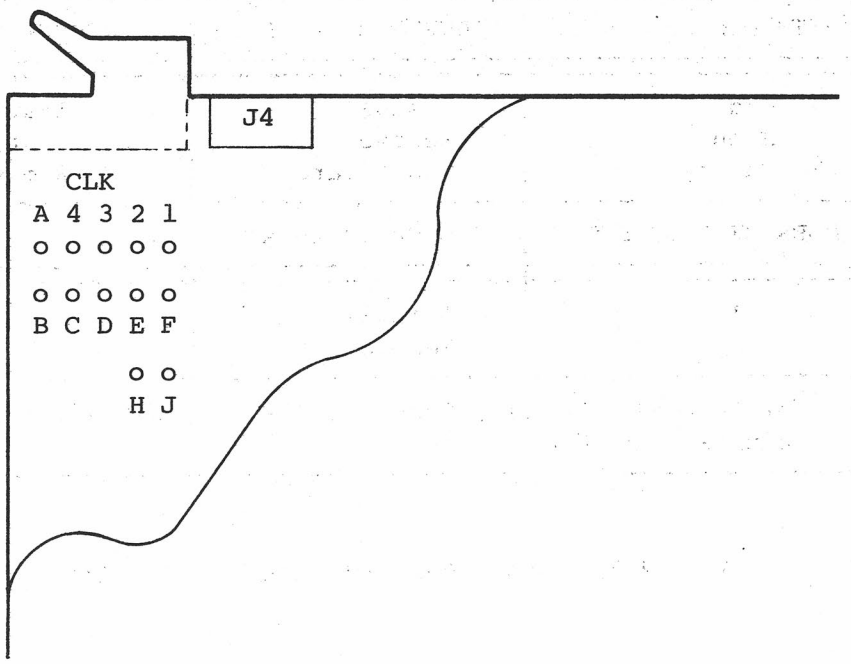


FIGURE 2-2: BAUD RATE JUMPER LOCATIONS

2.2.5 Data Word Format

The data word format for each of the channels on the PM-DLV11J is independently jumper selectable. The number of data bits, the number of stop bits, and the parity mode are determined as shown in Table 2-7.

UART*		
NUMBER OF DATA BITS	JUMPER B3 TO A3	JUMPER B2 to A2
5 6 7 8	Install Install Remove Remove	Install Remove Install Remove
PARITY MODE	JUMPER B1 to A1	JUMPER B5 to A5
Odd Even No Parity	Install Remove Don't Care	Install Install Remove
NUMBER OF STOP BITS	JUMPER B4 to A4	
1 2	Install Remove	

* UART for Channel 1 is U19; Channel 2 is U17; Channel 3 is U15; Channel 4 is U13.

TABLE 2-7: DATA, STOP BIT, AND PARITY SELECT

2.2.6 Serial Interface Selection

The PM-DLV11J can interface with standard EIA-232C, RS-423 and RS-422 devices. The serial interface for each channel is independently jumper selectable as shown in Table 2-8.

	RS-232C or RS 432		RS-422		SIGNAL
	FROM	TO	FROM	TO	
Channel 1	1E 1D	1F 1B	1G 1C	1F 1B	XMT DATA 1+ XMT DATA 1-
Channel 2	2E 2D	2F 2B	2G 2C	2F 2B	XMT DATA 2+ XMT DATA 2-
Channel 3	3E 3D	3F 3B	3G 3C	3F 3B	XMT DATA 3+ XMT DATA 3-
Channel 4	4E 4D	4F 4B	4G 4C	4F 4B	XMT DATA 4+ XMT DATA 4-

TABLE 2-8: SERIAL INTERFACE JUMPERS

NOTE

When a channel is configured for EIA-RS-422, the following resistor should be replaced by 100 ohm resistor.

Channel 1 R20
Channel 2 R19
Channel 3 R18
Channel 4 R17

The serial interface connector (J1, J2, J3, or J4) is shown in Figure 2-3. The respective interface connection pin designations are defined in Table 2-9.

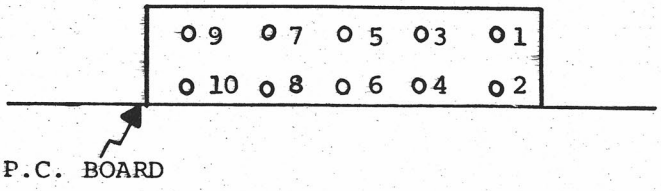


FIGURE 2-3: I/O CONNECTOR

I/O CONNECTOR PIN NUMBER	SIGNAL
1	CLK
2	GND
3	XMT DATA+
4	XMT DATA-
5	GND
6	
7	RCV DATA-
8	RCV DATA+
9	GND
10	+12VDC

TABLE 2-9: I/O PIN DESIGNATIONS

2.2.7 Interrupt Priorities

Interrupt priorities within the PM-DLV11J module are structured as shown in Table 2-10.

PRIORITY	REGISTER
7 (high)	CH4 RBUF
6	CH3 RBUF
5	CH2 RBUF
4	CH1 RBUF
3	CH4 XBUF
2	CH3 XBUF
1	CH2 XBUF
0 (low)	CH1 XBUF

TABLE 2-10: INTERRUPT PRIORITIES

2.2.8 Master Reset of the UART

The UARTs can be jumper selected to do a Master Reset on DCOKL or INITH. See Table 2-11.

MASTER RESET SIGNAL	JUMPER	
	FROM	TO
DCOKL	E1	E2
INITH	E3	E2

TABLE 2-11: MASTER RESET OF THE UART

2.2.9 Backplane

After switch positions, jumper selects, and channel priorities have been determined, plug the PM-DLV11J into the appropriate backplane slot. The PM-DLV11J can be mounted in the following backplanes:

- PM-F11/LS4 — Plessey 4 slot backplane
- PM-F11/LS9 — Plessey 9 slot backplane
- PM-F11/QU — Plessey 9 slot backplane
- PM-DDV11/B — Plessey 9 slot expanded backplane
- H9270 — DEC 4 slot backplane
- DDV11-B — DEC 9 slot backplane

Bus signals and their pin assignments are shown in Table 2-12.

CONNECTOR A		CONNECTOR B	
PIN	SIGNAL NAME	PIN	SIGNAL NAME
AA1	Not Used	BA1	BDCOK H
AB1	Not Used	BB1	Not Used
AC1	Not Used	BC1	Not Used
AD1	Not Used	BD1	Not Used
AE1	Not Used	BE1	Not Used
AF1	Not Used	BF1	Not Used
AH1	Not Used	BH1	Not Used
AJ1	GND	BJ1	GND
AK1	Not Used	BK1	Not Used
AL1	Not Used	BL1	Not Used
AM1	GND	BM1	GND
AN1	Not Used	BN1	Not Used
AP1	BHALH	BP1	Not Used
AR1	Not Used	BR1	Not Used
AS1	Not Used	BS1	Not Used
AT1	GND	BT1	GND
AU1	Not Used	BU1	Not Used
AV1	Not Used	BV1	+5VDC
AA2	+5VDC	BA2	+5VDC
AB2	Not Used	BB2	Not Used
AC2	GND	BC2	GND
AD2	+12VDC	BD2	Not Used
AE2	BDOUT L	BE2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	Not Used	BK2	BDAL6 L
AL2	BIRQL	BL2	BDAL7 L
AM2	BIAKI L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDALO L	BU2	BDAL14 L
AV2	BDALI L	BV2	BDAL15 L

TABLE 2-12: BUS SIGNLAS AND PINS ASSIGNMENTS

Section 3
Functional Description

3.1 ADDRESS SELECTION

The PM-DLV11J can respond to any address in the upper 4K peripheral page. It is limited to blocks of 16 addresses which start at addresses whose last two digits are either 00 or 40. If channel 4 is used as the console device, 12 slot memory blocks started at XXXX00 or XXXX40 can be used. Each channel has four device registers which can be individually addressed by the program. The device registers are as follows:

Receiver Control/Status Register (RCSR)
Receiver Buffer (RBUF)
Transmitter Control/Status Register (XCSR)
Transmitter Buffer (XBUF)

If channel 4 is configured as a dedicated console interface, its device register addresses will be 177560-177566.

The device address format is shown in Figure 3-1.

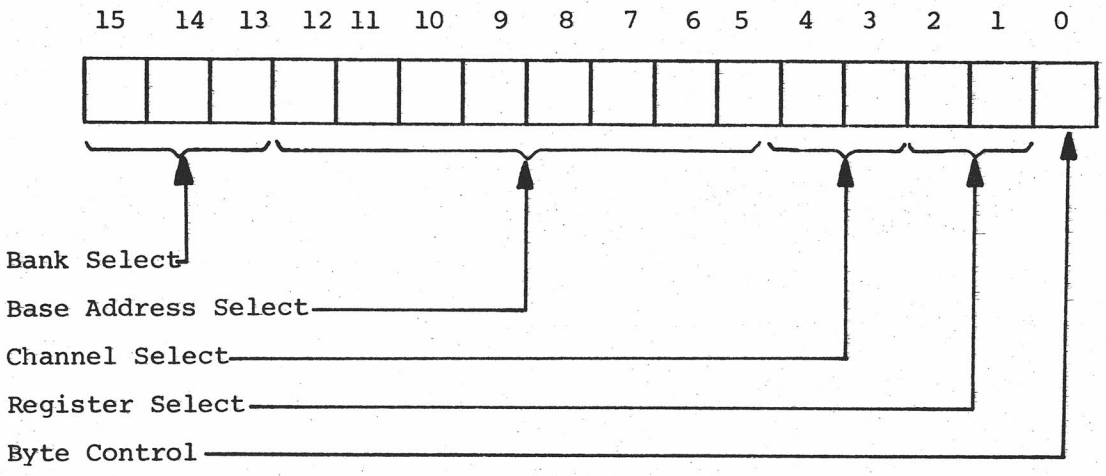


FIGURE 3-1: DEVICE ADDRESS FORMAT

The base address is selected by switch S2. See Table 2-1, and refer to Paragraph 2.2.1 for a switch setting example.

Channel and register select bits are set as shown in Table 3-1. These bits are not switch selectable, but are decoded automatically by the PM-DLV11J logic.

CHANNEL SELECT			REGISTER SELECT		
Channel	Bit 4	Bit 3	Register	Bit 2	Bit 1
1	0	0	RCSR	0	0
2	0	1	RBUF	0	1
3	1	0	XCSR	1	0
4	1	1	XBUF	1	1

TABLE 3-1: CHANNEL AND REGISTER SELECTION

3.2 VECTOR FORMAT

Eight interrupt vectors are switch and PROM selected on PM-DLV11J. Each channel is capable of generating two interrupts, one from the receiver buffer, and one from the transmitter buffer. Vector address range from 000 to 776. The console device interrupt vectors are 60 and 64. If an interrupt acknowledge is granted, the vector address is placed on the data/address bus lines. The format for the vector address is shown in Figure 3-2.

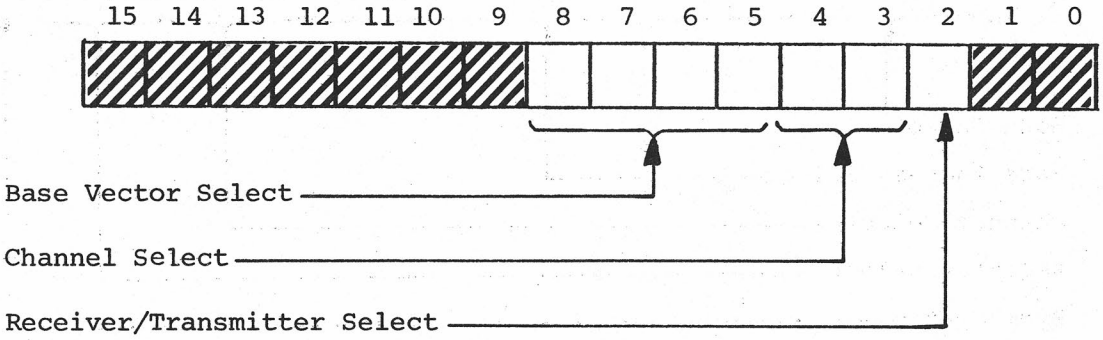


FIGURE 3-2: VECTOR ADDRESS FORMAT

The base vector is selected by switch S1. See Table 3-2, and refer to Section 2.2.2. for a switch setting example.

VECTOR ADDRESS BIT	SWITCH
8	S1-5
7	S1-6
6	S1-7
5	S1-8

TABLE 3-2: VECTOR ADDRESS BIT SWITCHES

NOTE

If channel 4 is used as the console device interface, S1-3 should be ON.

The channel select bits are PROM, not switch selected. They are decoded as shown in Table 3-3.

CHANNEL	BIT 4	BIT 3
1	0	0
2	0	1
3	1	0
4	1	1

TABLE 3-3: VECTOR CHANNEL SELECT

The receiver/transmitter select bit is decoded as:

0 = Receiver
1 = Transmitter

This bit is not switch selectable, but is set automatically by the PM-DLV11J.

Although the PM-DLV11J has eight separate interrupting registers, it is capable of handling only one interrupt at a time. Therefore, the interrupts are prioritized on the board as shown in Table 2-10.

3.3 REGISTER WORD FORMATS

The PM-DLV11J has four word formats associated with it, one for each of the four registers associated with each channel.

3.3.1 Receiver Control/Status Register (RCSR)

Refer to Figure 3-3.

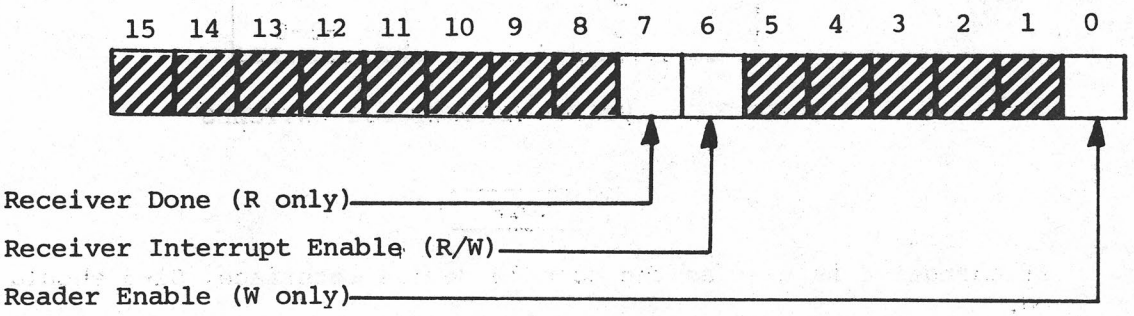


FIGURE 3-3: RECEIVER CONTROL/STATUS REGISTER

Bit 15-8 Not used, will be read as zeros.

7 Receiver Done: Read only. Set when an entire word has been received, and is ready for transmission to the processor. If Receiver Interrupt Enable (bit 6) is set, setting Receiver Done will start an interrupt sequence.

6 Receiver Interrupt Enable: Read/Write. Set under program control, enables receiver done (bit 7) to initiate an interrupt sequence. Cleared by INIT or program control.

1-5 Not used. Read as zeros.

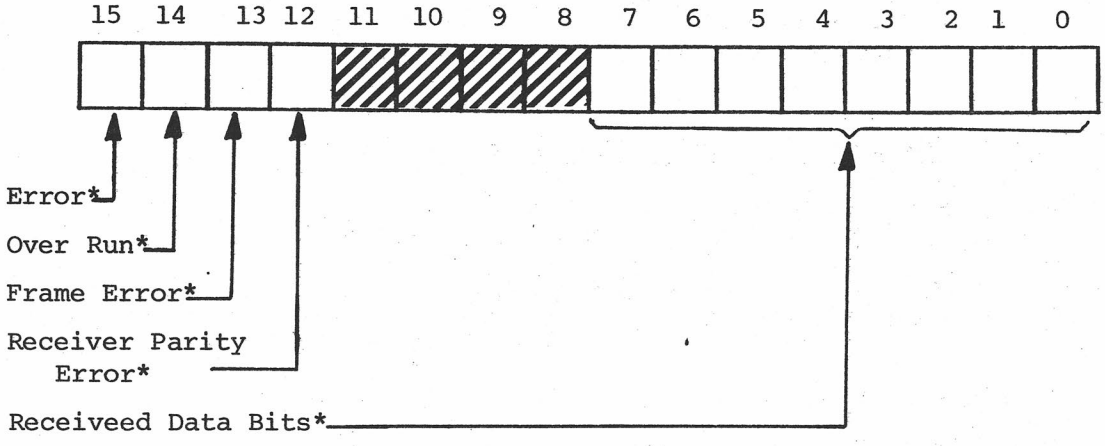
0 Reader Enable: Write only. Setting bit 0 advances the paper tape reader on an LT-33 terminal one character. Setting this bit also clears Receiver Done (bit 7). Read as zero.

NOTE

Current loop option is necessary for the operation of this bit.

3.3.2 Receiver Buffer Register (RBUF)

Refer to Figure 3-4.



* All Bits READ only.

FIGURE 3-4: RECEIVER BUFFER REGISTER

Bit 15 Error: Read only. Set whenever bit 14, 13, or 12 set.

14 Over Run: Read only. Set when previous character was not completely read (RCSR bit 7 not cleared) prior to receiving a new character. Cleared by INIT.

NOTE

One full character time is allowed between Receiver Done (CSR bit 7) being set and the setting of the Over Run bit when back-to-back characters are being received.

13 Frame Error: Read only. Set when no valid STOP bit present for the character being received. Cleared by INIT.

12 Receiver Parity Error: Read only. Set when the received parity does not agree with the expected parity. Always zero if the device is configured for NO PARITY.

NOTE

All Error bits remain valid until the next character is received.

8-11 Not used. Read as zeros.

0 -7 Received Data Bits: Read only. Contains five to eight data bits in a right-justified format. Upper bits read zero when not enabled.

3.3.3 Transmitter Control/Status Register (XCSR)

Refer to Figure 3-5.

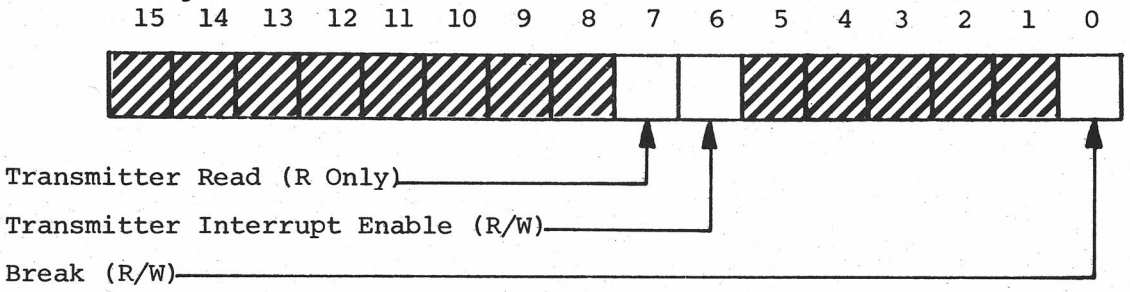


FIGURE 3-5: TRANSMITTER CONTROL/STATUS REGISTER

Bit

8-15 Not used. Read as zeros.

7 Transmitter Ready: Read only. Set when XBUF is ready to receive another character from the processor. Transmitter Ready will start an interrupt sequence if bit 6 (Transmitter

6 Interrupt Enable) is set.

Transmitter Interrupt Enable: Read/Write. Set under program control if an interrupt sequence should be started when Transmitter Ready (bit 7) is set. Cleared by program control or INIT.

1-5 Not used. Read as zeros.

0 Break: Read/Write. Set or cleared under program control. When break is set, a continuous space level is transmitted. Transmitter Ready (bit 7) and Transmitter Interrupt Enable (bit 6) are still operable, allowing software timing of Break. When Break is not set, character transmission can proceed in a normal fashion. Cleared by INIT.

3.3.4 Transmitter Buffer (XBUF)

Refer to Figure 3-6.

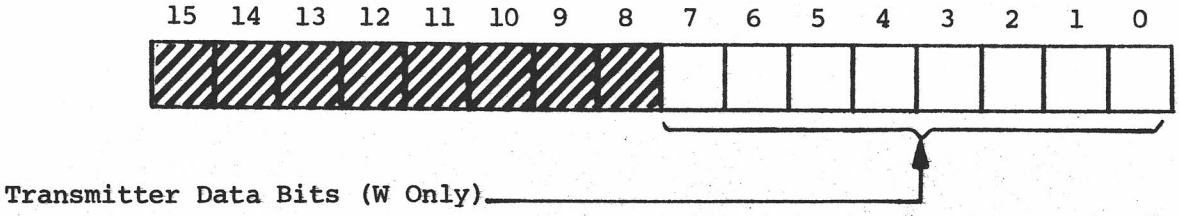


FIGURE 3-6: TRANSMITTER BUFFER

Bit	
8-15	Not used. Read as zeros.
0- 7	Transmitter Data Bits: Write only. Contains five to eight right-justified data bits. loaded under software control for serial transmission.

3.4 ASYNCHRONOUS TRANSMISSION FORMAT

In asynchronous transmission, for proper data recovery by the receiver, data characters are transmitted in the format shown in Figure 3-7.

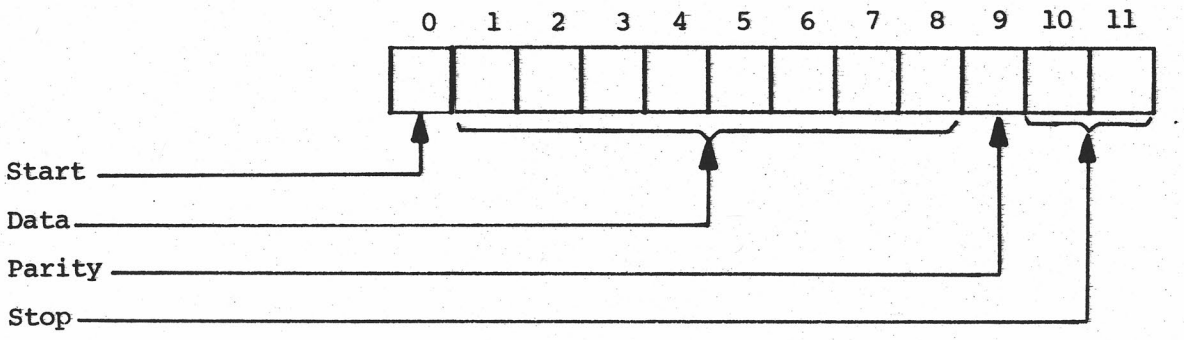


FIGURE 3-7: SERIAL DATA WORD FORMAT

The START bit is detected by the UART as a mark-to-space transition, causing it to begin loading the character into the storage register.

Data can be five to eight characters long. It is shifted by the UART so the least significant bit is in the lowest bit position in the register (right-justified).

The parity can be configured for odd, even, or no parity. If the device is configured for no parity, the STOP bits follow immediately after the Data bits.

The STOP bits can be configured for either one or two STOP bits. When the first STOP bit is received, the UART shifts the data in parallel from the receiver shift register to a parallel holding register. All START, STOP and PARITY bits are removed from the data. The receiver asserts Receiver Done (RSCR bit 7), and all data and error bits become valid.

Section 4

Theory of Operation

4.1 GENERAL INFORMATION

The PM-DLV11J is an asynchronous serial interface with four independent channels. It receives parallel data from the LSI-11 bus, converts it to serial data, and transmits it to an I/O device. It also receives serial data from the I/O device and converts it to parallel for use on the LSI-11 bus. This theory of operation will be divided into three main sections: address logic, interrupt logic, and data manipulation. Refer to schematic SD 703330. Refer to DEC Microcomputer Processors for bus timing information.

The block diagram for the DLV11J serial line interface is shown in Figure 4-1.

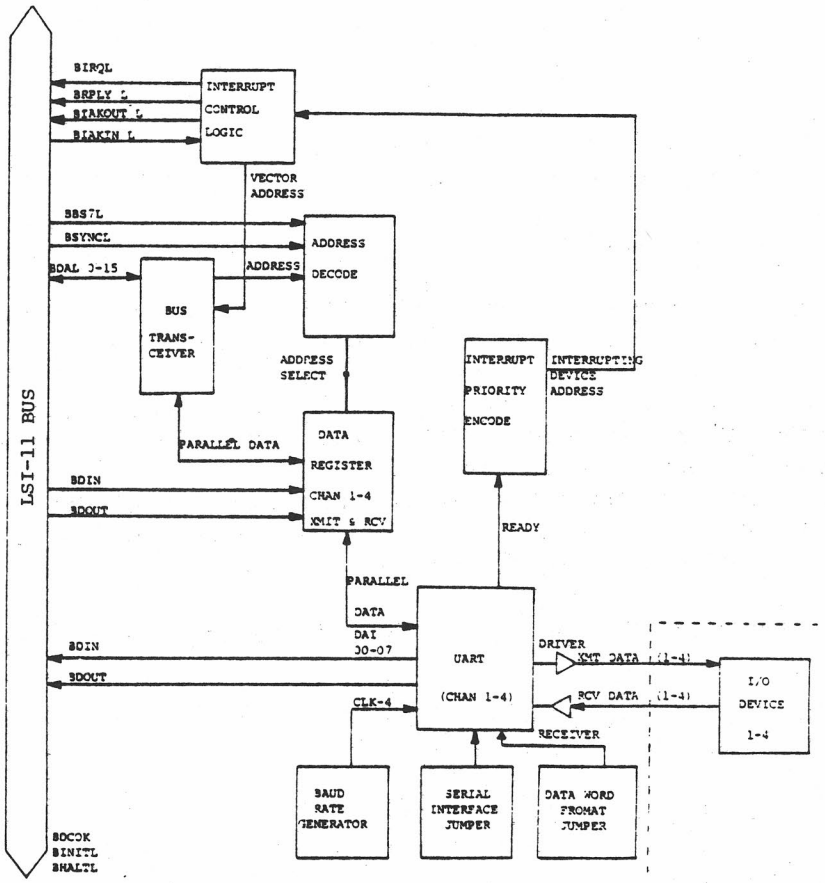
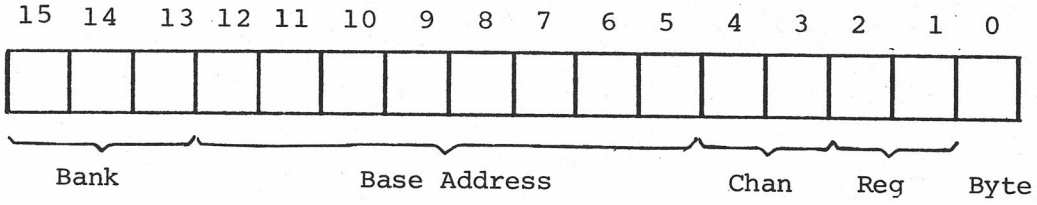


FIGURE 4-1: PM-DLV11J BLOCK DIAGRAM

4.2 ADDRESS LOGIC



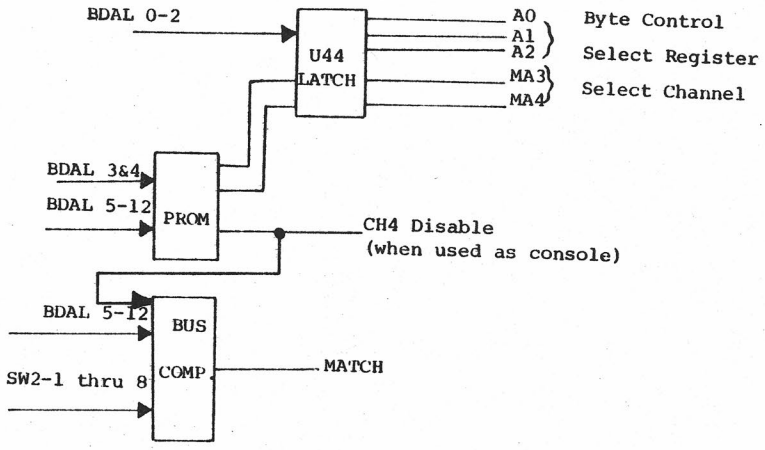


FIGURE 4-2: ADDRESS SELECT BLOCK DIAGRAM

BS7 and bits 5 through 12 are compared to the user selected switch settings (S2-1 through S2-8) by two 8136 bus comparators (U57 and U58). If the correct address is present, MATCH is asserted. MATCH enables the data registers, and causes BRPLYL to be asserted.

Bits 3 and 4 are used as channel select bits. They are used (along with bits 5-12) to address a PROM which outputs a two bit address for channel select. It is latched into U44 and output as MA3 and MA4. The PROM also puts out two control lines which disable the channel 4 address and enable the console device address (177560) when channel 4 is used as the console interface.

Bit 0, 1 and 2 are latched into U44 and used to select registers and bytes.

4.3 INTERRUPT LOGIC

The transmitter ready and receiver ready on each channel can cause interrupt if the interrupt enable bit is set.

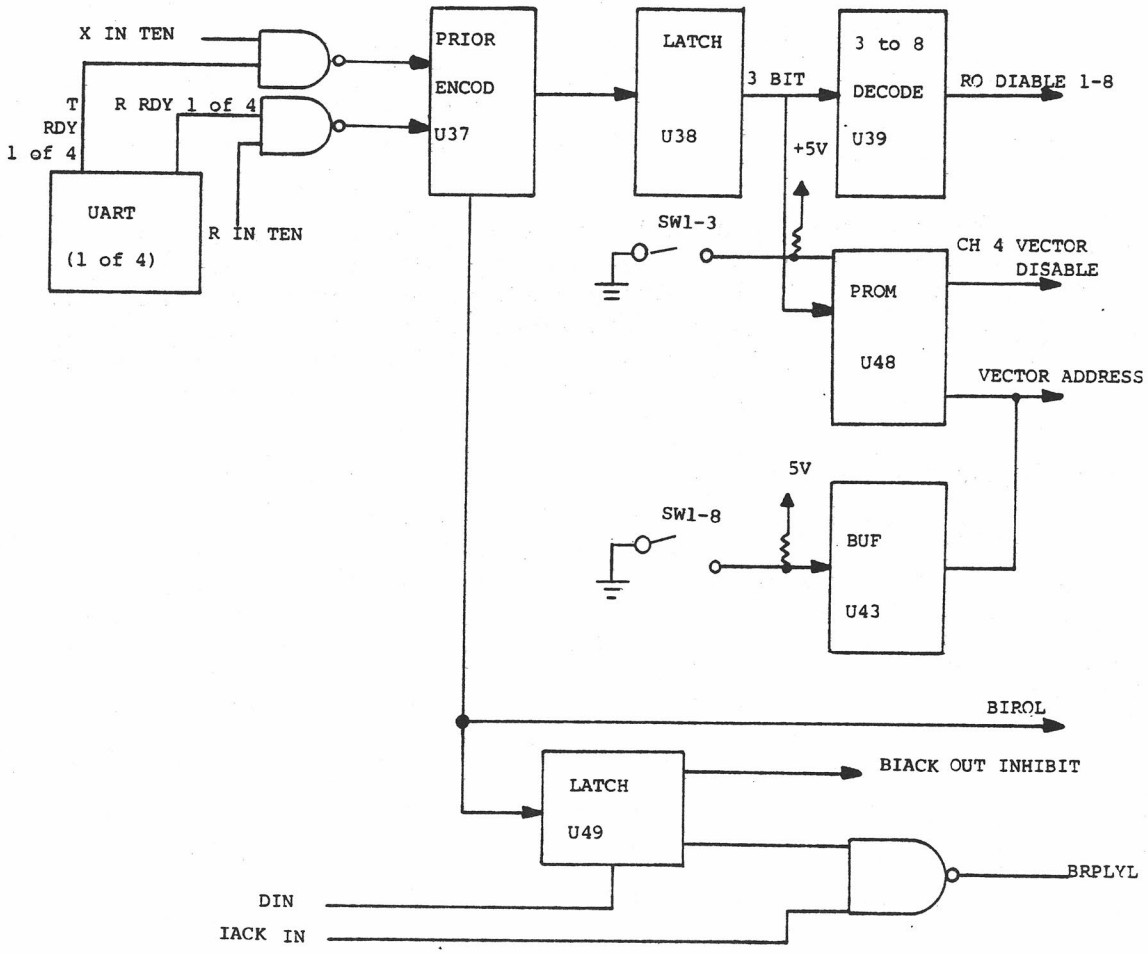


FIGURE 4-3: INTERRUPT SEQUENCE BLOCK DIAGRAM

The UART for the appropriate channel asserts T RDY or R RDY. If the interrupt enable bit was set for that channel and register, a request line (RQ) is asserted. RQ1-8 are prioritized and encoded by an 8 to 3 encoder (U37). The 3-bit address is latched into a storage register by the interrupt acknowledge signal from the processor (IACKIN). The 3-bit address is converted back to eight lines and used to disable the interrupt request when IACKIN is received. The 3-bit address is used to address a PROM which asserts the base vector address. The PROM also is used with switch S1-3 to enable vectors 60 and 64 when channel 4 is used as the console device.

BIROL, the bus request signal, is asserted whenever a RQ line is detected by the 74148 priority encoder. DINH latches the request information into U49, inhibiting BIAKOUTL and asserting BRPLYL when IACKIN is received. At the same time, the vector address is placed on the bus data/address lines. The assertion of IACKIN by the processor clears the RQ line.

4.4 DATA MANIPULATION

Incoming data from the processor is routed through a bus transceiver (U52 through U55) then latched into the UART by XBUF. The UART converts it to serial data which is output on the SERIAL OUT line, through a line driver (U2, U3, U10 or U11) and out to the I/O device.

Serial data coming in is received by a line receiver (U4 or U5), goes into the UART on its SERIAL IN line, and is translated into parallel data. The received data is routed through a buffer (74LS244) to the bus transceivers and onto the LSI-11 buses.

The error bits are also routed through a buffer to the bus transceivers. The buffers are enabled by the RRBUF signals for each channel. See Figure 4-4.

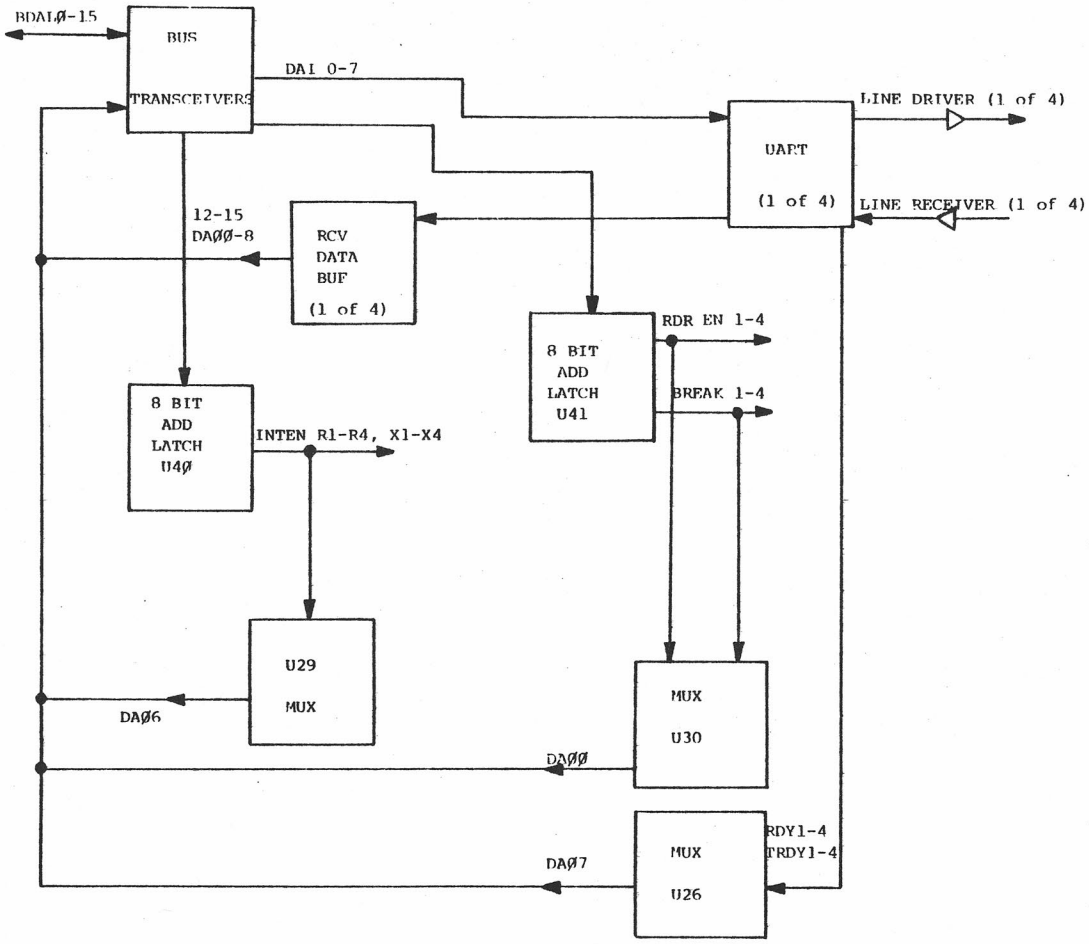


FIGURE 4-4: DATA FLOW BLOCK DIAGRAM

Only three bits are used in the CSRs. Bit 7 is transmitter or receiver ready (TRDY or RRDY). These signals come directly from the UARTs and are multiplexed before going to the bus transceiver. Bit 6 is the interrupt enable bit (INTEN) and is latched into U40. The output of U40 enables the RQ lines and is multiplexed for output to the bus transceiver. Bit 0 is reader enable (RDREN) in the XCSR and BREAK in the RCSR. It is used only with the current loop option in the XCSR. The BREAK bit is set or cleared under software control. When set, a continuous high level is output, disabling the SERIAL OUT line. RDR ENBL and BREAK information for all four channels is stored in an eight bit addressable latch (74LS259), U41.

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