

**TECHNICAL MANUAL**  
**Volume 2**

**PBC 1002 Revision 1**

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*WR-2A*

**pb Packard Bell Computer**

A SUBSIDIARY OF PACKARD BELL ELECTRONICS  
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## PREFACE

This manual is provided for the use of technical personnel engaged in PB250 Computer installation, operation, checkout, and maintenance. It is assumed that such technical personnel are familiar with basic computer technology.



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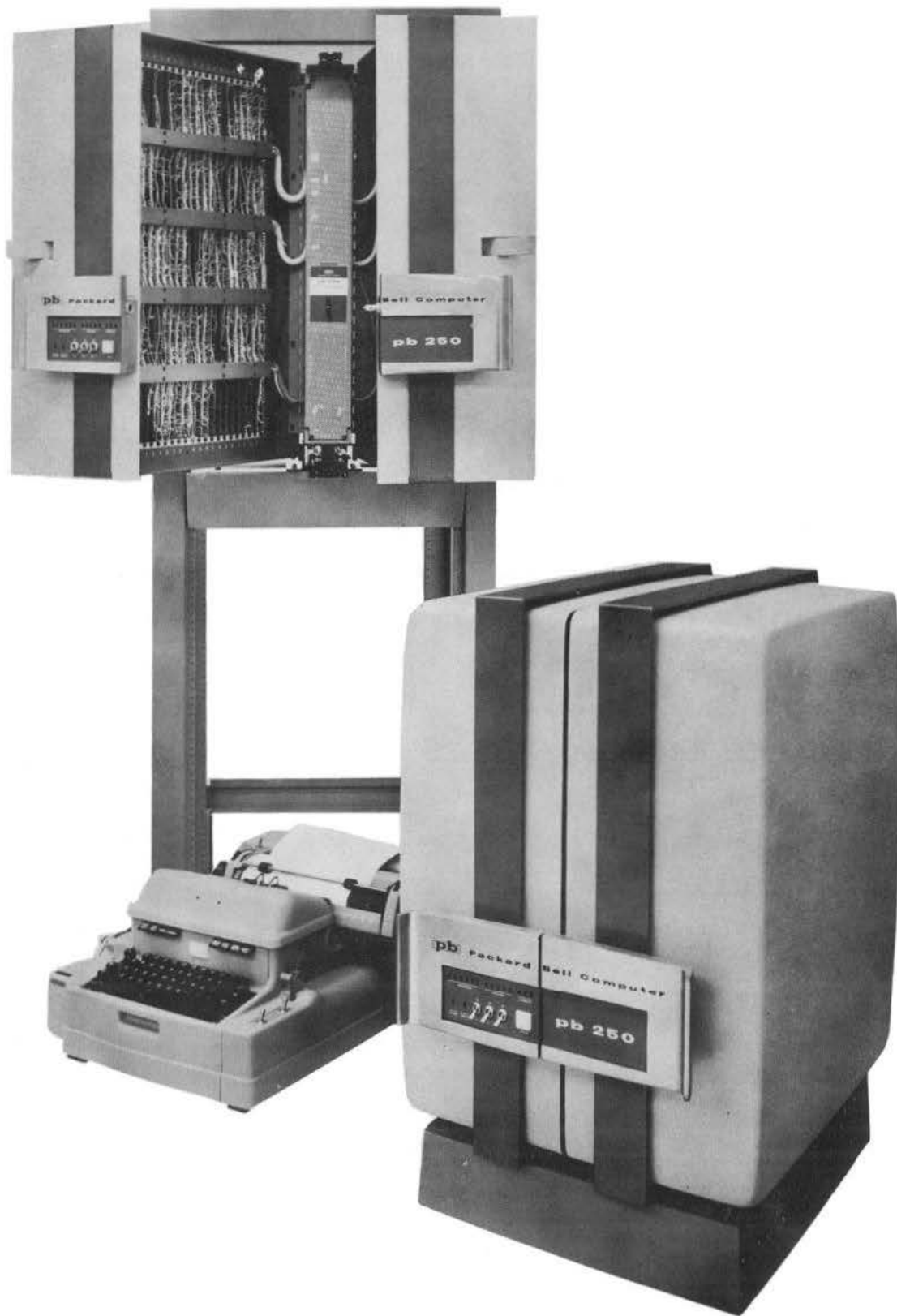


Figure 1-1. PB250 Computer Rack and Desk Mounted

## I. DESCRIPTION

### A. GENERAL (Figure 1-1)

This publication comprises operating and maintenance instructions for the PB250 Computer manufactured by Packard Bell Computer, Los Angeles, California.

Detailed description and applicable leading particulars are contained in Volume I of this manual.

### B. CONTROLS AND INDICATORS

The controls and indicators on the front panel of the PB250 are shown in Figure 1-2 and the applicable functions are described in Table 1-1. The controls and indicators on the front panel of the PS-7 Power Supply are shown in Figure 1-3 and the applicable functions are described in Table 1-2. The Flexowriter manual controls and indicators are shown in Figure 1-4 and the applicable functions are described in Table 1-3. For further information on the Flexowriter switches and keys refer to the vendor's manual, shipped with the Flexowriter.

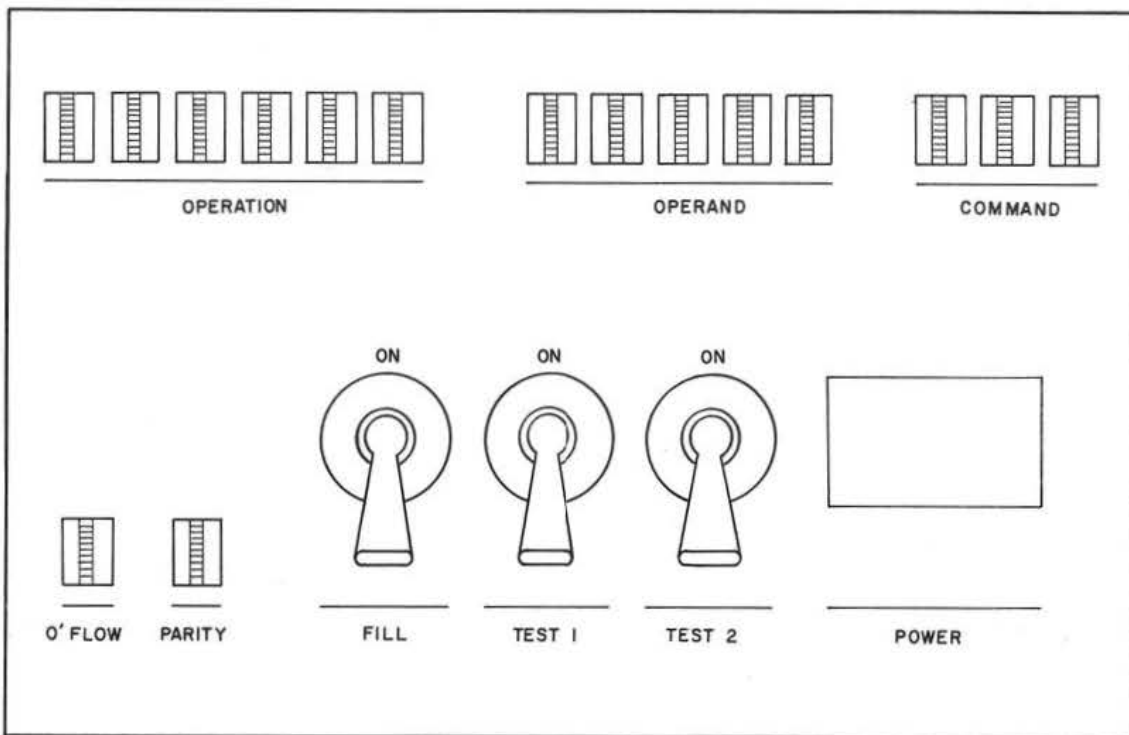


Figure 1-2. PB250 Control Panel

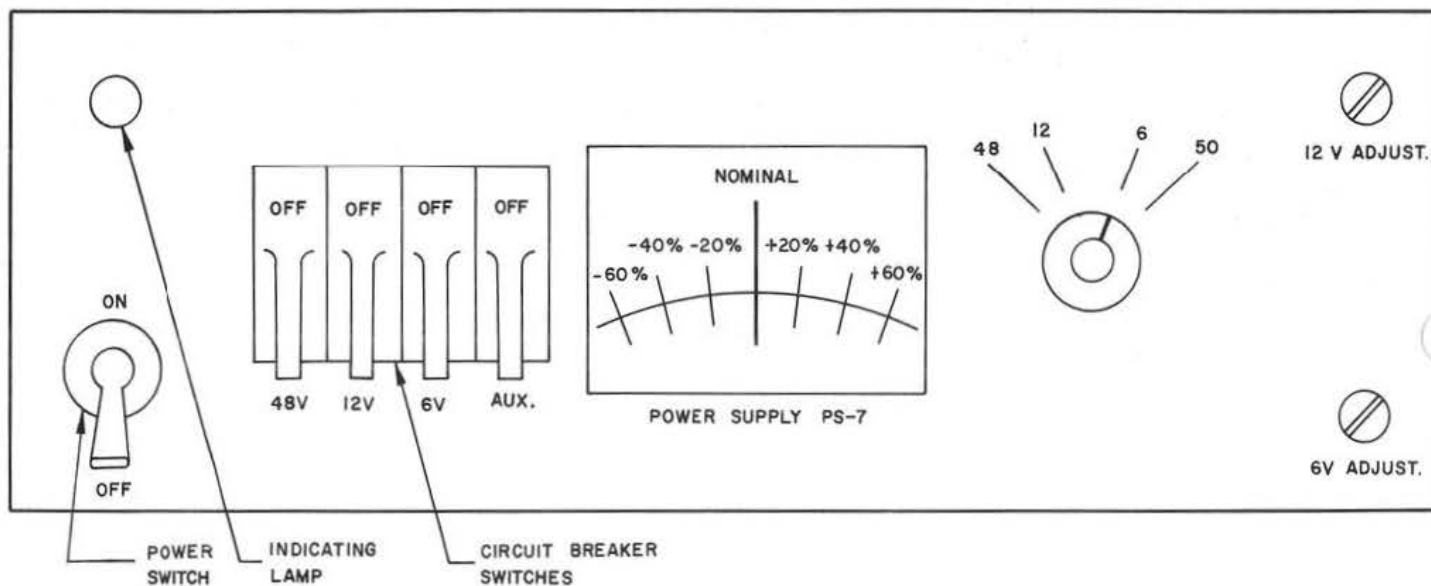


Figure 1-3. PB250 Power Supply Control Panel

Table 1-1. (Sheet 1 of 2)  
PB250 CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
OPERATION	Green	<p>Within certain limitations, these six indicators specify which op code has been executed, i. e. ADD (command 14 in octal), LOAD A (command 05 in octal) etc. Using a light on to indicate 1 and a light off to indicate 0, the pattern 001100 represents the command ADD in binary format.</p>
OPERAND	Green	<p>These five indicators specify the line number portion of the address.</p>
COMMAND	Green	<p>These three indicators specify from which command line the commands are being executed.</p>
O'FLOW	Green	<p>This indicator is on when an overflow has occurred.</p>
PARITY	Green	<p>This indicator is on when a parity check error is present, or a halt occurs.</p>

Table 1-1. (Sheet 2 of 2)  
PB250 CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
FILL		This switch is used to load the bootstrap routine. When this switch is in the ON position, it sets up certain conditions which command the computer to read and store the bootstrap information into memory line one.
TEST 1		This switch is used in marginal testing of the computer circuitry (see Section IV).
TEST 2		This switch is also used in marginal testing of the computer circuitry (see Section IV).
POWER	White	This backlighted indicator switch is used to apply power to the computer, and remains lit as long as power is applied to the computer.

Table 1-2. (Sheet 1 of 2)

PS-7 POWER SUPPLY CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
Power Switch		This toggle switch is used to apply ac power to the computer POWER switch.
Indicating Lamp	Amber	The indicating lamp is lit when the PS-7 power switch is in the ON position.
Circuit Breaker Switches		The four magnetic circuit breaker switches provide circuit protection against overload of voltage supplies within the PS-7.
Output Voltage Meter		This meter is used in conjunction with the Voltage Selection Switch to check indicated voltages. The meter also is used in calibration of the +6 and -12-volt dc output voltages. When these voltages have been correctly adjusted, the needle will be in NOMINAL position. Other indications are plus or minus percentages of the nominal output voltage.

Table 1-2. (Sheet 2 of 2)

PS-7 POWER SUPPLY CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
Voltage Selection Switch		This four-position rotary switch allows selection of a particular voltage as shown on the switch.
12 V ADJUST 6 V ADJUST		These potentiometers are used to adjust the +6 or -12-volt output voltages to the required reading on the Output Voltage Meter.*

\*For correct adjustment procedures, refer to Section II of PS-7G Power Supply Technical Manual PBC 3006.



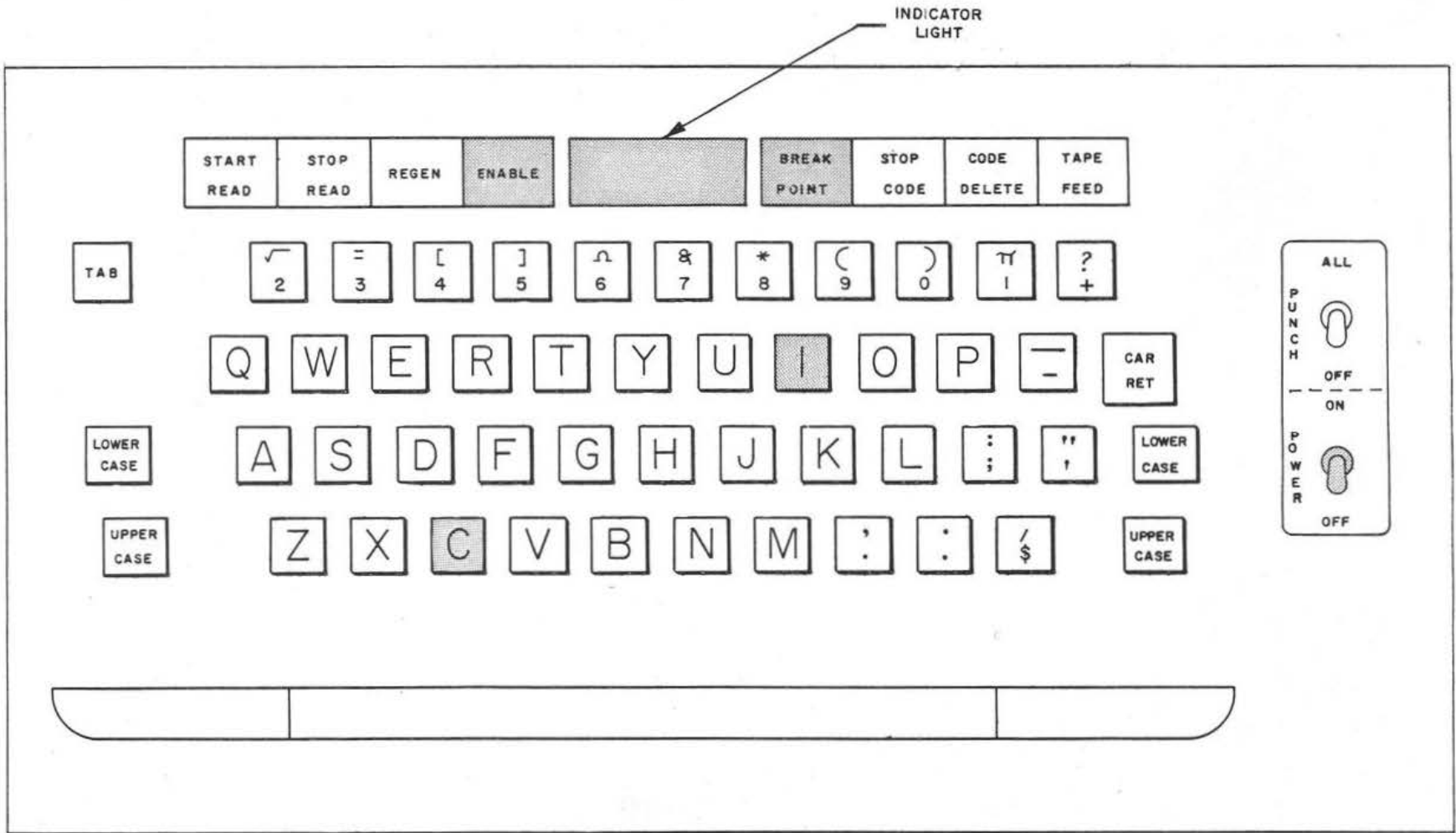


Figure 1-4. Flexowriter Keyboard

Table 1-3. (Sheet 1 of 2)

FLEXOWRITER CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
ENABLE Switch		This switch is used to interrupt the PB250 computation process, and condition for use switches and keys of the Flexowriter.
BREAKPOINT Switch		This switch causes signals to be sent to the PB250 which may be tested by TES (Transfer on External Signal) command, and together with the ENABLE switch in down position will clear the parity flip-flop (PARITY indicator light lit, see Figure 1-2).
"I" Key		When the "I" key is operated with the ENABLE switch in down position, the PB250 will be set to execute the command in memory location 00001.
"C" Key		When the "C" key is operated with the ENABLE switch in down position, the PB250 will read and execute the next desired command,

Table 1-3. (Sheet 2 of 2)

FLEXOWRITER CONTROLS AND INDICATORS

Control or Indicator	Color	
"C" Key (Continued)		and then halt. The "C" key is referred to as the "single-cycle key."
Indicating Light	White	When the indicating light is lit, it indicates that the PB250 is ready to receive information.

B-1. ELAPSED TIME INDICATOR

The five digit elapsed time indicator is mounted above the computer master circuit breaker on the spine inside the computer. The indicator employs a synchronous motor for 50-60 cycles per second operation, and accuracy of the unit is determined by the regulation of the line frequency. Power consumption of this unit is approximately 3 watts at 115-volts ac and it will operate reliably within a voltage variation of  $\pm 10\%$ . Temperature rise of the motor is less than  $45^{\circ}\text{C}$  at rated voltage and frequency; tolerance on the reading, at 50-60 cycles per second, is  $\pm 1$  digit.

B-2. MASTER CIRCUIT BREAKER

The computer master circuit breaker is mounted below the elapsed time indicator on the spine inside the computer. The single pole circuit breaker has an electrical rating of 125-volts ac, 60 cycles per second, 0.020 amp to 50 amps. Circuit interruption may occur at 1% but must occur at 25% over the rated load.

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## II. INSTALLATION

### A. GENERAL

This section of the manual covers the basic considerations pertinent to installation procedures for the PB250 Computer or computer system. The initial installation of the PB250 Computer is made by a customer service representative of Packard Bell Computer Corporation.

### B. INSTALLATION REQUIREMENTS

The following paragraphs discuss the preinstallation, installation, and preoperational requirements for the PB250 Computer.

#### B-1. SPACE

The PB250 Computer has been constructed to occupy a minimum space, whether table or rack mounted. Figure 2-1 shows the typical space requirements of the PB250R. Both equipments require identical extension areas, but differ in height requirements.

Prior to the installation of computer or computer system, consideration must be given to the space required for storage of tapes, spare parts, tools, test equipment, and other miscellaneous equipment.

#### B-2. PREINSTALLATION

Before a decision is made on the precise location of the PB250 in the selected area, the following points should be observed.

- a) Ensure that computer programmer will have unobstructed view of the PB250 Computer and Flexowriter, and other associated equipment, from a given position.
- b) Ensure the existence of ample good lighting in the data processing area.
- c) Ensure isolation of the PB250 Computer from noisy machinery of manufacturing areas. Noise may distract the computer programmer and lead to possible errors.
- d) Ensure that the data processing area is restricted to authorized, qualified personnel. Ideal facilities are such that the computer programmer may work while completely free of any interruption or diverting influence.

### B-3. TEST AND MAINTENANCE EQUIPMENT

In addition to the requirements contained in paragraph B-1, consideration must be given to the space required for test and maintenance equipment.

The following equipment is recommended for proper test and maintenance of the PB250 Computer.

- a) Oscilloscope. Tektronix Type 545A with 53C and CA Plug-In Units.
- b) Module Tester. Packard Bell, Type MT-I, for testing all modules and delay lines.
- c) Work Bench. To facilitate working on modules or units.
- d) Electrical Outlets. A sufficient number for connection of test equipment and soldering irons.



- e) Filing System. The initiation of a filing system will greatly assist the recording of modifications, changes or malfunctions of equipment. Reference to this record may help to establish a failure rate of the computer or computer system and provide data useful in troubleshooting.

Up-to-date schematics of the equipment should be readily available in the immediate vicinity of the computer. A system may be established in the field service group to cover modifications and changes which can be helpful to other field service engineers. A documentary paper detailing the latest changes should be published periodically and made available to all personnel concerned with the equipment.

#### B-4. ENVIRONMENT

For proper PB250 Computer operation, the ambient temperature in the data processing area must be between the limits 41<sup>o</sup>F and 113<sup>o</sup>F (5<sup>o</sup>C and 45<sup>o</sup>C). Most data processing areas are air-conditioned to maintain a stable temperature for the equipment.

#### B-5. POWER

Operating power for the PB250 Computer is a 115-volt, 60-cycle, single-phase input which should be free of transients and have reasonably good regulation. The computer operates satisfactorily between the parameters with line voltage variations between 100-volts ac and 125-volts ac (115-volts ac optimum) and under normal conditions, draws approximately 110 watts.

#### B-6. CABLING

Installation of the cables from the PB250 Computer and the Flexo-writer has been simplified by keying of the connectors. The cables consist of one input, one output, and two ac line cords. During installation of the



computer or computer system, it is preferable that interconnecting cables be run in channels beneath the floor level. This method ensures a neat system layout and eliminates possible hazards to personnel.

C. PRECAUTIONS

The following precautions must be observed when installing or operating the PB250 Computer.

- 1) If the unit is to be uncrated by other than a Packard Bell Computer representative, caution must be exercised when removing the base of the shipping crate. The large Phillips-head bolts must be removed one at a time and similarly replaced by the bolts supplied in the attached plastic bag. The one-by-one sequence is important because these bolts support the power supply.
- 2) Do not attempt to remove the balance weight from the base of the PB250R (rack-mounted) computer unless the computer has been securely bolted down.
- 3) Use caution in extending the PB250R Computer or Flexowriter from the rack frame.
- 4) Do not attempt to unlatch or open the sides of the computer until the unit has been fully extended.
- 5) Do not attempt to move the computer until the sides are closed and the front handles latched.

### III. OPERATION

#### A. GENERAL

The PB250 Computer is designed to function efficiently as a systems component to connect directly with various items of peripheral equipment. These devices are fully described in Packard Bell Computer Technical Manuals as listed below.

1)	MTU-1	Magnetic Tape Unit	PBC 1014
2)	MTC-1	Magnetic Tape Control Unit	PBC 1015
3)	HSB-N	High-Speed Buffer Register	PBC 1007
4)	HSR-1	High-Speed Reader	PBC 1010
5)	HSP-1	High-Speed Punch	PBC 1009
6)	MX-1	Memory Extension	PBC 1011
7)	PS-7G	Power Supply	PBC 3006
8)	PS-8	Power Supply	PBC 1013
9)		Flexowriter	PBC 1016
10)		Interface	PBC 1005

#### B. OPERATING PROCEDURE

The sequential operating procedure for the PB250 Computer is as follows:

- 1) Preoperational Setup
- 2) Operational Procedures

## B-1. PREOPERATIONAL SETUP

The following procedures are to be followed for preoperational setup:

- 1) Make certain that cabling between computer and Flexowriter are properly secured.
- 2) Check that all switches on computer and Flexowriter are off or in normal position.
- 3) Check that ac cables from computer and Flexowriter are connected to proper external source of 115-volt ac power.
- 4) Open computer and set circuit breaker switch to ON position. (Breaker switch is located on spine of computer.)
- 5) On front panel of power supply set all breaker switches to ON.
- 6) On front panel of power supply turn power switch to ON.
- 7) On computer front panel press POWER switch to ON. After pushbutton release make certain that switch remains back-lighted.
- 8) On Flexowriter set POWER switch to ON.

## B-2. OPERATIONAL PROCEDURES

The following step-by-step procedures are followed, a) check the Flexowriter, and b) load the computer, and c) check computer operation.

- 1) On Flexowriter insert bootstrap tape into reader mechanism.
- 2) On front panel of computer set FILL switch to ON.
- 3) On Flexowriter press ENABLE switch, then press and release BREAKPOINT switch. (BREAKPOINT switch will reset parity flip-flop.) The computer begins to read tape. The computer will stop after the first stop code has been read.

- 4) When tape stops turn FILL switch to OFF.
- 5) To start computer operation under computer control, press ENABLE switch on Flexowriter to down position.
- 6) On Flexowriter strike "I" key.
- 7) On Flexowriter press BREAKPOINT switch to down position.
- 8) On Flexowriter release BREAKPOINT switch.
- 9) On Flexowriter release ENABLE switch. Computer operation will begin.



## IV. MAINTENANCE AND TROUBLESHOOTING

### A. GENERAL

The PB250 Computer is designed to function with a comparatively trouble-free life and the necessary maintenance is at a minimum. However, the computer should be regularly tested under marginal conditions. If the computer fails to meet these marginal requirements, the probable cause may be a weak module card.

The following paragraphs are intended as a guide in performing marginal checks on the ability of the computer memory and of all the commands to function properly under marginal conditions.

### B. MARGINAL CHECKING

To find the margin of safety between the condition of a system and the point of failure, use is made of marginal checking. In the PB250, this procedure is normally followed in routine maintenance to locate deteriorating components before they cause system failure, although in many instances, routine marginal checking may not be necessary due to the comparatively long life of modern transistors. Marginal checking of the PB250 is accomplished by use of:

- 1) PROBE I Diagnostic Routine.
- 2) TEST 1 and TEST 2 switches on the computer control panel (Figure 1-2).

- 3) Varying the +6 and -12 voltage levels on the PS-7 Power Supply between  $\pm 5\%$  limits (Figure 1-3).

#### B-1. CHECKING PROCEDURE

The marginal checking procedural steps are as follows:

- a) Load and start operation of PROBE I (see paragraph C, below).
- b) Set TEST 1 switch to ON position.
- c) Wait two minutes then set TEST 1 switch to OFF position. If failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.
- d) Set TEST 2 switch to ON position.
- e) Wait two minutes then set TEST 2 switch to OFF position. If failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

#### NOTE

Both TEST switches must not be in ON position at the same time or an illegal indication may result.

- f) Set Voltage Selector switch to 6.
- g) Allow PROBE I to run, and decrease the +6-volt supply by 5% by means of the adjustable control on the power supply front panel (Figure 1-3). Adjust meter indication to NOMINAL, if no failure is apparent, proceed to step h. If failure exists

the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

- h) Allow PROBE I to run, and increase +6-volts by 5% as explained in step g. Adjust meter indication to NOMINAL, if failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.
- i) Set Voltage Selector switch to 12.
- j) Allow PROBE I to run, and rotate voltage selection switch on the power supply front panel to 12. Decrease -12-volts by 5% as explained in step g. Adjust meter indication to NOMINAL, if no failure is apparent, proceed to step k. If failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.
- k) Allow PROBE I to run, and increase -12-volts by 5% as explained in step g. Adjust meter indication to NOMINAL, if failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

C. PROBE I DIAGNOSTIC ROUTINE (CAT. # 9003)

A description of the PROBE I diagnostic routine is provided in Table 4-1, followed by the program listing in Table 4-2 and the flow diagrams in Figure 4-1.



Table 4-1. (Sheet 1 of 10)

PROBE I DIAGNOSTIC ROUTINE

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Purpose:	<p>To test the read-write circuitry of the PB250 memory under operator control.</p> <p>To check all commands in the PB250 under marginal operation.</p> <p>To check the punching and reading phases of the Flexo-writer.</p> <p>In addition, the program may link test routines for various peripheral equipments by changing one of the commands (see Use).</p>
Restrictions:	<p>Lines 00 through 07 must be in the machine. Line 00 must be a medium line.</p> <p>If more than minimal operation is desired, an external switch bank must be connected to the computer.</p>
Storage:	<p>All sectors of lines 02 and 03 are used by the program.</p> <p>Sectors 000 through 051, and sector 377 of line 01 are used by the bootstrap loader. The contents of these sectors may be destroyed once the program is loaded.</p> <p>All line 00 sectors are used for temporary storage.</p>
Timing:	<p>When checking memory, the program requires approximately three seconds to write and read one line (optimized).</p> <p>When checking commands, the program requires about one second to test all commands in one line.</p>

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Table 4-1. (Sheet 2 of 10)

PROBE I DIAGNOSTIC ROUTINE

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Timing: When checking the punch-read phase of the Flexowriter,  
(Continued) the program proceeds at the Flexowriter speed of 15  
characters per second.

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Use:

1. Loading

Two tapes are available; one has its own bootstrap loader, and the other may be loaded by the Octal Utility Package. Total time required to load the program is (depending on the tape used) 3-1/2 - 4 minutes.

a. Bootstrap Loading

This tape may be loaded by bootstrap control through conventional use of the FILL switch on the console. Upon completion of loading, if there is no checksum error, control is transferred to sector 000 of line 02. A TRU command to 00002 will be placed in sector 000 of line 01 by the bootstrap so that control may be returned to the beginning of the program at any time by using the ENABLE switch and I key. If there has been a checksum error, the machine will halt and display a line number of  $37)_8$  on the OPERAND lights.

b. Octal Utility Package Loading

This tape may be loaded by the Octal Utility Package by inserting the tape in the mechanical reader and striking the F key. Be sure the BREAK-POINT switch is raised, or loading will halt half way through. Should this happen, the remainder of the tape may be loaded by re-striking the F key. On completion of successful loading, the keyboard light will come back on and control may be transferred to the program by striking the T key. If there has been a checksum error, the machine will halt and display a line number of  $37)_8$ .

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PROBE I DIAGNOSTIC ROUTINE

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Sector 000 of line 02 is the beginning of the program and contains a HALT with a line number of 30)<sub>8</sub>. The HALT instruction indicates the beginning of the program and allows the operator to set up the desired switch configuration. Once everything is in order, the program may be started by clearing parity and raising the ENABLE switch.

2. Modes of Operation

There are two basic modes of operation in the program; Memory and Command. The mode is determined by the position of the BREAKPOINT switch as follows: with BREAKPOINT in the raised position the program operates in Memory Mode (Write-Read II); with BREAKPOINT in the depressed position the program operates in Command Mode. In Memory Mode all lines may be checked except lines 00, 01, 02, and 03. In Command Mode, all commands are checked except DVR, RTK, PTU, and BSO. With no external switch bank connected, the program will check lines 04 through 07 in Memory Mode and lines 03 through 07 in Command Mode. For more specific or extended uses, an external switch bank must be connected to the computer.

3. Switch Bank

For more effective operator control, the program has been set up to scan a switch bank and limit or extend its operation according to the switch settings. The switch bank should be connected so as to be addressable by TES commands on lines 10 through 17. The switches should be wired such that transfer of control will be effected when a switch is in a raised position. Wiring instructions and lists are in Section VI, Logic Diagrams.

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Table 4-1. (Sheet 4 of 10)

PROBE I DIAGNOSTIC ROUTINE

The switch bank is divided into two sections of four switches each. The four left-hand switches define an instruction, and the four right-hand switches define an address. All address designations are in octal.

a. Memory Mode

The following sub-table shows the switch controls for operation in the Memory Mode.

MEMORY MODE *breakpoint w/p*

Switch Line	Raised	Lowered
10	Program halts after checking specified lines.	Program continues after checking specified lines. Switches are rescanned for new instructions.
11	Program will only WRITE random numbers into specified lines.	Program write-reads continuously through all specified lines.
12	Program checks only that line indicated on <i>ADDRESS SWITCHES</i>	Program checks all lines from 04 up to line indicated on address switches.
13	Program write-reads lines 04 through 17.	Program write-reads lines 04 through 07.

When the program is instructed to halt (switch 10), it will halt and display a line number of  $30_8$  which indicates the beginning of the program. Clearing parity at this point will resume computation. Where possible

PROBE I DIAGNOSTIC ROUTINE

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ambiguities occur, lower numbered switches have priority over higher numbered ones. Thus, if switches 12 and 13 are both raised, switch 13 is ignored. With switch 11 raised, random numbers are stored continuously throughout memory but no checking is done. When it is desired to return to Write-Read (by lowering switch 11), the ENABLE switch must be depressed and the I key struck to return control to the beginning. Failure to do this will cause the program to go directly to the Read phase of the Write-Read program and an apparent error will occur due to the fact that the original random number is no longer correct. No complications will result other than the usual error punch-out which may be interrupted by pressing the ENABLE switch.

If an error is detected during a Write-Read phase, the Flexowriter will punch out the sector and line where the error occurred, followed by the number that should have been found and the number that was found. If the error is one of parity, the machine will halt and display an 05 code in the OPERATION lights and the line number where the error occurred in the OPERAND lights. Clearing parity will resume punch-out. Whenever five consecutive errors are noted, the entire line is assumed to be bad and the program will continue with no further punch-out for that line. Switches may be altered during any phase, but their states will not be determined until the current phase is complete. This is a cardinal rule for all operations in the program.

NOTE

No new phase will be initiated, regardless of switch positions, until the current phase is complete. In some cases, this may be 30 or 40 seconds.

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Table 4-1. (Sheet 6 of 10)

PROBE I DIAGNOSTIC ROUTINE

Switches 14 through 17 indicate a line address associated with the operation indicated in switches 10 through 13. Thus, 1001 on the switch bank specifies line 11). A line configuration of 0000 will indicate lines 04 through 07/17 are to be checked, depending upon the state of switch 13. In this case, switch 12 is ignored. Line configuration 0001, 0010, and 0011 are unused in this mode and will be rejected. In the event unused codes are encountered, the program will loop and rescan the switch bank until a legitimate combination is indicated. Sector 073 of line 02 contains a TAN command which notes if an illegal combination is present and returns control to rescan the switches. If so desired, these unused positions may be used to transfer out of PROBE I to other test programs by changing the TAN command to transfer to the desired location. When returning from an external test program, a transfer to sector 000 of line 02 will halt computation at the beginning of PROBE I. If it is desired to return to PROBE I without halting, transfer should be made to sector 001 of line 02.

b. Command Mode

The following sub-table shows the switch controls for operation in Command Mode.

COMMAND MODE *breakpoint down*

Switch Line	Raised	Lowered
10	Program halts after each <i>Block check</i>	Program continues after each block is checked.

Raised: Program halts after  
each block check

Lowered: Program continues  
after each block is checked

Table 4-1. (Sheet 7 of 10)

PROBE I DIAGNOSTIC ROUTINE

COMMAND MODE (Continued) *Breakpoint down*

Switch Line	Raised	Lowered
11	Program repeats current block using same number only if error occurs.	Program halts if error in current block and displays block number in OPERAND lights.
12	Program repeats current block using different numbers unless error.	Program continues to next block in sequence with a different number unless error.
13	Program executes commands in all lines, 03 through 17.	Program executes commands in all lines, 03 through 07.

There are  $20)_8$  command blocks in this mode which operate with random numbers where applicable. Command blocks are numbered  $01)_8$  through  $20)_8$ , consecutively and the commands checked in each block are listed below. When one block is complete, if no error is noted, the next block in sequence is checked, and so on. When the last block has been checked, the program is moved to the next higher line and the process repeats. When the last line has been checked, the program returns to scan the switches and proceeds from there. The time required to check the entire  $16)_10$  blocks is about one second and the progress of the program through the lines may be noted by observing the K flip-flops on the computer console.

PROBE I DIAGNOSTIC ROUTINE

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Whenever the program executes a halt in this mode, the block number where the halt occurred will be displayed on the OPERAND lights except when the last block is reached and the program returns to the beginning, at which time the line number displayed will be 30)<sub>8</sub>. If switch 10 is raised, the program will halt unconditionally after each block. Thus, if it is desired to repeat block 06 continuously, switch 10 should be raised and the program cycled by means of the ENABLE switch until 06 appears on the OPERAND lights. Then switch 12 should be raised, switch 10 lowered, and the program allowed to run. In this manner, block 06 will be checked continuously with different numbers until an error is detected or the switch configuration is changed.

Switches 14 through 17 define an address to be used in reference to the other switches. A switch configuration of 0000 will automatically check lines 03 through 07/17 depending on the setting of switch 13. An address of 0010 will initiate a punch-read phase. In this phase, five inches of leader are punched, followed by a marker character of 8 "ones" and 64 frames of random digits. When the last frame has been punched, another five inches of trailer is punched and the frames punched are read back into the machine and checked. During punch-out, there will be sufficient time for the operator to insert the tape in the mechanical reader so that reading may be started immediately on completion of punching. When an error is detected, the reader halts momentarily (about three seconds) and the light on the Flexo-writer flashes. If the ENABLE switch is pressed while this light is on, the character just read may be viewed in the OPERATION and OPERAND lights on the console. By comparing the state of the lights against the frame just read, the operator may determine which read channel has failed. If the frame and display agree, then the error occurred during the punch phase. Raising the ENABLE switch will allow resumption of the test. When

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Table 4-1. (Sheet 9 of 10)

PROBE I DIAGNOSTIC ROUTINE

the test is complete, the program returns to the beginning and halts with a line display of 30)<sub>8</sub>.

All other configurations of the address switches indicate which line is to be tested. Only the particular line indicated will be tested. Line 01 may be tested, but if the Octal Utility Package is in this line, it will be destroyed. When the program is loaded by bootstrap, a TRU command to 00002 is stored in sector 000 of line 01 so that control may be returned to the beginning of the program at any time by use of the I key. This TRU command is also in sector 000 of line 03 and, when line 01 is tested, this command will be moved to 00001 so that the operator may still return to sector 000 of line 02 even after destroying the former contents of line 01 by checking that line.

The following sub-table lists the command blocks by number (in octal) and the commands checked in that block. Commands which are not listed in this sub-table are considered to have been checked elsewhere, i. e., LAI, CIB, etc.

COMMAND BLOCK NUMBERS

Block Diagram	Commands Checked
01	IAC, IBC, ROT
02	LDC, CLA, ADD, SUB
03	MUP, DIV
04	MAC, AMC, EXF, AOC
05	LDP, STD, DPA, DPS, TOF
06	TAN, TBN, TCN, TRU, CLB
07	LDB, STB, EBP, IAM
10	LDA, CLC, STC, NAD, SAI
11	RSI, CAM
12	MLX, LST <small>SLT</small> ( 26, 21*)

Table 4-1. (Sheet 10 of 10)  
PROBE I DIAGNOSTIC ROUTINE

COMMAND BLOCK NUMBERS (Continued)

Block Diagram	Commands Checked
13	RFU, DIU, TES (36)
14	LRS, GTB (33, 41)
15	NOP
16	SBR, LSD
17	BSI, STA
20	SQR

Table 4-2. (Sheet 1 of 19)

## PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OF CODE	REMARKS
000	000 0030;	HLT	= Start of program
001	002S0702;	LDP	Clear A and put marker bit in B
002	000S0000;	CONST	
003	000 0000;	CONST	
004	020S7100;	MCL	Initialize
005	[050 7710;]	TES	Add 1 if switch lowered
006	047S1400;	ADD	
007	000 00001	CONST	1
010	052 2110;	LST	
011	047 3602;	TBN	
012	112S0100;	IAC	Increment line
013	125 0500;	LDA	
014	135S1400;	ADD	
015	000 0001;	CONST	
016	145 1100;	STA	Return to next switch
017	044S0100;	IAC	
020	045S3700;	TRU	Read switches
021			Begin memory mode
022	023S0402;	LDC	
023	000 0002;	CONST	
024	015 1000;	STC	Set first line = 04
025	034 2210;	RST	6
026	032 3602;	TBN	Switch 13
027	030S0402;	LDC	$\overline{S13}$ ; last line = 07
030	000 0043;	CONST	
031	034S1000;	STC	S13; last line = 17
032	033S0402;	LDC	
033	000 0047;	CONST	
034	014 1000;	STC	1
035	037 2200;	RSI	

Table 4-2. (Sheet 2 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OF CODE	REMARKS
036	042 3602;	TBN	Switch 12
037	040S0402;	LDC	S12; Disable setting of last line
040	076 3502;	TAN	
041	044S3702;	TRU	
042	043S0402;	LDC	S12; Enable setting of last line
043	015 1100;	STA	
044	075 1002;	STC	
045	050 2210;	RST	2
046	056S3702;	TRU	
047	000 1100;	STA	Save scanned word
050	051S0502;	LDA	Take one's complement
051	000 0377;	CONST	
052	000 1500;	SUB	
053	100 7735;	TES	B. P.
054	022S3702;	TRU	
055			
056	062 3602;	TBN	Switch 10
057	060S0402;	LDC	S10; Set return for no halt
060	001S3702;	TRU	
061	064S3702;	TRU	
062	063S0402;	LDC	S10; Set return for halt
063	000S3702;	TRU	
064	264 1003;	STC	
065	072 2110;	LST	4
066	000 4500;	CLA	
067	075 2110;	LST	Save address only
070	003 5602;	CAM	If address = 0000, exit to Write-Read II
071	077 7502;	TOF	
072	023 1502;	SUB	Subtract 4,
073	001 3502;	TAN	If negative, return to rescan

Table 4-2. (Sheet 3 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OF CODE	REMARKS
074	023 1402;	ADD	Not negative, restore address
075	[015 1100;]	STA TAN	Address = first line if S12
076	014 1100;	STA	Address = last line
077	124S4400;	CLC	Set read mode and exit
100	101S0402;	LDC	Begin command mode
101	000 0041;	CONST	
102	103 1037;	STC	Set index = 03
103	104S4002;	EBP	
104	377S7720;	CONST	For switch 13
105	110 3502;	TAN	
106	030 0402;	LDC	$\overline{S13}$ ; set last line = 07
107	111S3702;	TRU	S13; set last line = 17
110	033 0402;	LDC	
111	012 1000;	STC	Extract off address
112	000 0100;	IAC	
113	033 4202;	AMC	Exit if address = 0000
114	000 0300;	ROT	
115	003 5602;	CAM	Exit to punch-read if address = 0010
116	372 7503;	TOF	
117	120S5602;	CAM	Exit to punch-read if address = 0010
120	000 0001;	CONST	
121	265 7503;	TOF	Otherwise address to index
122	123 1137;	STA	
123	012 1100;	STA	And last line
124	372S3703;	TRU	Exit to command mode
125	160 1002;	STC	Store phase constant
126	127S0502;	LDA	Prestore first random number
127	047 2646;	CONST	
130	004 1100;	STA	
131	005 1100;	STA	

Table 4-2. (Sheet 4 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OF CODE	REMARKS
132	141 3402;	TCN	Test phase constant
133	135 2100;	LSD	Was read, set write
134	160 1002;	STC	
135	005 0500;	LDA	Ki → Ko
136	004 1100;	STA	First line to index
137	155 0600;	LDB	
140	143S1237;	STB	Was write, set read
141	143 2200;	RSI	
142	160 1002;	STC	
143	171S3702;	TRU	Test phase constant = read
144	152 3402;	TCN	
145	146S0702;	LDP	Reset error counter (Ce) and prestore CAM
146	000 0000;	CONST	
147	200 5600I	CAM	
150	007 1200;	STB	
151	154S3702;	TRU	Prestore STA
152	153S0502;	LDA	
153	200 1100I	STA	Put store-check sequence in line 00
154	156 1102;	STA	
155	164S7100;	MCL	Store and check sequence
156	200 1100I	CAM STA	
157	240S0400;	LDC	
160	377S7777I	CONST	
161	244 7502;	TOF	With Ki
162	250 3402;	TCN	
163	266S3702;	TRU	
164	165S0600;	LDB	= +2304555
165	355S6567I	CONST	
166	167S0402;	LDC	
167	046 2233I	CONST	

Table 4-2. (Sheet 5 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
170	220S3200;	MUP	Generate $K_i + 1$
171	004 0500;	LDA	$K_o \rightarrow K_i$
172	005 1100;	STA	
173	137S3702;	TRU	
174	007 1000;	STC	(From 276) $C_e + 1 = C_e$
175	176S1102;	STA	Save $N_r$ = read phase number
176		CONST	
177	016 0500;	LDA	Prepare to pick up
200	201S1502;	SUB	
201	000 5100;	CONST	
202	203 1102;	STA	Nw = write phase number
203	204 0500I	LDA	
204	165 1102;	STA	
205	016 0600;	LDB	Pick up $N_w$
206	000 4500;	CLA	
207	221 2110;	LST	With CAM in check sequence
210	000 0100;	IAC	
211	212 0637;	LDB	
212	233 2110;	LST	16
213	000 0100;	IAC	Merge with SSS
214	227 2210;	RST	10
215	006 1200;	STB	Save for punch out
216	376 0706;	LDP	Save 37606 and 37706
217	220S4400;	CLC	
220	225S1200;	STB	Save B for next random number
221	010 1300;	STD	
222	012 1000;	STC	To reset space counter
223	306 0702;	LDP	Set space punch mode and limit = 5
224	263 1302;	STD	
225	226S0600;	LDB	

Table 4-2. (Sheet 6 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
226	236S3700;	TRU	Exit to store-check sequence
227	000 4500;	CLA	
230	234 2110;	LST	3, to extract one digit
231	006 1200;	STB	Save rest for later punching
232	000 4300;	CLB	
233	000 4400;	CLC	Copy digit to C
234	235 0000;	MAC	
235	003 5602;	CAM	Is digit = 0?
236	000 4100;	GTB	To check parity
237	000 0100;	IAC	Return original digit to A
240	243 3402;	TCN	Parity odd or even?
241	245 1402;	ADD	Was even, add 1 At 17
242	241 7502;	TOF	Digit was zero, add again
243	251S1402;	ADD	Add into WOC
244	245S4500;	CLA	No error, reset Ce
245	000 0004;	CONST	= 1 at 17
246	247S1100;	STA	In Ce
247	313S3702;	TRU	Punch return
250	256S0500;	LDA	With CAM/STA
251	000 1400;	CONST	WOC skeleton and delay number
252	277 2210;	RST	Put command in B
253	247 0502;	LDA	With punch return
254	376 1306;	STD	
255	251 0402;	LDC	To line 06 for punch-out
256	376S3706;	TRU	
257	260S1402;	ADD	
260	001 0000;	CONST	Increment sector
261	276S1100;	STA	
262	000 6116;	WOC	Carriage return
263	000 0000;	CONST	For punch limit



Table 4-2. (Sheet 7 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
264	000 6116;	WOC	Space or carriage return
265	321S3702;	TRU	
266	267S0400;	LDC	With Ce
267	377S7736I	CONST	Limit = 8
270	271S0100;	IAC	Save A in C
271	010 0000;	CONST	N = 1, for command mode
272	273S5602;	CAM	If Ce = 5, no further punching
273	000 0042;	CONST	
274	250 7502;	TOF	Ce ≠ 5, exit to punch-out sequence
275	337 1402;	ADD	
276	173S0100;	IAC	(From 261) overflow if last sector
277	301 7502;	TOF	
300	165S0600;	LDB	Not last sector, return to begin
301	302S4500;	CLA	To reset Ce
302	303S1137;	STA	(From 377) restore index
303	304S0437;	LDC	With index
304	004S3700I	TRU	Return to begin of command mode
305	307S1100;	STA	In Ce
306	377S7776I	CONST	Limit = 5,
307	000 6020;	WOC	
310	311S4202;	AMC	Extract off line number
311	000 0047;	CONST	
312	331S0300;	ROT	From index register
313	263 0402;	LDC	
314	316 2200;	RSI	Increment digit counter
315	263 1002;	STC	
316	225 3402;	TCN	Return to punch if not through
317	264 0702;	LDP	Word done; punch space or carriage return and go to 321
320	254S3702;	TRU	
321	264 0502;	LDA	With termination character

Table 4-2. (Sheet 8 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
322	262 5602;	CAM	If carriage return, line done
323	360 7502;	TOF	
324	267 0602;	LDB	Line not done, set punch Limit = 8
325	263 1202;	STB	
326	012 0500;	LDA	Test space counter
327	365 3502;	TAN	
330	267 1402;	ADD	Space counter +; make -
331	012 1100;	STA	
332	341S3702;	TRU	
333	334S5600;	CAM	(From 312) compare index with last line
334			
335	357 7502;	TOF	Not last line, increment index and return to begin
336	337S1402;	ADD	
337	000 0040;	CONST	
340	163S1137;	STA	Since space counter +, Pick up Nw
341	165 0602;	LDB	
342	165 0402;	LDC	Extract sign
343	345 2110;	LST	
344	006 1200;	STB	Check sign of Nw/Nr
345	352 3402;	TCN	
346	347S0702;	LDP	Sign positive, punch +
347	000 6036;	[WOC]	
350	225S3702;	[TRU]	
351	254S3702;	TRU	Sign negative, punch -
352	353S0702;	LDP	
353	000 6037;	[WOC]	
354	225S3702;	[TRU]	
355	254S3702;	TRU	Pick up phase constant
356			
357	360S0400;	LDC	



Table 4-2. (Sheet 10 of 19)

## PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OF CODE	REMARKS
00003\$	000S3702;	TRU	Return to beginning
001	011 1100;	STA	(From 37303) set first block(N = 1)
002	127 0502;	LDA	Prestore first random number
003	006 1100;	STA	
004	005S7100I	MCL	Move test to indexed line and transfer there
005	006S3700I	TRU	
006	167 0602;	LDB	Generate random number
007	006 0400;	LDC	
010	040 3200;	MUP	
011	006 1200;	STB	
012	010 1100;	STA	Assemble jump command for transferring to block N
013	011 0500;	LDA	
014	15S1400I	ADD	
015	051S3700I	[TRU]	
016	020 1100I	STA	
017	010 0500;	LDA	Pick up random number
020	[251S3700I]	TRU	Transfer to block N
021	010 5600;	CAM	Transfer to 032
022	032 7500I	TOF	if no error
023	017 7711;	TES	Switch 11: repeat if error halt & display N if error
024	025S3700I	TRU	
025	011 0500;	LDA	Pick up block number
026	047 2210;	RST	
027	031 2537;	IAM	Save index
030	000 0000I	HLT	Halt and display N
031	033 2537;	IAM	Restore index
032	011 0500;	LDA	Pick up N
033	034S5600I	CAM	Test for maximum N
034	200 0000;	CONST	
035	254 7500I	TOF	Transfer to 254 if through

Table 4-2. (Sheet 11 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
036	041 7712;	TES	S12: Do not increment N
037	271 1402;	ADD	S12: Increment N
040	011 1100;	STA	
041	043 7710;	TES	
042	004S3703;	TRU	S10: Halt and display N
043	374S3702;	TRU	S10: Continue in Sequence
044	045 0437;	LDC	Pick up index
045	033 4202;	AMC	Extract off line number
046	000 0300;	ROT	Is this last line?
047	012 5600;	CAM	
050	001 7502;	TOF	Transfer to 00102 if last line
051	337 1402;	ADD	Not last line; increment index
052	053 1137;	STA	
053	271 0502;	LDA	Set N = 1
054	011 1100;	STA	
055	041S3703;	TRU	Return to test S10
056	060 7710;	TES	(From 256LL)
057	044S3700I	TRU	Halt and display N if S10
060	056S0030;	HLT	

Table 4-2. (Sheet 12 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
254	006 0500;	LDA	(From 035LL) Change original random number
255	127 1102;	STA	
256	056S3700I	TRU	
257	253S6000;	WOC	(From 371LL) Flash light and display Input character
260	174 0402;	LDC	
261	256S5100;	RTK	
262	005 0500;	LDA	Change random number and return to scan switches
263	127 1102;	STA	
264	000S3702;	TRU	
265	127 0502;	LDA	Begin punch-read: initialize First random number
266	007 1100;	STA	
267	000 4500;	CLA	
270	010 1100;	STA	Set punch phase
271	104 0602;	LDB	
272	006 1200;	STB	
273	274S0703;	LDP	Set limit = 64
274	000 6000;	[WOC]	
275	301S3703;	[TRU]	
276	074 0402;	LDC	To punch leader
277	376 1306;	STD	
300	376S3706;	TRU	
301	010 0400;	LDC	With large delay number
302	313 3403;	TCN	
303	007 0500;	LDA	
304	011 1100;	STA	Punch 5 inches of leader
305	306S0703;	LDP	
306	000 6737;	[WOC]	
307	336S3703;	[TRU]	Transfer to 31303 if read phase
310	311S0403;	LDC	
311	000 2000;	CONST	
			Pick up first random number
			Punch 8-channel marker and go to 33603
			Delay = +0004000

Table 4-2. (Sheet 13 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
312	27753703;	TRU	Initiate read phase
313	011 0500;	LDA	
314	007 1100;	STA	
315	31650503;	LDA	Turn read switch off (To remain off until marker is read)
316	32755503;	[LAI]	
317	321 1103;	STA	
320	32254500;	CLA	Enter read sequence
321	36455503;	LAI	Read one frame
322	32035200;	RPT	
323	324 5200;	RPT	
324	323 7736;	TES	
325	322 7736;	TES	
326	32455700;	CIB	
327	000 01771	CONST	LAI mask
330	327 5603;	CAM	Transfer to 33303 when marker frame is read
331	333 7503;	TOF	
332	32254500;	CLA	Return to read sequence
333	33450503;	LDA	Marker has been read; Turn read switch on
334	36455503;	[LAI]	
335	321 1103;	STA	Generate next random digit
336	007 0600;	LDB	
337	167 0402;	LDC	
340	370 3200;	MUP	Save LSH for next number
341	007 1200;	STB	
342	000 0100;	IAC	Extract off eight bits
343	327 4203;	AMC	
344	010 0400;	LDC	Transfer to 36203 if read phase
345	362 3403;	TCN	
346	375 2110;	LST	Assemble into WOC command
347	251 1402;	ADD	

Table 4-2. (Sheet 14 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OF CODE	REMARKS
350	375 2210;	RST	Set return address
351	352S0503;	LDA	
352	355S3703;	TRU	
353	251 0402;	LDC	With delay
354	277S3703;	TRU	Out to punch digit
355	006 0500;	LDA	Return from digit punchout
356	007 1402;	ADD	
357	006 1100;	STA	
360	336 3503;	TAN	Return to 33603 if not done
361	270S1000;	STC	Through; restore counter (From 34405) Save random digit and return to read
362	012 1200;	STB	
363	322S4500;	CLA	
364	000 01771	CONST	LAI mask
365	012 5600;	CAM	Enter here after marker frame read; go to 37403 if no error
366	374 7503;	TOF	
367	372 2110;	LST	Error: assemble input character into WOC command & go to 26003
370	250 1403;	ADD	
371	257S1103;	STA	(From 12402) pick up N = 1 Go to beginning of command mode
372	271 0502;	LDA	
373	001S3703;	TRU	
374	006 0500;	LDA	Pick up frame counter
375	007 1402;	ADD	Increment
376	006 1100;	STA	Restore counter
377	336 3503;	TAN	Return if not last frame



Table 4-2. (Sheet 15 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
06103	062S0100;	IAC	BLOCK 01
063	064S0200;	IBC	
065	017S0300;	ROT	
07103	010 0400;	LDC	BLOCK 02 Put number in C Zeros to C Number to A If C negative, error Test ADD and SUB
072	073S4500;	CLA	
074	075S0100;	IAC	
076	023 3400I	TCN	
077	020 1400I	ADD	
100	020S1500I	SUB	
10103	074S0100;	IAC	BLOCK 03 Number to C, copy to B Check MUP, DIV If negative, correct quotient Return to check DIV correction Return to check
075	102S4200I	AMC	
102	-7777777	CONST	
103	132 3200;	MUP	
104	133 3100;	DIV	
105	107 3600I	TBN	
106	017S0300;	ROT	
107	030 1600I	DPA	
110	017S0300;	ROT	
030	+000000I	CONST	
11103	000 4400;	CLC	BLOCK 04 Copy number to C Copy number to B Check AMC, EXF, AOC Return to check
112	113 0000;	MAC	
113	114S4200I	AMC	
114	-7776000	CONST	
115	000 0200;	IBC	
116	114 4700I	EXF	
117	114 4600I	AOC	
120	017S0300;	ROT	

Table 4-2. (Sheet 16 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OF CODE	REMARKS
12103	114 0600I	LDB	Negative number to B
122	124 3600I	TBN	
123	023S3700I	TRU	
124	017 1600I	DPA	If TBN fails, error Check DPA, STD
125	000 1300;	STD	
126	061S4500;	CLA	Check for zero after CLA
062	063S4300;	CLB	
064	066S5600I	CAM	
066	+0000000	CONST	
067	127 7500I	TOF	Error if TOF fails
070	023S3700I	TRU	
127	000 0700;	LDP	Check LDP, DPS
130	017S1700I	DPS	
13103	072S4300;	CLB	Zero to C
073	131S0200;	IBC	
132	133 0000;	MAC	Copy A to C Copy C to B
133	102 4200I	AMC	
134	157 3500I	TAN	If A positive then B and C must be also If not, error
135	023 3600I	TBN	
136	023 3400I	TCN	
137	032S3700I	TRU	Continue to next block
157	167 3600I	TBN	A was negative, B must be or else error
160	023S3700I	TRU	
167	032 3400I	TCN	A and B negative, C must be or else error
170	023S3700I	TRU	

Table 4-2. (Sheet 17 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
14103	127 0600I	LDB	With 7 at 14 <span style="float: right;">BLOCK 07</span>
142	004 1200;	STB	Save in F04
143	145 2500;	IAM	Interchange random number & F04
144	114 4000I	EBP	Extend bit 12 to sign bit
145	147 3500I	TAN	A must now be negative, other wise error
146	023S3700I	TRU	
147	004 0500;	LDA	Pick up original number and return to check
150	021S3700I	TRU	
15103	000 4400;	CLC	Set C = 0 <span style="float: right;">BLOCK 10</span>
152	226 2000;	NAD	Normalize then rescale (C) should = 0
153	227 2300;	SAI	
154	000 0100;	IAC	Number to C, then to F00
155	000 1000;	STC	
156	020S0500;	LDA	Pick up number & return to check
16103	000 4400;	CLC	Set C = 0 <span style="float: right;">BLOCK 11</span>
162	203 2200;	RSI	Right shift 16 places (C) should now be +0000020
163	000 0100;	IAC	
164	245 5602;	CAM	Check to see if it is
165	032 7500I	TOF	
166	023S3700I	TRU	To error sequence
24502	+0000020	CONST	
20103	000 5300;	RFU	sRf, sTf <span style="float: right;">BLOCK 13</span>
202	023 7736;	TES	Should not transfer
203	000 5000;	DIU	rRf, rTf
204	032 7736;	TES	Should now transfer

Table 4-2. (Sheet 18 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

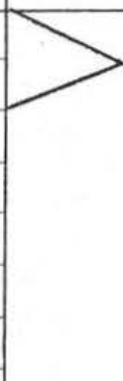
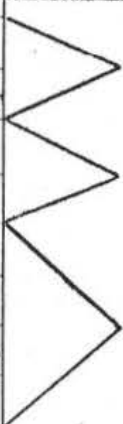


LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
17103	177S2600I	MLX	 <p>Move block to 07</p> <p>With random number</p> <p>With 1 at 17</p> <p>Should shift right 17 places</p> <p>Back 17 places</p> <p>Out to check</p>
177	172S3707;	TRU	
172	010 0400;	LDC	
173	245 0602;	LDB	
174	223 3200;	MUP	
175	217 2110;	LST	
176	021S3700I	TRU	
21103	200 0500I	LDA	 <p>Constant to A</p> <p>Parity is even therefore</p> <p>A should be positive</p> <p>Check GTB</p>
200	+0222222	CONST	
212	215 3320;	LRS	
213	023 3500I	TAN	
214	000 4100;	GTB	
215	216S5600I	CAM	
216	-7707070	CONST	
217	022S3700I	TRU	
22103	140S2400;	NOP	 <p>Check NOP and Oc</p>
140	220S2400;	NOP	
220	021S2400;	NOP	
23103	221S4400;	CLC	 <p>Set C = 0</p> <p>Should clear A</p> <p>Check for A = 0</p> <p>A not equal to zero; error</p> <p>See if C decrements; since</p> <p>C was zero, should now be neg.</p> <p>Error exit if C not negative</p>
222	226 3300;	SBR	
223	066 5600I	CAM	
224	226 7500I	TOF	
225	023S3700I	TRU	
226	233 2100;	LSD	
227	032 3400I	TCN	
230	023S3700I	TRU	
066	+0000000	CONST	

Table 4-2. (Sheet 19 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

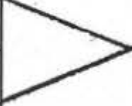




LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
24103	245 11001	STA	Put number in 245 <span style="float: right; border: 1px solid black; padding: 2px;">BLOCK 17</span>
242	102 04001	LDC	 Put all 1's in F05  If no external buffer, 245 → F05  BSI mask  Pick up BSI'ed word  Out to error check
243	005 1000;	STC	
244	246S7300;	BSI	
245	+0000000	CONST	
246	005 0500;	LDA	
247	021537001	TRU	
102	-7777777	CONST	
25103	032 35001	TAN	Reject if number neg: <span style="float: right; border: 1px solid black; padding: 2px;">BLOCK 20</span>
252	204S0100;	IAC	 Square number  Take square root  Subtract original number difference should be no →A: more than $2^{-21}$
205	010 0600;	LDB	
206	235 3200;	MUP	
207	235 3000;	SQR	
210	230S1700;	DPS	 Check for $+ 2^{-21}$
232	000 0300;	ROT	
233	030 56001	CAM	 Check for zero
234	032 75001	TOF	
235	066 56001	CAM	 Check for $- 2^{-21}$
236	032 75001	TOF	
237	102 56001	CAM	
240	022S37001	TRU	

Table 4-3.

ABBREVIATIONS USED IN PROBE I FLOW DIAGRAM

RETN	Return
STRT	Start
PR	Punch Read
MEM	Memory
COM	Command
ES	Error Sequence
CAM/STA	Compare A and M/Store A
TOF	Transfer on Overflow
OF	Overflow
BP	Breakpoint
SSS	Three digit symbol to indicate sector number
LL	Two digit symbol to indicate line number

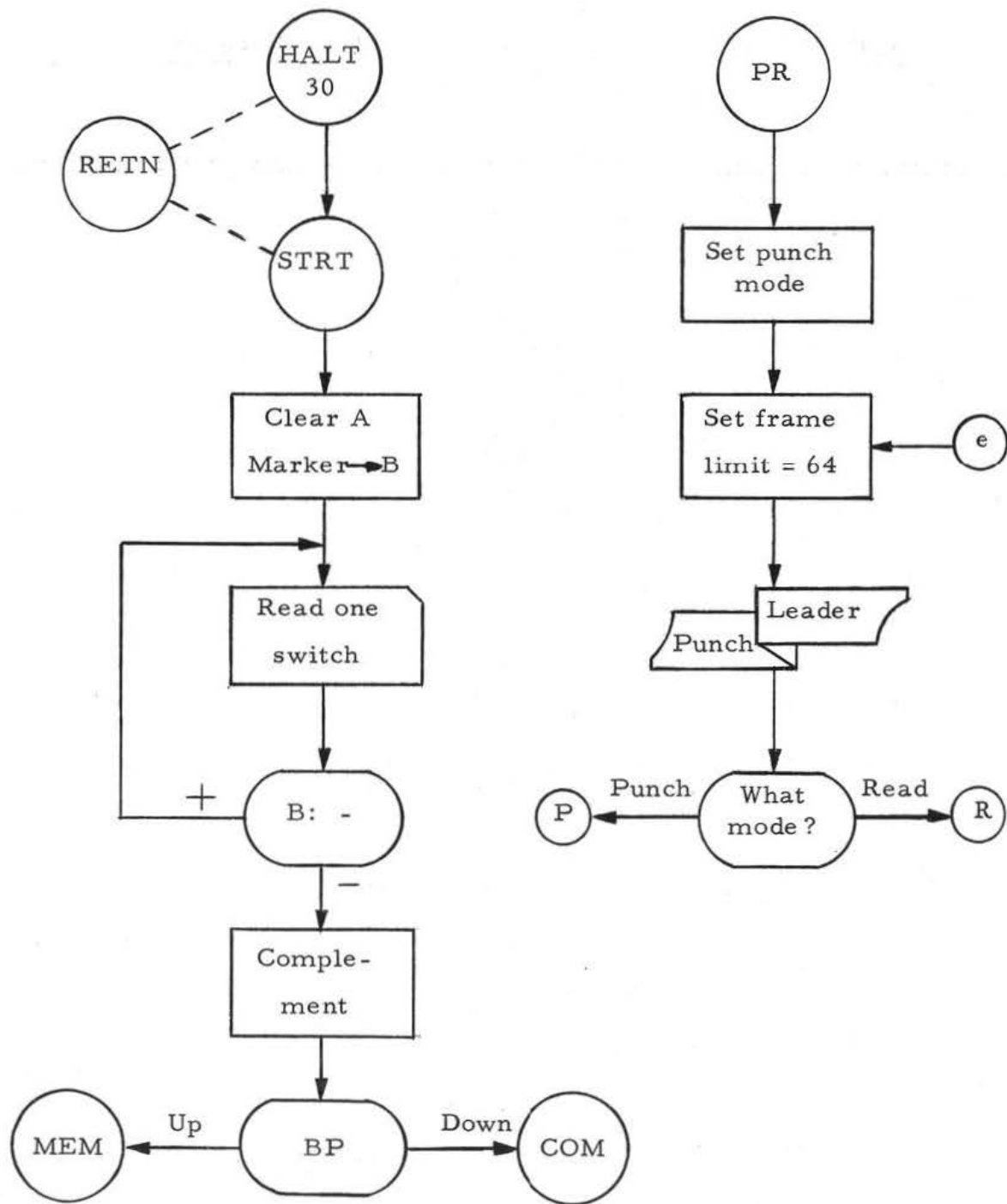


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 1 of 8)

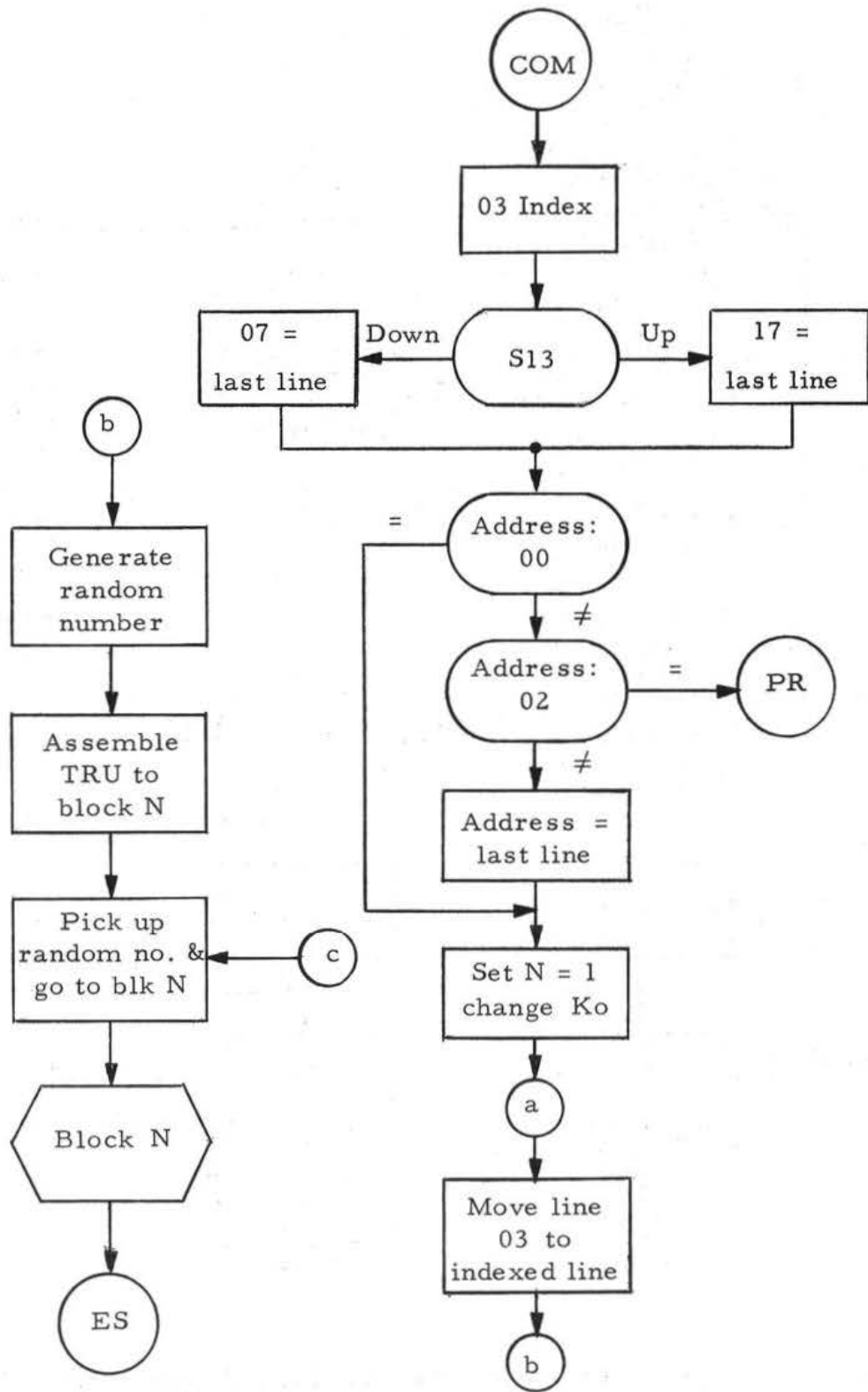


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 2 of 8)



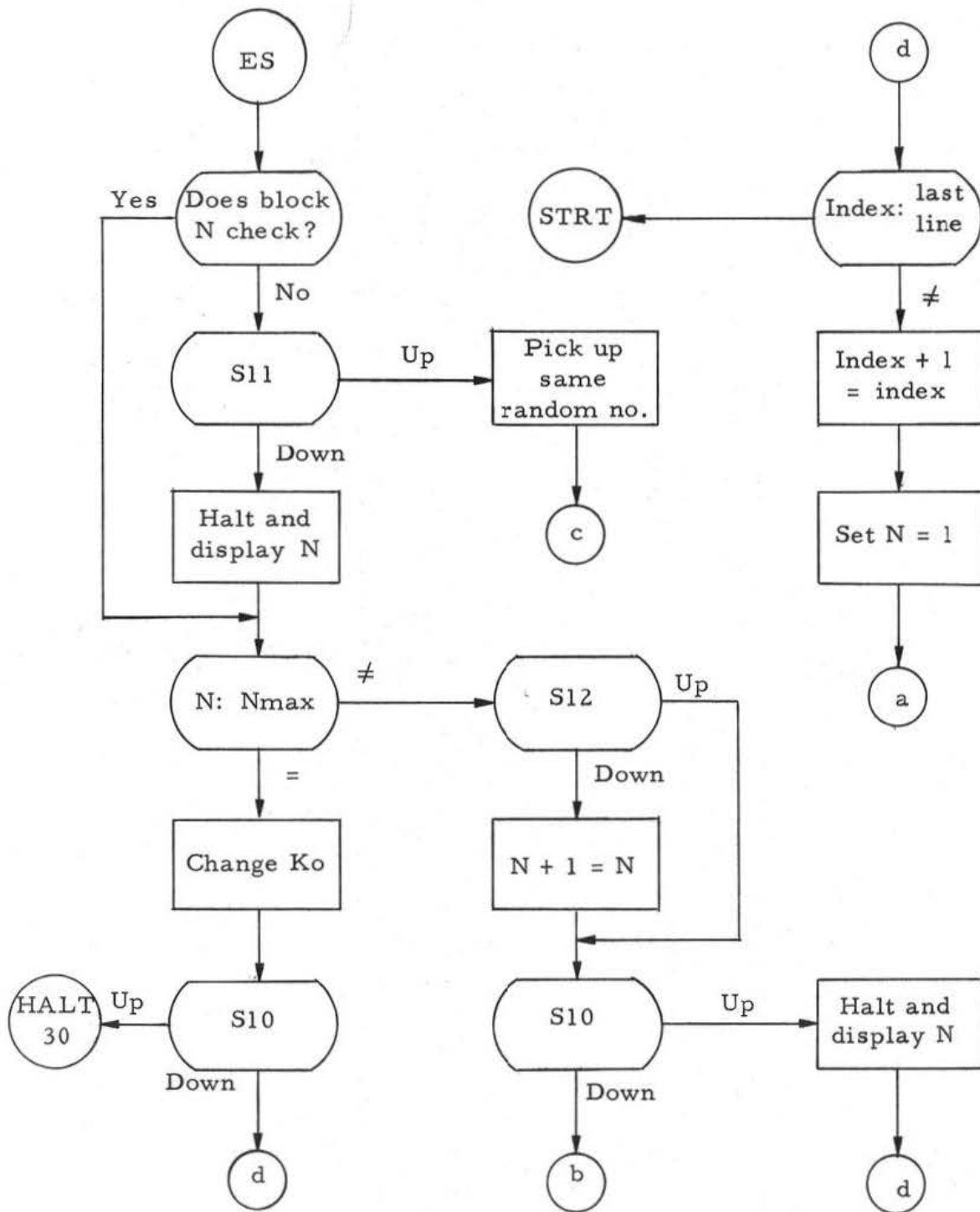


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 3 of 8)

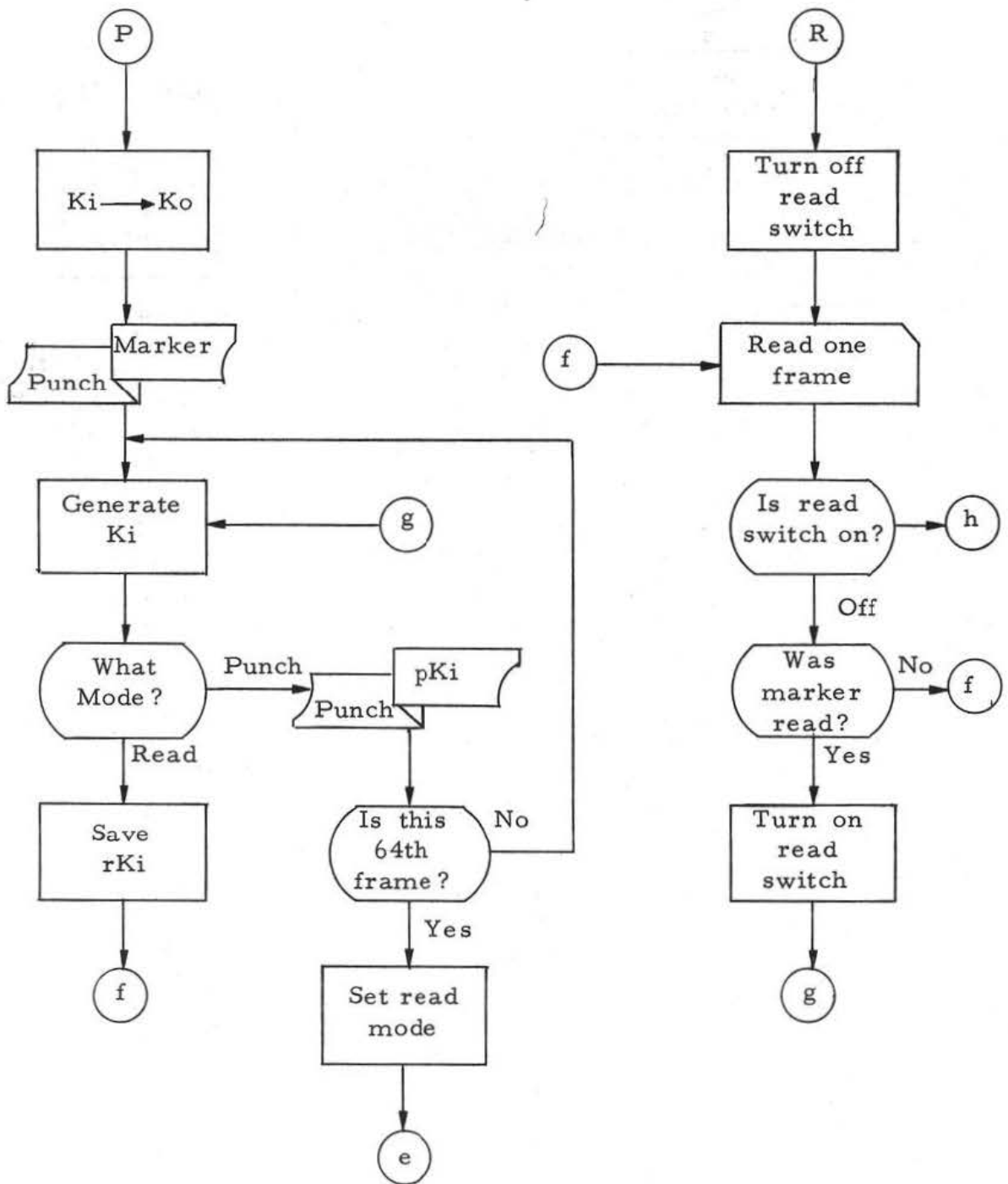


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 4 of 8)

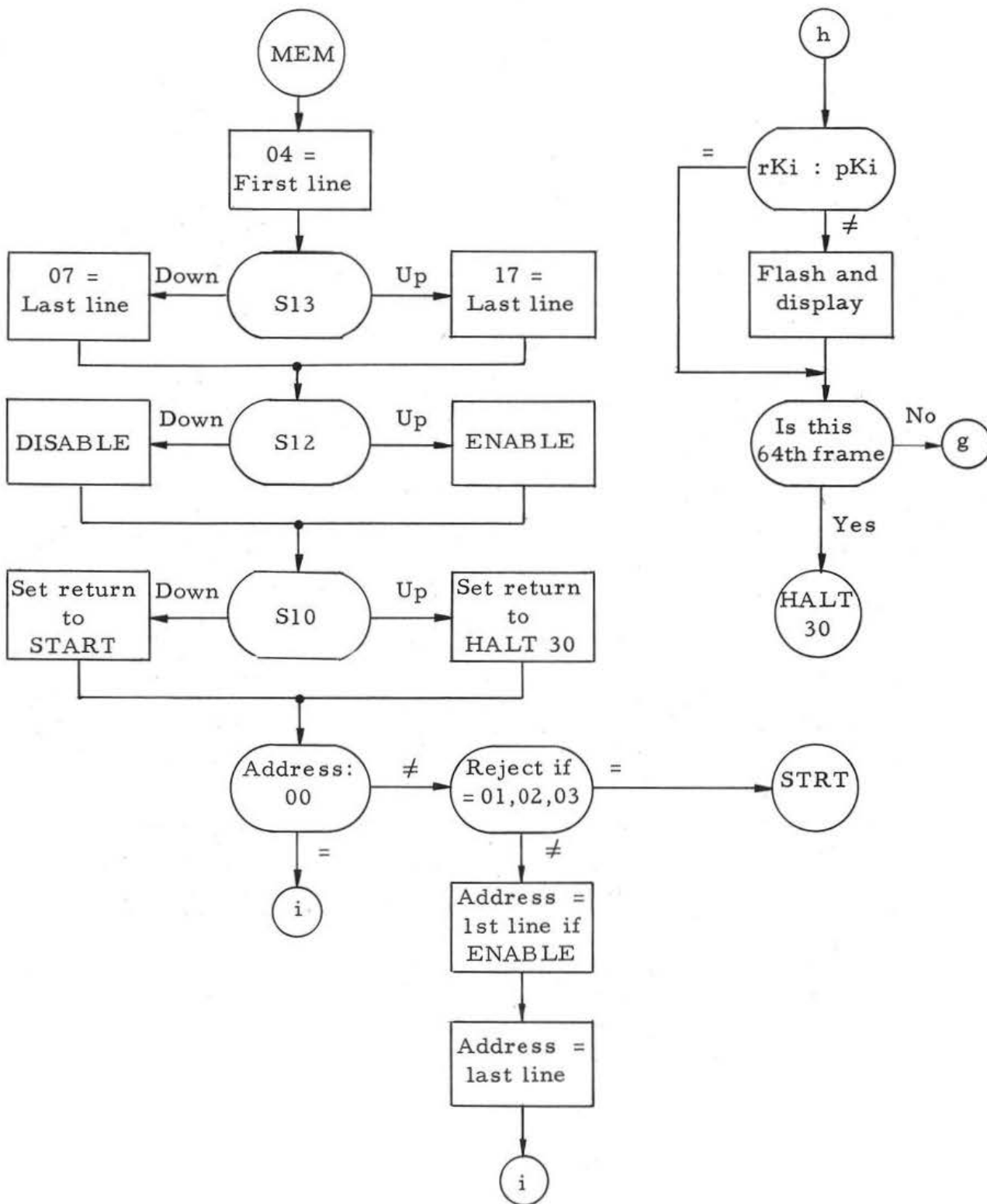


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 5 of 8)

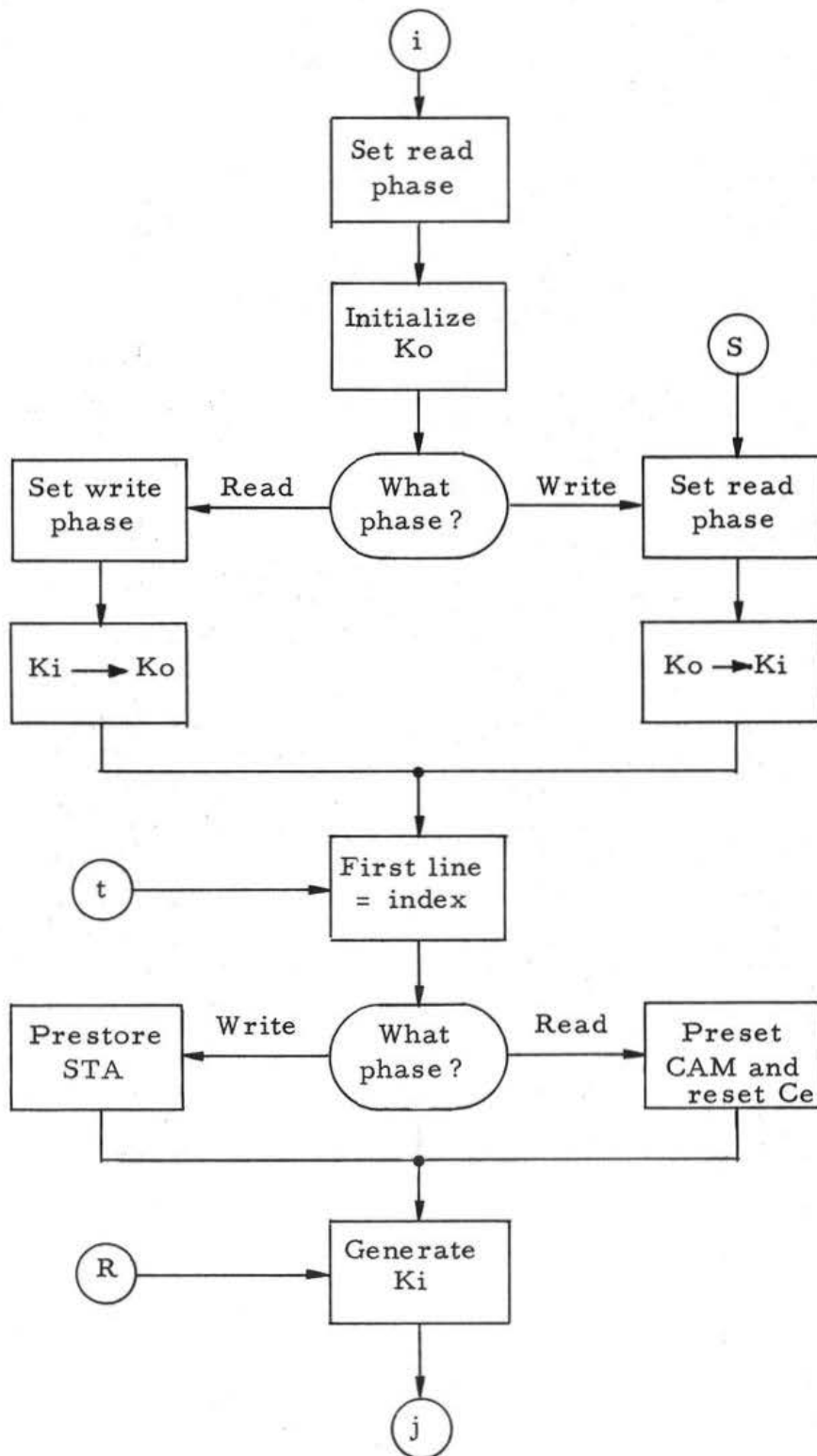


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 6 of 8)

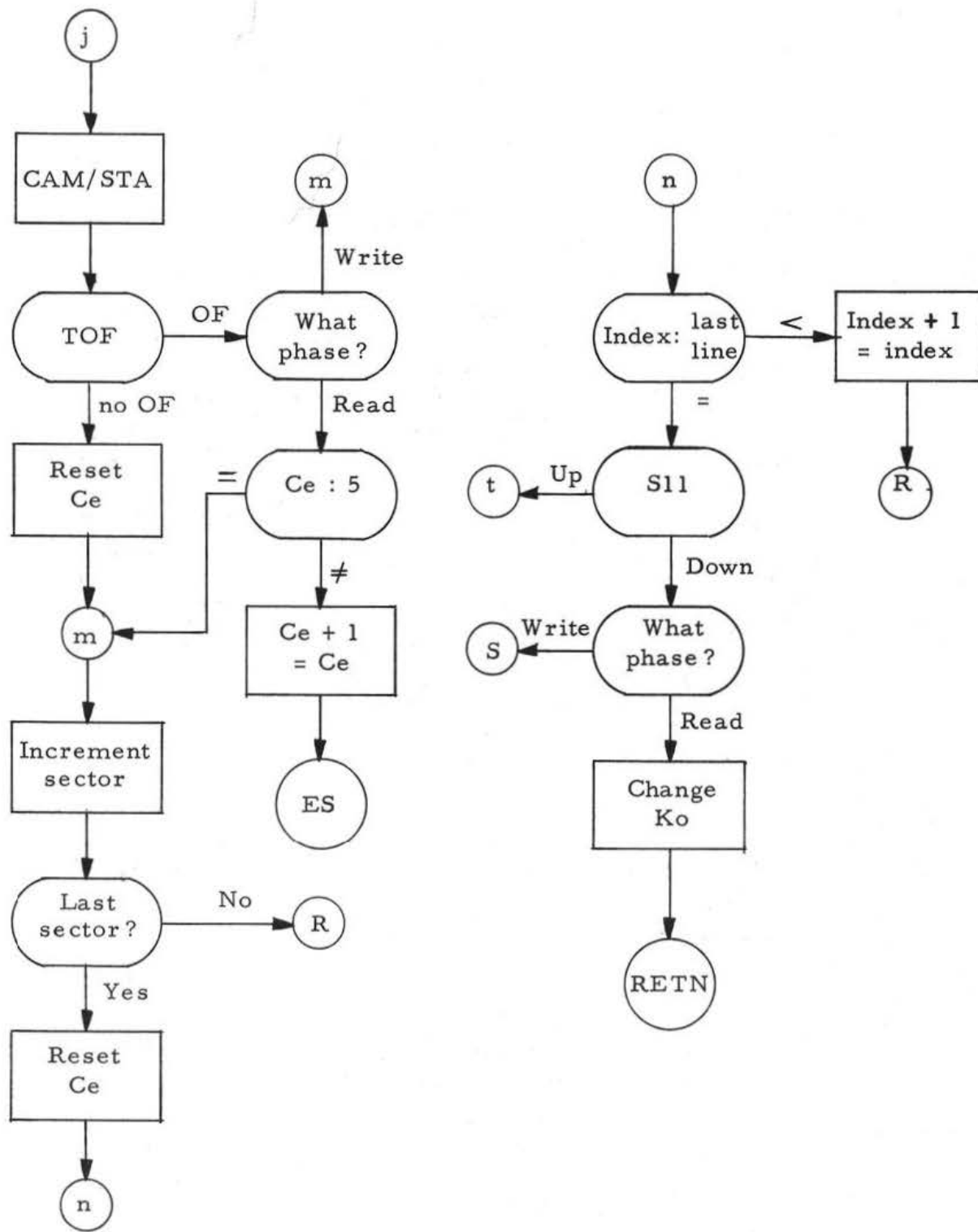


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 7 of 8)

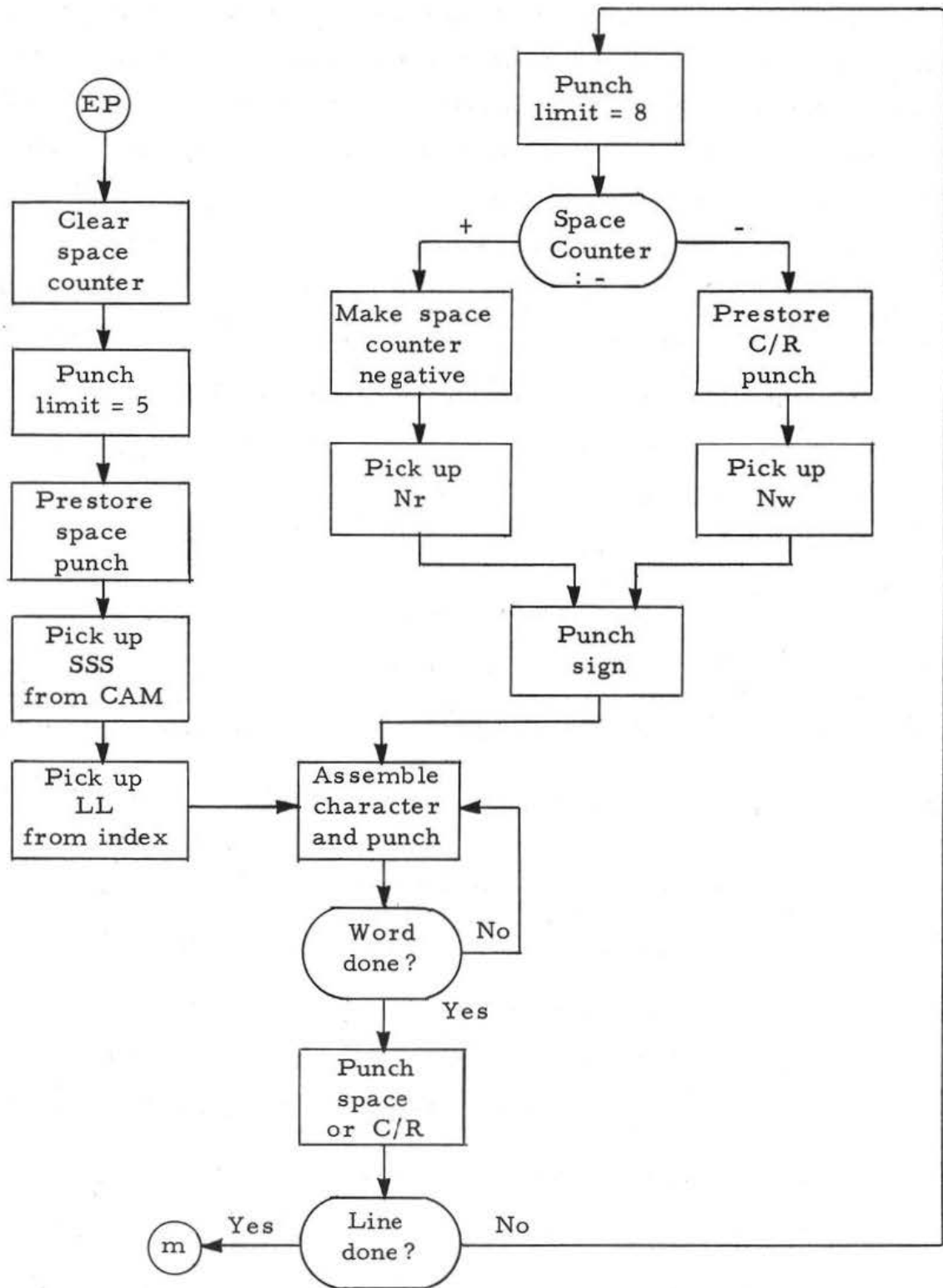


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 8 of 8)

#### D. BOOTSTRAP DIAGNOSTIC ROUTINES

After the particular failure area has been defined by the PROBE I diagnostic routine, it is desirable to use a bootstrap test routine together with an oscilloscope and the applicable logic diagrams to further identify the marginal components. The applicable bootstrap diagnostic routines are described in this paragraph. These routines are given in listable octal format and their bootstrap serial binary format. Tapes supplied with standard technical literature kits are punched in bootstrap binary format, and punched at the end of each tape is an extra filler bit (zero) and a stop code.

To check the commands, it is necessary to enter simple programs, such as those shown on the following pages, in the basic bootstrap format. The steps for entering a program are as follows:

- 1) Insert the tape in the reader.
- 2) Turn computer power on.
- 3) Turn Flexowriter power on.
- 4) Turn FILL switch on the front of computer to the ON position.
- 5) Press ENABLE switch then BREAKPOINT switch to reset the parity flip-flop, then release the BREAKPOINT switch. The computer will now read the tape.
- 6) When the tape stops, turn the FILL switch to off position.
- 7) To start computer operation under computer control, press ENABLE switch on Flexowriter to down position.
- 8) On Flexowriter strike "I" key, then depress BREAKPOINT switch.
- 9) Release BREAKPOINT switch.
- 10) Release ENABLE switch. Computer operation will begin. *at 00001*

A command list showing operations, mnemonic and numeric codes, and descriptions is provided in Table 4-4.

Table 4-4.

## COMMAND LIST OF OPERATIONS AND CODES

Operation	Mnemonic Code	Numeric Code	Description
Arithmetic	ADD	14	Add
	SUB	15	Subtract
	DPA	16	Double Precision Add
	DPS	17	Double Precision Subtract
	SQR	30	Square Root
	DIV	31	Divide
	DVR	31	Divide Remainder
	MUP	32	Multiply
	CLA	45	Clear A
	CLB	43	Clear B
	CLC	44	Clear C
	GTB	41	Gray to Binary
	CAM	56	Compare A and M
Transfer	TAN	35	Transfer if A Negative
	TBN	36	Transfer if B Negative
	TCN	34	Transfer if C Negative
	TRU	37	Transfer Unconditionally
	TOF	75	Transfer on Overflow
	TES	77	Transfer on External Signal
Loading & Storing	LDA	05	Load A
	LDB	06	Load B
	LDC	04	Load C
	LDP	07	Load Double Precision
	IAC	01	Interchange A & C
	IBC	02	Interchange B & C
	ROT	03	Rotate
	IAM	25	Interchange A & M
	STA	11	Store A
	STB	12	Store B
	STC	10	Store C
	STD	13	Store Double Precision
	MCL	71	Move Command Line Block
MLX	26	Move Line X to Line 7	
Logical & Shifting	EBP	40	Extend Bit Pattern
	AMC	42	AND M & C
	MAC	00	Merge A into C
	AOC	46	AND OR Combined
	EXF	47	Extract Field
	NAD	20	Normalize and Decrement
	LSD	21	Left Shift and Decrement
	RSI	22	Right Shift and Increment
	SAI	23	Scale Right and Increment
	SBR	33	Shift B Right
Control	NOP	24	No Operation
	HLT	00	Halt
Input-Output	DIU	50	Disconnect Input Unit
	RTK	51	Read Typewriter Keyboard
	RPT	52	Read Paper Tape
	RFU	53	Read Fast Unit
	LAI	55	Load A From Input Buffer
	CIB	57	Clear Input Buffer
	WOC	6X	Write Output Character
	PTU	70	Pulse to Specified Unit
	BSO	72	Block Serial Output
	BSI	73	Block Serial Input



D-1. LOAD, STORE AND CLEAR REGISTERS

The A, B, and C Registers are successively loaded, stored and cleared. Each is loaded with a different pattern of bits. The A Register is stored in sector 006, the B in 010 and the C in 012.

Location	Instruction	Symbolic Op Code	Remarks
377	000S0501;	LDA	
0	012S4552;	[CLA]	(A) 10000101011001010101010
1	002S0601;	LDB	
2	+6314631		(B) 10110011001100110011001
3	004S0401;	LDC	
4	+3434343		(C) 10011100011100011100011
5	006S1101;	STA	
6	-7777777		
7	010S1201;	STB	
10	+0000000		
11	012S1001;	STC	
12	-7777777		
13	014S4500;	CLA	
14	+0000000		
15	016S4300;	CLB	
16	+0000000		
17	376S4400;	CLC	

### D-2. LOAD AND STORE DOUBLE PRECISION

The A and B Registers are first loaded double precision and then stored.

Location	Instruction	Symbolic Op Code	Remarks
377	+0000000		
0	001S0701;	LDP	
1	-2525252		
2	+6314631		
3	376S1301;	STD	

### D-3. INTERCHANGES

The A, B, and C Registers are loaded and then interchanged, first with a ROT, then with an IAC and IBC. The net result of these is that after one complete memory recirculation, each register should contain its original pattern.

Location	Instruction	Symbolic Op Code	Remarks
377	000S0100;	IAC	(A) 1101010101010101010101 (B) 101100110011001100110011 (C) 100111000111000111000111
0	002S0701;	LDP	
1	005S0200;	IBC	
2	-2525252	CONST	
3	+6314631	CONST	
4	005S0401;	LDC	
5	+3434343	CONST	
6	375S0300;	ROT	

#### D-4. ADD AND SUBTRACT IN SINGLE AND DOUBLE PRECISION

The A and B Registers are first loaded with constants. A constant is added to A. A double precision constant is added to A and B, and another constant subtracted from A and B. Finally, a constant is subtracted from A alone and the cycle repeats.

Location	Instruction	Symbolic Op Code	Remarks
377	+1010102	$D_4$	
0	001S0701;	LDP	$D_0$
1	-5454540	$D_0$	
2	+4646460	$D_0'$	
3	004S1401;	ADD	$D_1$
4	+0202022	$D_1$	
5	006S1601;	DPA	$D_2$
6	-0404042	$D_2$	
7	+1010100	$D_2'$	
10	011S1701;	DPS	$D_3$
11	-1414141	$D_3$	
12	+1414140	$D_3'$	
13	377S1501;	SUB	$D_4$

This chart shows contents of A and B Registers after each of the five operations.

D-4

	S	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
LDP	1	1	0	1	1	0	0	1	0	1	1	0	0	1	0	1	1	0	0	0	0	0	(B) D <sub>0</sub>
	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	0	0	0	(A) D <sub>0</sub> '
ADD	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	D <sub>1</sub>
	1	1	0	1	1	0	0	1	0	1	1	0	0	1	0	1	1	0	0	0	0	0	(B)
DPA	0	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	0	(A)
	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	D <sub>2</sub>
DPS	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	D <sub>2</sub> '
	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	0	(B)
SUB	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	(A)
	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	D <sub>3</sub>
SUB	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	D <sub>3</sub> '
	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	(B)
SUB	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	0	(A)
	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	D <sub>4</sub>
SUB	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	(B)
	0	0	1	1	1	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	0	0	(A)

#### D-5. TRANSFERS

The C Register is loaded with a negative number and the A Register is cleared. A negative constant is added to A and the sign of C tested. Since it is negative, a transfer is made to a TES Breakpoint which, if on, will transfer back to the CLA and start again. If the Breakpoint is off, the overflow is tested, and since it is now off, the negative constant is again added to A. The program cycles in this loop with a TCN (34) command displayed on the console until A overflows and goes positive.

The TOF will cause a transfer to a ROT which moves the negative constant to B and the positive constant to C. The program starts again with the CLA and ADD except that this time the C Register is positive so control passes through the TCN to a TBN (36) which will appear on the console until A overflows.

When A overflows this time, the positive constant from C is rotated to B and the constant from A to C. The CLA and ADD begin again, and now control passes through both the TCN and TBN to a TAN which appears as a 35 on the console. This time, control does not pass through the TES or TOF before adding, so when A overflows and becomes positive, the TAN does not transfer; instead, a TRU carries control back to the start of the routine in sector 000.

## D-5

Location	Instruction	Symbolic Op Code	Remarks
377	000S0300;	ROT	002
0	001S0401;	LDC	-N
1	-2525252	-N	
2	004S4500;	CLA	005
3	002 7735;	TES	B. P. 002
4	377 7501;	TOF	377
5	066S1401;	ADD	
6	-7770000	-77	
7	003 3401;	TCU	003
10	003 3601;	TBN	003
11	005 3501;	TAN	005
12	000S3701;	TRU	000

D-6. LOGICAL COMMANDS

The A Register is loaded with a constant which is modified by an EBP command and then moved to C. From C, part of the pattern is modified and moved to B with an AMC. Additional bits from C are moved to B with an AOC. The result in B is partially cleared with an EXF command and the process begins again in A.

Location	Instruction	Symbolic Op Code	Remarks
377	-6564040	S	
0	001S0501;	LDA	N
1	-0202026	N	
2	003S4001;	EBP	M
3	-1414146	M	
4	005S0100;	IAC	
5	+0000000		
6	007S4201;	AMC	Q
7	+1414147	Q	
10	011S4601;	AOC	R
11	+0706077	R	
12	377S4701;	EXF	S

This chart shows the contents of the A and B Registers after each of the five operations.

D-6

	S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
LDA	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	N
	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	(A)
EBP	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	M
	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	(A)
IAC	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	(C)
AMC	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1	Q
	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	(B)
AOC	0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	R
	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	(B)
EXF	1	1	1	0	1	0	1	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	S
	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	(B)



### D-7. SHIFTING (UNCONDITIONAL)

The A and C Registers are cleared and B is loaded with a pattern of bits. If the Breakpoint is up, a left shift and decrement is executed for two sectors and the sign of B tested. The B Register will be negative so control goes back to the TES Breakpoint and another shift is executed. This continues until B is positive, and then a right shift and increment moves the pattern two bit positions into B. This should make B negative, so control will go back to the right shift until a zero is shifted into the sign of B. When B is positive, control goes back to the left shift. If the Breakpoint is down the shifts will be without incrementing or decrementing C and will only execute for one sector.

Location	Instruction	Symbolic Op Code	Remarks
377	004S0601;	LDB	-B 005
0	010S4500;	CLA	011
1	003 7735;	TES	B. P.
2	005S2100;	LSD	2
3	005S2110;	LSO	1
4	-7355143	-B	-B
5	001 3601;	TBN	
6	010 7735;	TES	B. P.
7	012S2200;	RSI	2
10	012S2210;	RSO	1
11	376S4400;	CLC	377
12	006 3601;	TBN	
13	001S3701;	TRU	001 0

#### D-8 SHIFTING (CONDITIONAL)

This routine operates similar to D-7 in that it shifts back and forth from A and B. First, a negative number is loaded into B, and A and C are cleared. A normalize and decrement of three is executed and the sign of B tested, if negative, another NAD is executed. Going in steps of three, it will take seven full shifts plus a one-bit shift to normalize the number. In this way, both the normal shifting feature plus the conditional terminating feature of the NAD are tested. The B Register should be positive when the number is normalized.

During normalization, the C Register will have been decremented to the negative of the number of normalizing shifts required. It should be possible by now, executing scale right and increment commands in steps of three, to move the number back to its original condition with A and C equal to zero.

When C is scaled to zero, control will go back to the NAD loop. If the BREAKPOINT is pressed, computation will hang up in a TES loop after either normalizing or scaling.

## D-8

Location	Instruction	Symbolic Op Code	Remarks
377	003S2000;	NAD	003
0	000S4500;	CLA	001
1	011S0601;	LDB	-N 012
2	006S2300;	→SRI	006
3	377 3601;	TBN	377
4	004 7735;	TES	B. P. 004
5	022S3701;	TRU	
6	002 3601;	←TBN	
7	007 7735;	TES	B. P. 007
10	377S3701;	TRU	377
11	-7153514	-N	-N
12	376S4400;	CLC	377

D-9. CAM AND GTB

A number is loaded in A and compared with itself. If overflow occurs, the number is converted from Gray code to binary and compared to the correct result. If overflow occurs, control goes to a Breakpoint test. If Breakpoint is up, the routine starts again; if Breakpoint is down, the binary number is compared with the original number and overflow should not occur.

When comparing the converted number with the correct result, if overflow does not occur the sign of A is tested, and if negative, a transfer is made to 000 with a TAN (35). if not negative, the transfer will be a TBN (36).

Location	Instruction	Symbolic Op Code	Remarks
377	002 7735;	TES	B. P. 002
0	001S0501;	LDA	N <sub>G</sub>
1	+5252525	N <sub>G</sub>	N <sub>G</sub>
2	003S5601;	CAM	N <sub>G</sub>
3	+5252525	N <sub>G</sub>	N <sub>G</sub>
4	006 7501;	TOF	002
5	002S3701;	TRU	
6	007S4100;	GTB	
7	+0000000		
10	011S5601;	CAM	N <sub>B</sub>
11	-1463146	N <sub>B</sub>	N <sub>B</sub>
12	377 7501;	TOF	377
13	000 3501;	TAN	000
14	000S3601;	TBN	000 S

D-10. TO TEST INDEX REGISTER, HLT, MAC, AND NOP

The A and C Registers are cleared and A stored in the Index Register. A and C are OR gated into C and computation halts, displaying the contents of the Index Register in the OPERAND lights. When parity is cleared, a NOP is executed and the contents of the Index Register picked up, incremented by one and restored. Then another MAC and halt are executed.

This process continues each time the parity is cleared. The Ar will show a count, and the Cr a buildup from the right.

Location	Instruction	Symbolic Op Code	Remarks
377	000S1401;	ADD	001
<i>start</i> 0	001S4540;	CLA	002 (00000011 00 010000010)
1	002S1137;	STA	I. R. 003
2	000S4400I	CLC	001
3	004S0000I	MAC	005
4	006S2400I	NOP	006
5	004S0000I	HLT	004
6	376S0537;	LDA	I. R. 377

*Index register*

D-11. MOVE LINE AND IAM

The Index Register is cleared to zero and line 01 is moved to 00. Then the Index Register is incremented by one and another MCL is executed. This continues through line 36, and then the MCL is changed to a MLX by means of an IAM. Using the Index Register, each line from 00 through 36 is moved to line 07 and the routine then repeats.

If the Breakpoint is down, the program halts after each move and displays the line moved.

Location	Instruction	Symbolic Op Code	Remarks
377	000S0100;	IAC	
000	002S0501;	LDA	X
1	004S1401;	ADD	N
2	010S7100I	X	(MCL) I
3	005S4400;	CLC	
4	+0200002	N	N +.020 0002
5	006S0100;	IAC	
6	010S2501;	IAM	
7	010S2600I	MLX	I
010	003 7501;	TOF	
1	013 7735;	TES	35
2	376S1037;	STC	37 377
3	012S0000I	HLT	

## D-12. MULTIPLY, DIVIDE AND SQUARE ROOT

This routine executes in line 00, therefore it is not possible to single step and always obtain the correct answer. However, all pertinent operations occur in the first  $073)_8$  sector times.

The same number is loaded into the B and C Registers and garbage into A. A multiply for 22-word times is executed, and the result in A compared to the correct result. The overflow is not tested, but it may be observed on the console. After the multiply, if the Breakpoint is up, a divide for 22-word times is executed and the remainder in A compared with +0000000. If the Breakpoint is down, a square root for 21-word times is executed and the remainder in A compared to +0000000. When executing the divide, the comparison is true and the overflow occurs. The square root has a remainder of  $-7777777)_8$  and will not compare.

By observing sector time  $073)_8$ , the results of both the divide and square root may be seen.

Location	Instruction	Symbolic Op Code	Remarks
377	+5252525	$X_B$	$X_B$
0	014S7100;	$X_A$	MCL
1	030S3200;	MUL	S = 22 030
2	+3434343	$Y_1$	$Y_1$
3	045 7735;	TES	B. P. 045
4	073S3100;	DIV	S = 22 073 R: (A) = +0000000
5	073S3000;	SQR	S = 21 073 R: (A) = -7777777
6	+0000000	$Y_2$	$Y_2$
7	111S0400;	LDC	$X_C$
010	042S5600;	CAM	$Y_1$ 043
1	+5252525	$X_C$	$X_C$
2	377S0701;	LDP	$X_{A \& B}$ 001
3	106S5600;	CAM	$Y_2$ 107
4	107S7500;	TOF	

D-13. RTK, RPT, LAI, WOC AND CIB

After pressing the "I" key and raising the ENABLE switch, the Flexowriter light will come on and a character may be typed. This character will be loaded into the A Register, added to a WOC, and the WOC used to display it on the console for about two seconds. After the WOC, a HLT with a line number of 13)<sub>8</sub> will occur.

When parity is cleared, another character may be entered. The character will come from the tape reader if the Breakpoint is down, and from the keyboard if the Breakpoint is up.

Location	Instruction	Symbolic Op Code	Remarks
377	010 0013;	D	HLT
000	000S4500;	CLA	
1	001S5700;	CIB	
2	004 7735;	TES	B. P.
3	006S5100;	RTK	
4	006S5200;	RPT	
5	+0000377	M	M
6	010 7736;	TES	36
7	005S5501;	LAI	M
010	010S4300;	CLB	
1	014 2110;	LSO	2
2	013S1401;	ADD	
3	377S6000;	WOC	0 377
4	377 0401;	LDC	D
5	016 1101;	STA	\$ + 1



D-14. FLEXOWRITER TYPING AND PUNCHING.

Both lines 05 and 06 must be present for this test. Every possible character from 000 through 377)<sub>8</sub> will be typed, then punched. Some of these are not valid keyboard characters and will not print, but all should be punched.

Location	Instruction	Symbolic Op Code	Remarks
377	001S3706;	TRU	06
0	017S7106;	MCL	→ 06 017 move 00101 → 01601 to 00106 - 01606 next command 01701
1	002S0406;	LDC	D <sub>2</sub>
2	+0002424	D <sub>2</sub>	D <sub>2</sub>
3	000 6000;	WOC	000
4	005S1406;	ADD	C
5	+0000004	C	C
6	007S5606;	CAM	E
7	000 7000;	E	E
010	000 7501;	TOF	I
1	003 1106;	STA	06
2	376 1105;	STA	05
3	014S0406;	LDC	D <sub>1</sub>
4	+0003232	D <sub>1</sub>	D <sub>1</sub>
5	015 7737;	TES	37
6	376S3705;	TRU	05 376
7	003 0501;	LDA	WOC 0
020	012S7105	MCL	→ 05 012 chm 01101 → line 5 gr to 01201

DIU

D-15. DIV, RFU AND RfTf TEST

A DIV is given, followed by a TES  $36)_8$  which could be true. Then an RFU and a TES  $36)_8$  which should now be false. If the TES  $36)_8$  is false, after the DIV, a halt will occur with 50-37 displayed. This means that the RFU did not set either Rf or Tf. When the program runs correctly, a 53-00 is displayed.

Location	Instruction	Symbolic Op Code	Remarks
377	001 7736;	TES	
000	001S5000;	DIU	
1	376S5336;	RFU	
2	004 7736;	TES	
3	001S5036;	DIU	
4	376S5300;	RFU	

D-16. PTU

Two PTU's are executed, each for approximately 3 ms. One has a line number of  $37)_8$ , the other 00.

Location	Instruction	Symbolic Op Code	Remarks
377	000S7037;	PTU	37
0	377S7000;	PTU	0

#### D-17. BSO, BSI

After pressing the "I" key, a BSO from line 01 is executed for 3 ms, and as long as the Breakpoint is up, Block Serial Inputs will continue. If the Breakpoint is down, after the first BSO, then BSI's will be executed until it is raised.

Location	Instruction	Symbolic Op Code	Remarks
377	001 7735;	TES	35
0	377S7201;	BSO	
1	377S7301;	BSI	

#### D-18. FLEXOWRITER FORMAT

If the tapes which are punched in bootstrap binary format are reproduced on a Flexowriter they will appear in serial binary Flexowriter format as shown in Figure 4-2. The type-outs D-1 through D-17 relate directly to paragraphs D-1 through D-17. In this format, H = binary one and 0 = binary zero.



## E. TROUBLESHOOTING

A general guide to the troubleshooting sequence for the PB250 Computer is provided in Figure 4-3. Further information regarding the numbered blocks, is given in the following paragraphs.

### E-1. VOLTAGES (BLOCK ①)

Proceed as follows:

- a) Turn on power supply and check meter for NOMINAL voltage reading.
- b) Using a voltmeter take voltage readings on the power busses. If the readings are within 5%, no adjustments should be made. The indicator lamps on the front panel should be lit. If the readings are in excess of 5%, reference must be made to the PS-7G Power Supply Technical Manual, PBC 3006, or the PS-8 Power Supply Technical Manual, PBC 1013, before making adjustments.

### E-2. SA-100 (BLOCK ②)

This is an optional module card which is not used in all PB250 Computers. Paragraph H contains full details of this module.

### E-3. CLOCK DISTRIBUTION (BLOCK ③)

For pin connections refer to the applicable logic diagram in Section VI and use a Tektronix Type 545A Oscilloscope with 53C and CA Plug-In Units for all waveform analyses. Refer to Figure 4-4A and proceed as follows:

- a) Check the waveform on the CD-100 and one output of the GD-100 module for distributing the general computer clock.

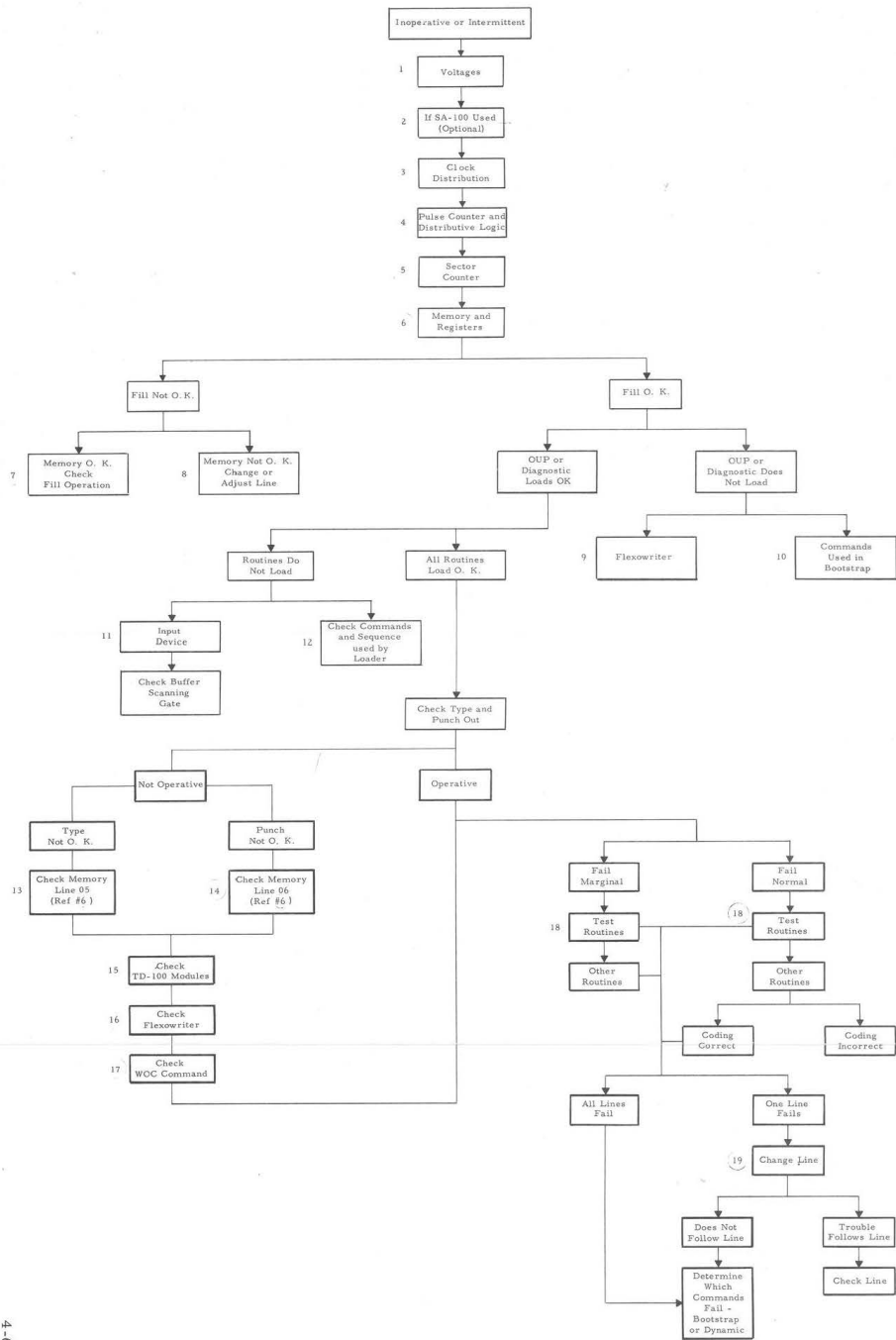


Figure 4-3. Troubleshooting Sequence Block Diagram

- b) Check the waveform on the three outputs of the GD-100 module for the distribution of the memory clock.
- c) Watch for overloaded outputs.

NOTE

There are two marginal test switches on the front of the computer which are used for changing the width of the computer clock and the memory clock. When the TEST 1 switch is in the ON position, it lengthens the memory clock from  $0.155\mu\text{sec} \pm 10\%$  to  $0.170\mu\text{sec} \pm 10\%$ . See Figure 4-4B.

When the TEST 2 switch is in the ON position, it shortens the computer clock width from  $0.27\mu\text{sec} \pm 5\%$  to  $0.24\mu\text{sec} \pm 10\%$ , and shortens the memory clock from  $0.155\mu\text{sec} \pm 10\%$  to  $0.140\mu\text{sec} \pm 10\%$ . See Figure 4-4C.

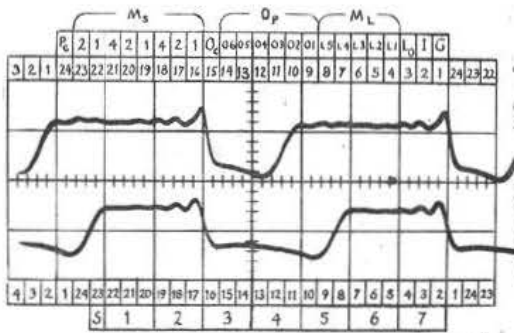
E-4. PULSE COUNTER AND DISTRIBUTIVE LOGIC (BLOCK ④)

Proceed as follows:

- a) Check the operation of the pulse counter by following the procedures shown below Figure 4-4, waveforms D through H.
- b) Check the output signals of the following pulses and their time relationship to the pulse counter as follows:

$P1, \overline{P1}, P2, \overline{P2}, P3, \overline{P3}, P23, \overline{P23}, P24, \overline{P24}$   
(P8-P15), (P16-P23) and (P24-P7)

COMMAND FORMAT

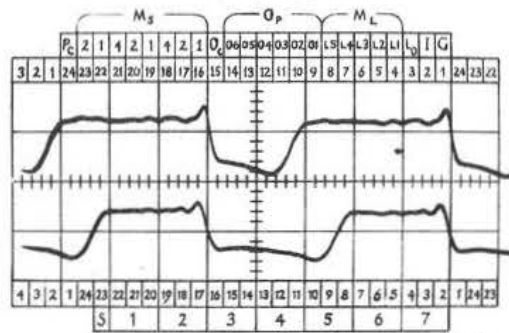


DATA FORMAT

Oscilloscope Settings:  
 SWEEP A  
 TIME/CM 0.1  $\mu$  sec  
 TRIGGER P24  
 VOLTS/CM 10 volts  
 CHANNEL A Trace Memory Clock. 25B24  
 CHANNEL B Trace Computer Clock. 25B14

Computer Front Panel Settings:  
 TEST switch 1 off  
 TEST switch 2 off

COMMAND FORMAT

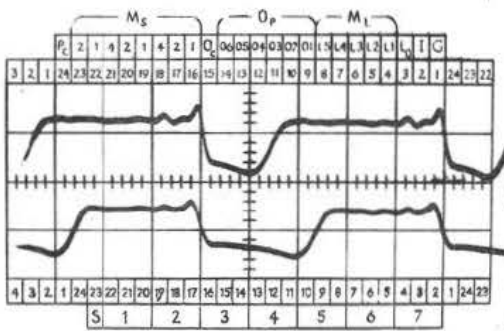


DATA FORMAT

Oscilloscope Settings:  
 SWEEP A  
 TIME/CM 0.1  $\mu$  sec  
 TRIGGER P24  
 VOLTS/CM 10 volts  
 CHANNEL A Trace Memory Clock. 25B24  
 CHANNEL B Trace Computer Clock. 25B14

Computer Front Panel Settings:  
 TEST switch 1 ON  
 TEST switch 2 off

COMMAND FORMAT

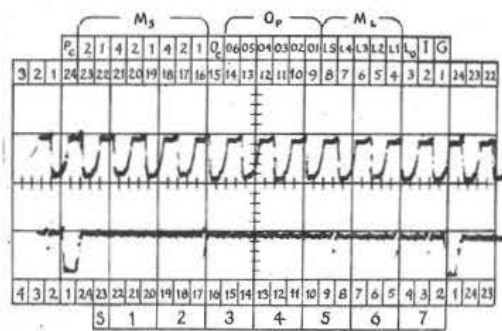


DATA FORMAT

Oscilloscope Settings:  
 SWEEP A  
 TIME/CM 0.1  $\mu$  sec  
 TRIGGER P24  
 VOLTS/CM 10 volts  
 CHANNEL A Trace Memory Clock. 25B24  
 CHANNEL B Trace Computer Clock. 25B14

Computer Front Panel Settings:  
 TEST switch 1 off  
 TEST switch 2 ON

COMMAND FORMAT



DATA FORMAT

Oscilloscope Settings:  
 SWEEP A  
 TIME/CM  $\approx 0.1 \mu$  sec  
 TRIGGER P24  
 VOLTS/CM 10 volts  
 CHANNEL A Trace F1, 2A14  
 CHANNEL B Trace P24, 3E4

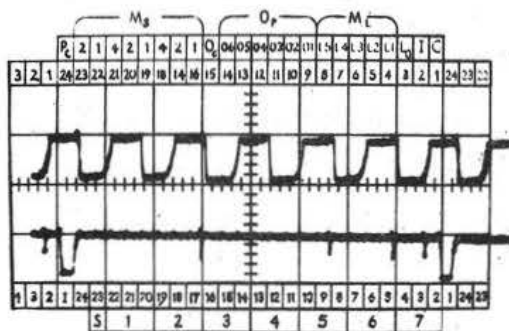
Computer Front Panel Settings:  
 TEST switch 1 off  
 TEST switch 2 off

\* Calibrated to one word time.

Figure 4-4. Clocks and Pulse Counter Waveforms (Sheet 1 of 2)



COMMAND FORMAT



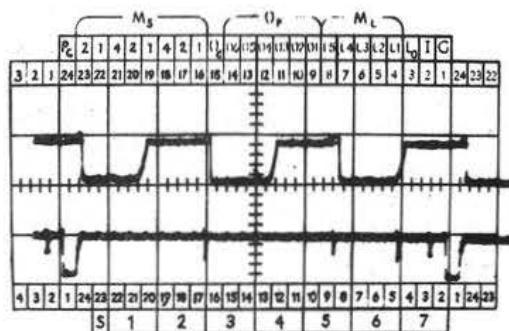
DATA FORMAT

Oscilloscope Settings:  
 SWEEP A  
 TIME/CM \*0.1μ sec  
 TRIGGER P24  
 VOLTS/CM 10 volts  
 CHANNEL A Trace F2, 2A22  
 CHANNEL B Trace P24, 3E4

Computer Front Panel Settings:  
 TEST switch 1 off  
 TEST switch 2 off

\* Calibrated to one word time.

COMMAND FORMAT



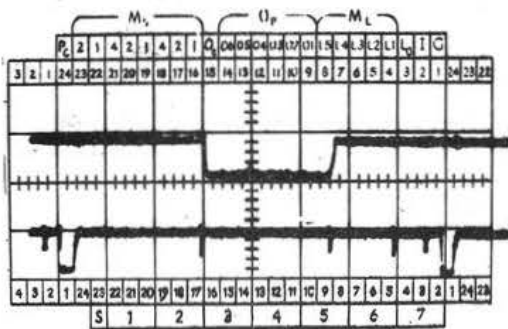
DATA FORMAT

Oscilloscope Settings:  
 SWEEP A  
 TIME/CM \*0.1μ sec  
 TRIGGER P24  
 VOLTS/CM 10 volts  
 CHANNEL A Trace F3, 3A14  
 CHANNEL B Trace P24, 3E4

Computer Front Panel Settings:  
 TEST switch 1 off  
 TEST switch 2 off

\* Calibrated to one word time.

COMMAND FORMAT



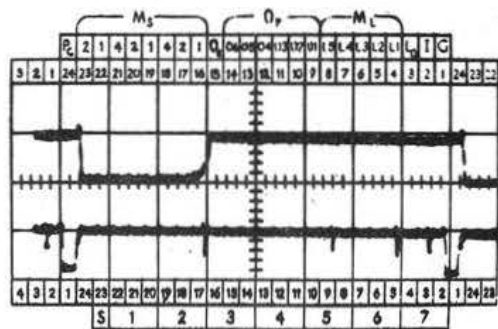
DATA FORMAT

Oscilloscope Settings:  
 SWEEP A  
 TIME/CM \*0.1μ sec  
 TRIGGER P24  
 VOLTS/CM 10 volts  
 CHANNEL A Trace F4, 3A22  
 CHANNEL B Trace P24, 3E4

Computer Front Panel Settings:  
 TEST switch 1 off  
 TEST switch 2 off

\* Calibrated to one word time.

COMMAND FORMAT



DATA FORMAT

Oscilloscope Settings:  
 SWEEP A  
 TIME/CM \*0.1μ sec  
 TRIGGER P24  
 VOLTS/CM 10 volts  
 CHANNEL A Trace F5, 5A14  
 CHANNEL B Trace P24, 3E4

Computer Front Panel Settings:  
 TEST switch 1 off  
 TEST switch 2 off

\* Calibrated to one word time.

Figure 4-4. Clocks and Pulse Counter Waveforms (Sheet 2 of 2)

Sc = sector counter  
Cs = c register?  
Qg = sector counter clear term

#### E-5. CHECKING sSc GATE (BLOCK ⑤)

Without the sector counter plugged in, check the waveform of sSc. It should be true during P7 and P15. Replace the sector counter and check its counting ability by observing the Sr output and triggering the oscilloscope from the Cs gate. The Cs gate outputs should be 3.072 milliseconds apart. After satisfactory locking on one machine cycle, expand the waveform and check the counting, sector by sector.

#### E-6. MEMORY AND REGISTERS (BLOCK ⑥)

Full details of changing or adjusting delay lines are given in paragraph F, below.

#### E-7. MEMORY OK, CHECK FILL OPERATION (BLOCK ⑦)

Proceed as follows:

- a) Turn the FILL switch (Figure 1-2) to ON position and check that  $\textcircled{Fi}$  blocks computation by locking the machine in Phase I ( $\overline{Ec}\overline{Rc}$ ).
- b) Check the sector counter to see if  $\textcircled{Fi}$  is synchronizing via Qg, the two sector numbers P23 + P16.
- c) Check the 06 flip-flop. It should be on for (P16-P23) once per machine cycle. 5C14

#### E-8. MEMORY NOT OK (BLOCK ⑧)

Change or adjust delay line. Refer to paragraph F, below, for details on changing or adjusting magnetostrictive delay lines.

#### E-9. FLEXOWRITER (BLOCK ⑨)

For complete details of the Flexowriter, refer to the Flexowriter Technical Manual, PBC 1016.

E-10. COMMANDS USED IN BOOTSTRAP (BLOCK 10)

Use the individual bootstrap diagnostic routines described in paragraph D, above. These routines may be correlated using the oscilloscope and the particular logic diagram provided in Section VI.

E-11. INPUT DEVICE (BLOCK 11)

Refer to the applicable technical manuals for the Flexowriter, PBC 1016, High-Speed Reader, PBC 1010, Magnetic Tape Unit, PBC 1014, or the High-Speed Buffer Register, PBC 1007.

E-12. CHECK COMMANDS AND SEQUENCE USED BY LOADER (BLOCK 12)

If the input devices have been ascertained as operative, use the individual bootstrap diagnostic routines described in paragraph D, above.

E-12. CHECK MEMORY LINE 05 (BLOCK 13)

Change or adjust memory line 05. Refer to paragraph F, below, for details on changing or adjusting magnetostrictive delay lines.

E-14. CHECK MEMORY LINE 06 (BLOCK 14)

Change or adjust memory line 06. Refer to paragraph F, below, for details on changing or adjusting magnetostrictive delay lines.

E-15. CHECK TD-100 MODULES (BLOCK 15)

These modules are the output cards used to operate the Flexowriter. Refer to Table 6-1 for the locations of TD-100 module cards and the applicable logic diagram for test points.

E-16. CHECK FLEXOWRITER (BLOCK ①⑥)

For complete details of the Flexowriter, refer to the Flexowriter Technical Manual, PBC 1016.

E-17. CHECK WOC COMMAND (BLOCK ①⑦)

To check this command, refer to the bootstrap diagnostic routine described in paragraph IV D; above.

E-18. TEST ROUTINE (BLOCK ①⑧)

Refer to the individual bootstrap diagnostic routines in paragraph IV D above, and eliminate the marginal components.

E-19. CHANGE LINE (BLOCK ①⑨)

Change or adjust delay line. Refer to paragraph F, below for details on changing or adjusting magnetostrictive delay lines.

## F. ADJUSTMENT OF MAGNETOSTRICTIVE DELAY LINES

The magnetostrictive delay lines are pre-adjusted at the manufacturer's facility and will not normally require adjustment in the field. However, should adjustment appear necessary, it is advisable to contact the Packard Bell Computer representative. The basic procedure for setting amplifier gain, dc level, and magnetostrictive delay time, is as follows.

### F-1. READ AMPLIFIER, DC LEVEL ADJUSTMENT

- a) Temporarily connect test point TP 2 to ground, to clear the memory lines.
- b) Calibrate the gain on the plug-in vertical amplifier of the oscilloscope.
- c) The dc level present at test point TP 1 should be -1.3 volts.
- d) For means of adjustment, refer to Figure 4-5.

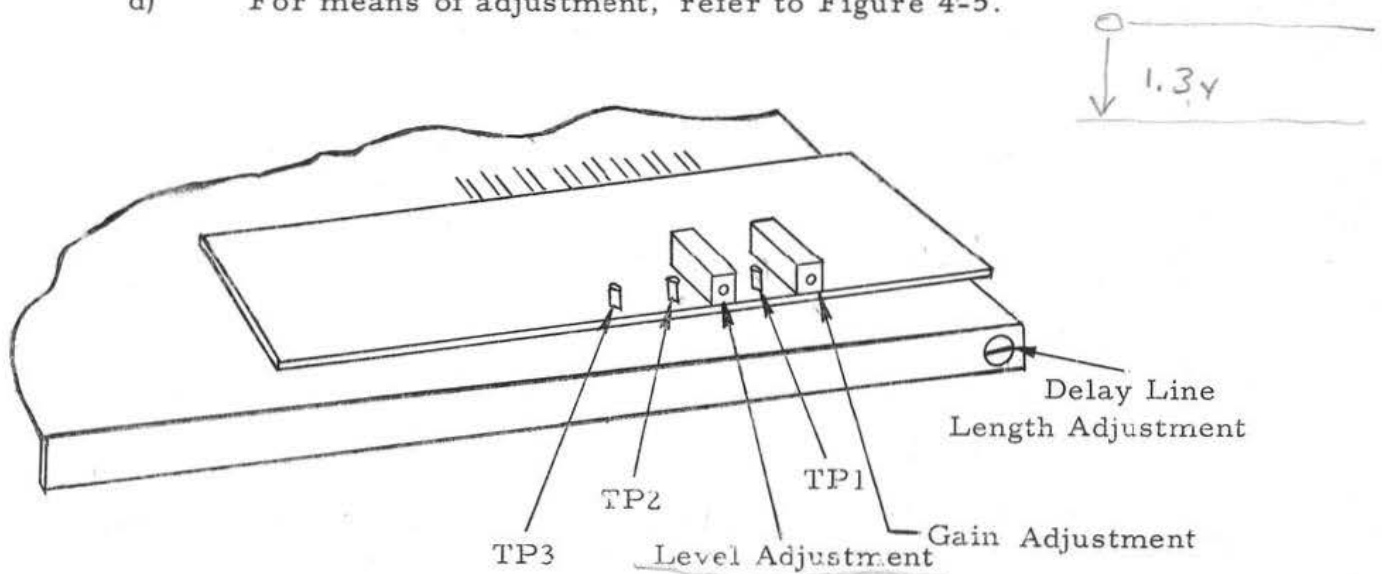


Figure 4-5. Adjustment of Read Amplifier

F-2. READ AMPLIFIER, GAIN ADJUSTMENT

- a) Fill the line with information by temporarily connecting test point TP 2 to the output of the pulse counter (pin number 3E6, (F-5) Figure 4-8).
- b) The displayed information at test point TP 1 should be as shown in Figure 4-6. The information signal should be at an amplitude of 2.4 volts. For means of adjustment, refer to Figure 4-5.

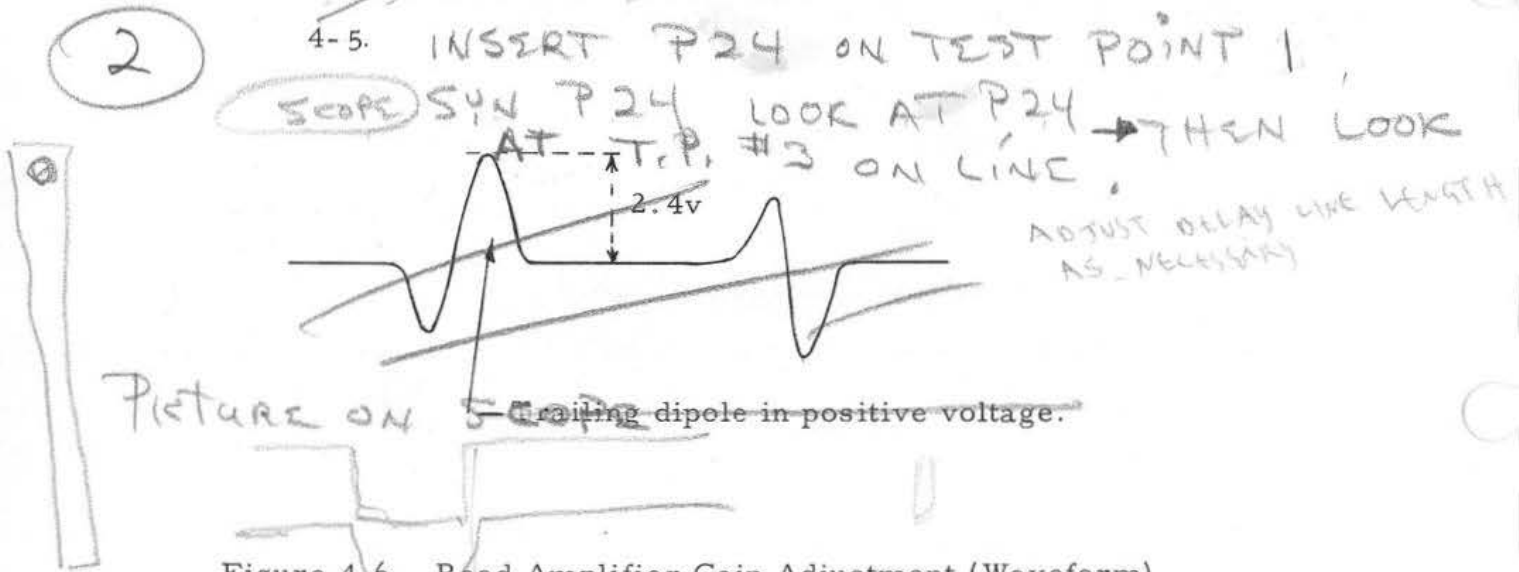


Figure 4-6. Read Amplifier Gain Adjustment (Waveform)

F-3. DELAY LINE LENGTH ADJUSTMENT

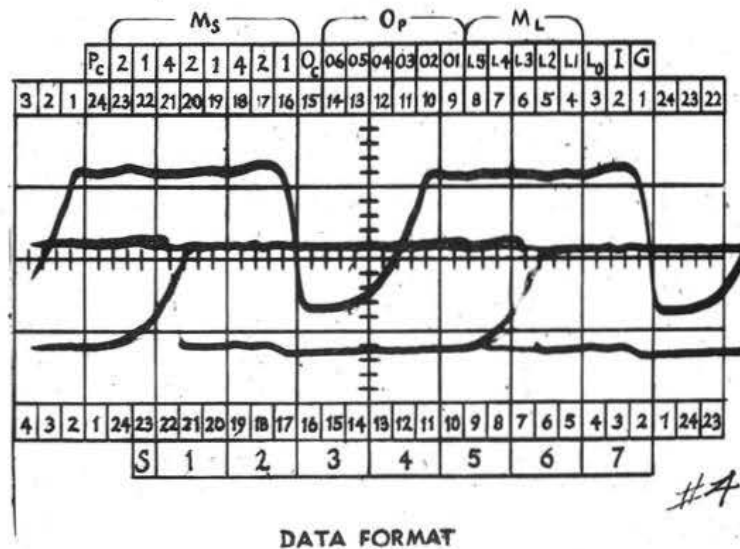
- a) Fill the line with information by temporarily connecting test point TP 2 to the output of the sector counter (pin number 3E1, (5r) Figure 4-8).
- b) Use a dual trace oscilloscope input with alternate sweep and trigger. Trigger the sweep from the computer clock.
- c) With channel B of the vertical amplifier of the oscilloscope, observe the memory clock signal.

P24

TP3 - MSR - 1 MHz

- d) With channel A of the vertical amplifier of the oscilloscope, observe test point TP 2 or TP 3 of the subject magnetostrictive delay line. The display should be shown in Figure 4-7.
- e) Adjust the length of the delay line by moving the center of the spread in trigger transition time so that it locates in the center of the positive period of the memory clock. For means of adjustment, refer to Figure 4-5.

### COMMAND FORMAT



#### Oscilloscope Settings:

SWEEP	A
TIME/CM	0.1 $\mu$ sec
TRIGGER	P24 (3E4)
VOLTS/CM	5 volts
CHANNEL A Trace	Memory Clock. 19E6
CHANNEL B Trace	TP3-MSR-1 Module.

#### Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	off

Figure 4-7. Delay Line Adjustment

G. TEST POINT FUNCTIONS

Mounted on the left side of the PB250 Computer is a panel of fourteen test points (Figure 4-8) located in row "E", connector numbers two and three. The function of these test points is to make readily available certain terms for programming, maintenance, and troubleshooting analysis with an oscilloscope. These terms are shown in Table 4-5.

Table 4-5 (Sheet 1 of 3)

TEST POINT FUNCTIONS

Location	Term	Description
2E1	Ar	The A Register read flip-flop. This point will display the contents of the A Register.
2E2	Br	The B Register read flip-flop. This point will display the contents of the B Register.
2E3	Ir	The Instruction Register read flip-flop. This point will display the contents of the Instruction Register, which includes the Index Register, the sector of the next command, and the sector address.

*See Fig 2-10, A.2-19, v.11*



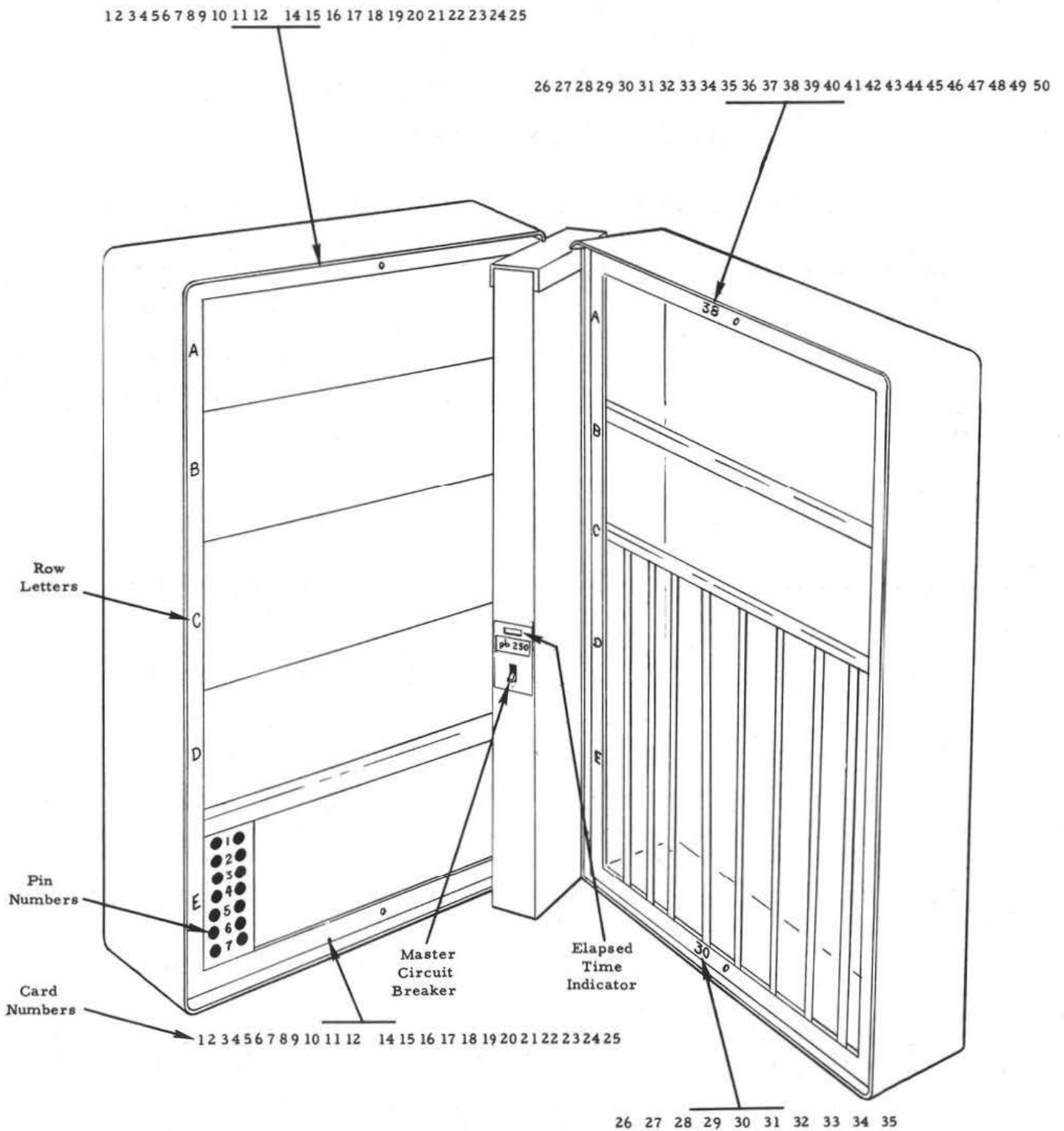


Figure 4-8. Test Points

Table 4-5. (Sheet 2 of 3 )

TEST POINT FUNCTIONS

Location	Term	Description
2E4	Vg	The command gate. This point will display the contents of the line from which the computer is receiving its instructions.
2E5		Blank test point.
2E6	Cs	The cycle trigger. This pulse occurs once every machine cycle (approximately three msec) and is used for sync output to the oscilloscope. Pulse begins sweep at sector 000 during memory cycle.
2E7	GND	This point is computer ground.
3E1	Sr	The sector counter read flip-flop. This point will display the counting of the sector counter and also the input buffer.

Table 4-5. (Sheet 3 of 3)

TEST POINT FUNCTIONS

Location	Term	Description
3E2	Cr	The C Register read flip-flop. This point will display the contents of the C Register.
3E3	Fg	The "Fetch" gate. This point displays the data coming from the memory.
3E4	P24	The twenty-fourth pulse of the word counter. This is used to reference the display of a word on the oscilloscope.
3E5		Blank test point.
3E6	F5	The output of F5 is used to provide output for sync of the oscilloscope. F5 occurs during time P16 through P23.
3E7	GND	This point is computer ground.

## G-1. USE OF OSCILLOSCOPE

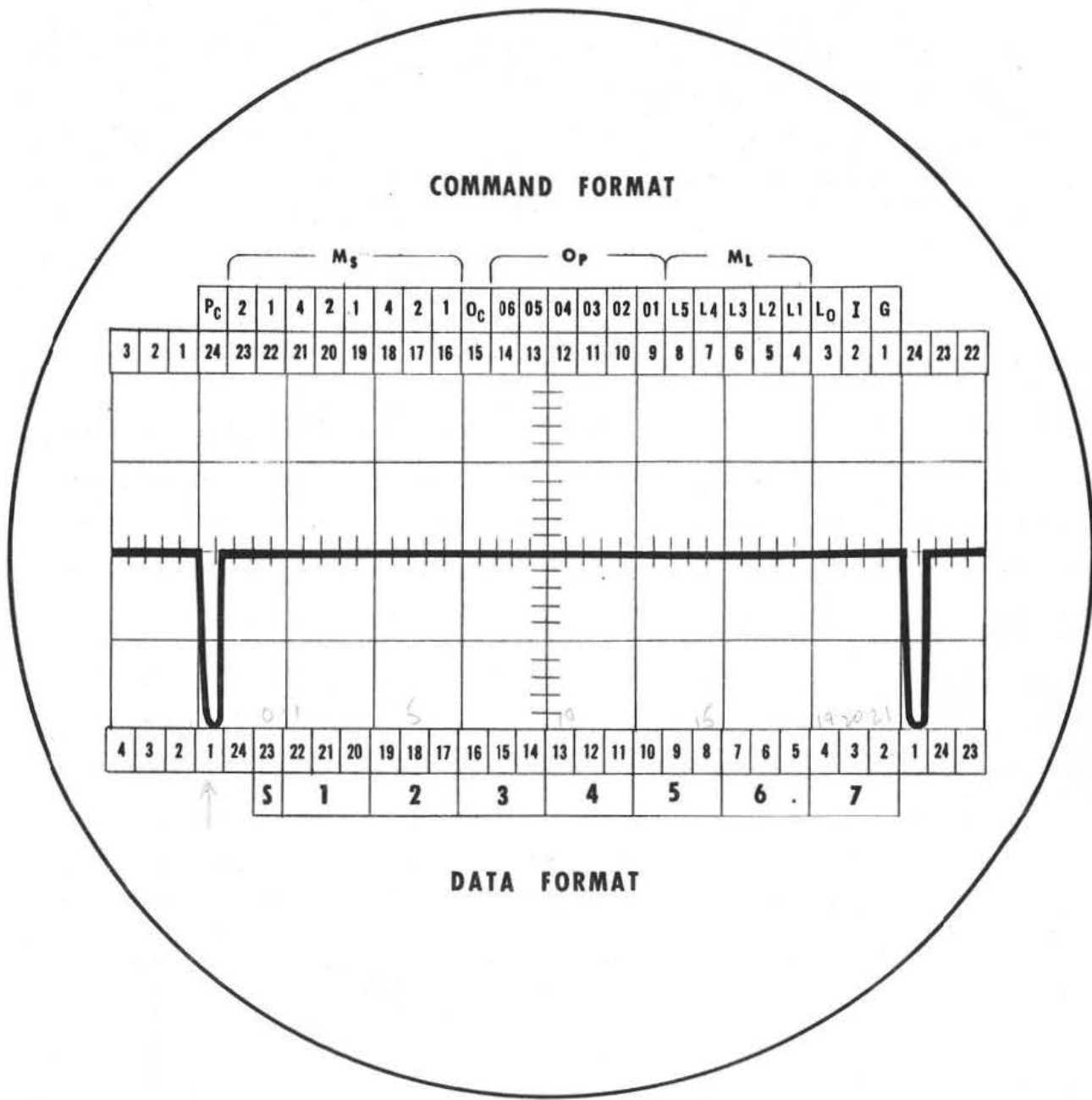
The recommended oscilloscope is a Tektronix Type 545A with delay sweep. The required preamplifier is a Type CA plug-in unit for the dual channels. Refer to the applicable manufacturer's manual for details of operation of oscilloscope and preamplifier.

Calibrate the preamplifier and adjust the test probes. Ground the oscilloscope to the computer by means of a lead from the oscilloscope connected to the computer ground (2E7 or 3E7, Figure 4-8). Connect the sync from cycle trigger (2E6) to the oscilloscope sync input A or B.

Use the following procedure for preliminary adjustment. After the computer has been turned on (see paragraph III B, page 3-1, attach the oscilloscope probes to P24 (3E4). By adjusting the calibration knob of the TIME/CM control, position P24 to occur where indicated on the format pattern, on the oscilloscope screen (see Figure 4-9). If there is no format pattern, remove probe from P24 (3E4) and hook it to F1 (1A35) and calibrate until there are three bits per cm or grid line. This will establish a one-word reference on the oscilloscope. Figure 4-9 shows the P reticle format with a modified P24 pulse waveform added. The reticle is an optional item and may be purchased from Packard Bell Computer, Los Angeles, California.

## G-2. A, B, AND C REGISTERS

The A, B and C Registers may be observed for analyzing programs and may be used in isolating possible malfunctions in the equipment. By using one oscilloscope probe on P24 and synchronizing on single cycle, it is possible by means of the delay sweep of the oscilloscope, to view the contents of the A, B, or C Register during a machine cycle. The operation of the computer may be single cycled by having the Flexowriter ENABLE switch (see Flexowriter Technical Manual, PBC 1016) down, and pressing the C key once for each machine command. This allows the operator to analyze the contents



### DATA FORMAT

Figure 4-9. Oscilloscope Format

of the registers, as each cycle represents the reading and execution of one command.

By changing the sync input to different terms, the operation may be viewed during a particular command. Selection of a sync pulse ensures that the display of the registers viewed on the oscilloscope is occurring during the subject operation. For instance, a division may be viewed closely by synchronizing on the divide gate.

#### H. SA-100 SINEWAVE AMPLIFIER

The SA-100 sinewave amplifier module shown in Figure 4-10, is a tuned class C amplifier used for synchronization of a PB250 Computer system consisting of one or more computers and their peripheral equipment. Figure 4-11 shows an example of a distribution system from an SA-100 module to a PB250 Computer system consisting of three computers (one master and two slaves) each with a Memory Unit and two High-Speed Buffers.

The SA-100 accepts the two megacycle sinewave generated by the oscillator section of an XCG-101 module, amplifiers and distributes it to the various units which comprise a PB250 system. The output of the SA-100 is processed in each unit by the shaper section of the XCG-101 module to produce computer and memory clock signals. Distribution of the SA-100 output is established to allow synchronization of the clock signals within 0.01 microsecond between the computer system units. Specifications of the SA-100 are given in Table 4-6.

Standard 35-pin module.  
All other pins have no connections.

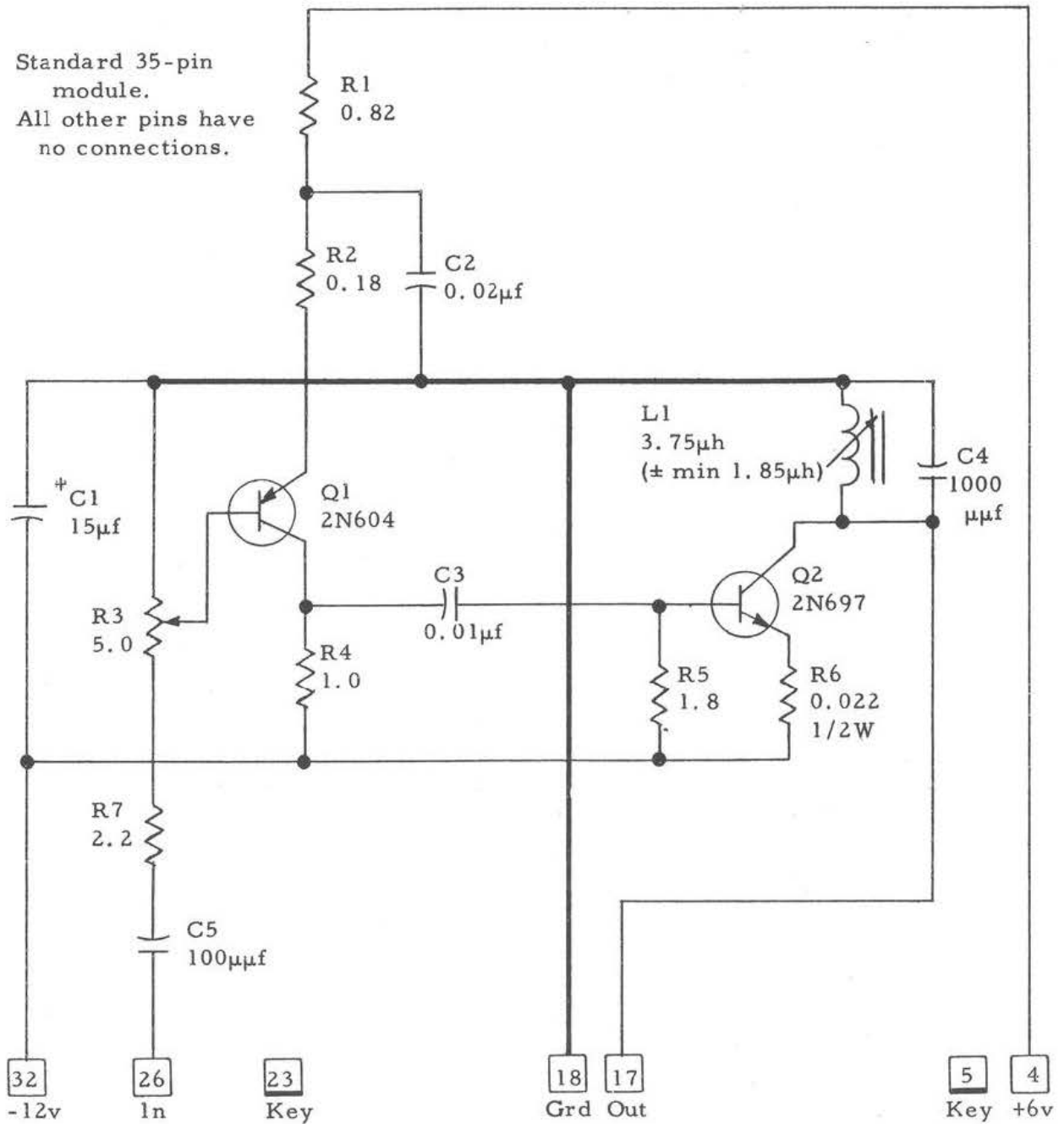


Figure 4-10. SA-100 Sinewave Amplifier schematic

Applicable cabling details are as follows:

- a) All connections are made with Microdot 95-3920 coaxial cable ( $Z_o = 95$  ohms, capacitance per foot =  $13\mu\text{mf}$ ).
- b) Total cable length in distribution system is a maximum of 110 ft.
- c) Cable length from the SA-100 to any load point is a maximum of 24 ft.

## H-2. FINAL ADJUSTMENT

After the clock system is installed and turned on, the SA-100 is first tuned for maximum output by means of variable inductor L1 (see Figure 4-12). The output amplitude is then set to 12 volts peak-to-peak by means of potentiometer R3 (see Figure 4-12).

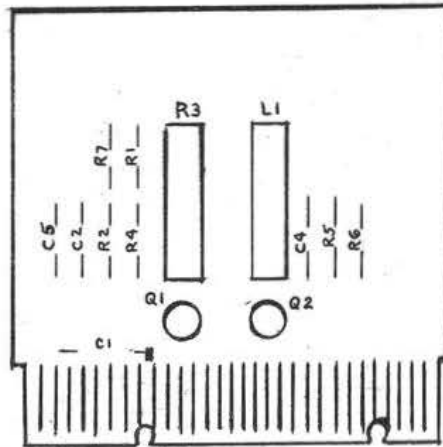
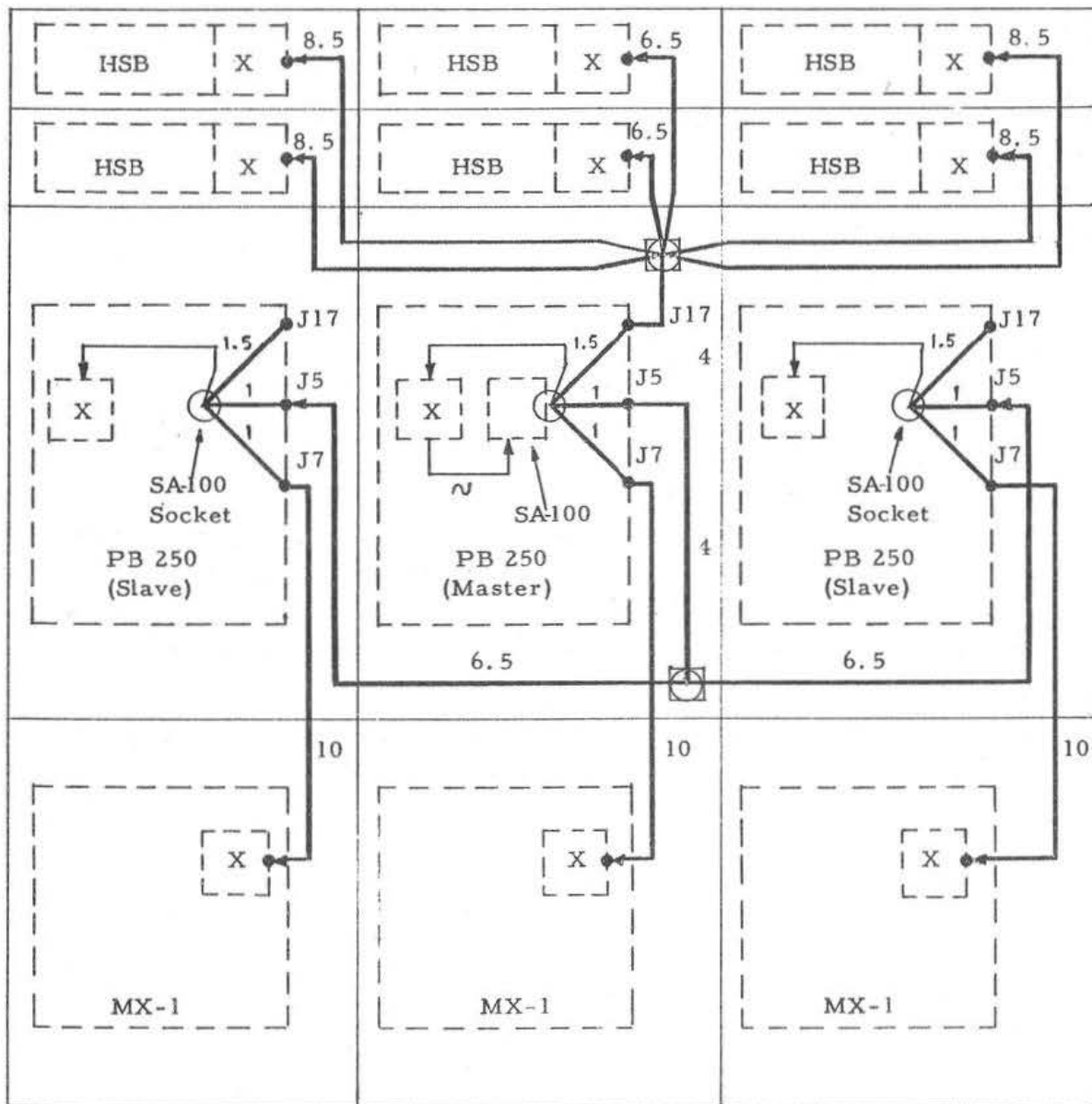


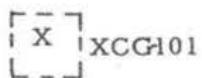
Figure 4-12. SA-100 Printed Wiring Assembly

To tune the SA-100 module for maximum output, it is necessary to remove the locking screw from the variable inductor L-1. After the required adjustment has been made, the locking screw must be replaced.





Symbols:



XCG101

Coaxial  
Distribution  
Cable

● Connector

○ Fan-out  
Junction

□ Junction  
Box

All dimensions are in feet

Figure 4-11. SA-100 Clock Distribution

Table 4-6

SA-100 SPECIFICATIONS

Requirements	Measurements
Input (sinewave with the following characteristics)	
Frequency	2Mc
Amplitude	3.5 to 5.5 volts rms
Impedance	4.3 kilohms at 2Mc
Output (at maximum load)	
Number of XCG shapers	12
Distribution cabling capacitance	1500
Power	
-12v	22ma
+ 6v	6ma

H-1. DISTRIBUTION CABLING

The first cable junction is at the socket of the SA-100, with a maximum fan-out of four primary lines. Any one of the primary lines may in turn have one junction with a maximum fan-out of six secondary lines. Where a primary line fans out into two secondary lines only, each secondary line is allowed a third junction with a fan-out of two tertiary lines.

## V. PARTS LIST

The PB250 Computer Assembly is shown in Figure 5-1. The number assigned to each subassembly or part in the figure corresponds to the number in the Figure and Index column of the Parts List in Table 5-1.

Information concerning parts and procurement may be obtained from the Packard Bell Computer Corporation, Los Angeles 25, California.

Table 5-1. (Sheet 1 of 2)

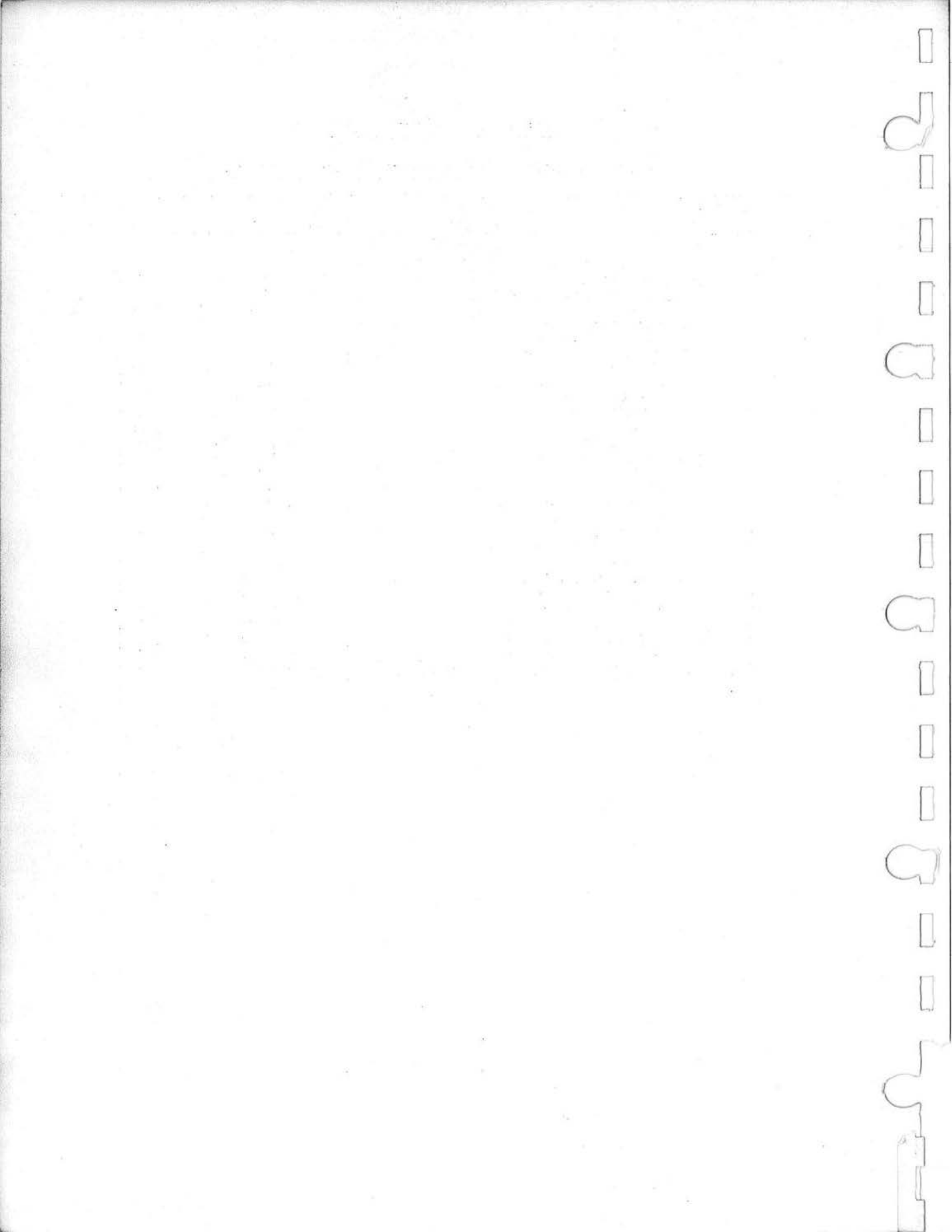
PB250 COMPUTER ASSEMBLY, PARTS LIST

Figure and Index	Part Description	Ref. Desig.	PBCC Part Number	Qty	Usable On Code
Fig. 5-1	PB250 ASSY . . . . .		502617	1	
1, 2	. HANDLES ASSY . . . . .		500033	1	
3	. FRAME ASSY, Right . . . . .		502480	1	
4	. FRAME ASSY, Left . . . . .		502464	1	
5	. POST, Center . . . . .		502203	1	
6	. PLATE ASSY, Connector . . . . .		502585	1	
7	. COVER, Front . . . . .		502228	1	
8	. MOUNT ASSY, Time Indicator . . . . .		504554	1	
9	. COVER, Standard Wiring . . . . .		502487	5	
10	. COVER, Offset Wiring . . . . .		502596	1	
11	. MODULE, Crystal Clock Generator, XCG-101 . . . . .		506521	1	
12	. MODULE, Clock Driver, CD-100 . . . . .		502692	1	
13	. MODULE, Gate Driver, GD-100 . . . . .		502492	6	
14	. MODULE, Driver, TD-100 . . . . .		502473	4	
15	. MODULE, Emitter-Follower, EF-100 . . . . .		502454	5	
16	. MODULE ASSY, Memory, 1 Word, MSR-2 . . . . .		504398-11-23	3	
17	. MODULE, Flip-Flop, TF-100 . . . . .		502433	17	
18	. MODULE ASSY, Memory, 16 Word, MSR-1 . . . . .		504276-191	1	
19	. MODULE, Diode Gate, DG-102 . . . . .		502336	29	
20	. MODULE, Diode Gate, DG-101 . . . . .		502321	38	
21	. MODULE, Diode Gate, DG-100 . . . . .		502334	16	
22	. MODULE, Filter Card, FC-100 . . . . .		504580	3	
23	. MODULE, Emitter-Follower, EF-101 . . . . .		504625	4	
24	. SCREW, Pan Head, No. 4-40 x 7/16 . . . . .		503505-7-2	16	
25	. SCREW, Pan Head, No. 6-32 x 5/16 . . . . .		503507-5-2	10	
26	. SCREW, Flat Head, No. 6-32 x 1/4, csk 100 <sup>o</sup> . . . . .		503506-4-2	48	
27	. SCREW, Flat Head, No. 8-32 x 7/16, csk 100 <sup>o</sup> . . . . .		503508-7-2	8	
28	. SCREW, Pan Head, No. 8-32 x 5/16 . . . . .		503509-5-2	10	
29	. SCREW, Pan Head, No. 6-32 x 1/2 . . . . .		503507-8-2	2	
30	. WASHER, Flat, No. 6 . . . . .		503519-4-2	2	
31	. SCREW, Flat Head, No. 6-32 x 7/8, csk 100 <sup>o</sup> . . . . .		503506-14-2	4	
32	. Deleted				
33	. CABLE, AC Power . . . . .		504263	1	
34	. BUSHING . . . . .		503149-10	1	
35	. BUSHING . . . . .		503149-7	1	
36	. RELAY . . . . .		503193	1	
37	. CABLE ASSY, Power Supply, PB250 . . . . .		504596	1	
38	. SLEEVING, Spiral Wrap . . . . .		503077-2	AR	
39	. CORD, Black Lacing . . . . .		503216-2	AR	
40	. SOLDER (QQ-S-571, Type SN60) . . . . .			AR	
41	. WIRE, Stranded, Teflon Insulation . . . . .		503045-24	AR	
42	. WIRE, 24 AWG, Solid, Teflon Insulation . . . . .		503089-24	AR	
43	. CLAMP, Cable . . . . .		503018-7	4	
44	. WIRE, 16 AWG, Stranded, Teflon Insulation . . . . .		503091-16-2	AR	
45	. WIRE, 24 AWG, Stranded, Teflon Insulation . . . . .		503091-24-2	AR	
46	. WIRE, 16 AWG, Stranded, Teflon Insulation . . . . .		503045-16	AR	
47	. WIRE, 16 AWG, Stranded, Teflon Insulation . . . . .		503091-16-4	AR	
48	. SLEEVING, Plastic, No. 24 . . . . .		503047-24	AR	

Table 5-1. (Sheet 2 of 2)

PB250 COMPUTER ASSEMBLY, PARTS LIST

Figure and Index	Part Description	Ref. Desig.	PBCC Part Number	Qty	Usable On Code
Fig. 5-1					
49	. SLEEVING, Plastic, No. 22 . . . . .		503047-22	AR	
50	. SLEEVING, Plastic, No. 24 . . . . .		503092-24-2	AR	
51	. SLEEVING, Plastic, No. 24 . . . . .		503092-24-1	AR	
52	. TERMINAL, Solderless . . . . .		503122-1	3	
53	. TERMINAL, Solderless . . . . .		503122-2	10	
54	. WASHER, Lock, Flat, Internal Tooth, No. 6 . . . . .		503520-6-2	14	
55	. TERMINAL, Standoff, Molded, (modified) .		505060	2	
56	. DIODE, IN2069 . . . . .		503178	2	
57	. SLEEVING, Plastic, No. 16 . . . . .		503047-16	AR	
58	. WIRE, Solid Uninsulated No. 16 . . . . .		503048-16	AR	
59	. SLEEVING, Plastic, Clear, No. 14 . . . . .		503092-14-1	AR	
60	. RESISTOR, 6.8k ±5%, 1/4 w. . . . .		503100-682	18	
61	. RESISTOR, 2.7k ±5%, 1/4 w. . . . .		503100-272	6	
62	. RESISTOR, 5.6k ±5%, 1/4 w. . . . .		503100-562	25	
63	. RESISTOR, 15k ±5%, 1/4 w . . . . .		503100-153	1	
64	. RESISTOR, 18k ±5%, 1/4 w . . . . .		503100-183	5	
65	. NAMEPLATE, Escutcheon . . . . .		504532	1	
66	. MODULE ASSY, Memory, 256 Words, MRS-1 . . . . .		504276-3071	3	
67	. RESISTOR, 1k ±5%, 1/4 w . . . . .		503100-102	3	
68	. RESISTOR, 1.5k ±5%, 1/4 w . . . . .		503100-152	8	
69	. RESISTOR, 1.2k ±5%, 1/4 w . . . . .		503100-122	2	
70	. DIODE, Germanium, High Speed . . . . .		503050	5	
71	. RESISTOR, 1.8k ±5%, 1/4 w . . . . .		503100-182	1	
72	. MODULE ASSY, Memory, 1 Word, MSR-2 .		504398-11-24	2	
73	. RESISTOR, 10k ±5%, 1/4 w . . . . .		503100-103	8	



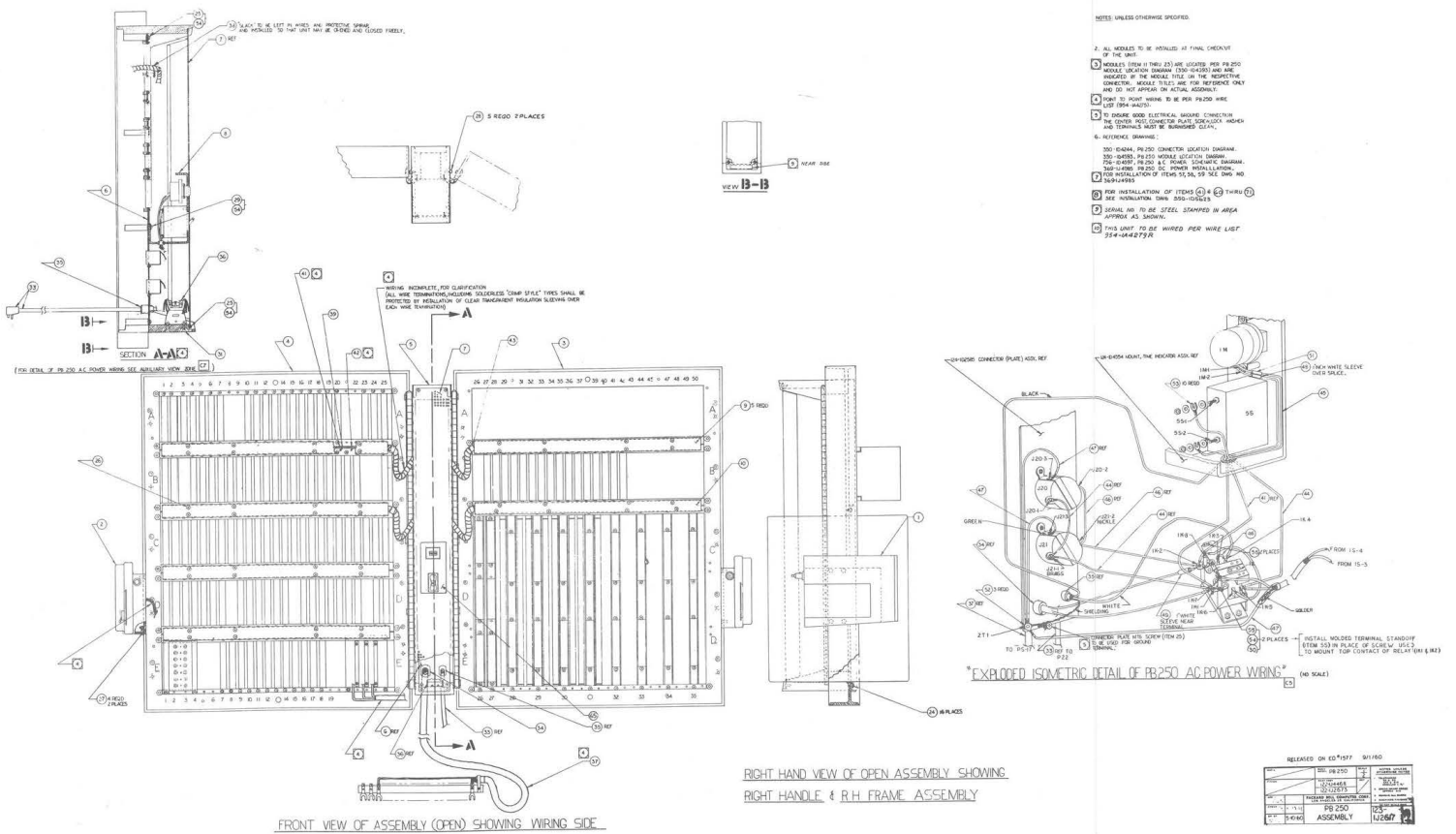


Figure 5-1. PB250 Assembly

## VI. LOGIC DIAGRAMS

This section contains logic layout diagrams of the PB250 Computer. Table 6-1 identifies the module location with the logic layout sheet pertaining to the location of each module, and the type of module.

These logic diagrams may be used in conjunction with the module schematic diagrams in Section VII.



( ) don't have

Table 6-1. (Sheet 1 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
1A	26, 35, 67	DG-102
2A	26	TF-100
3A	26	TF-100
4A	26, 28, 60, 67	DG-101
5A	26, 28	TF-100
6A	28, 29	DG-100
7A	29	MSR-2 <i>SECTOR COUNTER</i>
8A		
9A	26, 27, 29, 60, 67	EF-101
10A	27, 31, 74	GD-100
11A	27, 32, 75	DG-101
12A	27, 32, 74	DG-102
13A	30, 33	DG-101
14A	27, 28, 14, 69	DG-101
15A	27, 68, 69, 73	DG-101
16A	68	DG-101
17A	27, 60, 67, 68, 69	DG-102
18A	<sup>1</sup> 46, <sup>1</sup> 67, <sup>2</sup> 69, <sup>3</sup> 73	EF-100
19A	<sup>1</sup> 36, <sup>2</sup> 37, <sup>1</sup> 38, <sup>2</sup> 69	EF-100
20A	27, 69, 72	GD-100
21A	26, 30, 67, 72	DG-101
22A <i>comp. Coupling</i>	26, 30	(EF-101)
23A	25, 67	FC-100
24A	25, 67	FC-100

Table 6-1. (Sheet 2 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
25A	25, 67	FC-100
26A	47	DG-101
27A	47	DG-102
28A	47	DG-101
29A	47	DG-102
32A	77	GD-100
33A	77	GD-100
1B	34, 35	DG-101
2B	34	MSR-2 INSTRUCTION REG.
3B		
4B	31, 34	DG-101
5B	26, 31, 34, 44, 74	DG-102
6B	31	DG-100
7B	31	TF-100
8B	31, 46	DG-101
9B	33, 46	DG-101
10B	33, 46	DG-100
11B	33, 46	TF-100
12B	46	TF-100
13B	33, 60	DG-102
14B	28, 60	DG-101
15B	27, 47, 60, 74	DG-102
16B	44, 47, 60	DG-101
17B	26, 60, 74	GD-100

Table 6-1. (Sheet 3 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
18B	44, 69	DG-101
19B	36, 37, 38, 39, 40 <sup>46?</sup>	EF-100
20B	66	DG-100
21B	66	TF-100
22B	24	CD-100
23B	24	EF-101
24B	24	SA-100
25B	24	XCG-101
26B	59, 75	(EF-101) <i>with missing Ext. &amp; computer coupling</i>
27B	59, 64, 72	DG-101
28B	47, 64	DG-101
29B	47	DG-101
30B	47	DG-102
31B	59, 62	DG-101
32B	59	DG-101
33B	59	DG-101
34B	59, 64, 71, 72	DG-102
35B	59, 64	DG-101
36B	64, 71	DG-101
37B	71, 72	DG-101
38B	62, 71	DG-101
39B	71	DG-102
40B	59, 71	DG-101
41B	71	(DG-101)

Table 6-1. (Sheet 4 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
42B	71 <i>extra jump control</i>	DG-101
43B	63,76 <i>may base only</i>	DG-101
44B	76	TF-100
45B	63,65,76	DG-102
46B	63,65	DG-101
47B	63,65	DG-101
48B	63,65	DG-101
49B	63	EF-101
1C	35,37	DG-100
2C	32,35,36,37	DG-102
3C	35,37	TF-100
4C	36,37	DG-100
5C	36	TF-100
6C	36,37,42,43	DG-102
7C	36,37	DG-100
8C	36,37	TF-100
9C	36,37,38	DG-100
10C	37,38,43,49	DG-102
11C	38,43	TF-100
12C	43	DG-100
13C	41,42	TF-100
14C	41,42	DG-100
15C	27,40,42,43,60,61	DG-102
16C	40,41	DG-100

Table 6-1. (Sheet 5 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
17C	39, 40, 41, 42, 58, 60, 61	DG-102
18C	39, 40	DG-100
19C	39, 40	TF-100
20C	40, 76, 59, 51	DG-102
21C	42, 43, 45, 53, 61, 73	DG-102
22C	27, 44, 45, 66	DG-102
23C	40, 41, 42, 43, 45	EF-100
24C	44, 45, 60	DG-102
25C	44 <i>N09 - N79</i>	EF-100
26C	70	TD-100
27C	75	(GD-100)
28C	62, 63	MSR-1
29C	62	MSR-1
30C	62, 63	MSR-1
31C	62	MSR-1
32C	62	MSR-1
33C	62	MSR-1
34C	62	MSR-1
35C	62	MSR-1
1D	49	DG-101
2D	37, 49, 59	DG-102
3D	49	DG-101
4D	49, 73	DG-101
5D	36, 49, 51	DG-102

*used for  
memory retention  
+ computer input*

Table 6-1. (Sheet 6 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
6D	49, 51	DG-101
7D	49 <i>A REGISTER</i>	MSR-2
8D		
9D	49, 51	TF-100
10D	49, 51, 53	DG-102
11D	51 <del>B REGISTER</del>	DG-101
12D	51, 61	DG-102
13D	51, 55	DG-101
14D	51 <i>B REGISTER</i>	MSR-2
15D		
16D	58, 61	DG-100
17D	58, 61	DG-100
18D	53, 61	TF-100
19D	53, 61, 76	DG-102
20D	53	DG-101
21D	53, 61	DG-101
22D	53 <i>C REGISTER</i>	MSR-2
23D		
24D	43, 76 <i>magnet mem gat</i>	( TF-100 )
25D	45 <sup>4</sup>	( EF-100 ) <i>used for memory</i>
26D	70	TD-100 <i>cat.</i>
27D		
28D	62, 64	MSR-1
29D	62	MSR-1
30D	62	MSR-1

Table 6-1. (Sheet 7 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
31D	62, 64	MSR-1
32D	62	MSR-1
33D	62	MSR-1
34D	62	MSR-1
35D	62, 65	MSR-1
1E		
2E		Test jack
3E		Test jack
4E		
5E	46	DG-100
6E	46	TF-100
7E		
8E	49, 51, 55	EF-101
9E	54, 55, 56, 76	DG-102
10E	54, 55	DG-101
11E	54, 55	DG-101
12E	55	DG-101
13E	49, 51, 54, 57, 58	DG-102
14E	56, 67	DG-102
15E	24, 57, 58	DG-102
16E	56, 58	DG-100
17E	56, 58	TF-100
18E	57	DG-101
19E	24, 53	EF-101

Table 6-1. (Sheet 8 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
20E	24	GD-100
21E		
22E		Terminal strips
23E		Terminal strips
24E		Terminal strips
25E		
26E	67, 70	TD-100
27E	70	TD-100
28E		
29E		
30E		



B. L.	E. O. NO.	REV. LTR.	REVISION	BY	DATE	APP.	CHK.
NO	---	Q	(HISTORY RECORDED L THRU Q) COVER PAGE REVISED. CHANGED PER EDR #338. IDENTIFIED PAGES AND REV OF THIS DWG WITH CHG LETTERS CORRESPONDING TO WIRE LIST CHGS. RELEASED.	RH	7/14/61	[Signature]	[Signature]
NO	-	R	CHANGED PER DCR 1190. (DELETED SHT. 6, 8)	AM	7/2/61	[Signature]	[Signature]
NO	-	S	REVISED (PER DCR NO. 1349)	FG	12/2/61	[Signature]	[Signature]
NO	-	T	REVISED (PER DCR'S 1522 & 1051) SH. NO. CHANGES NOTED ON E.O.	K.W.	4/5/62		

SH 1 OF 77

505782

T

COVER SHEET FOR PB-250 LOGIC LAYOUT DIAGRAM

THIS DRAWING CONSISTS OF 77 SHEETS:

- 1) TITLE PAGE
- 2 & 3) REVISION INDEX
- 4) ALPHABETICAL INDEX SHEET
- 5 THRU 77) LOGIC

6-10

RELEASED ON S.C. #080-144873/REV. 10 DATED 7/16/61

MAT'L		BASIC MODEL	SCALE	NOTES: UNLESS OTHERWISE NOTED  1. TOLERANCES: XX ± .03 XXX ± .010 ANGULAR ± 1/4°  2. BREAK SHARP EDGES APPROX. .010  3. REMOVE ALL BURRS  4. MACHINED FINISHES TOG
FINISH		FE-250	REF	
APP.		NEXT ASSY.		
J.W.W.	3/15/61			
CHECK		PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		DO NOT SCALE DWG.
K.A.B.	3/15/61	PB-250 LOGIC LAYOUT		
DR. BY		DIAGRAM		
H.M.	3/14/61			505782
				SH 1 OF 77
				T
				CHK.

REVISION INDEX SHEET

DWG NO. 505782

REF  
T

SHEET NO. 2

SHEET	REVISION	SHEET	REVISION	SHEET	REVISION	SHEET	REVISION
1	T	19	T	37	T	55	T
2	T	20	T	38	T	56	T
3	T	21	DELETED PER REV E	39	T	57	T
4	T	22	T	40	T	58	T
5	T	23	T	41	T	59	T
6	T	24	T	42	T	60	T
7	T	25	T	43	T	61	T
8	T	26	T	44	T	62	T
9	T	27	T	45	T	63	T
10	T	28	T	46	T	64	T
11	T	29	T	47	T	65	T
12	T	30	T	48	T	66	T
13	T	31	T	49	T	67	T
14	T	32	T	50	T	68	T
15	T	33	T	51	T	69	T
16	T	34	T	52	T	70	T
17	T	35	T	53	T	71	T
18	T	36	T	54	T	72	T

6-11-9



PB 250 ALPHABETICAL INDEX

SHEET		SHEET		SHEET	
Function	Page	Function	Page	Function	Page
Ae	49	Hsg	72	(R) - (R8)	31
Ar	49	Ig, Ig	60	(R1) + (T1) + (S1) + (U1)	25
Aw	49	Ir, Iw	34	(R2) + (T2) + (S2) + (U2)	25
Be	51	Is	33	(R3) + (T3) + (S3) + (U3)	25
Br	51	Jg, Jo-J28	71	(R4) + (T4) + (S4) + (U4)	25
Bw	51	Kg	47	(R5) + (T5) + (S5) + (U5)	25
Bg, Bg	68	K1 K2 K3	46	(R6) + (T6) + (S6) + (U6)	25
(Bp)	25,61,71	Lg	44	(R7) + (T7) + (U7)	25
(B1)	61	LPC, LP1-LP8	70	(R8) + (S8) + (U8)	25
(B4)	38	LTC, LT1-LT6	70	Rc, Rc	31
(B5)	36	Lo, L1	43	Rf, Rf	66
(B6)	36,38	L2	42	Rf Tf	67
Ca	56	L3	41	Rf Tf	67
Ce	53	L4	40	(S1) --- (S8)	25
Clock Dist.	24	L5	39	Sc, Sc	28
Cog, Cpg	69	(M1), (M1)	66	Sp, Sp	76
Cr	53	Mog-M7g	45	Sr, Sr	29
Cw	53	Mor-M15r	62	Sw, Sw	29
Cycle Sync	76	Mow, M4w	63	(T1) --- (T6)	25
Dg, Dg	57	M1w, M7w	64	(Tb)	25
Ec	31	M15w	65	(Tc)	25
(Ec Rc), (Ec Rc)	74	Nog-N7g	44	Tf, Tf	66
Eg	32	Oc	35	Tg	70
(E1)	25,34,35,46,61,67	Of	58	(U1) --- (U8)	25
(E1)	25,31	Og, O1	38	Vg, Vg	47
(E1) + (Rf Tf)	67	O2, O3	57	Wg, WXg	60
Fg, Fg, Gdg	59	O4, O5, O6	36	Xg, Xg	55
(F1)	25,30,36,38,64,65	(O5 + O3)	73	Yg, Yg	54
(F1)	25,31,64	(O6 O5 O3)	73	Zg, Zg	54
F1-F5	26	(O6 O5 O4 O3 O2)	73		
(F1 F2)	74	(O6 O5 O4 O3 O2)	73		
(F1 F2 F3)	28	P1, P1	27		
(F3 F4 F5)	74	P2, P2	27		
Gdg	59	P3, P3	27		
Gsg	72	(P8-P15) ← F4	26		
		(P16-P23) ← F5	26		
		P23, P23	27		
		P24, P24	27		
		(P24-P7)	27		
		Pc	61		
		Pg	70		
		Ø1, Ø2	76		
		Qg, Qg	30		

505782 T  
SH. 4























TYPE 50S

No. 12J

FUNCTION BOOTSTRAPS IN.

Origin	Pin No.	Dest.	Term
	1	2D25	B6
	2	25A27	Rc
	3	9C2	B5
	4	25A33	Rc
	5	9C16	B4
	6	25A14	R4
	7	16D2	B1
	8	23A7	R1
	9		
	10		
	11		
	12	20B21	Mr
	13	22C34	Mr
	14		
	15	14J33	HSR Start
	16	18J33	MTU Start
14E33	17		H.S. Start
	18		
	19		
	20		
	21		
	22		
	23		
	24		
	25		
	26		
	27		
	28		
	29		
	30		
	31		
	32		
	33		
	34	14J6	S6
	35	18J6	U6
	36	14J5	S5
	37	18J5	U5
	38	14J4	S4
	39	18J4	U4
	40	14J1	S1
	41	18J1	U1
	42		
	43		
18J25	44	12J45	Gnd
12J44	45	24E4R	Gnd
14J25	46	12J47	-12
12J46	47	23E4R	-12
	48	14J37	HSR Stop
	49	18J37	MTU Stop
23B1	50		H.S. Stop









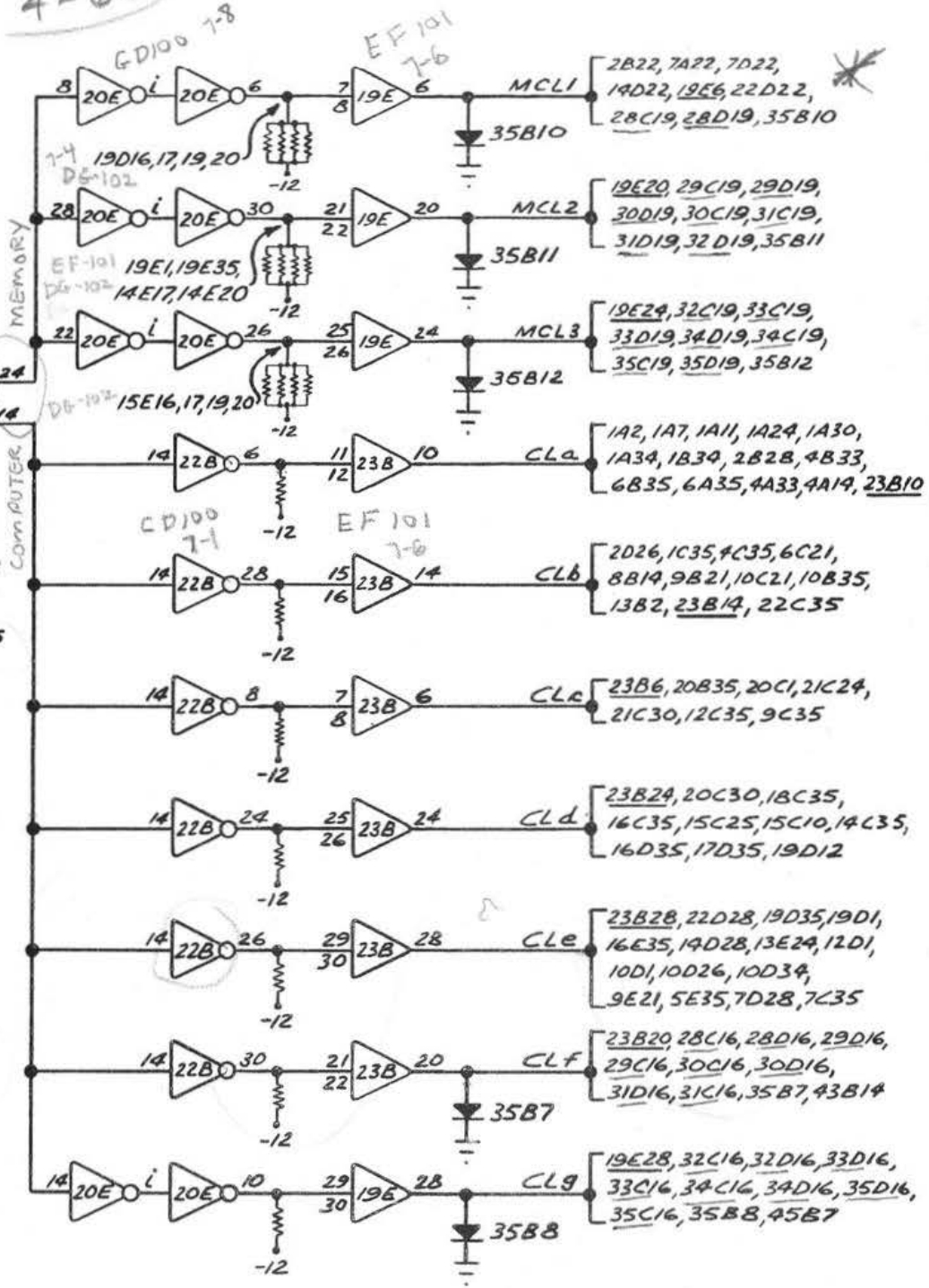
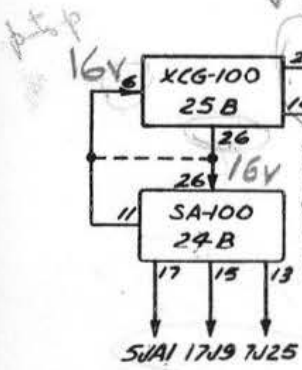








REF. TO  
4-68



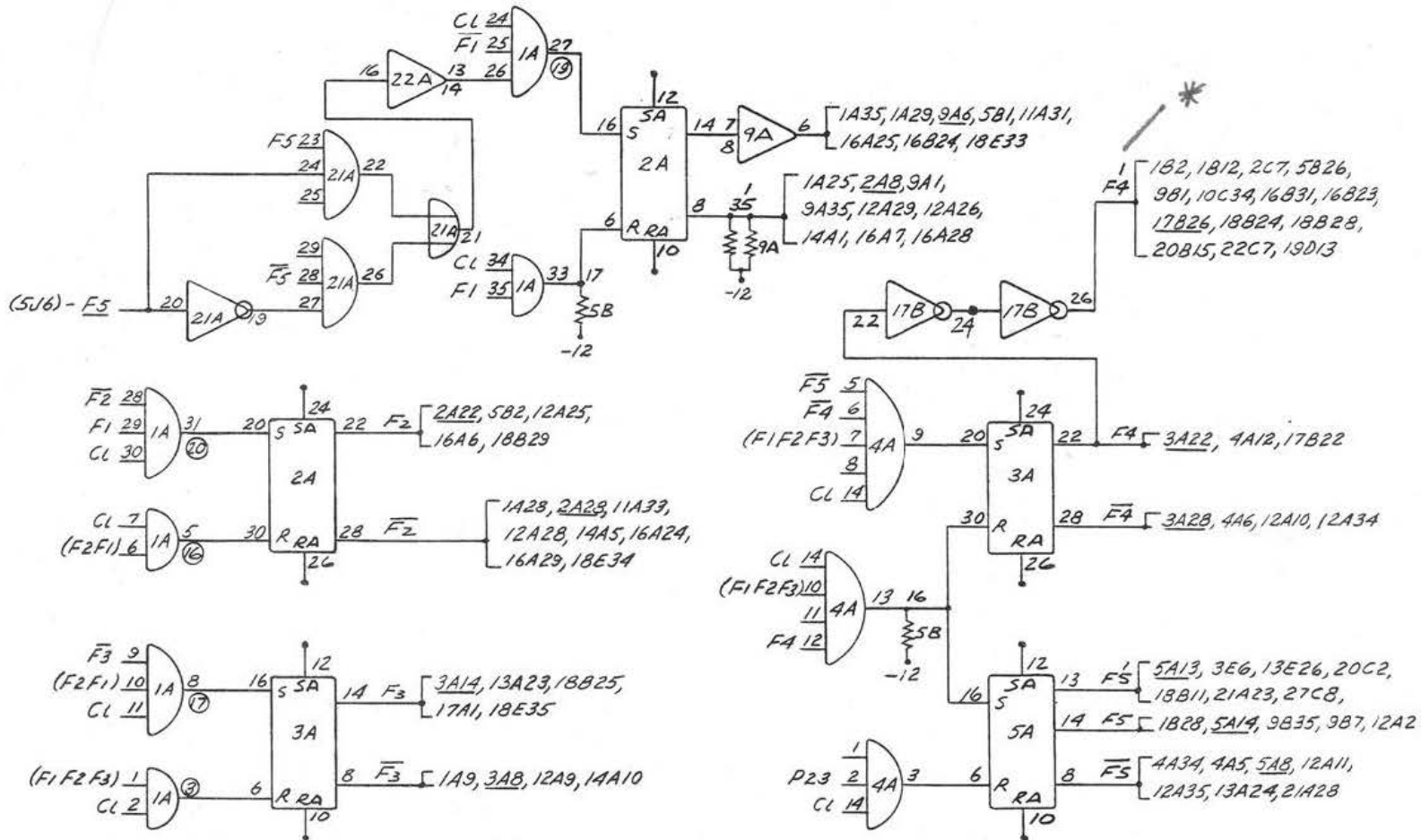
**LOGIC LAYOUT**

LOGIC SECT. \_\_\_\_\_ CLOCK DIST. \_\_\_\_\_ TERM \_\_\_\_\_  
 DWG NO. 505782 T DATE 12-27-61  
 DRAWN BY H. Berma APP. \_\_\_\_\_  
 SH. 24





6-34



$$SF1 = \bar{F}_1 (E_5 F_5 + \bar{F}_5 \bar{F}_5)$$

$$IF1 = F1$$

$$SF2 = \bar{F}_2 F1$$

$$IF2 = F2 F1$$

$$SF3 = \bar{F}_3 F2 F1$$

$$IF3 = F3 F2 F1$$

$$SF4 = \bar{F}_5 \bar{F}_4 F3 F2 F1$$

$$IF4 = F4 F3 F2 F1$$

$$SF5 = F4 F3 F2 F1$$

$$IF5 = P23$$

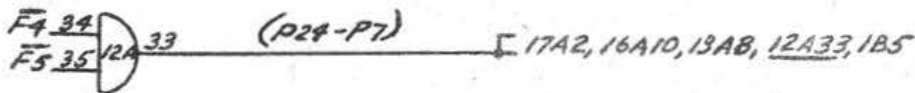
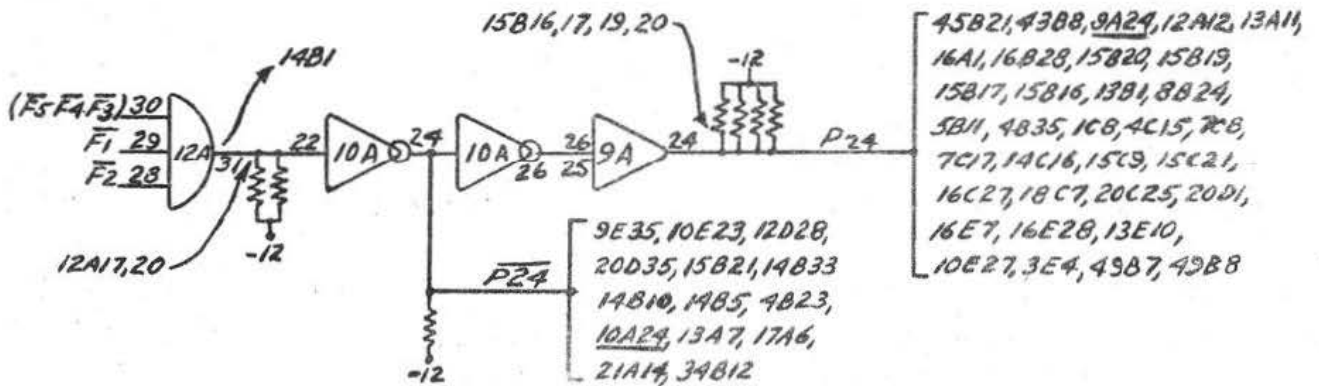
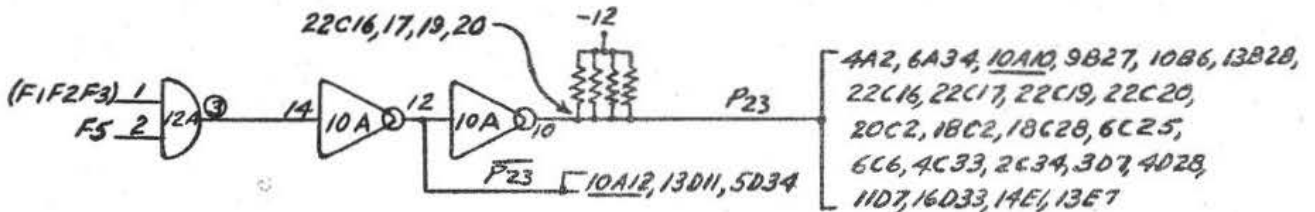
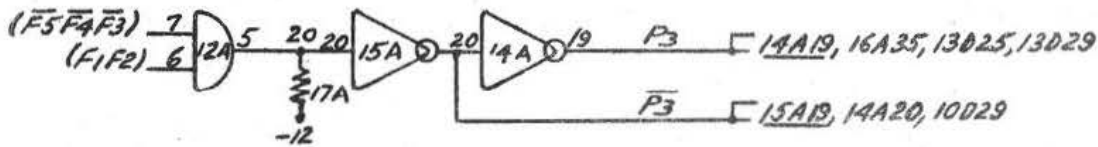
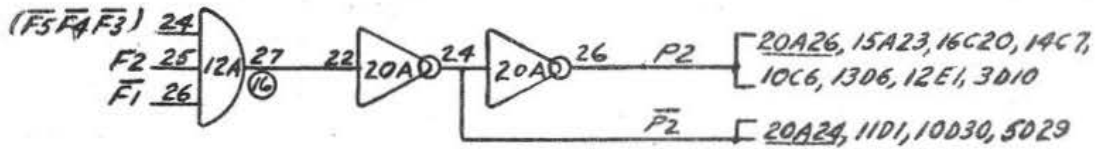
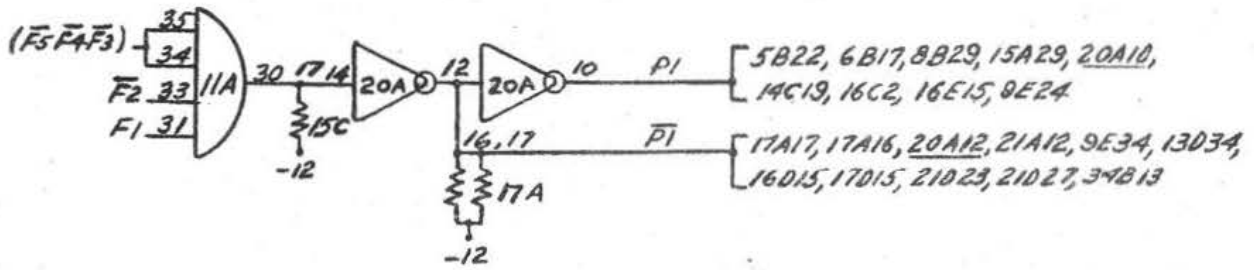
**LOGIC LAYOUT**

LOGIC SECT. P. & S. COUNTER TERM \_\_\_\_\_

DWG. NO. 505782 T DATE 1-8-62

DRAWN BY H. Mendelsohn APP. \_\_\_\_\_

SH. 26



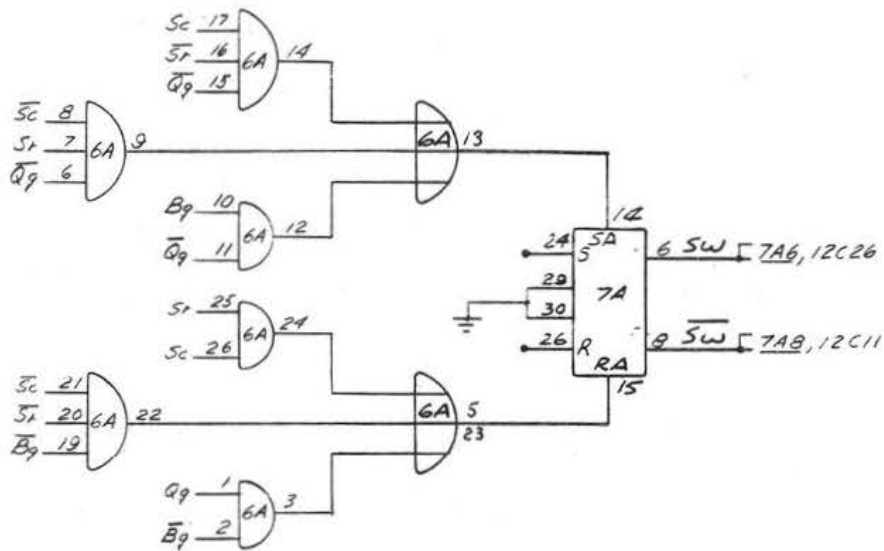
$P1 = \overline{F_5} \overline{F_4} \overline{F_3} \overline{F_2} F_1$      $P23 = F_5 F_3 F_2 F_1$   
 $P2 = \overline{F_5} \overline{F_4} \overline{F_3} F_2 \overline{F_1}$      $P24 = \overline{F_5} \overline{F_4} \overline{F_3} \overline{F_2} F_1$   
 $P3 = \overline{F_5} \overline{F_4} \overline{F_3} F_2 F_1$      $(P24-P7) = \overline{F_5} \overline{F_4}$

## LOGIC LAYOUT

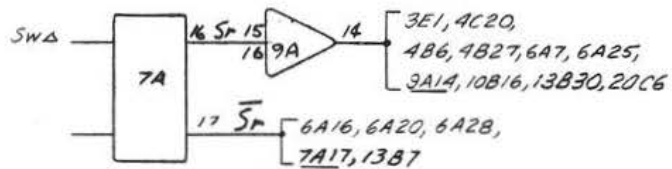
LOGIC SECT. P. & S. COUNTER TERM  
 DWG. NO. 5057E2 T    DATE 1-8-62  
 DRAWN BY H. Mendelssohn    APP. \_\_\_\_\_

SH. 27





6-37



$$sSw = Sc \bar{S}_r \bar{Q}_9 + \bar{S}_c S_r \bar{Q}_9 + B_9 \bar{Q}_9$$

$$rSw = Sc S_r + \bar{S}_c \bar{S}_r \bar{B}_9 + Q_9 \bar{B}_9$$

$$sSr = Sw \text{ DELAYED } 2R \text{ PULSE TIMES}$$

$$rSr = \bar{Sw} \text{ DELAYED } 2R \text{ PULSE TIMES}$$

## LOGIC LAYOUT

LOGIC SECT. P. & S. COUNTERS TERM 5w & Sr

DWG. NO. 505782 T

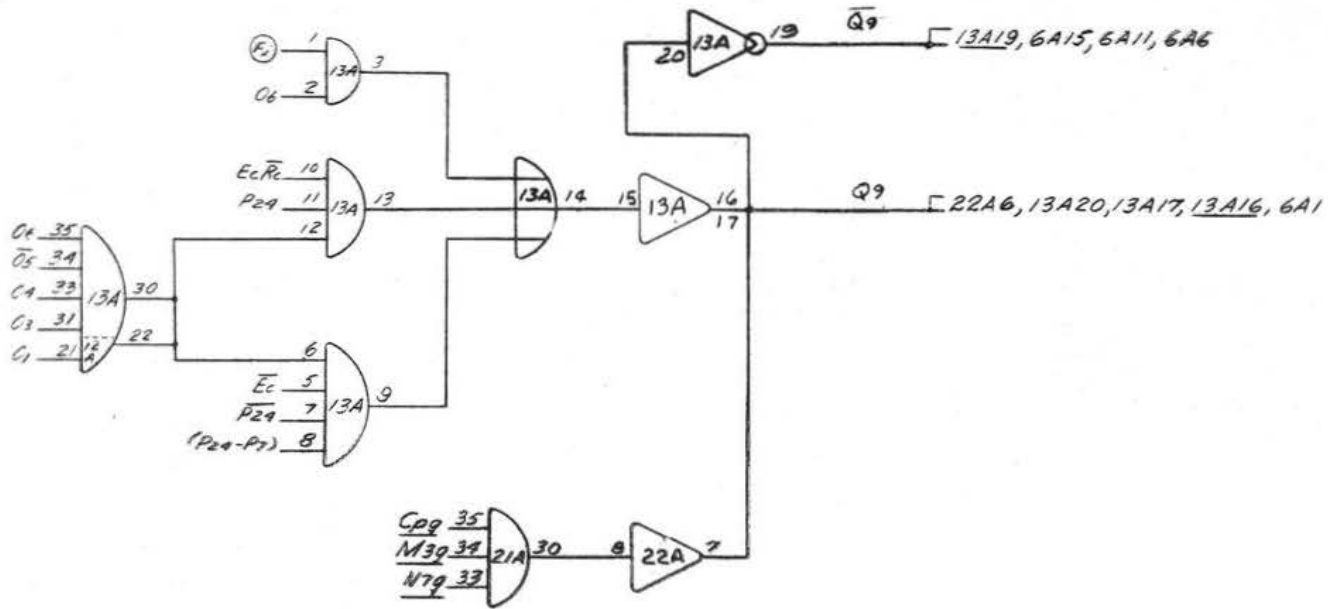
DATE 1-6-62

DRAWN BY H. D. [unclear]

APP. \_\_\_\_\_

SH. 29

6-38



$$Q_9 = \bar{E}_c O_6 \bar{O}_5 O_4 O_3 O_1 \bar{P}_{24} (P_{24} - P_7) + (F_j) O_6 + C_{p9} \underline{M}_{39} \underline{N}_{79} + E_c \bar{R}_c O_6 \bar{O}_5 O_4 O_3 O_1 P_{24}$$

$$\bar{Q}_9 = (\bar{Q}_9)$$

### LOGIC LAYOUT

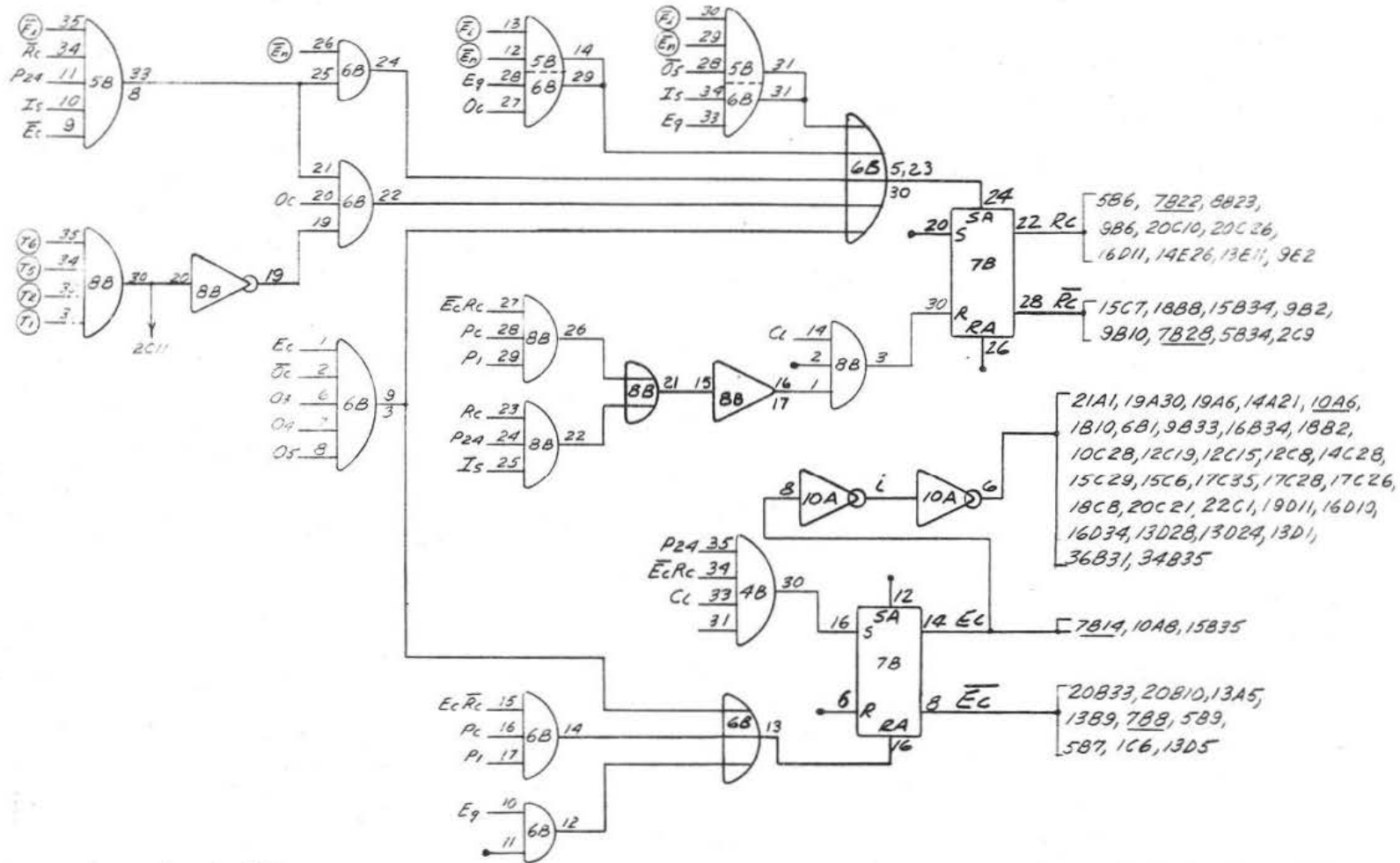
LOGIC SECT. P.L.S. COUNTERS TERM Q<sub>9</sub>

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. V. ... APP. \_\_\_\_\_

SH. 30

6-39



$$sEc = P24 \bar{E}c Rc$$

$$rEc = E9 + Ec Os O4 O3 \bar{O}c + Ec \bar{R}c Pc Pi$$

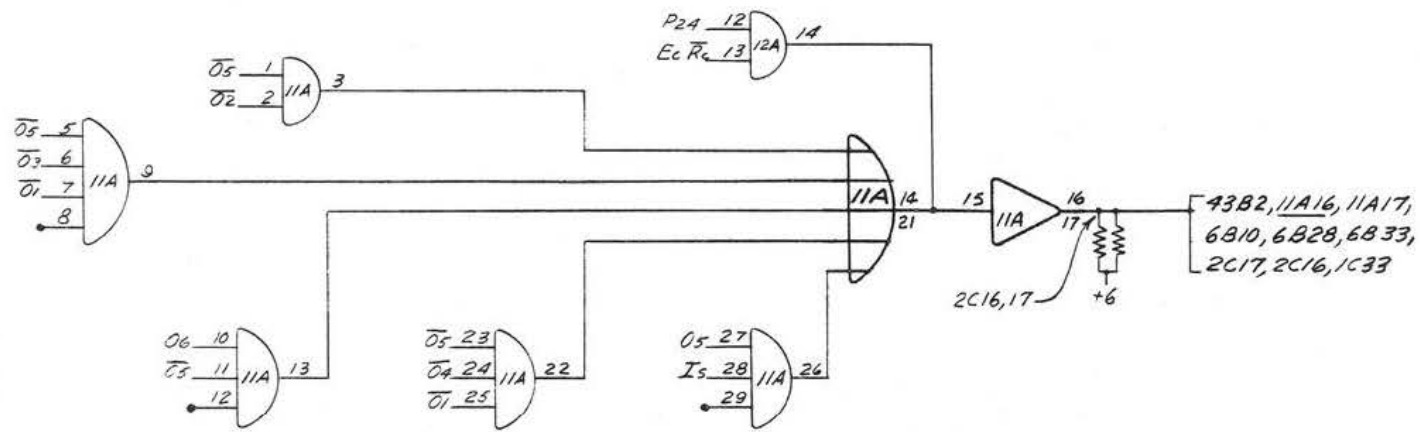
$$sRc = (\bar{E}n) (\bar{F}j) E9 Oc + (\bar{E}n) (\bar{F}j) E9 Os Is + P24 \bar{E}c \bar{R}c Is (\bar{E}n + Oc (\bar{T}6) (\bar{T}5) (\bar{T}2) (\bar{T}1)) (\bar{F}j) + Ec Os O4 O3 \bar{O}c$$

$$rRc = P24 Rc Is + \bar{E}c Rc Pc Pi$$

**LOGIC LAYOUT**

LOGIC SECT. INST. REF. & CONT. TERM  $E_2 \cdot 2+$   
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mendelsohn APP. \_\_\_\_\_  
 SH. 31

6-40



$$E_g = P_{24} E_c \overline{R_c} (\overline{O_5} \overline{O_2} + \overline{O_5} O_6 + \overline{O_5} \overline{O_3} \overline{O_1} + \overline{O_5} \overline{O_4} \overline{O_1} + O_5 I_5)$$

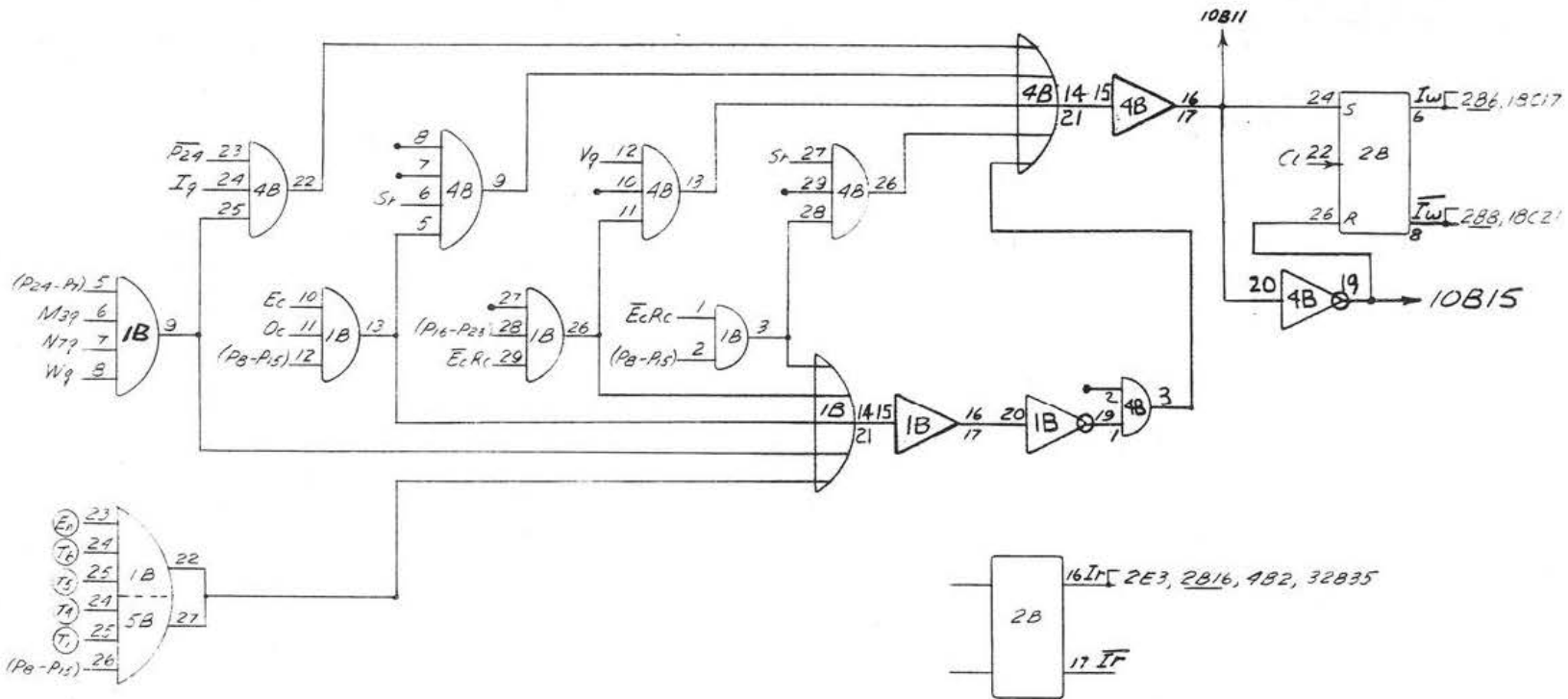
**LOGIC LAYOUT**

LOGIC SECT. INST. REG. & CONT. TERM E<sub>g</sub>  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mandelsohn APP. \_\_\_\_\_  
 SH.32



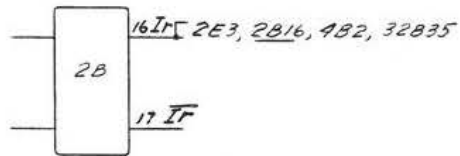


6-42



$$sIw = \bar{E}cRc(P8-P15)Sr + \bar{E}cRc(P16-P23)V9 + EcOc(P8-P15)Sr + \bar{P}24(P29-P7)M39N79W9I9 \\ + I9[\bar{E}cRc(P8-P15) + \bar{E}cRc(P16-P23) + EcOc(P8-P15) \\ + (P29-P7)M39N79W9 + \bar{E}7(T6)(T5)(T4)(T1)(P8-P15)]$$

$$Iw = (sIw)$$



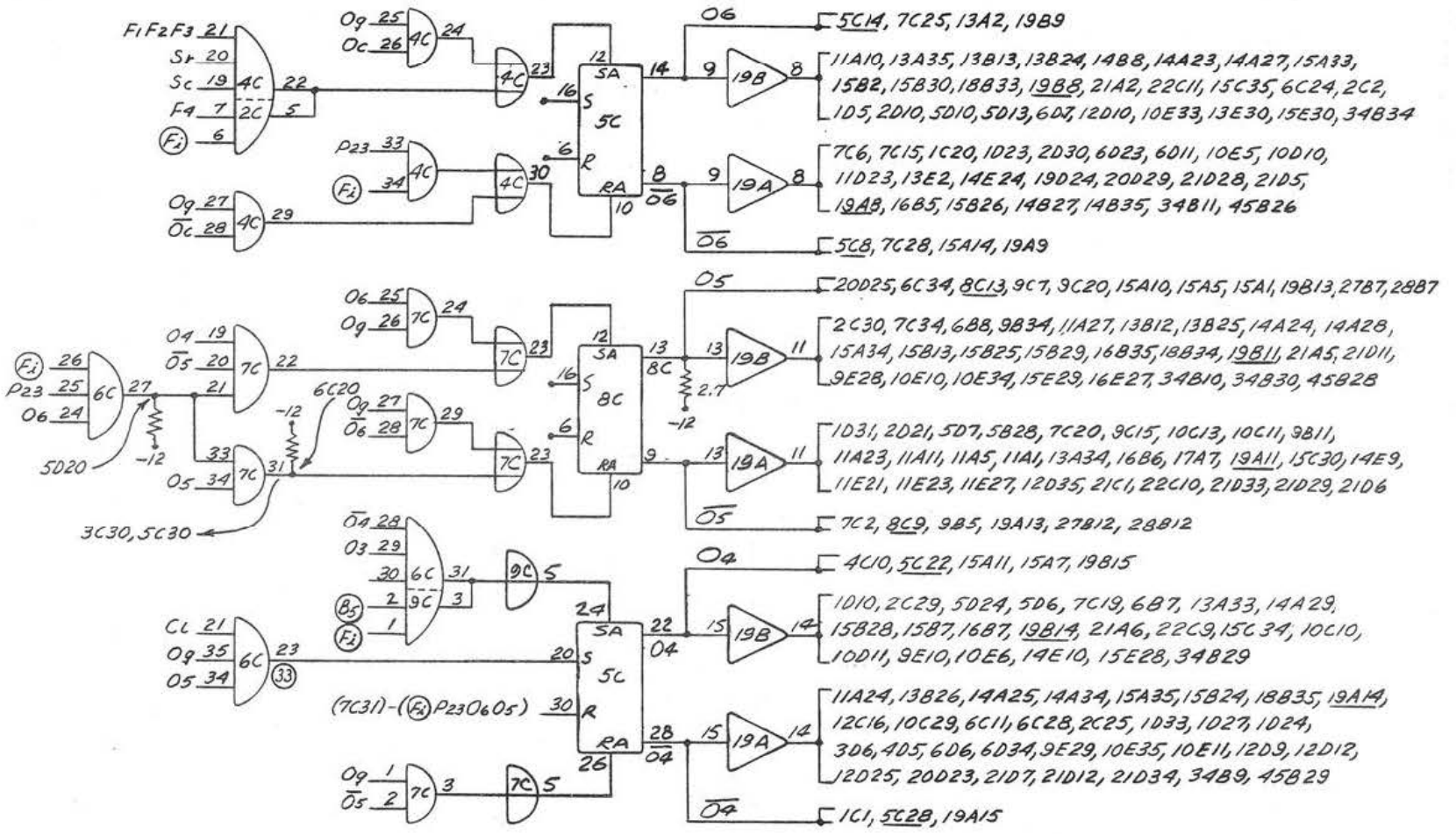
**LOGIC LAYOUT**

LOGIC SECT. INST. REG. & CNT. TERM: Iw & Iw-bar  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. J. ... APP. ...

SH 34



6-44

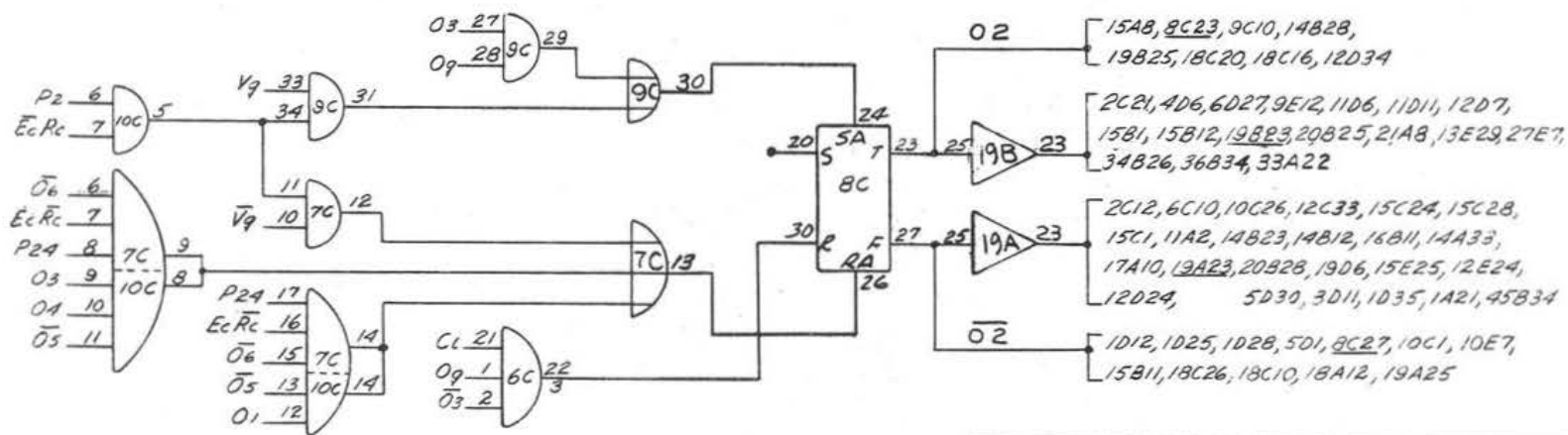
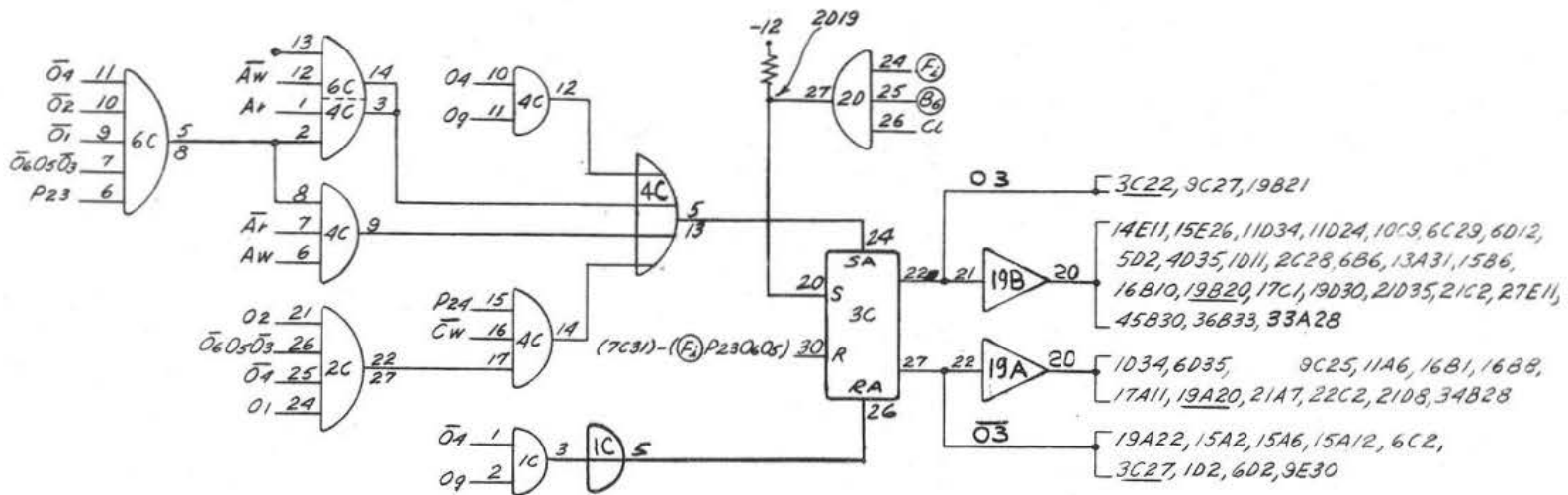


$$\begin{aligned}
 506 &= O_9 O_c + \textcircled{2} F_4 F_3 F_2 F_1 S_1 S_c \\
 \pm 06 &= \textcircled{2} P_{23} + O_9 \bar{O}_c \\
 505 &= O_9 O_6 + \textcircled{2} P_{23} O_6 \bar{O}_5 O_4 \\
 \pm 05 &= \textcircled{2} P_{23} O_6 O_5 + O_9 \bar{O}_6 \\
 504 &= O_9 O_5 + \textcircled{2} \textcircled{3} \bar{O}_4 O_3 \\
 \pm 04 &= \textcircled{2} P_{23} O_6 O_5 + O_9 \bar{O}_5
 \end{aligned}$$

**LOGIC LAYOUT**

LOGIC SECT.	OR CODE REG.	TERM	O <sub>6</sub> , O <sub>5</sub> , O <sub>4</sub>
DWG. NO.	505782 T	DATE	1-6-62
DRAWN BY	H. Mendelsohn	APP.	

SH. 36

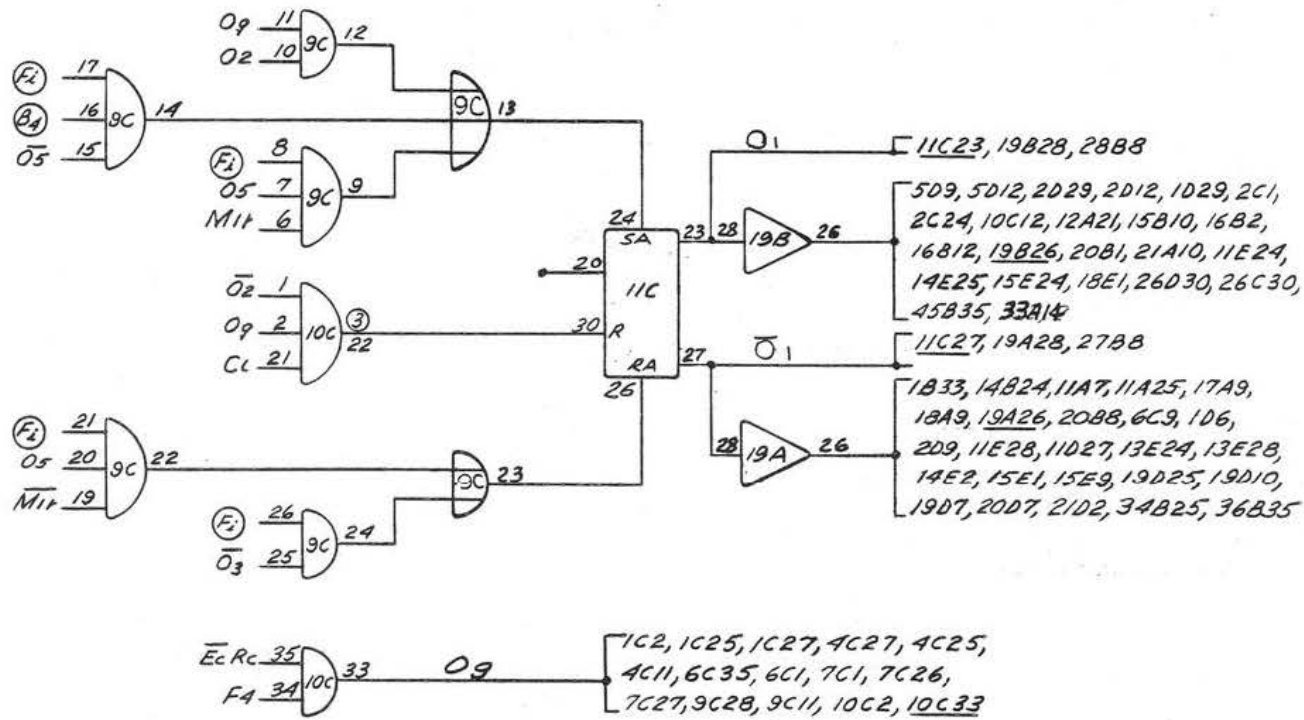


$sO3 = O9O4 + P23O6O5O4O3O2O1(Aw\bar{A}r + \bar{A}wAr) + P24O6O5O4O3O2O, \bar{C}w + (F_2) (B_6)$   
 $+ O3 = O9O4 + (F_2) P23O6O5$   
 $sO2 = O9O3 + \bar{E}cRcP2V9$   
 $+ O2 = O9O3 + P24EcRcO6O5O1 + P24EcRcO6O5O1O3 + \bar{E}cRcP2V9$

### LOGIC LAYOUT

LOGIC SECT. OF CODE REG. TERM O3, O2  
 DWG. NO. 505782T DATE 1-6-62  
 DRAWN BY H. Wendt/ser.111 APP. \_\_\_\_\_

6-46



$$sO_1 = O_q O_2 + \overline{F_i} \overline{B_4} \overline{O_s} + \overline{F_i} O_s M_i$$

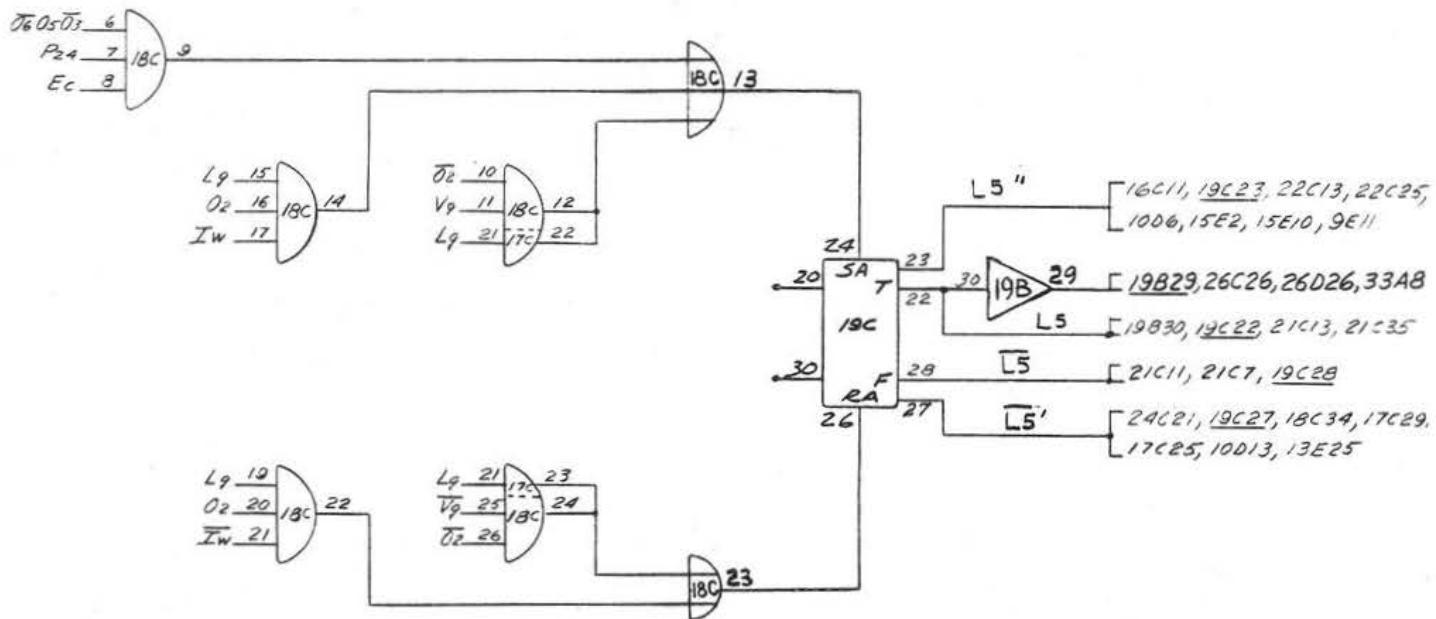
$$rO_1 = O_q \bar{O}_2 + \overline{F_i} \bar{O}_3 + \overline{F_i} O_s \bar{M}_i$$

$$O_q = \bar{E}cRc F_4$$

### LOGIC LAYOUT

LOGIC SECT. OP CODE REG. TERM  $O_1, O_q$   
 DWG. NO. 505782 T DATE 1-6-62  
 DWN. BY H. Mendelsohn APP. \_\_\_\_\_

SH. 38



6-47

$$sL5 = L_9 \overline{O_2} V_9 + L_9 O_2 I_w + \overline{O_2} O_1 \overline{O_3} P_{24} E_c$$

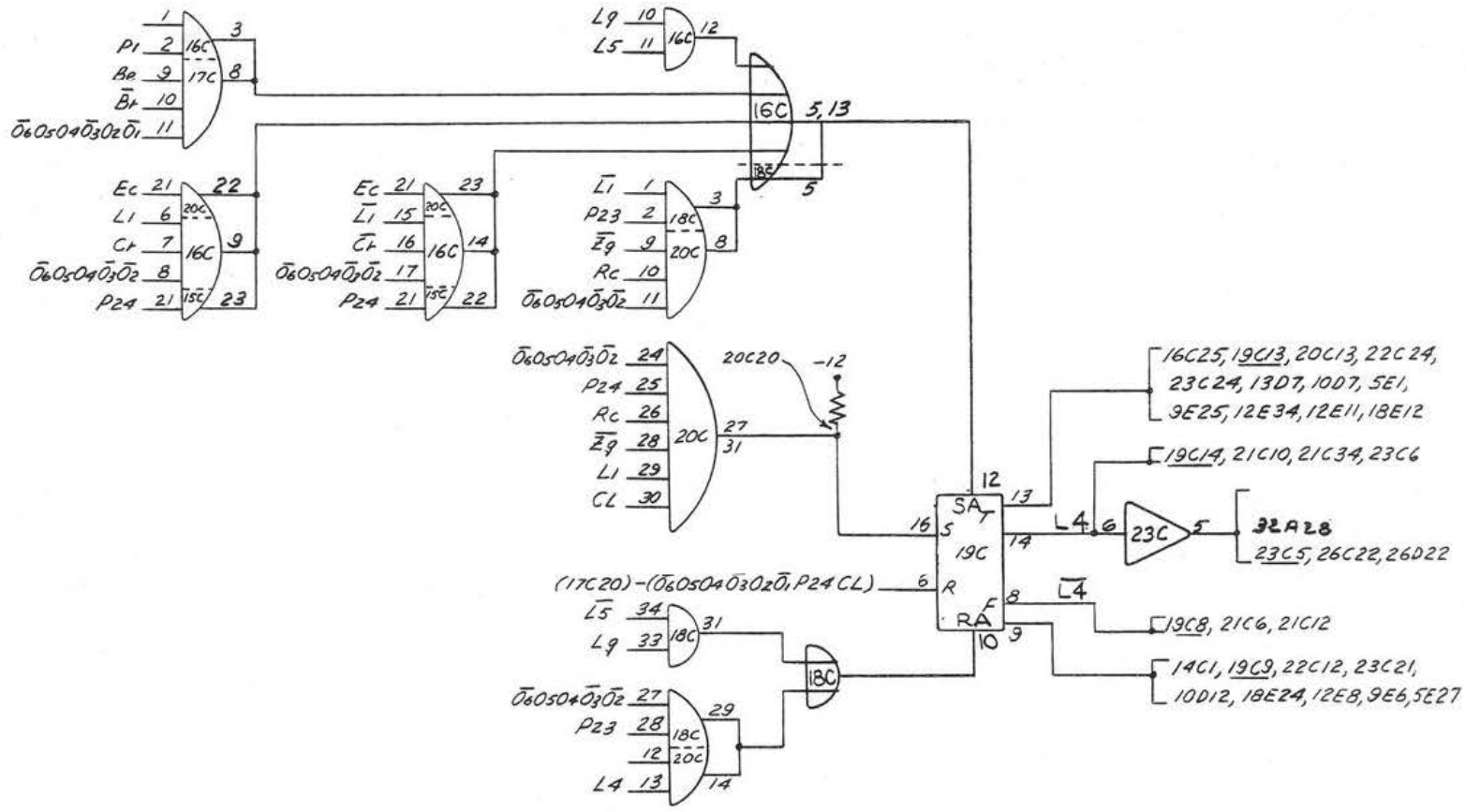
$$rL5 = L_9 \overline{O_2} \overline{V_9} + L_9 O_2 \overline{I_w}$$

### LOGIC LAYOUT

LOGIC SECT. CP LINE SEL. TERM L5  
 DIVG. NO. 505782T DATE 1-6-62  
 DRAWN BY: H. H. Hodelmann APP. \_\_\_\_\_

SH. 39

6-48



$$sL4 = L9L5 + \bar{O}_6O_5O_4\bar{O}_3\bar{O}_2 [P24Ec(L1C1 + \bar{L}1\bar{C}1) + P23Rc\bar{L}1\bar{Z}9 + P24RcL1\bar{Z}9] + \bar{O}_6O_5O_4\bar{O}_3O_2\bar{O}1P1Be\bar{B}1$$

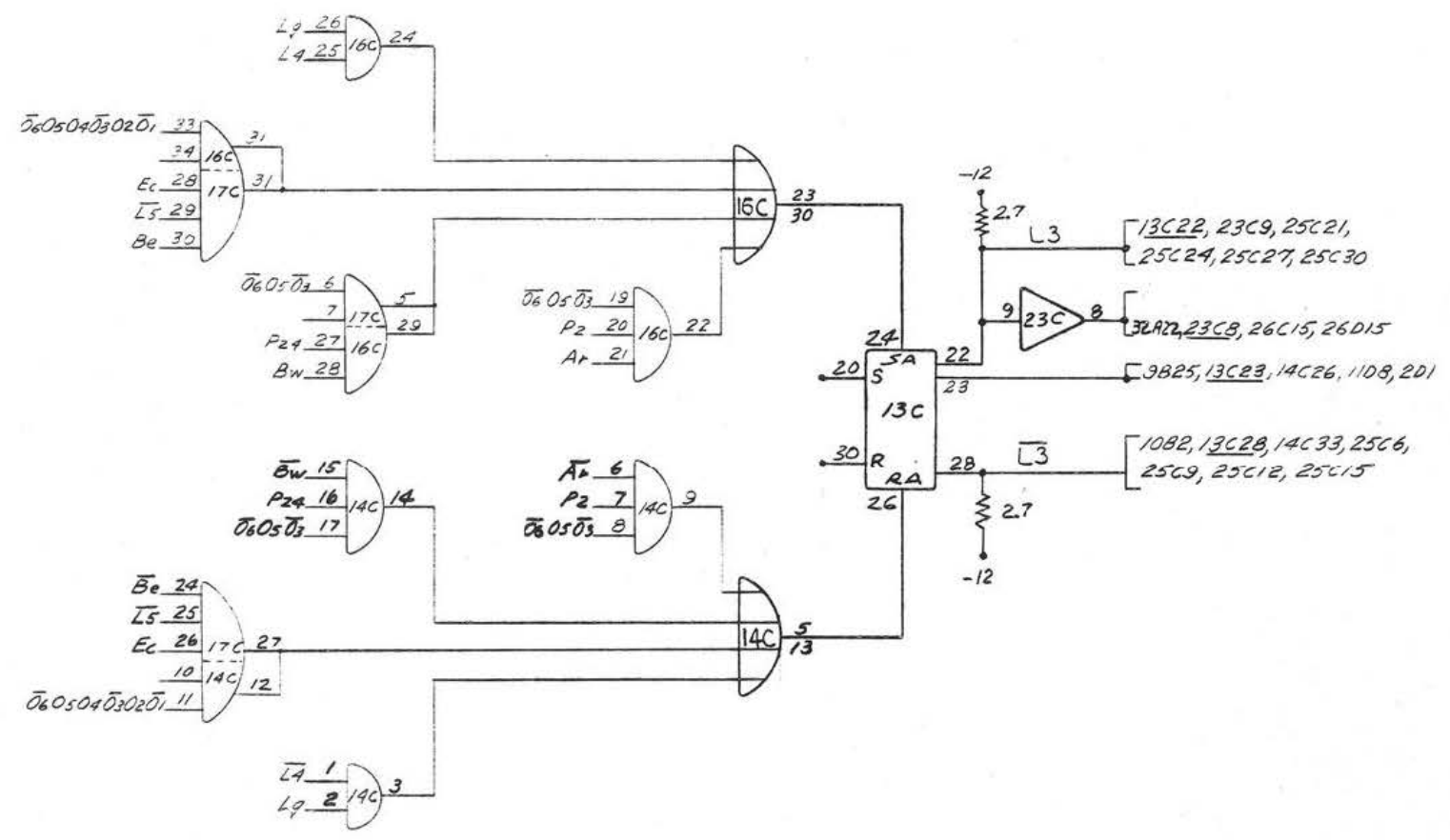
$$tL4 = L9\bar{L}5 + \bar{O}_6O_5O_4\bar{O}_3\bar{O}_2P23L4 + \bar{O}_6O_5O_4\bar{O}_3O_2\bar{O}1P24$$

**LOGIC LAYOUT**

LOGIC SECT.	<u>OP. LINE SEL.</u>	TERM	<u>L4</u>
DWG. NO.	<u>505782T</u>	DATE	<u>1-9-62</u>
DRAWN BY	<u>H. Mendelsohn</u>	APP.	

SH. 40

6-49



$$sL3 = LpL4 + \bar{O}_6O_5\bar{O}_3(P_{24}B_w + P_2A_r) + \bar{O}_6O_5O_4\bar{O}_3O_2\bar{O}_1E_c\bar{I}_5B_e$$

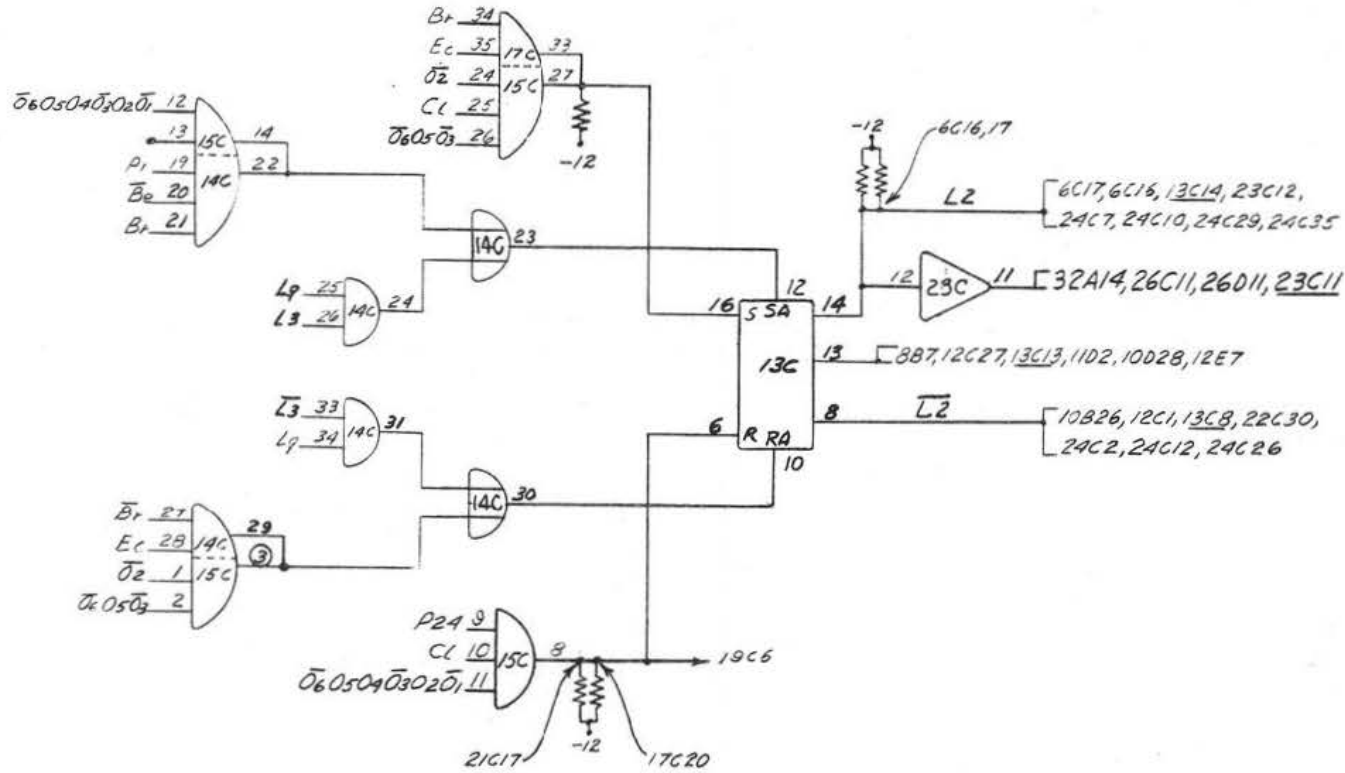
$$rL3 = Lp\bar{I}_4 + \bar{O}_6O_5\bar{O}_3(P_{24}\bar{B}_w + P_2\bar{A}_r) + \bar{O}_6O_5O_4\bar{O}_3O_2\bar{O}_1E_c\bar{I}_5\bar{B}_e$$

**LOGIC LAYOUT**

LOGIC SECT. OR LINE SEL. TERM L3  
 DWG. NO. 505782T DATE 1-6-62  
 DRAWN BY H. Mandelsohn APP. \_\_\_\_\_  
 SH. 41



6-50



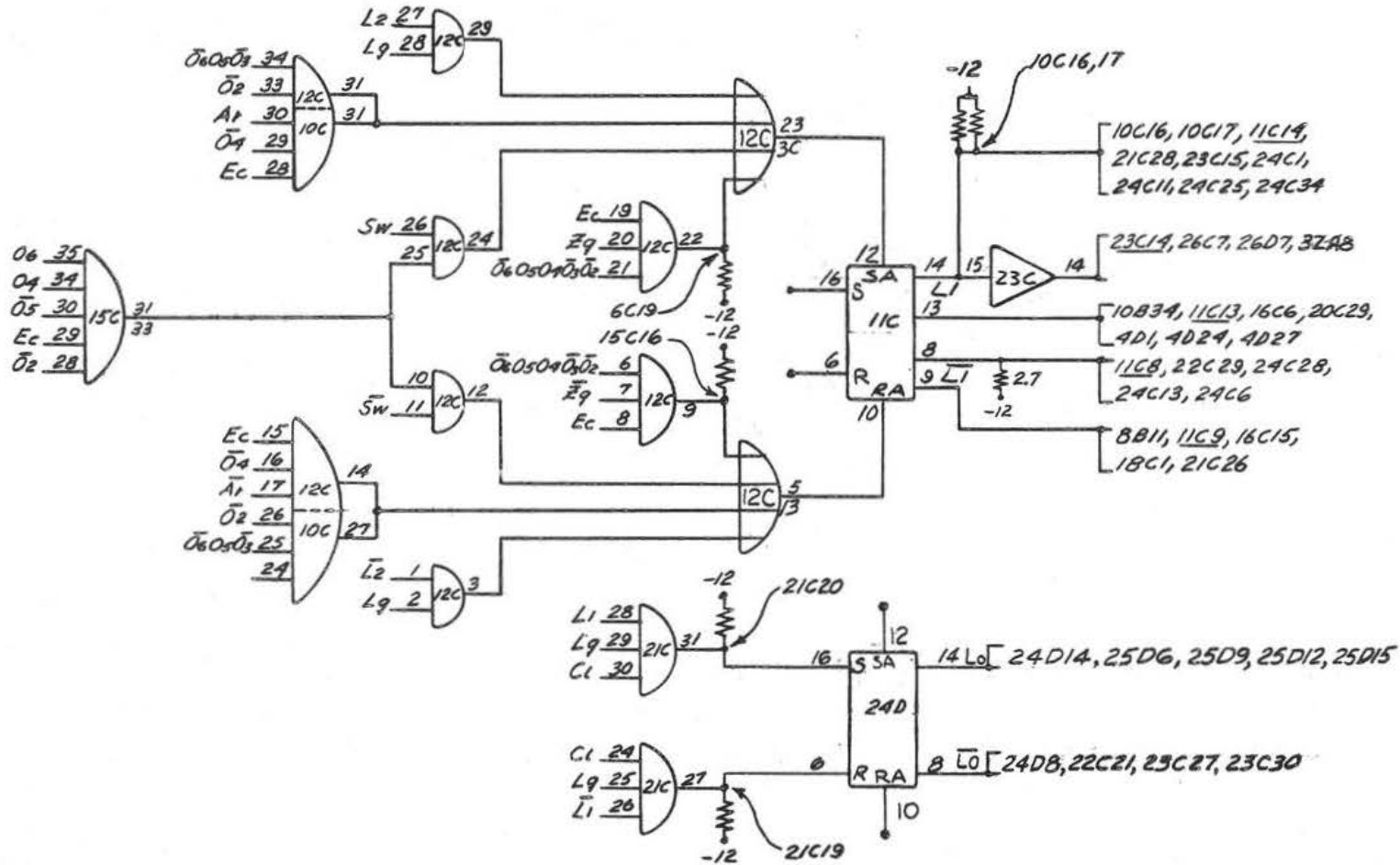
$$sL_2 = L_9 L_3 + \bar{O}_6 O_5 \bar{O}_3 \bar{O}_2 E_c B_r + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 \bar{B}_r B_r P_1$$

$$rL_2 = L_9 \bar{L}_3 + \bar{O}_6 O_5 \bar{O}_3 \bar{O}_2 E_c \bar{B}_r + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 P_{24}$$

### LOGIC LAYOUT

LOGIC SECT. OP. LINE SEL. TERM L2  
 DWG. NO. 5057B2 T DATE 1-6-62  
 DRAWN BY H. D. and Isoku APP. \_\_\_\_\_

SH. 42



$$sL0 = L1L9$$

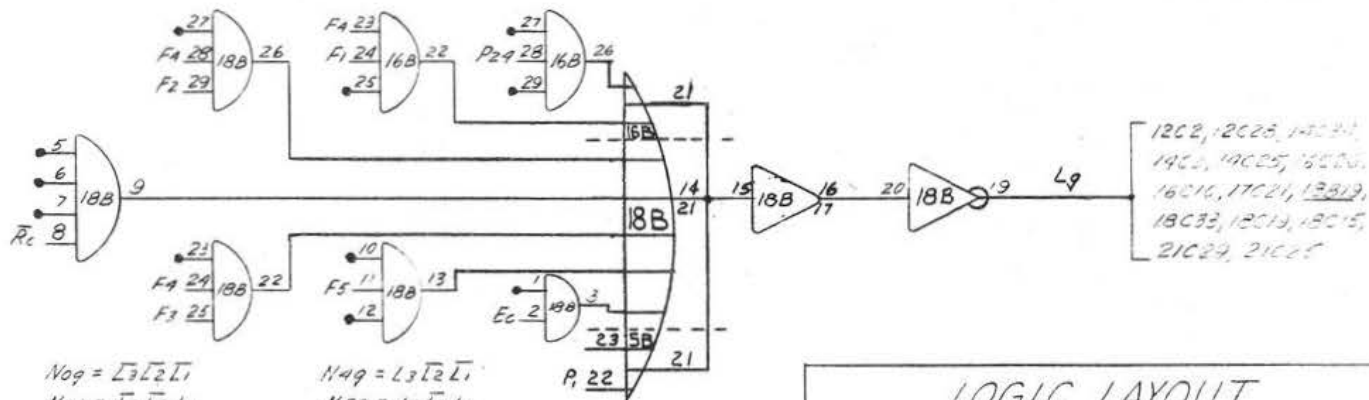
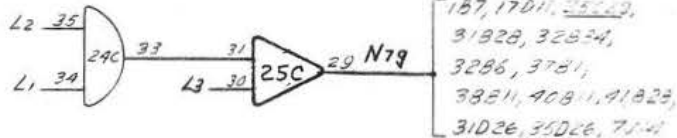
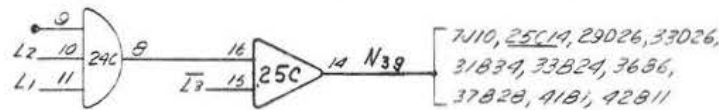
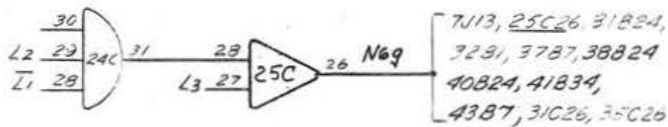
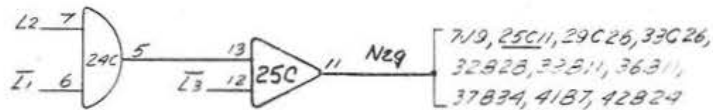
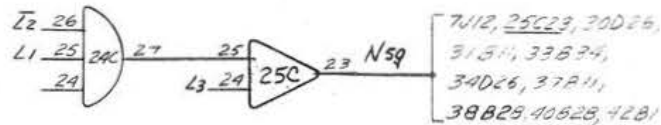
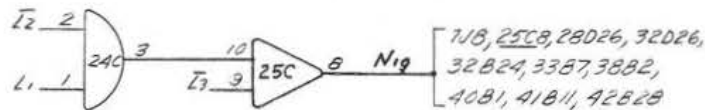
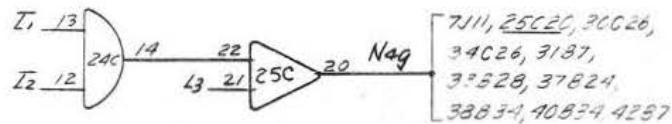
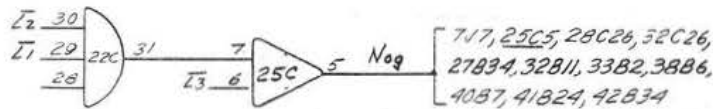
$$iL0 = \bar{L1}L9$$

$$sL1 = L9L2 + \bar{O6}O5\bar{O3}\bar{O2}Ec(\bar{Z9}O4 + A1\bar{O4}) + O6\bar{O5}O4\bar{O2}EcSw$$

$$iL1 = L9\bar{L2} + \bar{O6}O5\bar{O3}\bar{O2}Ec(\bar{Z9}O4 + A1\bar{O4}) + O6\bar{O5}O4\bar{O2}EcSw$$

**LOGIC LAYOUT**

LOGIC SECT. OP LINE SEL TERM L1, L0  
 DWG. NO. 505782T DATE 1-6-62  
 DRAWN BY W. Bernman APP. \_\_\_\_\_  
 SH. 43

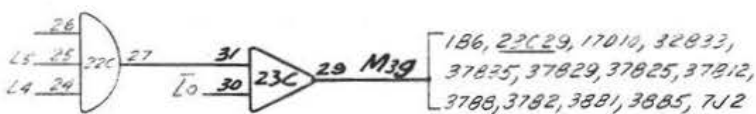
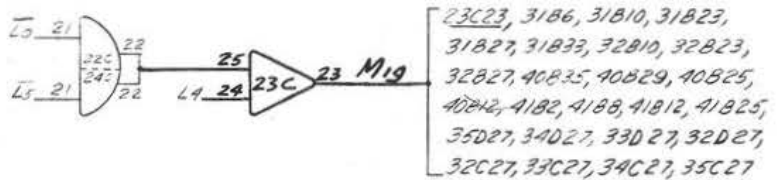
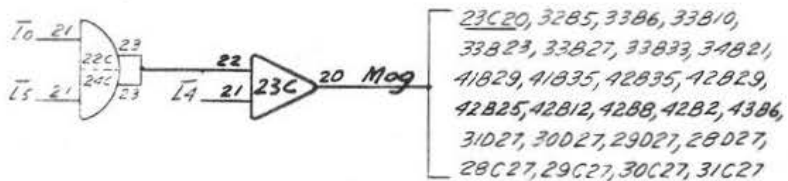


$N_{09} = \bar{L}_3 \bar{L}_2 \bar{L}_1$   
 $N_{19} = \bar{L}_3 \bar{L}_2 \bar{L}_1$   
 $N_{29} = \bar{L}_3 \bar{L}_2 \bar{L}_1$   
 $N_{39} = \bar{L}_3 \bar{L}_2 \bar{L}_1$   
 $N_{49} = \bar{L}_3 \bar{L}_2 \bar{L}_1$   
 $N_{59} = \bar{L}_3 \bar{L}_2 \bar{L}_1$   
 $N_{69} = \bar{L}_3 \bar{L}_2 \bar{L}_1$   
 $N_{79} = \bar{L}_3 \bar{L}_2 \bar{L}_1$

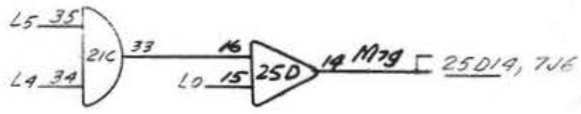
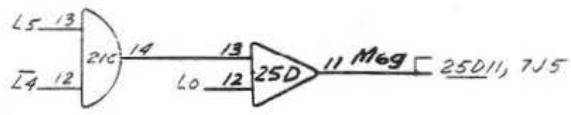
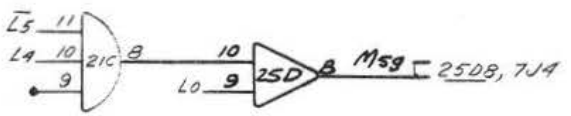
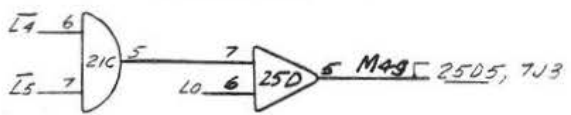
$L_9 = \bar{E}_c + \bar{R}_c + F_5 + F_4 F_3 + F_4 F_2 + F_4 F_1 + P_{24} + P_1$

**LOGIC LAYOUT**

LOGIC SECT. OR LINE SEL. TERM. L9 & N09-N79  
 DWG. NO. 505782 T DATE 6-62  
 DRAWN BY H. Mend. Ischn APP  
SH. 44



OPTIONAL



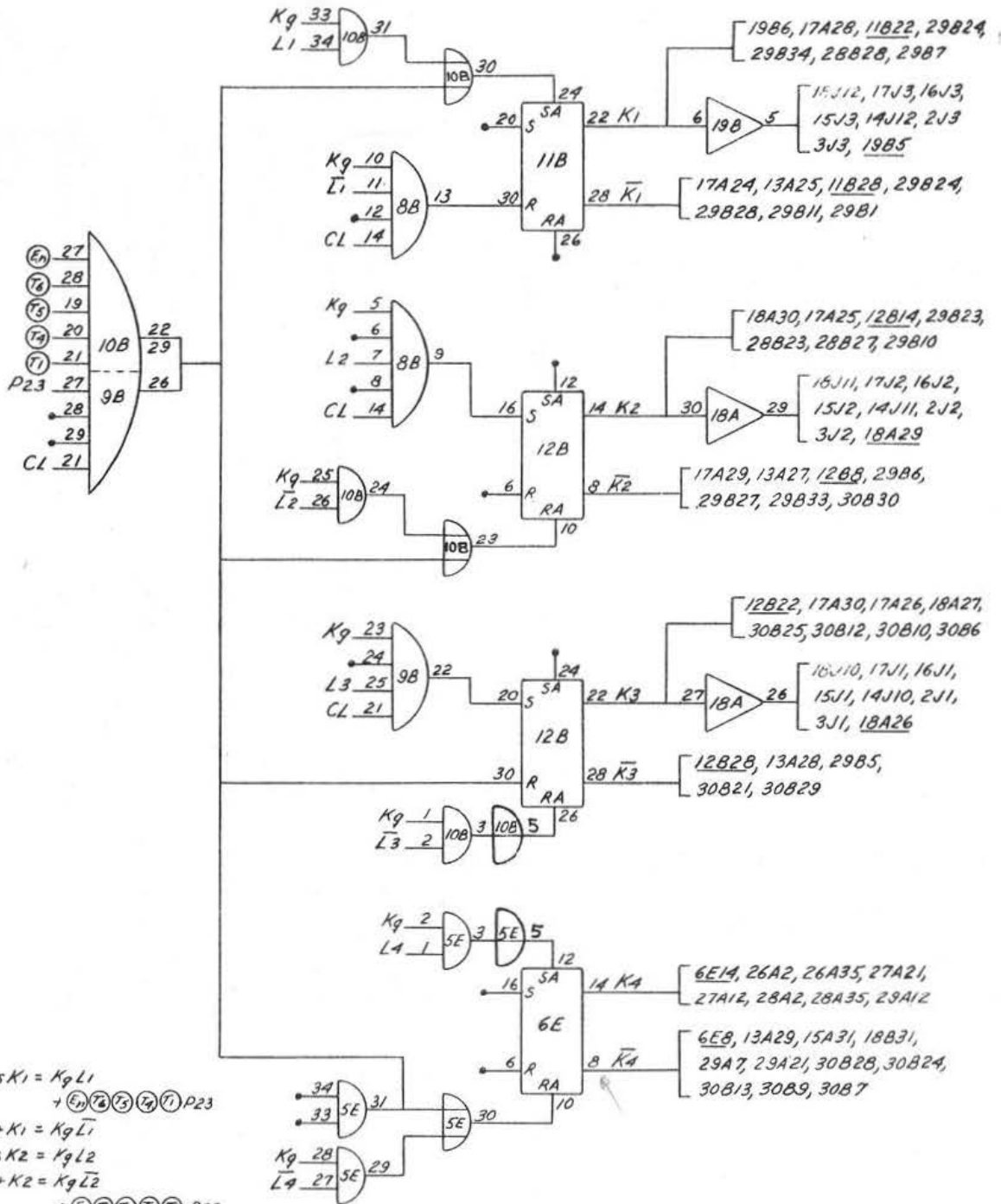
6-53

ADD ?  
K4  
30  
31  
15J 10

M09 =  $\bar{L}0 \bar{L}5 \bar{L}4$   
M19 =  $\bar{L}0 \bar{L}5 L4$   
M29 =  $\bar{L}0 L5 \bar{L}4$   
M39 =  $\bar{L}0 L5 L4$

M49 =  $L0 \bar{L}5 \bar{L}4$   
M59 =  $L0 \bar{L}5 L4$   
M69 =  $L0 L5 \bar{L}4$   
M79 =  $L0 L5 L4$

LOGIC LAYOUT  
LOGIC SECT. DR. LINE SEL. TERM M09-M79  
DWG. NO. 505782 T DATE 1-6-62  
DRAWN BY H. Mendelsohn APP. \_\_\_\_\_  
SH.45

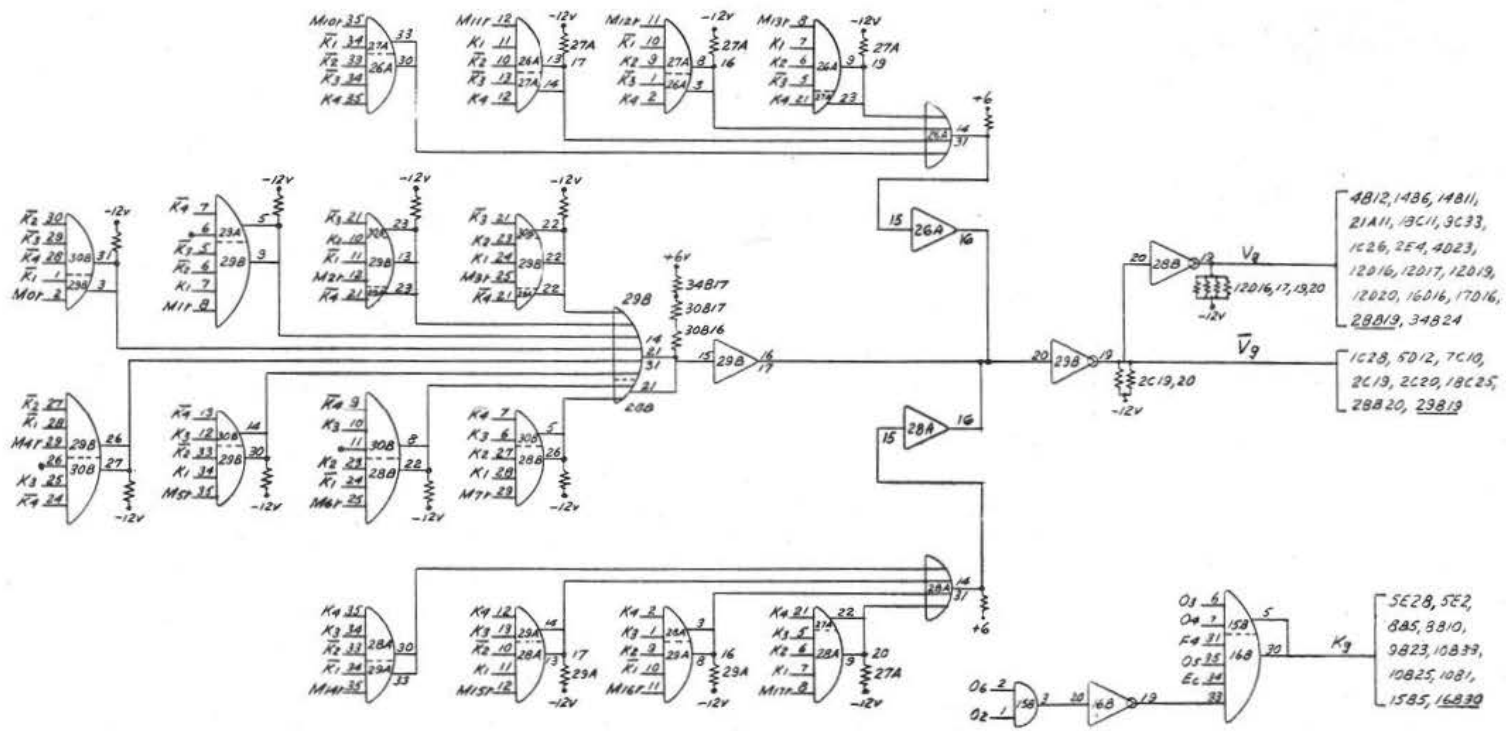


$S K_1 = K_9 L_1 + \textcircled{E_6} \textcircled{T_6} \textcircled{T_5} \textcircled{T_4} \textcircled{T_1} P_{23}$   
 $K_1 = K_9 \bar{L}_1$   
 $S K_2 = K_9 L_2 + \textcircled{E_6} \textcircled{T_6} \textcircled{T_5} \textcircled{T_4} \textcircled{T_1} P_{23}$   
 $K_2 = K_9 \bar{L}_2$   
 $S K_3 = K_9 L_3 + \textcircled{E_6} \textcircled{T_6} \textcircled{T_5} \textcircled{T_4} \textcircled{T_1} P_{23}$   
 $K_3 = K_9 \bar{L}_3 + \textcircled{E_6} \textcircled{T_6} \textcircled{T_5} \textcircled{T_4} \textcircled{T_1} P_{23}$   
 $S K_4 = K_9 L_4 + \textcircled{E_6} \textcircled{T_6} \textcircled{T_5} \textcircled{T_4} \textcircled{T_1} P_{23}$   
 $K_4 = K_9 \bar{L}_4 + \textcircled{E_6} \textcircled{T_6} \textcircled{T_5} \textcircled{T_4} \textcircled{T_1} P_{23}$

**LOGIC LAYOUT**

LOGIC SECT.          COM. LINE SEL.          TERM           
 DWG. NO. 505782 DATE 1-6-62  
 DRAWN BY H. Mendelsohn APP.         

SH. 46



$$\begin{aligned}
 Vg &= \bar{K}_4 \bar{K}_3 \bar{K}_2 \bar{K}_1 M_{0r} + \bar{K}_4 \bar{K}_3 \bar{K}_2 K_1 M_{1r} + \bar{K}_4 \bar{K}_3 K_2 \bar{K}_1 M_{2r} + \bar{K}_4 \bar{K}_3 K_2 K_1 M_{3r} \\
 &+ \bar{K}_4 K_3 \bar{K}_2 \bar{K}_1 M_{4r} + \bar{K}_4 K_3 K_2 \bar{K}_1 M_{5r} + \bar{K}_4 K_3 K_2 K_1 M_{6r} + \bar{K}_4 K_3 K_2 K_1 M_{7r} \\
 &+ K_4 \bar{K}_3 \bar{K}_2 \bar{K}_1 M_{10r} + K_4 \bar{K}_3 \bar{K}_2 K_1 M_{11r} + \dots + K_4 K_3 K_2 \bar{K}_1 M_{16r} + K_4 K_3 K_2 K_1 M_{17r} \\
 \bar{V}g &= (\bar{V}g) \\
 Kq &= E_c O_5 O_4 O_3 F_4 (\bar{O}_6 + \bar{O}_2)
 \end{aligned}$$

**LOGIC LAYOUT**

LOGIC SECT. COMA. LINE SEL. TERM Vg, Kq  
 DWG. NO. 5057B2 T DATE 1-3-62  
 DRAWN BY H. Monda'iso4n APP. \_\_\_\_\_  
 SH. 47

$$\begin{aligned}
sAw = & E_c \bar{R}_c \bar{O}_6 \bar{O}_4 O_3 \bar{O}_2 O_1 F_g \\
& + E_c \bar{R}_c \bar{O}_6 \bar{O}_5 O_4 O_3 \bar{O}_2 Z_g \\
& + E_c \bar{R}_c O_6 \bar{O}_5 \bar{O}_4 \bar{O}_3 \bar{O}_2 O_1 P_c \\
& + E_c \bar{R}_c O_6 \bar{O}_5 O_4 O_3 \bar{O}_2 O_1 (L_1 V_g + A_r \bar{V}_g) \\
& + E_c \bar{R}_c \bar{O}_6 O_5 \bar{O}_3 \bar{O}_2 (\bar{P}_{23} \bar{P}_2 L_1 + P_2 L_3 + P_{23} O_4 L_1) \\
& + E_c \bar{R}_c \bar{O}_6 O_5 \bar{O}_4 \bar{O}_3 O_2 \bar{P}_{23} A_e \\
& + \bar{O}_6 O_5 \bar{O}_4 \bar{O}_3 P_{23} A_r \\
& + E_c \bar{R}_c O_6 \bar{O}_5 \bar{O}_4 \bar{O}_3 \bar{O}_2 \bar{O}_1 F_g A_w \\
& + E_c \bar{R}_c \bar{O}_6 \bar{O}_5 \bar{O}_4 \bar{O}_3 \bar{O}_2 O_1 C_r \\
& + E_c \bar{P}_c \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 Z_g \\
& + A_r [E_c \bar{R}_c (\bar{O}_5 \bar{O}_4 \bar{O}_2 O_1 + \bar{O}_5 O_4 O_3 \bar{O}_2 + \bar{O}_6 O_5 \bar{O}_3 + O_6 \bar{O}_5 \bar{O}_4 \bar{O}_3 \bar{O}_2 \bar{O}_1 F_g + \bar{O}_6 \bar{O}_4 \bar{O}_2 O_1)]
\end{aligned}$$

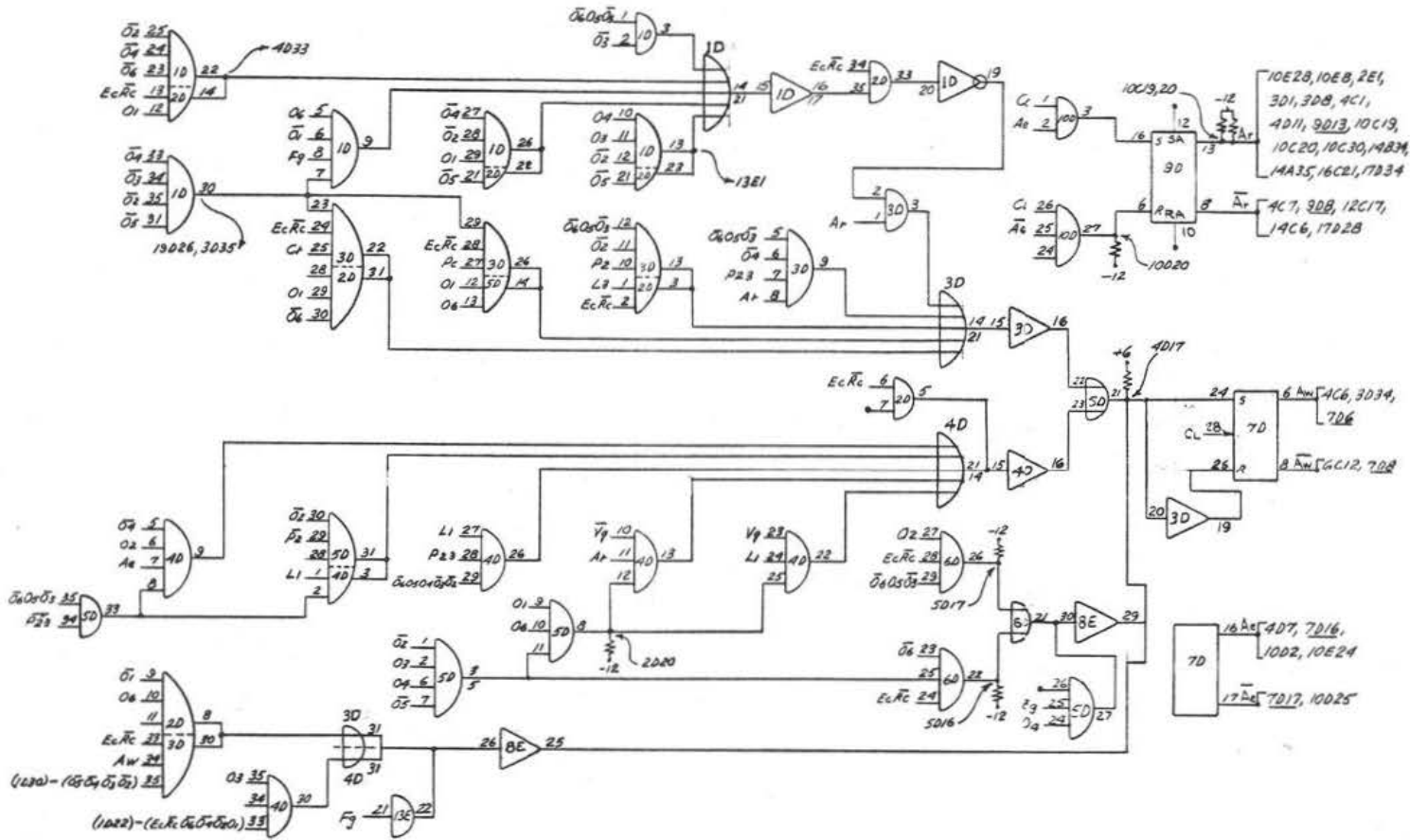
$$rAw = (\overline{sAw})$$

### LOGIC LAYOUT

LOGIC SECT. A-REGISTER TERM sAw  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mendelsohn APP. \_\_\_\_\_

SH.48

6-57



**LOGIC LAYOUT**

LOGIC SECT.	<u>1-REGISTER</u>	TEAM
DWG. NO.	<u>503782-1</u>	DATE
DRAWN BY	<u>H. Mandelstein</u>	APP.
		<u>SH. 40</u>



$$\begin{aligned}
sB_w &= E_c \bar{R}_c \bar{O}_6 \bar{O}_5 \bar{O}_4 O_3 O_2 F_g \\
&+ E_c \bar{R}_c \bar{O}_6 \bar{O}_5 O_4 O_3 O_2 Z_g \\
&+ E_c \bar{R}_c O_6 \bar{O}_5 \bar{O}_4 O_2 \bar{O}_1 F_g C_r \\
&+ E_c \bar{R}_c \bar{O}_6 O_5 \bar{O}_4 \bar{O}_3 \bar{O}_2 \bar{P}_2 L_2 \\
&+ E_c \bar{R}_c \bar{O}_6 O_5 \bar{O}_3 O_2 (\bar{P}_{23} B_e + P_{23} L_3) \\
&+ E_c \bar{R}_c \bar{O}_6 \bar{O}_5 \bar{O}_4 \bar{O}_3 O_2 C_r \\
&+ \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 (E_c \bar{P}_2 \bar{P}_3 L_2 + E_c P_3 \bar{L}_5 \bar{L}_4 + E_c P_3 L_5 L_4 + \bar{E}_c P_2 L_4) \\
&+ \bar{P}_1 B_r [E_c \bar{R}_c (\bar{O}_6 \bar{O}_5 O_3 O_2 + \bar{O}_6 O_5 \bar{O}_3 + O_6 \bar{O}_5 \bar{O}_4 O_2 F_g + \bar{O}_5 \bar{O}_4 \bar{O}_3 O_2)]
\end{aligned}$$

6-58

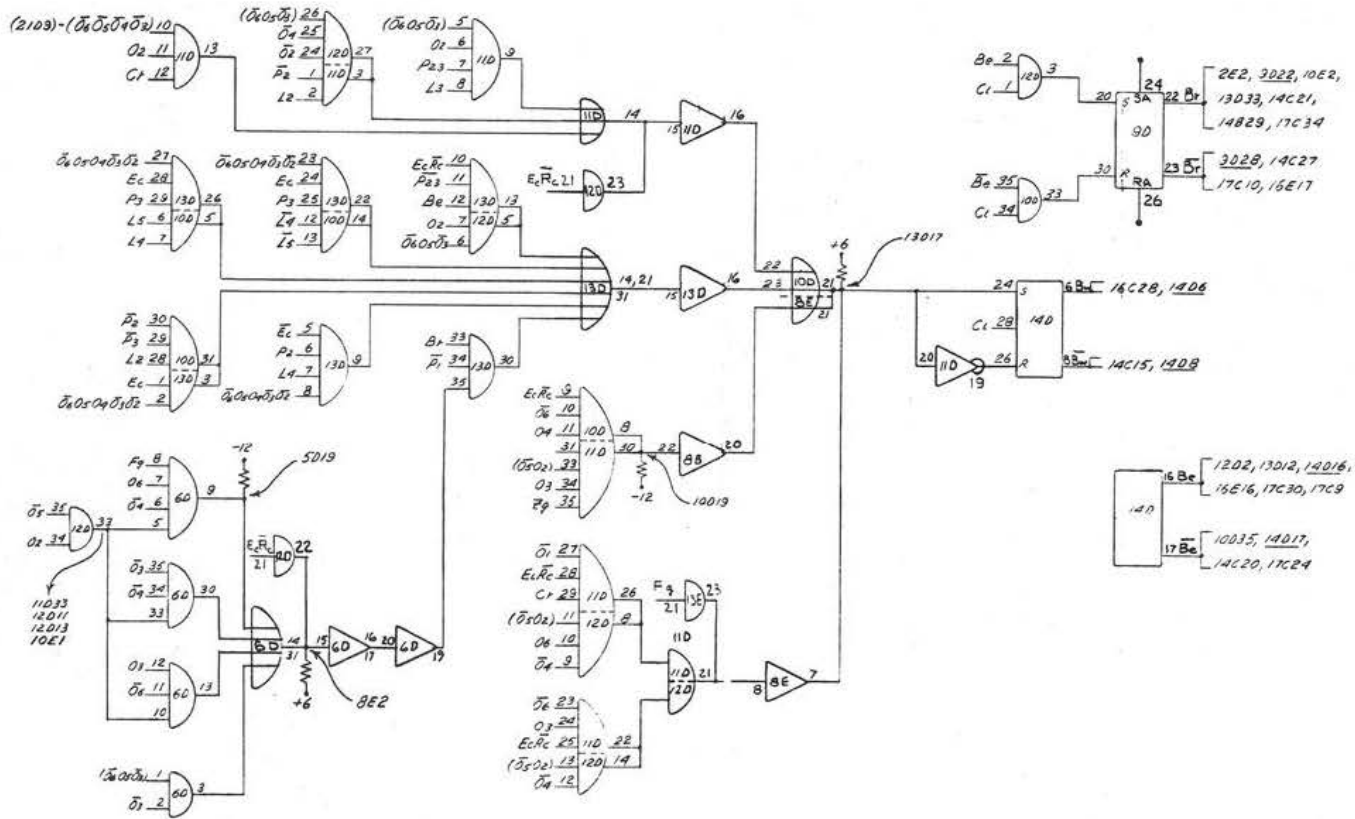
$$rB_w = (\overline{sB_w})$$

### LOGIC LAYOUT

LOGIC SECT. B REGISTER TERM Bw  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mond. Sahni APP. \_\_\_\_\_

SH. 50

6-59



LOGIC LAYOUT  
 LOGIC SECT B-REGISTER TERM B-5, B-8  
 DWS NO. 50738 DATE 1-6-62  
 DRAWN BY HANSEN DATE  
 APP. SH. 51

$$\begin{aligned}
sC_w &= E_c \bar{R}_c \bar{O}_6 \bar{O}_5 \bar{O}_4 O_3 \bar{O}_2 \bar{O}_1 F_g \\
&+ E_c \bar{R}_c \bar{O}_6 \bar{O}_5 \bar{O}_4 \bar{O}_3 I_g \\
&+ P_{24} C_w \\
&+ E_c \bar{R}_c O_5 \bar{O}_4 Z_g \\
&+ E_c \bar{R}_c \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 \bar{O}_1 D_g \\
&+ \bar{P}_{24} C_r [E_c \bar{R}_c (\bar{O}_5 \bar{O}_4 O_3 \bar{O}_2 \bar{O}_1 + \bar{O}_6 \bar{O}_5 \bar{O}_4 \bar{O}_3 + O_5 \bar{O}_4 + \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 \bar{O}_1)]
\end{aligned}$$

$$rC_w = (\bar{sC_w})$$

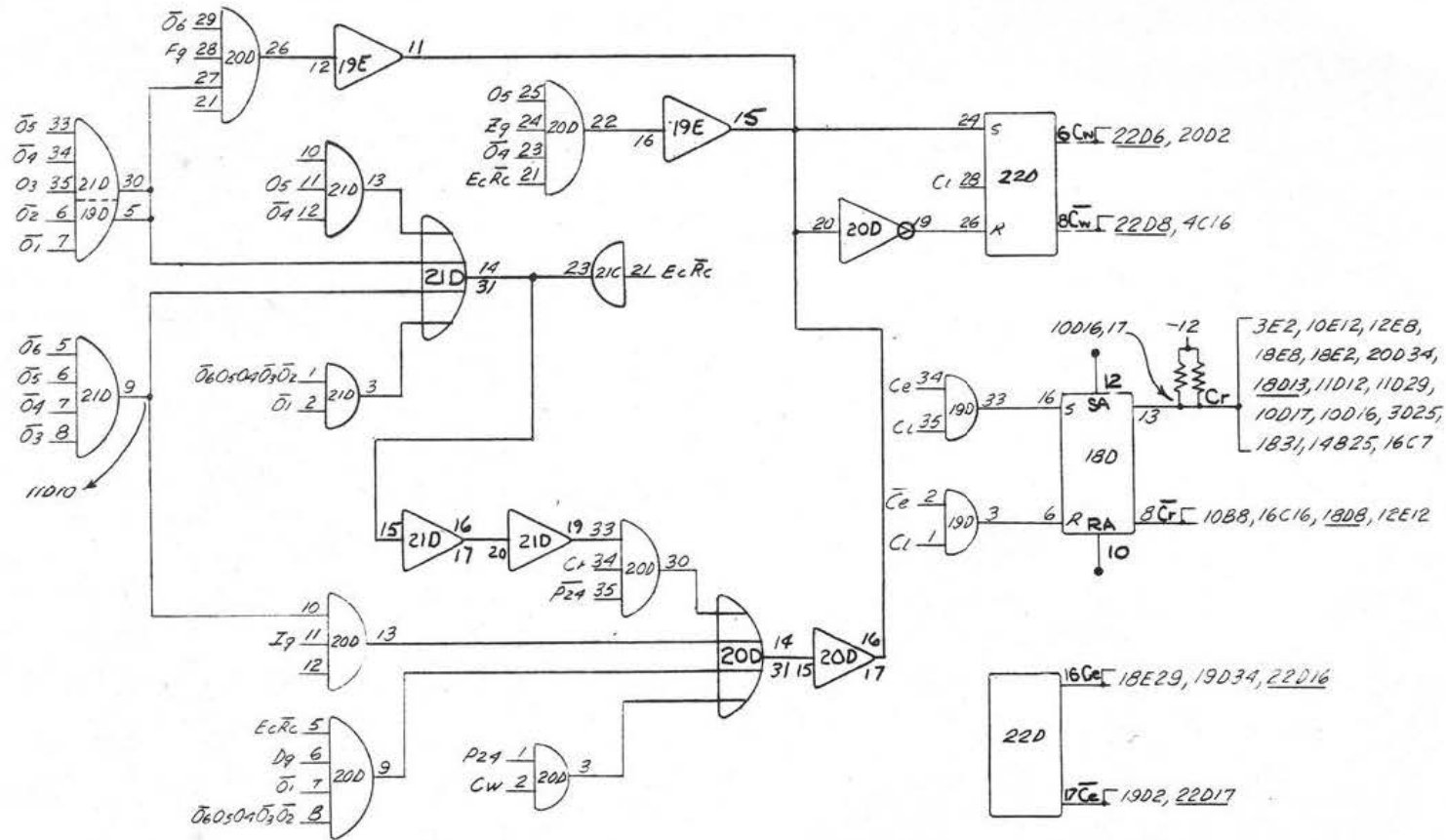
09-9

### LOGIC LAYOUT

LOGIC SECT. C REGISTER TERM CW  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. H. H. H. H. H. APP. \_\_\_\_\_

SH. 52

6-61

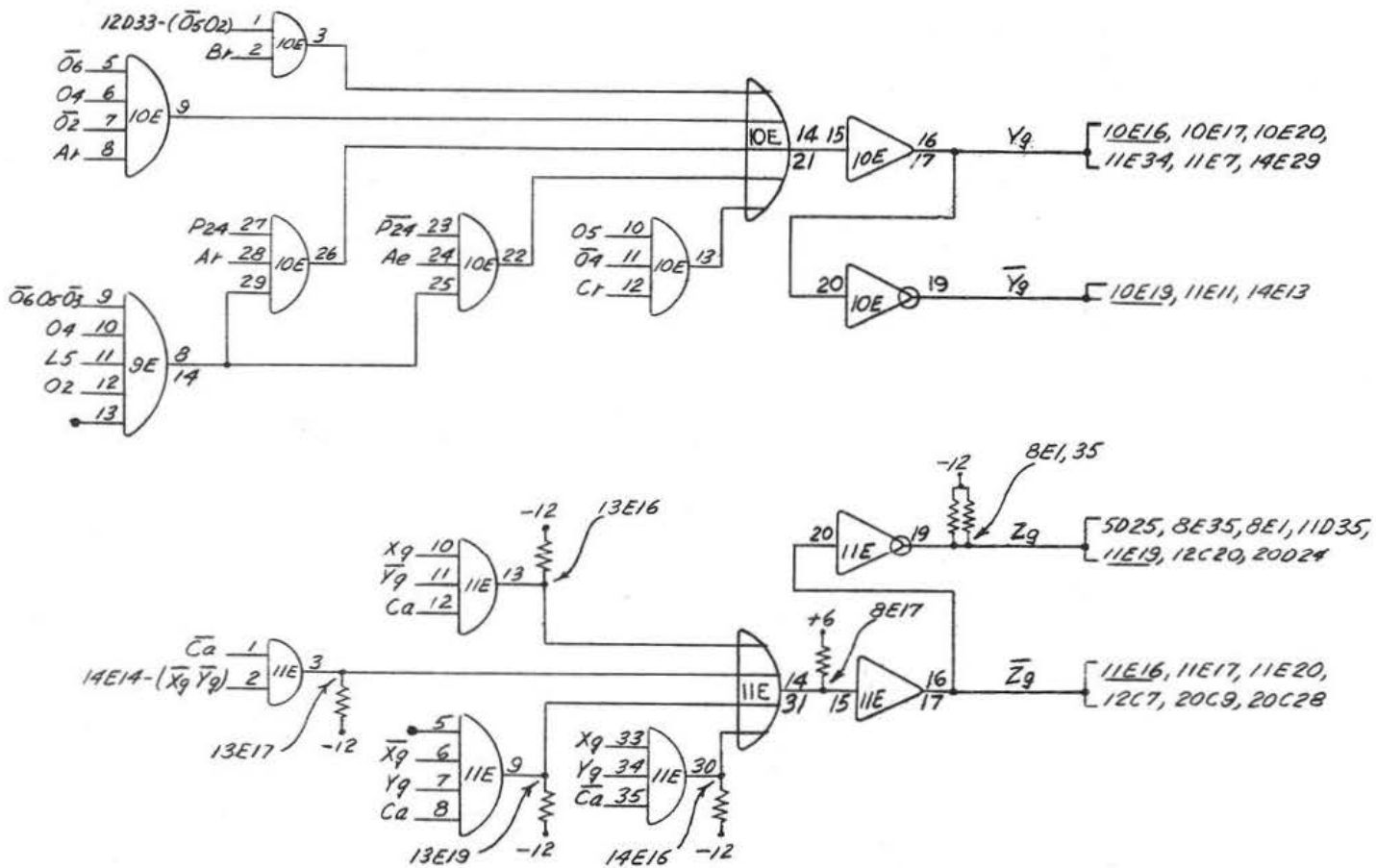


### LOGIC LAYOUT

LOGIC SECT. C-REGISTER TERM Cw, Co, Cr  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mendelsohn APP. \_\_\_\_\_

SH. 53

6-62



$$Y_9 = \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 L_5 (\bar{P}_{24} A_e + P_{24} A_r) + \bar{O}_6 O_4 \bar{O}_2 A_r + \bar{O}_5 O_2 B_r + O_5 \bar{O}_4 C_r$$

$$\bar{Y}_9 = (Y_9)$$

$$\bar{Z}_9 = X_9 Y_9 \bar{C}_a + X_9 \bar{Y}_9 C_a + \bar{X}_9 Y_9 C_a + \bar{X}_9 \bar{Y}_9 \bar{C}_a$$

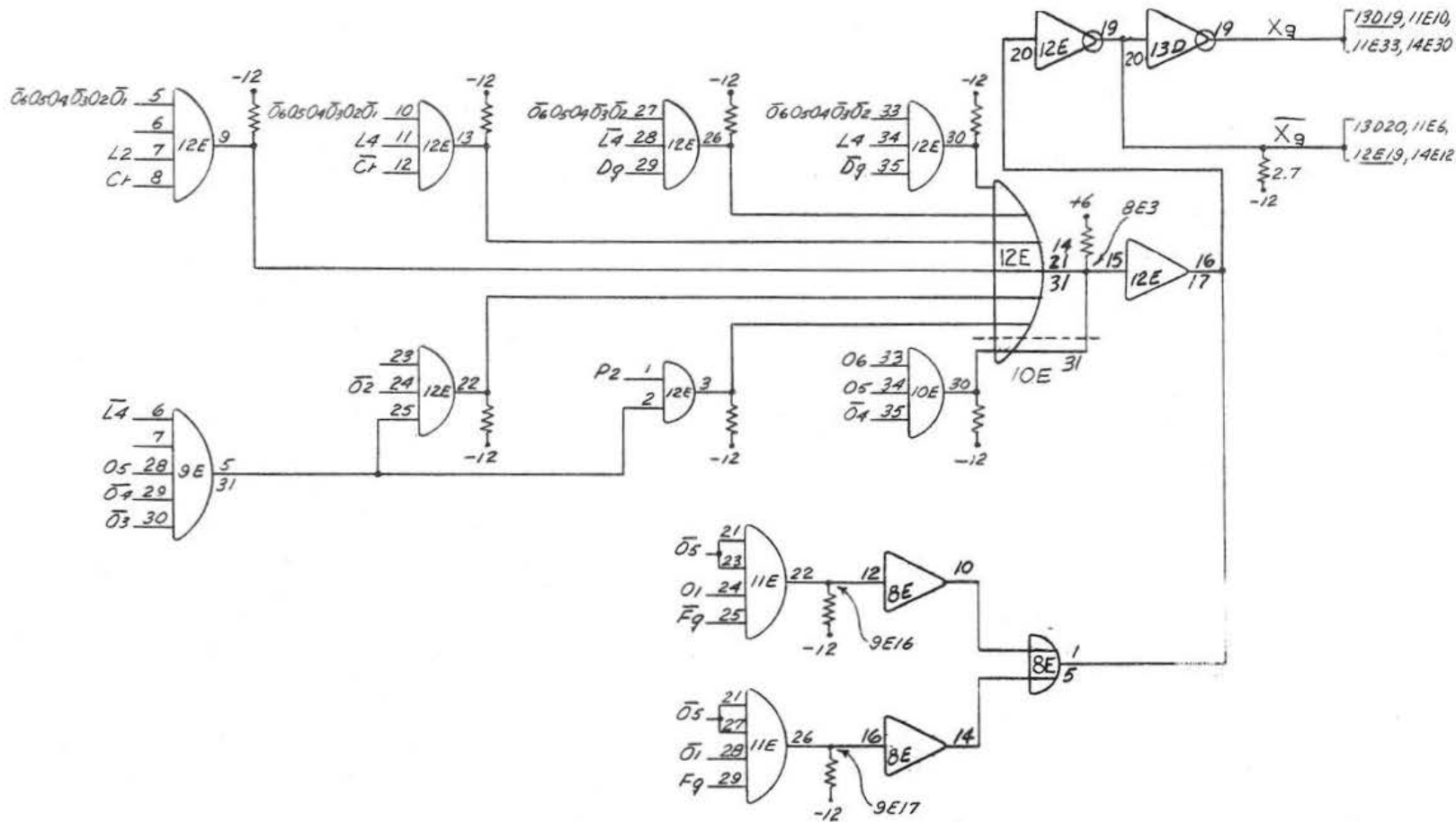
$$Z_9 = (\bar{Z}_9)$$

### LOGIC LAYOUT

LOGIC SECT. ADDER TERM Y9 & Z9  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mendelsohn APP. \_\_\_\_\_

SH.54

6-63



$$Xq = \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 (\bar{L}_4 Dq + L_4 \bar{D}q) + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 (L_2 C+ + L_4 \bar{C}+) + \bar{O}_5 \bar{O}_1 Fq + \bar{O}_5 O_1 \bar{F}q + O_6 O_5 \bar{O}_4 + O_5 \bar{O}_4 \bar{O}_3 \bar{L}_4 (\bar{O}_2 + P_2)$$

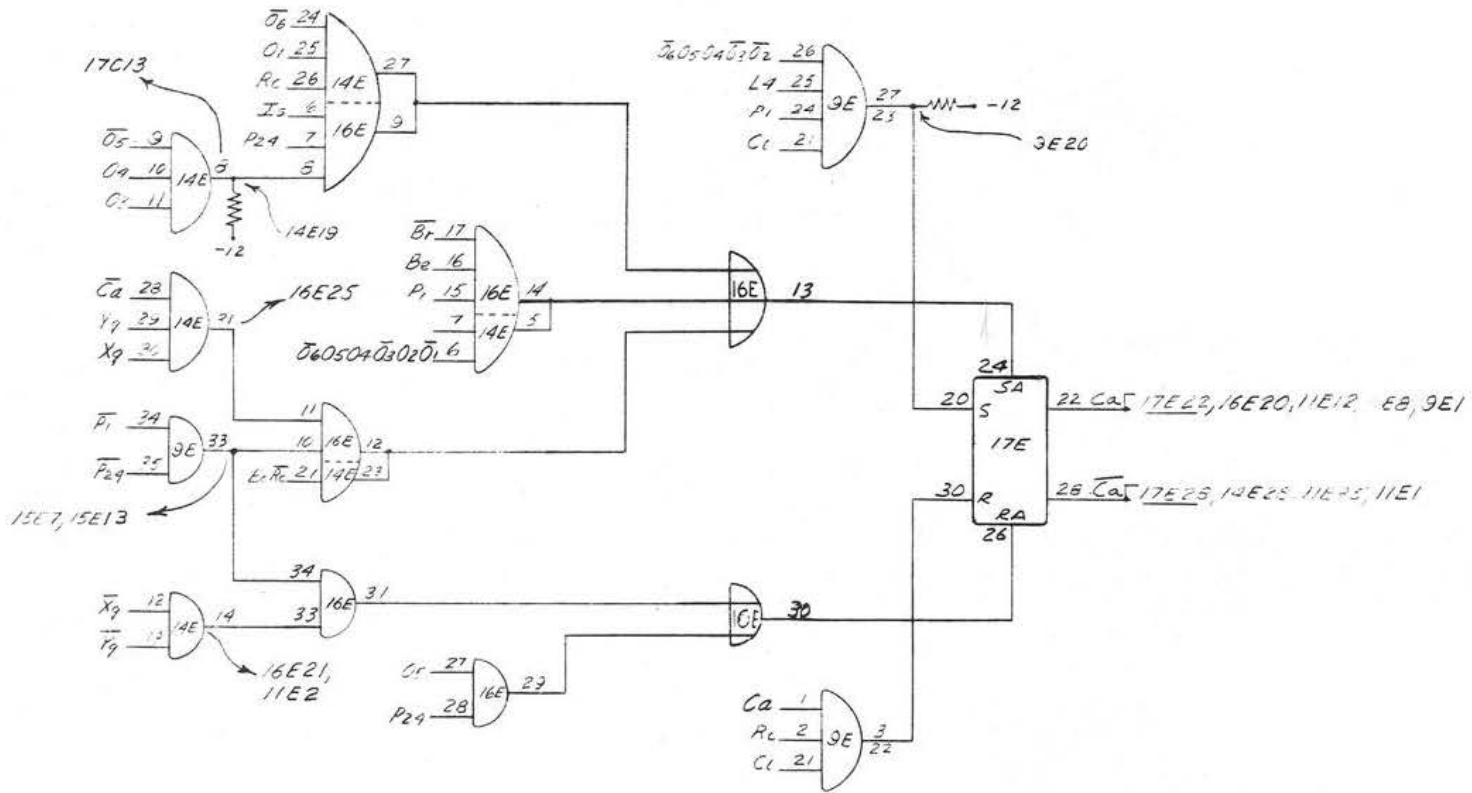
$$\bar{X}q = \overline{(Xq)}$$

**LOGIC LAYOUT**

LOGIC SECT.	ADDER	TERM	Xq
DWG. NO.	505782 T	DATE	1-6-62
DRAWN BY	H. Mendelsohn	APP.	

**SH. 55**

6-64

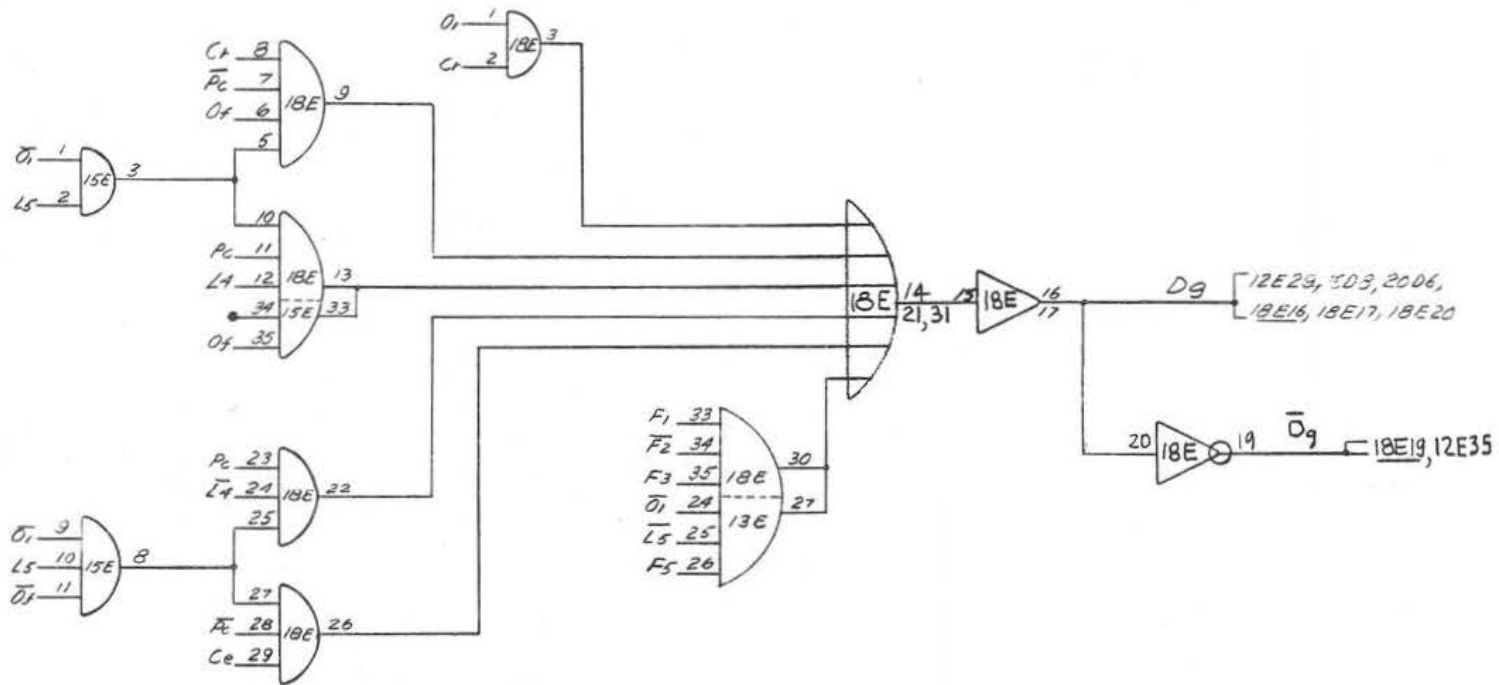


$$\begin{aligned}
 SCa &= P_1 P_{24} \bar{C}_a E_c \bar{R}_c X_q Y_q + P_{24} R_c I_s \bar{O}_6 \bar{O}_5 O_4 O_3 O_1 \\
 &\quad + \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 P_1 L_4 + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 P_1 B + \bar{B}_r \\
 +Ca &= \bar{P}_1 \bar{P}_{24} \bar{X}_q \bar{Y}_q + C_a R_c + O_5 P_{24}
 \end{aligned}$$

**LOGIC LAYOUT**

LOGIC SECT. ADDER      TERN. Ca  
 DWG. NO. 505782 T      DATE 1-6-62  
 DRAWN BY H. J. K. [unclear]      APP. [unclear]  
SH. 56

6-65



$$D_9 = O_1 C_1 + \overline{O_1} L_5 (O_f \overline{P_c} C_1 + O_f P_c L_4 + \overline{O_f} P_c \overline{L_4} + \overline{O_f} P_c C_e) + \overline{O_1} \overline{L_5} F_5 F_3 \overline{F_2} F_1$$

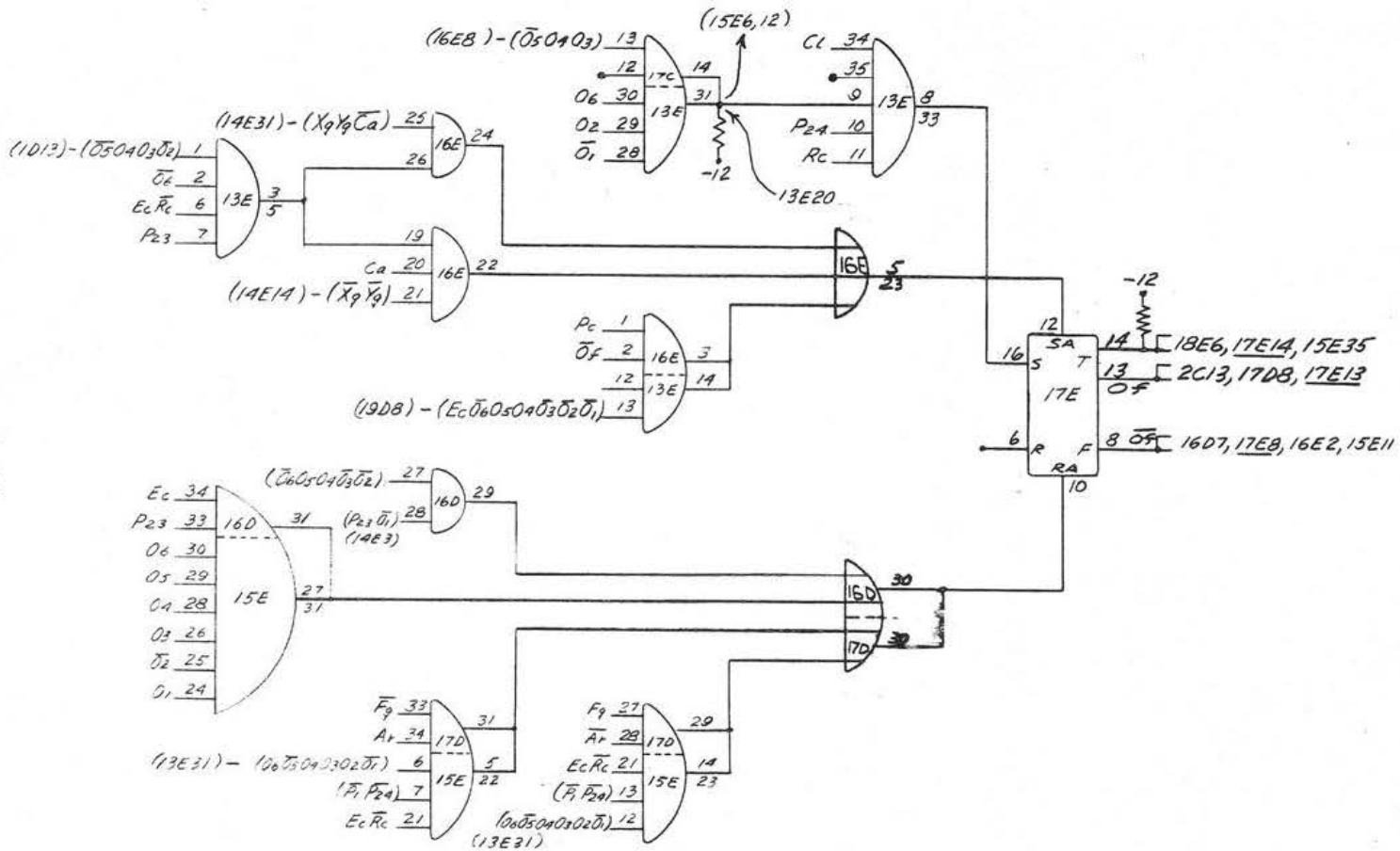
$$\overline{D_9} = (\overline{D_9})$$

**LOGIC LAYOUT**

LOGIC SECT. ADDER TERM. D9  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Hendrickson APP. \_\_\_\_\_  
 SH. 57



99-9

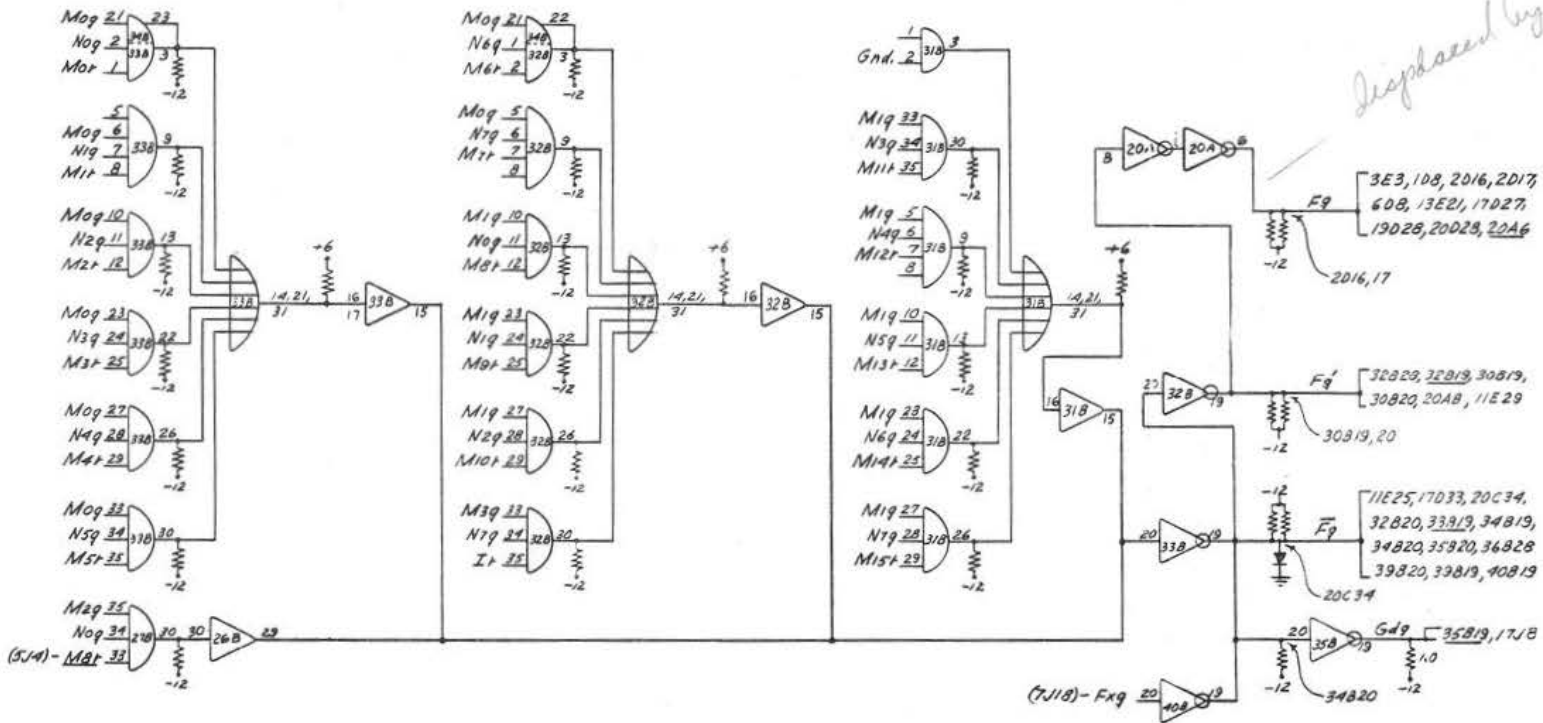


$$\begin{aligned}
 SOF &= P_{23} E_c \bar{R}_c \bar{O}_6 \bar{O}_5 O_4 O_3 \bar{O}_2 (\bar{X}_9 \bar{Y}_9 C_a + X_9 Y_9 \bar{C}_a) \\
 &\quad + \bar{O}_F E_c \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 \bar{O}_1 P_c + P_{24} R_c O_6 \bar{O}_5 O_4 O_3 O_2 \bar{O}_1 \\
 OF &= P_{23} E_c O_6 O_5 O_4 O_3 \bar{O}_2 \bar{O}_1 + P_{23} \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 \bar{O}_1 \\
 &\quad + \bar{P}_1 \bar{P}_{24} E_c \bar{R}_c O_6 \bar{O}_5 O_4 O_3 O_2 \bar{O}_1 (F_9 \bar{A}_r + \bar{F}_9 A_r)
 \end{aligned}$$

**LOGIC LAYOUT**

LOGIC SECT. ADDER      TERM OF  
 DWG. NO. 505782 T      DATE 1-6-62  
 DRAWN BY H. Mendelsohn      APP. \_\_\_\_\_  
SH.58

6-67

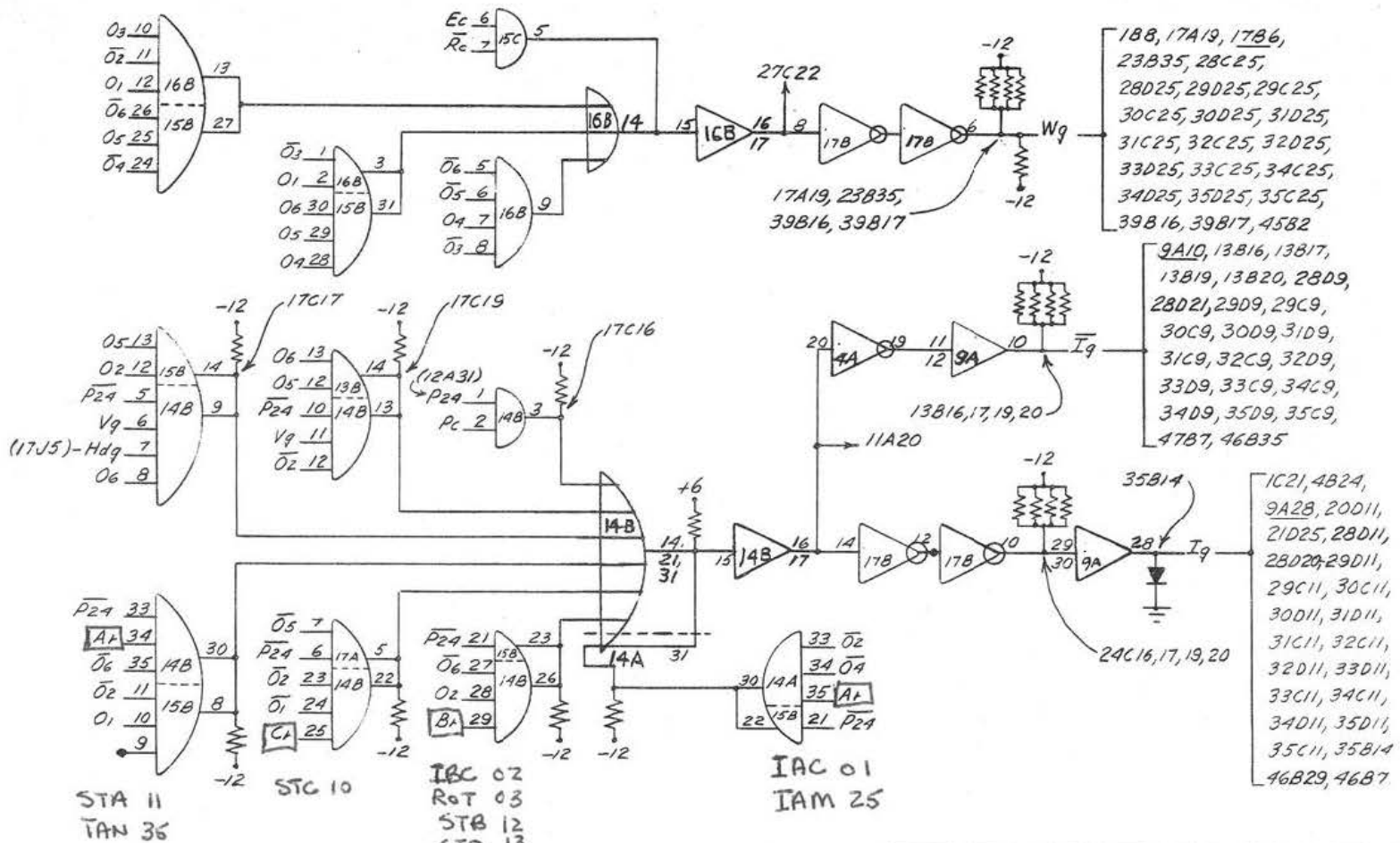


$$Fg = \text{Mog Nog Mor} + \text{Mog Nig Mir} + \dots + \text{Mig Nig Mir} + \text{M39 Nig I} + \text{Fxg}$$

### LOGIC LAYOUT

LOGIC SECT. DATA TRANS. GATES TERM Fg  
 DWS. NO. 505782 T DATE 1-3-62  
 DRAWN BY H. M. K. / S. W. A. P. A.  
 SH. 53

89-9



$$Wg = (\bar{O}_6 \bar{O}_5 O_4 \bar{O}_3 + O_6 O_5 O_4 \bar{O}_3 O_1 + \bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1) Ec \bar{R}_c$$

$$Iq = \bar{P}_{24} \bar{O}_5 \bar{O}_2 \bar{O}_1 C_1 + \bar{P}_{24} \bar{O}_6 \bar{O}_2 O_1 A_1 + \bar{P}_{24} \bar{O}_6 O_2 B_1 + \bar{P}_{24} \bar{O}_4 \bar{O}_2 A_1 + \bar{P}_{24} O_6 O_5 \bar{O}_2 V_9 + \bar{P}_{24} O_6 O_5 O_2 V_9 Hd_9 + P_{24} P_c$$

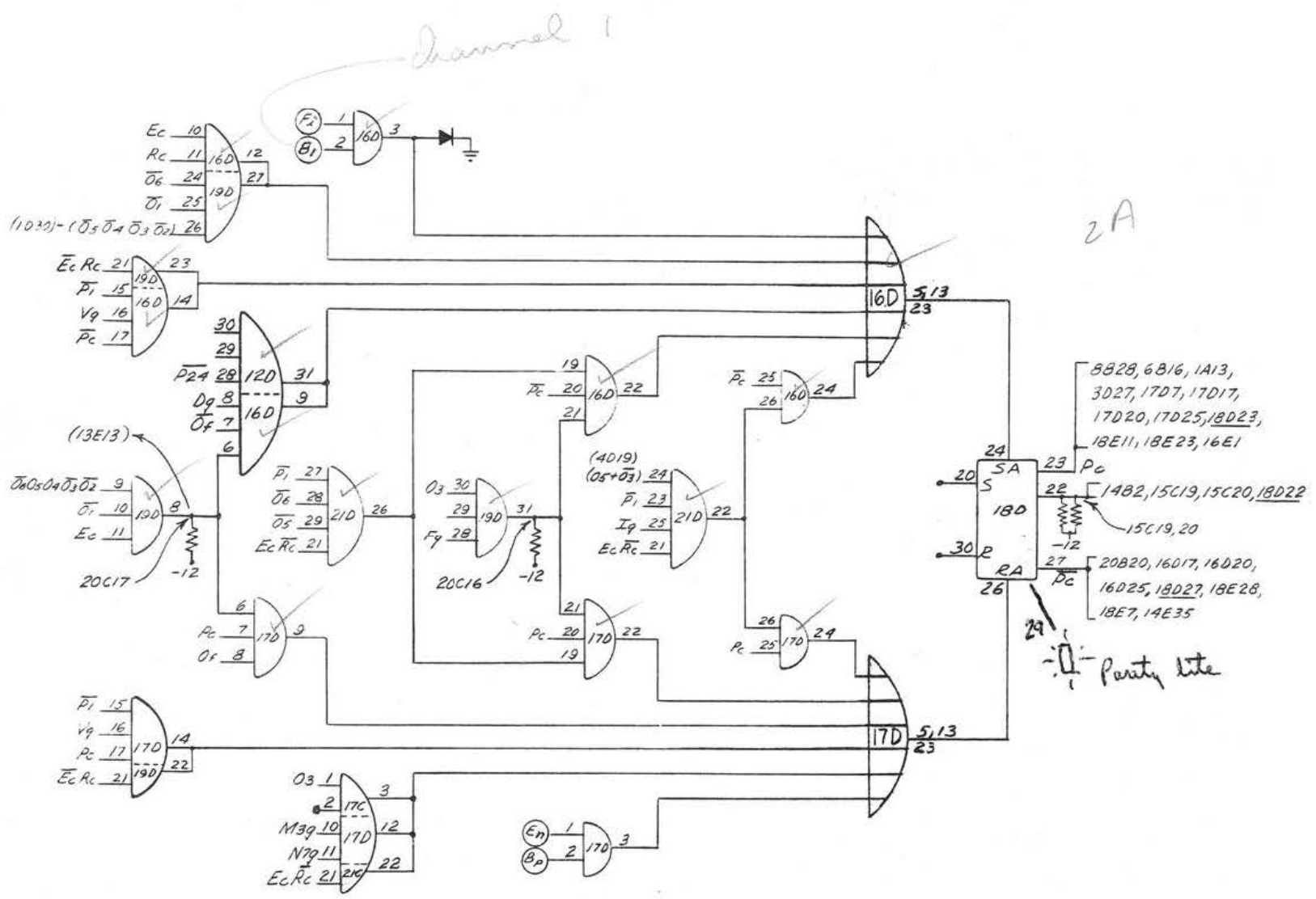
$$\bar{I}_q = (\bar{I}_q)$$

### LOGIC LAYOUT

LOGIC SECT. DATA TRANS. GATES TERM Wg & Iq  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mordtschuh APP. \_\_\_\_\_

SH.60

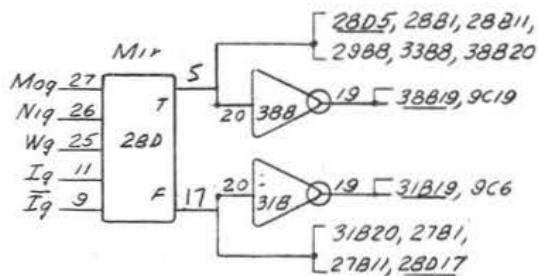
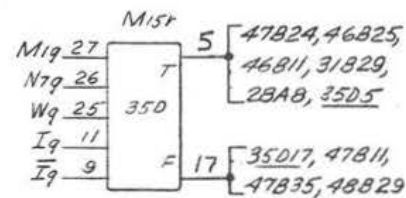
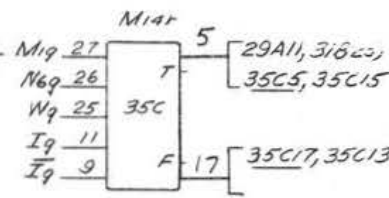
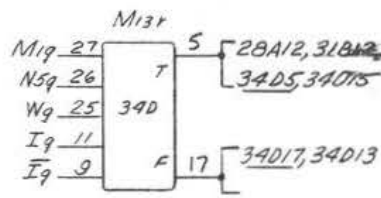
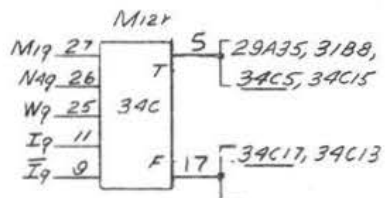
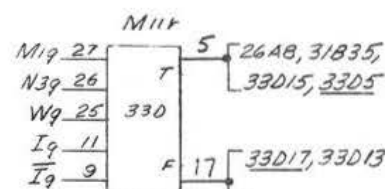
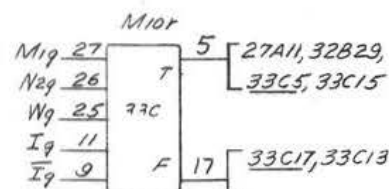
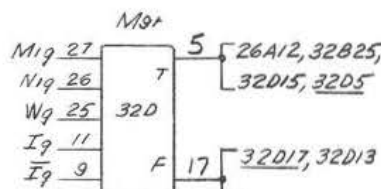
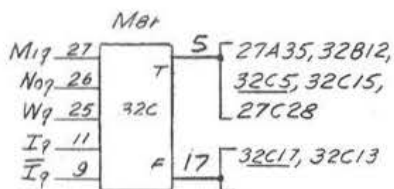
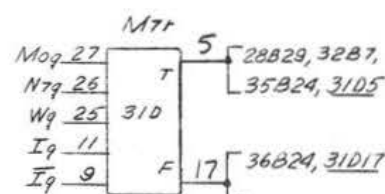
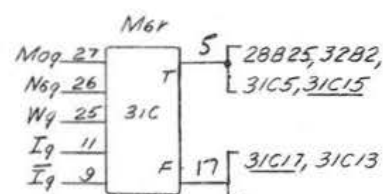
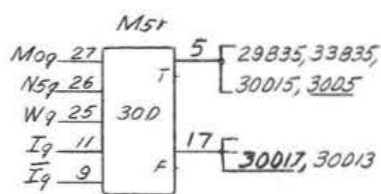
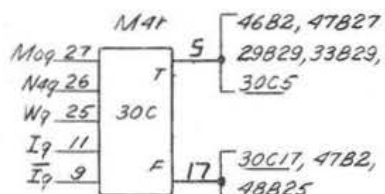
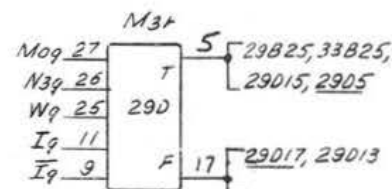
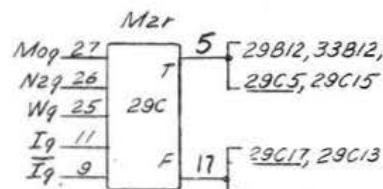
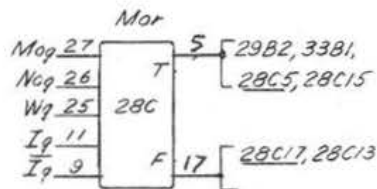
69-9



$$\begin{aligned}
 sPc &= EcRc\bar{P}_i\bar{O}_5O_3I_9Pc + \bar{P}_iEcRc\bar{O}_6\bar{O}_5O_3F_9Pc + \bar{P}_iEcRcV_9Pc \\
 &+ \bar{P}_2\bar{A}Ec\bar{O}_6O_5O_4\bar{O}_3\bar{O}_2\bar{O}_1\bar{O}_7D_9 + (\bar{F}_1)(\bar{B}_1) + EcRc\bar{O}_6\bar{O}_5O_4\bar{O}_3\bar{O}_2\bar{O}_1 \\
 tPc &= EcRc\bar{P}_i\bar{O}_5O_3I_9Pc + \bar{P}_iEcRc\bar{O}_6\bar{O}_5O_3F_9Pc + M39N79EcRcO_3 \\
 &+ \bar{P}_iEcRcV_9Pc + (E_n)(B_n) + Ec\bar{O}_6O_5O_4\bar{O}_3\bar{O}_2\bar{O}_1O_7Pc
 \end{aligned}$$

**LOGIC LAYOUT**  
 LOGIC SECT. DATA TRANSFER TERM Pc  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. J. Mendelsohn APP. \_\_\_\_\_  
 SH 61

6-70

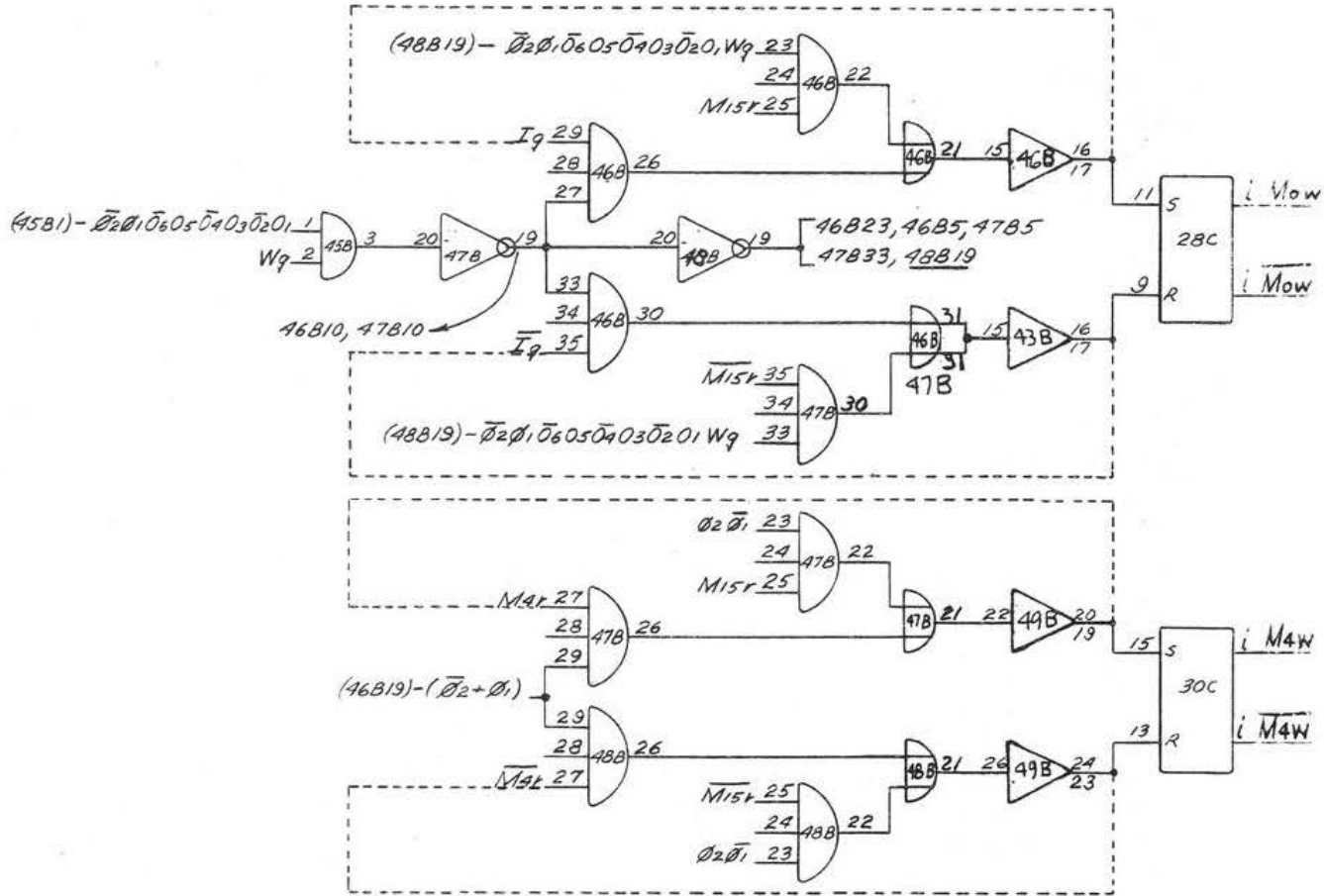


### LOGIC LAYOUT

LOGIC SECT. MEMORY LINES TERM \_\_\_\_\_  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mandelsohn APP \_\_\_\_\_

SH 62

6-71



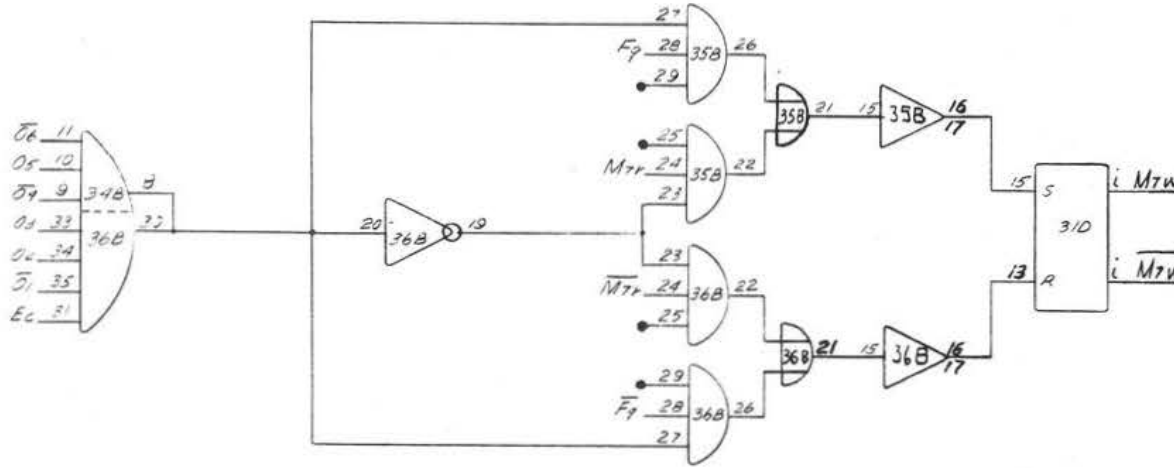
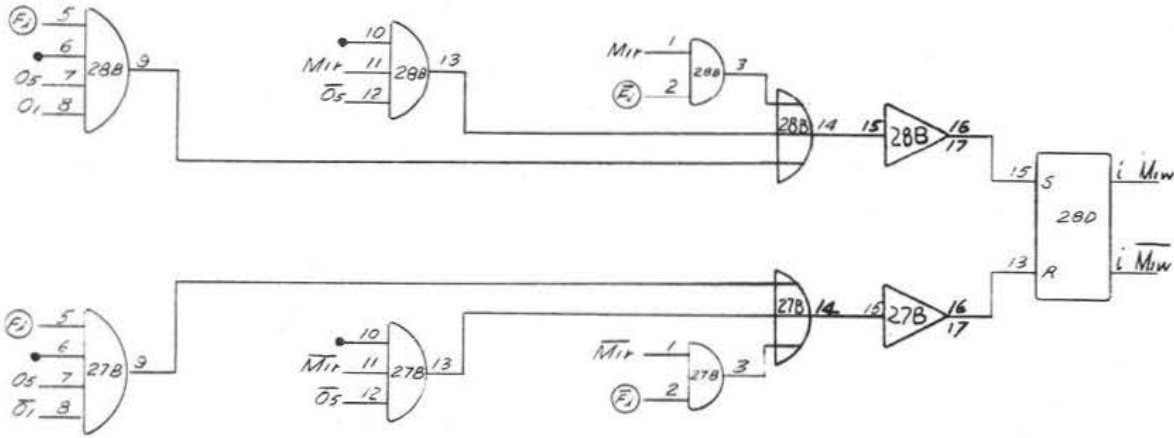
$$\begin{aligned}
 S Mow &= M0q N0q Wq [\bar{\theta}_2 \bar{\theta}_1 (\bar{\theta}_6 \bar{\theta}_5 \bar{\theta}_4 \bar{\theta}_3 \bar{\theta}_2 \theta_1) M15r + Wq \bar{\theta}_2 \bar{\theta}_1 (\bar{\theta}_6 \bar{\theta}_5 \bar{\theta}_4 \bar{\theta}_3 \bar{\theta}_2 \theta_1) Iq] + \dots \\
 r Mow &= M0q N0q Wq [\bar{\theta}_2 \bar{\theta}_1 (\bar{\theta}_6 \bar{\theta}_5 \bar{\theta}_4 \bar{\theta}_3 \bar{\theta}_2 \theta_1) \bar{M15r} + Wq \bar{\theta}_2 \bar{\theta}_1 (\bar{\theta}_6 \bar{\theta}_5 \bar{\theta}_4 \bar{\theta}_3 \bar{\theta}_2 \theta_1) \bar{Iq}] + \dots \\
 S M4w &= \dots + [M0q N4q Wq] [\bar{\theta}_2 \bar{\theta}_1 M15r + (\bar{\theta}_2 + \theta_1) M4r] \\
 r M4w &= \dots + [M0q N4q Wq] [\bar{\theta}_2 \bar{\theta}_1 \bar{M15r} + (\bar{\theta}_2 + \theta_1) \bar{M4r}]
 \end{aligned}$$

**LOGIC LAYOUT**

LOGIC SECT. MEMORY LINES TERM Mow, M4w  
 DWG. NO. 505782 T DATE 1-6-72  
 DRAWN BY H. H. ... APP

SH. 63

6-72

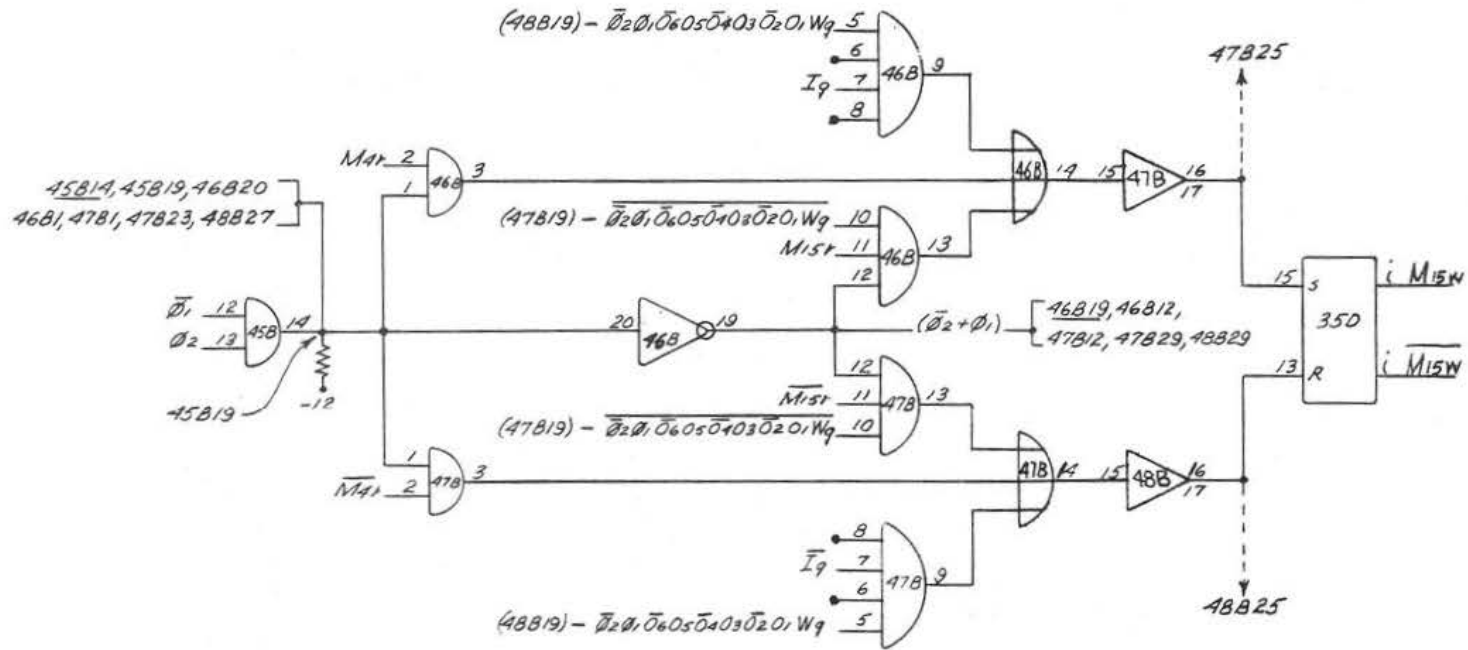


$$\begin{aligned}
 sM_{1w} &= M_{0q}N_{1q}W_qI_q + [M_{0q}N_{1q}W_q][\overline{M_{1r}}(\overline{O_5}) + (O_5)O_1] \\
 iM_{1w} &= iM_{0q}N_{1q}W_q\overline{I_q} + [M_{0q}N_{1q}W_q][\overline{M_{1r}}(O_5) + (O_5)\overline{O_1}] \\
 sM_{7w} &= M_{0q}N_{7q}W_qI_q + [M_{0q}N_{7q}W_q][\overline{M_{7r}}(\overline{O_6}O_5O_7O_3O_2\overline{O_1}Ec) + (\overline{O_6}O_5\overline{O_7}O_3O_2\overline{O_1}Ec)F_q] \\
 iM_{7w} &= iM_{0q}N_{7q}W_q\overline{I_q} + [M_{0q}N_{7q}W_q][\overline{M_{7r}}(\overline{O_6}O_5\overline{O_7}O_3O_2\overline{O_1}Ec) + (\overline{O_6}O_5\overline{O_7}O_3O_2\overline{O_1}Ec)F_q]
 \end{aligned}$$

**LOGIC LAYOUT**

LOGIC SECT. MEMORY LINES TERM  $M_{1w}$  &  $M_{7w}$   
 DWG. NO. 505782 T DATE 1-8-62  
 DRAWN BY H. J. ... APP. ...  
 SH. 64

6-73



$$SM_{15W} = \overline{\overline{M_{1q} N_{7q} W_q}} [\overline{\phi_2 \bar{\phi}_1} M_{4r} + \overline{\phi_2 \phi_1} (\overline{\phi_6 \phi_5 \phi_4 \phi_3 \phi_2 \phi_1}) W_q I_q] + (\overline{\phi_2} + \phi_1) \overline{W_q \phi_2 \phi_1} (\overline{\phi_6 \phi_5 \phi_4 \phi_3 \phi_2 \phi_1}) M_{15t}$$

$$+ M_{15W} = \overline{\overline{M_{1q} N_{7q} W_q}} [\overline{\phi_2 \bar{\phi}_1} \bar{M}_{4r} + \overline{\phi_2 \phi_1} (\overline{\phi_6 \phi_5 \phi_4 \phi_3 \phi_2 \phi_1}) W_q \bar{I}_q] + (\overline{\phi_2} + \phi_1) \overline{W_q \phi_2 \phi_1} (\overline{\phi_6 \phi_5 \phi_4 \phi_3 \phi_2 \phi_1}) \bar{M}_{15t}$$

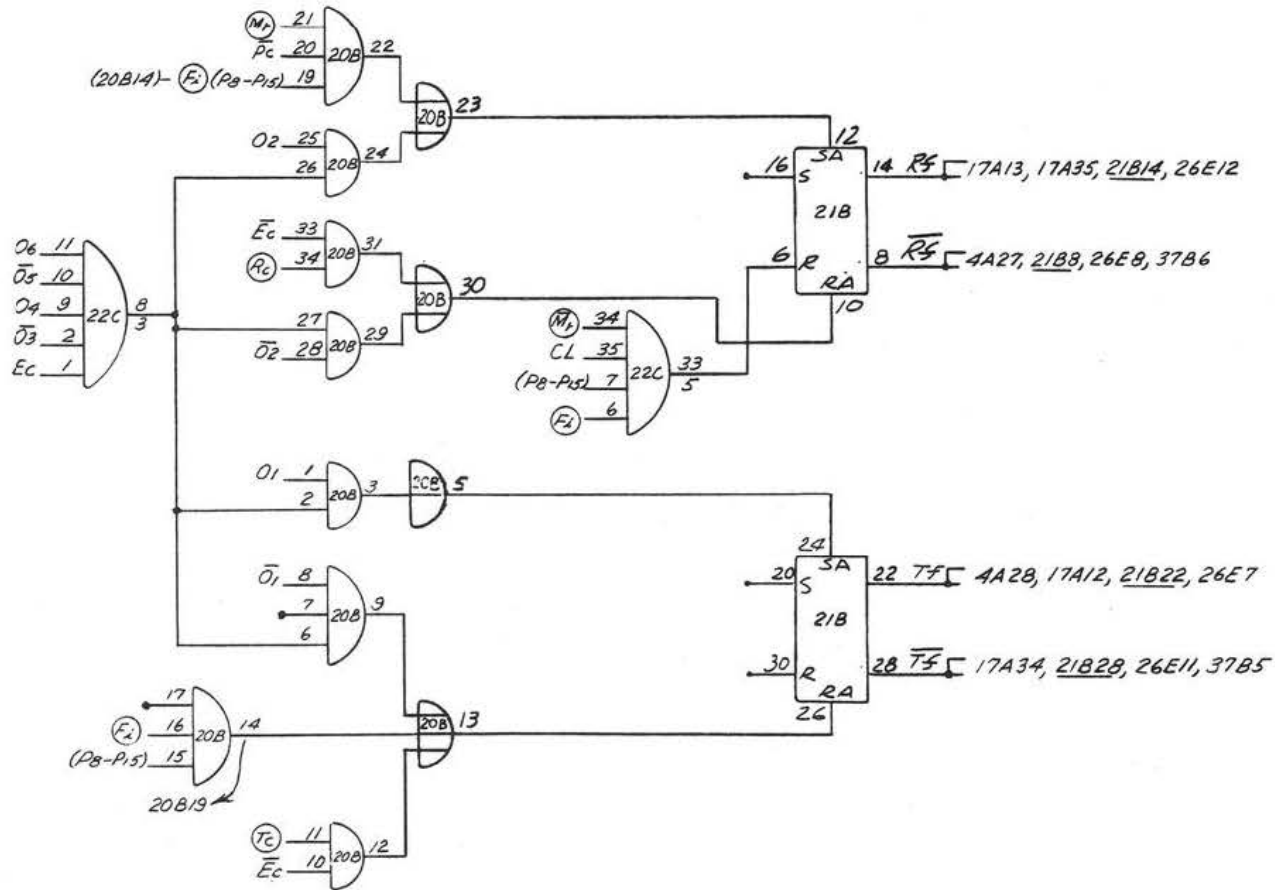
**LOGIC LAYOUT**

LOGIC SECT.	MEMORY LINES	TERM	M15W
DWG. NO.	505782 T	DATE	1-6-62
DRAWN BY	H. Mendelsohn	APP.	

SH. 65



6-74



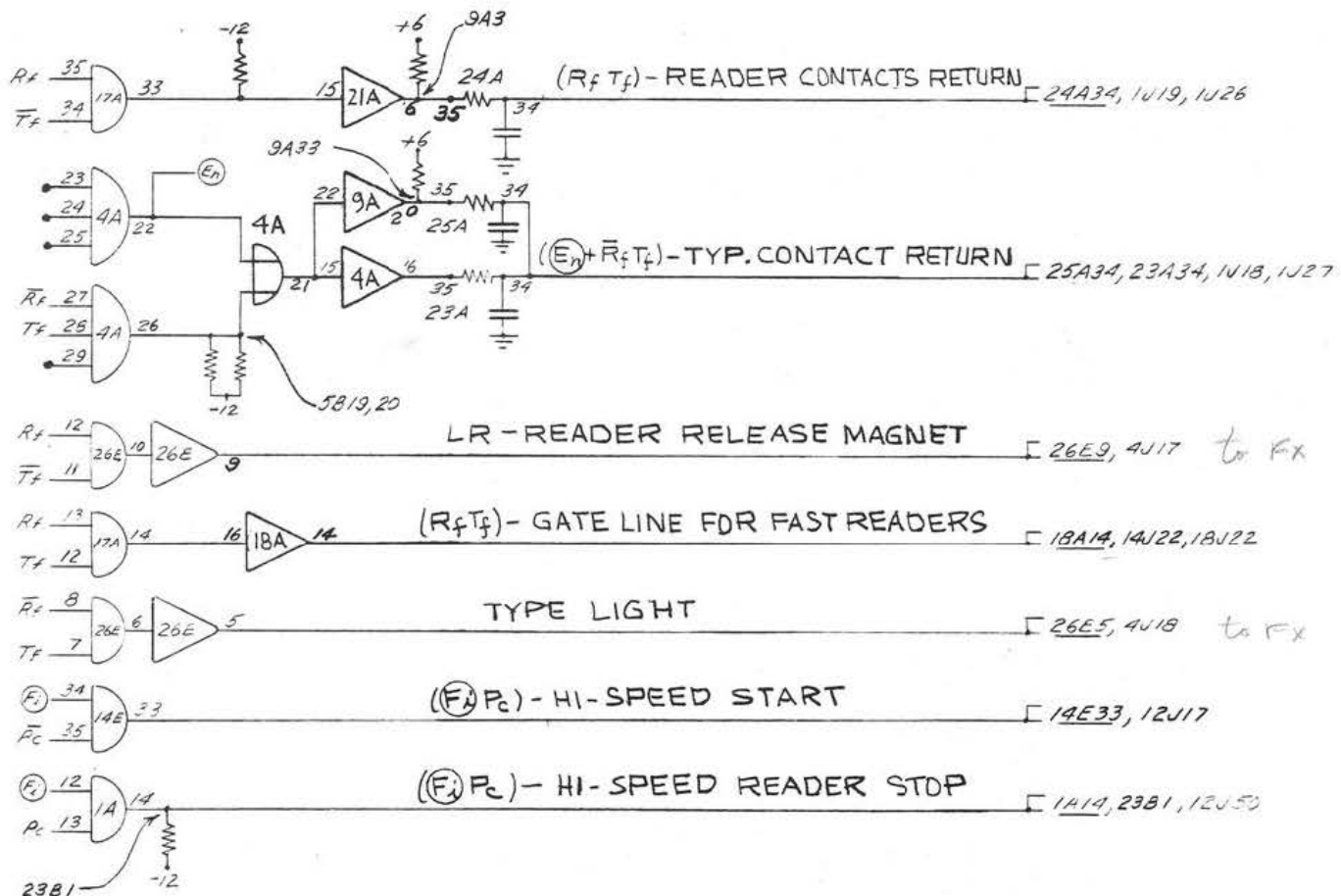
$$\begin{aligned}
 SRf &= E_c O_6 \bar{O}_5 O_4 \bar{O}_3 O_2 + \bar{F}_2 \bar{P}_c (P_8 - P_{15}) \bar{M}_p \\
 Rf &= E_c O_6 \bar{O}_5 O_4 \bar{O}_3 \bar{O}_2 + \bar{F}_2 \bar{M}_p (P_8 - P_{15}) + \bar{R}_c \bar{E}_c \\
 STf &= E_c O_6 \bar{O}_5 O_4 \bar{O}_3 O_1 \\
 Tf &= E_c O_6 \bar{O}_5 O_4 \bar{O}_3 \bar{O}_1 + \bar{T}_c \bar{E}_c + \bar{F}_2 (P_8 - P_{15})
 \end{aligned}$$

**LOGIC LAYOUT**

LOGIC SECT.	CHAR.	INPUT	TERM	Rf, Tf
DWG. NO.	505782	T	DATE	1-6-62
DRAWN BY	H. Mendelsohn	APP.		

SH.66

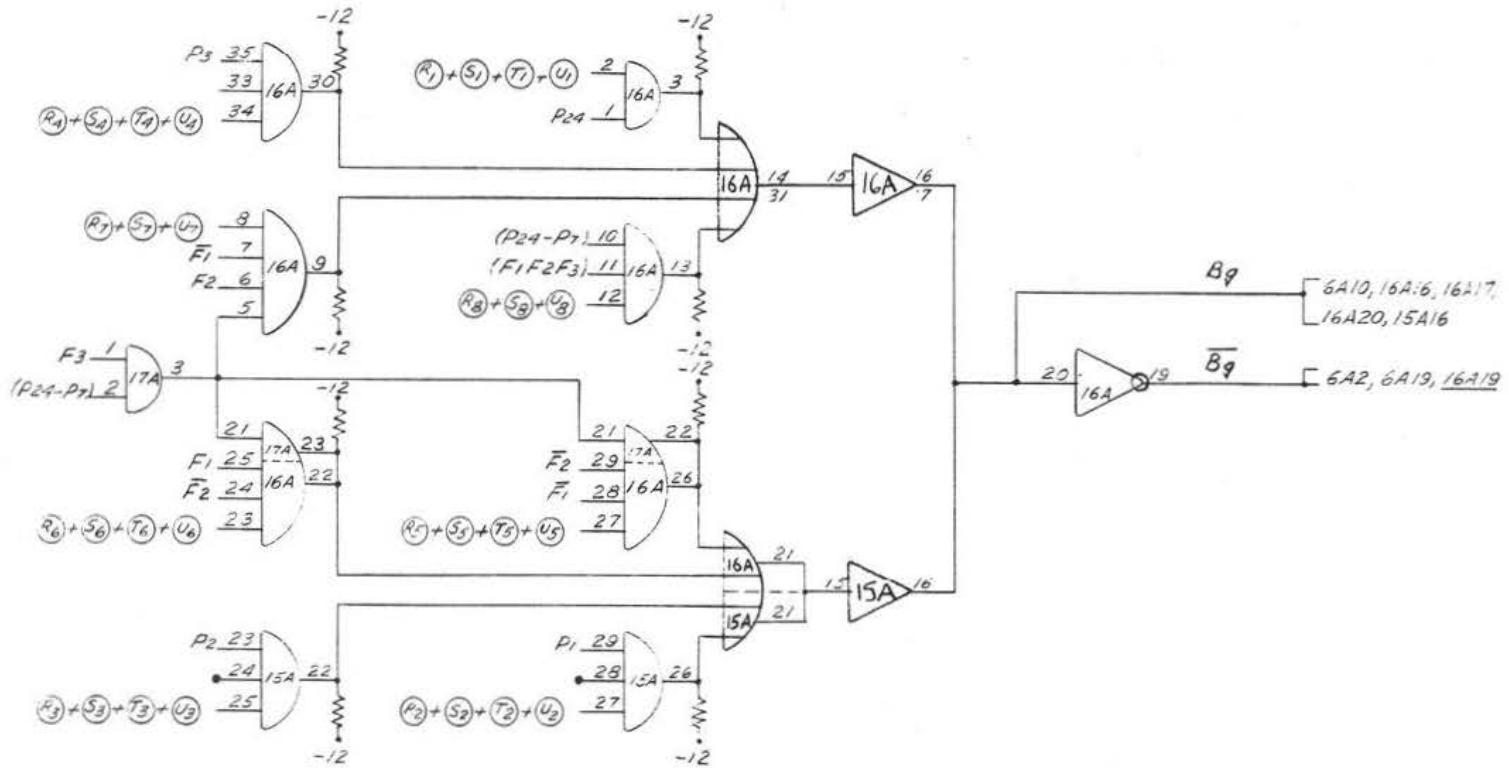
6-75



LOGIC LAYOUT

LOGIC SECT. CHAR. INPUT TFR: 8  
 DWS. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. J. ... APP. ...  
 SH. 67

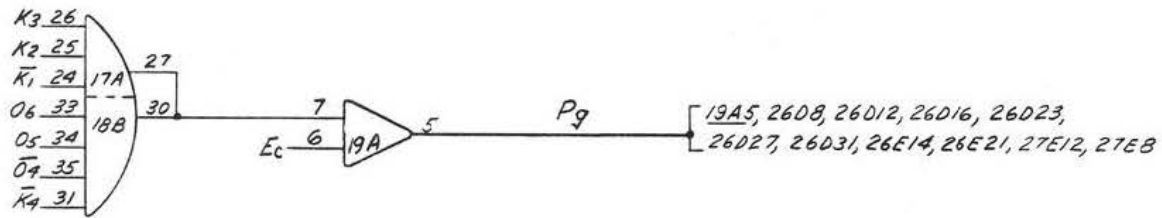
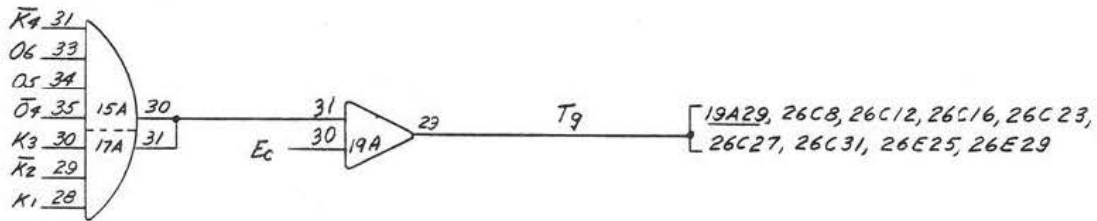
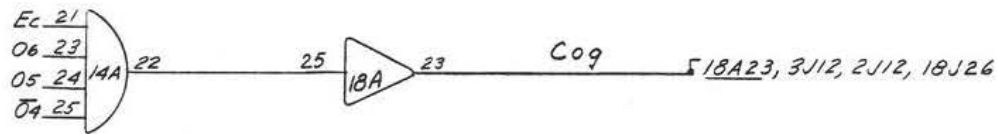
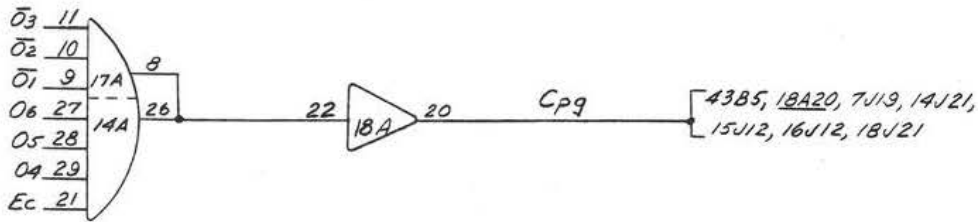
6-76



$$\begin{aligned}
 Bg &= P_{24} (R_1 + S_1 + T_1 + U_1) + (R_2 + S_2 + T_2 + U_2) P_1 + P_2 (R_3 + S_3 + T_3 + U_3) \\
 &+ P_3 (R_4 + S_4 + T_4 + U_4) + (P_{24} - P_7) F_3 \bar{F}_2 F_1 (R_5 + S_5 + T_5 + U_5) \\
 &+ (P_{24} - P_7) F_3 \bar{F}_2 F_1 (R_6 + S_6 + T_6 + U_6) + (P_{24} - P_7) F_3 F_2 F_1 (R_7 + S_7 + U_7) \\
 &+ (P_{24} - P_7) F_3 F_2 F_1 (R_8 + S_8 + U_8)
 \end{aligned}$$

**LOGIC LAYOUT**

LOGIC SECT. CHARACTER INPUT TERM  $Bg$   
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mandelsohn APP. \_\_\_\_\_  
 SH.68



6-77

$$Cp9 = Ec O6 O5 O4 \bar{O}_3 \bar{O}_2 \bar{O}_1$$

$$Co9 = Ec O6 O5 \bar{O}_4$$

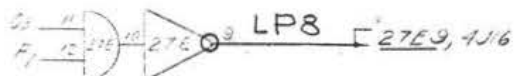
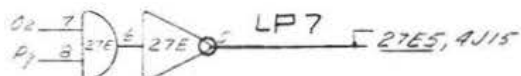
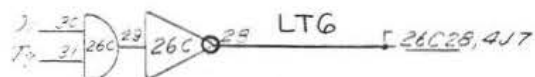
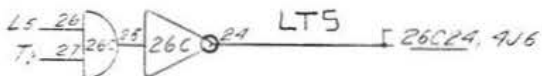
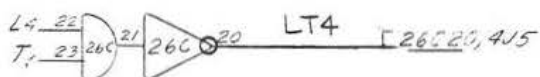
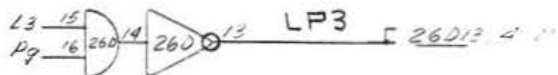
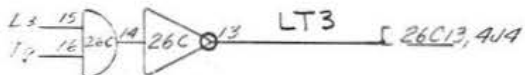
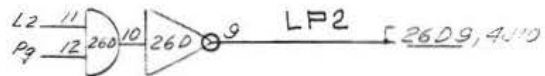
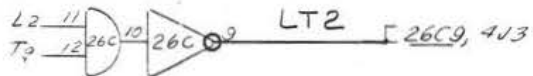
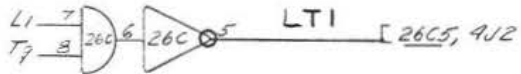
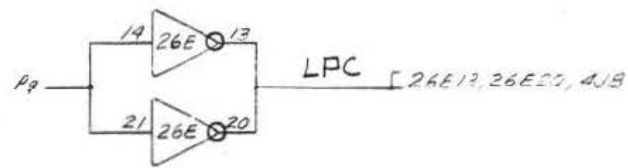
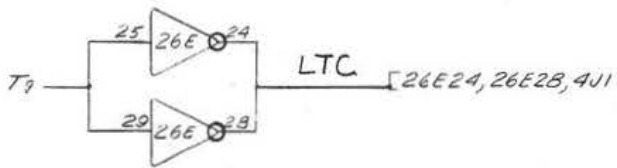
$$T9 = Ec O6 O5 \bar{O}_4 K_3 \bar{K}_2 K_1 \bar{K}_4$$

$$P9 = Ec O6 O5 \bar{O}_4 K_3 K_2 \bar{K}_1 \bar{K}_4$$

### LOGIC LAYOUT

LOGIC SECT.	CHAR. & CONT.	OUT TERM
DWG. NO.	505782 T	DATE 1-6-62
DRAWN BY	H. Mendelsohn	APP. _____

SH.69

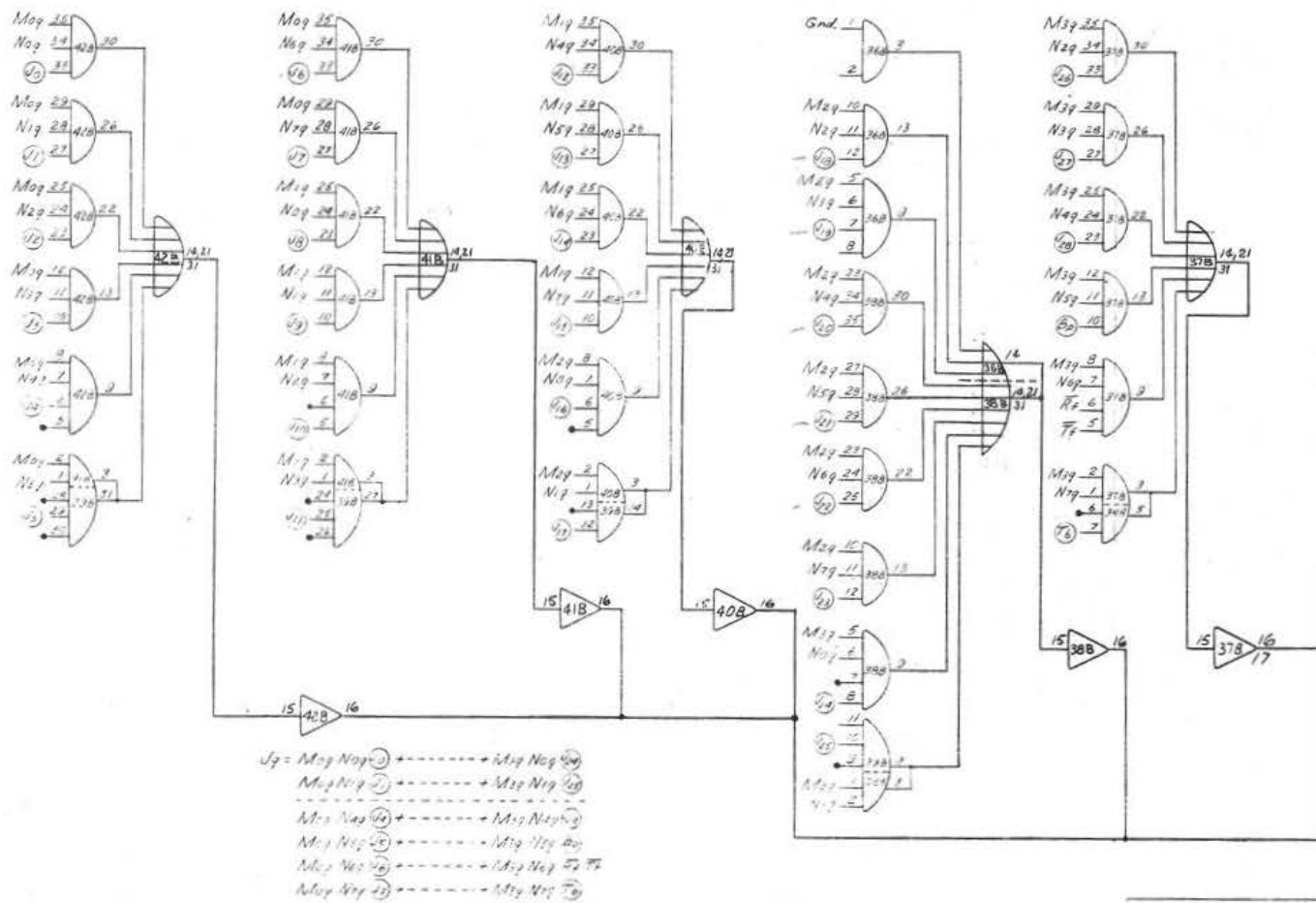


6-78

**LOGIC LAYOUT**

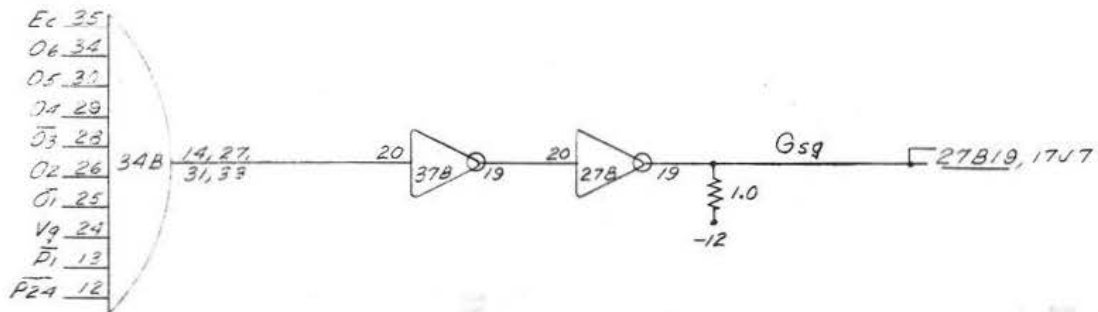
LOGIC SECT CHARACTER OUT TEP  
 DWG. NO. 505782 T DATE 1-6-61  
 DRAWN BY H.D. [unclear] APP. [unclear]  
 SH. 70

6-79

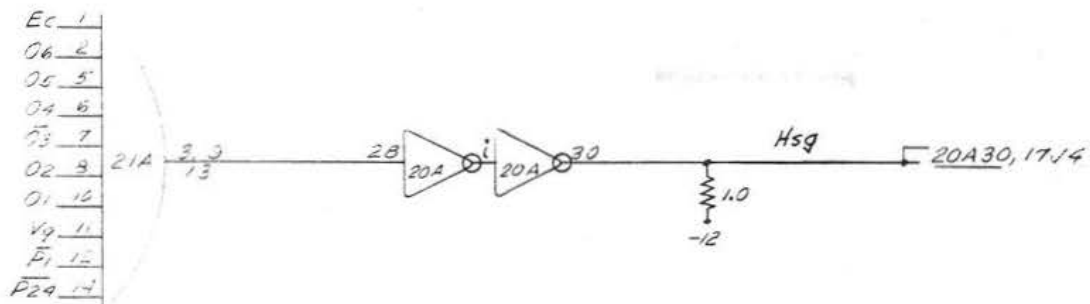


LOGIC LAYOUT  
 508782 T  
 1-6-62  
 SH-71

1818-0-18182 K2



08-9



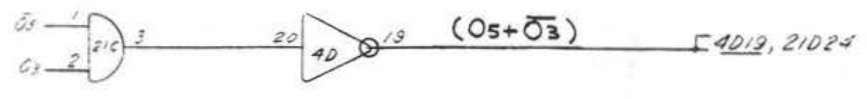
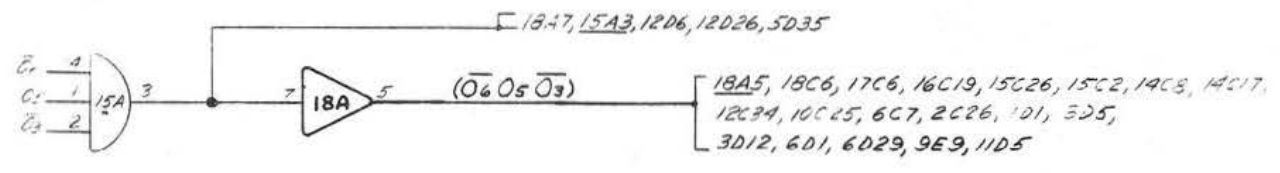
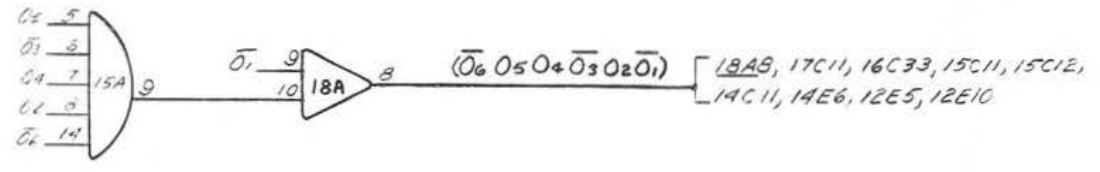
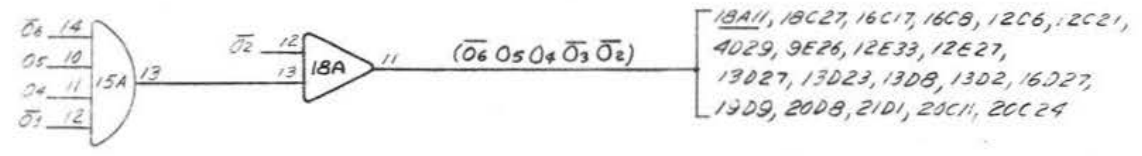
$$Gsq = Ec O6 O5 O4 O3 O2 O1 Vq \bar{P}_i \bar{P}_{24}$$

$$Hsq = Ec O6 O5 O4 O3 O2 O1 Vq \bar{P}_i \bar{P}_{24}$$

**LOGIC LAYOUT**

LOGIC SECT. SERIAL IN/OUT TERM \_\_\_\_\_  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. Mendelsohn APP. \_\_\_\_\_  
 SH. 72

18-9



**LOGIC LAYOUT**

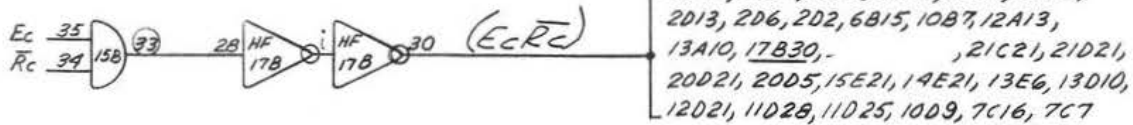
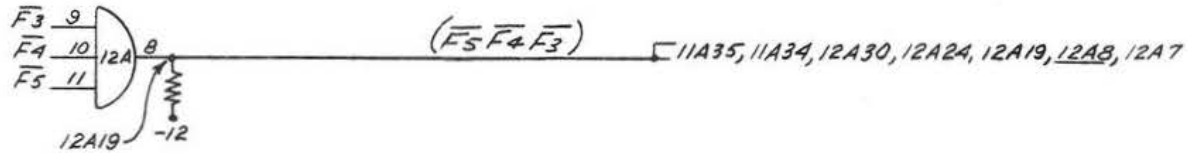
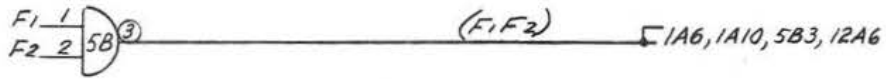
LOGIC SECT. DIST. LOGIC TERM         

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. M. ... APP.         

SH. 73





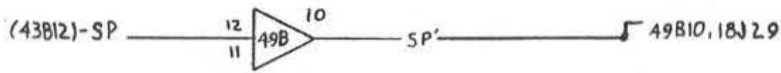
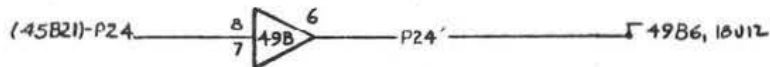
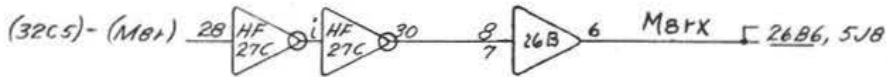
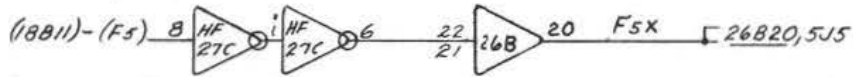
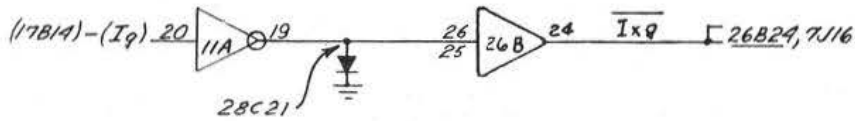
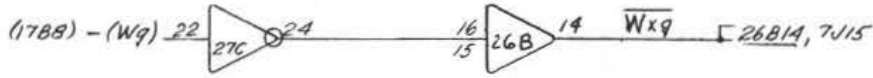
6-82

### LOGIC LAYOUT

LOGIC SECT. DIST. LOGIC TERM \_\_\_\_\_  
 DWG. NO. 505782 T DATE 1-9-62  
 DRAWN BY H. Mendelsohn APP. \_\_\_\_\_

SH. 74

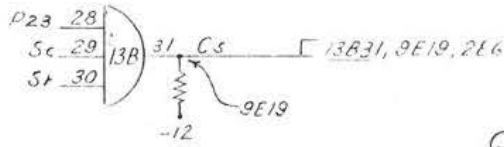
1J la memory ext.  
5J la computer coupling



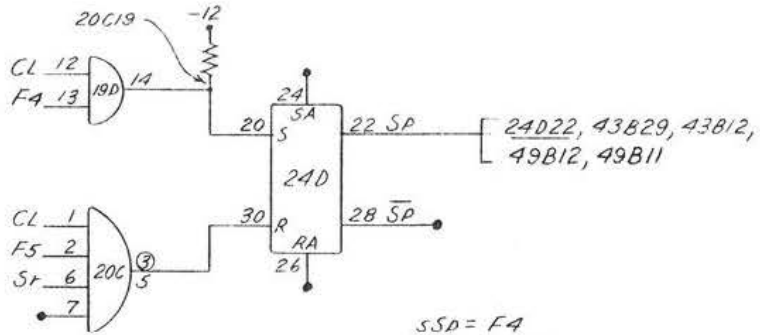
### LOGIC LAYOUT

LOGIC SECT. \_\_\_\_\_ TERM \_\_\_\_\_  
 DWG. NO. 505782 T DATE 1-6-62  
 DRAWN BY H. H. [unclear] APP. \_\_\_\_\_

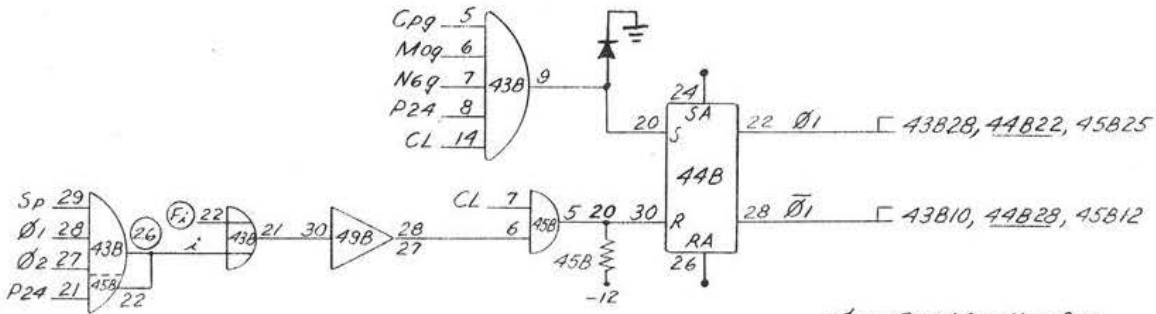
SH. 75



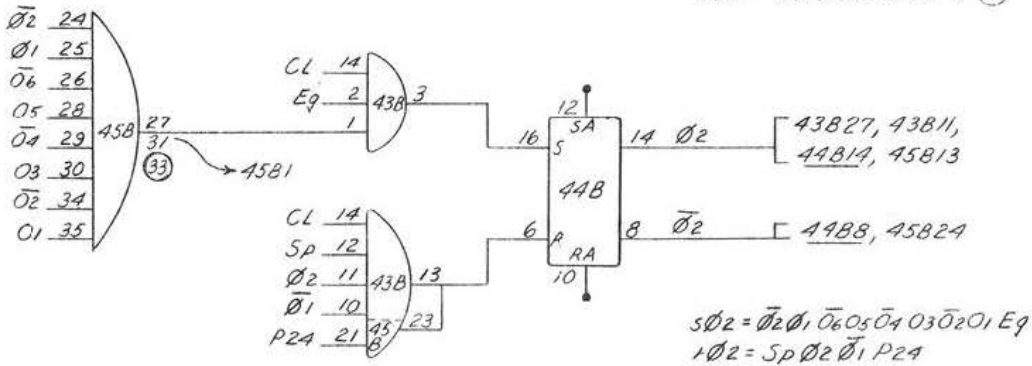
$C5 = P23 Sc St$



$SSD = F4$   
 $SP = F5 St$



$SØ1 = Cp9 Mog N69 P24$   
 $Ø1 = Sp Ø1 Ø2 P24 + (F4)$

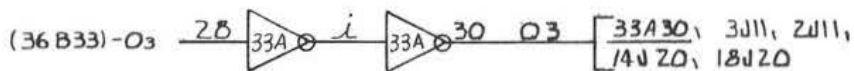
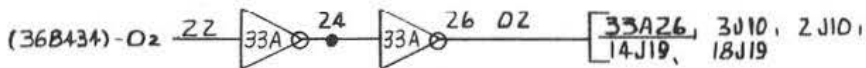
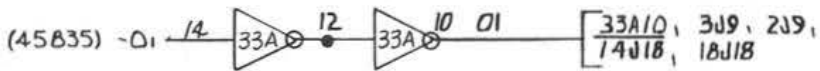
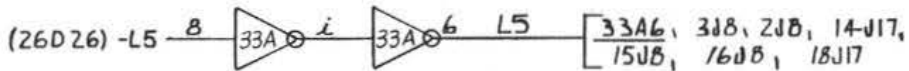
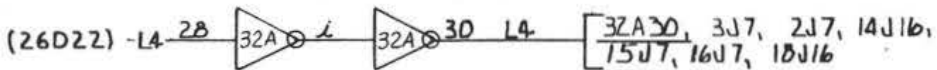
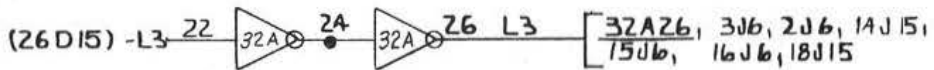
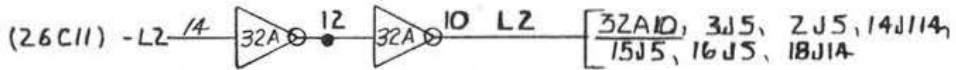
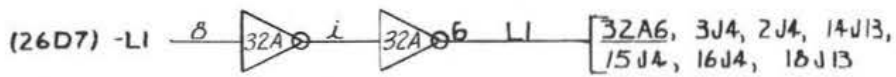


$SØ2 = Ø2 Ø1 Ø6 Ø5 Ø4 Ø3 Ø2 O1 E9$   
 $Ø2 = Sp Ø2 Ø1 P24$

**LOGIC LAYOUT**

LOGIC SECT. \_\_\_\_\_ TERM Cs, Sp, Ø1, Ø2  
 DWG. NO. 505782 T DATE 1-9-62  
 DRAWN BY H. Wendelschn APP \_\_\_\_\_

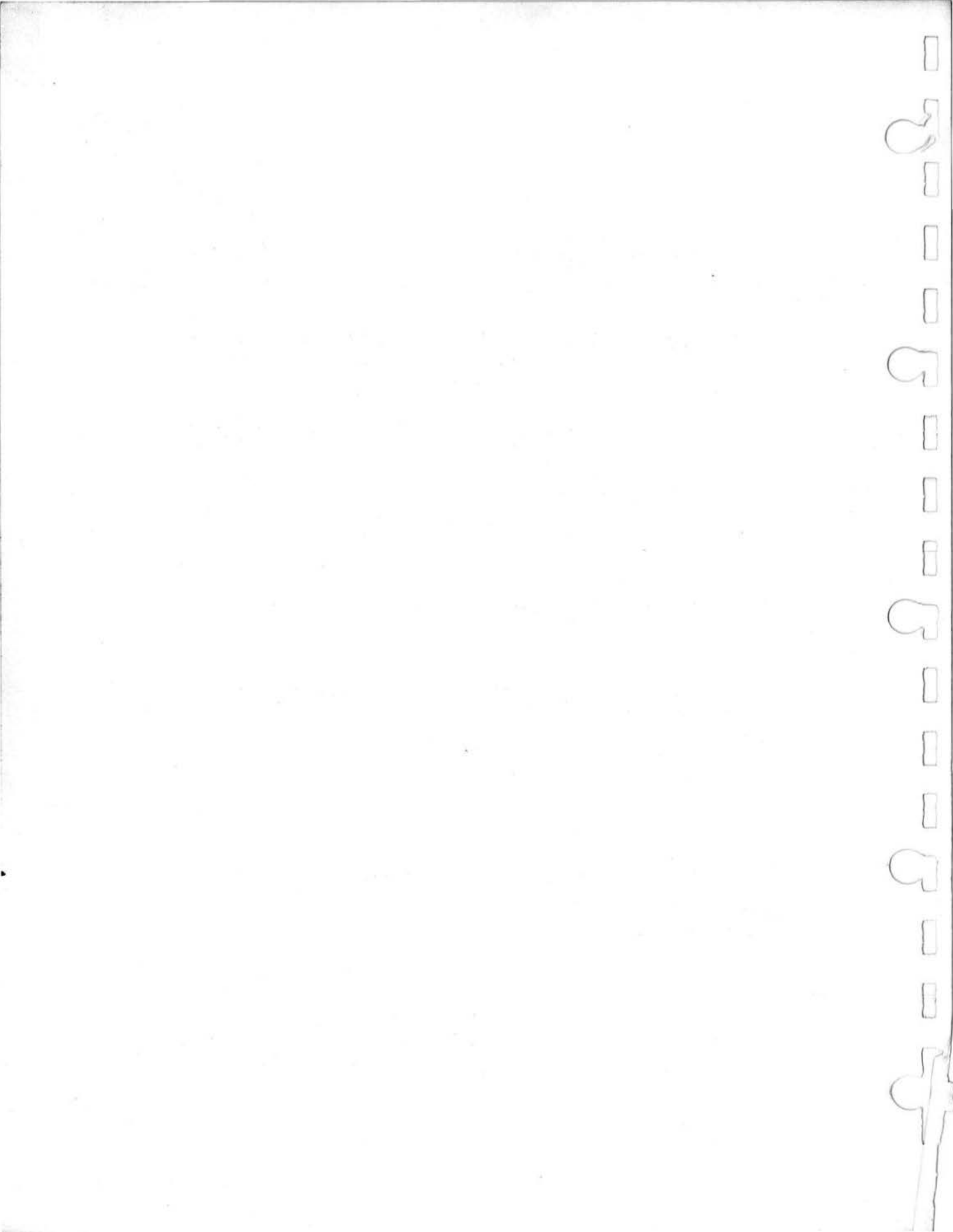
SH. 76



### LOGIC LAYOUT

LOGIC SECT SIGNAL BUFFERING TERM \_\_\_\_\_  
 DWG NO. 505782 U DATE 2-2-62  
 DRAWN BY K. WOODIE APP. \_\_\_\_\_

SH. 77



## VII. ENGINEERING DRAWINGS

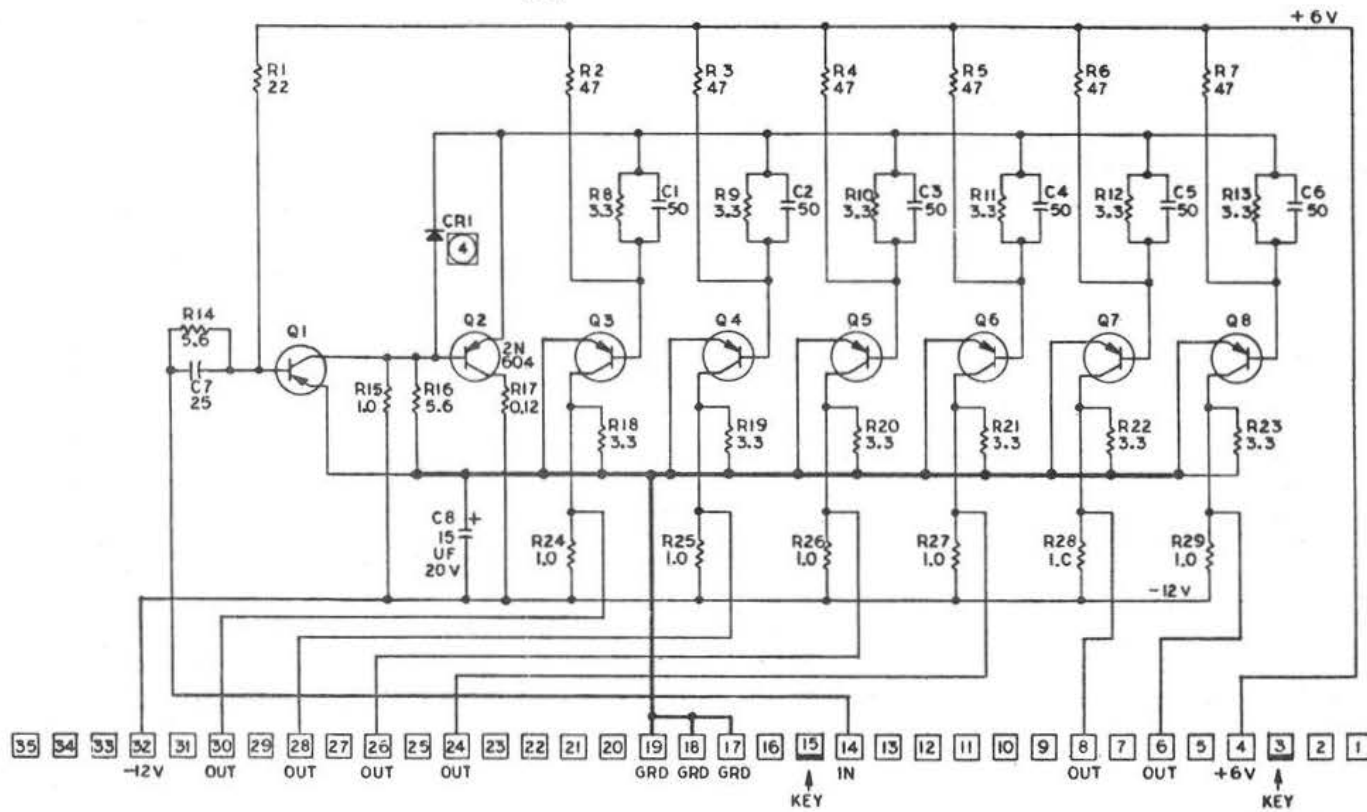
This section contains engineering drawings. Table 7-1 lists the drawing number, title, and page number of drawings applicable to the PB250 Computer.

Table 7-1.  
ENGINEERING DRAWINGS

Drawing No.	Fig-Title	Page
1C2503	CD-100 Schematic 7-1	7-2
1C2333	DG-100 Schematic 7-2	7-3
1C2320	DG-101 Schematic 7-3	7-4
1C2335	DG-102 Schematic 7-4	7-5
1C2426	EF-100 Schematic 7-5	7-6
1C4535	EF-101 Schematic 7-6	7-7
1C4496	FC-100 Schematic 7-7	7-8
1C2477	GD-100 Schematic 7-8	7-9
1D2429	MSR-1 Schematic 7-9	7-10
1D2472	MSR-2 Schematic 7-10	7-11
1C2449	TD-100 Schematic 7-11	7-12
1C2425	TF-100 Schematic 7-12	7-13
1D6519	XCG-101 Schematic 7-13	7-14
1D4593	PB250 Module Location Diagram	7-15
1J4985	PB250 DC Power Wiring Installation Drawing	7-17
1D5623	PB250 Component Installation Drawing	7-19
1D4224	PB250 Connector Location Diagram	7-20
1C4597	PB250 AC Power Schematic	7-21
1D4411	Indicators Schematic	7-22

FIRST	LAST	DELETED
C1	C8	
CRI		
Q1	Q8	
R1	R29	

- NOTES: UNLESS OTHERWISE SPECIFIED,  
 1. ALL RESISTOR VALUES ARE IN KILOHMS  $\pm 5\%$ ,  $1/4$  W.  
 2. ALL CAPACITORS ARE IN UUF.  
 3. ALL TRANSISTORS ARE 2N1500.  
 4. CRI TO BE PER PBCC DWG NO. 358-1A3050.



7-2

RELEASED ON EO 1418		6-1-0
DATE	BASIC MODEL	DM-100
FORM	REV. AMB.	124-102692
APPROVED	DATE	6-1-60
BY	DATE	5/12/60
BY	DATE	4-27-68
PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		CD-100 CLOCK DRIVER SCHEMATIC DIAGRAM
NOTES: UNLESS OTHERWISE NOTED		756-1C2503 C

Figure 7-1

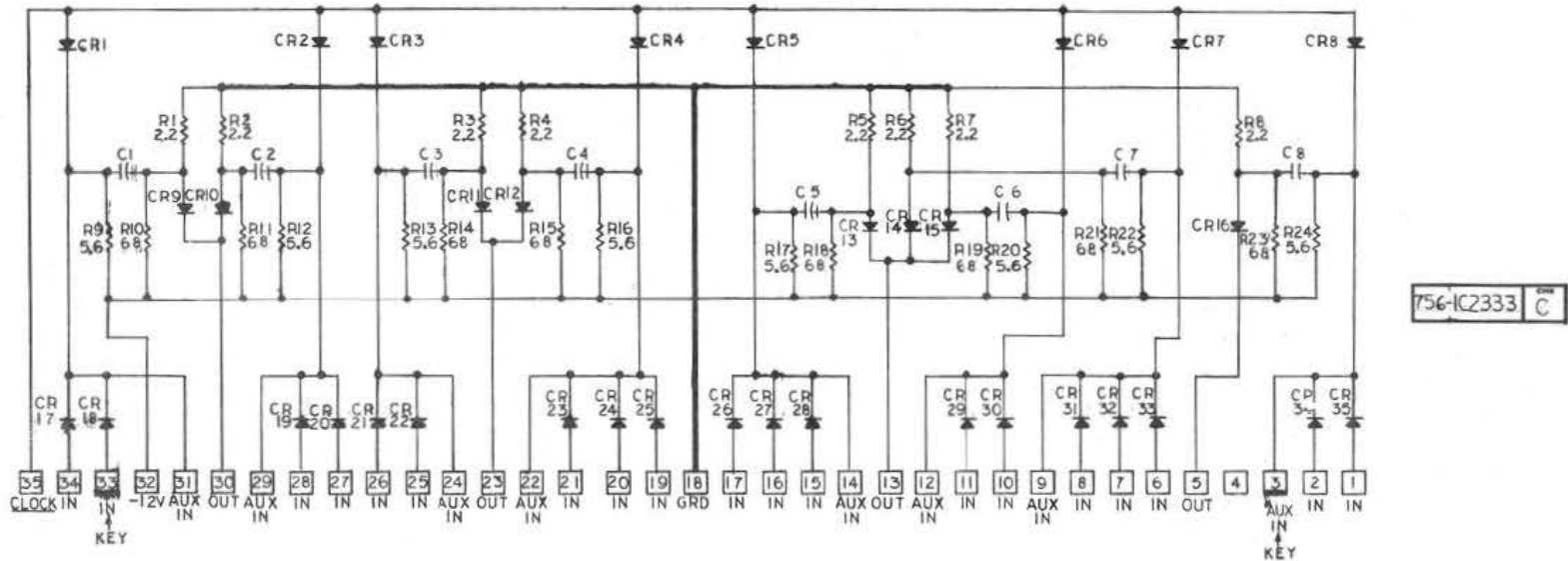
CD-100 Schematic

FIRST	LAST	DELETED
R1	R24	
C1	C8	
CR1	CR35	

- NOTES: UNLESS OTHERWISE SPECIFIED  
 1 ALL RESISTORS ARE IN KILOHMS  
 $\pm 5\%$ , 1/4 W.  
 2 ALL DIODES TO BE PER PBCC  
 DWG NO. 358-1A3C50.  
 3 ALL CAPACITORS ARE 50UUF.

NOTE: all Resistors Nailed @ 68 are ~~37K~~ 6.8K

7-3



RELEASED ON EO #1418		6-10	
DATE:	BASIC MODEL:	SCALE:	NOTES: UNLESS OTHERWISE NOTED
	DM-100		1. TOLERANCES: AS SHOWN UNLESS OTHERWISE SPECIFIED
FINISH:	NEXT ASSEMBLY:	REF:	2. BREAK CHART EDGES PERIOD. 311
	124-102334		3. MACHINING FINISHES TO SPEC
DESIGNED BY:	DATE:	PACKARD BELL COMPUTER CORP.	DO NOT REPAIR THIS
R.H.	7/7/60	LOS ANGELES 29, CALIFORNIA	
DR. BY:	DATE:	DG-100	
p.j.d.	3/28/60	SCHEMATIC DIAGRAM	756-IC2333 C

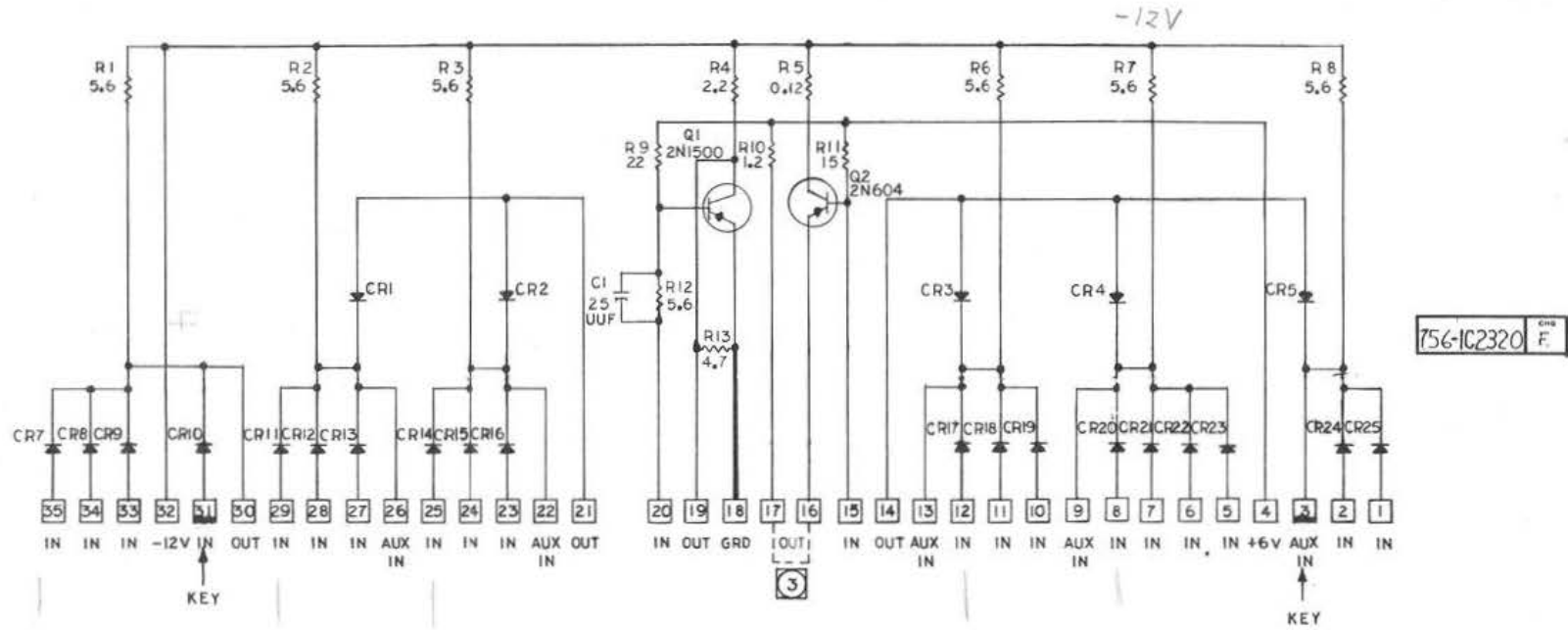
Figure 7-2 DG-100 Schematic



FIRST	LAST	DELETED
R1	R13	
C1	C1	
CR1	CR25	CR6
Q1	Q2	

NOTES: UNLESS OTHERWISE SPECIFIED  
 1 ALL RESISTOR VALUES ARE IN KILOHMS  $\pm 5\%$ , 1/4 W.  
 2 ALL DIODES TO BE PER PBCC DWG NO. 356-1A3050.  
 3 WHEN PARALLELING EMITTER FOLLOWERS, THE CONNECTION BETWEEN CONTACT TERMINAL 16 & 17 IS OMITTED.

7-4

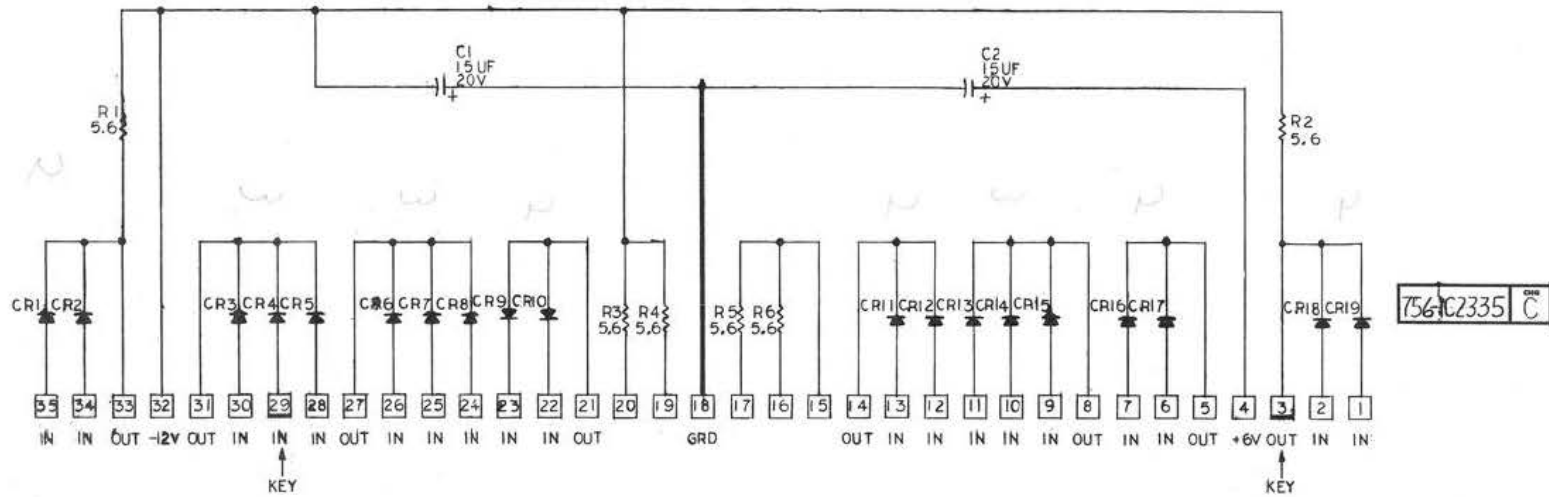


RELEASED ON EO# 1418		6-10	
DATE	BASIC MODEL	SCALE	1" = 100 UNLESS OTHERWISE NOTED
	DM-100		
FINISH	NET ASBY.	REV.	1. TOLERANCES UNLESS OTHERWISE SPECIFIED
	124-102321		2. DIMENSIONS TO FACE UNLESS OTHERWISE SPECIFIED
APPROVED	PACKARD BELL COMPUTER CORP.	3. REMOVE ALL BURRS	
6-1-60	LOS ANGELES 25, CALIFORNIA	4. MACHINED FINISHES TO	
DR BY	DG-101	DO NOT SCALE DIMS	
PJD 3-17-60	SCHEMATIC DIAGRAM	756-1C2320	E

Figure 7-3 DG-101 Schematic

FIRST	LAST	DELETED
C1	C2	
CR1	CR19	
R1	R6	

NOTES: UNLESS OTHERWISE SPECIFIED  
 1. ALL RESISTOR VALUES ARE IN KILOHMS  $\pm 5\%$ , 1/4W  
 2. ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050.



7-5

RELEASED ON EO #1418		6-1-0
MAT'L	BASIC MODEL	SCALE
	DM-100	
FINISH	NEXT ASBY.	REF.
	124-1D2336	
DATE	PACKARD BELL COMPUTER CORP.	NOTES: UNLESS OTHERWISE NOTED
6-1-60	LOS ANGELES 25, CALIFORNIA	1. TOLERANCES: XX ± .03, XX ± .05, ANGULAR ± 1/4°
CHECK		2. BREAK SHARP EDGES
R/K		3. REMOVE ALL BURRS
	DG-102	4. MACHINED FINISHED TO .0007
DR. BY	SCHMATIC DIAGRAM	DO NOT SCALE DIMS.
PJD		
3/18/60		756102335 C

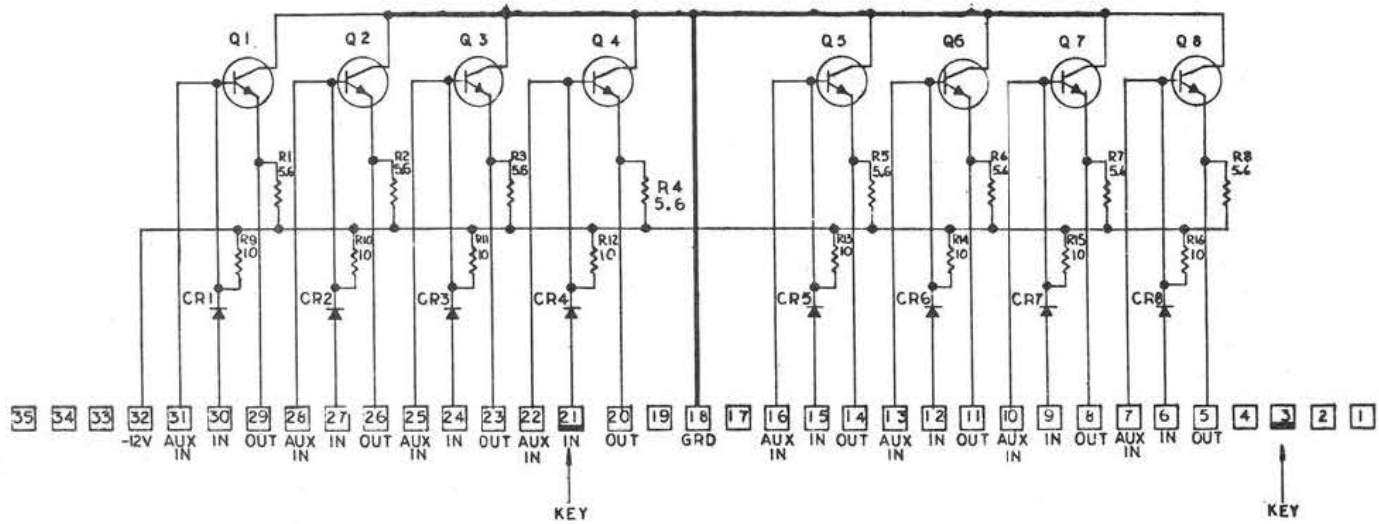
Figure 7-4 DG-102 Schematic

FIRST	LAST	DELETED
CR 1	CR 8	
Q 1	Q 8	
R 1	R 16	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN KILOHMS  $\pm 5\%$ , 1/4W.
2. ALL DIODES TO BE PER PDC DWG NO. 358-1A3050.
3. ALL TRANSISTORS ARE 2N1605.

7-6

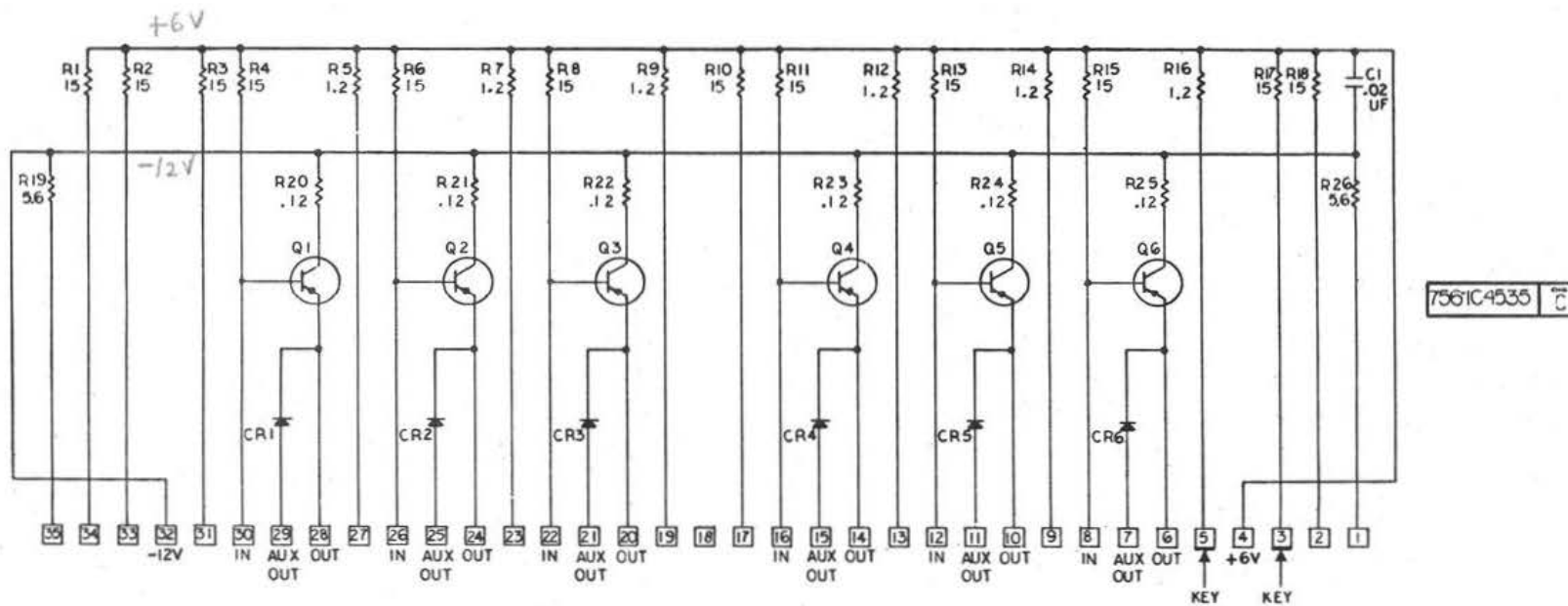


756-1C2426 C

RELEASED ON EO #1418		610	
MAT'L	DM-100	SCALE	NOTES: UNLESS OTHERWISE NOTED
FINISH	DM-100	REF.	1. TOLERANCES: UNLESS SPECIFIED ANGULAR $\pm 15^\circ$
DATE	6-1-60	PACKARD BELL COMPUTER CORP.	2. BREAK-DOWN POWER APPROX. .513
CHK'D	3/5/60	LOS ANGELES 22, CALIFORNIA	3. REMOVE ALL BURRS
DRN BY	p j d	EF-100	QUANTITY SCALE
	7/18/60	SCHEMATIC DIAGRAM	756-1C2426 C

Figure 7-5 EF-100 Schematic

NOTES: UNLESS OTHERWISE SPECIFIED  
 1. ALL DIODES ARE PER PBCC DWG. NO. 358-1A3050  
 2. ALL RESISTOR VALUES ARE IN KIL OHMS  $\pm 5\%$  1/4W  
 3. ALL TRANSISTORS ARE 2N604



7-7

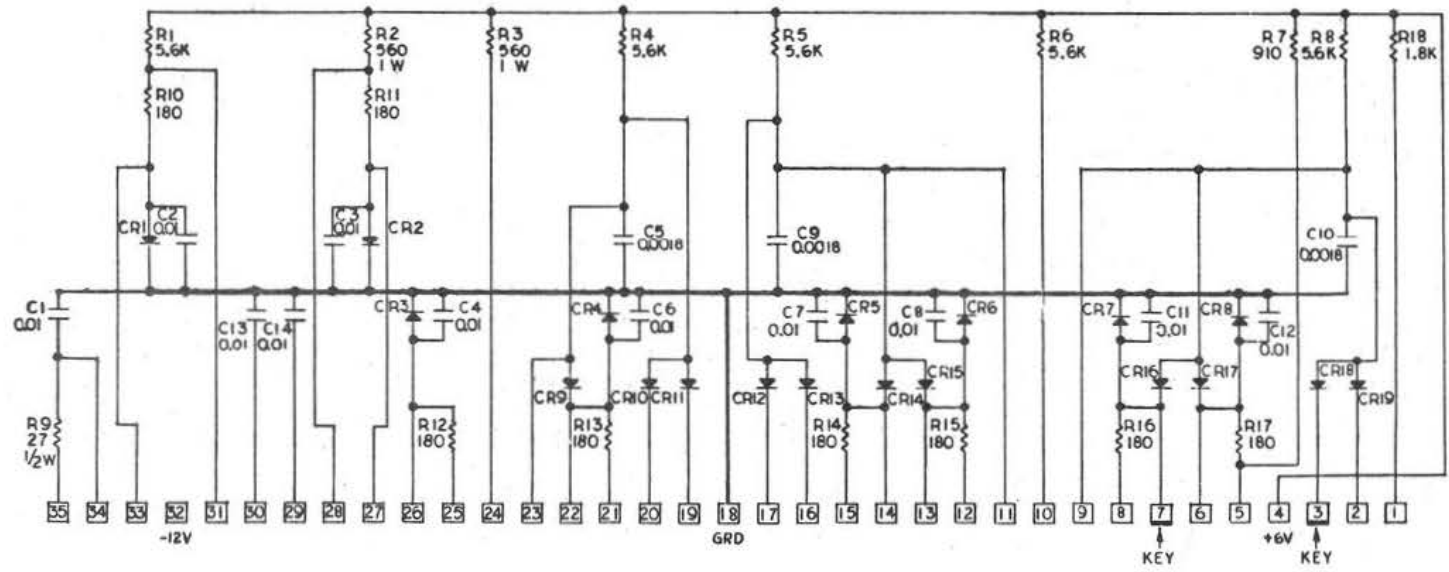
RELEASED ON EO #1560 9/1/60

NAT'L		BASIC MODEL	DM-100	REVISION	NOTES: UNLESS OTHERWISE NOTED
FIGURE		WEEK	NOV 4625	REV.	1. TOLERANCES AS SHOWN UNLESS OTHERWISE SPECIFIED
APP. BY	DATE	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		REV.	2. BREAK SHARP EDGES OFFICE USE
DESIGN	DATE	EF-101		REV.	3. SHOWS ALL DIMENSIONS UNLESS OTHERWISE SPECIFIED
CHK. BY	DATE	SCHEMATIC DIAGRAM		REV.	4. MACHINED PARTS TO SPECIFICATION
				NO. 756-IC4535	C

Figure 7-6 EF-101 Schematic

- NOTES: UNLESS OTHERWISE SPECIFIED  
 1. ALL DIODES TO BE PER PBCC DWG NO. 358-IA3050  
 2. ALL RESISTOR VALUES IN OHMS  $\pm 5\%$  1/4W.  
 3. CAPACITOR VALUES IN UF.

7-8



756-IC4496 C

RELEASED ON 30 45609/1/60

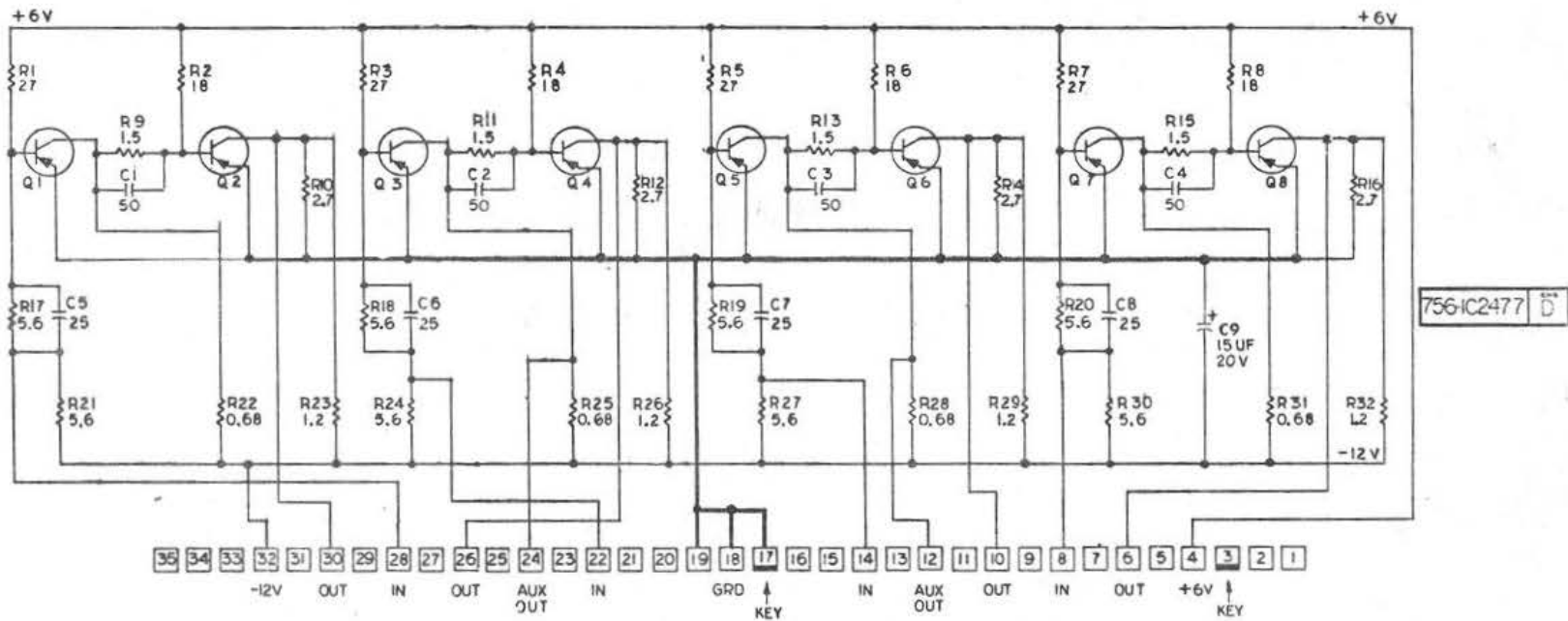
DATE:	REV. DM-100	SCALE:	NOTES UNLESS OTHERWISE NOTED
DESIGNER:	TEST UNIT:	REF.:	1. TOLERANCES UNLESS OTHERWISE SPECIFIED
	124-IC4580		2. DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
APP. <i>U-10</i> 7/28/60	PACKARD BELL COMPUTER CORP.		3. SHOW ALL DIMENSIONS
CHKD <i>Tomal</i> 7/1/60	LOS ANGELES 25, CALIFORNIA		4. MATCHED PARTS/IC'S
DRN BY <i>A.H.</i> 7-21-60	FC-100		DO NOT SCALE DIM.
	SCHEMATIC DIAGRAM		756-IC4496 C

Figure 7-7 FC-100 Schematic

FIRST	LAST	DELETED
Q1	Q8	
R1	R32	
C1	C9	

NOTES: UNLESS OTHERWISE SPECIFIED  
 1. ALL RESISTOR VALUES IN KILOHMS  $\pm 5\%$ ,  $\frac{1}{4}$ W.  
 2. ALL CAPACITOR VALUES IN UUF.  
 3. ALL TRANSISTORS 2N1500.

7-9



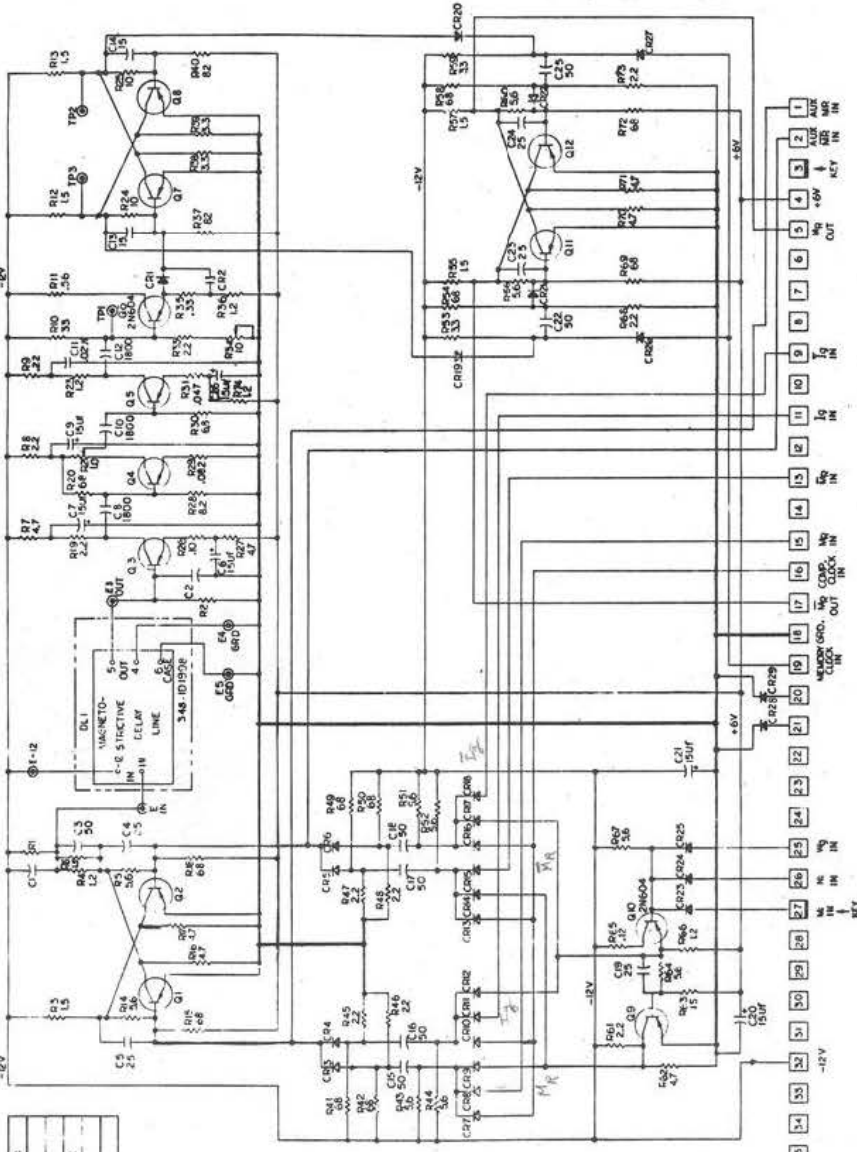
RELEASED ON EO 14176		610
DATE	BASE	SCALE
FINISH	DR: 100	REF
	124-1D2492	
REV	6-1-60	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA
DESIGN	R/E	GD-100
BY	M.C.	413-60
		SCHMATIC DIAGRAM
		756-IC2477
		NOTES: UNLESS OTHERWISE NOTED 1. TOLERANCES 2. ALL DIMENSIONS 3. UNLESS OTHERWISE SPECIFIED 4. REMOVE ALL BURRS 5. MACHINED FINISH 6. SURFACE SCALE 7. C

Figure 7-8 GD-100 Schematic

NOTES: UNLESS OTHERWISE SPECIFIED,  
ALL DIMENSIONS ARE IN INCHES ±.015.  
ALL DIMENSIONS ARE 350-143030

2. ALL RESISTOR VALUES ARE IN OHMS ±5% & WATT.  
3. R1, R2, C1, C2 & C3 VALUES SPECIFIED BY DELAY LINE  
VENDOR.

4. ALL CAPACITIVE VALUES IN MUF.  
5. A.-L TRANSISTORS ARE 2N130C.



PART	QTY	DESCRIPTION
R1	1	100Ω
R2	1	100Ω
R3	1	100Ω
R4	1	100Ω
R5	1	100Ω
R6	1	100Ω
R7	1	100Ω
R8	1	100Ω
R9	1	100Ω
R10	1	100Ω
C1	1	100μF
C2	1	100μF
C3	1	100μF
C4	1	100μF
C5	1	100μF
C6	1	100μF
C7	1	100μF
C8	1	100μF
C9	1	100μF
C10	1	100μF

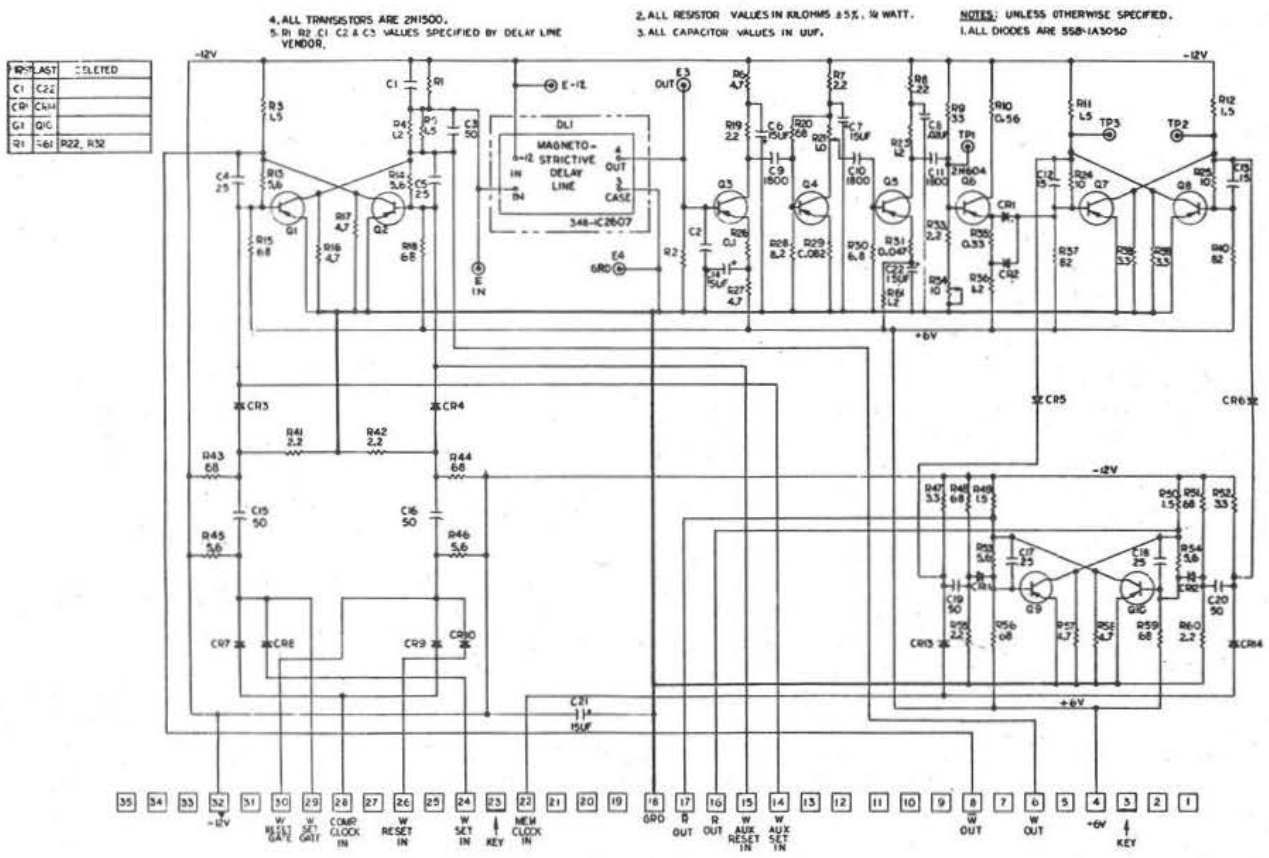
75600000

REV	DATE	BY	CHKD	DESCRIPTION
1	124-10-134			MSR-1
2				MSR-1
3				MSR-1
4				MSR-1
5				MSR-1
6				MSR-1
7				MSR-1
8				MSR-1
9				MSR-1
10				MSR-1
11				MSR-1
12				MSR-1

Figure 7-9 MSR-1 Schematic

256 words

7-11



756-102476 76

DESIGNED BY: EC 7002 1-60

DATE	REV.	BY	CHKD.
	1		
PROJECT: MSR-2		124-10445	
FACILITY: MISSOURI COMMERCE CENTER			
TITLE: MSR-2 MAGNETOSTRICTIVE DELAY LINE SCHEMATIC DRAWING			
SCALE: V.2	4.12-9		

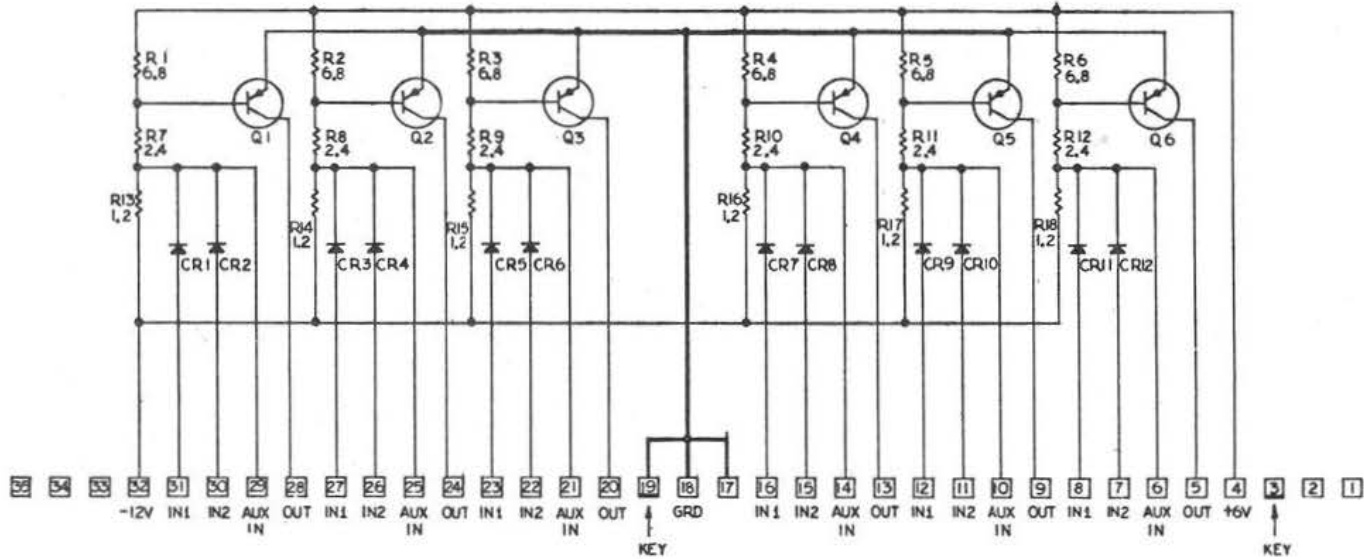
Figure 7-10 MSR-2 Schematic



FIRST	LAST	DELETED
Q 1	Q 6	
R 1	R 18	
CR 1	CR 12	

NOTES: UNLESS OTHERWISE SPECIFIED.  
 1. ALL RESISTOR VALUES IN KILOHMS  $\pm 5\%$ , 1/4 W.  
 2. ALL DIODES TO BE PER PBCC DWG NO. 358-1A 3050.  
 3. ALL TRANSISTORS ARE 2N1184 B.

7-12



756-C2449 D

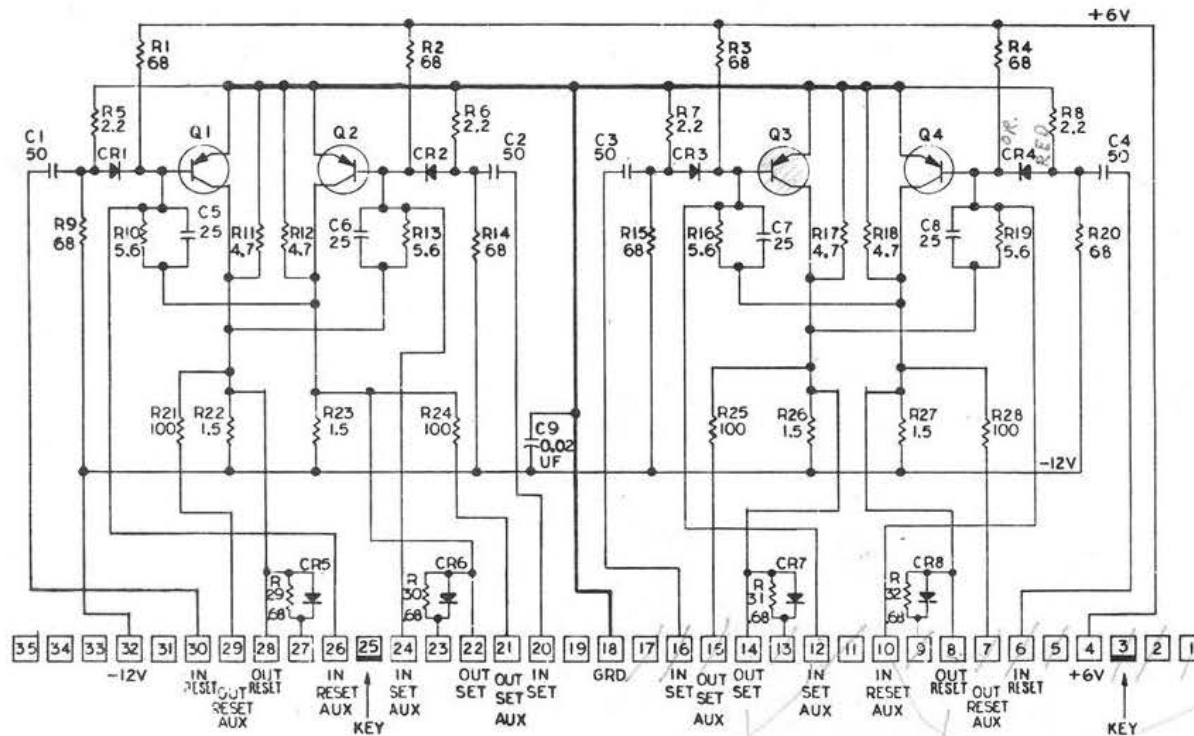
RELEASED ON EO 1418		610
MAT'L	BASE MODEL	NOTES: UNLESS OTHERWISE NOTED
	DM-100	1. TERMINATIONS: 20 $\pm$ .005 ANGULAR $\pm$ .15"
FINISH	REV. AMPY.	2. DIMENSIONS UNLESS OTHERWISE SPECIFIED
	124-102473	3. REMOVE ALL BURRS
DATE	6-1-60	4. REWORKED PARTS TO BE IDENTIFIED
BY	KA	5. UNLESS OTHERWISE SPECIFIED
CHK BY	4/9/60	
SC	4/7/60	
PACKARD BELL COMPUTER CORP. LOS ANGELES 28, CALIFORNIA		
TD-100 (DRIVER)		756-
SCHEMATIC DIAGRAM		IC2449 D

Figure 7-11 TD-100 Schematic

FIRST	LAST	DELETED
Q1	Q 4	
R1	R 32	
C1	C 9	
CR1	CR 8	

- NOTES: UNLESS OTHERWISE SPECIFIED.  
 1. ALL RESISTOR VALUES ARE IN KILOHMS  $\pm 5\%$ ,  $\frac{1}{4}$  W.  
 2. ALL DIODES TO BE PER PBCC DWG NO.358-IA3050.  
 3. ALL CAPACITOR VALUES ARE IN UUF.  
 4. ALL TRANSISTORS ARE 2N1500

*may clock train on 16 outputs K2 @ 8*



756-IC2425 E

7-13

*12 mo*

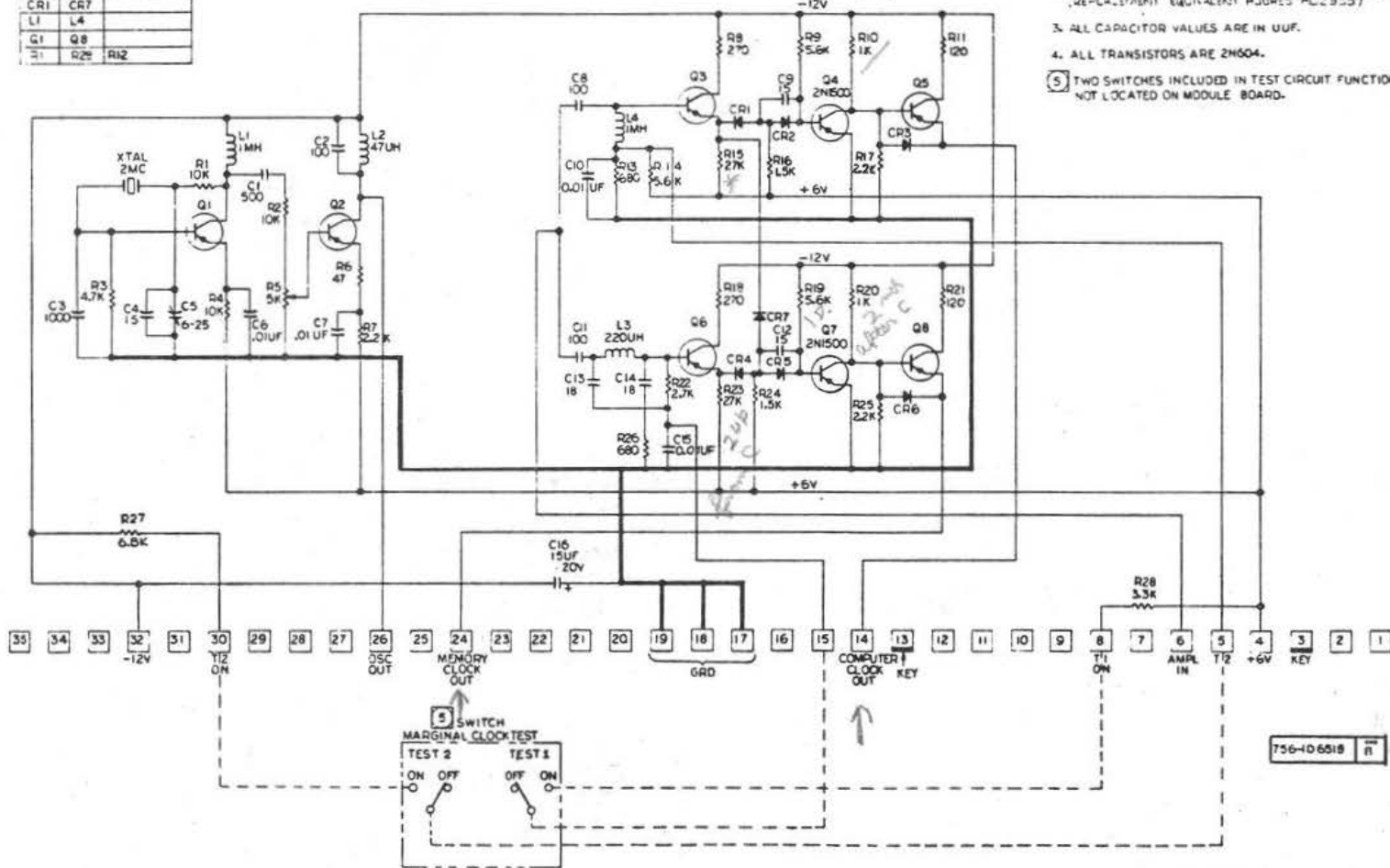
*K4 pos/gnd on lines Resistor 10*

*K4 may on lines Resistor 10*

RELEASED ON EO #1418		6-10
DATE:	BASIC MODEL:	SCALE:
	CM-100	
FINISH:	REV AMBY:	REP:
	124-ID2433	
APP. R.H.V.:	PACKARD BELL COMPUTER CORP.	NOTES: UNLESS OTHERWISE NOTED
11/15/60	LOG ANGELES 25, CALIFORNIA	1. TOLERANCES: ALL $\pm .01$ UNLESS OTHERWISE SPECIFIED
CHECK K.R.:	TF-100	2. BREAK SHARP EDGES APPROX. .010
4/5/60		3. REMOVE ALL BURRS MACHINED FINISHES ONLY
DR. BY C.R.:	4-5 60	DO NOT SCALE DTS
	SCHEMATIC DIAGRAM	756-IC2425 E

Figure 7-12 TF-100 Schematic

REFERENCE DESIGNATIONS		
FIRST	LAST	DELETED
C1	C16	
CR1	CR7	
L1	L4	
Q1	Q8	
R1	R26	R32



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS ± 5% 1/4W.
2. ALL DIODES DEC STANDARD PART NO. 1N22-1N25C (REPLACEMENT EQUIVALENT HUGHES HC2555)
3. ALL CAPACITOR VALUES ARE IN UUF.
4. ALL TRANSISTORS ARE 2N5004.
5. TWO SWITCHES INCLUDED IN TEST CIRCUIT FUNCTION NOT LOCATED ON MODULE BOARD.

7-14

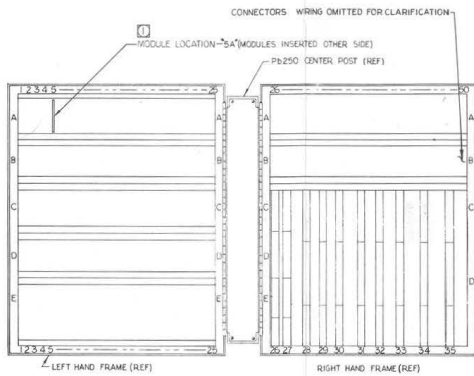
DATE	REV.	BY	CHKD.	APPROVED
	1	F.ZBI		
124-106521				
FACSIMILE COPY OF ORIGINAL				
(CLOCK GENERATOR)				
SCHEMATIC DIAGRAM				
				756-106518

Figure 7-13. XCG-101 Schematic

2. FOR MODULE CONNECTOR LOCATIONS SEE 350-D4244.

NOTES: UNLESS OTHERWISE SPECIFIED  
 □ LOCATION "SA" AS SHOWN WOULD BE THE ACTUAL LOCATION OF MODULE "TF-100" IN THE COMPUTER.

LOCATION IN FRAME ASSEMBLY	MODULE MODEL NO.														
	MSR-1B-191	MSR-2	MSR-3	MSR-4	MSR-5	MSR-6	MSR-7	MSR-8	MSR-9	MSR-10	MSR-11	MSR-12	MSR-13	MSR-14	MSR-15
28 C	25 B	22 B	7 A	10 A	18 A	2 A	6 A	4 A	1 A	26 C	24 A	19 E	18 E	17 E	16 E
			2 B	29 C	17 B	19 A	3 A	6 B	11 A	12 A	26 D	25 A	18 E	17 E	16 E
			7 D	30 C	27 C	19 B	10 B	13 A	17 A	25 E	23 A	18 E	17 E	16 E	15 E
			14 D	31 C	20 E	23 C	7 B	20 B	14 A	5 B	27 E	23 B	18 E	17 E	16 E
			22 D	28 D	25 C	11 B	1 C	15 A	13 B	13 B	13 B	13 B	13 B	13 B	13 B
			29 D	33 A	28 A	12 B	4 C	16 A	15 B	15 B	15 B	15 B	15 B	15 B	15 B
			30 D	33 A	28 A	21 B	7 C	1 B	30 B	30 B	30 B	30 B	30 B	30 B	30 B
			31 D	33 A	28 A	3 C	9 C	4 B	34 B	34 B	34 B	34 B	34 B	34 B	34 B
			32 C	32 C	5 C	12 C	8 B	39 B	39 B	39 B	39 B	39 B	39 B	39 B	39 B
			32 D	32 D	8 C	14 C	9 B	2 C	2 C	2 C	2 C	2 C	2 C	2 C	2 C
					11 C	16 C	16 B	6 C	6 C	6 C	6 C	6 C	6 C	6 C	6 C
					13 C	18 C	16 B	10 C	10 C	10 C	10 C	10 C	10 C	10 C	10 C
					17 E	16 D	18 B	15 C	15 C	15 C	15 C	15 C	15 C	15 C	15 C
					19 C	17 D	27 B	17 C	17 C	17 C	17 C	17 C	17 C	17 C	17 C
					9 D	16 E	28 B	21 C	21 C	21 C	21 C	21 C	21 C	21 C	21 C
					16 D	5 E	29 B	24 C	24 C	24 C	24 C	24 C	24 C	24 C	24 C
					6 E		31 B	2 D	2 D	2 D	2 D	2 D	2 D	2 D	2 D
					34 B		32 B	5 D	5 D	5 D	5 D	5 D	5 D	5 D	5 D
							33 B	10 D	10 D	10 D	10 D	10 D	10 D	10 D	10 D
							35 B	12 D	12 D	12 D	12 D	12 D	12 D	12 D	12 D
							36 B	19 D	19 D	19 D	19 D	19 D	19 D	19 D	19 D
							37 B	9 E	9 E	9 E	9 E	9 E	9 E	9 E	9 E
							38 B	13 E	13 E	13 E	13 E	13 E	13 E	13 E	13 E
							21 A	14 E	14 E	14 E	14 E	14 E	14 E	14 E	14 E
							26 A	15 E	15 E	15 E	15 E	15 E	15 E	15 E	15 E
							28 A	22 C	22 C	22 C	22 C	22 C	22 C	22 C	22 C
							1 D	20 C	20 C	20 C	20 C	20 C	20 C	20 C	20 C
							3 D	27 A	27 A	27 A	27 A	27 A	27 A	27 A	27 A
							4 D	29 A	29 A	29 A	29 A	29 A	29 A	29 A	29 A
							6 D	4 E	4 E	4 E	4 E	4 E	4 E	4 E	4 E
							11 D								
							13 D								
							23 D								
							21 D								
							10 E								
							11 E								
							12 E								
							16 E								
							44 B								
							45 B								
							46 B								
							47 B								
							48 B								
							49 B								
							45 B								

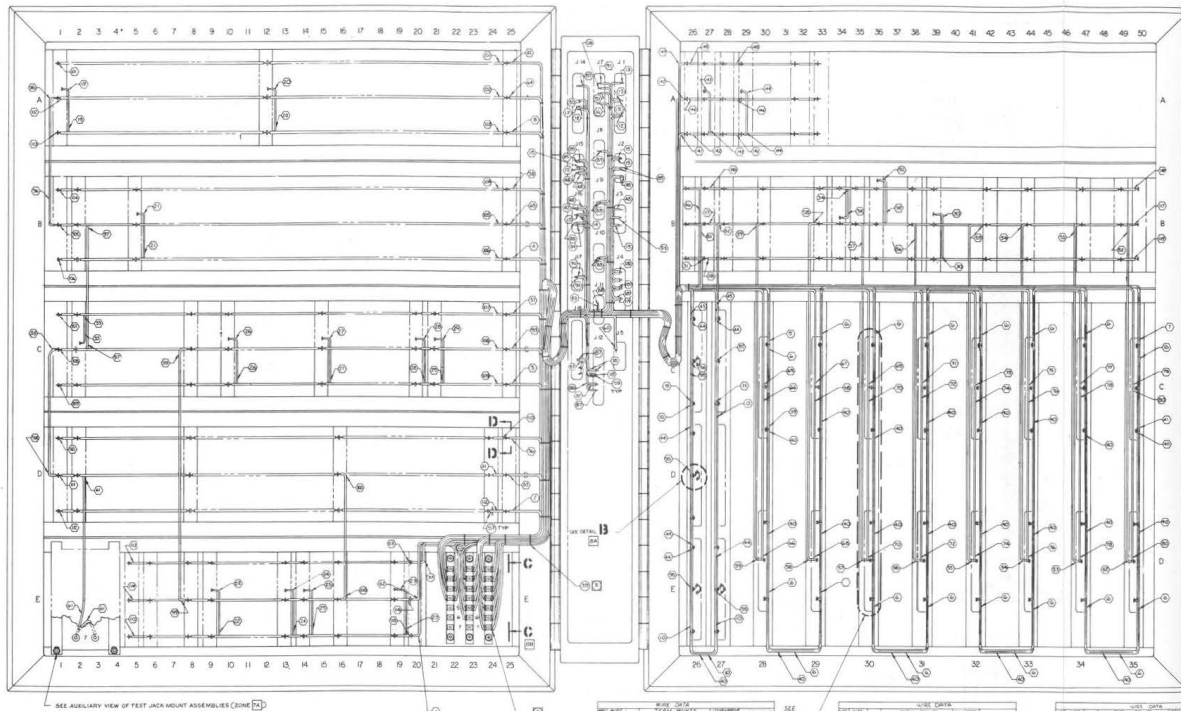
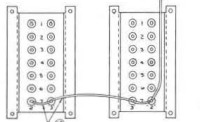
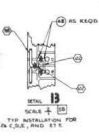
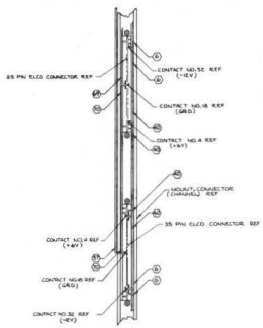
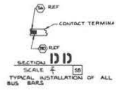
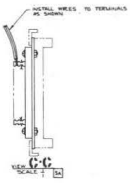


FRONT VIEW OF FRAME ASSEMBLIES (OPEN) PB250 COMPUTER

SA 140  
24 B

DATE	REV	DESCRIPTION	NOTES UNLESS OTHERWISE SPECIFIED
11/14/66	1	PACKAGED REL COMPUTER COMP	1. PB250 MODULE LOCATION DIAGRAM
11/14/66	2	PB250 MODULE LOCATION DIAGRAM	2. 350-D4593

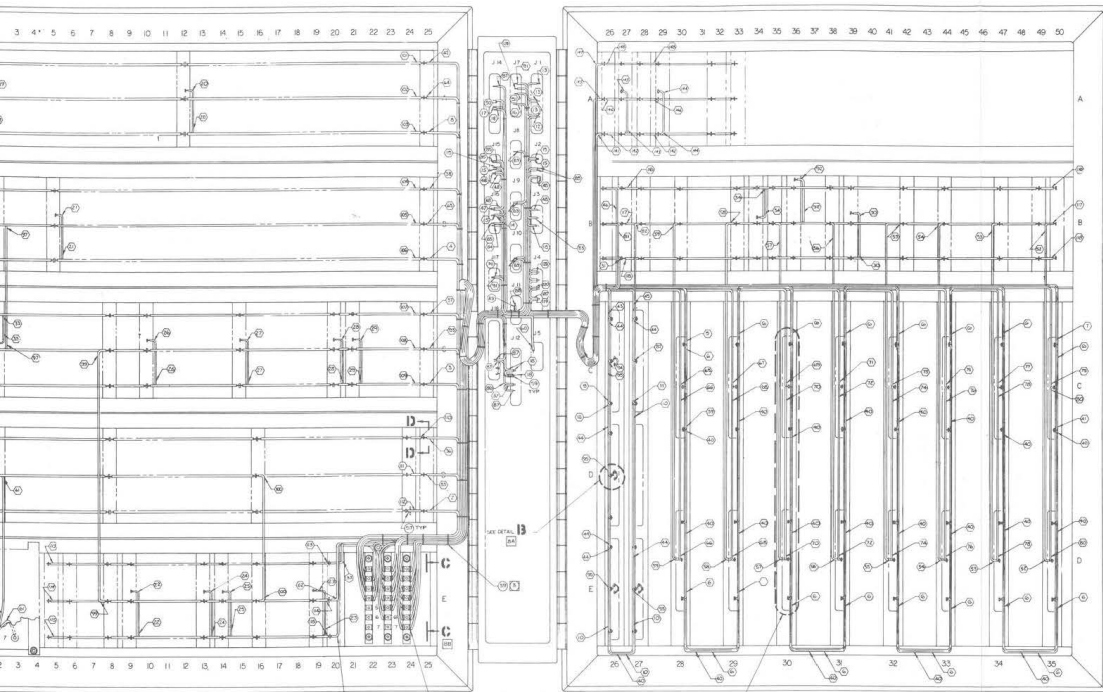
Figure 7-14 PB250 Module Location Diagram



REF	SYMBOL	DESCRIPTION	QUANTITY	REMARKS
101	RES	10K OHM	1	
102	RES	100K OHM	1	
103	RES	100 OHM	1	
104	RES	100K OHM	1	
105	RES	100 OHM	1	
106	RES	100K OHM	1	
107	RES	100 OHM	1	
108	RES	100K OHM	1	
109	RES	100 OHM	1	
110	RES	100K OHM	1	
111	RES	100 OHM	1	
112	RES	100K OHM	1	
113	RES	100 OHM	1	
114	RES	100K OHM	1	
115	RES	100 OHM	1	
116	RES	100K OHM	1	
117	RES	100 OHM	1	
118	RES	100K OHM	1	
119	RES	100 OHM	1	
120	RES	100K OHM	1	

REF	SYMBOL	DESCRIPTION	QUANTITY	REMARKS
201	RES	10K OHM	1	
202	RES	100K OHM	1	
203	RES	100 OHM	1	
204	RES	100K OHM	1	
205	RES	100 OHM	1	
206	RES	100K OHM	1	
207	RES	100 OHM	1	
208	RES	100K OHM	1	
209	RES	100 OHM	1	
210	RES	100K OHM	1	
211	RES	100 OHM	1	
212	RES	100K OHM	1	
213	RES	100 OHM	1	
214	RES	100K OHM	1	
215	RES	100 OHM	1	
216	RES	100K OHM	1	
217	RES	100 OHM	1	
218	RES	100K OHM	1	
219	RES	100 OHM	1	
220	RES	100K OHM	1	

REF	SYMBOL	DESCRIPTION	QUANTITY	REMARKS
301	RES	10K OHM	1	
302	RES	100K OHM	1	
303	RES	100 OHM	1	
304	RES	100K OHM	1	
305	RES	100 OHM	1	
306	RES	100K OHM	1	
307	RES	100 OHM	1	
308	RES	100K OHM	1	
309	RES	100 OHM	1	
310	RES	100K OHM	1	
311	RES	100 OHM	1	
312	RES	100K OHM	1	
313	RES	100 OHM	1	
314	RES	100K OHM	1	
315	RES	100 OHM	1	
316	RES	100K OHM	1	
317	RES	100 OHM	1	
318	RES	100K OHM	1	
319	RES	100 OHM	1	
320	RES	100K OHM	1	



ALTERNATE VIEW OF TEST JACK MOUNT ASSEMBLIES (CONT.)

REF ID	QTY	DESCRIPTION	REMARKS
1	1	TEST JACK MOUNT ASSEMBLY	
2	2	TEST JACK MOUNT ASSEMBLY	
3	2	TEST JACK MOUNT ASSEMBLY	
4	2	TEST JACK MOUNT ASSEMBLY	
5	2	TEST JACK MOUNT ASSEMBLY	
6	2	TEST JACK MOUNT ASSEMBLY	
7	2	TEST JACK MOUNT ASSEMBLY	
8	2	TEST JACK MOUNT ASSEMBLY	
9	2	TEST JACK MOUNT ASSEMBLY	
10	2	TEST JACK MOUNT ASSEMBLY	
11	2	TEST JACK MOUNT ASSEMBLY	
12	2	TEST JACK MOUNT ASSEMBLY	
13	2	TEST JACK MOUNT ASSEMBLY	
14	2	TEST JACK MOUNT ASSEMBLY	
15	2	TEST JACK MOUNT ASSEMBLY	
16	2	TEST JACK MOUNT ASSEMBLY	
17	2	TEST JACK MOUNT ASSEMBLY	
18	2	TEST JACK MOUNT ASSEMBLY	
19	2	TEST JACK MOUNT ASSEMBLY	
20	2	TEST JACK MOUNT ASSEMBLY	
21	2	TEST JACK MOUNT ASSEMBLY	
22	2	TEST JACK MOUNT ASSEMBLY	
23	2	TEST JACK MOUNT ASSEMBLY	
24	2	TEST JACK MOUNT ASSEMBLY	
25	2	TEST JACK MOUNT ASSEMBLY	

REF ID	QTY	DESCRIPTION	REMARKS
1	1	TEST JACK MOUNT ASSEMBLY	
2	2	TEST JACK MOUNT ASSEMBLY	
3	2	TEST JACK MOUNT ASSEMBLY	
4	2	TEST JACK MOUNT ASSEMBLY	
5	2	TEST JACK MOUNT ASSEMBLY	
6	2	TEST JACK MOUNT ASSEMBLY	
7	2	TEST JACK MOUNT ASSEMBLY	
8	2	TEST JACK MOUNT ASSEMBLY	
9	2	TEST JACK MOUNT ASSEMBLY	
10	2	TEST JACK MOUNT ASSEMBLY	
11	2	TEST JACK MOUNT ASSEMBLY	
12	2	TEST JACK MOUNT ASSEMBLY	
13	2	TEST JACK MOUNT ASSEMBLY	
14	2	TEST JACK MOUNT ASSEMBLY	
15	2	TEST JACK MOUNT ASSEMBLY	
16	2	TEST JACK MOUNT ASSEMBLY	
17	2	TEST JACK MOUNT ASSEMBLY	
18	2	TEST JACK MOUNT ASSEMBLY	
19	2	TEST JACK MOUNT ASSEMBLY	
20	2	TEST JACK MOUNT ASSEMBLY	
21	2	TEST JACK MOUNT ASSEMBLY	
22	2	TEST JACK MOUNT ASSEMBLY	
23	2	TEST JACK MOUNT ASSEMBLY	
24	2	TEST JACK MOUNT ASSEMBLY	
25	2	TEST JACK MOUNT ASSEMBLY	

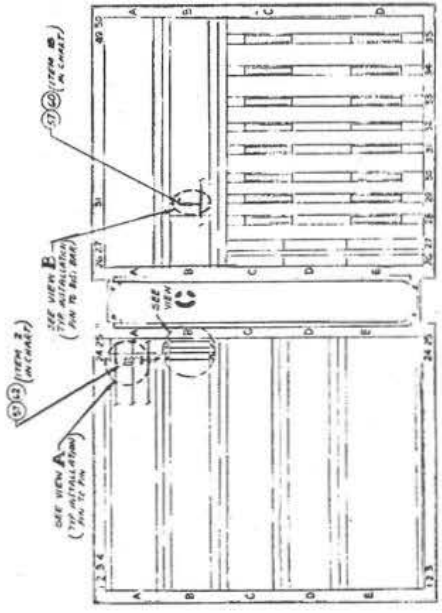
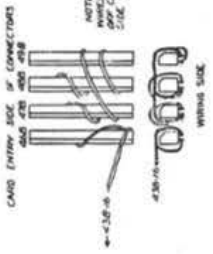
REF ID	QTY	DESCRIPTION	REMARKS
1	1	TEST JACK MOUNT ASSEMBLY	
2	2	TEST JACK MOUNT ASSEMBLY	
3	2	TEST JACK MOUNT ASSEMBLY	
4	2	TEST JACK MOUNT ASSEMBLY	
5	2	TEST JACK MOUNT ASSEMBLY	
6	2	TEST JACK MOUNT ASSEMBLY	
7	2	TEST JACK MOUNT ASSEMBLY	
8	2	TEST JACK MOUNT ASSEMBLY	
9	2	TEST JACK MOUNT ASSEMBLY	
10	2	TEST JACK MOUNT ASSEMBLY	
11	2	TEST JACK MOUNT ASSEMBLY	
12	2	TEST JACK MOUNT ASSEMBLY	
13	2	TEST JACK MOUNT ASSEMBLY	
14	2	TEST JACK MOUNT ASSEMBLY	
15	2	TEST JACK MOUNT ASSEMBLY	
16	2	TEST JACK MOUNT ASSEMBLY	
17	2	TEST JACK MOUNT ASSEMBLY	
18	2	TEST JACK MOUNT ASSEMBLY	
19	2	TEST JACK MOUNT ASSEMBLY	
20	2	TEST JACK MOUNT ASSEMBLY	
21	2	TEST JACK MOUNT ASSEMBLY	
22	2	TEST JACK MOUNT ASSEMBLY	
23	2	TEST JACK MOUNT ASSEMBLY	
24	2	TEST JACK MOUNT ASSEMBLY	
25	2	TEST JACK MOUNT ASSEMBLY	

NOTES: UNLESS OTHERWISE SPECIFIED:  
 1. DIMENSIONS ARE IN INCHES.  
 2. DIMENSIONS IN PARENTHESES ARE FOR REFERENCE ONLY.  
 3. DIMENSIONS IN BRACKETS ARE FOR REFERENCE ONLY.  
 4. DIMENSIONS IN SQUARE BRACKETS ARE FOR REFERENCE ONLY.  
 5. DIMENSIONS IN CIRCLES ARE FOR REFERENCE ONLY.  
 6. DIMENSIONS IN TRIANGLES ARE FOR REFERENCE ONLY.  
 7. DIMENSIONS IN DIAMONDS ARE FOR REFERENCE ONLY.  
 8. DIMENSIONS IN PARALLELOGRAMS ARE FOR REFERENCE ONLY.  
 9. DIMENSIONS IN OVALS ARE FOR REFERENCE ONLY.  
 10. DIMENSIONS IN HEPTAGONS ARE FOR REFERENCE ONLY.  
 11. DIMENSIONS IN OCTAGONS ARE FOR REFERENCE ONLY.  
 12. DIMENSIONS IN NONAGONS ARE FOR REFERENCE ONLY.  
 13. DIMENSIONS IN DECAGONS ARE FOR REFERENCE ONLY.  
 14. DIMENSIONS IN DODECAGONS ARE FOR REFERENCE ONLY.  
 15. DIMENSIONS IN TRIGONS ARE FOR REFERENCE ONLY.  
 16. DIMENSIONS IN SQUARES ARE FOR REFERENCE ONLY.  
 17. DIMENSIONS IN RECTANGLES ARE FOR REFERENCE ONLY.  
 18. DIMENSIONS IN RHOMBUSES ARE FOR REFERENCE ONLY.  
 19. DIMENSIONS IN TRAPEZOIDS ARE FOR REFERENCE ONLY.  
 20. DIMENSIONS IN KITES ARE FOR REFERENCE ONLY.  
 21. DIMENSIONS IN PARALLELOGRAMS ARE FOR REFERENCE ONLY.  
 22. DIMENSIONS IN RHOMBUSES ARE FOR REFERENCE ONLY.  
 23. DIMENSIONS IN TRAPEZOIDS ARE FOR REFERENCE ONLY.  
 24. DIMENSIONS IN KITES ARE FOR REFERENCE ONLY.  
 25. DIMENSIONS IN PARALLELOGRAMS ARE FOR REFERENCE ONLY.

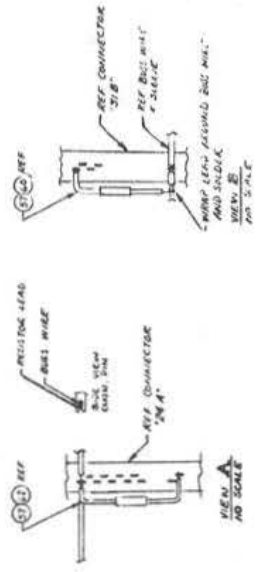
REF ID	QTY	DESCRIPTION	REMARKS
1	1	TEST JACK MOUNT ASSEMBLY	
2	2	TEST JACK MOUNT ASSEMBLY	
3	2	TEST JACK MOUNT ASSEMBLY	
4	2	TEST JACK MOUNT ASSEMBLY	
5	2	TEST JACK MOUNT ASSEMBLY	
6	2	TEST JACK MOUNT ASSEMBLY	
7	2	TEST JACK MOUNT ASSEMBLY	
8	2	TEST JACK MOUNT ASSEMBLY	
9	2	TEST JACK MOUNT ASSEMBLY	
10	2	TEST JACK MOUNT ASSEMBLY	
11	2	TEST JACK MOUNT ASSEMBLY	
12	2	TEST JACK MOUNT ASSEMBLY	
13	2	TEST JACK MOUNT ASSEMBLY	
14	2	TEST JACK MOUNT ASSEMBLY	
15	2	TEST JACK MOUNT ASSEMBLY	
16	2	TEST JACK MOUNT ASSEMBLY	
17	2	TEST JACK MOUNT ASSEMBLY	
18	2	TEST JACK MOUNT ASSEMBLY	
19	2	TEST JACK MOUNT ASSEMBLY	
20	2	TEST JACK MOUNT ASSEMBLY	
21	2	TEST JACK MOUNT ASSEMBLY	
22	2	TEST JACK MOUNT ASSEMBLY	
23	2	TEST JACK MOUNT ASSEMBLY	
24	2	TEST JACK MOUNT ASSEMBLY	
25	2	TEST JACK MOUNT ASSEMBLY	

Figure 7-15 PB250 DC Power Wiring Installation Drawing

NOTES:  
 1. MAINTAIN COMPONENTS FROM NO. 111 & 117 OF ASSY. ON PHILCO ASSY 123-122417.  
 2. THIS DRAWING IS USED TO INSTALL COMPONENTS LISTED ON PHILCO ASSY 123-122417.  
 3. THESE PARTS TO BE INSTALLED AFTER ALL OTHER PARTS HAVE BEEN CHECKED WITH THE WIRING TEST CARDS.



FRONT VIEW OF FRAME ASSY (OPEN) SHOWING WIRING SIDE OF CONNECTORS



ITEM NO.	DESCRIPTION	QUANTITY	UNIT
48	25430	3	3ANCS
49	27679	2	27679
50	36509	2	36509
51	36510	2	36510
52	22886	2	-12V BUIS
53	22886	2	22886
54	24824	2	24824
55	22826	2	22826
56	22828	2	22828
57	22830	2	-12V BUIS
58	18225	2	18225
59	18227	2	18227
60	17514	2	17514
61	20853	2	-12V BUIS
62	20859	2	20859
63	20863	2	20863
64	20865	2	20865
65	30005	2	30005
66	30008	2	30008
67	30004	2	-12V BUIS
68	30022	2	-12V BUIS
69	20015	2	20015
70	20018	2	20018
71	20019	2	20019
72	20018	2	20018
73	20019	2	20019
74	20019	2	20019
75	20015	2	20015
76	20015	2	20015
77	20015	2	20015
78	20015	2	20015
79	20015	2	20015
80	20015	2	20015
81	20015	2	20015
82	20015	2	20015
83	20015	2	20015
84	20015	2	20015
85	20015	2	20015
86	20015	2	20015
87	20015	2	20015
88	20015	2	20015
89	20015	2	20015
90	20015	2	20015
91	20015	2	20015
92	20015	2	20015
93	20015	2	20015
94	20015	2	20015
95	20015	2	20015
96	20015	2	20015
97	20015	2	20015
98	20015	2	20015
99	20015	2	20015
100	20015	2	20015

REFERENCE INFORMATION  
 ITEMS LISTED BELOW ARE ITEMS IN BOM OF PB-250 ASSY 123-122417

5	IS SLEEVING
6	IS RES. 6.8K. 1/4W. 15%
7	IS RES. 2.7K. 1/4W. 15%
8	IS RES. 20K. 1/4W. 15%
9	IS RES. 15K. 1/4W. 15%
10	IS RES. 10K. 1/4W. 15%
11	IS RES. 1K. 1/4W. 15%
12	IS RES. 100K. 1/4W. 15%
13	IS RES. 10K. 1/4W. 15%
14	IS RES. 1.5K. 1/4W. 15%
15	IS RES. 1.2K. 1/4W. 15%
16	IS DUAL. AN2000
17	IS RES. 1.5K. 1/4W. 15%
18	IS RES. 1.2K. 1/4W. 15%
19	IS RES. 1.5K. 1/4W. 15%
20	IS RES. 1.2K. 1/4W. 15%

COMPONENT INSTALLATION CHART

ITEM NO.	DESCRIPTION	QUANTITY	UNIT
1	111-1	1	111-1
2	111-2	1	111-2
3	111-3	1	111-3
4	111-4	1	111-4
5	111-5	1	111-5
6	111-6	1	111-6
7	111-7	1	111-7
8	111-8	1	111-8
9	111-9	1	111-9
10	111-10	1	111-10
11	111-11	1	111-11
12	111-12	1	111-12
13	111-13	1	111-13
14	111-14	1	111-14
15	111-15	1	111-15
16	111-16	1	111-16
17	111-17	1	111-17
18	111-18	1	111-18
19	111-19	1	111-19
20	111-20	1	111-20
21	111-21	1	111-21
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44	111-44	1	111-44
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46	111-46	1	111-46
47	111-47	1	111-47
48	111-48	1	111-48
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53	111-53	1	111-53
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65	111-65	1	111-65
66	111-66	1	111-66
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68	111-68	1	111-68
69	111-69	1	111-69
70	111-70	1	111-70
71	111-71	1	111-71
72	111-72	1	111-72
73	111-73	1	111-73
74	111-74	1	111-74
75	111-75	1	111-75
76	111-76	1	111-76
77	111-77	1	111-77
78	111-78	1	111-78
79	111-79	1	111-79
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92	111-92	1	111-92
93	111-93	1	111-93
94	111-94	1	111-94
95	111-95	1	111-95
96	111-96	1	111-96
97	111-97	1	111-97
98	111-98	1	111-98
99	111-99	1	111-99
100	111-100	1	111-100

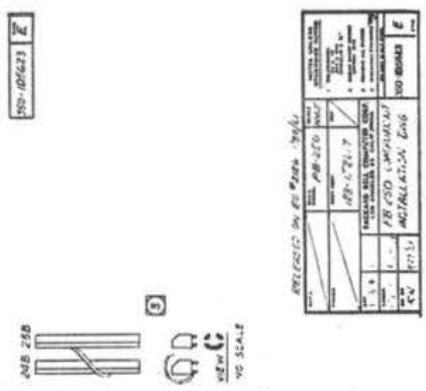
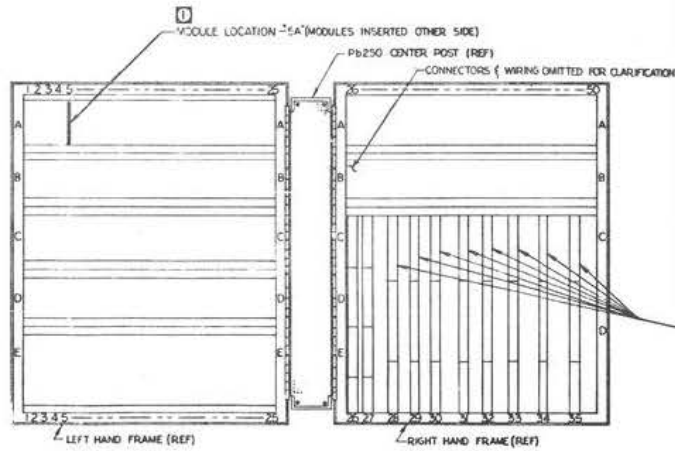


Figure 7-16 PB250 Component Installation Drawing



FRONT VIEW OF FRAME ASSEMBLIES (OPEN)-PB250 COMPUTER

NOTES: UNLESS OTHERWISE SPECIFIED

D LOCATION 'SA', AS SHOWN, WOULD BE THE ACTUAL LOCATION OF 'MODULE TF-100' CONNECTOR IN THE COMPUTER.

NO.	MODULE MODEL NO. (CONNECTORS)														
	XCG100	CD100	MSR-2	MSR-1	BD100	EF100	TF100	DS100	DG101	DS102	TR100	FC100	EF101	SA-100	
KEYING →	3-13	3-15	3-23	3-27	3-17	3-21	3-25	3-33	3-31	3-29	3-19	3-7	3-5	5-23	
LOCATION- IN FRAME ASSEMBLY	25 B	22 B	7 A	20 C	10 A	16 A	2 A	6 A	4 A	1 A	20 C	24 A	19 C	24 B	
			2 B	29 C	17 B	19 A	3 A	6 B	11 A	12 A	26 C	25 A	8 E		
			7 D	30 C	27 C	19 B	D 5 A	10 B	15 A	17 A	26 E	23 A	9 A		
			14 D	31 C	20 A	23 C	7 B	20 B	14 A	5 B	27 E		23 B		
			22 D	32 C	20 E	25 C	11 B	1 C	15 A	13 B			26 B		
				35 C	10 A	25 D	12 B	4 C	16 A	15 B			49 B		
				34 C	10 A		21 B	7 C	1 E	30 B			22 A		
				35 C			3 C	9 C	4 B	34 B					
				28 C			5 C	12 C	8 B	39 B					
				29 C			8 C	14 C	9 B	2 C					
				30 C			11 C	16 C	14 B	6 C					
				31 D			13 C	18 C	16 B	10 C					
				32 C			24 D	16 C	15 B	15 C					
				33 D			19 C	17 C	27 B	17 C					
				34 D			9 C	16 E	28 B	21 C					
				35 C			17 E	5 E	29 B	24 C					
							44 B		31 B	2 D					
									32 B	5 D					
									44 E	33 B	10 D				
									6 E	35 B	12 D				
										36 B	19 D				
										37 B	9 E				
										38 B	13 E				
										40 B	14 E				
										41 B	15 E				
										42 B	22 C				
										1 D	20 C				
										3 D	45 B				
										4 D	27 A				
										6 D	29 A				
										11 D					
										13 D					
										20 D					
										21 D					
										10 C					
										11 E					
										12 E					
										18 E					
										21 A					
										46 B					
										45 B					
										47 B					
										48 B					
										26 A					
										28 A					

THESE CONNECTORS ARE INVERTED WITH RESPECT TO ALL OTHER CONNECTORS

350-D4244 H

RELEASED ON R.O. 12/13/83-P-60

DATE	BY	REASON	APPROVED
PACKARD BELL COMPUTER CORP. LOS ANGELES, CALIFORNIA		350-1 H	
PB250 CONNECTOR LOCATION DIAGRAM		D-4244	

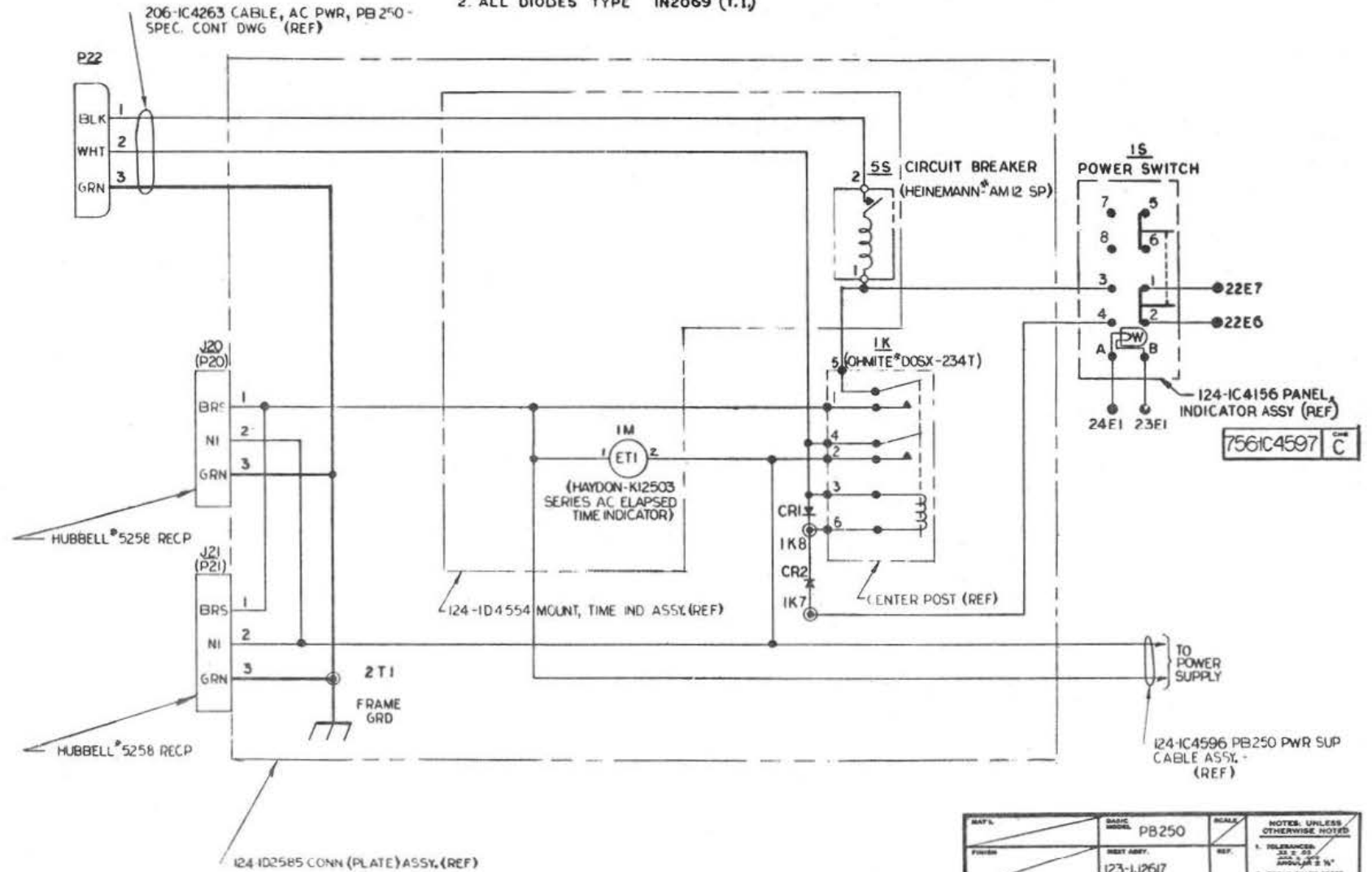
Figure 7-17 PB250 Connector Location Diagram



NOTES: UNLESS OTHERWISE SPECIFIED

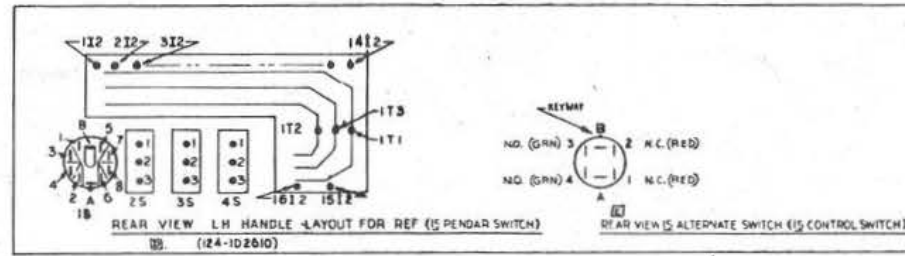
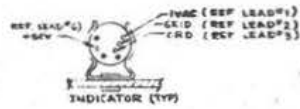
1. ABBREVIATIONS PER MIL-STD-12.
2. ALL DIODES TYPE IN2069 (T.1)

7-21



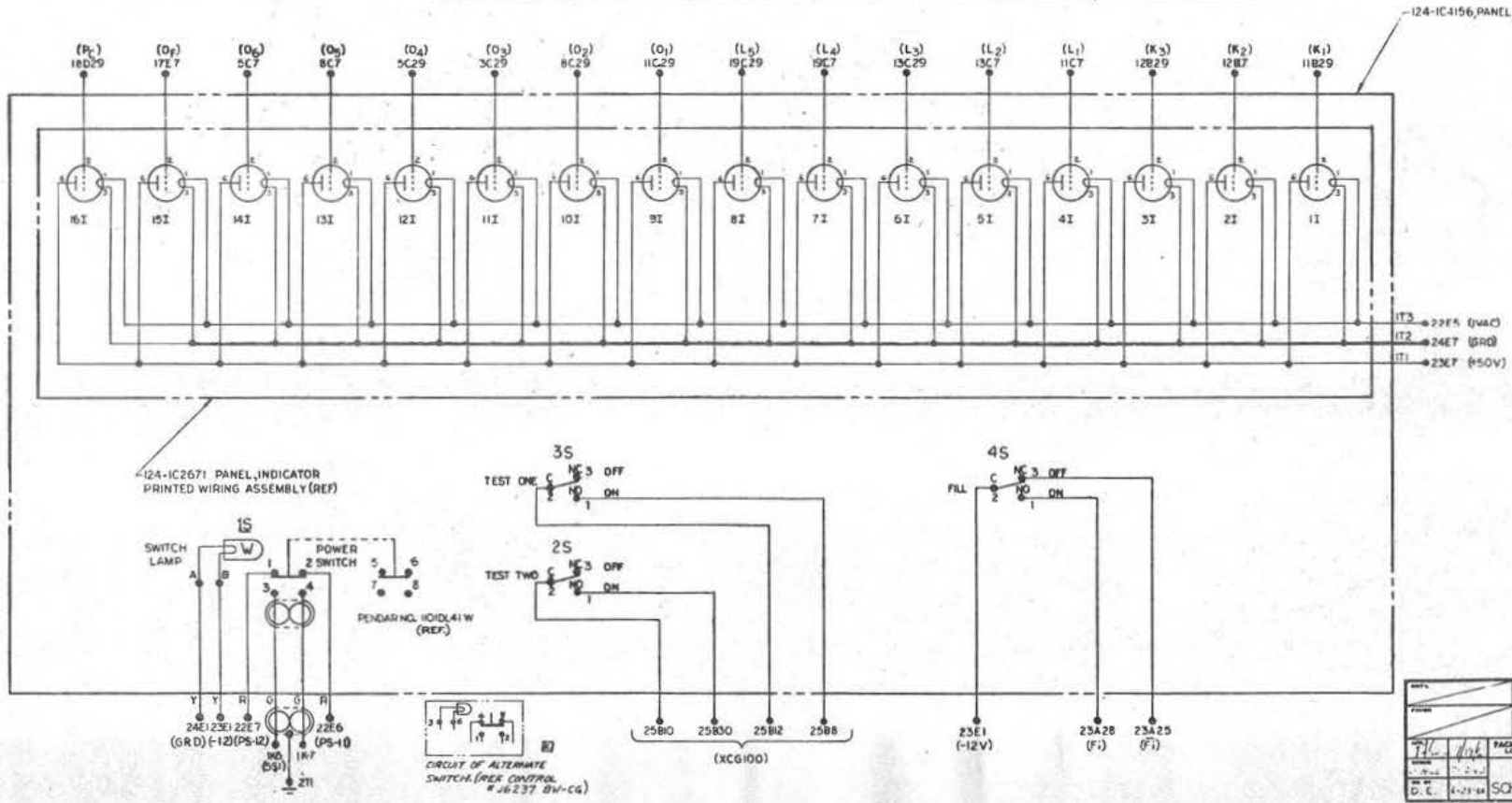
DATE	BASIC MODEL	REVISION	NOTES: UNLESS OTHERWISE NOTED
	PB250		1. TOLERANCES: 25.0 ± .05 ANGULAR ± 1/4"
	123-1J2617		2. BREAK SHARP CORNER APPROX. .015
APP. <i>W. P.</i> 2/1/60	PACKARD BELL COMPUTER CORP. LOS ANGELES 28, CALIFORNIA		3. REMOVE ALL SWIRL 4. MACHINED FINISHES TYP.
CHKD. JH 2-8-60	PB 250 AC POWER SCHEMATIC DIAGRAM		DO NOT SCALE DIMS
DR. BY M.C. 9-1-60			756-IC4597 C

Figure 7-18 PB250 AC Power Schematic



Handwritten notes: K4, 6E7, 7

7-22



756-D4411

REV		PB250	REV	
DATE		123-1J2617	DATE	
F.L. D.E.		PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		PHOTO LITHOGRAPH REPRODUCTION 1. 123-1J2617 2. 756-D4411 3. 123-1J2617 4. 123-1J2617 5. 123-1J2617 6. 123-1J2617 7. 123-1J2617 8. 123-1J2617 9. 123-1J2617 10. 123-1J2617 11. 123-1J2617 12. 123-1J2617 13. 123-1J2617 14. 123-1J2617 15. 123-1J2617 16. 123-1J2617 17. 123-1J2617 18. 123-1J2617 19. 123-1J2617 20. 123-1J2617 21. 123-1J2617 22. 123-1J2617 23. 123-1J2617 24. 123-1J2617 25. 123-1J2617 26. 123-1J2617 27. 123-1J2617 28. 123-1J2617 29. 123-1J2617 30. 123-1J2617 31. 123-1J2617 32. 123-1J2617 33. 123-1J2617 34. 123-1J2617 35. 123-1J2617 36. 123-1J2617 37. 123-1J2617 38. 123-1J2617 39. 123-1J2617 40. 123-1J2617 41. 123-1J2617 42. 123-1J2617 43. 123-1J2617 44. 123-1J2617 45. 123-1J2617 46. 123-1J2617 47. 123-1J2617 48. 123-1J2617 49. 123-1J2617 50. 123-1J2617 51. 123-1J2617 52. 123-1J2617 53. 123-1J2617 54. 123-1J2617 55. 123-1J2617 56. 123-1J2617 57. 123-1J2617 58. 123-1J2617 59. 123-1J2617 60. 123-1J2617 61. 123-1J2617 62. 123-1J2617 63. 123-1J2617 64. 123-1J2617 65. 123-1J2617 66. 123-1J2617 67. 123-1J2617 68. 123-1J2617 69. 123-1J2617 70. 123-1J2617 71. 123-1J2617 72. 123-1J2617 73. 123-1J2617 74. 123-1J2617 75. 123-1J2617 76. 123-1J2617 77. 123-1J2617 78. 123-1J2617 79. 123-1J2617 80. 123-1J2617 81. 123-1J2617 82. 123-1J2617 83. 123-1J2617 84. 123-1J2617 85. 123-1J2617 86. 123-1J2617 87. 123-1J2617 88. 123-1J2617 89. 123-1J2617 90. 123-1J2617 91. 123-1J2617 92. 123-1J2617 93. 123-1J2617 94. 123-1J2617 95. 123-1J2617 96. 123-1J2617 97. 123-1J2617 98. 123-1J2617 99. 123-1J2617 100. 123-1J2617
INDICATOR		SCHEMATIC (A3-FAM)		756-D4411

Figure 7-19 Indicators Schematic