NATIONAL CLASS 310-2
ELECTRONIC DATA PROCESSOR

ENGINEERING DESCRIPTION

VOLUME 2
MAINTENANCE

National*

For

The National Cash Register Company

Dayton 9, Ohio

BY THE CONTROL DATA CORPORATION

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CDC 101

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CHAPTER IV

MAINTENANCE

This section presents complete logic package maintenance information for the computer. When mechanical adjustments are needed for the high-speed punch, typewriter, etc., refer to commercial manuals supplied with those equipments.

Control Data:	350 Paper Tape Reader, Technical Manual (for photoelectric reader).
Teletype:	Bulletin #215B, Technical Manual; High Speed Tape Punch Set (BRPE-11).
Teletype:	Bulletin #1154B; Parts, High Speed Tape Punch Set (BRPE-11).

System maintenance may be preventive or corrective. Preventive maintenance is designed to eliminate failures during operation by lubricating, cleaning, running test programs, and checking for worn or marginal parts. Corrective maintenance consists of diagnosing, locating, and remedying the cause of a failure after it has occurred.

TEST EQUIPMENT AND TOOLS

Standard VOM
Oscilloscope (Tektronix 543 or equivalent)
Model 150 Card Tester
Taper Pin insertion tool
Taper Pin crimping tool
Card extender
Usual hand tools for electrical and mechanical maintenance

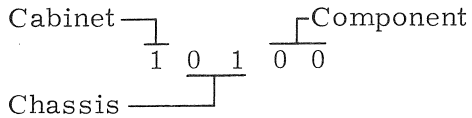
CORRECTIVE MAINTENANCE AIDS

The ability of a maintenance engineer to locate malfunctions in the equipment depends upon three factors: his knowledge of system logic, his insight, and his ability to use the maintenance aids. Four aids to the maintenance personnel in this instruction book series are:

1) Equation File
2) Card Placement Charts
3) Logic, Schematic, and Wiring Diagrams
4) Instruction Timing Charts

COMPONENT NUMBERING SYSTEM

Military standards have been followed in the numbering of cabinets, chassis, and components. The ten-thousands system, has been used as shown below.



The computer cabinet designation is 10000.

When identifying components by means of frame labeling or through designations on drawings or photographic call-outs, the shortest designator is used, consistent with clearness. In addition to the full length designation (J10102, for example), two shorthand methods are employed.

The first method describes components by affixing a chassis number to the component designator and is used where there might be some confusion as to the number of a chassis carrying the particular component:

1J02

The chassis number always precedes the component designator in this system.

The second shorthand system is used whenever the chassis to which the component is attached is clearly identifiable or in other respects unmistakable. This method is used in labeling component locations on cabinet and chassis frames:

J02

Components such as blowers which are mounted within a cabinet but not on a chassis carry the prefix "0", either expressed or implied.

(0) B01

The relay panel of the computer cabinet (chassis 10200) uses a standard coordinate system to locate the relays. Thus, relay KC01 is found in the third row from the top (row C) and at the extreme left of the panel when facing the relay - not the wiring - side. Under the coordinate system individual component locations are not labeled.

The computer cabinet contains several chassis.

Chassis No.	Use
10100	Computer Logic
10200	Console and Relay Chassis
10300	Interchange Panel
10400	Punch Control Unit
10500	60 ~ Power Supply
10700	Photoelectric Reader
10800	High-Speed Punch

LOGIC MAINTENANCE

This section contains information to help maintenance personnel in trouble-shooting the equipment. Photographs showing important component positions and chassis locations within the various cabinets are included, as well as diagrams showing the method of numbering pins or connection points on relays, digital display units, etc.

COMPONENT CONNECTION POINTS

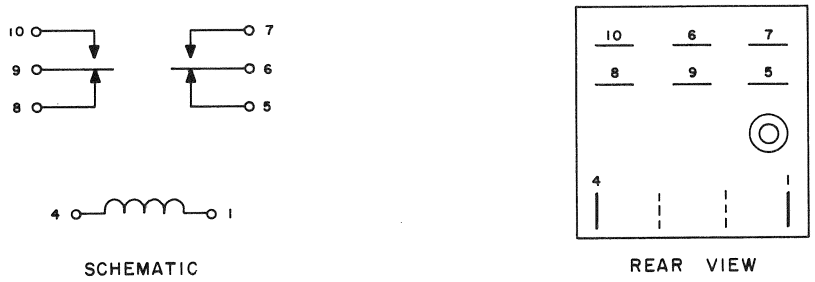
Figure 4-1 shows the schematic and connection diagrams for two types of relays used in the equipment. Figure 4-2 shows the schematic diagram and pin arrangement for a typical 4C type lever switch, a fuseholder, and a digital display unit. When replacing the fuseholder, the "A" contact must carry the hot lead to the fuse. This assures that contact "B" -in close proximity to the grounded mounting ring on indicating fuseholders of this type - is not live after the fuse blows.

GENERAL COMPONENT LAYOUT

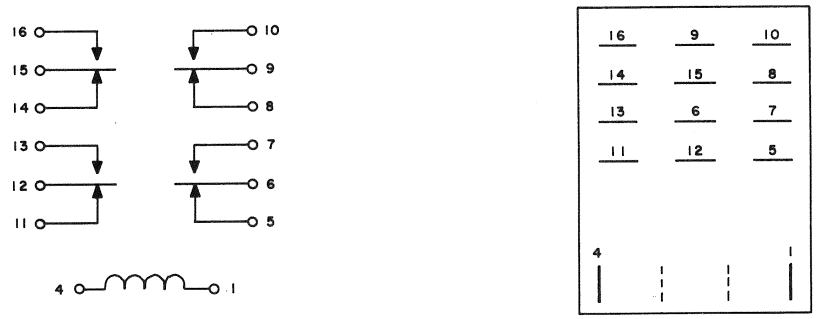
Figures 4-3 through 4-10 are views of the main computer cabinet which show most of the important components and connectors. Figure 4-10 is a picture of the memory stack.

STATUS INDICATORS

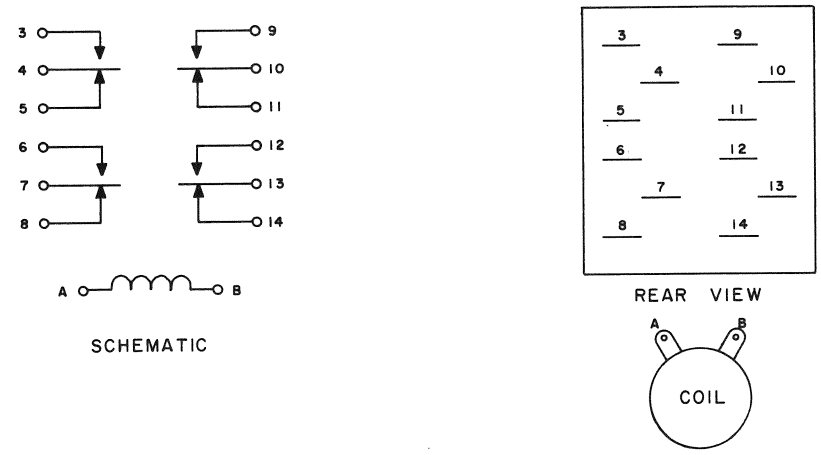
Special lights on the console display panel indicate the condition of the program currently being executed:



ALLIED CONTROL
2C

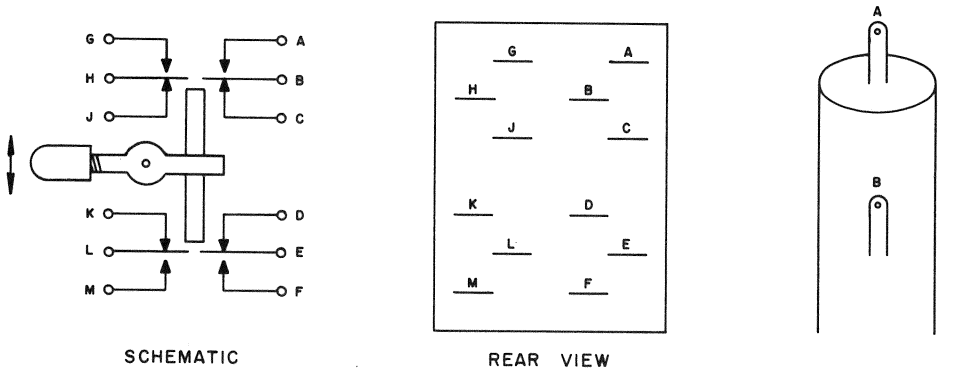


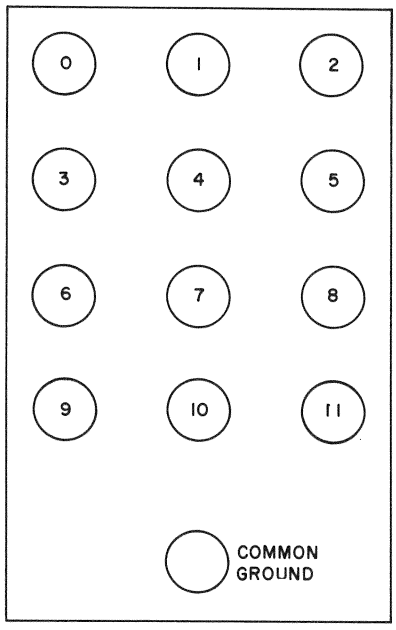
ALLIED CONTROL
4C



POTTER & BRUMFIELD (K1, K2)
4C

Figure 4-1. Relay Connections





DIGITAL DISPLAY (DD)
UNIT
(REAR VIEW)

Figure 4-2. Lever Switch, Fuseholder, and Digital Display Unit Connections

Status Panel (DS13)

GREEN background light: Computer running

RED background light: Computer stopped

The red light will indicate one of the following conditions, as evidenced by the symbol within the background light:

ERR	Error Stop	A	Storage reference cycle to be executed when Run-Step switch is next actuated
SEL	Computer waiting for selected external equipment to respond	B, C	
OUT	Output (73, 74) instruction	D	
IN	Input (72, 76) instruction		

P Register Panel (DS12-DS09)

Displayed numerals indicate octal address of next storage reference.

A Register Panel (DS08-DS05)

Displayed numerals indicate octal address of next storage reference.

RED background light: Main timing fault

Z Register Panel (DS04-DS01)

Displayed numerals indicate register contents (octal).

GREEN background light: Number displayed is a program step.

COMPUTER

Logic maintenance of the computer involves determining the area to be investigated through maintenance tests and subsequent console diagnosis of instructions causing the malfunction, and examining this area with an oscilloscope.

Maintenance tests will narrow the field of instruction suspected of giving trouble. The tests to be performed will be determined by the type of trouble: input, output, storage, and so forth.

The console with its display of register contents, colored background lights and operating controls provides for the first level of diagnosis. A test program indicates a malfunction and the general area of the computer causing it. To localize the failure to a given register or instruction the basic procedure at the console is to execute, in the step mode, the instructions which involve the area containing the malfunction. Compare the results displayed on the console with those known to be correct. Discrepancies can be from several possible causes. Enter more instructions (manually) and step

through to eliminate causes. After several repetitions of this procedure, the area of the malfunction will be limited to a great degree.

After console diagnosis has indicated the circuits which may be causing the malfunction examine these circuits with an oscilloscope.

In some cases observation of circuits in a static condition is sufficient; however, examination of dynamic circuit conditions is often required. This is done by repeated execution of an instruction that uses the circuit. To repeat an instruction, store it and a jump instruction in an unused area of storage to form a loop. The analyzing instruction may be repeated at a high speed rate (Run) or by storage reference cycles (Step).

Information for localizing the cause to a group of circuits and then to an individual circuit is contained in:

1) the instruction timing charts (Appendix C)
2) logic diagrams (volume 3)
3) the file of equations (volume 4)

The jack location and test point information required in taking waveforms for each circuit are provided by equations and diagrams.

Waveforms taken at the circuit test point indicate directly the circuit output. However, test point waveforms are the inversion of the circuit inputs. The common ground connection for the oscilloscope is at the outer chassis edge. A synchronizing signal for the oscilloscope can be obtained from the test point of another circuit. Typically the synchronizing source is chosen to produce a signal just in advance of that time when a circuit is to be examined.

To look at signals on the individual pins of a card, remove the bar which holds that row of cards in position, remove the card, insert the card extender, and plug the card into the extender. Waveforms of representative cards provide a basis for determining the condition of the card under test.

PRINTED CIRCUIT CARDS

Corrective maintenance isolates the trouble to some electrical component such as a blown fuse, loose E-strip connection, broken cable lead, etc., or to some electronic component, such as a printed circuit card. This section provides a series of waveforms against which the individual cards may be compared, and gives procedures for determining which component on the faulty card is defective. A definitive analysis of each

card is presented in the 150 C ard Tester manual. For all waveforms the oscilloscope has been connected so that negative voltages produce upward deflection.

Logic Cards

Logic cards are all standard inverters (figure 4-11), control delays (figure 4-12) and flip-flops. The flip-flop waveform is not given, since the pulse width from this type of card is an arbitrary value depending on set and clear signals. The rise time of the pulse should be substantially under 0.1 μsec. Anything slower than this approaches the area where clock pulses (nominally 0.2 μsec wide) may not act on the pulse at the right time or, if they do, produce a runt pulse.

Storage Cards

In general, these waveforms were taken with the computer in Sweep mode, which accounts for the composite nature of the oscillographs. In figure 4-14, the waveform shows both the working time of the diverter (rectangular portion) and also the period when it is not in use (base line). Type 53 is omitted due to its similarity to the standard inverter card.

Adequate spares are provided for all card types in the system. If an oscilloscope check points to a card as the source of trouble, that card is replaced and set aside for future examination. The most definitive check on faulty cards is made with the card tester which will show up low beta transistors as well as shorted, open, or reversed diodes.

In lieu of the card tester, the ohmic value of all resistive components, as well as the presence of open or shorted diodes, may be determined by using the OHMS setting of a standard VOM. The T-1G diode used throughout the card types has a back resistance varying from 50K to 200K ohms. The forward resistance is a function of the current flowing through it. Average readings of 4-5 on the X1 scale, or 20-30 on the X10 scale are satisfactory. After determining the direction of current flow in the ohm meter circuit, it is well to mark the meter leads to facilitate future diode checking.

Schematic diagrams for every card type used in the computer are given in Appendix E to this volume. In the lower right-hand corner of each is a layout of the card to aid in locating faulty components.

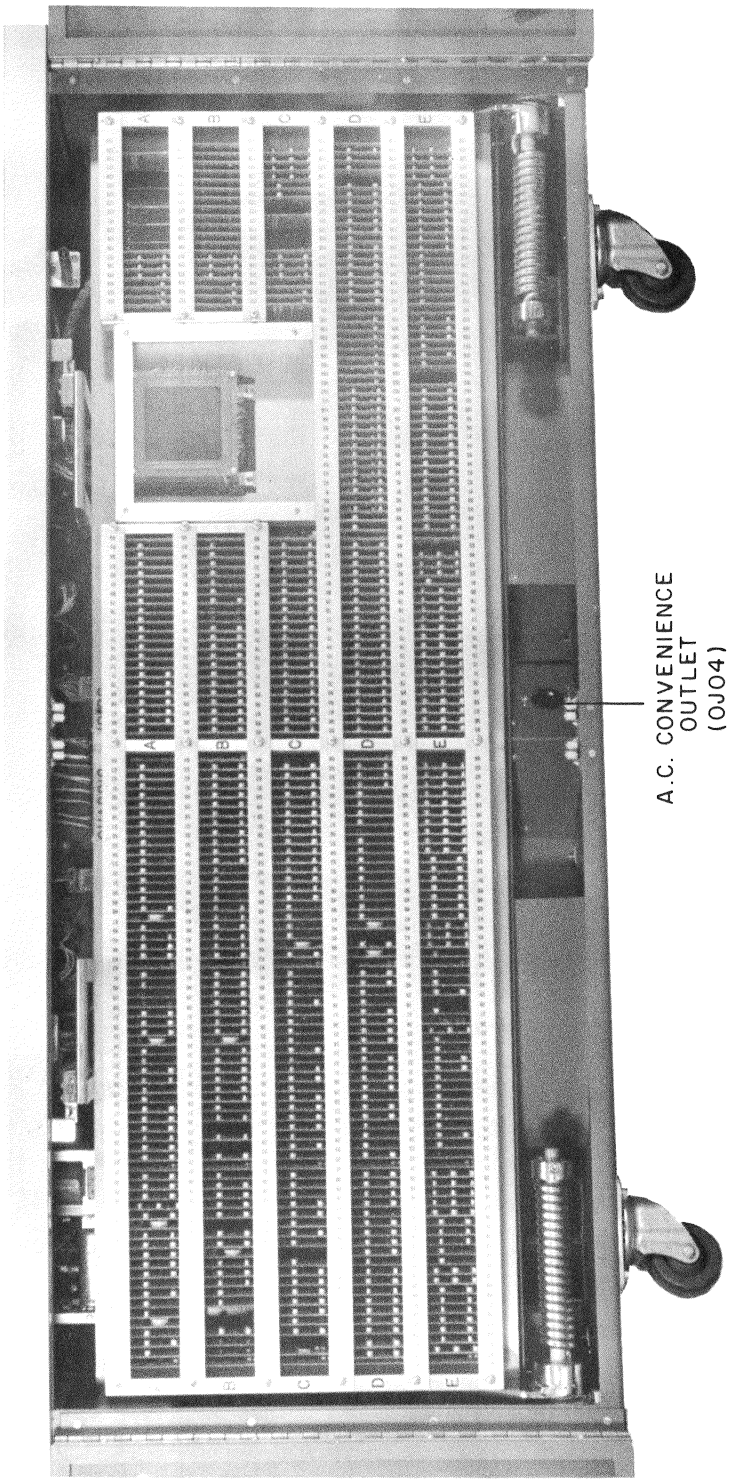


Figure 4-3. Computer Cabinet, Rear View with Doors Open

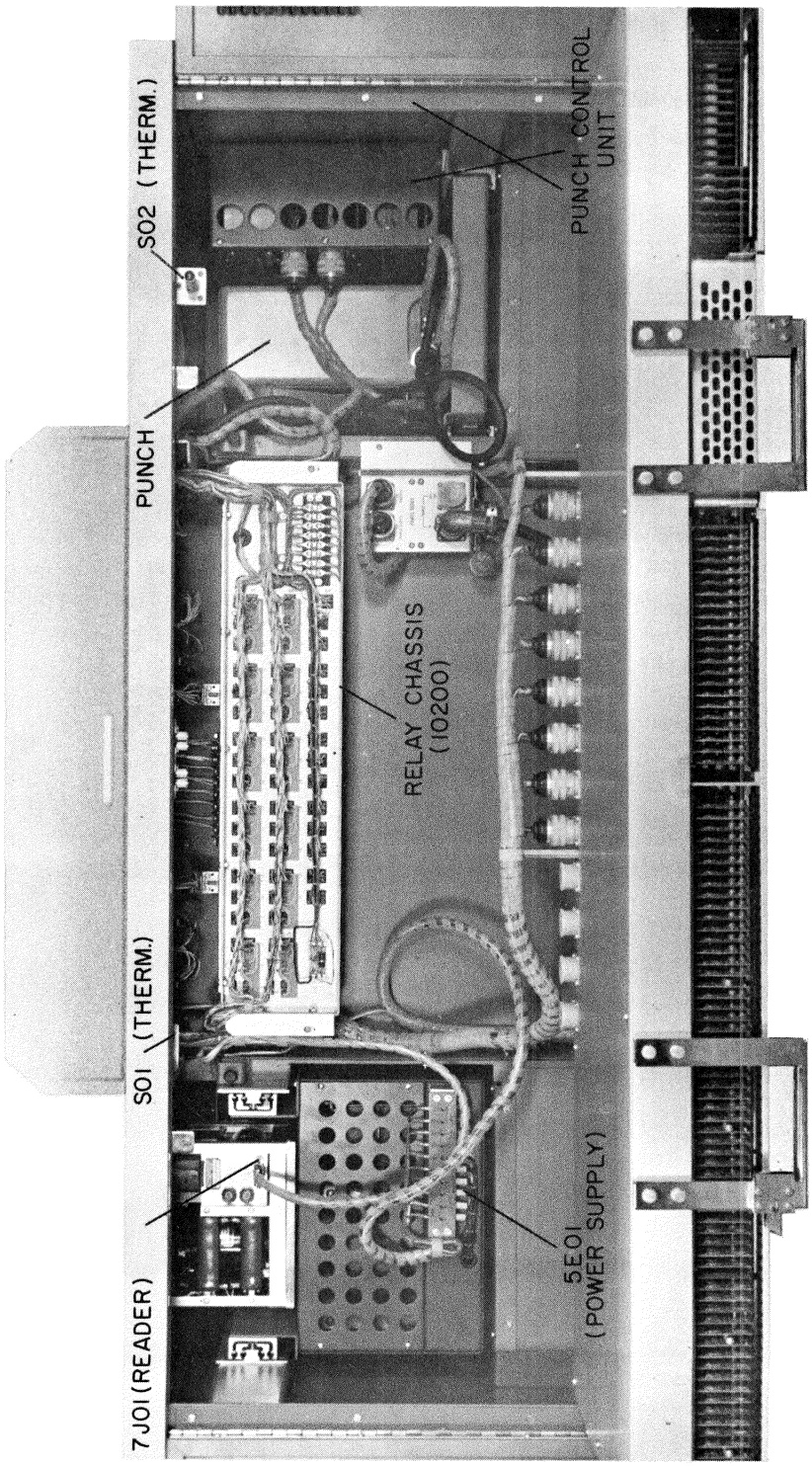


Figure 4-4. Computer Cabinet, Rear View with Logic Chassis Lowered

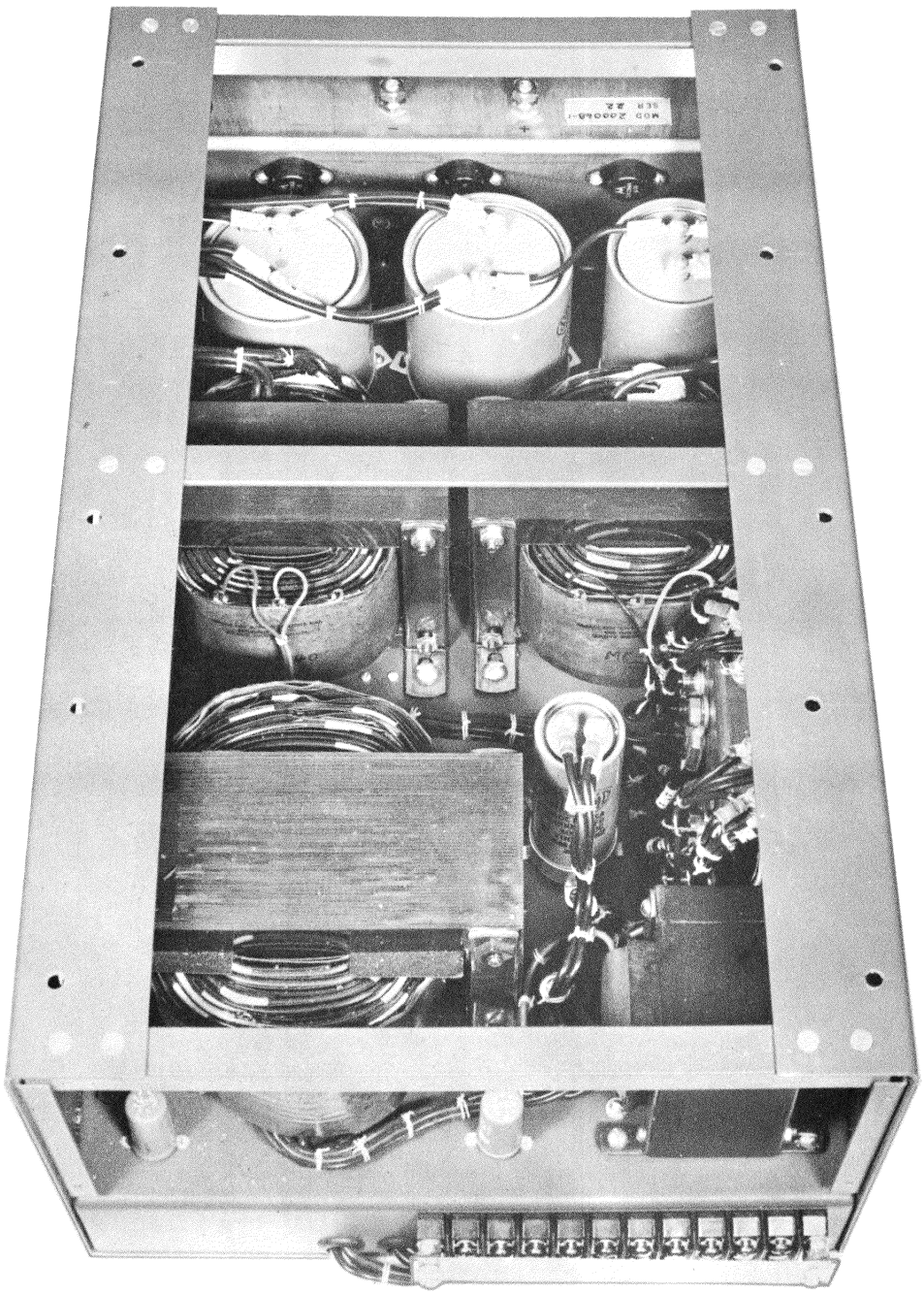


Figure 4-5. 60-cycle Power Supply

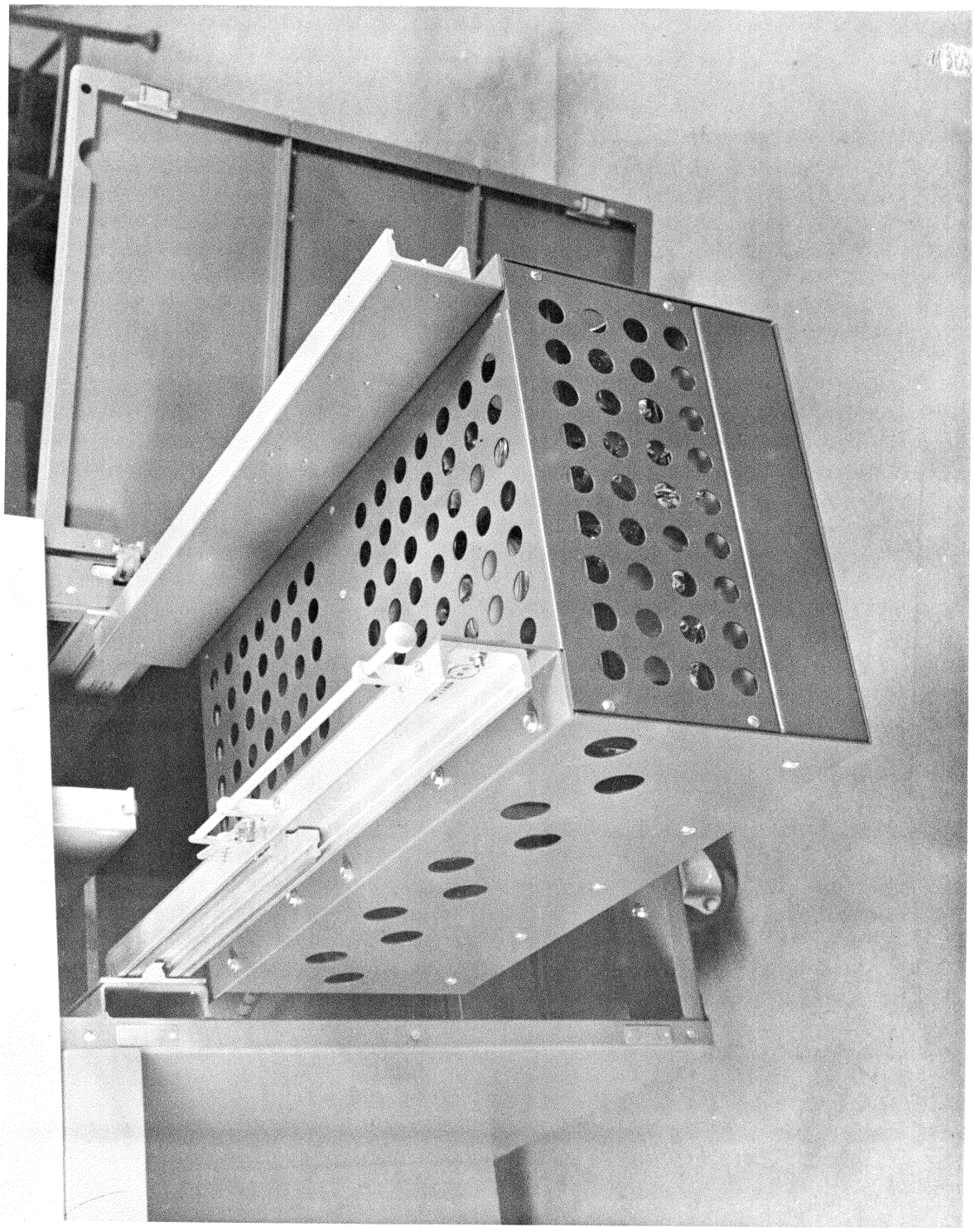


Figure 4-6. 60-cycle Power Supply Extended

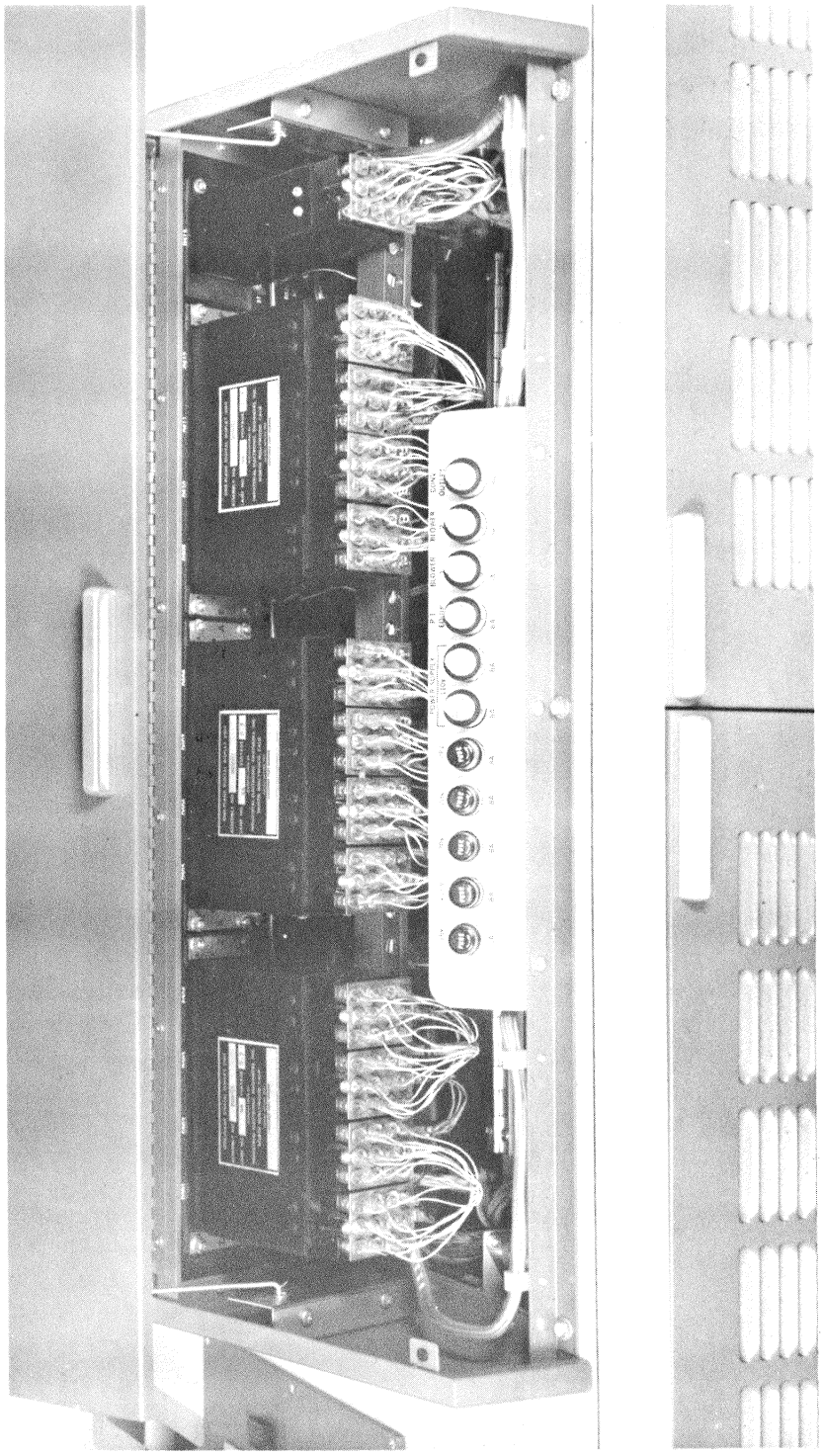


Figure 4-7. Console; Rear View with Cover Open

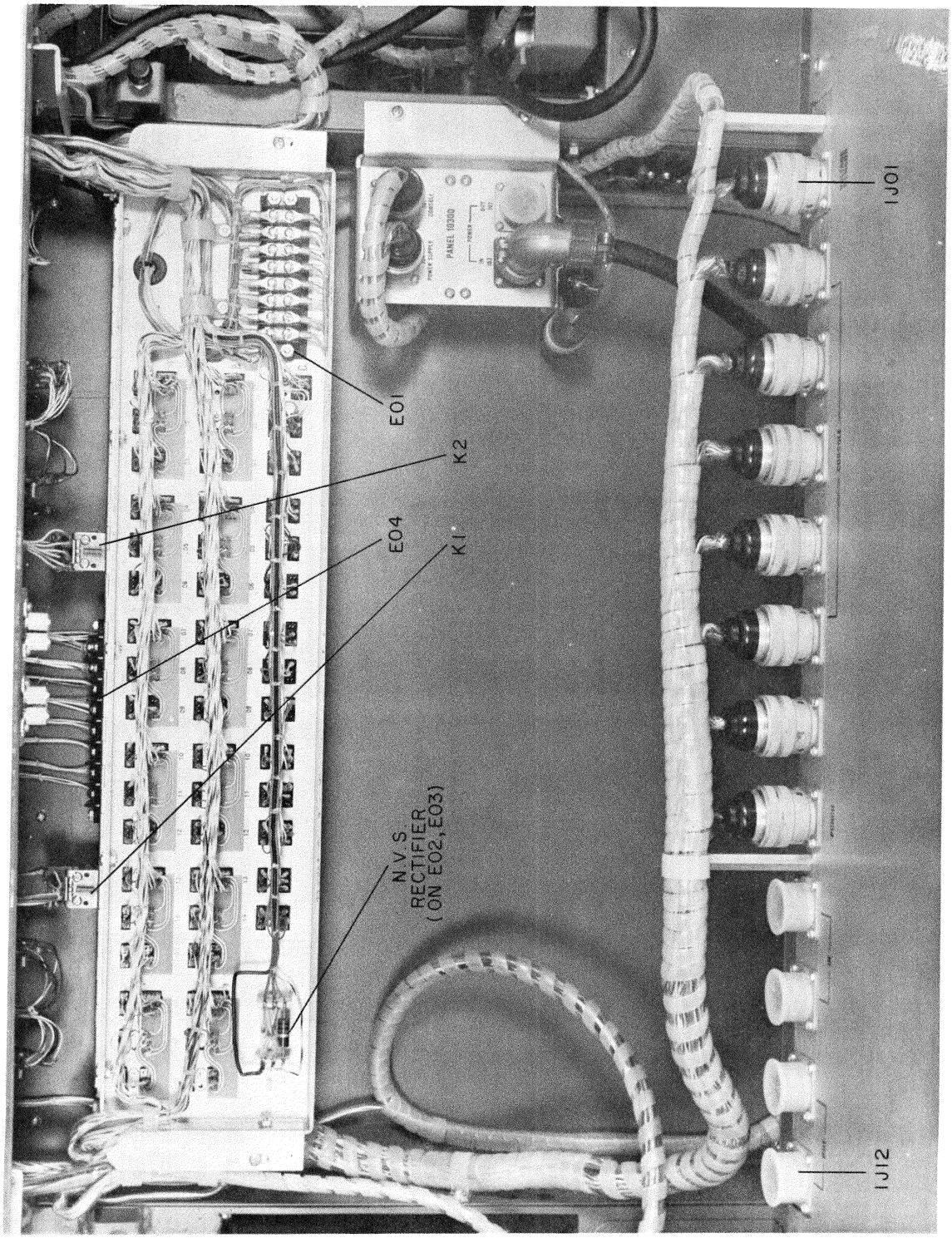


Figure 4-8. Relay Panel, Chassis 10200

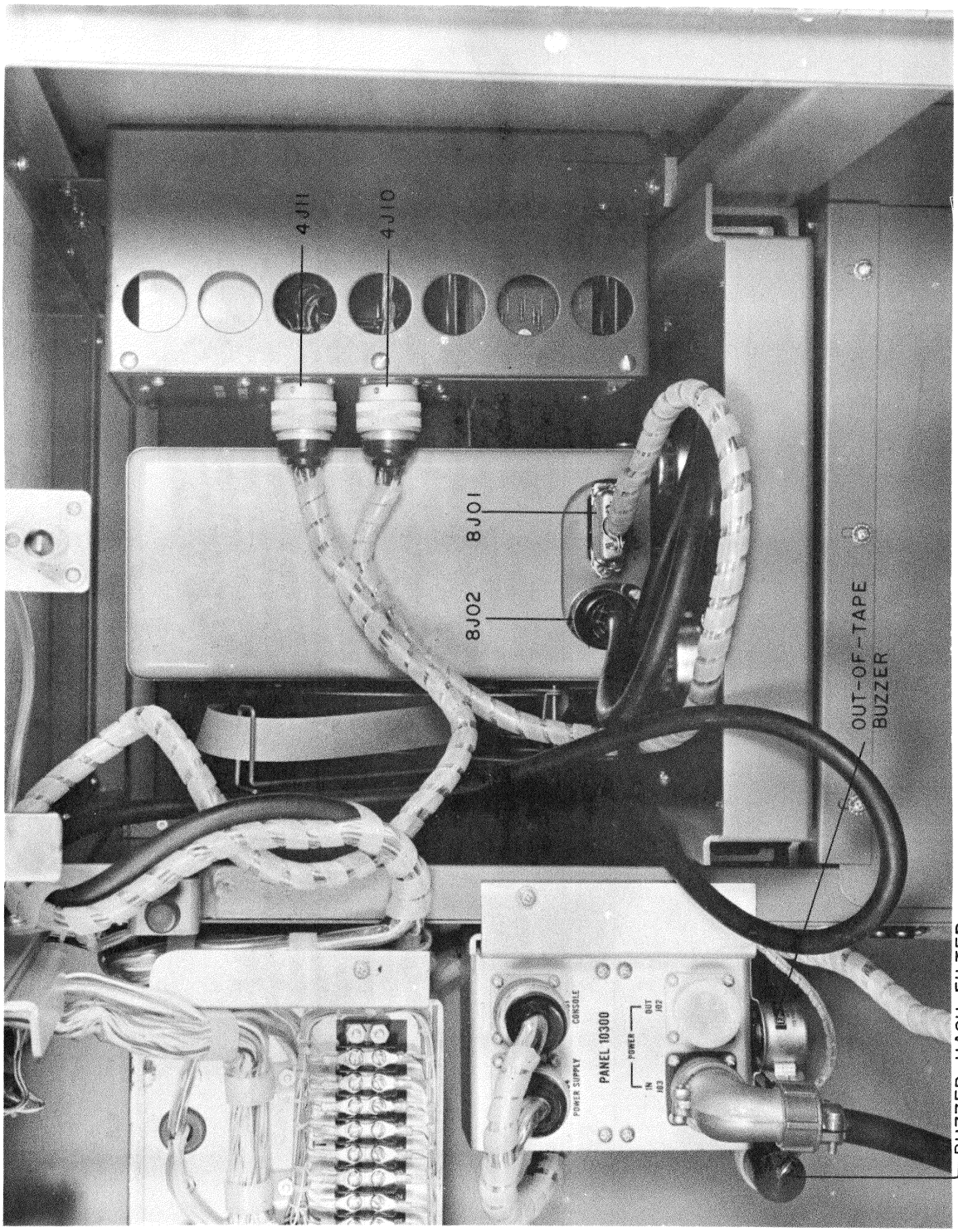


Figure 4-9. High-Speed Punch Connections

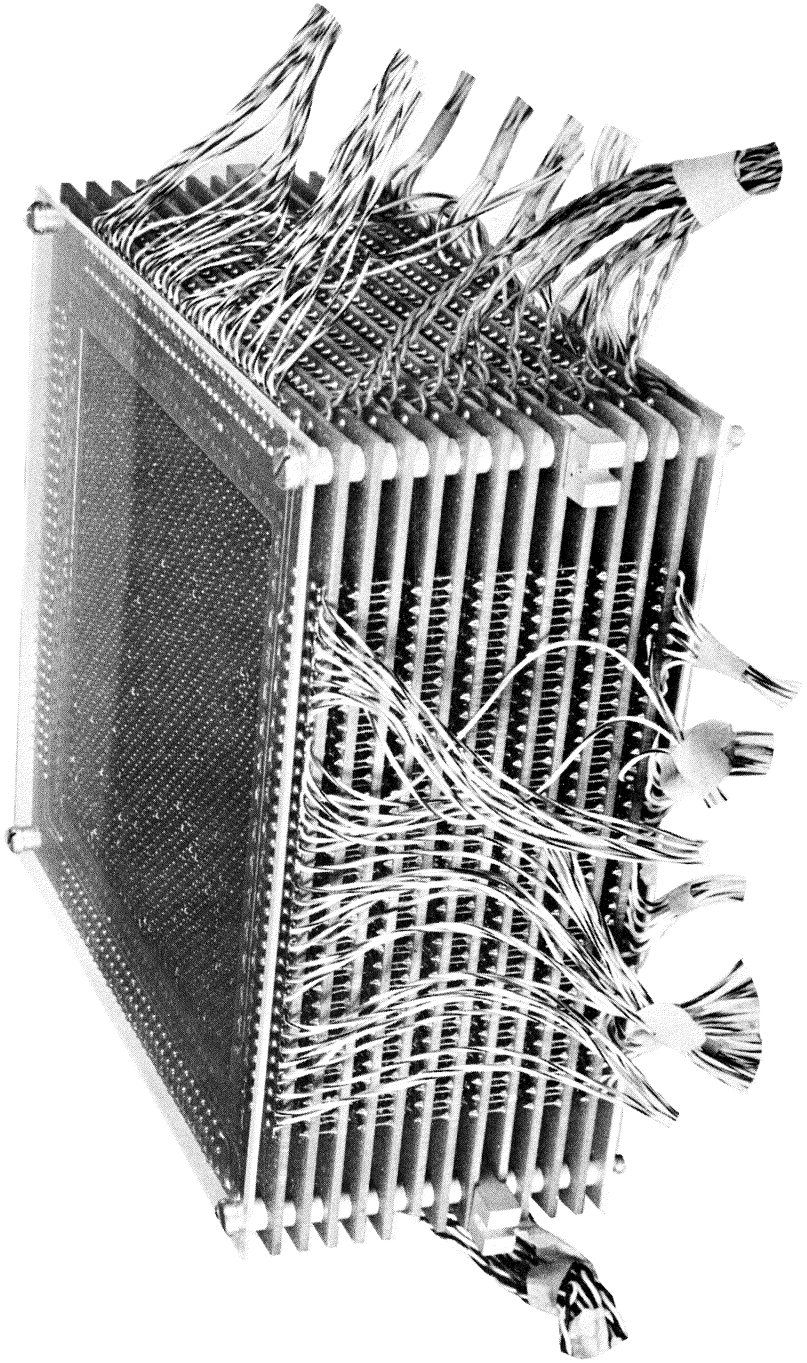
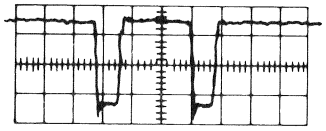
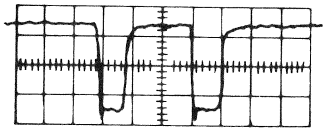


Figure 4-10. Memory Stack



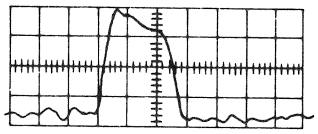
(a) Good inverter output (forced from "1" to "0" as a result of a 1 usec pulse recurring at 3.2 usec intervals.



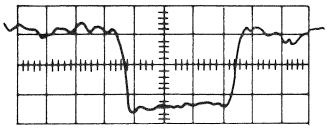
(b) Slow-fall inverter output (conditions as outlined above).

Vertical Sensitivity: 1 volt/cm
Sweep: 1 usec/cm

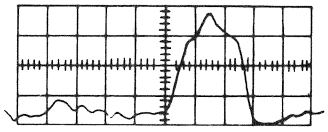
Figure 4-11. Standard Inverter Waveforms



(a) Clocked input to first inverter (H_1).



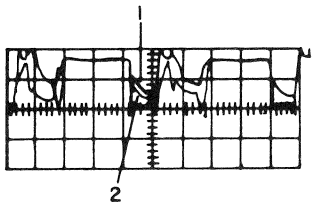
(b) Output from H_1 ("A" side of control delay card).



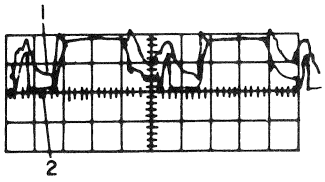
(c) Delayed output from V element.

Vertical Sensitivity: 1 volt/cm
Sweep: 0.1 usec/cm

Figure 4-12. Control Delay Waveforms



Read Side, Test Point A



Write Side, Test Point C

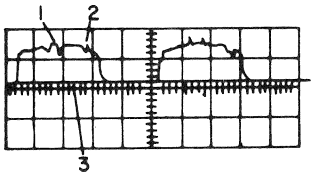
1) Rounded pulse is a reflected read pulse from another driver that is turned on when this one is off.

2) Squared off pulse shows when this driver is turned on.

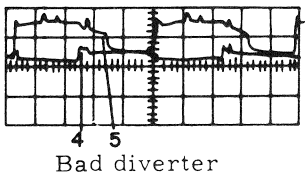
Vertical Sensitivity: 10 volts/cm

Sweep: 2 μsec/cm

Figure 4-13. R/W Driver, 51 Card



Good diverter



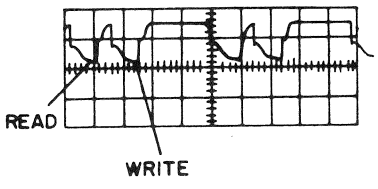
Bad diverter

1) End of read pulse
2) End of write pulse
3) Straight base line (a sign of a good diverter) shows time when diverter is on.
4) Step in base line indicates bad diverter due to faulty output transistor.
5) Slow drop off indicates marginal card.

Vertical Sensitivity: 5 volts/cm

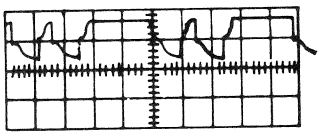
Sweep: 2 μsec/cm

Figure 4-14. Diverter, 52 Card



Vertical R/W source

Vertical and horizontal sources should be very similar

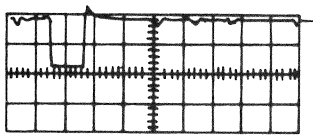


Horizontal R/W source

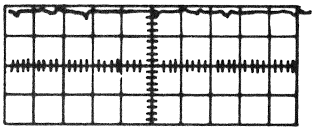
Vertical Sensitivity: 1 volt/cm

Sweep: 2 μsec/cm

Figure 4-15. Current Source, 54 Card



all "0's"

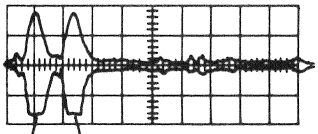


all "1's"

Vertical Sensitivity: 10 volts/cm

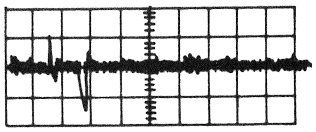
Sweep: 2 μsec/cm

Figure 4-16. Inhibit Generator, 58 Card

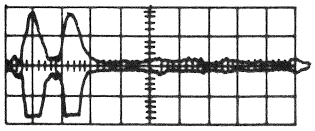


all "1's"

Test Point A



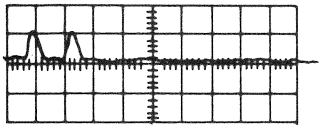
all "0's"



Test Point B

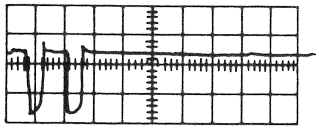
Test points A and B should yield essentially the same waveforms.

all "1's"



Test Point C

all "1's"



Test Point D

Vertical Sensitivity: 1 volt/cm

Sweep: 2 μsec/cm

all "1's"

Figure 4-17. Sense Amplifier, 57 Card

MAINTENANCE TESTS

Eight maintenance tests are provided in order to check all phases of the computer operations. These tests are listed below. Those preceded by an asterisk are considered of prime importance and every effort should be made to include them in the weekly preventive maintenance schedules. Explanatory notes for each of the tests are included herein. These notes are also presented, followed by a flow chart, if applicable, the test procedure, and then the routine itself, under separate cover.

COMPUTER CABINET

*Worst Pattern	(Storage)
Bit Picker	(Storage)
*Arithmetic	
*Command	(Pyramid)
Paper Tape	

TYPEWRITER CABINET

*Typewriter	Input (2 parts)
	Output (2 parts)

MAGNETIC TAPE SYSTEM

*Magnetic Tape Test

COMPUTER CABINET

WORST PATTERN TEST

A marginally operating core matrix memory will be most prone to err when the unique pattern of ones and zeros stored in a plane is such that the noise generated by the half-selected cores is maximum and of opposite polarity to the output current of the selected core. This worst pattern is generated by a test program which loads a word of all ones followed by a word of zeros successively from address 0000 through 0077, then all zeros followed by ones for the next 100 (octal) memory locations, etc. After loading the pattern, each memory location will be read and restored ten times. The program will then compare the memory contents with the original pattern. It will stop and display the address of any location which fails. The pattern will then be reversed and the test repeated. See the equipment diagrams in Volume 2 for detailed drawings of memory addressing and input wiring.

A Margin Switch is provided on the computer console. This switch enables the operator to run the test with normal, low or high bias on the sense amplifiers. The test will be run with the switch in each of the positions.

BIT PICKER

This program is designed to check the ability of the memory to hold a pattern of all zeros or all ones.

Load the program tape at location zero. Start at zero. If a bit changes from a zero to a one, or a one to a zero, the routine will stop at 26 with Z = 7701 and the word which failed displayed in A. On running again, the program will resume the testing.

The program lays a pattern of all zeros or all ones in all memory locations. It then scans memory eight times to see if there is any change. It then lays down the reverse pattern.

The test is run first with the Margin Switch in the HI position. This reduces the sensitivity of the sense amplifiers and tends to cause weak signals to be dropped. The test is run again with Margin in LO. This increases sensitivity and tends to cause spurious noise to be picked up.

ARITHMETIC TEST

This program checks the operation of each of the arithmetic and logical instructions of the computer using both positive and negative operations. Should a test failure be encountered the computer will stop and display the command or command group which failed. The test program will take known operands and combine them to produce a known result. If a comparison of the result and the preset result indicates a discrepancy, an error indication will be given.

Next, a series of variables known as A through G are set to zero. The operands are combined in a sequence twice and the result is checked to see if the two results are equal. Then the result is operated on in essentially a reverse order to reduce to the original operand. If both of these operations are successful, the operands A through G are incremented by different constants to obtain new random operands and the procedure is repeated again starting at block 4.

COMMAND TEST

This will indicate whether or not all internal transmission paths of the computer are functioning properly. First, a relative command from address 0000 will test the transmission of zeros from P to the pyramid. Then a relative command from address 7777 will test the same path's ability to transmit ones. Next all addressing modes will be tested and the end around borrow of the pyramid will be checked. Following this the shift replace commands will be tested. Should any failures be encountered, the computer will stop and indicate what failed.

The Command Test also checks the ability of the pyramid to combine all possible operands. The first part of the program tests each of the operations of add, subtract, load, and load complement with known operands. On passing this test, the routine takes two operands (A and B) and combines them in four different ways to check all types of inputs to the pyramid. Then A is increased by one until a cycle of 4095 values has been used. B is then increased by a fixed constant to create a new random value for B and the entire 4095 values of A are run again. This process is continued until B reaches the value zero.

PAPER TAPE TEST

This test is a proof of the paper tape punch and reader operation.

The reader will be tested for its ability to read information correctly from a tape loop. This loop will contain a series of frames of alternate octal 125 and 52 codes. The test program will accept inputs from the reader and compare each frame of the input data with a storage location containing the expected information codes. If an error is found the computer will stop and display the current input frame.

After completion of the above test, a second test will be run which will cause a repetitive pattern to be punched on tape by the high-speed punch. The free end of this tape will be looped around and inserted in the reader. A frame of information will be accepted by the computer from the reader. It will then be checked for parity with the information previously punched. If parity is found, the information will again be punched on the tape. Should a discrepancy be encountered the computer will stop and display the error.

TYPEWRITER CABINET

MONITORING TYPEWRITER

The typewriter may be tested either for the output function only or for the input and output function.

INPUT TEST

There are two input tests. In the first test, ten characters are typed manually, the carriage is returned and the same ten characters are repeated by the typewriter. A second input test is run with the disconnect switch in the Automatic mode. For this test, the operator types any number of characters followed by a carriage return. The typewriter then types out the same information. In both tests, accuracy is verified by visual inspection.

OUTPUT TESTS

Two tests are made of the output of the typewriter. One test consists of typing out a pattern of the alphabet in upper and lower case plus the numbers and various special functions. This pattern of typing is repeated by the typewriter and the results examined by visual inspection of the output printing. A second output test consists of transmitting a pattern of characters from binary zero to binary or octal 77. The resultant output can be checked by visual examination. This second test checks the ability of the typewriter to ignore illegal characters.

MAGNETIC TAPE SYSTEM

The magnetic tape test alternately writes and reads blocks of data while checking for parity errors. At the same time, the original word, as transmitted to the tape unit from computer storage, is compared with that word as recorded on the tape. The first test determines any errors in writing or reading within the tape system; the second checks for failures in the transmission path between computer and tape unit. The basic program is outlined below.

1) Clear program counters.
2) Write one block.
3) Check parity -- Error?
   - Yes: Backspace, add 1 to counter #1, repeat step 2.
   - No: Go to step 6.
4) Check parity -- Error?
   - Yes: Backspace, add 1 to counter #2, repeat step 2.

No: Go to step 6.

5) Check parity -- Error?

Yes: Type out parity error write and go to step 6.

No: Go to step 6.

6) Read block written in step 2.

7) Check parity -- Error?

Yes: Backspace, repeat step 6.

No: Go to step 10.

8) Same as 7.

9) Check parity -- Error?

Yes: Type out parity error read and go to step 10.

No: Go to step 10.

10) Backspace one block and compare -- Error?

Yes: Type out comp and go to step 2.

No: Go to step 2 for writing next block.

For satisfactory operation, parity counter #2 should equal zero at the end of the test. Under this condition, there will be no parity error type-outs. Parity counter #1 may have as many as 50 errors for 18,000 words without cause for alarm. A moderate count in parity counter #2 will be evidence of a worn tape, incorrect margin adjustment of the control unit, or a logic failure.

On an 18,000 word test, comp errors should be less than 7. More errors are evidence of a transmission difficulty.

POWER AND COOLING

POWER SUPPLY

The computer system operates from one basic power input (115 vac, 60 cps taken directly from the line) which operates such equipment as the convenience outlets, fan motors, punch motor, reader motor and the input to the power supply unit. The +20v and -20v supply is identical, only the -20v is described. Groups of circuit components are represented by blocks.

The power transistors in this supply unit operate in the (saturated) switched mode, for greater efficiency. The power transistors switch on and off approximately 1200 times per second. Automatic control of the duty cycle provides constant output voltage at any required level of load current within the rating or any variation of source voltage between the limits of 90 and 130v rms.

In the off position of the regulator (figure 4-18) Q1 is biased off by PS2 through R1 and R2; Q2 is biased off by PS4. The amount of bias on Q2 is limited to the forward drop across the silicon diode CR2. In the off condition power from PS1 is blocked by Q1 and a zero voltage drop appears across RL.

The magnetic amplifier (figure 4-19) is a pulse width modulator controlled by the value of E_c. Negative pulses from this amplifier are applied to the base of Q2. Resistor R4, being ten times the value of R5, causes the positive off bias voltage from PS4 to appear at Q2 only during the absence of pulses from the magnetic amplifier. Flow of excessive reset current from PS4 through the gate windings of the magnetic amplifier would reduce gain. CR2 prevents this.

Triggering the magnetic amplifier causes Q2 to turn on, releasing current from PS3 through R3 and turning on Q1. Current is released from PS1 into the filter circuit and RL. The end of the magnetic amplifier pulse removes the bias from Q1 and Q2 and stops the flow of current from PS1. Energy stored in L1 continues to flow into RL and the damping diode CR1 until the next pulse from the magnetic amplifier occurs.

A voltage detector and stabilization network (figure 4-20) completes the regulating loop. Adjusting the voltage detector by varying R9 provides a constant voltage of 20v across RL. Oscillation is prevented by the stabilizing network consisting of the secondary winding on L1 together with R6, R7 and C2. This circuit generates currents of the

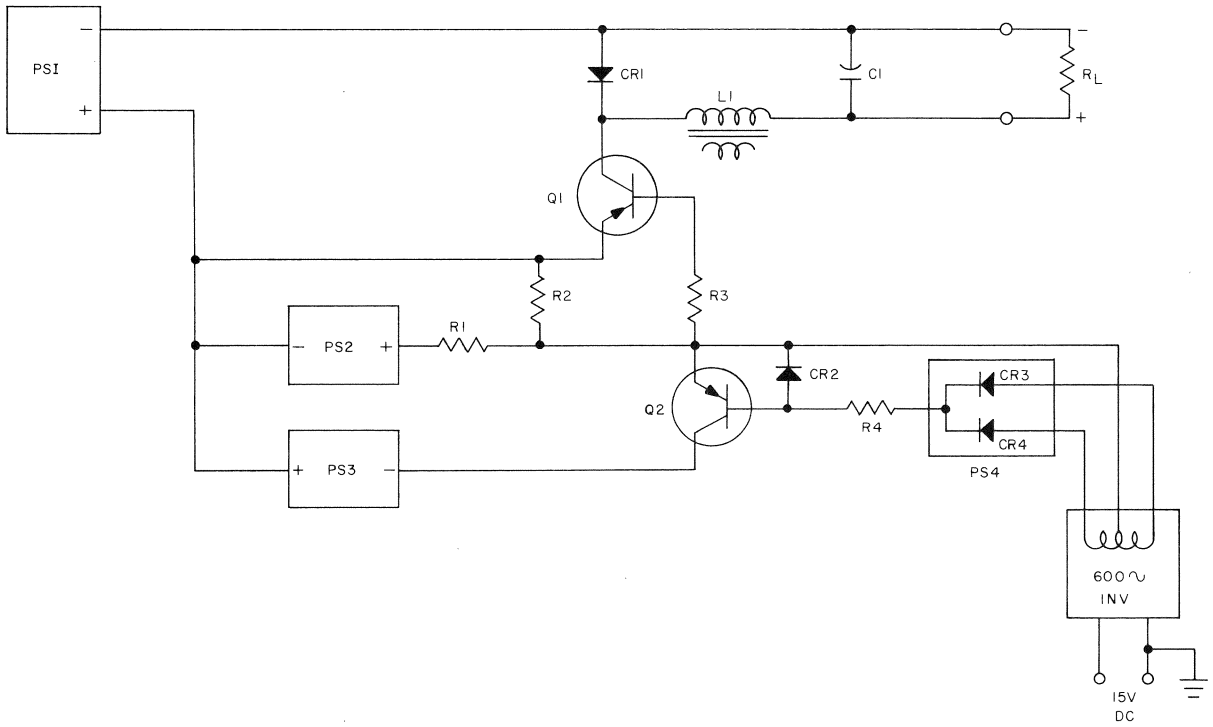


Figure 4-18. Steady-State OFF Condition

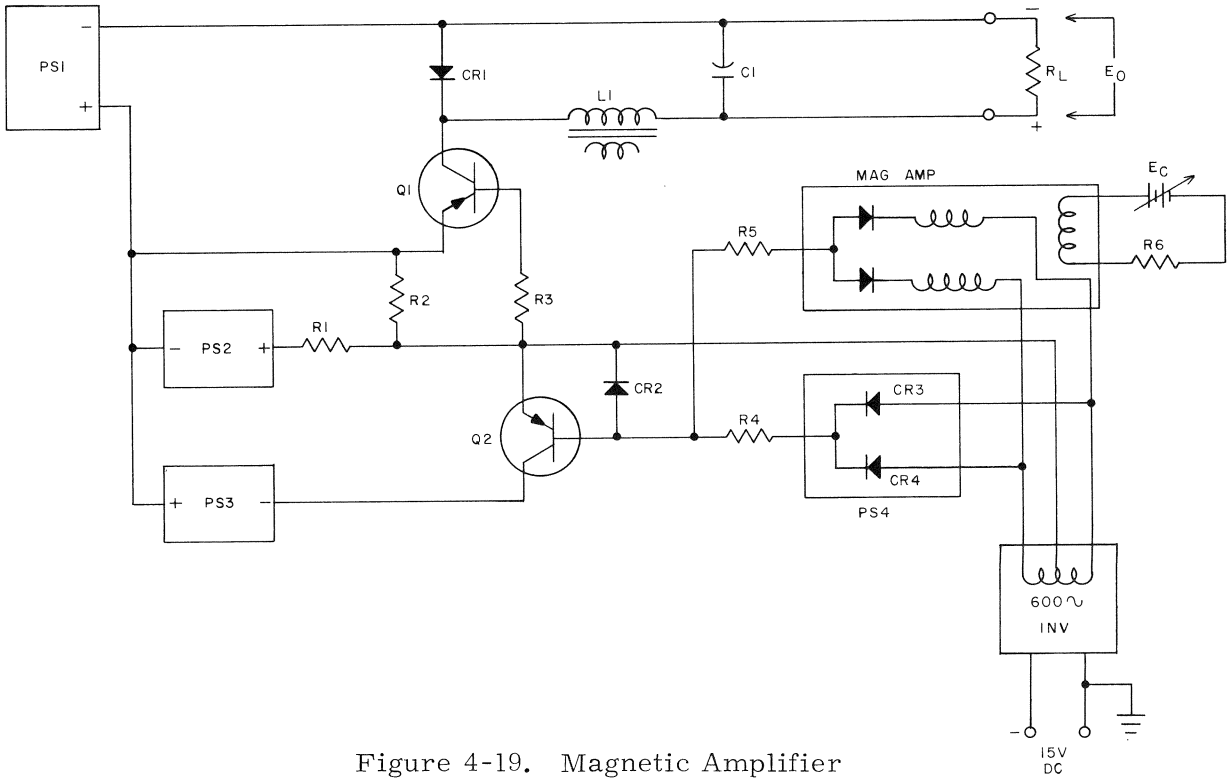


Figure 4-19. Magnetic Amplifier

correct amplitude and phase and applies them to the feedback winding on the magnetic amplifier. A filter (R6 and C2) removes 1200 cps noise from the feedback signal. The voltage detector operates only on the -20v section. A sense circuit, connected between -20v and +20v, provides an input to the -20v magnetic amplifier (T_4) in order to ensure that the magnitude of +20 output voltage follows that of the -20v section.

The overvoltage protection circuit, figure 4-21, prevents any prolonged overvoltage at the output terminals of the power supply unit in event of transistor failure. In most cases, a failure of this type will appear as a short between collector and emitters, resulting in a surge of approximately 25v above the normal 20v output. Relay RY1 energizes when the total output voltage rises to near 60 volts. Relay RY2 is energized by contact 1A and locked in by contact 2A which opens contact 2B, de-energizing the primary winding of the power transformer T1.

The overload protection circuit (figure 4-22) contains two saturable core reactor units threaded into the output leads; one for each supply. More than the maximum load causes the saturable reactor to trigger the silicon controlled rectifier SCR. When this occurs, power is immediately removed from the inverter and RY3 removes the primary voltage to T1. The speed of RY3 is not a controlling factor for this circuit because removal of the inverter voltage inactivates the magnetic amplifier and the output voltage of the power supply falls to zero even if RY3 is removed from the circuit. This circuit has response time that is approximately twice that of a high-speed fuse and it does not require the tremendous current overshoots necessary to blow a fuse rapidly. The power supply may be reset from the computer control console by pressing the OFF button and then the ON button.

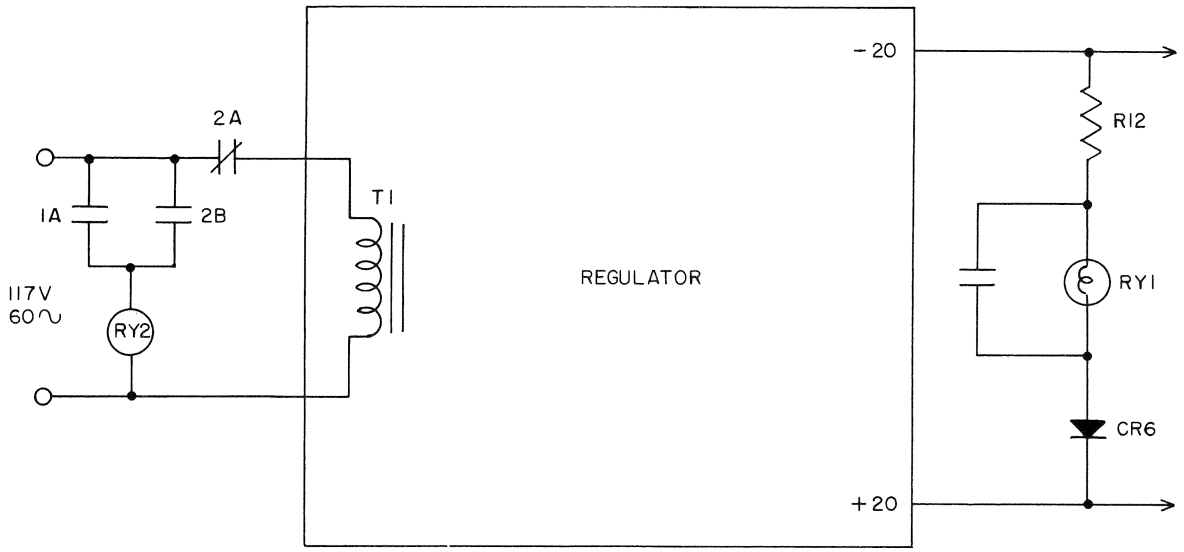


Figure 4-20. Voltage Detection and Stabilization Network

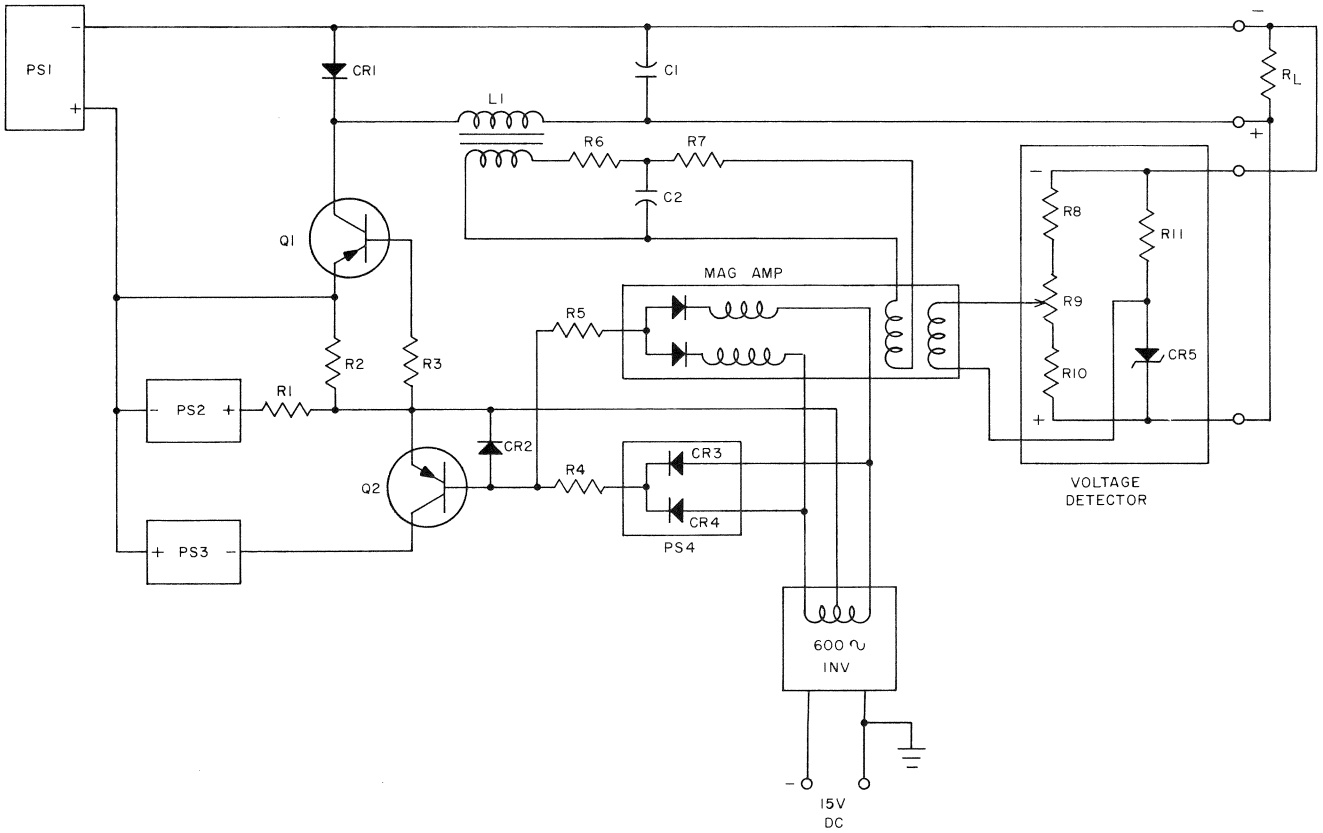


Figure 4-21. Over Voltage Protection Circuit

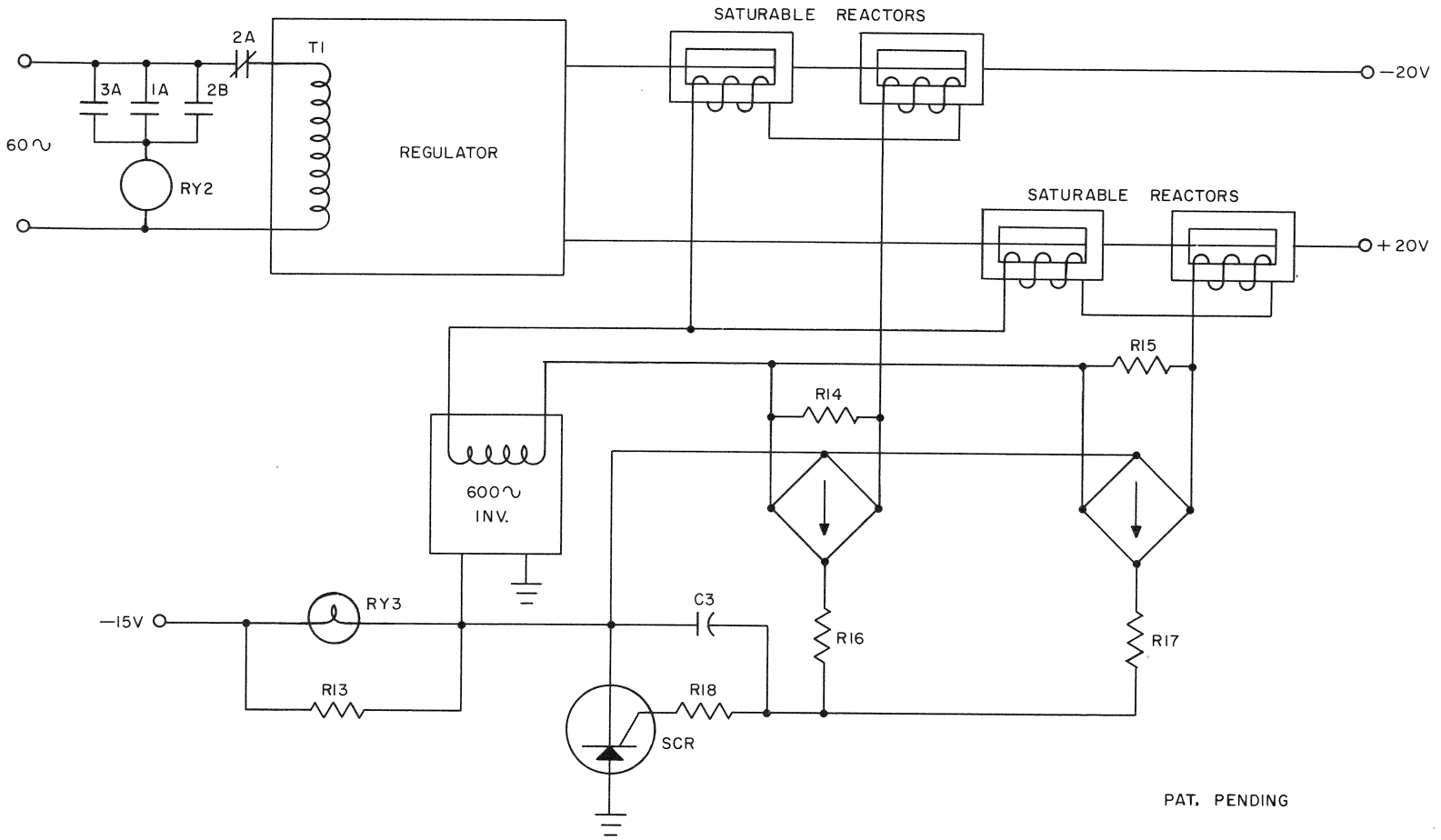


Figure 4-22. Overload Protection Circuit

POWER DISTRIBUTION

Power requirements for the computer are listed in Appendix F. Volume 3 shows the cabling requirements. Fuses to protect power wiring are listed below by chassis numbers.

	Fuse No.	Rating	Type	Protects
Computer Cabinet Console (chassis 10200)	F01	8A	ind.	Convenience Outlet
	F02	2A	ind.	B02
	F03	2A	ind.	B01
	F04	5A	ind.	Punch & Reader, 60 cps power
	F08	5A*	glass	-20 vdc
	F09	5A*	glass	-20 vdc
	F10	5A	glass	+20 vdc
	F11	5A	glass	-15 vdc
Photoelectric Reader (chassis 10700)	F01	2A	min. cart.	T01 - 115 vac
	F02	2A	min. cart.	Motor - 115 vac

COOLING

All blowers and fans use grease-sealed ball bearings and should require no maintenance for the life of the machine. Blower filters should be cleaned weekly. Total heat generated by the system cabinets is given in Appendix F, Installation.

* If one fuse blows, the other will blow through increased load.

MAINTENANCE SCHEDULES

Typewriter maintenance information is included here. Schedules for magnetic tape maintenance are in the Magnetic Tape System instruction books.

DAILY

Clean: 1) Computer room: desk top and floors, especially.
2) Photoelectric reader: remove tape setting clip to clean photocell block.

WEEKLY

Clean: 1) Air filters in all cabinets

Lubricate: 1) Punch: toggle arm shaft - saturate felt washers
punch bail shaft - saturate felt washers
tape reel bearings - grease
2) Typewriter: grease metal-on-metal friction points, oil springs, and pivot points

It is strongly recommended that the following tests be run weekly. They consume less than one-half hour and will aid greatly in preventive maintenance. (See Maintenance tests for the routines.)

Worst Pattern Test (Storage)	Typewriter Test
Command Test (Pyramid)	Paper Test
Arithmetic Test	

MONTHLY

Clean: 1) Typewriter: keys and platen
2) Punch: punch blocks, using solvent, chad drawer and paper lint on punch.

Lubricate: 1) Photoelectric reader: motor bearings
2) Punch: motor bearings and feed sprocket ratchet, tape reel bearings if needed (see Teletype manual, p.3-1),
toggle arm shaft - saturate felt washers,
punch bail shaft - saturate felt washers.

Inspect: 1) Typewriter: worn ribbon

SEMI ANNUALLY

Inspect: 1) Relay contacts - clean with 6/0 sandpaper
2) Exciter - Regulator tubes - use tube checker
3) Punch: punches for wearing
4) Reader: festoon lamp - change lamp

Clean and Lubricate: 1) Typewriter

APPENDIX C
INSTRUCTION TIMING CHARTS

The following pages present a time base analysis of instructions in the computer repertoire. Only those times wherein a command or enable occurs are shown. Also, common functions such as advancing the excursions counter (see figure 3-12 in Volume 1) are omitted.

As an aid to using the charts which follow, a verbal analysis of one of the more complex instructions, 72 INPUT, is included. Definite storage addresses have been assumed as well as the values assigned to their contents, in order to show more clearly the functions involved in each step.

The instructions appear in sequence, 01 through 76. No analysis of 00 or 77 is needed, since in these instructions the function translation effected during the third quarter of the Read Next Instruction (D) cycle stops the timing chain at the end of that cycle.

Table 1 lists each instruction in terms of storage reference cycles. Because in the majority of cases each initial D cycle is similar, it has not been repeated for each instruction. A sample D cycle is shown on page 11.

INPUT (72) INSTRUCTION

GENERAL

The 72 instruction allows the computer to input a predetermined number of 12-bit words and store them in a designated block of sequential storage addresses. The number of words stored is delineated by a starting address and a terminating address such that the first word is stored in the starting address and the last word is stored in the memory location just one position ahead of the terminating address. After each word has been stored, a comparison is made between the next available storage location and the terminating address. If the result of that comparison is not zero, the computer requests another input word. If the result is zero, indicating that all available locations in the designated block have been filled, the input operation is terminated and the computer proceeds to the next programmed instruction.

The storage reference sequence used for the input instruction is D B C D - CD - C D, etc.

The following analysis presents the important machine functions for each of the cycles in the basic storage reference sequence. It is assumed that the 75 (external function) instruction has already alerted the desired input device, and that 100 words are to be stored in the computer, beginning with address 2100, after which the program will be terminated by a Stop (77) instruction. The input instruction plus pertinent information must occupy three storage addresses. The fourth address (0002) contains the next instruction - in this case a Stop.

The 72 instruction uses the forward addressing scheme. This means that the six-bit quantity E is added to the contents of P in order to derive the storage location of the starting address. Thus, when 7203 is extracted from storage address 0000, the computer performs an input operation (72), beginning with the starting address stored E positions forward of the current instruction. In this manner, the contents of 0003 (2100) is determined as the starting address, and the first input word is stored at address 2100.

Storage address		
0 0 0 0	7203	(instruction)
0 0 0 1	2200	(terminating address)
0 0 0 2	7700	(next instruction - STOP)
0 0 0 3	2100	(starting address)

ANALYSIS OF INSTRUCTION

During the first quarter of the D cycle the P input to the pyramid (P→Q) is always enabled unless there is a jump instruction. In addition, the +1 input (+1→ R) is enabled except following a Clear P or a Master Clear. Since the first storage address in this example is 0000, it may be assumed that P previously was cleared, and that +1→ R is not extant. This is indicated on the D cycle chart by brackets around +1 →R. A capsule analysis follows, showing the D cycle by quarters.

1. P→ S (through pyramid and B)
2. S→P
   instruction (7203) to Z
3. Z→ F
4. Nothing

The box on the D cycle chart shows the contents of the registers at the end of the initial D cycle.

The B cycle starts by transferring Z1 (containing the location of the starting address) to S. During the second quarter the operand specified by the contents of S (2100, the starting address) is sent to Z. This address is transferred to A during the third quarter, at which time an Input Request signal is issued by the computer. At the end of the fourth quarter the advance to cycle C is made, whereupon the computer awaits an Input Ready signal from the external equipment.

1. Z1 → S
2. starting address → Z
3. Set Input Request FF; Z → A
4. Initiate input; advance to C and await Ready.

Again, the box on the cycle chart shows the register contents.

During the C cycle the incoming word is transferred to Z and subsequently deposited in the storage address specified by S. In addition, A is increased by 1. Since the Z register must be used to hold the incoming word, the contents of the storage address specified by S cannot be read into Z during the Read portion of the storage cycle. As a result, the address to which the first input word is to be sent is effectively cleared of its contents during the Write phase.

1. A → S
2. Clear input word storage address
3. Begin Write phase
4. Add 1 to A

The second D cycle adds 1 to P and transmits the terminating address to Z, whereupon it is subtracted from the content of A. If the resultant value (in A) is not zero, Z is added to A, thus restoring A to its previous value, and a return to cycle C is made, thus initiating another input. This input is repeated until A = 0; then the computer reads the next instruction - in this case a Stop 77.

Subsequent D cycles do not cause an advance in the value of P, since the first level control for +1→ R is inhibited.

1. P + 1→ S (first time only)
2. terminating address→ Z
3. A - Z

Sense A = 0

Yes	No
Clear I/O Sequence FF	Restore A by adding Z to A

4. Restore A by adding Z to A
   Advance to D and read next instruction

SPECIAL ADDRESSING MODES

On forward constant (fc) or indirect constant (ic) addressing modes (E=00 on f or i) a P+2 command is necessary to permit skipping the storage location of G when reading the next instruction. The special commands entailed for **fc** and **ic** addressing modes are outlined below.

fc		ic	
Cycle Time	Action	Cycle Time	Action
D 00	En P; n + 1		
D 05	B → S	D 00-37	Same as fc mode
D 12	S → P; Clr E=0 FF	A 00	En P; En + 1
D 17	Set E=0 FF	A 05	B → S (addr. of G in S reg.)
B 00	En P; En + 1		
B 05	B → S (addr. of G in S reg.)	B 00-37	normal read operand cycle
D 00	En P; En + 2		
D 05	B → S	D 00-37	same as fc mode
D 12	S → P (addr. of NI in P)		
D 12	Clr E=0 FF		

72 Instruction

Initial D Cycle

```
00      P→ Q; (+1→ R)
01
02
03
04
05      B→S (0000)
06      ~~B→ S  (0000)~~
07

10
11      Clr P
12      S→ P  (0000)
13
14
15      MCS→ I
16      Clr Z
17      I→Z  (7203)

20
21
22      Clr F
23      Z→ F (72)
24
25
26
27

30                                          F = 72
31                                          Z = 7203
32                                          S = 0000
33                                          A = XXXX
34                                          B = XXXX
35                                          P = 0000
36
37

0000    7203
0001    2200    Terminating Address
0002    7700    Stop Instruction
0003    2100    Starting Address
```

$^{72}_{B}$

00 Z1→ R
01
02
03
04
05 B→S(03)
06 ~~B→S (03)~~
07

10
11
12
13
14
15 MCS→I
16 Clr Z
17 I→ Z (contents of 03, or st. add. 2100)

20 Set Input Request FF; Z→R
21
22
23
24
25
26 B→A(2100)
27 ~~B→A (2100)~~

30
31 Set Wait Input; Issue Inp. Req.
32
33
34
35
36
37 Progress to C and await Input Ready
Set I/O Sequence Control FF

F = 72
Z = 2100
S = 03
A = 2100
P = 0000

^{72}C

00 A → Q
01
02
03
04
05 B → S (2100)
06 ~~B → S (2100)~~
07

10
11
12
13 Read out MCS
14 but do not use
15
16
17

20
21
22
23
24
25
26 +1 → R; A → Q; Set Write FF
27

30
31
32
33
34
35 Blk + 1 → R
36 B → A (2101)
37 ~~B → A (2101)~~

F = 72
Z = (2100) *
S = 2100
A = 2101
P = 0000

* The contents of 2100 will be the first word of input data.

00 +1 → R; P → Q
01
02
03
04
05 B → S (0001)
06 ~~B → S (0001)~~
07

10
11 Clr P
12 S → P (0001)
13
14
15 MCS → I
16 Clr Z A → Q; -Z → R, (initiate A - Z)
17 I → Z (2200)

F = 72
Z = 2200
S = 2101
A = 2101
P = 0001

20
21
22
23
24
25
26 A → Q; Z → R (initiate restore A)
~~27~~ 26 B → A (A hold A-Z, or 2101-2200)

30
31
32
33 Clear I/O Sequence FF if A = 0
34
35 Set Wait Input FF and issue Input Request if A ≠ 0
36
~~37~~ 36 B → A (A holds restored value, or 2101)
Advance to C and await Input Ready, then execute C and progress to D

TABLE 1. STEPS IN EXECUTING INSTRUCTIONS

Instructions	Phase	Z Register	A Register
00, 77	D	Instruction	NC ≡
01, 02, 03, 04, 05, 06, 07	D	Instruction	Result
10, 14, 20, 24, 30, 34			
12, 16, 22, 26, 32, 36	D	Instruction	NC
13, 17, 23, 27, 33, 37	B	Operand	Result
11, 15, 21, 25, 31, 35	D	Instruction	NC
	A	Address of Operand	NC
	B	Operand	Result
40, 42, 43	D	Instruction	NC
	B	Previous Content of Location	NC
	C	Result	NC
41	D	Instruction	NC
	A	Address of Operand	NC
	B	Previous Content of Location	NC
	C	Result	NC
44, 46, 47	D	Instruction	NC
50, 52, 53	B	Operand	Result
54, 56, 57	C	Result	Result
45, 51, 55	D	Instruction	NC
	A	Address of Operand	NC
	B	Operand	Result
	C	Result	Result

≡ NC indicates no register change

TABLE 1. (CONT'D)

Instruction	Phase	Z Register	A Register
60, 61, 62, 63 64, 65, 66, 67	D	Instruction	NC
70, 71	D	Instruction	NC
	B	Jump Address	NC
72	D	Instruction	NC
	B	Starting Address	Location of 1st input
	C	Input Character	Next input location
	D	Term. Address	NC
	C → D cycle continues until input location compares with final storage location		
73	D	Instruction	NC
	B	Starting Address	Location of Output
Repeated	C	Output Character	Location of Next Output
	D	Term. Address	NC
74	D	Instruction	NC
75	D	Instruction	NC
	B	Function Code	NC
76	D	Instruction (Green Background	NC
	C	Input Character (No Green Background)	Input Character

CODE		Sample D Cycle
	TIME	COMMAND	REMARKS
	00	P→Q, + 1 → R U	ZL → R
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B → S	
	10	MCS → I	
	11	Clear P	
	12	S → P	
	16	Clear Z	
	17	I → Z	
	22	Clear F	
	23	Zu → F	
	25	Init. Zl → Q	
	25	Clear Au, Al → Q	
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	36	B → A	

CODE SHA 01	Shift A	Left shift contents of A; D sequence 6.4μs.

D Cycle	TIME	COMMAND	REMARKS
	00	P→Q, + 1→R	
	01	Clear B	Formation of address
	03	Toggle B	
	04	Probe B	
	06	B→S	
	10	MCS→I	Read Instruction
	11	Clear P	
	12	S→P	Display Address
	16	Clear Z	
	17	I→Z	Z Holds Instruction Word
	22	Clear F	
	23	Z_u → F	
	25	A →R and/or Q	For Left Shift (See Table below)
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	36	B→A	Execution of Instruction
	37	Reset D Cycle FF	

Pyramid inputs for indicated shift
(at time 25)

1 place: A→R
3 places: A→Q
dec. 10 mult.: A→R; A→Q

Magnitude of shift is determined by value of E, as shown:

02 = left 1 place
10 = left 3 places
12 = decimal 10 multiply

CODE LPN 02	Logical Product	Form in A the logical product of original contents of A and Operand; D Cycle, 6.4μs.
D Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	P→Q, + 1→R	
	01	Clear B	
	03	Toggle B	Form Address
	04	Probe B	
	05	B→S	Location of instruction
	10	MCS→I	Read instruction
	11	Clear P	Prepare for address
	12	S→P	
	16	Clear Z	Prepare for instruction
	17	I→Z	
	22	Clear F	
	23	Zu→F	
	25	Init. Zl→Q	Zl=1st operand
	25	Clear Au, Al→Q	Al=2nd operand
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	36	B→A	Result

CODE LSN 03	Logical Sum	Form in A the logical sum of original contents of A and lower 6 bits of instruction; D cycle, 6.4μs.

D Cycle	TIME	COMMAND	REMARKS
	00	P→Q, +1→R	
	01	Clear B	
	03	Toggle B	Form Address
	04	Probe B	
	05	B→S	Location of instruction
	10	MCS→I	Read instruction
	11	Clear P	Prepare for new address
	12	S→P	Display address
	16	Clear Z	Prepare for instruction
	17	I→Z	
	22	Clear F	
	23	Zu→F	
	25	Zl→R, A→Q	Zl = Operand Zu=0 in pyramid (+1→Ru)
	31	Clear B	
	33	Toggle B	
	34	Block Probe B	For add-no carry
	36	B→A	

CODE		
LDN 04	LOAD	Replace contents of A with operand. D Cycle, 6.4μs.

D Cycle	TIME	COMMAND	REMARKS
	00	P→Q, + 1→R	
	01	Clear B	
	03	Toggle B	Form Address
	04	Probe B	
	~~06~~ 05	B→S	Location of instruction
	10	MCS→I	Read instruction
	11	Clear P	Prepare for address
	12	S→P	Display address
	16	Clear Z	Prepare for instruction
	17	I→Z	
	22	Clear F	
	23	Zu→F	
	25	Zl→R	(+1→Ru)
	25	Block A→Q	(No arithmetic operation)
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	~~37~~ 36	B→A	Result

CODE		
LCN 05	Load Complement	Replace contents of A with one's complement of lower 6 bits of instruction; D Cycle, 6.4μs.

D Cycle	TIME	COMMAND	REMARKS
	00	P→Q, +1→R	
	01	Clear B	
	03	Toggle B	Form Address
	04	Probe B	
	05	B→S	Location of instruction
	10	MCS→I	Read instruction
	11	Clear P	
	12	S→P	Display address
	16	Clear Z	Prepare for instruction
	17	I→Z	
	22	Clear F	
	23	Zu→ F	
	25	-Zl→R	
	25	Block A→Q	No arithmetic operation
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	36	B→A	Result

CODE ADN 06	Add	Form in A the sum of original contents of A and operand. D Cycle, 6.4μs.
D Cycle	TIME	COMMAND	REMARKS
	00	P→Q, + 1 →R	
	01	Clear B	
	03	Toggle B	Form Address
	04	Probe B	
	05	B→S	Location of instruction
	10	MCS→I	Read Instruction
	11	Clear P	
	12	S→P	Display address
	16	Clear Z	
	17	I→Z	Instruction word
	22	Clear F	
	23	Zu→F	
	25	Zl→R	(+1→Ru)
	25	A→Q	
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	36	B→A	Result

CODE SBN 07	Subtract	Form in A the difference of original contents of A and operand, D Cycle, 6.4μs.
D Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	P→Q, + 1→R	
	01	Clear B	
	03	Toggle B	Form Address
	04	Probe B	
	~~06~~ 05	B→S	Location of instruction
	10	MCS→I	Read instruction
	11	Clear P	
	12	S→P	Display address
	16	Clear Z	
	17	I→Z	Instruction word
	22	Clear F	
	23	Zu→F	
	25	-Z1→R	
	25	A→Q	
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	~~37~~ 36	B→A	Result

CODE		
LPD 10	Logical Product	Form in A the logical product of original contents of A and operand. D-B sequence, 12.8μs.

B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+1→Ru)
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	~~06~~ 05	B→S	
	10	MCS→I	Read contents of one of 1st 64 locations.
	16	Clear Z	
	17	I→Z	
	20	Z→Q, A→Q	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	~~27~~ 26	B→A	Result
	37	Set D cycle FF	

CODE		Form in A the logical product of original contents of
LPI 11	Logical Product	of A and operand. DAB sequences, 19. 2μs.

	TIME	COMMAND	REMARKS
A Cycle	00	Zl→R	(+ 1 → Ru)
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	~~06~~ 05	B→S	
	10	MCS→I	Read address of operand
	16	Clear Z	
	17	I→Z	
	37	Set B cycle FF	
B Cycle			
	00	Z→R	
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	~~06~~ 05	B→S	
	10	MCS→I	Read Operand
	15	A→Q, Z→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	~~27~~ 26	B→A	Result
	37	Set D Cycle FF	

CODE		Form in A the logical product of original contents of A and operand. D-B
LPF 12	Logical Product	

B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R, P→Q	(+1→Ru)
	01	Clear B	Form address forward
	03	Toggle B	
	04	Probe B	
	~~05~~ 05	B→S	
	10	MCS→I	Read operand
	15	A→Q, Z→Q	
	16	Clear Z	
	17	I→ Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	~~27~~ 26	B→A	Result
	37	See D cycle FF	

CODE		Form in A the logical product of original contents of A and operand. D-B sequence 6.4μs.
LPB 13	Logical Product	

B Cycle	TIME	COMMAND	REMARKS
	00	-Z1→R, P→Q	
	01	Clear B	
	03	Toggle B	Form address backward
	04	Probe B	
	05	B→S	
	10	MCS→I	Read Operand
	15	A→Q, Z→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	Form Product
	24	Probe B	
	26	B→A	Result
	37	Set D Cycle FF	

CODE LSD 14	Logical Sum	Form in A the logical sum of original contents of A and operand. D - B sequence, 12. 8μs.
B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+1→Ru)
	01	Clear B	
	03	Toggle B	Form Operand Address
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	Z→R, A→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Block Probe B	For logical sum only
	27	B→A	Result

CODE LSI 15	Logical Sum	Form in A the logical sum of original contents of A and operand. D. A. B sequence, 19. 2μs.

A Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+1→Ru)
	01	Clear B	
	03	Toggle B	Form indirect address
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read address of operand
	16	Clear Z	
	17	I→Z	
	37	Set B cycle FF	
B Cycle			
	00	Z→R	
	01	Clear B	
	03	Toggle B	Form Operand Address
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read Operand
	15	A→Q, Z→R	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Block Probe B	Logical sum only
	2726	B→A	Result
	37	Set D cycle FF	

CODE		Form in A the logical sum of original contents of A and operand. D-B sequence, 6.4μs.
LSF 16	Logical Sum	

B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R, P→Q	(+1→Ru)
	01	Clear B	Form address forward
	03	Toggle B	
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read operand
	15	A→Q, Z→R	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Block Probe B	
	2726	B→A	Result
	37	Set D cycle FF	

CODE LSB 17	Logical Sum	Form in A the logical sum of original contents of A and operand. D-B sequence, 12.8μs.

B Cycle	TIME	COMMAND	REMARKS
	00	-Z1→R, P→Q	
	01	Clear B	Form address backward
	03	Toggle B	
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	A→Q, Z→R	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Block Probe B	Logical sum only
	26	B→A	Result
	37	Set D cycle FF	

CODE LDD 20	Load	Replace contents of A with operand; D-B sequence, 12.8μs.

B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+1→Ru)
	01	Clear B	
	03	Toggle B	Form Operand Address
	04	Probe B	
	05	B→S	
	10	MCS→I	Read Operand
	15	En Z→R	
	15	Block A→Q	No arithmetic operation
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	Result
	37	Set D cycle FF	

CODE LDI 21	Load	Replace contents of A with operand D-A-B sequence, 19.2 us.
A Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	Z1→ R	(+1 → Ru)
	01	Clear B	Form indirect address
	03	Toggle B	
	04	Probe B	
	~~05~~ 05	B→ S	
	10	MCS →I	Read address of instruction
	16	Clear Z	
	17	I→Z	
	37	Set B cycle FF	
B Cycle	00	Z→ R	
	01	Clear B	Form operand address
	03	Toggle B	
	04	Probe B	
	~~05~~ 05	B→ S	
	10	MCS →I	Read operand
	15	Z →R	
	16	Clear Z	
	17	I→ Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	~~27~~ 26	B→ A	Result
	37	Set D cycle FF	

CODE LDF 22	Load	Replace Contents of A with operand D-B sequence, 12.8 us.
B Cycle	TIME	COMMAND	REMARKS
	00	Z1→ R, P→ Q	(+ 1→ Ru)
	01	Clear B	
	03	Toggle B	Form address forward
	04	Probe B	
	05	B→ S	
	10	MCS→ I	Read operand
	15	En Z→ R	
	16	Clear Z	
	17	I→ Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→ A	Result
	37	Set D cycle FF	

CODE LDB 23	Load	Replace contents of A with operand D-B sequence, 12.8 us.
B Cycle	TIME	COMMAND	REMARKS
	00	-Z1 → R, P → Q	Form address backward
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B → S	
	10	MCS → I	Read operand
	15	Z → R	
	16	Clear Z	
	17	I → Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B → A	Result
	37	Set P cycle FF	

CODE LCD 24	Load Complement	Replace contents of A with complement of operand. D-B sequence 12.8 us.
B Cycle	TIME	COMMAND	REMARKS
	00	Z1 → R	(+1 → Ru)
	01	Clear B	
	03	Toggle B	Form Operand address
	04	Probe B	
	05	B → S	
	10	MCS → I	Read operand
	15	-Z → R	
	16	Clear Z	
	17	I → Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B → A	Result
	37	Set D cycle FF	

CODE LCI 25	Load Complement	Replace contents of A with complement of operand. D-A-B sequence, 19.2μs.
A Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	Zl→R	(+1→Ru)
	01	Clear B	Form indirect address
	03	Toggle B	
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read indirect address
	16	Clear Z	
	17	I→Z	
	37	Set B cycle FF	
B Cycle			
	00	Z→R	
	01	Clear B	
	03	Toggle B	Form Operand Address
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read operand
	15	-Z→R	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	2726	B→A	Result
	37	Set D cycle FF	

CODE		Replace contents of A with complement of operand. D-B sequence, 12.8μs.
LCF 26	Load Complement	
B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R, P→Q	(+1→Ru)
	01	Clear B	
	03	Toggle B	Form address forward
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	-Z→R	
	16	Clear Z	
	17	I→Z	
	21	Clear Z	
	23	Toggle Z	
	24	Probe Z	
	26	B→A	Result
	37	Set D cycle FF	

CODE LCB 27	Load Complement	Replace contents of A with complement of operand D-B sequence, 12.8μs.
B Cycle	TIME	COMMAND	REMARKS
	00	-Z1→R, P→Q	
	01	Clear B	
	03	Toggle B	Form address backward
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read operand
	15	-Z→R	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	2726	B→A	Result
	37	Set D cycle FF	

CODE ADD 30	Add	Add contents of A to operand. D-B sequence, 12.8μs.
B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+1→Ru)
	01	Clear B	Form Operand Address
	03	Toggle B	
	04	Probe B	
	05	B→S	
	10	MCS→I	Read Operand
	15	A→Q, Z→R	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	Result
	37	Set D cycle FF	

CODE ADI 31	Add	Form in A the sum of original contents of A and operand. D-A-B sequence, 19.2μs.
A Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	Zl→R	(+1→Ru)
	01	Clear B	Form indirect address
	03	Toggle B	
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read indirect address
	16	Clear Z	
	17	I→Z	
	37	Set B cycle FF	
B Cycle			
	00	Z→R	
	01	Clear B	
	03	Toggle B	Form operand address
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read operand
	15	Z→R, A→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	2726	B→A	Result
	37	Set D cycle FF	

CODE		
ADF 32	Add	Form in A the sum of original contents of A and operand. D-B sequence, 12. μs.

B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R, P→Q	(+1→Ru)
	01	Clear B	Form forward address
	03	Toggle B	
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	Z→R, A→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	Result
	37	Set D cycle FF	

CODE		Form in A the sum of original contents of A and operand. D-B sequence, 12.8μs.
ADB 33	Add	

B Cycle	TIME	COMMAND	REMARKS
	00	-Z1→R, P→Q	
	01	Clear B	Form backward address
	03	Toggle B	
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	Z→R, A→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	Result
	37	Set D cycle FF	

CODE		
SBD 34	Subtract	Form in A the difference of original contents of A and operand. D-B sequence, 12.8μs.

B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+1→Ru)
	01	Clear B	
	03	Toggle B	Form operand address
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	-Z→R, A→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	Result
	37	Set D cycle FF	

CODE SBI 35	Subtract	Form in A the difference of original contents of A and operand. D-A-B sequence, 19.2μs.

A Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+1→Ru)
	01	Clear B	
	03	Toggle B	Form indirect address
	04	Probe B	
	05	B→S	
	10	MCS→I	Read indirect address
	16	Clear Z	
	17	I→Z	
	37	Set B cycle FF	
B Cycle			
	00	Z→R	
	01	Clear B	
	03	Toggle B	Form operand address
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	-Z→R, A→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	Result
	37	Set D cycle FF	

CODE		Form in A the difference of original content of A and operand. P-B sequence, 12.8μs.
SBF 36	Subtract	
B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R, P→Q	(+1→Ru)
	01	Clear B	
	03	Toggle B	Form address forward
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	-Z→R, A→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	Result
	37	Set D cycle FF	

CODE		Form in A the difference of original contents of A and operand. D-B sequence. 12.8 μs.
SBB 37	Subtract	

B Cycle	TIME	COMMAND	REMARKS
	00	-Z1→r, P→Q	
	01	Clear B	
	03	Toggle B	Form address backward
	04	Probe B	
	0605	B→S	
	10	MCS→I	Read operand
	15	-Z→R, A→Q	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	2726	B→A	Result
	37	Set D Cycle FF	

CODE STD 40	Store	Replace operand with contents of A, which remains unchanged. D-B-C sequence, 19.2μs.
B Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+l→Ru)
	01	Clear B	
	03	Toggle B	Form operand address
	04	Probe B	
	05	B→S	
	10	MCS→I	Read previous content of location
	16	Clear Z	
	17	I→Z	
	25	A→Q	
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	37	Set C cycle FF	
C Cycle			
	04	A→Q	
	10	B→I	
	11	Clear B	
	13	Toggle B	
	14	Probe B	B→I effected
	16	Clear Z	Clear original content of location
	17	I→Z	
	26	Set write FF	Store Z
	37	Set D cycle FF	

CODE		Replace operand with original content of A. D-A-B-C sequence, 25.6μs.
STI 41	Store	

A Cycle	TIME	COMMAND	REMARKS
	00	Zl→R	(+1→Ru)
	01	Clear B	
	03	Toggle B	Form indirect address
	04	Probe B	
	05	B→S	
	10	MCS→I	Read indirect address
	16	Clear Z	
	17	I→Z	
	37	Set B cycle FF	

B Cycle			
	00	Z→R	
	01	Clear B	Form operand address
	03	Toggle B	
	04	Probe B	
	05	B→S	
	10	MCS→I	Read previous content of location
	16	Clear Z	
	17	I→Z	
	37	Set C cycle FF	

CODE 41 Cont'c			
C Cycle	TIME	COMMAND	REMARKS
	05	A→Q	
	10	B→I	
	11	Clear B	
	13	Toggle B	
	14	Probe B	B→I effected
	16	Clear Z	Clear original content of location
	17	I→Z	
	26	Set WRITE FF	Store A
	37	Set D cycle FF	

CODE STF 42	Store	Replace operand with original content of A. D-B-C sequence, 19.2 us.
B Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	Z1 → R, P → Q	(+ 1 → Ru)
	01	Clear B	
	03	Toggle B	Form forward address
	04	Probe B	
	05	B → S	
	10	MCS → I	Read previous content of location
	16	Clear Z	
	17	I → Z	
	25	A → Q	
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	37	Set C cycle FF	
C Cycle			
	05	A → Q	
	10	B → I	
	11	Clear B	
	13	Toggle B	
	14	Probe B	B → I effected
	16	Clear Z	Clear original content of location
	17	I → Z	
	26	Set WRITE FF	Store A
	37	Set D cycle FF	

CODE STB 43	Store	Replace operand with original content at A-D-B-C sequence, 19.2 us.
B Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	-Z1 → R, P → Q	Form backward address
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	0605	B → S	
	10	MCS → I	Read previous content of location
	16	Clear Z	
	17	I → Z	
	25	A → Q	
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	37	Set C cycle FF	
C Cycle			
	05	A → Q	
	10	B → I	
	11	Clear B	
	13	Toggle B	
	14	Probe B	B → I effected
	16	Clear Z	Clear original content of location
	17	I → Z	
	26	Set WRITE FF	Store A
	37	Set D cycle FF	

CODE		Form in A the value of operand shifted left end around one bit position. Replace operand with result. D-B-C sequence, 19.2 us.
SRD 44	Shift Replace	

B Cycle	TIME	COMMAND	REMARKS
	00	Z1→ R	(+ 1 →Ru)
	01	Clear B	
	03	Toggle B	Form operand address
	04	Probe B	
	05	B →S	
	10	MCS →I	Read operand
	15	Z→ R, Z→ Q	Initiate left shift of operand
	16	Clear Z	
	17	I→ Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B, En A→ Q	
	26	B→ A	A →Q effected
	31	Clear B	Re-establish modified
	33	Toggle B	operand in B-register
	34	Probe B	
	37	Set C cycle FF	
C Cycle			
	05	A→ Q	Re-establish modified operand in B
	10	B→ I	
	11	Clear B	
	13	Toggle B	Establish modified
	14	Probe B	operand in Z-register
	16	Clear Z	
	17	I→ Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE		Form in A the value of the operand shifted left end around one bit position. Replace operand with result, D-A-B-C sequence, 25.6 us.
SRI 45	Shift Replace	

A Cycle	TIME	COMMAND	REMARKS
	00	Z → R	(+1 → Ru)
	01	Clear B	Form indirect address
	03	Toggle B	
	04	Probe B	
	05	B → S	
	10	MCS → I	Read indirect address
	16	Clear Z	
	17	I → Z	
	37	Set B cycle FF	
B Cycle	00	Z → R	Form Operand address
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B → S	
	10	MCS → I	Read operand
	15	Z → R, Z → Q	Initiate left shift of operand
	16	Clear Z	
	17	I → Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B, En A → Q	
	26	B → A	A → Q effected
	31	Clear B	Re-establish modified operand in B register
	33	Toggle B	
	34	Probe B	
	37	Set C cycle FF	

CODE 45	Continued		
C Cycle	TIME	COMMAND	REMARKS
	05	A → Q	
	10	B → I	Establish modified operand in Z-register
	11	Clear B	
	13	Toggle B	
	14	Probe B	
	16	Clear Z	
	17	I → Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE SRF 46	Shift replace	Form in A the value of the operand shifted left end around one bit position. Replace operand with result. D-B-C sequence, 19.2 us.
B Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	Zl→ R, P→ Q	(+ 1 →Ru)
	01	Clear B	Form forward address
	03	Toggle B	
	04	Probe B	
	05	B→ S	
	10	MCS→I	Read Operand
	15	Z→R, Z→Q	Initiate left shift of operand
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B, En A→Q	
	26	B→A	Z + Z Result in A
	37	Set C cycle FF	
C Cycle			
	05	A→ Q	
	10	B→I	Establish modified operand in Z-register
	11	Clear B	
	13	Toggle B	
	14	Probe B	
	16	Clear Z	
	17	I→ Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE SRB 47	Shift Replace	Form in A the value of the operand shifted left end around one bit position. Replace operand with result. D-B-C sequence. 19.2 us.

B Cycle	TIME	COMMAND	REMARKS
	00	-Z1 → R, P → Q	Form backward address
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B → S	
	10	MCS → I	Read operand
	15	Z → R, Z → Q	Initiate left shift of operand
	16	Clear Z	
	17	I → Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B, En A → Q	
	26	B → A	Z + Z, Result in A
	37	Set C cycle FF	
C Cycle	05	A → Q	
	10	B → I	Establish modified operand in Z-register
	11	Clear B	
	13	Toggle B	
	14	Probe B	
	16	Clear Z	
	17	I → Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE RAD 50	Replace ADD	Form in A the sum of original contents of A and operand. Replace operand. Replace operand with result. D-B-C sequence, 19.2 us.

B Cycle	TIME	COMMAND	REMARKS
	00	Z1→ R	(+ 1→ Ru)
	01	Clear B	
	03	Toggle B	Form operand address
	04	Probe B	
	0605	B→ S	
	10	MCS→I	Read operand
	15	A→ Q, Z→ R	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	2726	B→ A	Z + A in A
	37	Set C cycle FF	
C Cycle	05	A→ Q	
	10	B→ I	
	11	Clear B	
	13	Toggle B	Establish result in Z-register
	14	Probe B	
	16	Clear Z	
	17	I→ Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE RAI 51	Replace Add	Form in A the sum of original contents of A and operand. Replace operand with result. D-A-B-C sequence. 25.6 us.

A Cycle	TIME	COMMAND	REMARKS
	00	Z1→ R	(+ 1 →Ru)
	01	Clear B	
	03	Toggle B	Form indirect address
	04	Probe B	
	06 05	B→ S	
	10	MCS→ I	Read Indirect address
	16	Clear Z	
	17	I→ Z	
	37	Set B cycle FF	

B Cycle			
	00	Z→R	
	01	Clear B	
	03	Toggle B	Form Operand address
	04	Probe B	
	06 05	B→ S	
	10	MCS→I	Read operand
	15	A→ Q, Z→R	
	16	Clear Z	
	17	I →Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	27 26	B→ A	Z + A in A
	37	Set C cycle FF	

CODE 51	Continued	
C Cycle	TIME	COMMAND	REMARKS
	05	A→ Q	
	10	B→ I	Establish result in Z-register
	11	Clear B	
	13	Toggle B	
	14	Probe B	
	16	Clear Z	
	17	I→ Z	
	26	Set WRITE FF	
	37	Set D cycle FF	

CODE RAF 52	Replace Add	Form in A the sum of original contents of A and operand. Replace operand with result. D-B-C sequence, 19.2 us.

	TIME	COMMAND	REMARKS
B Cycle	00	Z1 → R, P → Q	(+ 1 → Ru)
	01	Clear B	
	03	Toggle B	Form forward address
	04	Probe B	
	05	B → S	
	10	MCS → I	Read operand
	15	A → Q, Z → R	
	16	Clear Z	
	17	I → Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B → A	Z + A in A
	37	Set C cycle FF	
C Cycle	05	A → Q	
	10	B → I	
	11	Clear B	Establish result
	13	Toggle B	in Z-register
	14	Probe B	
	16	Clear Z	
	17	I → Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE RAB 53	Replace Add	Form in A the sum of original contents of A and operand. Replace operand with results. D-B-C sequence, 19.2 us.

B Cycle	TIME	COMMAND	REMARKS
	00	-Z1 → R, P → Q	
	01	Clear B	
	03	Toggle B	Form backward address
	04	Probe B	
	05	B → S	
	10	MCS → I	Read operand
	15	A → Q, Z → R	
	16	Clear Z	
	17	I → Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B → A	Z + A in A
	37	Set C cycle FF	
C Cycle	05	A → Q	
	10	B → I	
	11	Clear B	
	13	Toggle B	Establish result in Z-register
	14	Probe B	
	16	Clear Z	
	17	I → Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE AOD 54	Replace Add One	Form in A the sum of operand and one. Replace operand with result. D-B-C sequence, 19.2 us.

	TIME	COMMAND	REMARKS
B Cycle	00	Zl → R	(+ 1 → Ru)
	01	Clear B	Form operand address
	03	Toggle B	
	04	Probe B	
	05	B → S	
	10	MCS → I	Read operand
	15	Z → Q, + 1 → R	
	16	Clear Z	
	17	I → Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B → A	Z + 1 in A
	37	Set C cycle FF	
C Cycle	05	A → Q	
	10	B → I	Establish operand plus one in Z-register
	11	Clear B	
	13	Toggle B	
	14	Probe B	
	16	Clear Z	
	17	I → Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE AOI 55	Replace Add One	Form in A the sum of operand and one, Replace operand with result. D-A-B-C sequence, 25.6 us.

A Cycle	TIME	COMMAND	REMARKS
	00	Zl→ R	(+ 1→ Ru)
	01	Clear B	
	03	Toggle B	Form indirect address
	04	Probe B	
	05	B→ S	
	10	MCS→ I	Read indirect address
	16	Clear Z	
	17	I →Z	
	37	Set B cycle FF	

B Cycle			
	00	Z→ R	
	01	Clear B	
	03	Toggle B	Form operand address
	04	Probe B	
	05	B→ S	
	10	MCS→ I	Read operand
	15	Z→ Q, + 1→ R	
	16	Clear Z	
	17	I→ Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→ A	
	37	Set C cycle FF	

CODE 55	Continued	
C Cycle	TIME	COMMAND	REMARKS
	05	A → Q	
	10	B → I	Establish operand plus one in Z-register
	11	Clear B	
	13	Toggle B	
	14	Probe B	
	16	Clear Z	
	17	I → Z	
	26	Set WRITE FF	
	37	Set D cycle FF	

CODE AOF 56	Replace Add One	Form in A the sum of operand and one. Replace operand with result. D-B-C sequence, 19.2 us.
B Cycle	TIME	COMMAND	REMARKS
	00	Zl→ R, P→ Q	(+ 1 →R)
	01	Clear B	
	03	Toggle B	Form forward address
	04	Probe B	
	05	B→ S	
	10	MCS →I	Read operand
	14	Z→ Q, + 1→ R	
	16	Clear Z	
	17	I→ Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→ A	Z + I in A
	37	Set C cycle FF	
C Cycle			
	05	A→ Q	
	10	B→ I	
	11	Clear B	
	13	Toggle B	Establish operand
	14	Probe B	plus one in Z-register
	16	Clear Z	
	17	I→ Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE AOB 57	Replace Add One	Form in A the sum of operand and one. Replace operand with result. D-B-C sequence, 19.2 us.

B Cycle	TIME	COMMAND	REMARKS
	00	-Z1→ R, P→Q	Form backward address
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B→S	
	10	MCS→I	Read operand
	15	Z→Q, + 1→ R	
	16	Clear Z	
	17	I→Z	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	Z + 1 in A
	37	Set C cycle FF	
C Cycle	05	A→Q	
	10	B→I	Establish operand plus one in Z-register
	11	Clear B	
	13	Toggle B	
	14	Probe B	
	16	Clear Z	
	17	I→Z	
	26	Set WRITE FF	Replace
	37	Set D cycle FF	

CODE		Jump if A contains all zeros, otherwise read next instruction. D cycle only, 6.4μs.
ZJF 60	Zero Jump	

D Cycle	TIME	COMMAND	REMARKS
			Next instruction address dependent on value of A.
	00	Zl→R, P→Q Blk + 1 →R	If A = 0, Jump
	00	P→Q, + 1→R	If A ≠ 0, go to next sequential address

CODE		If A does not contain all zeros, jump: otherwise read next instruction. D cycle, 6.4μs.
NZF 61	Not Zero Jump	

D Cycle	TIME	COMMAND	REMARKS
			Next instruction address dependent on value of A.
	00	Zl→R, P→Q, Blk + 1→R	If A ≠ 0, jump
	00	P→Q, + 1→R	If A = 0, go to next sequential address

CODE		Jump if A is positive; otherwise read next instruction. D cycle, 6.4μs.
PJF 62	Positive Jump	

D Cycle	TIME	COMMAND	REMARKS
			Next instruction address dependent on value of A.
	00	Zl→R, P→Q, Blk + 1→R	If A positive, jump
	00	P→Q, + 1→R	If A negative, go to next sequential address.

CODE		
NJF 63	Negative Jump	Jump if A is negative, otherwise read next instruction. D cycle, 6.4μs.

D Cycle	TIME	COMMAND	REMARKS
			Next instruction address dependent on value of A.
	00	Zl→R, P→Q, Blk + 1 →R	If A negative jump
	00	P→Q, + 1→R	If A positive go to next sequential address.

CODE		Jump if A contains all zeros; otherwise read next instruction. D cycle, 6.4μs.
ZJB 64	Zero Jump	

D Cycle	TIME	COMMAND	REMARKS
			Next instruction address dependent on value of A.
	00	-Z1→R, P→Q, Blk + 1→R	If A = 0 jump
	00	P→Q, + 1→R	If A ≠ 0 go to next sequential address

CODE		Jump if A does not contain all zeros; otherwise read next instruction. D cycle, 6.4μs.
NZB 65	Not Zero Jump	

D Cycle	TIME	COMMAND	REMARKS
			Next instruction address dependent on value of A.
	00	-Zl→R, P→Q, Blk + 1→R	If A ≠ 0, Jump
	00	P→Q, + 1→R	If A = 0, go to next sequential address

CODE		Jump if A is positive; otherwise read next instruction. D cycle, 6.4μs.
PJB 66	Positive Jump	

D Cycle	TIME	COMMAND	REMARKS
			Next instruction address dependent on value of A.
	00	-Z1→R, P→Q Blk + 1→R	If A positive, jump
	00	P→Q, + 1→R'	If A negative, go to next sequential address

CODE NJB 67	Negative Jump	Jump if A is negative, otherwise read next instruction. D cycle, 6.4μs.

D Cycle	TIME	COMMAND	REMARKS
			Next instruction address dependent on value of A.
	00	-Z1→R, P→Q, Blk + 1→R	If A negative jump
	00	P→Q, + 1→R	If A Positive go to next sequential address.

CODE		
JPI 70	Jump Indirect	Unconditional; obtain next instruction address from location specified by E, which designates one of first 64 locations. D-B sequence, 12.8 us.

B Cycle	TIME	COMMAND	REMARKS
	00	Z1→ R, Z→ R	+ 1→ R (B = 0)
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B →S	
	10	MCS →I	Read jump address
	16	Clear Z	
	17	I→ Z	
	37	Set D cycle FF	
		Next D Cycle	
	00	Block P→ Q, - 1→ R	
	00	Z→ R	
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B→ S	
	10	MCS →I etc.	

CODE JPF 71	Jump forward indirect	Unconditional; obtain next instruction from the location specified by (P + E). D-B sequence 12.8μs.

B Cycle	TIME	COMMAND	REMARKS
	00	Z1→R, (+1→Ru) P→Q	
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	0805	B→S	
	10	MCS→I	Read jump address
	16	Clear Z	
	17	I→Z	
	37	Set D cycle FF	

CODE		Read from selected input device into storage up to but not including terminating address. D-B-C-D-C-D. Sequence, $12.8 + 12.8^{n}\mu s$.
INP 72	Input	

B Cycle	TIME	COMMAND	REMARKS
	00	Z1→R, P→Q	(+1→Ru)
	01	Clear B	
	03	Toggle B	Starting Address to S
	04	Probe B	
	05	B→S	
	10	MCS→I	
	16	Clear Z	
	17	I→Z	
	20	Z→R	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	26	B→A	
	31	Set Wait Input FF	Disable timing chain recirculation;
	37	Set I/O Sequence Control FF	Issue Input Request
	37	Set C cycle FF	Await Input Ready
C Cycle			
	00	A→Q	Clear Wait Input FF, Chain starts when Resume is received.
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B→S	
	10	Ext. Input →I	
	16	Clear Z	
	17	I→Z	Input Word in Z
	26	Set Write FF	Record input word
	26	+1→R, A→Q	Increase A by 1
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	35	Set Block + 1→R	Every time Except 1st
	36	B→A	
	37	Set D cycle FF	
	37	Set Function Ready FF	to block P+1 in future D cycles

CODE 72 Cont'd			
D Cycle	TIME	COMMAND	REMARKS
	00	P→Q (+1→R)	lst time only (term. address to Z)
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	Set Wait Input FF	
	05	B→S	
	06	Clear Block +1→R	Permits A+1 on Next C Cycle
	10	MCS→I	
	11	Clear P	
	12	S→P	
	16	A→Q, -Z→R	Initiate A-Z
	16	Clear Z	
	17	I→Z	
	26	A→Q; +Z→R	Initiate Restore A
	26	B→A	Check A=0
	33	Clear I/O Seq. FF	if A = 0
	35	Set Wait Input FF	if A ≠ 0, and issue Input Request
	36	B→A	A holds restored value
	37	Set C Cycle FF Set wait input	Await Input Ready FF Wait for resume.

CODE		Transmit to selected output device from storage. D-B-C-D-C-D... Sequence, $12.8 + 12.8^{n}\mu s$.
OUT 73	Output	

	TIME	COMMAND	REMARKS
B Cycle	00	Z1→R, P→Q	
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	06 05	B→S	
	10	MCS→I	Read starting address
	16	Clear Z	
	17	I→Z	
	20	Z→R	
	21	Clear B	
	23	Toggle B	
	24	Probe B	
	27 26	B→A	
	37	Set I/O Sequence FF	
	37	Set C Cycle FF	
C Cycle	00	A→Q	
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	06 05	B→S	
	10	MCS→I	output word read
	16	Clear Z	
	17	I→Z	
	26	Set Write FF	Restore word to MCS
	26	+1→R, A→Q	Increase A by 1
	31	Set Wait Output	Send Information Ready signal
	31	En Z→Output lines	
	31	Clear B	
	33	Toggle B	
	34	Probe B	
	35	Set Block + 1→R	(Everytime except 1st)
	37 36	B→A	
	37	Set D Cycle FF	
	37	Set Function Ready	to block P + 1 in future D cycles

CODE 73 (Cont'd)			
D Cycle	TIME	COMMAND	REMARKS
	00	Clear Wait output	Resume starts chain
	00	P→Q, (+1→R)	First time only (term. address to Z)
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	05	B→S	
	06	Clear Block +1→R	Permits A +1 in next C cycle
	10	MCS→I	
	11	Clear P	
	12	S→P	
	16	A→Q, -Z→R	initiate A -Z
	16	Clear Z	
	17	I→Z	
	26	A→Q; +Z→R	Initiate Restore A
	26	B→A	Check A = 0
	33	Clear I/O Seq. FF	If A = 0
	36	B→A	A holds restored value
	37	Set C cycle FF	

CODE OTN 74	Output Direct	Transmit lower 6 bits of instruction to selected equipment. D cycle, 6.4μs.
D Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	P→Q, + 1→R	
	01	Clear B	Form address
	03	Toggle B	
	04	Probe B	
	06 05	B→S	
	10	MCS→I	Read instruction
	11	Clear P	
	12	S→P	
	16	Clear Z	
	17	I→Z	
	22	Clear F	
	23	Zu→F	
	35	Set Wait Output	Transmit information
	35	Enable Z→Output	
	37	Set D cycle FF stop	Wait for resume

CODE EXF 75	External Function	Transmit external function code to external equipment. D-B sequence, 12.8μs.
B Cycle	**TIME**	**COMMAND**	**REMARKS**
	00	Z1→R, P→Q	(+ 1 → Ru)
	01	Clear B	Form address forward
	03	Toggle B	
	04	Probe B	
	05	B → S	
	10	MCS → I	Read forward address
	16	Clear Z	
	17	I → Z	
	31	Set Function Ready	disable recirculation
		En Z→ Output lines	
	37	Set D Cycle FF	Chain stops, wait for Resume. On Resume, Clear Function Ready FF, start chain, RNI.

CODE		Read into A one frame of data from selected input device, clearing previous contents of A. D-C sequence, 12.8μs.
INA 76	Input to A	

C Cycle	TIME	COMMAND	REMARKS
	00	Z→Q	(Chain starts at Input Ready signal)
	01	Clear B	
	03	Toggle B	
	04	Probe B	
	06	B→A	Information requested in A.
	10	MCS→I	Read 76 instruction again
	16	Clear Z	
	17	I→Z	
	26	Set Write FF	Restore 76 instruction
	37	Set D cycle FF	
			(I/O Sequence Control and Wait Input FFs are set at D_{35} for 76 instructions)

APPENDIX D
BUILDING BLOCK

The basic building block of the computer is a single inverter transistor circuit. Thi circuit is used: (1) alone, as a single inverter; (2) in a pair to form a flip-flop; and (3) in a configuration of three to form a control delay. The major portion of the computer is constructed by interconnecting these circuits, which are packaged on 2 1/2 by 2 1/8 inch printed circuit cards (figure 1). Each card is equipped with a 15-pin male connector for plugging into the major equipment chassis.

ANALYSIS OF SINGLE INVERTER

Within the computer two signal levels are used, -3.0v, logical "1" and -0.5v, logical "0". The single inverter inverts these signal levels: a -3.0v input becomes a -0.5v output, and vice versa.

In the standard inverter circuit shown in figure 2, transistor Q01 is connected as an emitter-follower; Q02, as an amplifier. The collector circuits of the transistors have two feedback loops which prevent the transistors from being driven to cutoff or saturation. As a result, switching from one state to the other is accomplished in from 50 to 100 nanoseconds.

An input signal is applied via isolation diodes CR01 or CR02 to a voltage divider network composed of resistors R07, R08, R09, R10 and R11. An input signal of -0.5v (point A) results in -1.5v at point B and 0.8v at the base of Q01 (point C). CR01 is biased 1v in the backward direction to provide for noise suppression at the input of the inverter. Capacitor C01, between CR01 and the base of Q01, provides rapid coupling of input signal changes to Q01, improving the switching time of the circuit.

Transistors Q01 and Q02 each provide beta* current gains of approximately 100; loop gain of the two transistors is on the order of 10^4. The collector current of Q01 and Q02 develops the output voltage across resistor R07. Output diode CR09 isolates the output line from the other output line connected to CR10.

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* The beta current gain is the ratio of collector current to base current.

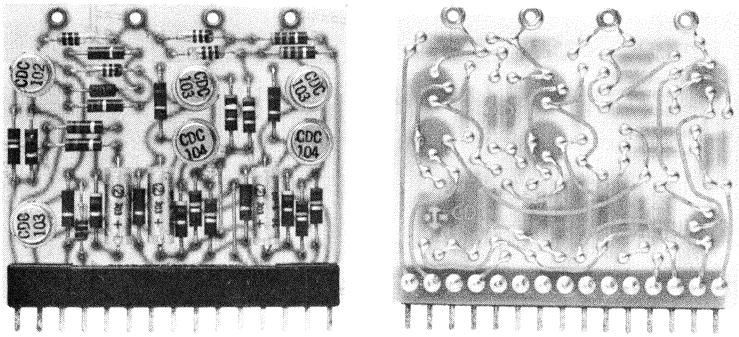


Figure 1. Typical Printed Circuit Card

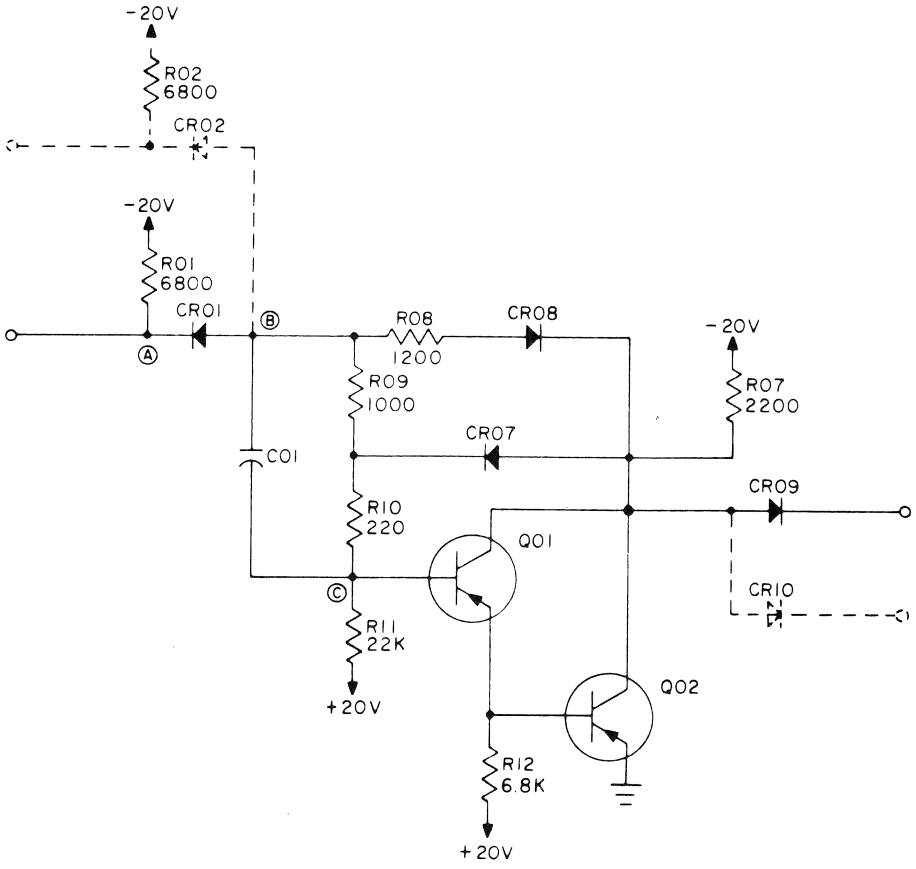


Figure 2. Schematic Diagram of Standard Inverter Circuit.

Diodes CR07 and CR08 form the feedback loops which prevent transistors Q01 and Q02 from being driven to cutoff or saturation. The positive-going limit allows a maximum transistor conduction that is less than saturation; the negative-going limit fixes a minimum conduction for the transistors. When the transistors approach cutoff, their collectors approach -3.0v. The collector potential is coupled back to the base of Q01 through CR08, R09 and R10. As a consequence the base of Q01 always is held at a sufficiently negative voltage to permit some minimum conduction of Q01 and thus Q02.

When the transistors approach saturation, the collectors approach 0v. The collector potential is coupled back to the base of Q01 through CR07 and R10. The base of Q01 is thus prevented from becoming so negative that saturation occurs.

FLIP-FLOP

All short term storage of information in the computer is accomplished by flip-flops (FFs). A FF is two single inverter circuits interconnected as shown in figure 3 (each rectangle represents a single inverter). One of the inverters is the set side of the FF; the other, the clear side. The FF is placed in the "1" (set) state by a set input that is "1". Conversely, it is placed in the "0" (cleared) state by a clear input that is "1". (Set and clear inputs are never "1" at the same time.)

The storage capability of a FF means simply that it remains in a state that is indicative of the last "1" input received. Specifically, if a "1" pulse is present at the set input, then the output of inverter A^{000} (figure 3) becomes "0". This output is applied as an input to A^{001} and the output then becomes "1". The output of A^{001} is fed back to A^{000} Thus, when the set input returns to "0", the feedback connection between A^{000} and A^{001} permits the storage of the state to which the "1" pulse on the set input forced the FF. Should the clear input later receive a "1" pulse, the output of A^{001} becomes "0", and the feedback input to A^{000} is "0". Consequently, A^{000} furnishes a "1" output which is returned to A^{001} to replace the "1" pulse at the clear input.

When the FF is set, A^{001} has a "1" output, and A^{000} has a "0" output. Conversely, when the FF is cleared, A^{001} has a "0" output, and A^{000} has a "1" output.

The conventional square or box symbol for a FF is used in figure 3 to show the relationship between it and the inverter configuration which forms the FF. The square which represents the FF encompasses the crossover of the outputs.

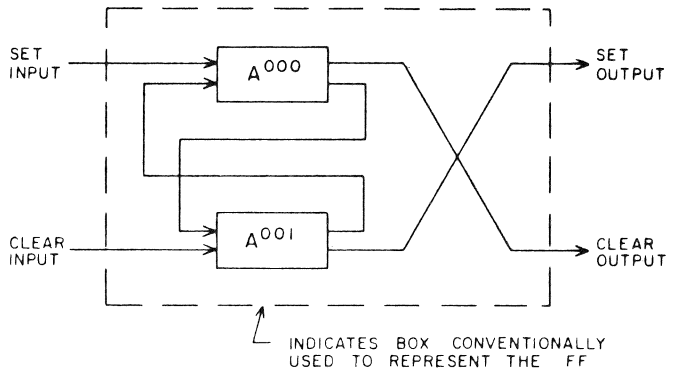


Figure 3. Interconnection of Inverters to Form a Flip-Flop

CONTROL DELAY

The single inverter and FF described above are static, unclocked devices; the output of the inverter is a steady-state inversion of its input. A set FF provides a steady "1" from the set output and a "0" from the clear output until it is cleared. Timed and properly spaced pulses are essential to computer operation. The control delay (figure 4) shapes and resynchronizes the signals to provide timed outputs.

Outputs from the master clock are two sine waves 180^{o} out of phase. Since these waves are clipped and shaped by the inverter circuits to which the clock cards are connected, they are square waves (C^{000} and C^{001}) in figure 4b. The difference in times that the simplified clock waves remain at 0v and -3v is due to the threshold (approximately -1.5v) of the subsequent inverters.

The control delay consists of a special FF (H^{---}) and one or more inverters (V^{---} or N^{---}) connected to the "0" output of the FF (figure 4a). The special FF has set inputs only, those going to I^{1}. The logic inputs (one of which must be clocked) are always signals from other building blocks. Feedback from I^{2} to I^{1} is gated by one of the clock phases, which is opposite to that applied to the output inverters. Thus, in figure 4a the odd phase (C^{001}) gates the feedback and clocks the input from K^{025}. The even phase, C^{000}, goes to output inverter V^{000}.

During the odd clock phase (C^{001}) the input signal sets FF, H^{000}. The internal feedback is gated during this clock phase so that the FF action extends (or delays) the original input signal. The even clock phase (C^{000}) gates the FF output. Duration of the output from V^{000} is established by the even clock phase.

In the waveforms for the control delay elements shown in figure 4b, the internal switching time of each inverter is the minimum value of 50 nanoseconds. Shaded areas indicate variations in pulses due to external wiring delays. If, for example, wiring delays were reduced to zero, the output of N^{901} would go to "0" at time 2 and remain "0" until time 5. At the other extreme, if the delay were a maximum of 50 nanoseconds, the output of N^{901} would go to "0" at time 3 and remain "0" until time 6.

The time at which the output of I^1 may go to "0" varies over a 100-nanosecond period. The delays introduced at N^{901} are felt at I^1 also. If N^{901} has the maximum delay but I^1 has no delay, the I^1 output goes to "0" at time 7 and remains "0" until time 13. If both N^{901} and I^1 have the full delay, the I^1 output is "0" from time 8 to time 14.

If capacitive wiring delays are zero, the leading edge of the output from V^{000} occurs at time 9 because the clock input to V^{000} from C^{000} does not go to "0" until time 8. The logic input signal to the control delay, gated by N^{901}, goes to "0" at time 10; however, C^{001} allows this signal to be replaced by gating the feedback from I^2 to I^1 until time 12. As a result, the original input signal is provided as an output from I^1 until at least time 13.

The output of I^1 encompasses the "0" portion of C^{000} (figure 4b). Since the output of V^{000} is the AND function of NOT C^{000} and NOT I^1, it is a "1" only when both are "0". Therefore, the occurrence and duration of the V^{000} output are determined by the period that C^{000} is a "0".

The delay interval of 0.2 microsecond is the period of the master clock; that is, the interval between the leading (or trailing) edges of successive clock phase pulses.

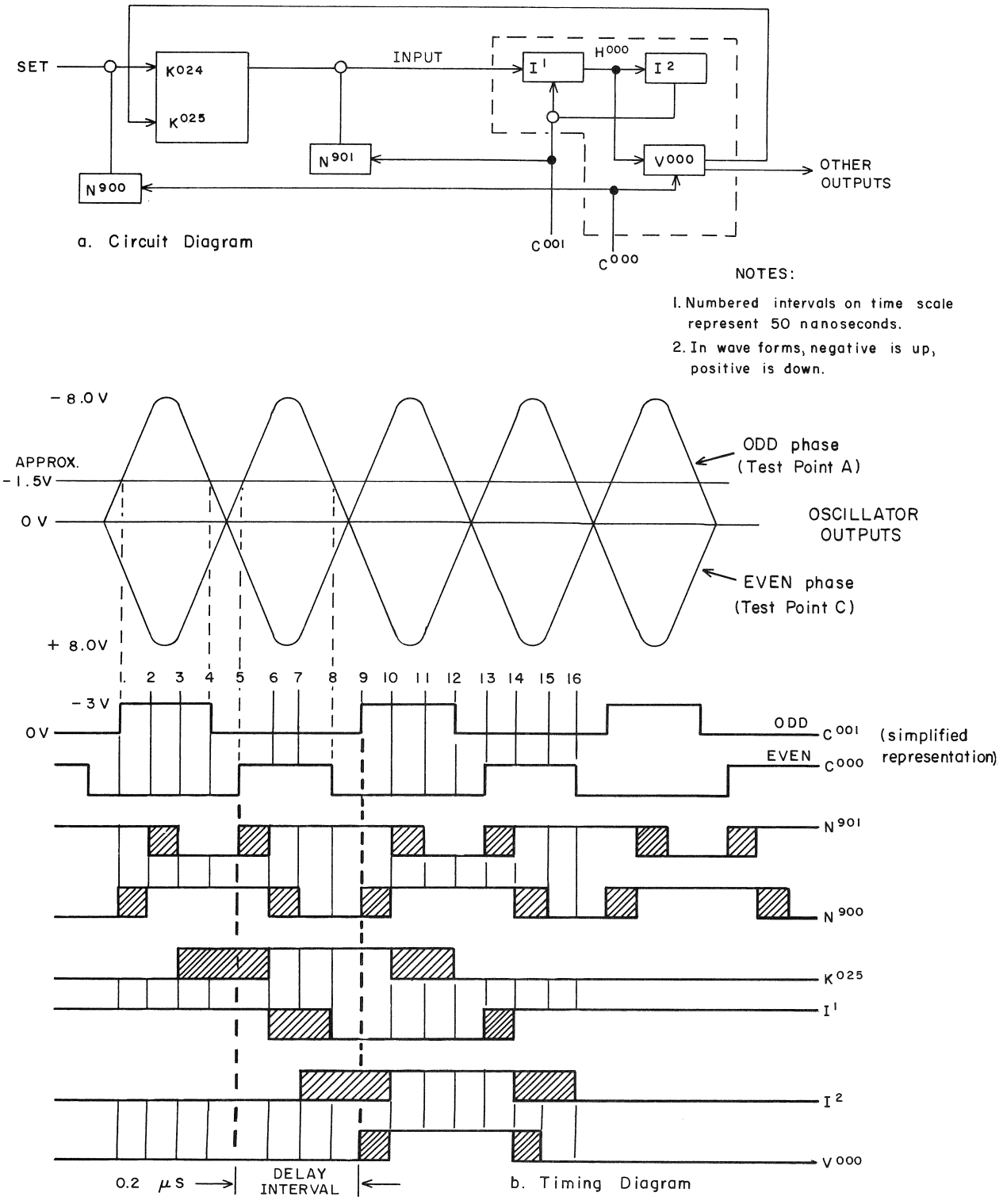


Figure 4. Control Delay

AND CIRCUIT

The AND circuit is shown in figure 5. The diodes of an AND circuit are the output diodes of inverters. As many as four diodes, each from different inverters, may be connected in an AND. The common cathode connection of the diodes is tied to the input of an inverter, which furnishes the remaining elements of the AND circuit. In order for the output of the AND to be a "1", that is, at -3.0v, inputs A, B and C must all three be at -3.0v. If any of the inputs are at -0.5v ("0"), then the cathodes of all three diodes are held at this potential, as is the output at D.

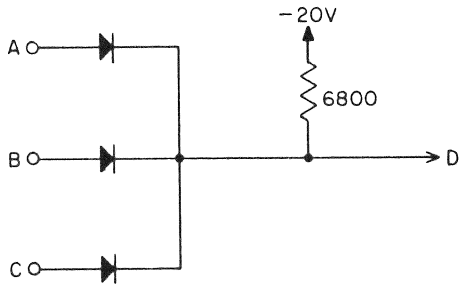


Figure 5. AND Circuit

OR CIRCUIT

The OR circuit consists of the input components of an inverter. The inverter shown in figure 2 has a two-input OR circuit, which involves R01, CR01, and R02 as well as voltage divider R09, R10 and R11 connected to -20v.

The potential at B, the common junction of the anodes of the OR diodes, is -1.5 (indicating a "0" in the circuit) only if both inputs at the cathodes of CR01 and CR02 are at 0.5v. If either OR input goes to -3.0v ("1"), then the potential at B is forced more negative than -1.5v. This more negative potential indicates a "1".

LOGIC EQUATIONS

A single inverter is a circuit which provides as an output the inverted form of its input. Thus if any of the inputs to an inverter is a "1", its output is a "0"; conversely, its output is a "1" only if all of its inputs are "0". An equation is a logic representation of the inverter. For example:

$$K^{310} = K^{311} + V^{220}\ F^{585}\ K^{415} + V^{676}\ F^{940}\ J^{134}$$

The symbol on the left of the equal sign, called the subject term, denotes the inverter described by the equation. The expression on the right of the equal sign describes the logical configuration of the inputs.

The + sign represents the OR function or logical sum; the absence of a sign between symbols represents the AND function or logical product. In the context of equations, the word term designates a single symbol or group of symbols that is a logical product. The equation given above for inverter K^{310} has three terms, each representing an input to the inverter. Thus K^{310} has a "0" output if: (1) K^{311} is a "1"; (2) the AND function of V^{220}, F^{585} and K^{415} is satisfied, that is, if each of them is a "1"; or (3) the AND function of V^{676}, F^{940} and J^{134} is satisfied, that is, if each of them is a "1".

Computer operations are timed by a two-phase master clock. Circuits which receive timing signals from the clock are denoted by symbols H, V and N. The base letter of master clock symbols is C. The even or odd character of the third superscript digit indicates timing relations as follows:

C---	with odd third digit	represents a circuit furnishing odd phase clock pulses
C---	with even third digit	represents a circuit furnishing even phase clock pulses
H--- V--- N---	with odd third digit	provides an output during odd clock phases receives an input during even clock phases
H--- V--- N---	with even third digit	provides an output during even clock phases receives an input during odd clock phases

Circuits with symbols L and M are not represented by complete equation entries. In these circuits only inputs or outputs (but not both) are represented by equation symbols.

LOGIC DIAGRAM SYMBOLS

The logic diagrams use five basic symbols to represent the logic properties of circuit configurations in the computer (figure 6).

Inputs to the diagram symbols are identified by arrows; outputs, by the absence of arrows. The OR function is represented on diagrams by arrows to the inverter. The AND function is represented by a small circle. An input to the AND is represented by

a line; the output from the AND (which is input to a logical element such as an inverter) is represented by an arrow.

The FF is a storage device with two stable states, "1" (set) and "0" (clear), and is composed of two inverters. The logic symbol for a FF is a square formed from the rectangles representing the two inverters. The logic designations of the two inverters appear within the square. In a logic diagram, the inverter which receives the set input is at the top and the inverter which receives the clear input is at the bottom. Set outputs are received from the top inverter and clear outputs from the bottom (figure 3).

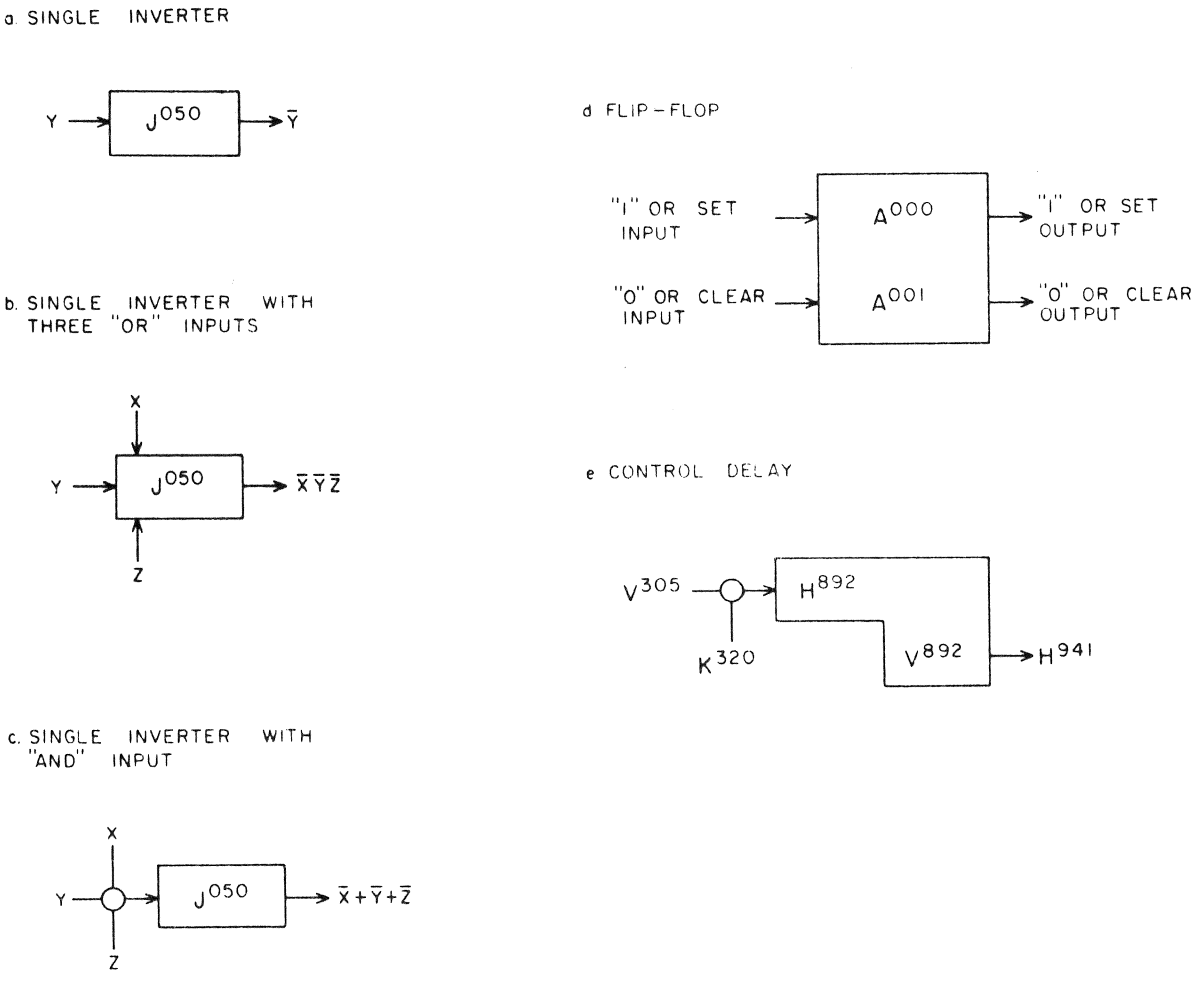


Figure 6. Logic Diagram Symbols

The logic designation of the set side of a FF has an even last digit and the clear side of the same FF is designated by the next odd digit; for example, $K^{942/943}$.

A control delay consists of an H^{---} part, which receives the input, and a V^{---} or N^{---} part, which provides the output. Control delays receive inputs during one clock phase and furnish an output during the opposite clock phase.

STANDARD CARD TYPES

The majority of printed circuit cards consist of one or two standard inverters on a single card. The cards differ in the number of inverters, the number of input and output diodes, and the electrical interconnections. An inverter may have a maximum of six inputs and a maximum of eight outputs. Since an unused input terminal is sensed as a "1" input, no more than the exact number of input terminals required can be present. Inverter cards, therefore, are provided with varying numbers of input and output terminals to handle the various logic requirements.

The inverter cards are assigned two-digit numbers; the higher-order designates the type of card, the lower-order the number of inputs associated with each inverter on the card. (On control delay cards, only one inverter has external inputs.) Inverter card types and the pin assignments for each are listed in table 1. The significance of letters is:

I - input
O - output
A or C - (as subscript) one of two inverters
C - (not as subscript), a clock pulse

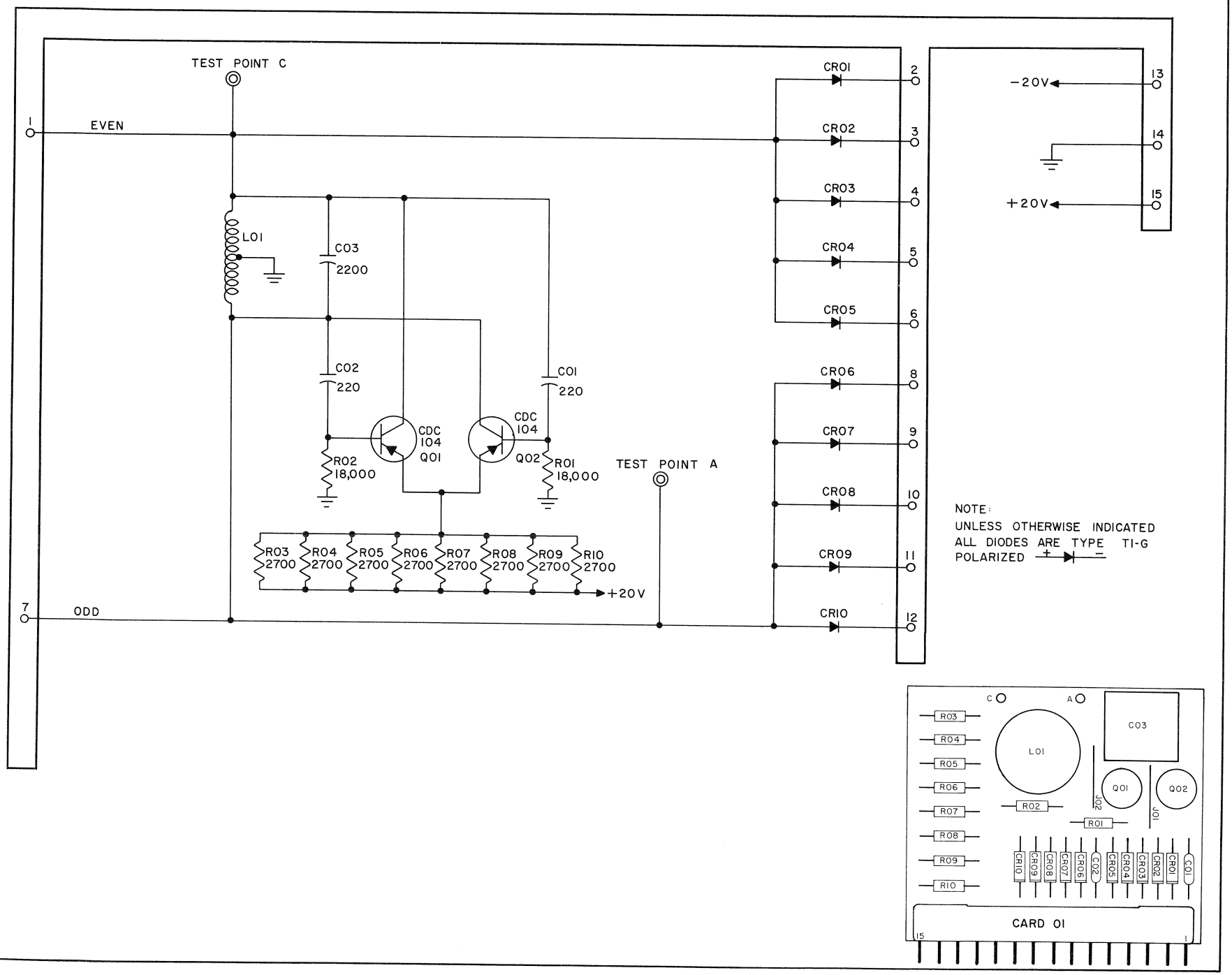
TABLE 1. DESCRIPTION OF STANDARD CARD TYPES

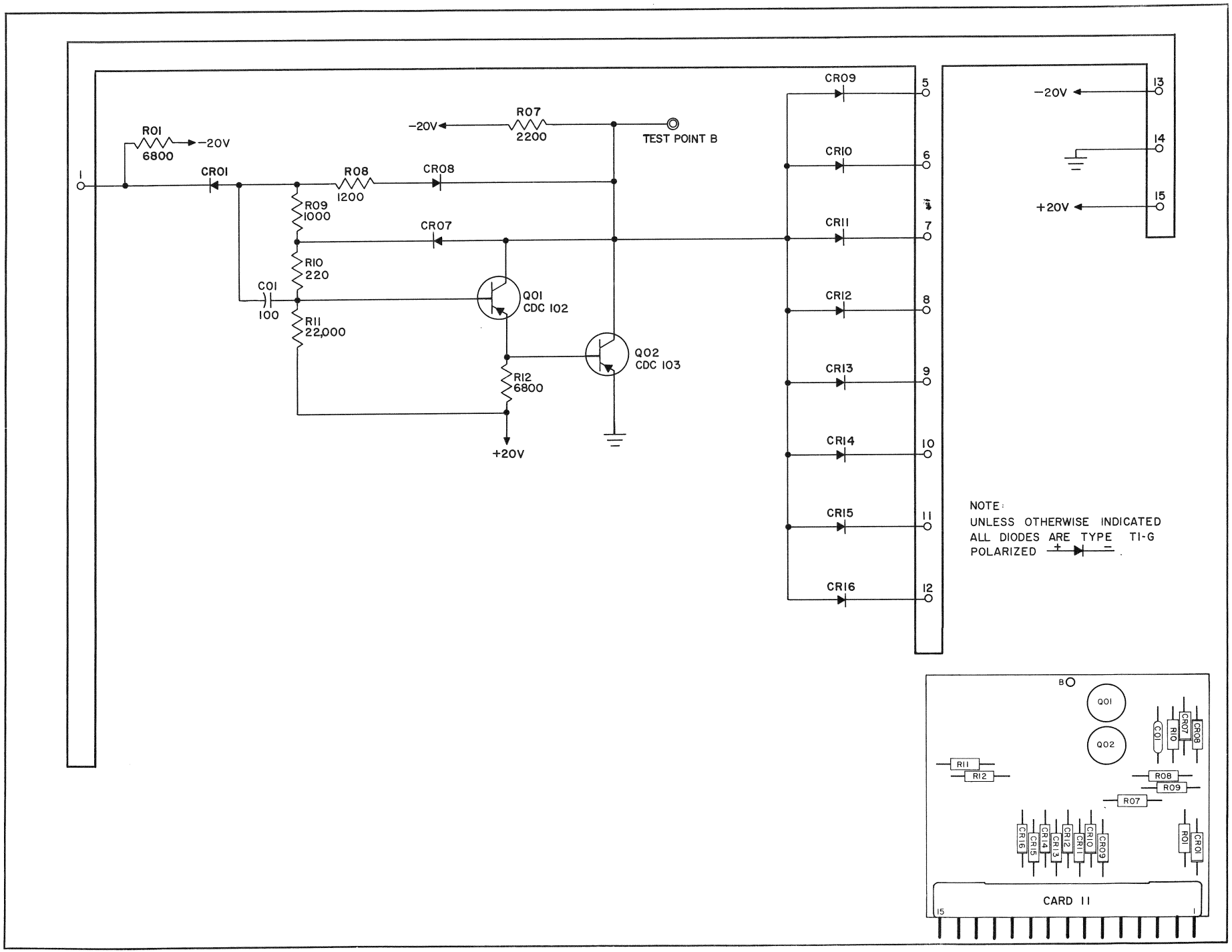
Type Designation	No. of Inverters	No. of inputs (per inverter)	No. of outputs (per inverter)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
11	1	1	8	I				O	O	O	O	O	O	O	O	-20V	Gd	+20V
12	1	2	8	I	I			O	O	O	O	O	O	O	O	-20V	Gd	+20V
13	1	3	8	I	I	I		O	O	O	O	O	O	O	O	-20V	Gd	+20V
14	1	4	8	I	I	I	I	O	O	O	O	O	O	O	O	-20V	Gd	+20V
15	1	5	7	I	I	I	I	I	O	O	O	O	O	O	O	-20V	Gd	+20V
16	1	6	6	I	I	I	I	I	I	O	O	O	O	O	O	-20V	Gd	+20V
21	2	1	5	I_A	O_A	O_A	O_A	O_A	O_A	I_C	O_C	O_C	O_C	O_C	O_C	-20V	Gd	+20V
22	2	2	4	I_A	I_A	O_A	O_A	O_A	O_A	I_C	I_C	O_C	O_C	O_C	O_C	-20V	Gd	+20V
23	2	3	3	I_A	I_A	I_A	O_A	O_A	O_A	I_C	I_C	I_C	O_C	O_C	O_C	-20V	Gd	+20V
24	2	4	2	I_A	I_A	I_A	I_A	O_A	O_A	I_C	I_C	I_C	I_C	O_C	O_C	-20V	Gd	+20V
31*	2	1	5	I_A	O_A	O_A	O_A	O_A	O_A	I_C	O_C	O_C	O_C	O_C	O_C	-20V	Gd	+20V
32*	2	2	4	I_A	I_A	O_A	O_A	O_A	O_A	I_C	I_C	O_C	O_C	O_C	O_C	-20V	Gd	+20V
33*	2	3	3	I_A	I_A	I_A	O_A	O_A	O_A	I_C	I_C	I_C	O_C	O_C	O_C	-20V	Gd	+20V
41**	2	1	6	I					C	O	O	O	O	O	O	-20V	Gd	+20V
42**	2	2	6	I	I				C	O	O	O	O	O	O	-20V	Gd	+20V
43**	2	3	6	I	I	I			C	O	O	O	O	O	O	-20V	Gd	+20V
44**	2	4	6	I	I	I	I		C	O	O	O	O	O	O	-20V	Gd	+20V
45**	2	5	6	I	I	I	I	I	C	O	O	O	O	O	O	-20V	Gd	+20V

* The types 31, 32, and 33 are two-inverter units which have internal feedback or flip-flop connections.
** The types 41, 42, 43, 44, and 45 are two-inverter units used in Control Delay circuits; a clock pulse applied to pin 6 controls the internal feedback connection.

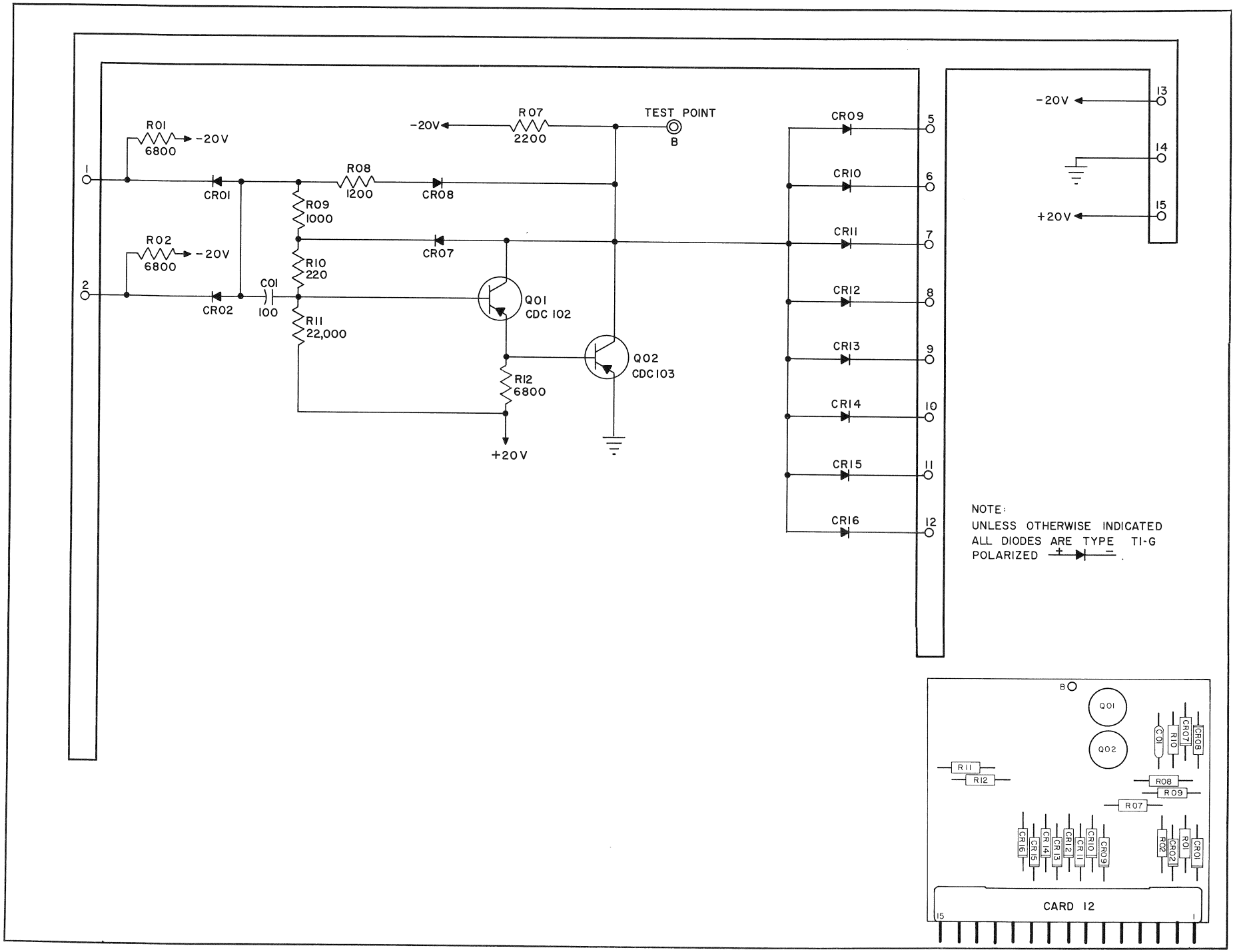
APPENDIX E
CARD SCHEMATICS

Schematic Diagrams	Card Type	Schematic Diagrams	Card Type
Oscillator	01	Control Delay	41
Single Inverter	11	Control Delay	42
Single Inverter	12	Control Delay	43
Single Inverter	13	R/W Driver	51
Single Inverter	14	Diverter	52A
Single Inverter	15	Selector	53
Single Inverter	16	Current Source	54
Double Inverter	21	Sense Amplifier	57
Double Inverter	22	Inhibit Generator	58
Double Inverter	23	Input Amplifier	61
Double Inverter	24	Output Amplifier	62
Flip-flop	31	Output Amplifier	67
Flip-flop	32	Filter	73A
Flip-flop	33	Reader Amp	75A
		Brake-Clutch (reader)	76A
		Filter	82
		Punch Puller	86

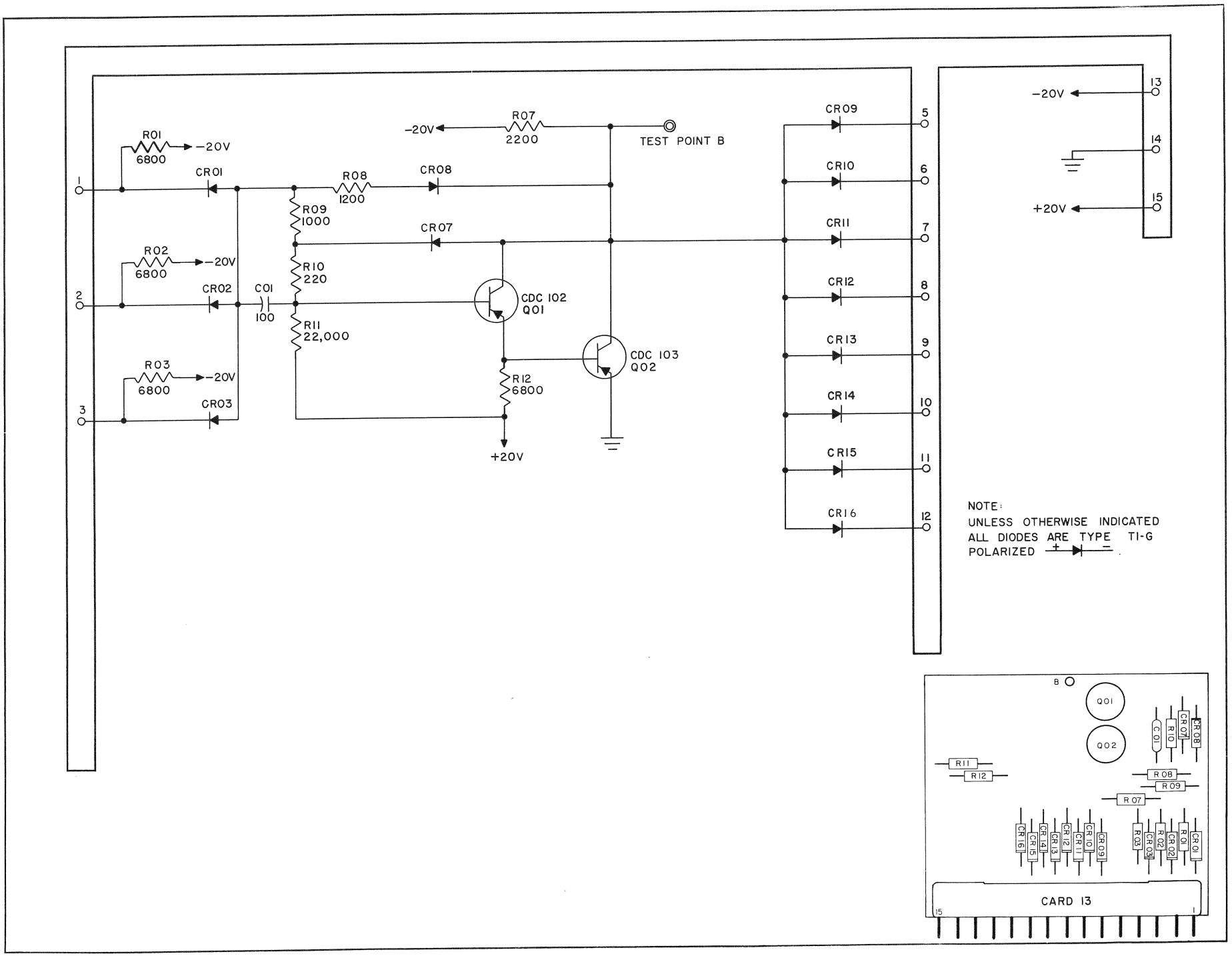

TEST POINT C
1
EVEN
L01
C03
2200
C02
220
C01
220
CDC
104
Q01
CDC
104
Q02
R02
18,000
R01
18,000
TEST POINT A
R03
2700
R04
2700
R05
2700
R06
2700
R07
2700
R08
2700
R09
2700
R10
2700
+20V
7
ODD
CR01
CR02
CR03
CR04
CR05
CR06
CR07
CR08
CR09
CR10
2
3
4
5
6
8
9
10
11
12
-20V
+20V
13
14
15
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
C
A
C03
L01
Q01
Q02
J02
J01
R02
R01
CR10
CR09
CR08
CR07
CR06
C02
CR05
CR04
CR03
CR02
CR01
C01
CARD 01
15
1



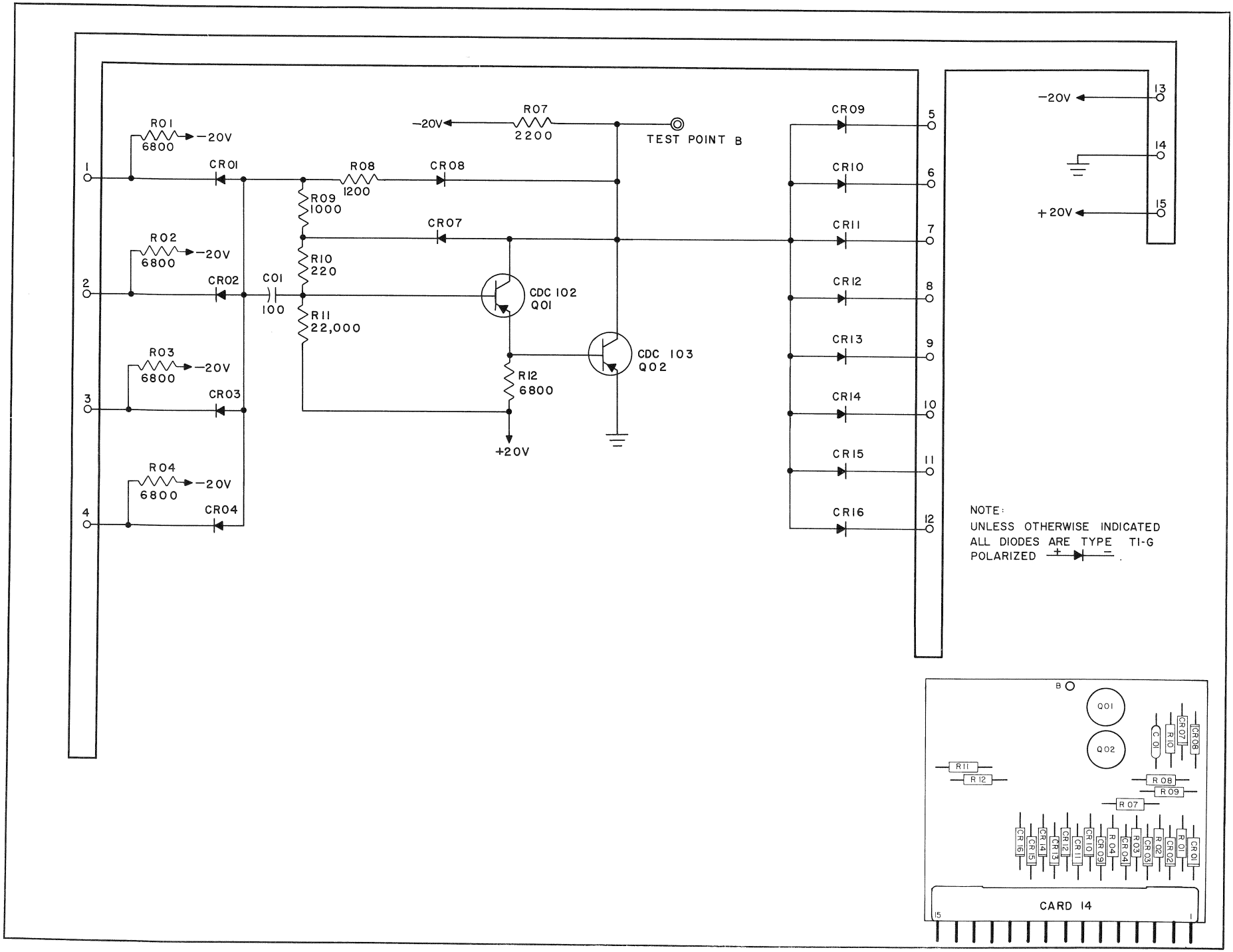
Single Inverter



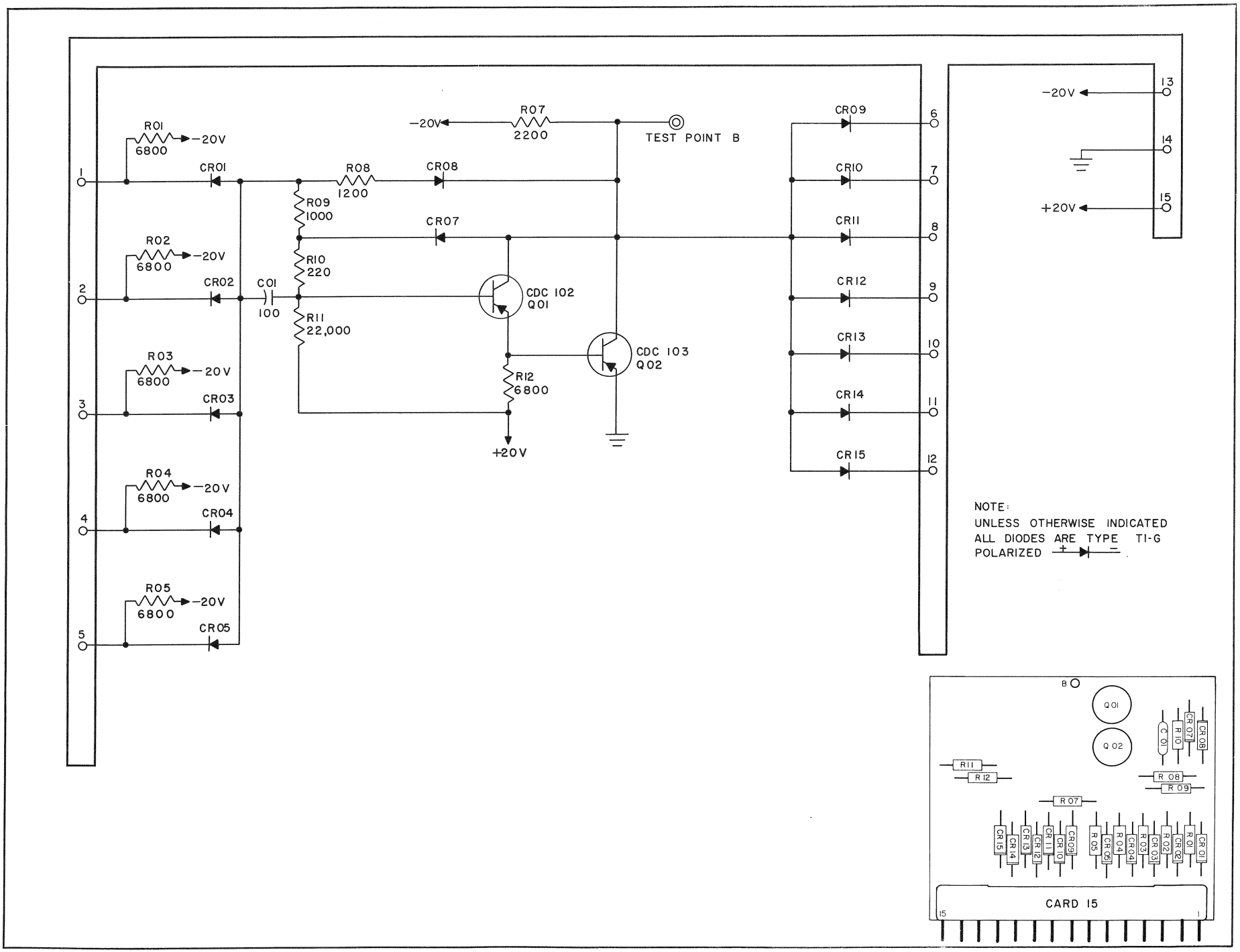
Single Inverter



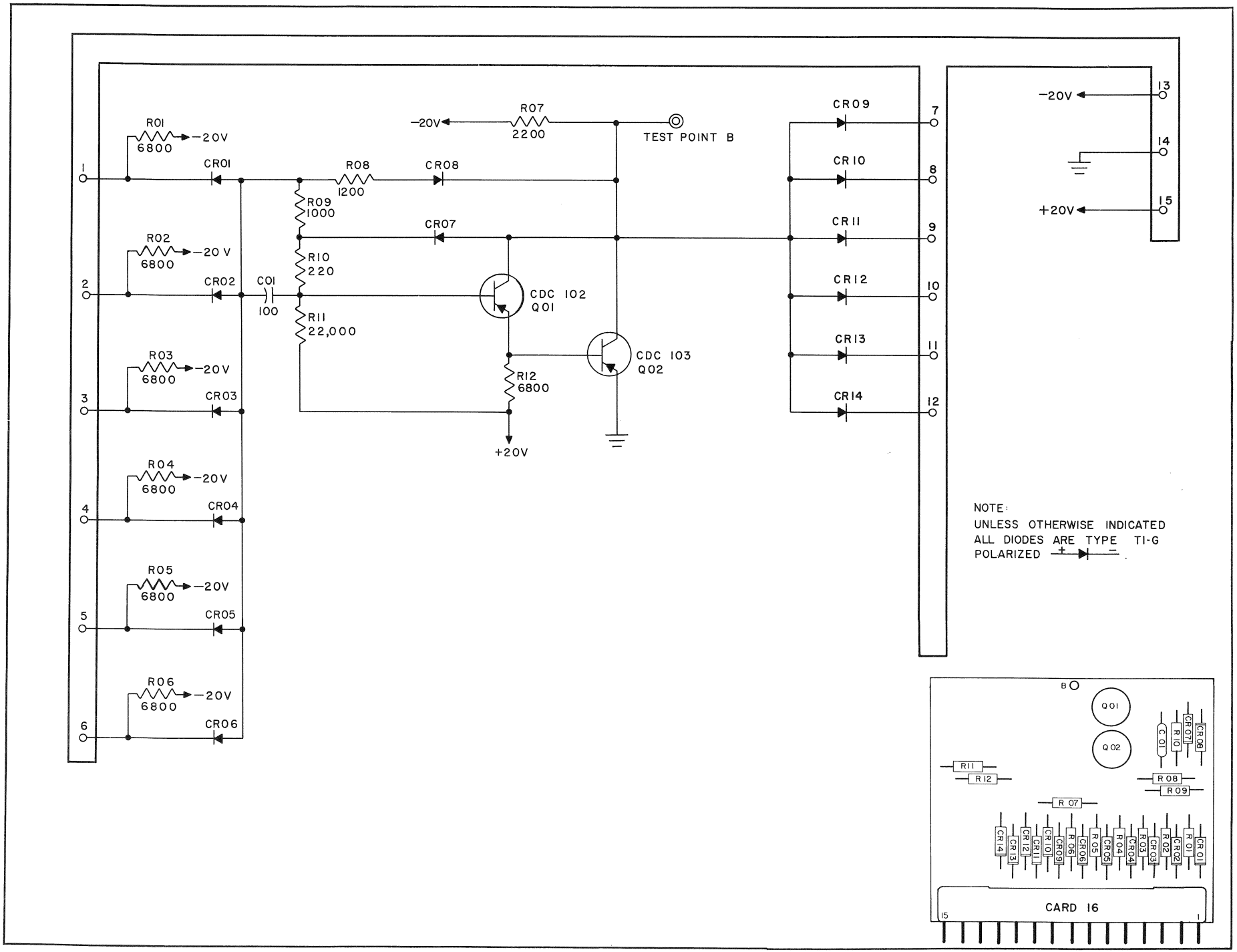
Single Inverter



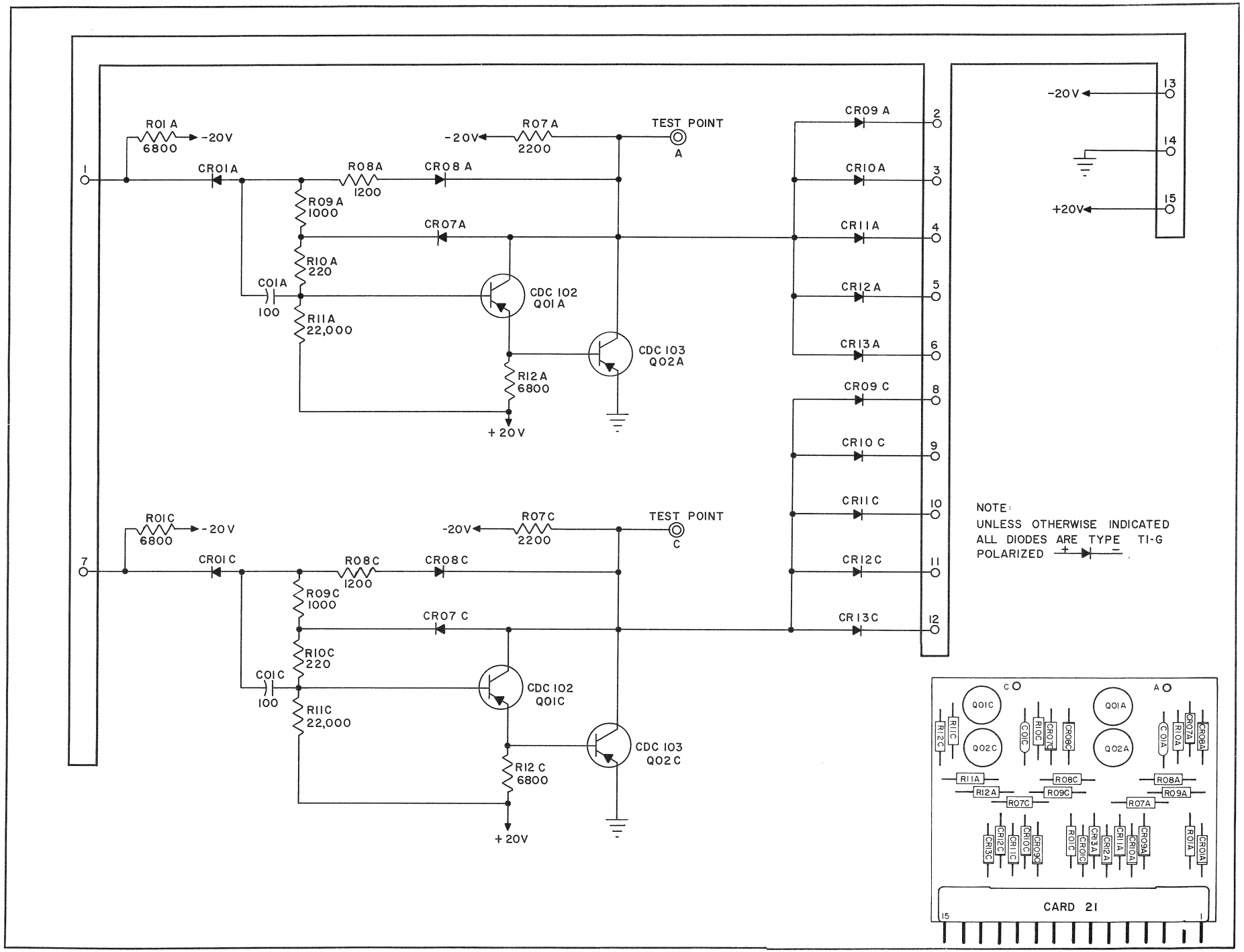
Single Inverter



Single Inverter

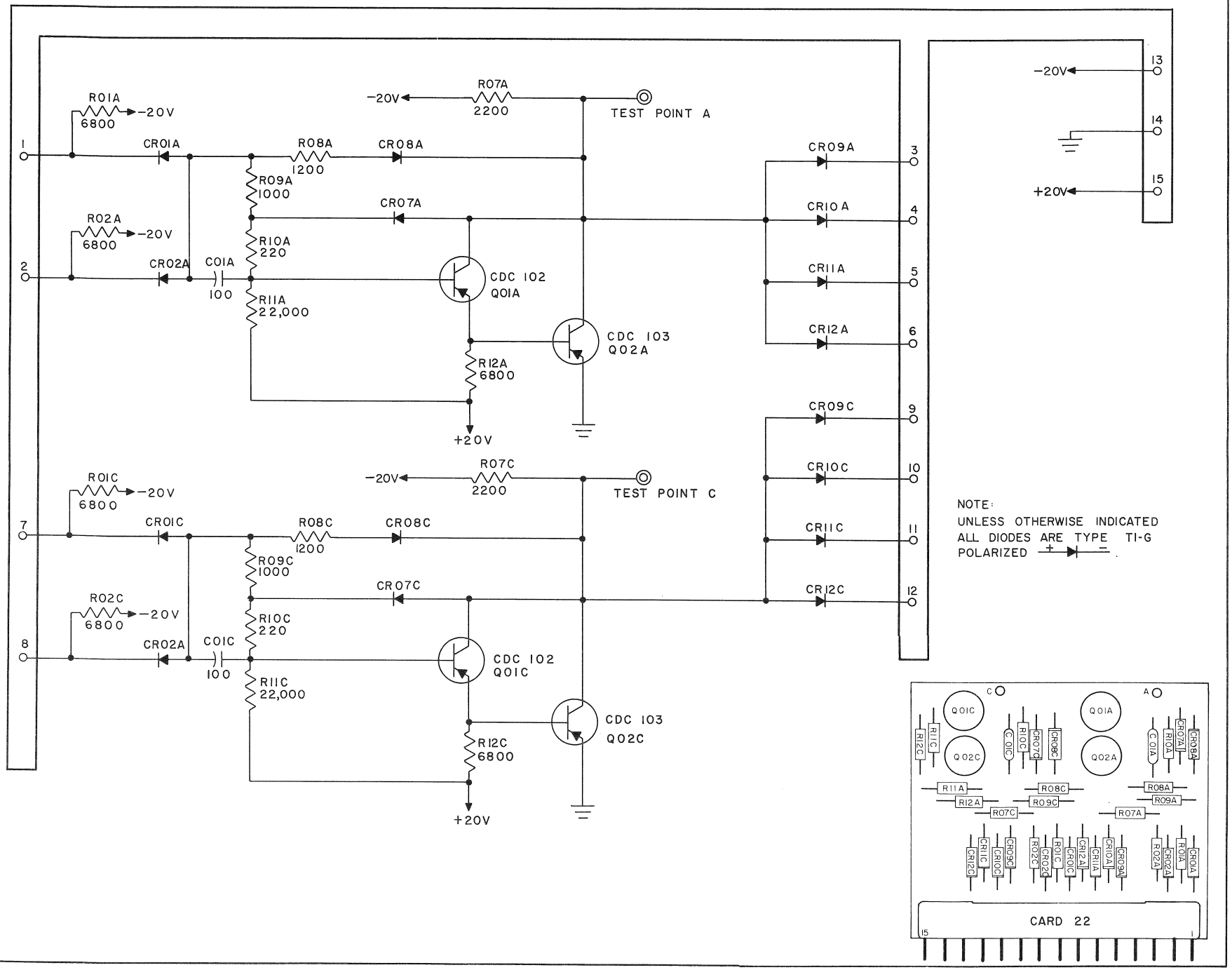


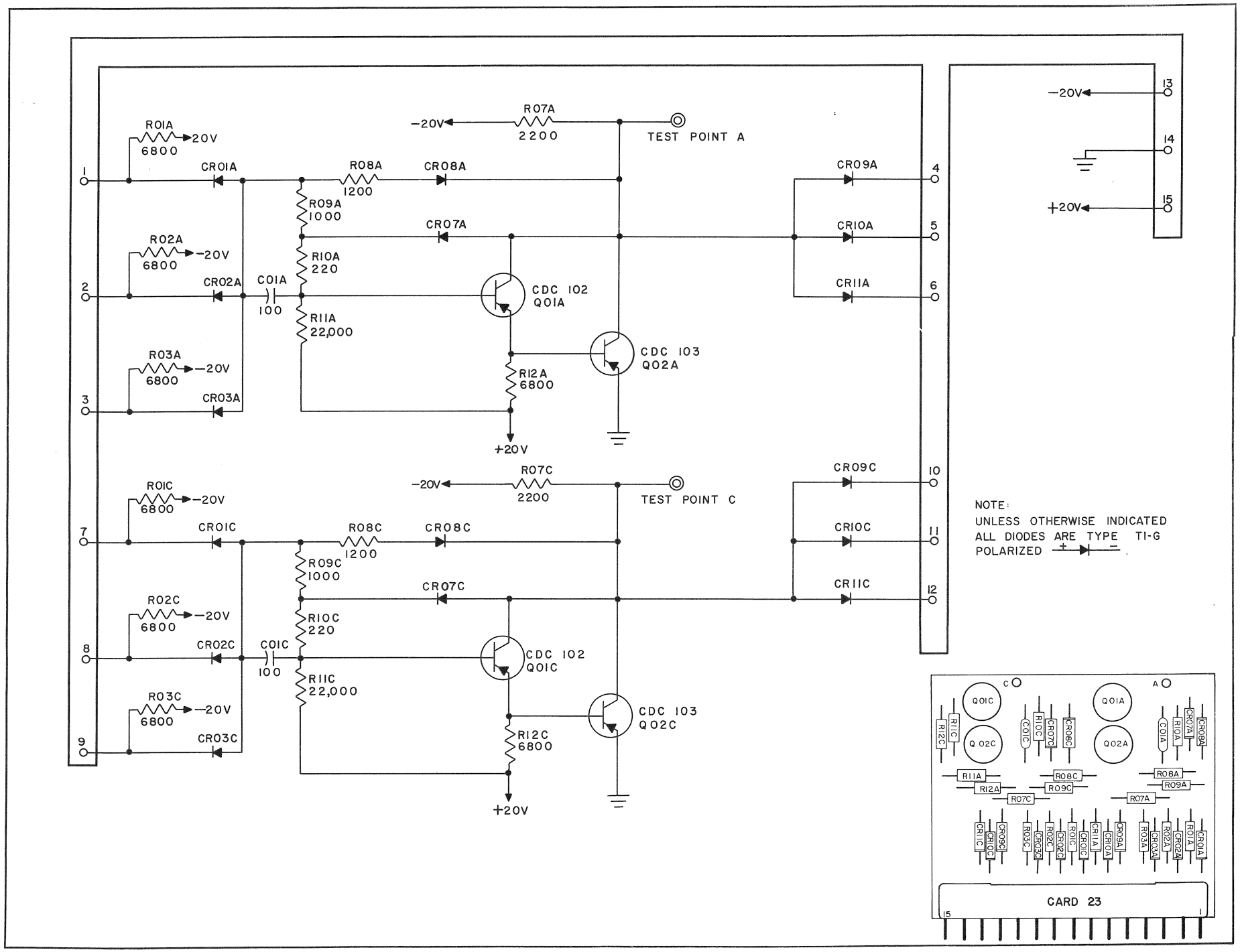
Single Inverter



Double Inverter

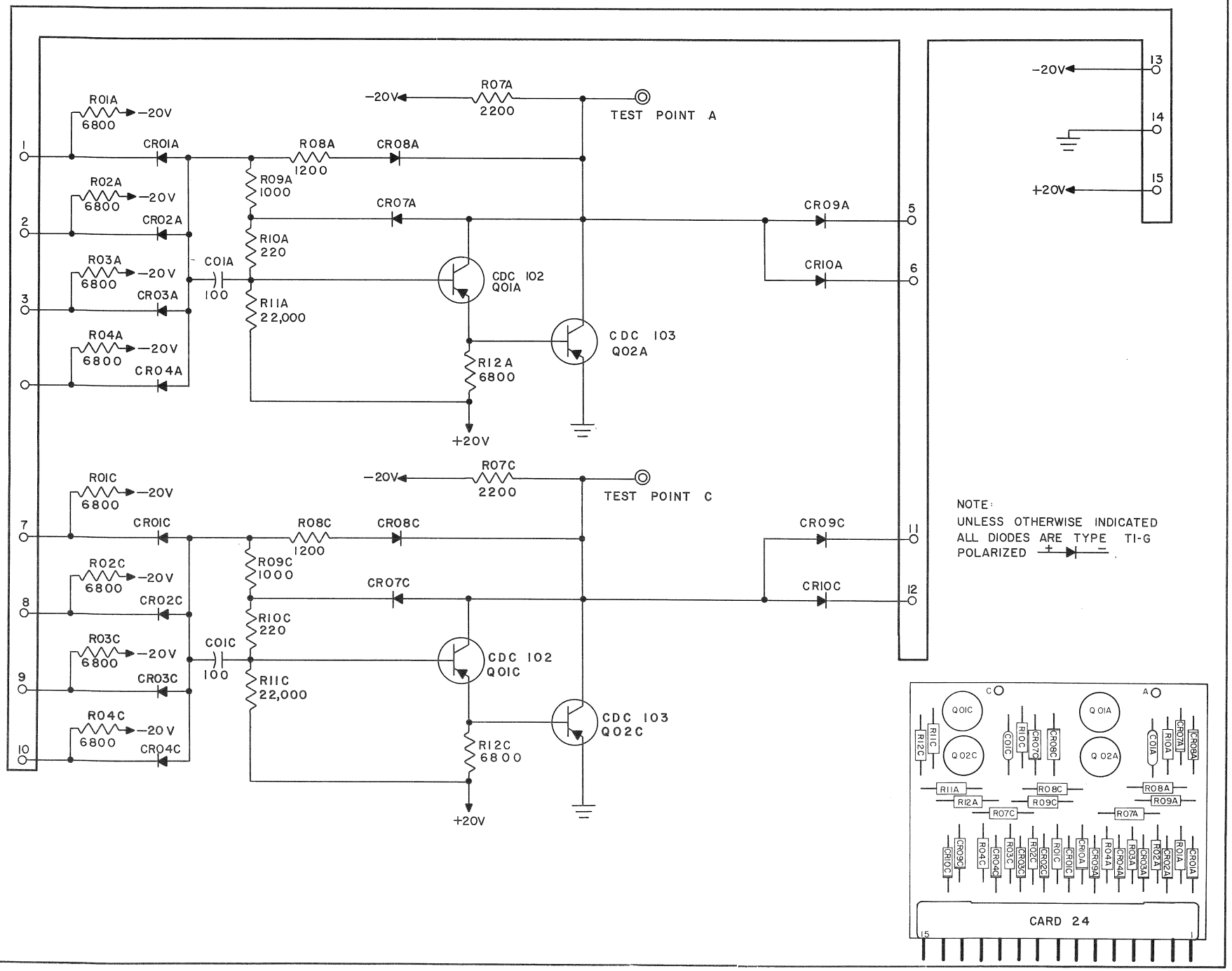
Double Inverter



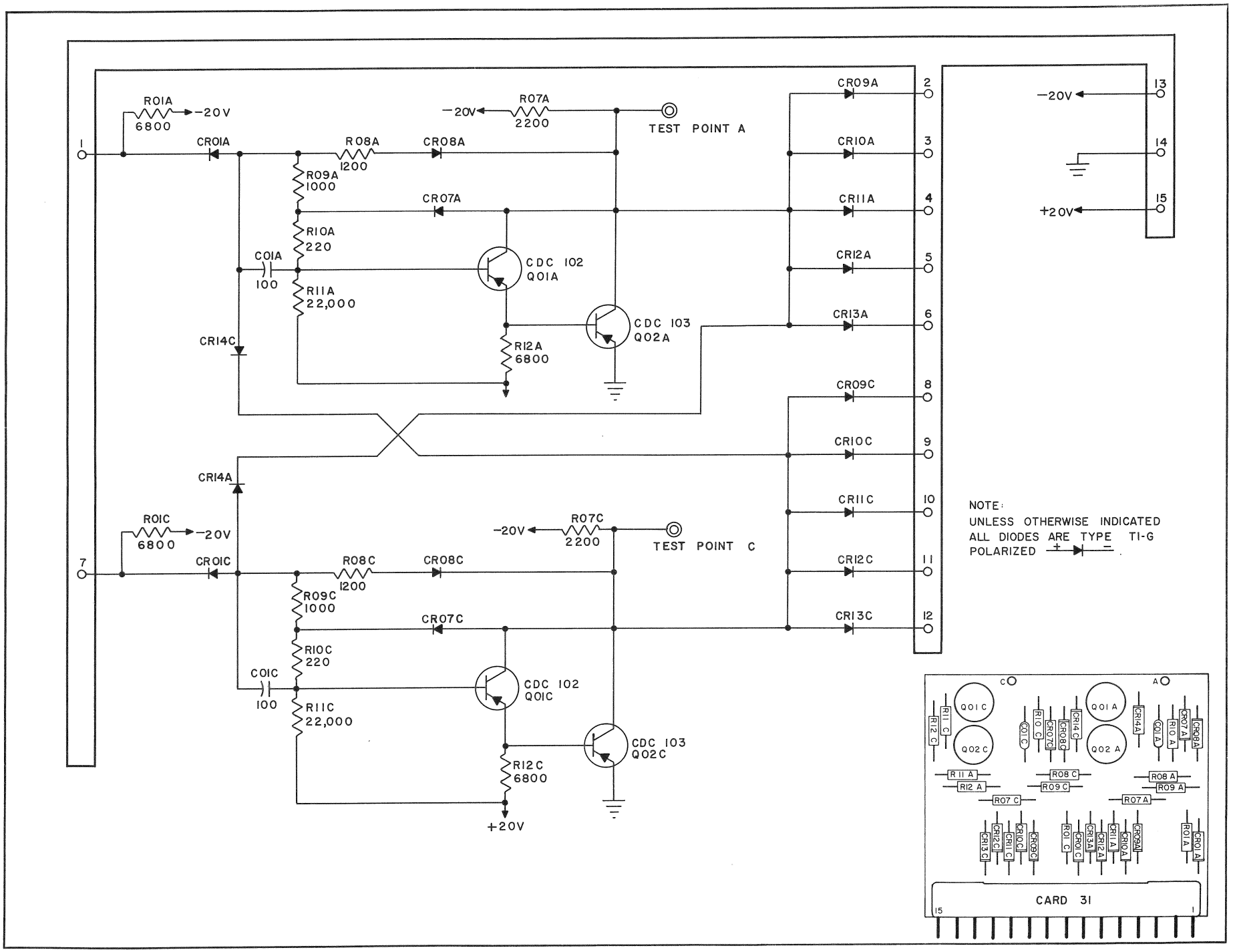


Double Inverter

Double Inverter



Flip-flop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6800
-20V
CR01A
R08A
1200
CR08A
R09A
1000
CR07A
R10A
220
C01A
100
R11A
22,000
CDC 102
Q01A
CDC 103
Q02A
R12A
6800
CR14C
R07A
2200
TEST POINT A
CR09A
CR10A
CR11A
CR12A
CR13A
2
3
4
5
6
13
14
15
+20V
CR09C
CR10C
CR11C
CR12C
CR13C
8
9
10
11
12
CR14A
R01C
6800
CR01C
R08C
1200
CR08C
R09C
1000
CR07C
R10C
220
C01C
100
R11C
22,000
CDC 102
Q01C
CDC 103
Q02C
R12C
6800
+20V
R07C
2200
TEST POINT C
7
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
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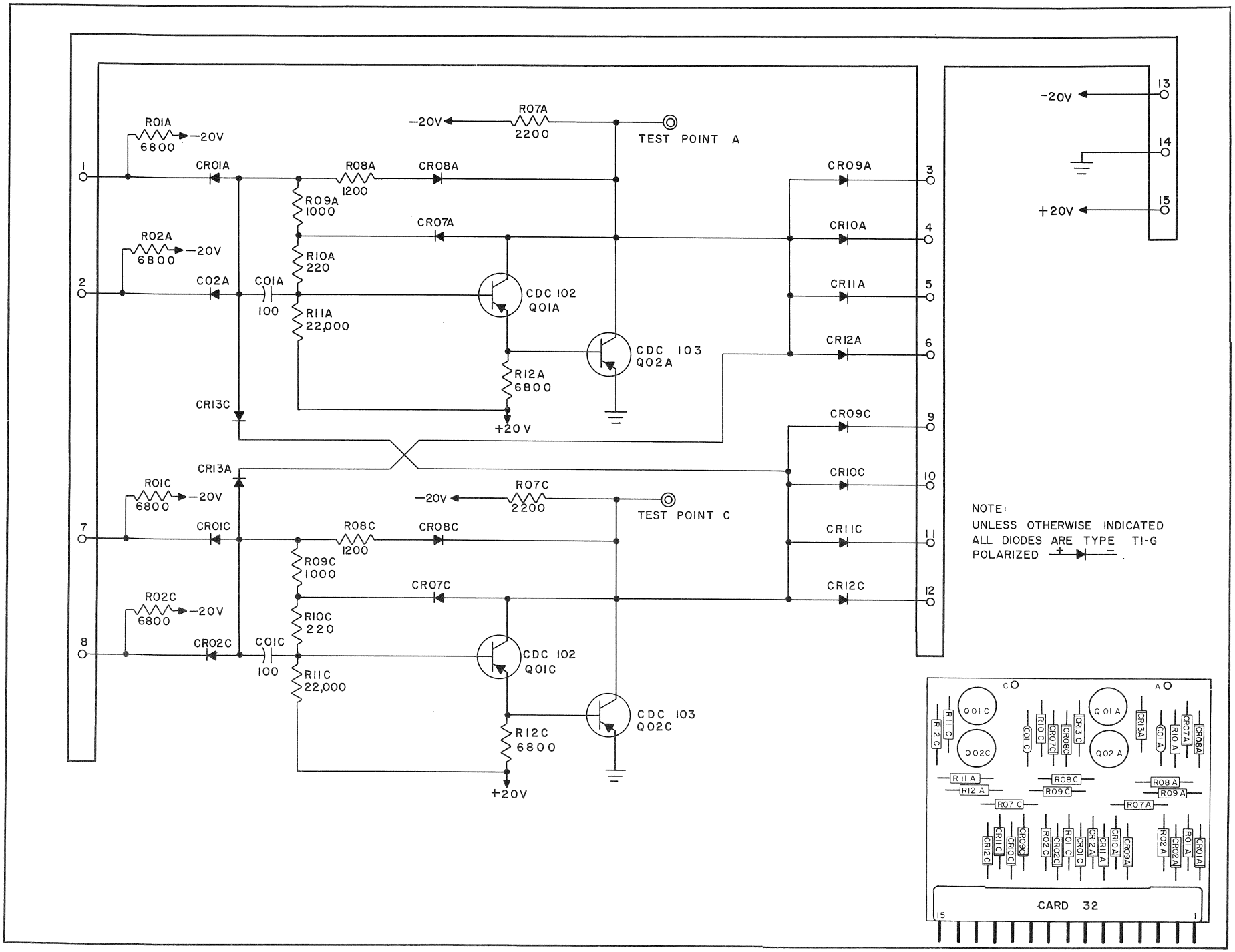
A
Q01C
Q02C
Q01A
Q02A
CARD 31
15
1

Flip-flop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CR01A
R08A
1200
CR08A
R07A
2200
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1000
CR07A
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6800
R10A
220
C02A
C01A
100
R11A
22,000
CDC 102
Q01A
CDC 103
Q02A
R12A
6800
+20V
CR13C
CR13A
R01C
R08C
CR08C
R07C
TEST POINT C
R09C
1000
CR07C
R02C
R10C
220
C02C
C01C
R11C
22,000
CR09A
CR10A
CR11A
CR12A
CR09C
CR10C
CR11C
CR12C
1
2
3
4
5
6
7
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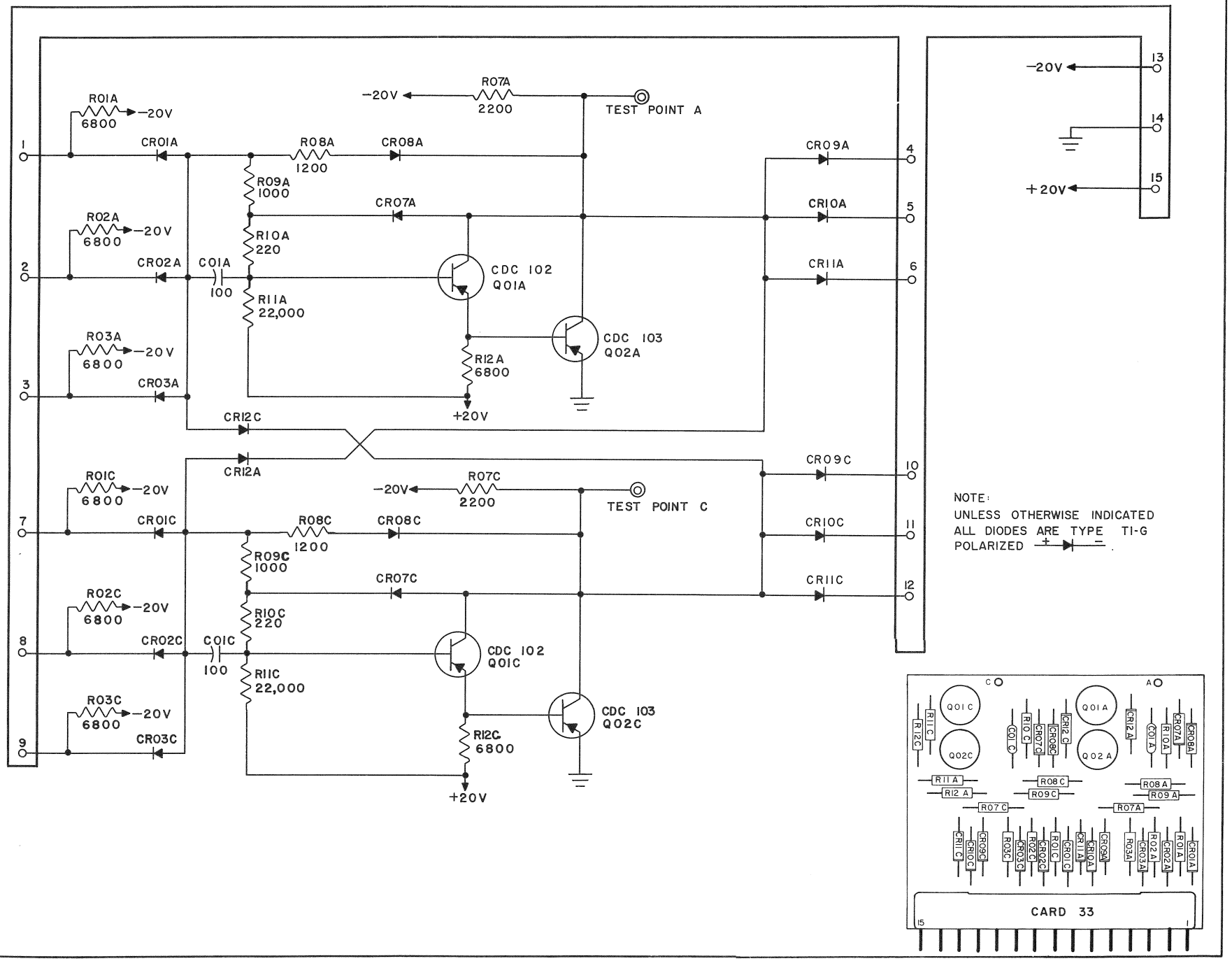
11
12
13
14
15
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
CARD 32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CR01A
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CR08A
R07A
2200
TEST POINT A
R09A
1000
CR07A
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CR10A
CR11A
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C01A
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CDC 103
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R03A
6800
R12A
6800
CR03A
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CR12C
CR12A
CR09C
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R07C
2200
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R08C
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CR08C
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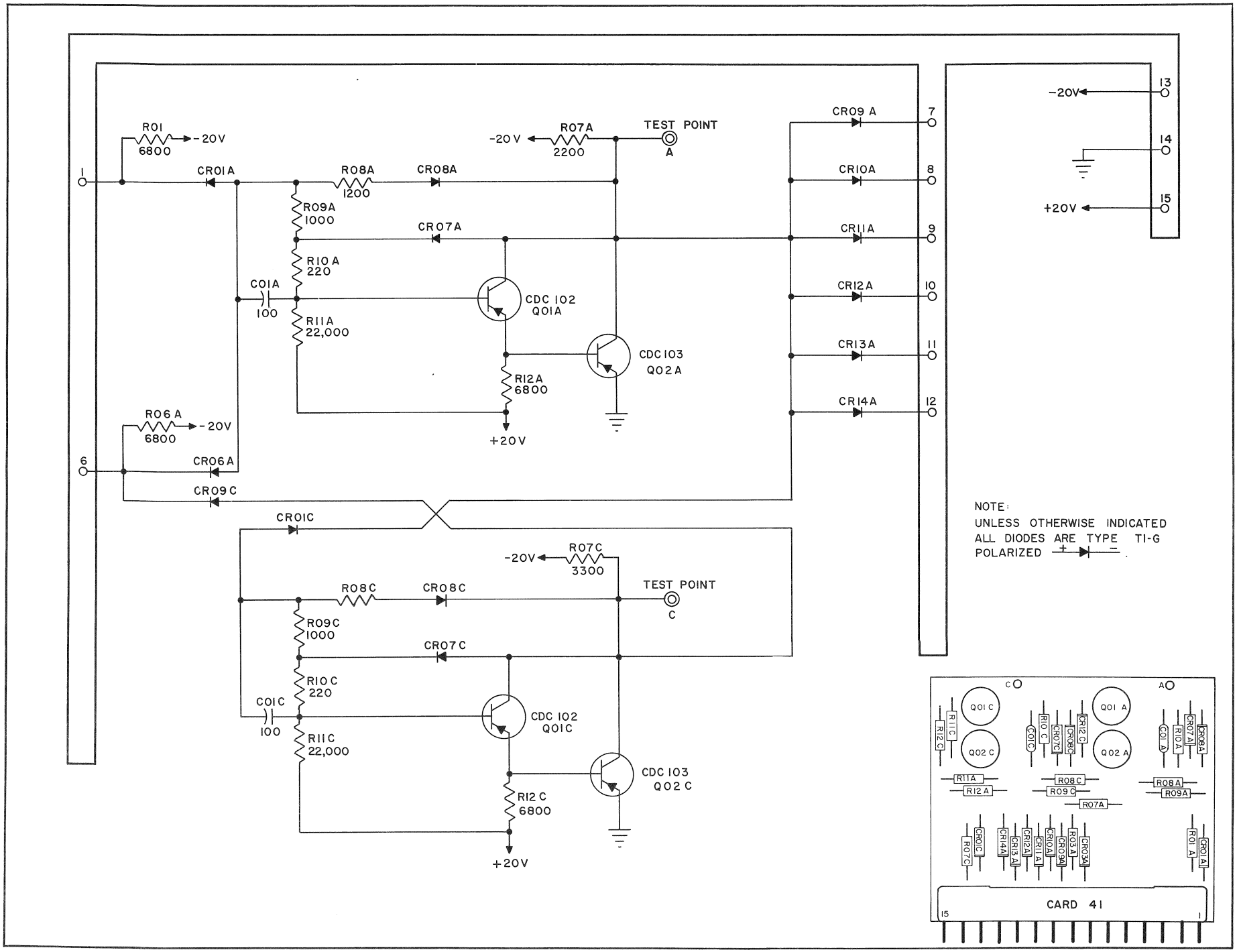
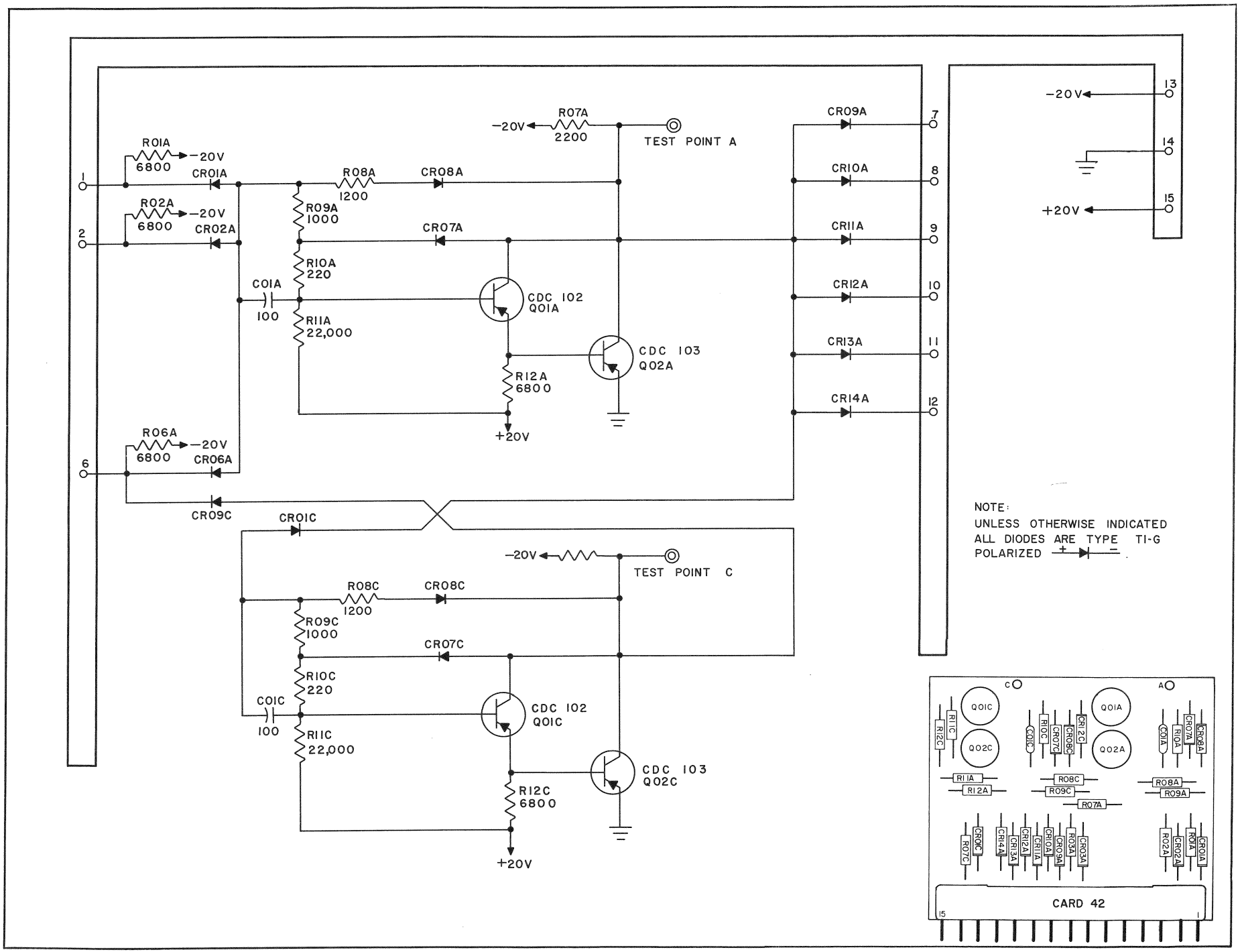
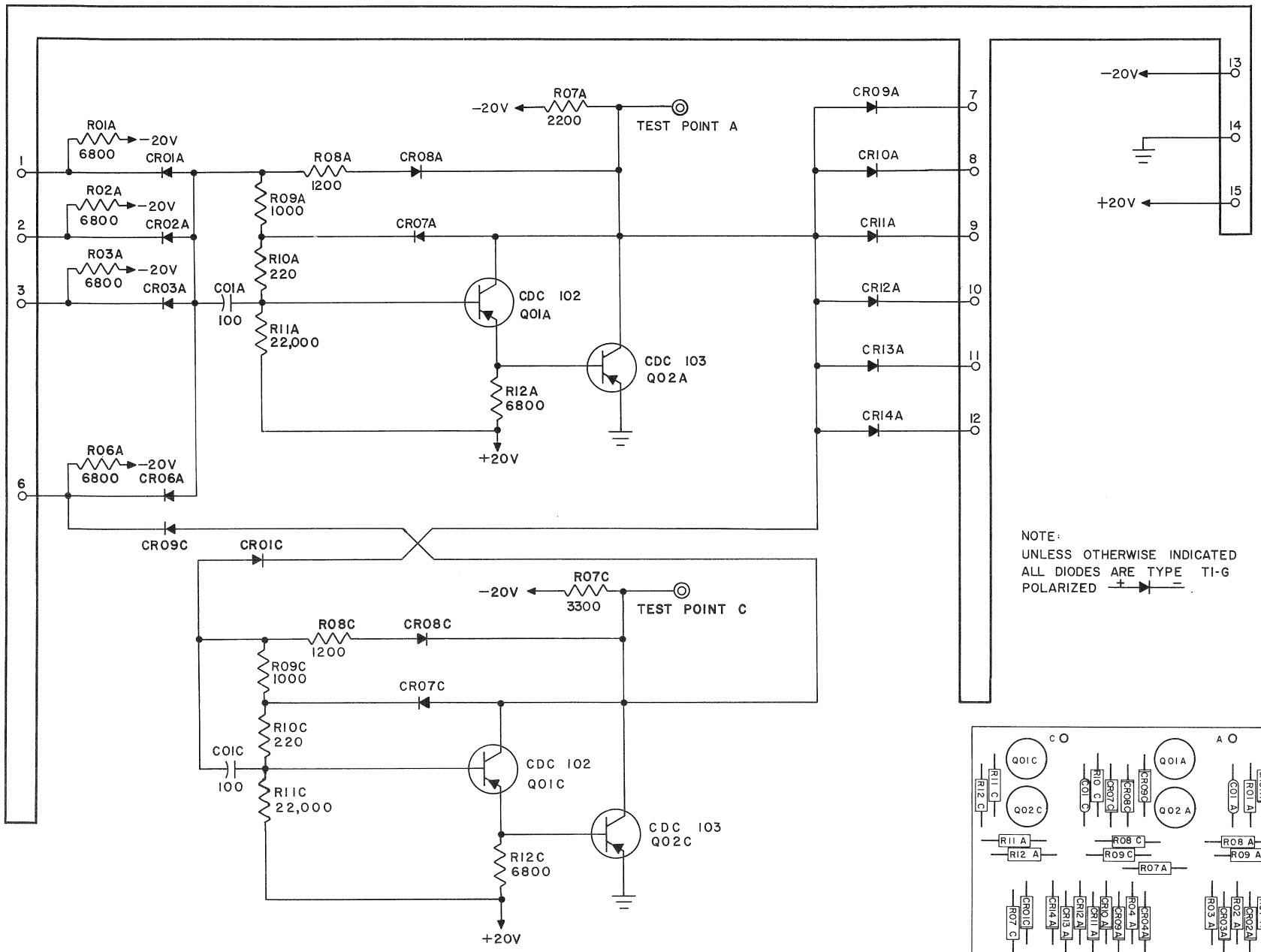
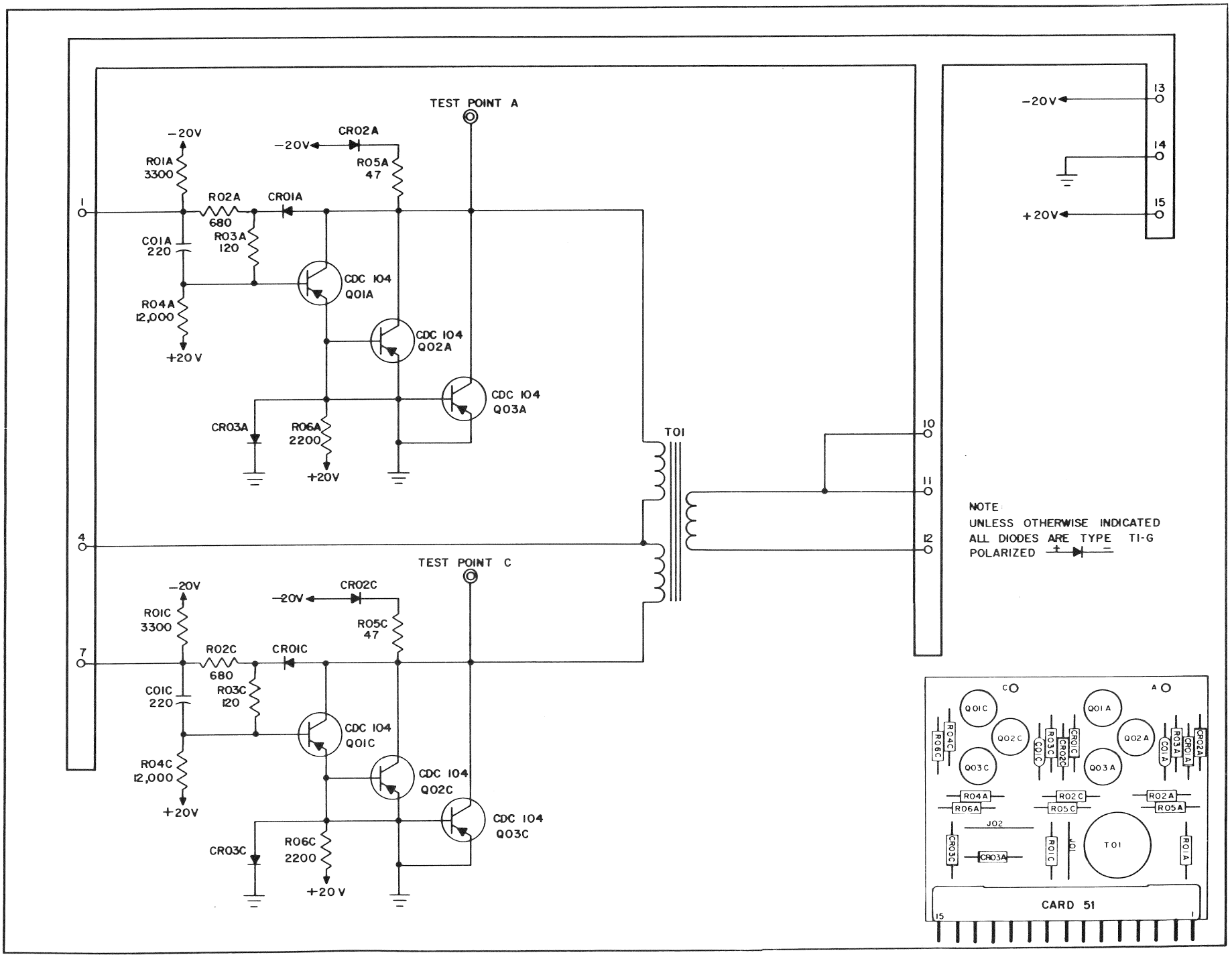
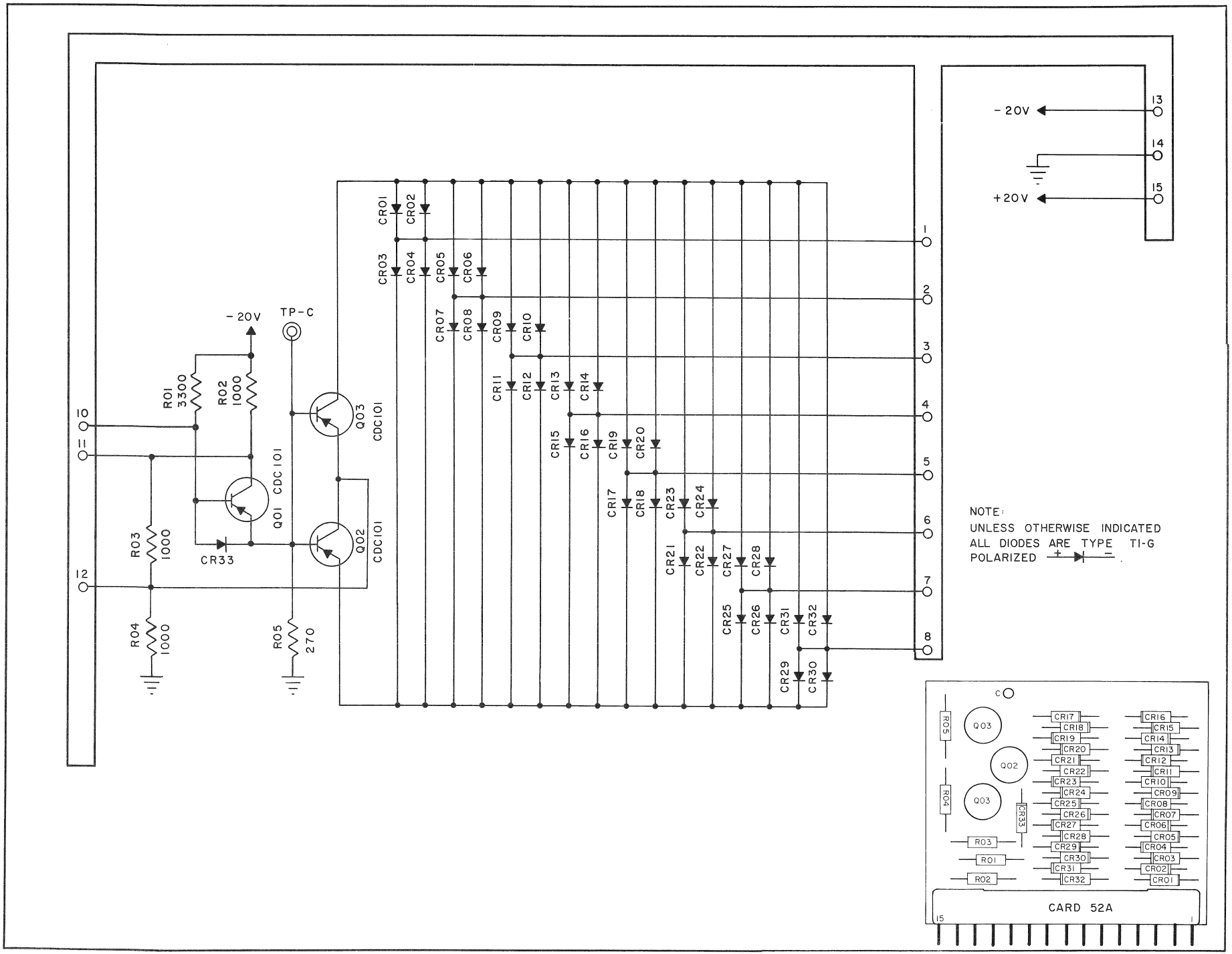
R09C
1000
CR07C
CR11C
R02C
6800
R10C
220
CR02C
C01C
100
CDC 102
Q01C
R11C
22,000
CDC 103
Q02C
R03C
6800
R12C
6800
CR03C
+20V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
-20V
+20V
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
C
A
Q01C
Q02C
Q01A
Q02A
CARD 33
15
1


R01
6800
-20V
CR01A
1
R08A
1200
CR08A
R09A
1000
CR07A
R10A
220
C01A
100
R11A
22,000
CDC 102
Q01A
CDC 103
Q02A
R12A
6800
+20V
-20V
R07A
2200
TEST POINT
A
R06A
6800
-20V
6
CR06A
CR09C
CR01C
-20V
R07C
3300
R08C
CR08C
TEST POINT
C
R09C
1000
CR07C
R10C
220
C01C
100
R11C
22,000
CDC 102
Q01C
CDC 103
Q02C
R12C
6800
+20V
CR09A
7
CR10A
8
CR11A
9
CR12A
10
CR13A
11
CR14A
12
-20V
13
14
+20V
15
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
C
A
Q01C
Q02C
Q01A
Q02A
R11C
R12C
C01C
R10C
CR07C
CR08C
R12C
C01A
R10A
CR07A
CR08A
R11A
R12A
R08C
R09C
R07A
R08A
R09A
R07C
CR01C
CR14A
CR13A
CR12A
CR11A
CR10A
CR09A
CR03A
R01A
CR01A
CARD 41
15
1

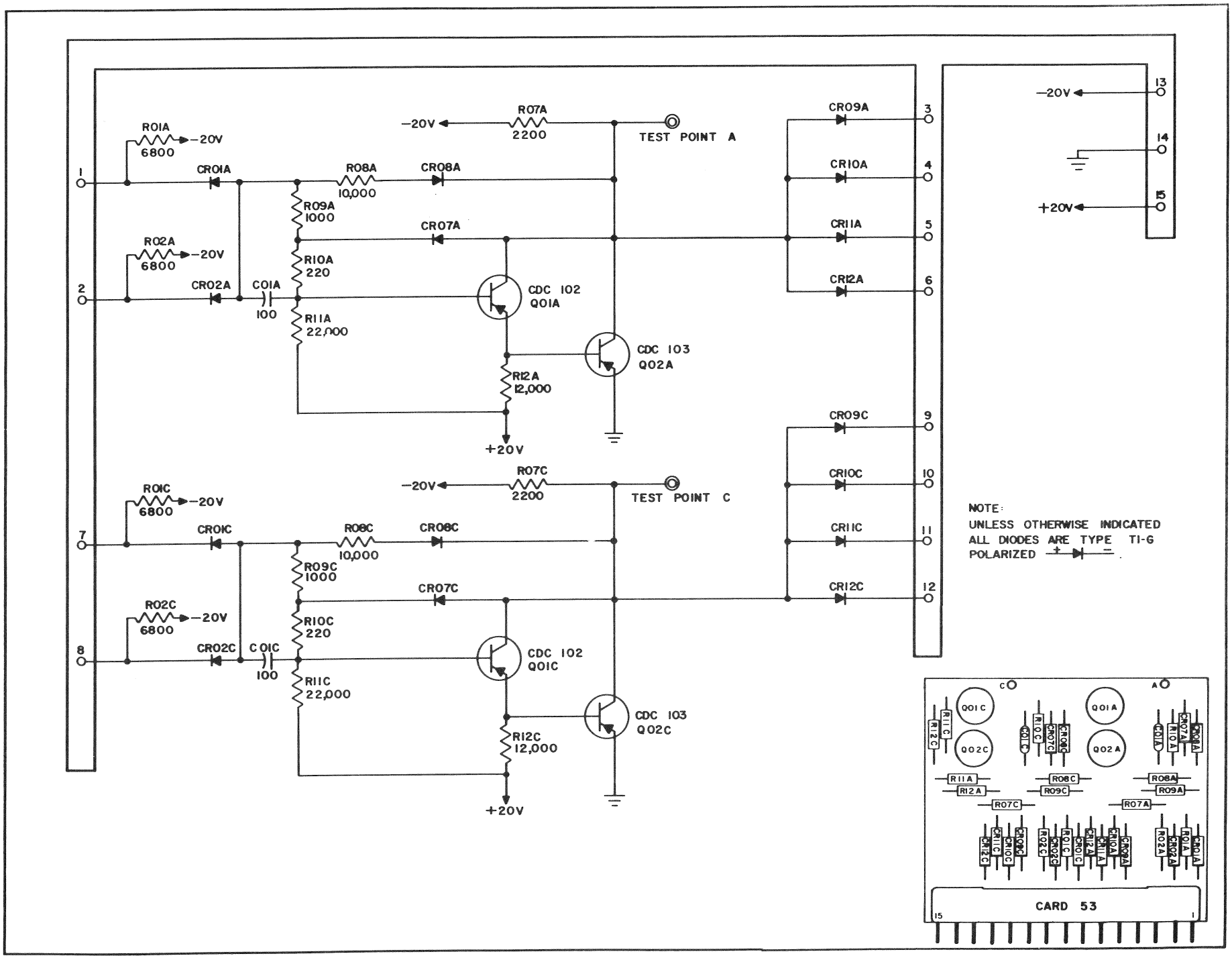

R01A
6800
-20V
CR01A
1
R02A
6800
-20V
CR02A
2
R06A
6800
-20V
CR06A
6
CR09C
R08A
1200
CR08A
R09A
1000
CR07A
R10A
220
C01A
100
R11A
22,000
CDC 102
Q01A
CDC 103
Q02A
R12A
6800
+20V
R07A
2200
-20V
TEST POINT A
CR09A
CR10A
CR11A
CR12A
CR13A
CR14A
7
8
9
10
11
12
13
14
15
-20V
+20V
CR01C
-20V
TEST POINT C
R08C
1200
CR08C
R09C
1000
CR07C
R10C
220
C01C
100
R11C
22,000
CDC 102
Q01C
CDC 103
Q02C
R12C
6800
+20V
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
C
A
Q01C
Q02C
Q01A
Q02A
CARD 42
15

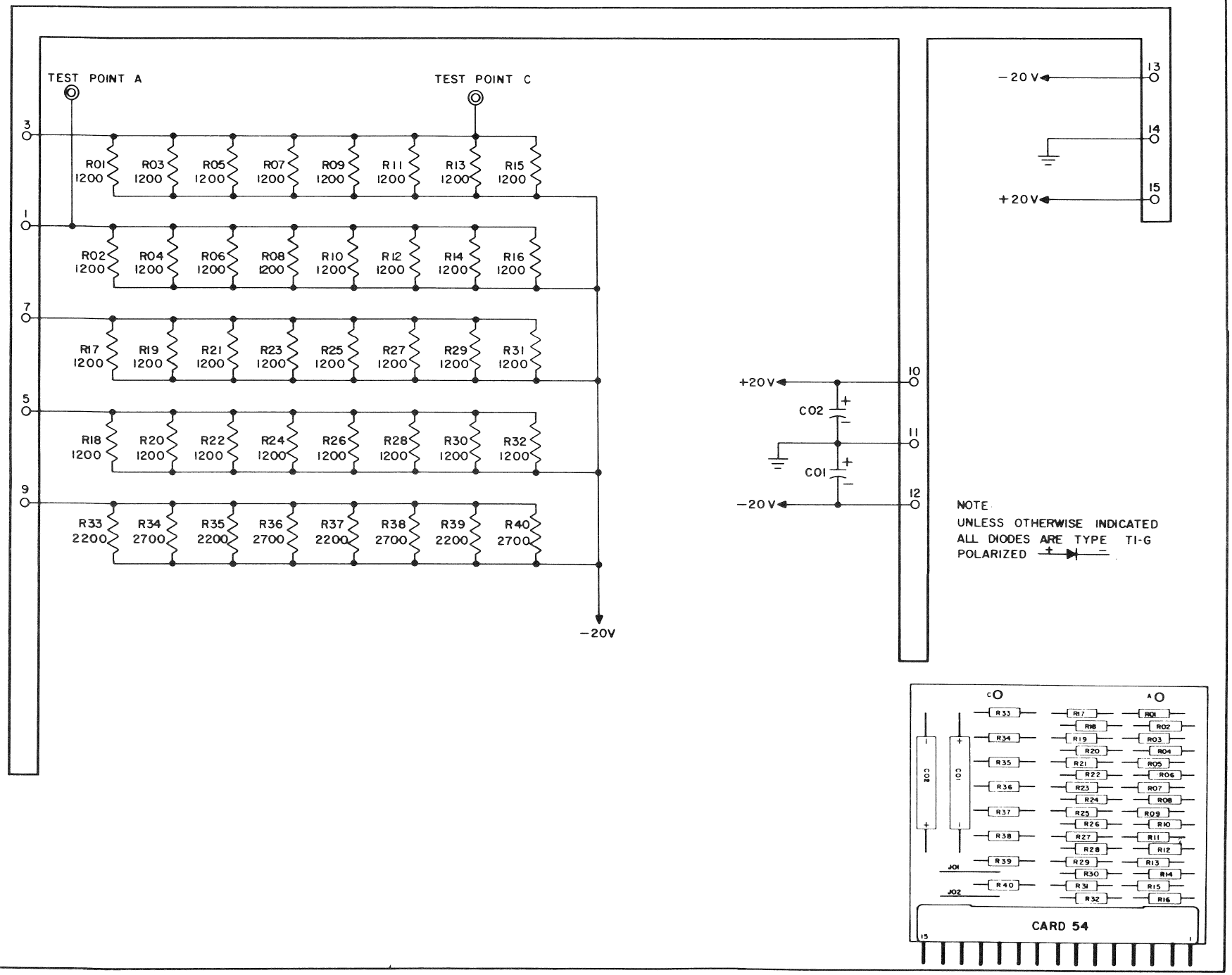

R01A
6800
-20V
CR01A
R02A
6800
-20V
CR02A
R03A
6800
-20V
CR03A
R06A
6800
-20V
CR06A
C01A
100
R09A
1000
R08A
1200
CR08A
R07A
2200
-20V
TEST POINT A
CR07A
R10A
220
R11A
22,000
CDC 102
Q01A
CDC 103
Q02A
R12A
6800
+20V
CR09A
CR10A
CR11A
CR12A
CR13A
CR14A
CR09C
CR01C
R07C
3300
-20V
TEST POINT C
R08C
1200
CR08C
R09C
1000
CR07C
R10C
220
C01C
100
R11C
22,000
CDC 102
Q01C
CDC 103
Q02C
R12C
6800
+20V
-20V
+20V
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
CARD 43

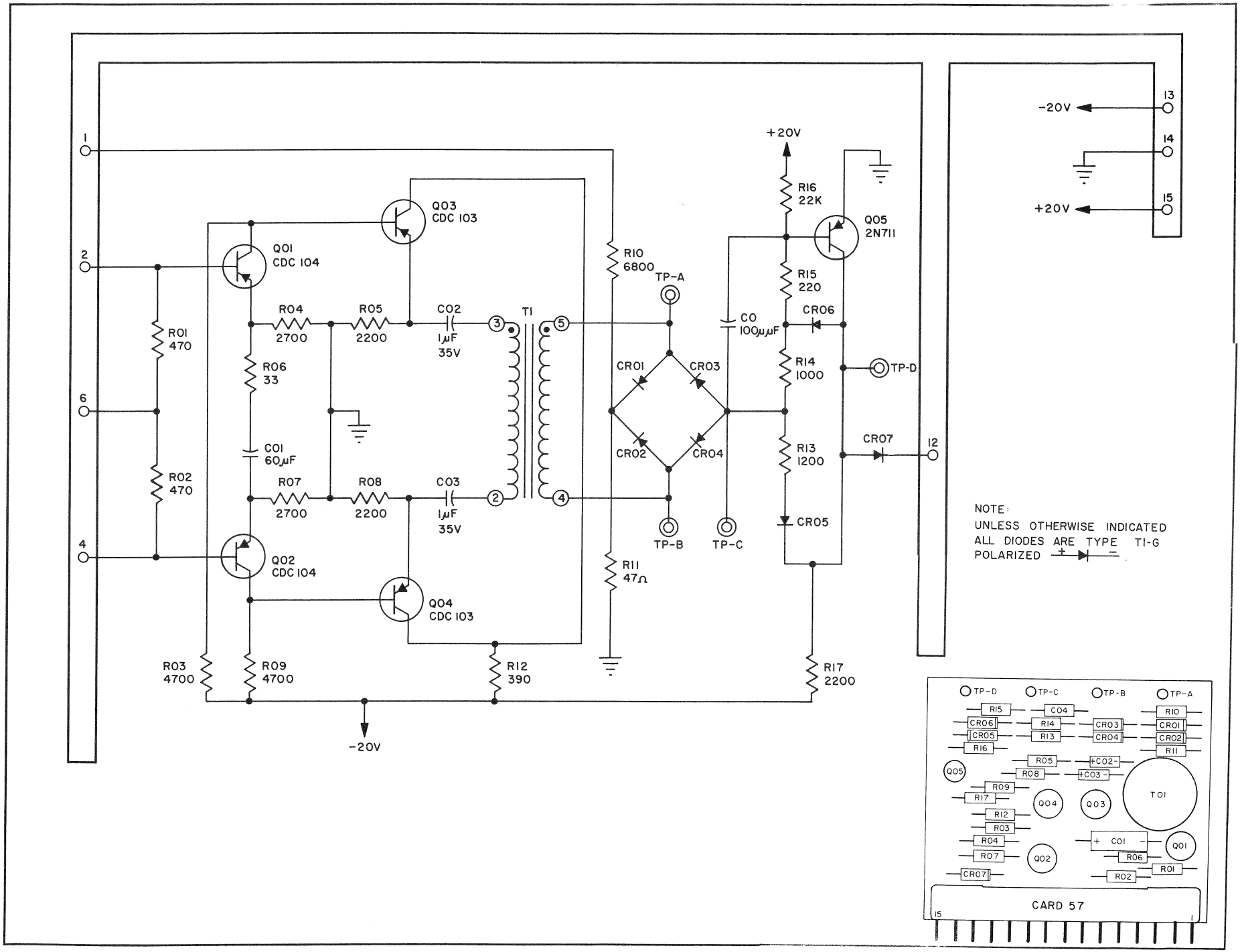

TEST POINT A
-20V
CR02A
R01A 3300
R05A 47
R02A 680
CR01A
C01A 220
R03A 120
CDC 104 Q01A
CDC 104 Q02A
CDC 104 Q03A
R04A 12,000
+20V
CR03A
R06A 2200
T01
1
4
7
10
11
12
13
14
15
TEST POINT C
R01C 3300
CR02C
R05C 47
R02C 680
CR01C
C01C 220
R03C 120
R04C 12,000
R06C 2200
CR03C
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
CARD 51

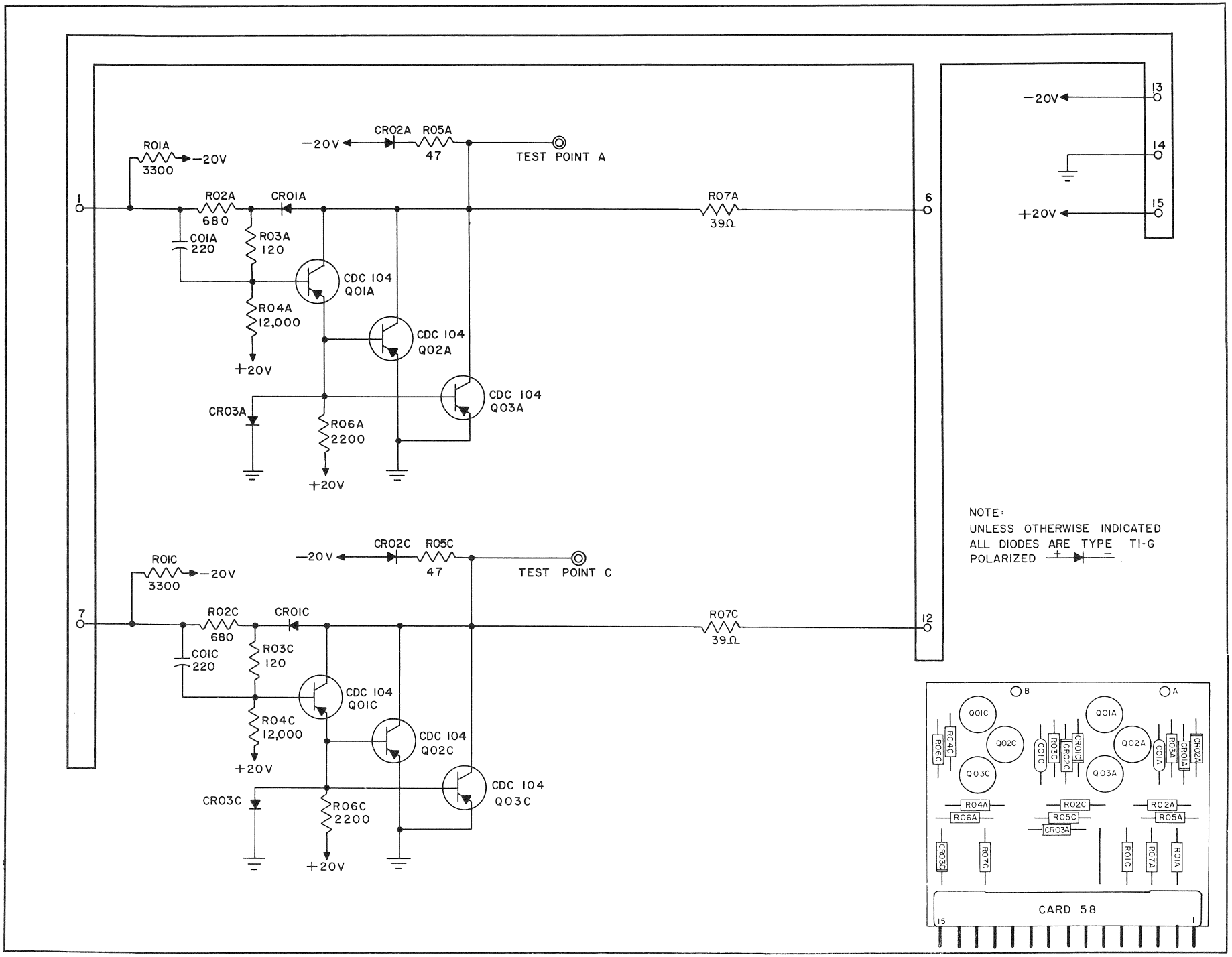

- 20V
TP-C
R01 3300
R02 1000
R03 1000
R04 1000
R05 270
Q01 CDC101
Q02 CDC101
Q03 CDC101
CR33
CR01 CR02 CR03 CR04 CR05 CR06 CR07 CR08 CR09 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR19 CR20 CR17 CR18 CR23 CR24 CR21 CR22 CR27 CR28 CR25 CR26 CR31 CR32 CR29 CR30
10
11
12
1
2
3
4
5
6
7
8
- 20V
+ 20V
13
14
15
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
C
Q03
Q02
Q03
R05
R04
R03
R01
R02
CR33
CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR30 CR31 CR32
CR16 CR15 CR14 CR13 CR12 CR11 CR10 CR09 CR08 CR07 CR06 CR05 CR04 CR03 CR02 CR01
CARD 52A
15
1

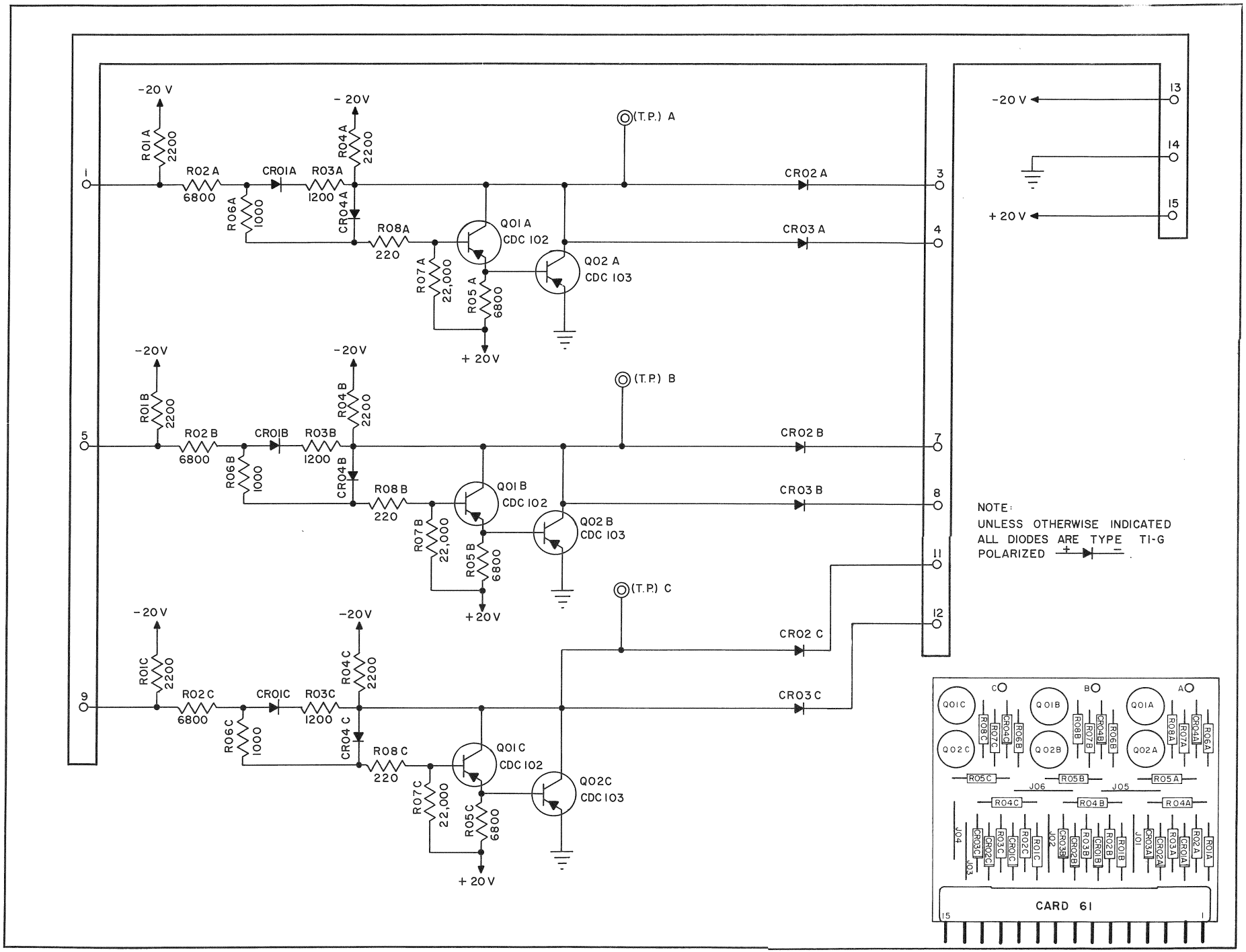
Diverter

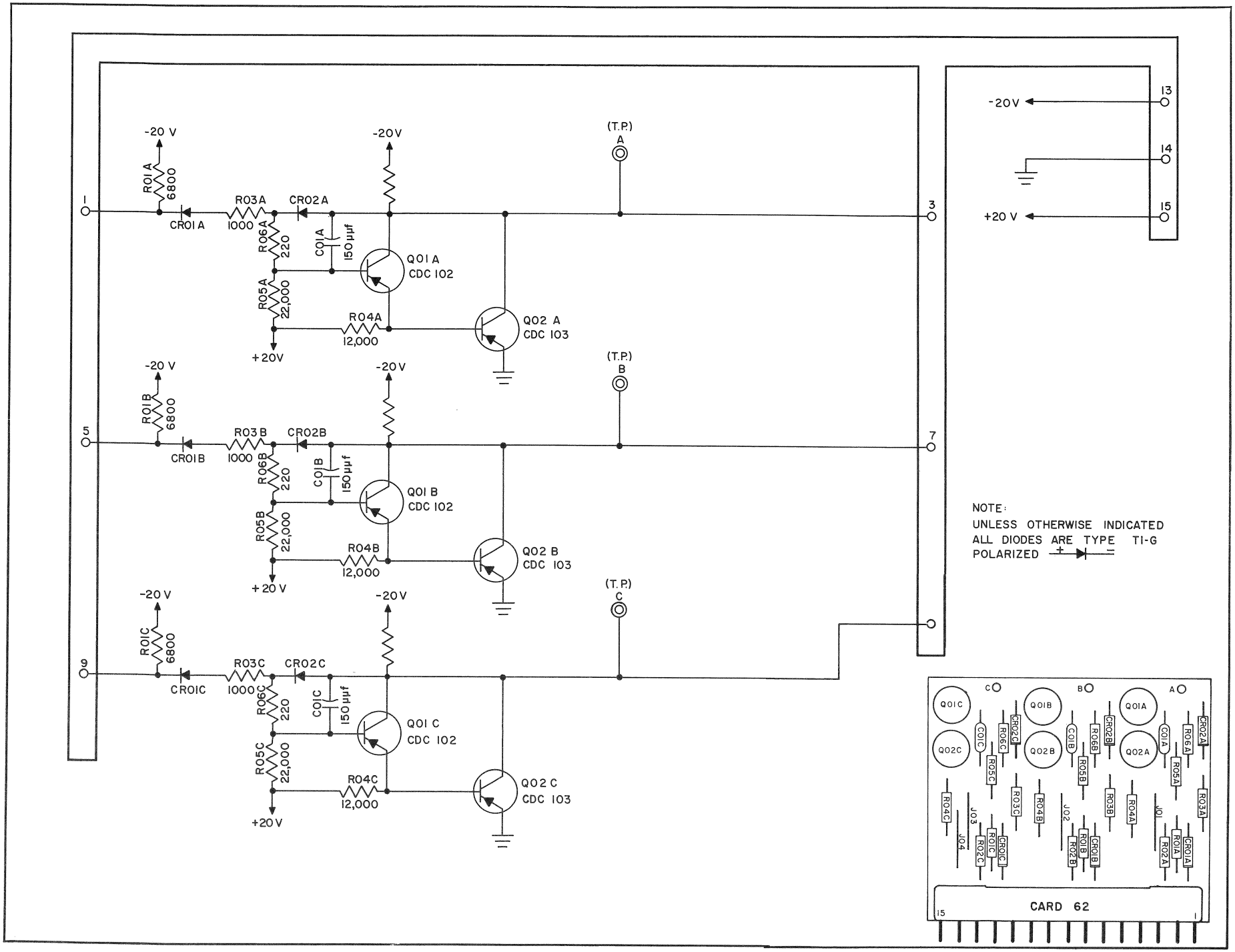

R01A
6800
-20V
CR01A
R08A
10,000
CR08A
R09A
1000
R07A
2200
TEST POINT A
CR09A
CR10A
CR11A
CR12A
R02A
6800
CR02A
C01A
100
R10A
220
R11A
22,000
CDC 102
Q01A
CDC 103
Q02A
R12A
12,000
+20V
R01C
6800
CR01C
R08C
10,000
CR08C
R09C
1000
R07C
2200
TEST POINT C
CR09C
CR10C
CR11C
CR12C
R02C
6800
CR02C
C01C
100
R10C
220
R11C
22,000
CDC 102
Q01C
CDC 103
Q02C
R12C
12,000
+20V
-20V
+20V
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
CARD 53


TEST POINT A
TEST POINT C
3
1
7
5
9
R01 1200
R03 1200
R05 1200
R07 1200
R09 1200
R11 1200
R13 1200
R15 1200
R02 1200
R04 1200
R06 1200
R08 1200
R10 1200
R12 1200
R14 1200
R16 1200
R17 1200
R19 1200
R21 1200
R23 1200
R25 1200
R27 1200
R29 1200
R31 1200
R18 1200
R20 1200
R22 1200
R24 1200
R26 1200
R28 1200
R30 1200
R32 1200
R33 2200
R34 2700
R35 2200
R36 2700
R37 2200
R38 2700
R39 2200
R40 2700
-20V
+20V
C02
C01
-20V
10
11
12
-20V
+20V
13
14
15
NOTE
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
C
A
C02
C01
J01
J02
CARD 54
15
1

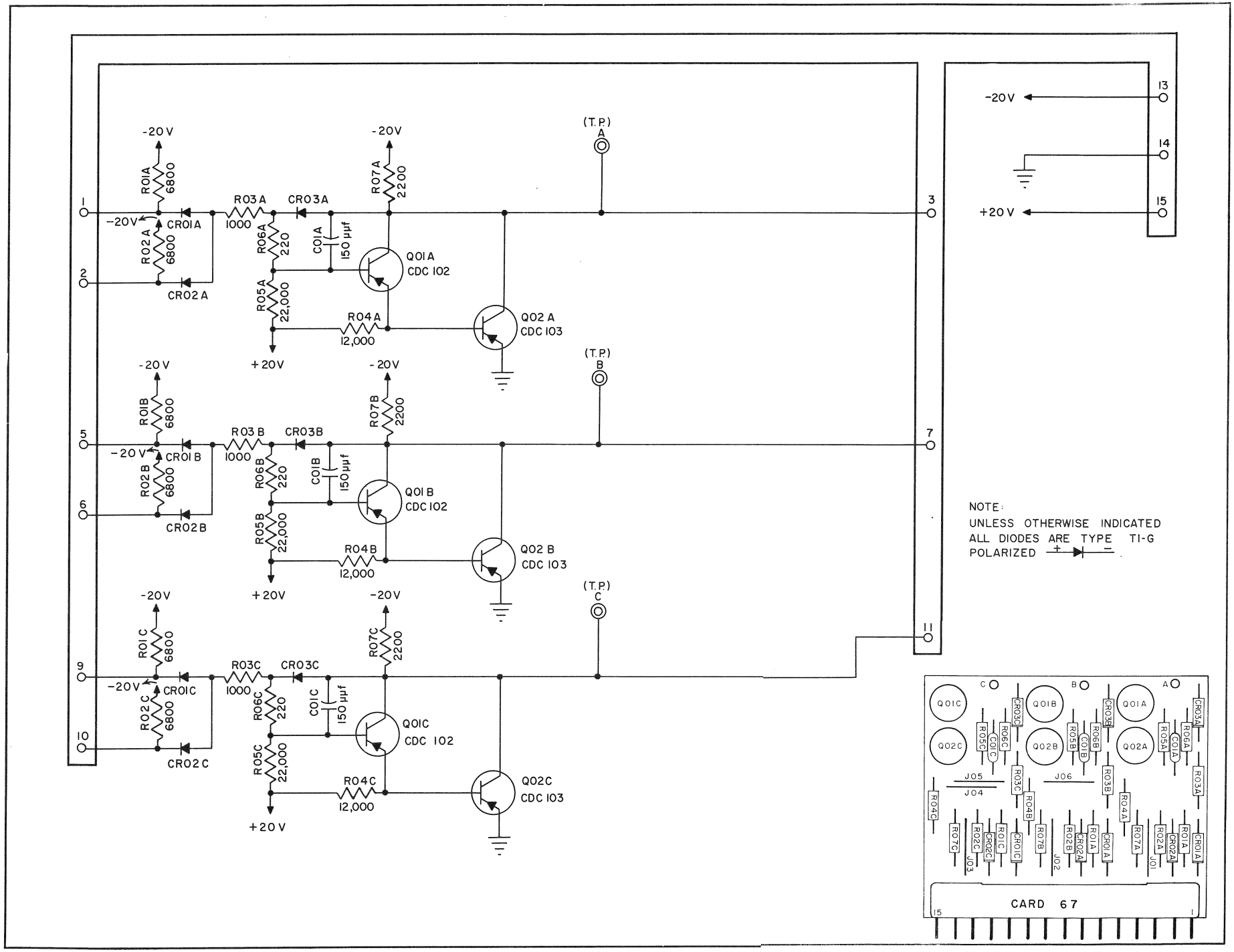

1
2
6
4
Q03
CDC 103
Q01
CDC 104
R01
470
R04
2700
R05
2200
C02
1μF
35V
T1
R06
33
C01
60μF
R02
470
R07
2700
R08
2200
C03
1μF
35V
Q02
CDC 104
Q04
CDC 103
R03
4700
R09
4700
R12
390
-20V
R10
6800
TP-A
TP-B
TP-C
CR01
CR03
CR02
CR04
+20V
R16
22K
Q05
2N711
R15
220
C0
100μμF
CR06
R14
1000
TP-D
R13
1200
CR07
CR05
12
R11
47Ω
R17
2200
-20V
13
14
15
+20V
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
TP-D
TP-C
TP-B
TP-A
R15
C04
R10
CR06
R14
CR03
CR01
CR05
R13
CR04
CR02
R16
R11
R05
+C02-
Q05
R08
+C03-
R09
R17
T01
Q04
Q03
R12
R03
R04
+ C01 -
Q01
R07
Q02
R06
CR07
R01
R02
CARD 57
15

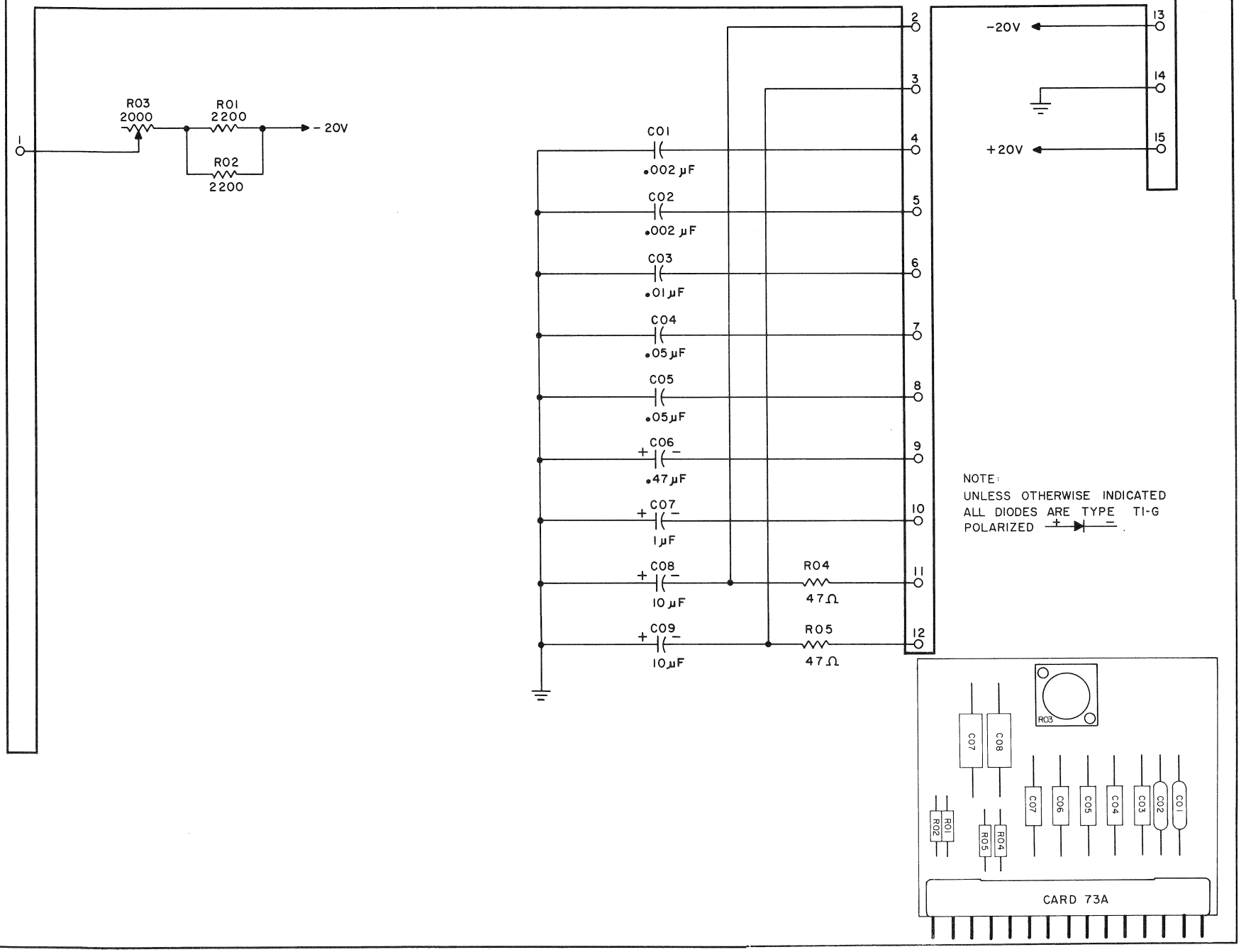

R01A
3300
−20V
CR02A
R05A
47
−20V
TEST POINT A
1
R02A
680
CR01A
R07A
39Ω
6
C01A
220
R03A
120
CDC 104
Q01A
R04A
12,000
+20V
CDC 104
Q02A
CDC 104
Q03A
CR03A
R06A
2200
+20V
13
−20V
14
15
+20V
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
R01C
3300
−20V
CR02C
R05C
47
−20V
TEST POINT C
7
R02C
680
CR01C
R07C
39Ω
12
C01C
220
R03C
120
CDC 104
Q01C
R04C
12,000
+20V
CDC 104
Q02C
CDC 104
Q03C
CR03C
R06C
2200
+20V
B
A
Q01C
Q02C
Q03C
Q01A
Q02A
Q03A
R04C
R06C
C01C
R03C
CR02C
CR01C
C01A
R03A
CR01A
CR02A
R04A
R06A
R02C
R05C
CR03A
R02A
R05A
CR03C
R07C
R01C
R07A
R01A
CARD 58
15
1

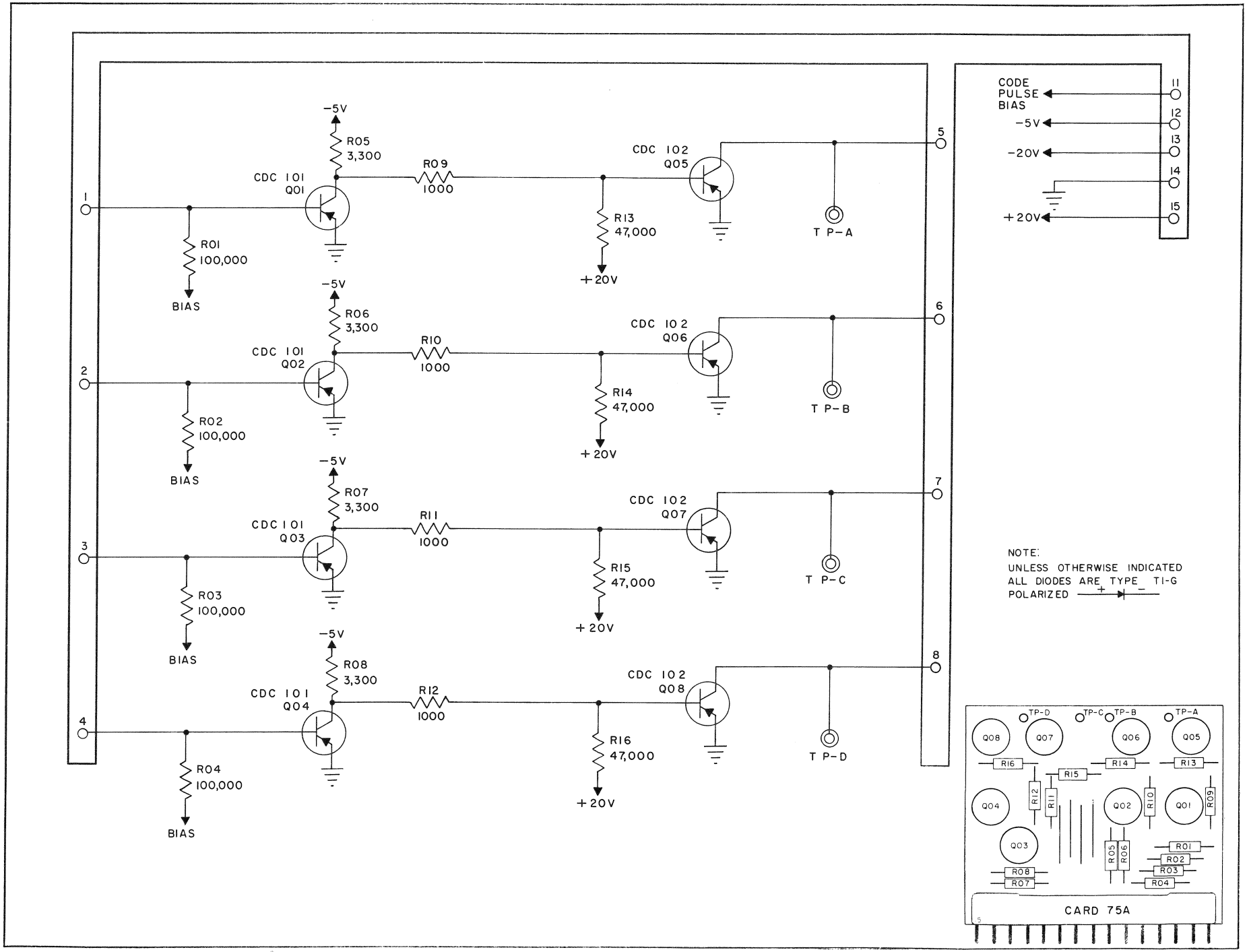

-20 V
R01A 2200
R02A 6800
R06A 1000
CR01A
R03A 1200
-20V
R04A 2200
CR04A
R08A 220
R07A 22,000
R05A 6800
+ 20V
(T.P.) A
Q01A CDC 102
Q02A CDC 103
CR02A
CR03A
1
3
4
5
R01B 2200
R02B 6800
R06B 1000
CR01B
R03B 1200
R04B 2200
CR04B
R08B 220
R07B 22,000
R05B 6800
(T.P) B
Q01B CDC 102
Q02B CDC 103
CR02B
CR03B
7
8
9
R01C 2200
R02C 6800
R06C 1000
CR01C
R03C 1200
R04C 2200
CR04C
R08C 220
R07C 22,000
R05C 6800
(T.P) C
Q01C CDC 102
Q02C CDC 103
CR02C
CR03C
11
12
13
14
15
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
CARD 61

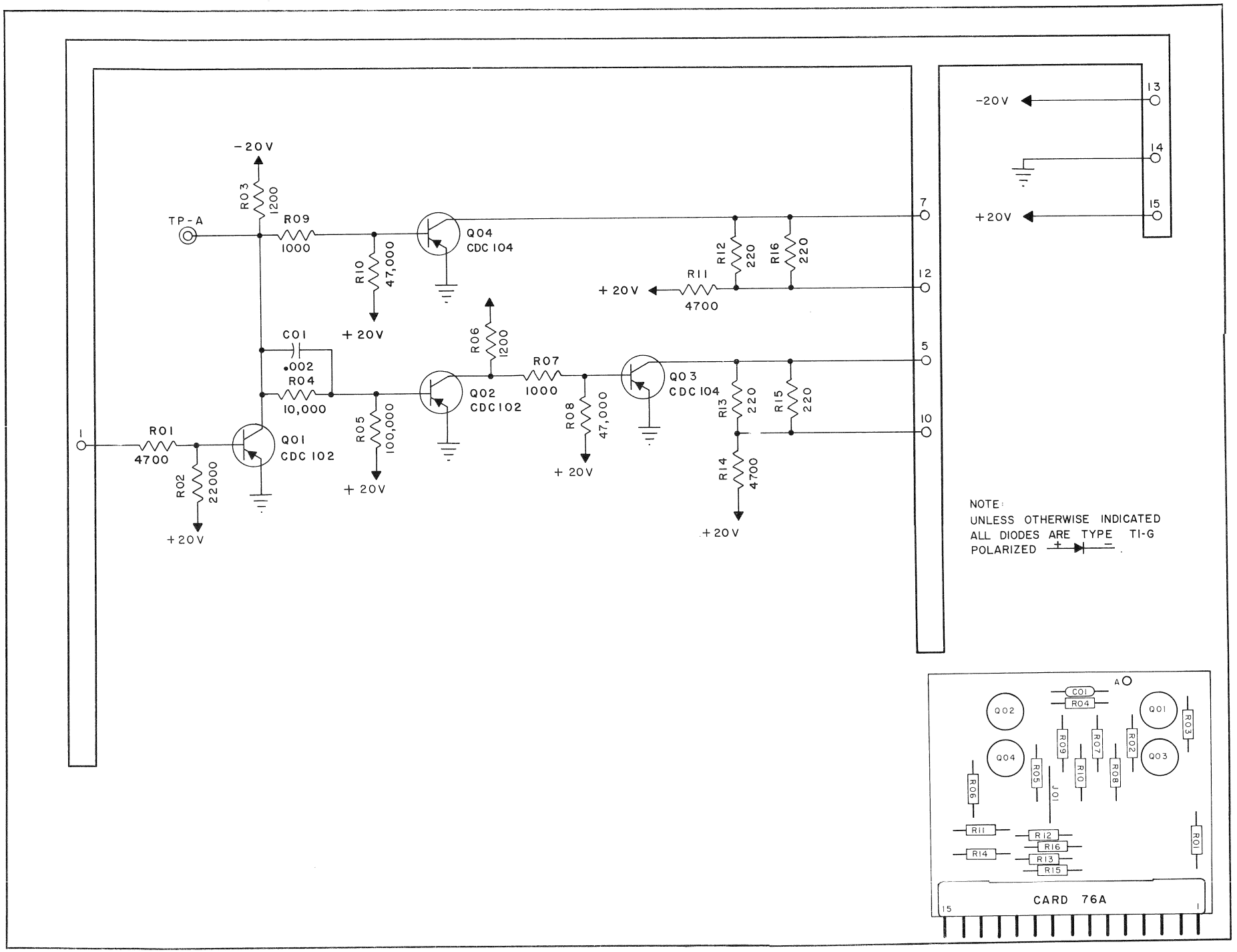


Output Amplifier

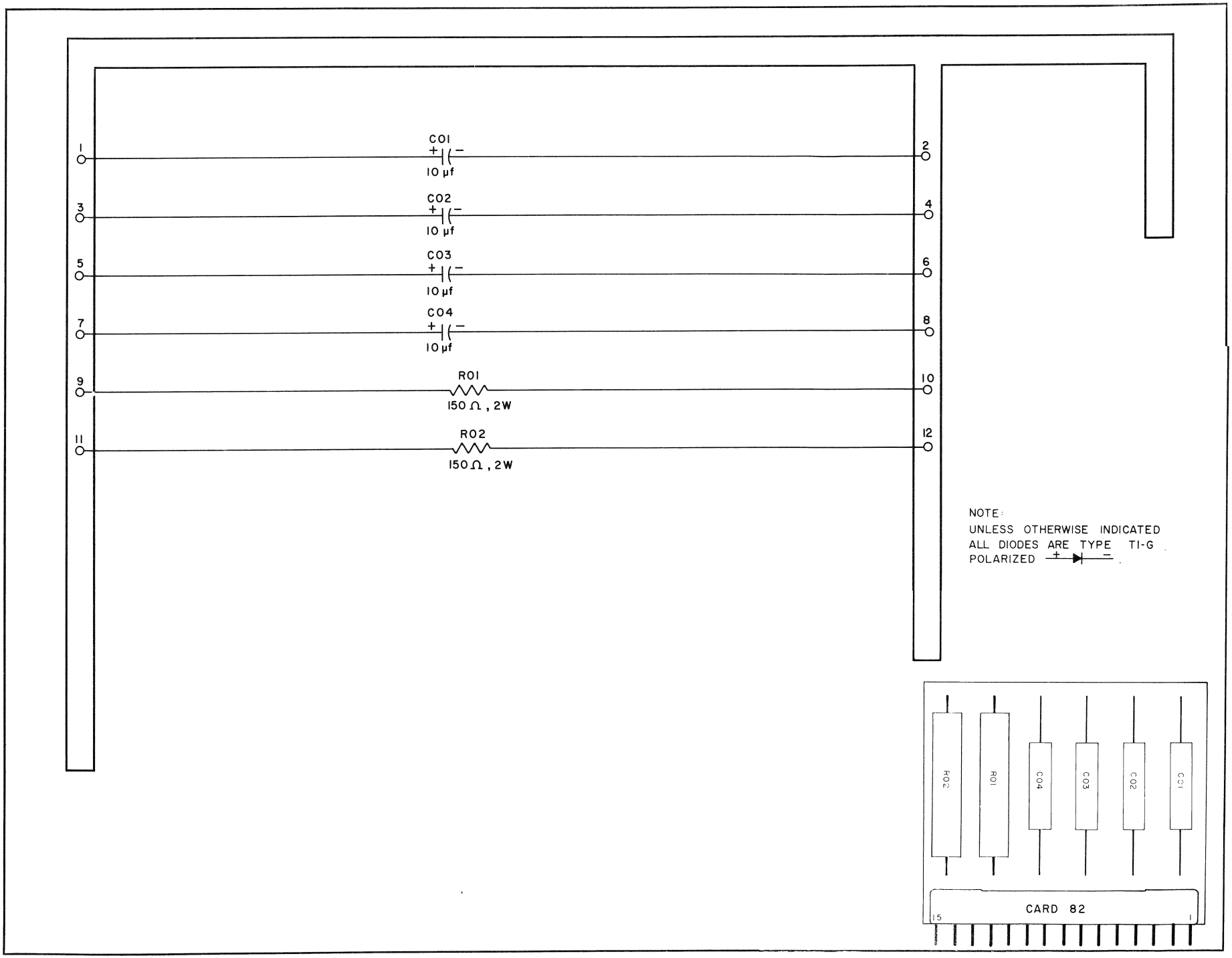

-20 V
+20 V
(T.P.) A
(T.P.) B
(T.P.) C
R01A 6800
R02A 6800
CR01A
CR02A
R03A 1000
CR03A
R06A 220
C01A 150 µµf
R05A 22,000
R04A 12,000
R07A 2200
Q01A CDC 102
Q02A CDC 103
R01B 6800
R02B 6800
CR01B
CR02B
R03B 1000
CR03B
R06B 220
C01B 150 µµf
R05B 22,000
R04B 12,000
R07B 2200
Q01B CDC 102
Q02B CDC 103
R01C 6800
R02C 6800
CR01C
CR02C
R03C 1000
CR03C
R06C 220
C01C 150 µµf
R05C 22,000
R04C 12,000
R07C 2200
Q01C CDC 102
Q02C CDC 103
1
2
3
5
6
7
9
10
11
13
14
15
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
CARD 67
J01
J02
J03
J04
J05
J06


R03
2000
R01
2200
- 20V
R02
2200
C01
.002 µF
C02
.002 µF
C03
.01 µF
C04
.05 µF
C05
.05 µF
C06
.47 µF
C07
1 µF
C08
10 µF
C09
10 µF
R04
47Ω
R05
47Ω
-20V
+20V
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
CARD 73A

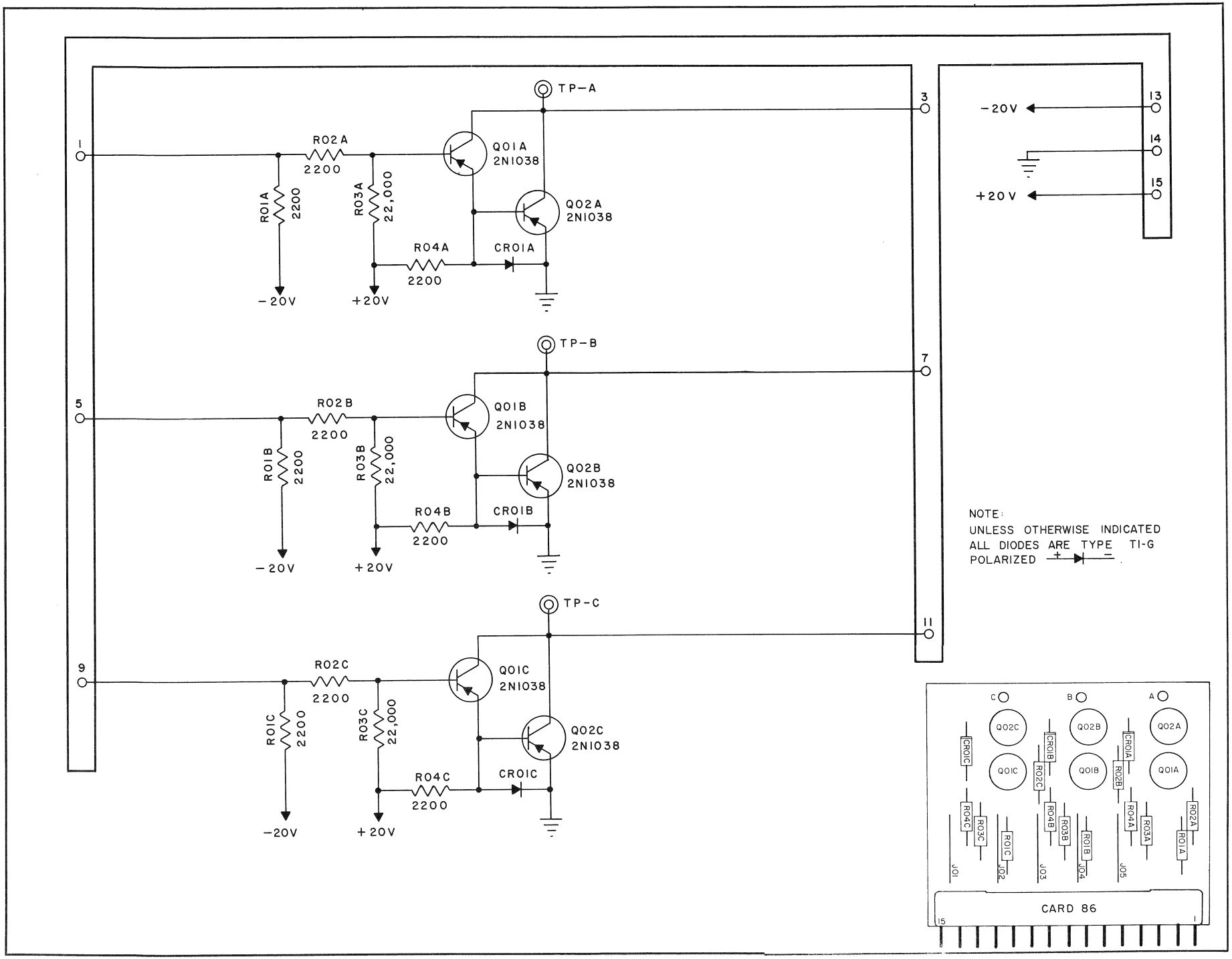

CODE PULSE BIAS
-5V
-20V
+20V
11
12
13
14
15
-5V
R05 3,300
CDC 101 Q01
R09 1000
CDC 102 Q05
R13 47,000
+20V
T P-A
R01 100,000
BIAS
-5V
R06 3,300
CDC 101 Q02
R10 1000
CDC 102 Q06
R14 47,000
+20V
T P-B
R02 100,000
BIAS
-5V
R07 3,300
CDC 101 Q03
R11 1000
CDC 102 Q07
R15 47,000
+20V
T P-C
R03 100,000
BIAS
-5V
R08 3,300
CDC 101 Q04
R12 1000
CDC 102 Q08
R16 47,000
+20V
T P-D
R04 100,000
BIAS
1
2
3
4
5
6
7
8
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
TP-D
TP-C
TP-B
TP-A
Q08
Q07
Q06
Q05
R16
R15
R14
R13
Q04
R12
R11
Q02
R10
Q01
R09
Q03
R05
R06
R01
R02
R03
R08
R07
R04
CARD 75A



Brake-Clutch (reader)


1
2
C01
+
−
10 µf
3
4
C02
+
−
10 µf
5
6
C03
+
−
10 µf
7
8
C04
+
−
10 µf
9
10
R01
150 Ω , 2W
11
12
R02
150 Ω , 2W
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
+
−
R02
R01
C04
C03
C02
C01
CARD 82
15
1

Filter


TP-A
TP-B
TP-C
R02A
2200
R01A
2200
R03A
22,000
R04A
2200
CR01A
Q01A
2N1038
Q02A
2N1038
R02B
2200
R01B
2200
R03B
22,000
R04B
2200
CR01B
Q01B
2N1038
Q02B
2N1038
R02C
2200
R01C
2200
R03C
22,000
R04C
2200
CR01C
Q01C
2N1038
Q02C
2N1038
-20V
+20V
3
5
7
9
11
13
14
15
-20V
+20V
NOTE:
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED
CARD 86
J01
J02
J03
J04
J05

APPENDIX F
INSTALLATION

The Control Data 160 computer system is designed to be used with a minimum of environmental restrictions. This manual, which will be furnished to the customer well in advance of shipment of the computer system, provides electrical and physical information to aid in the preparation of a suitable site for the system. Detailed data on equipment sizes, power requirements and cables are also included. For information concerning other than the more common equipments consult Control Data Corporation.

A Control Data Corporation engineer accompanies the system to the site and supervises the installation. General requirements for the system are reviewed at the time of installation and any modifications to the cabling system are resolved.

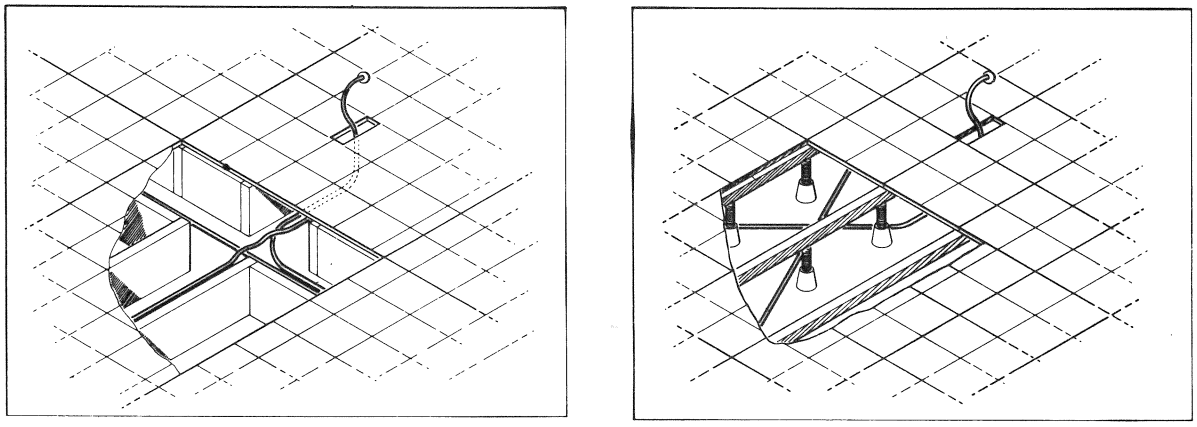
GENERAL REQUIREMENTS

FLOOR

Connecting cables in the computer system enter the cabinets through openings in the bottom. Raceways may be built into the floor, or cable troughs may be laid on top of the floor (optional with customer). If raceways are used, cables are protected from damage and may be routed without restriction (figure 1).

TEMPERATURE

Blowers or fans at the bottom of the cabinets cool the equipment by room air pulled through reuseable air filters and forced to circulate up through the cabinet and out



A. False Floor - Raceway Type

B. False Floor - Pedestal Type

Figure 1. False Floors

through louvres at the rear or top. The system operates in a normal room air environment not exceeding 80°F. Heat generated by the equipment should be quickly removed from the vicinity of the cabinets by circulation of the room air. The additional heat load (table 1) caused by the equipment can be dissipated through increased air conditioning capacity.

A low humidity limit of 40% will protect against static build up on magnetic tape; a high limit of 60% will protect punched card operation and prevent harm to acetate magnetic tape.

AREA CLEANLINESS

Clean the computer site regularly to avoid dust accumulation. Dust and cigarette ashes in the immediate vicinity of the tape handlers may collect on the magnetic tape and cause errors in operation. Avoid smoking when handling magnetic tapes.

FIRE PRECAUTIONS

Locate fire extinguishing equipment near the system; observe normal fire precautions.

SPACE AND LAYOUT REQUIREMENTS

The position of the equipment cabinets will be partially determined by the size and shape of the area available for the computer installation. In general, the operator seated at the computer should be able to view the tape handlers and other equipment with moving parts. Cabinets should be arranged to permit ease of access both for the operator and for maintenance personnel and their equipment.

Installation information, including dimensions and door swings, are given for each equipment on figure 2, 3 and 5. Dimensions and weights are summarized in table 1 and table 2 gives connector information.

The magnetic tape system may be either bolted to the floor or supplied with special stabilizing bars for added stability.

As an aid to planning, templets of the various equipments may be cut from figure 4 at the back of this manual. The templets are scaled 1/4 inch to one foot. There should be a three-foot clearance surrounding each piece of equipment to allow for free movement of personnel and test equipment.

POWER REQUIREMENTS

The power service facilities for the computer system are supplied by the customer and should be installed prior to arrival of the system. Exceptions are those items specifically noted to be supplied and installed by Control Data Corporation at the time of installation.

POWER SERVICE

The primary power requirement consists of 115 volt, 60 cycle single phase. Current requirements are listed in table 1. A typical 60 cps system uses normal convenience outlets in the computer area for the computer and typewriter (161) unit. Magnetic tape handlers (either 163 or 164) require special heavy-duty wiring. At the customer's option, this single phase power may be derived from one leg of a 3 phase, y connected source.

CABLES

The information cables which connect the various elements in the computer system will be delivered at the time of installation. All information cables are identical except for length. Total cable length should not exceed 75 feet. Prior to delivery, the customer can determine the length of the cables by referring to his equipment layout plan and if the total length of the cables exceeds 75 feet revisions can be made. The cable designations in table 2 are for the purpose of identification. Detailed cable makeup and interconnection data are found in the maintenance volume.

At the time the customer submits the final equipment configuration, Control Data Corporation should be advised of any unusual cabling requirements or obstructions beneath the floor that will interfere with the cables. This should be done no later than two months prior to shipment.

All cables in the system are supplied by Control Data Corporation at the time of delivery. Standard cable lengths are 15 feet and 25 feet. Any unusual lengths may be purchased from Control Data Corporation or supplied independently by the buyer.

Cables supplying power to the cabinets originate at the breaker panel where they are permanently installed. Sufficient spare cable should be allowed to accommodate minor changes in location of the equipment. The power cable should not exceed 100 feet in length.

TABLE 1. SPECIFICATION OF THE 160 COMPUTER SYSTEM

	160 Computer	161 Typewriter	163 Tape Unit Each	164 Tape Unit Each
WIDTH	61 5/8"	29 1/2"	26 5/8"	26 5/8"
DEPTH	30"	30"	27 1/2"	27 1/2"
HEIGHT	36"	37 1/2"	68"	68"
WEIGHT	760#	350#	690#	690#
BTU/HR	5900	2300	9500 (1)	5500 (2)
60 CYCLE POWER REQUIREMENTS				
115v	22A (3)	15A (3)	30A (3) (handler) 15A (control panel)	20A (3) (handler) 15A (control panel)

(1) Add 6500 BTU/Hr for each additional tape unit

(2) Add 2500 BTU/Hr for each additional tape unit.

(3) Maximum line current, including 8A for convenience outlets.

TABLE 2. CABLE CONNECTIONS, INPUT-OUTPUT EQUIPMENT

Type Designation	160 jack	161 jack	163-164 jack
Input Cable	1J09	1J06	J101
		1J07	J102
Output Cable	1J11	1J04	J103
		1J05	J104

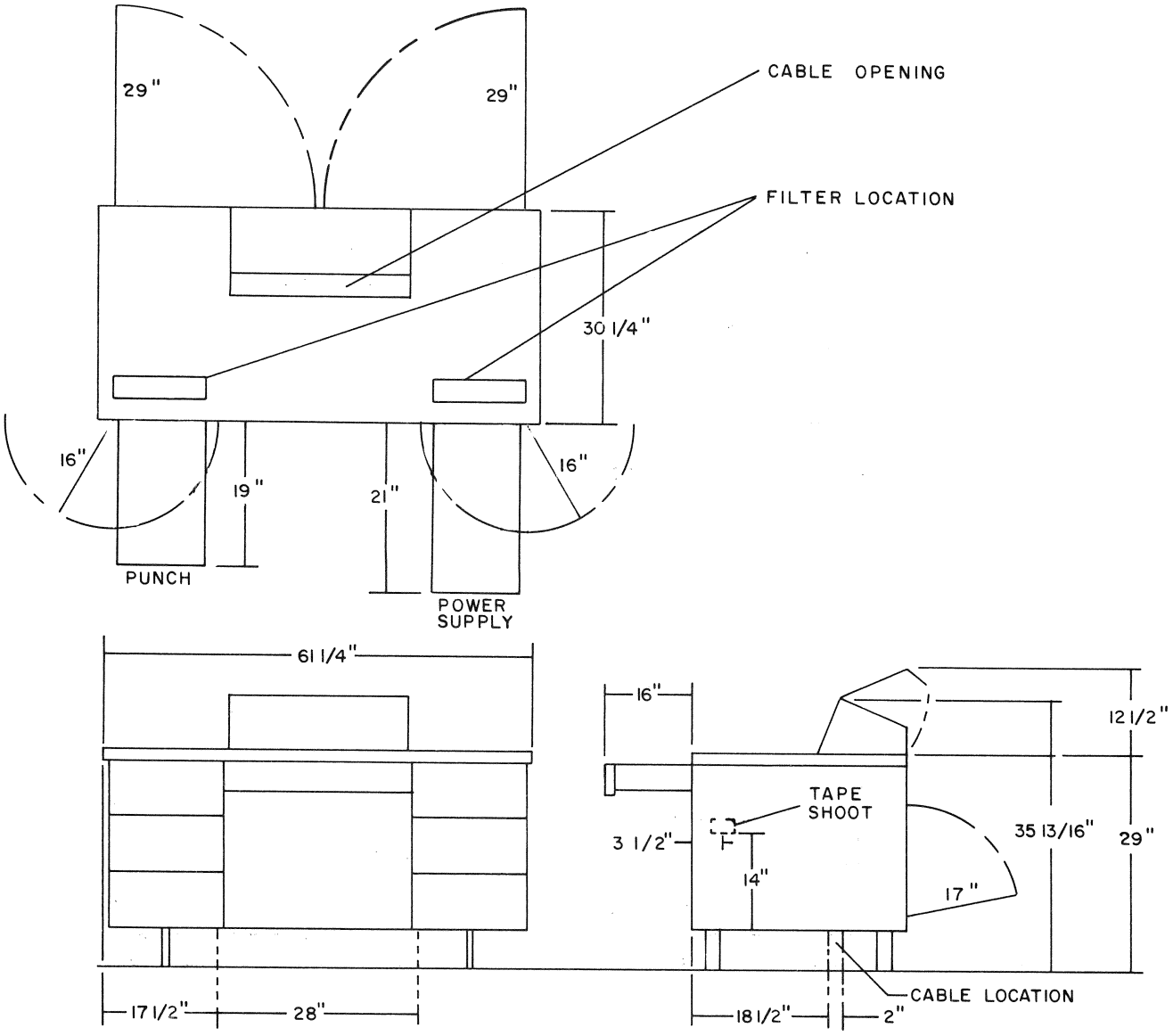


Figure 2. 160 Computer

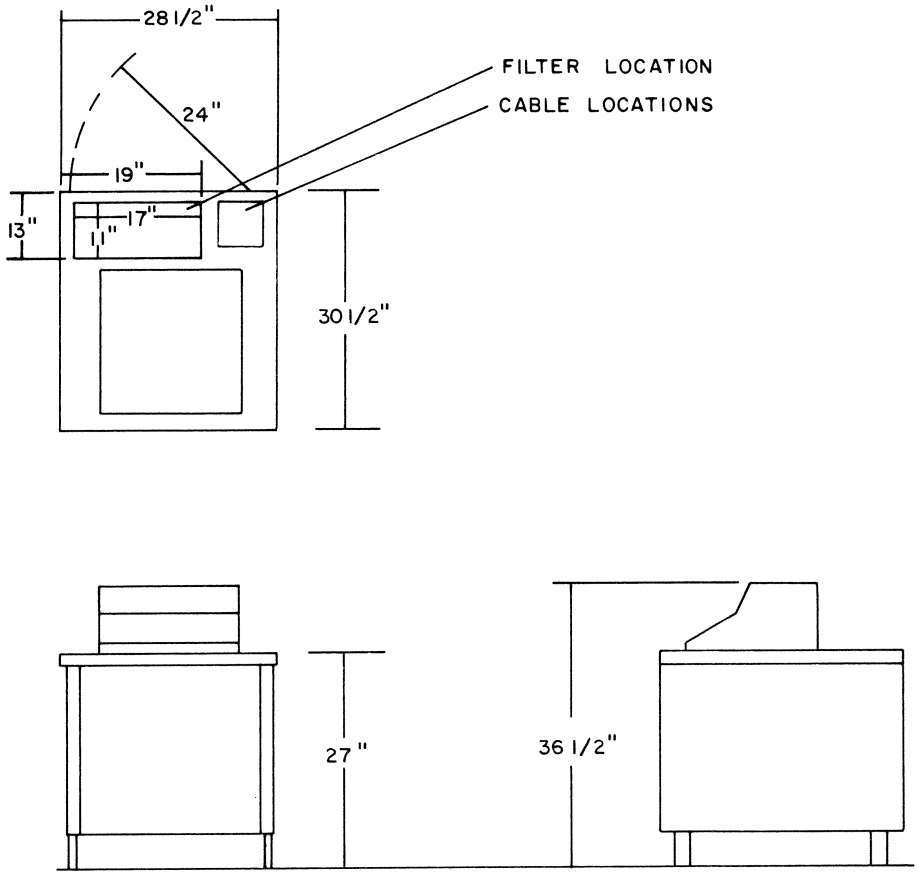


Figure 3. 161 Typewriter Unit

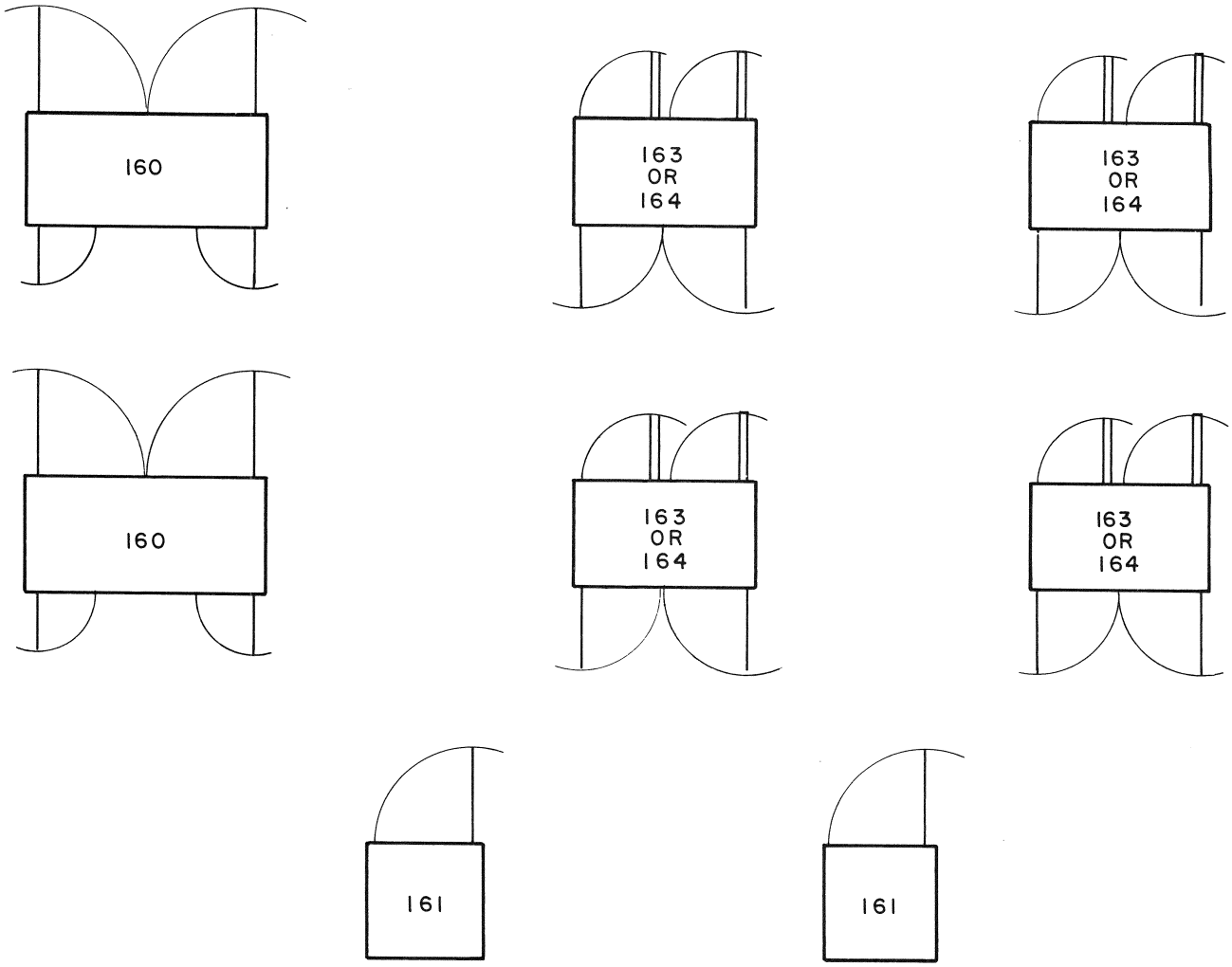


Figure 4. Computer System Layout Templets

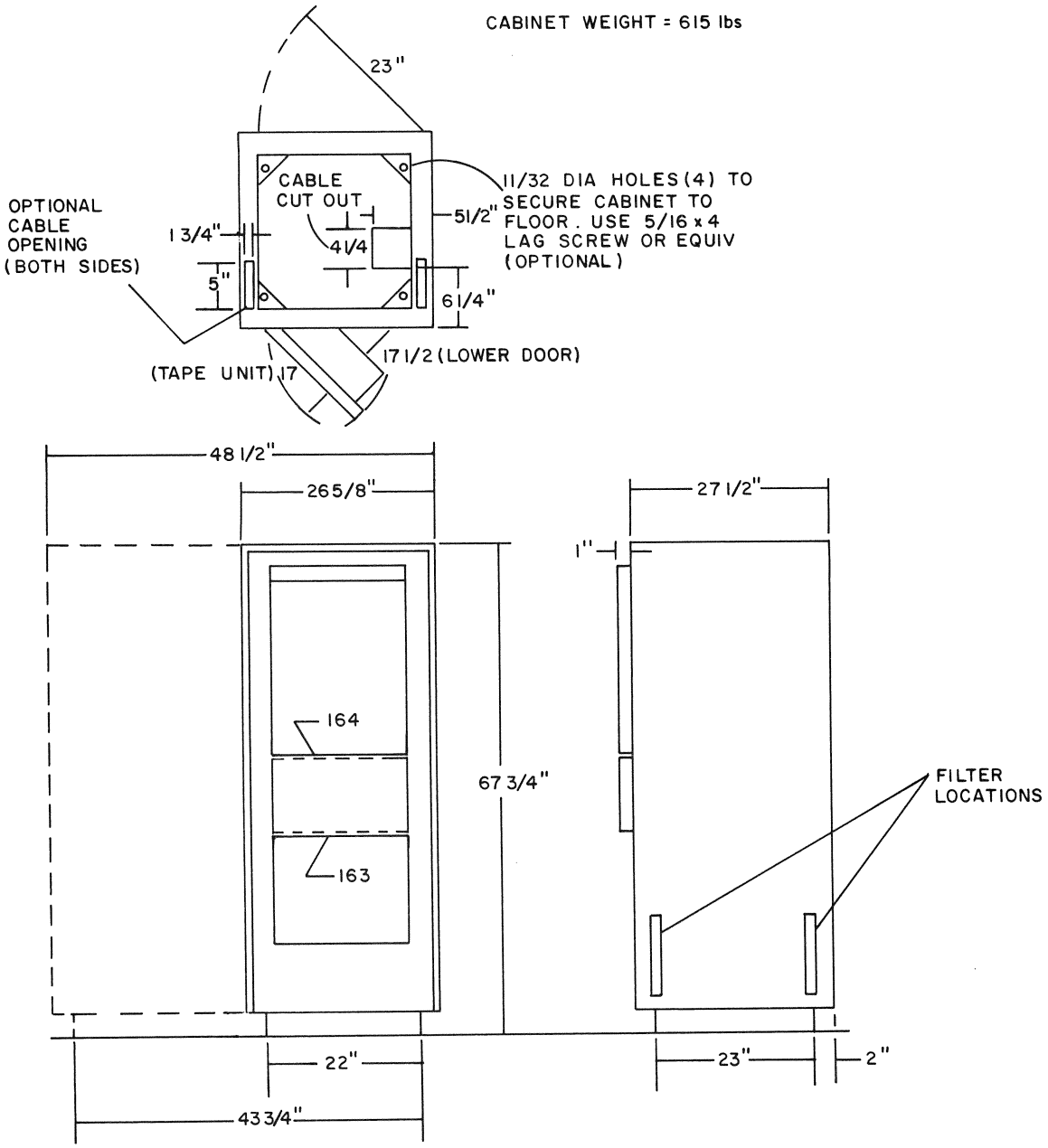


Figure 5. 163-164 Magnetic Tape System