MVME141/D1

MVME141-1/MVME141-2
32 Bit VMEbus/VSB-Based Microcomputer User's Manual

MVME141-1/MVME141-2

32-BIT VMEbus/VSB-BASED MICROCOMPUTER

USER'S MANUAL

(MVME141/D1)

PREFACE

This manual provides general information, hardware preparation, installation instructions, functional description, and support information for the MVME141 32-Bit VMEbus/VSB-based microcomputer.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system or in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be faimilar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

First Edition

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont.)

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This user's manual provides general information, preparation and installation instructions, operating information, and support information for the MVME141 Series of 32-bit VMEbus/VSB-based microcomputers. These modules are referred to as the MVME141 throughout the remainder of this manual.

1.2 FEATURES

The features of the MVME141 microcomputer include:

- MC68Ø3Ø Virtual Memory Microprocessor with 32-bit address and data at 25 or 33.3 MHz.
- MC68882 Floating Point Coprocessor (FPC) at 25 to 33.3 MHz.
- 64Kb of zero wait state physical cache.
- VMEbus Cache Monitor for software transparent cache operation.
- Write-posting interface for fast writes to system memory.
- Two 32-pin, JEDEC standard sockets for ROM/PROM/EPROM.
- One 24-pin, JEDEC standard socket for a 2K x 8 NVRAM/Time-Of-Day Clock.
- One 28-pin, JEDEC standard socket for 32K x 8 Static RAM.
- Two, front panel, RS-232C serial communications ports (MC68681).
- VSB Master interface using the MVSB24ØØ to provide:
  - VSB system controller with bus arbiter.
  - VSB requester with programmable timeout module.
  - Block transfer module with byte count register.
  - Status and Control Register.
- VMEbus Master Interface using the MVME6ØØØ VMEchip to provide:
  - VMEbus System Controller with 4-Level Arbiter.
  - VMEbus A32/A24/A16, D32/D16/DØ8 Master Interface.
  - VMEbus 4-Level Requester.
  - VMEbus 7-Level Interrupter.
  - VMEbus 7-Level Interrupt Handler.
  - Multiprocessor Control and Status Registers.
  - VMEbus access, VMEbus cycle, and Local watchdog timers.

- 16-bit programmable timer (MC68681).
- 24-bit programmable counter/timer (MC6823Ø).
- Front Panel **RUN**, **STATUS**, and **FAIL** LED indicators.
- Front Panel **RESET** and **ABORT** pushbutton switches.
- Four general purpose, software readable switches.
- VMEbus double-high, single-wide form factor.

1.3 SPECIFICATIONS

General specifications for the MVME141 microcomputer are provided in Table 1-1. Sections 1.3.1 and 1.3.2 detail cooling requirements and FCC compliance, respectively.

TABLE 1-1. MVME141 SPECIFICATIONS

Characteristic	Specification
Microprocessor	MC68Ø3Ø 32-Bit Microprocessor
Coprocessor	MC68882 Floating-Point Coprocessor
Operating Frequency:	
MVME141-1	25.Ø MHZ clock frequency
MVME141-2	33.3 MHZ clock frequency
	(The operating frequency for the MC68Ø3Ø and the MC68882 is set by the oscillator installed at location Y2.)
CACHE	64Kb of single-set, direct mapped physical cache supporting two cycle (zero wait state) read accesses at 25 and 33.3 MHz. Write operation is write-through with write-allocate on longword operations.
ROM	Two 32-pin, JEDEC standard sockets are provided for either 64K x 8 or 128K x 8 size, 25Ø nanosecond or faster EPROMs.
SRAM	One 24-pin, JEDEC standard socket is provided for a 2K x 8 NVRAM/Time-Of-Day Clock.
	One 28-pin, JEDEC standard socket is provided for a 32K x 8 Static RAM.
I/O	Two RS-232C asynchronous serial ports are provided using the MC68681 DUART.

TABLE 1-1. MVME141 SPECIFICATIONS (cont.)

Characteristic	Specification
Timers	One 24-bit counter/timer is provided through the MC68230 PI/T. One 16-bit tick timer is provided through the MC68681 DUART. (The tick timer interrupt from the DUART is provided as a separate interrupt source from the serial ports.)
VSB	A VSB system controller and master interface (A32/D32) is implemented using the MVSB2400 VSBchip.
VMEbus	A VMEbus system controller and master interface (A32/A24/A16, D32/D16/D8) is implemented using the MVME6000 VMEchip. The MVME6000 provides a programmable Arbiter, Requester, Interrupter, Interrupt Handler, Multiprocessor CSR, and watchdog timers.
Connectors	Both P1 and P2 backplane connectors are used to power the board and to access the VMEbus and VSB. Two 9-pin "D" connectors are provided on the front panel to access the serial ports.
Power Requirements	+5Vdc, 5.9 Amps maximum (5.3 A typical) +12Vdc, 250 mA maximum -12Vdc, 250 mA maximum
Operating Temperature	0 degree to 50 degrees C inlet air temperature with forced air cooling.
Storage Temperature	-40 degrees to 85 degrees C
Relative Humidity	5% to 90% (non-condensing)
Physical Size (PCB):	VME double-high, single-wide form-factor
Height x Width	9.2 inches (23.34 cm.) x 6.3 inches (16.00 cm.)
Thickness	0.062 inch (0.157 cm.)
Part Projections:	
Component Side	0.50 inch (1.27 cm.) maximum
Solder Side	0.067 inch (0.17 cm.) maximum

1.3.1 Cooling Requirements

Motorola VMEmodules are specified, designed, and tested to operate reliably with an incoming air temperature range from Ø degrees C to 55 degrees C (32 degrees F to 131 degrees F) with forced air cooling. Temperature qualification is performed in a standard Motorola VMEsystem 1ØØØ chassis. Twenty-five watt load boards are inserted in the two card slots, one on each side, adjacent to the board under test to simulate a high power density system configuration. An assembly of three axial lead fans, rated at 1ØØ CFM per fan, is placed directly under the MVME card cage. The incoming air temperature is measured between the fan assembly and the card cage where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 1Ø CFM flowing over the module. Less air flow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions it may be possible to operate the module reliably at higher than 55 degrees C with increased air flow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume of air flowing over a module.

1.3.2 FCC Compliance

The MVME141 microcomputer is tested in an FCC-compliant chassis, and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

1. Shielded cables on all external I/O ports.
2. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
3. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
4. Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the modules.

1.4 GENERAL DESCRIPTION

The MVME141 microcomputer is a VMEbus/VSB-based, high-performance, CPU engine utilizing the Motorola MC68Ø3Ø microprocessor. A block diagram of the MVME141 is illustrated in Figure 1-1.

The MVME141 features 64K bytes of software transparent, zero wait state, physical cache with a write-posting interface. The cache is configured as a single-set, direct-mapped cache containing 4K cache tags with four longword entries (16 bytes) per tag. The cache operates in synchronous mode with the MC68Ø3Ø to provide zero wait state, 2-cycle operation during read hits. During read misses, the cache causes a rerun sequence to the processor while the the write-posting interface simultaneously performs a read access to the target memory. During write operations, the cache operates in a write-allocate, write-through mode in which a cache tag is allocated for longword operations and the target memory is updated along with the cache entry.

Cacheable write operations are latched or "posted" at the write-posting interface. The write-posting interface runs the cycle to the target memory independently so that the processor can continue to operate out of cache while the memory write cycle completes over VSB or VMEbus.

Software transparency for the cache is achieved through a VMEbus Cache Monitor or "Snooper". The Snooper monitors the addresses of all write operations performed on VMEbus by other bus masters in the system. The cache uses the monitored addresses to detect and invalidate any addresses currently valid in the cache memory that have since been modified in system memory.

The MVME141 also features the VME Subsystem Bus (VSB). The VSB provides the processor with a priority port to system memory enabling the MVME141 to continue accessing system memory, even in a heavily active DMA or multiprocessor VMEbus environment. The VSB is implemented with the MVSB24ØØ bus interface chip. The MVSB24ØØ provides a full VSB A32/D32 master interface with system controller support for additional bus masters on VSB.

The MVME141 uses the MVME6ØØØ VMEchip and supporting bus driver chips to implement a VMEbus A32/A24/A16, D32/D16/D8 compatible master interface. The MVME6ØØØ includes the VMEbus system controller functions, a programmable master interface with programmable request level and request/release mode, a 7-level Interrupter and Interrupt Handler, a global register set, four address location monitors, plus other features. The global register set and location monitors provide support for multiprocessing applications. The global register set is accessible as a slave resource by other VMEmodules.

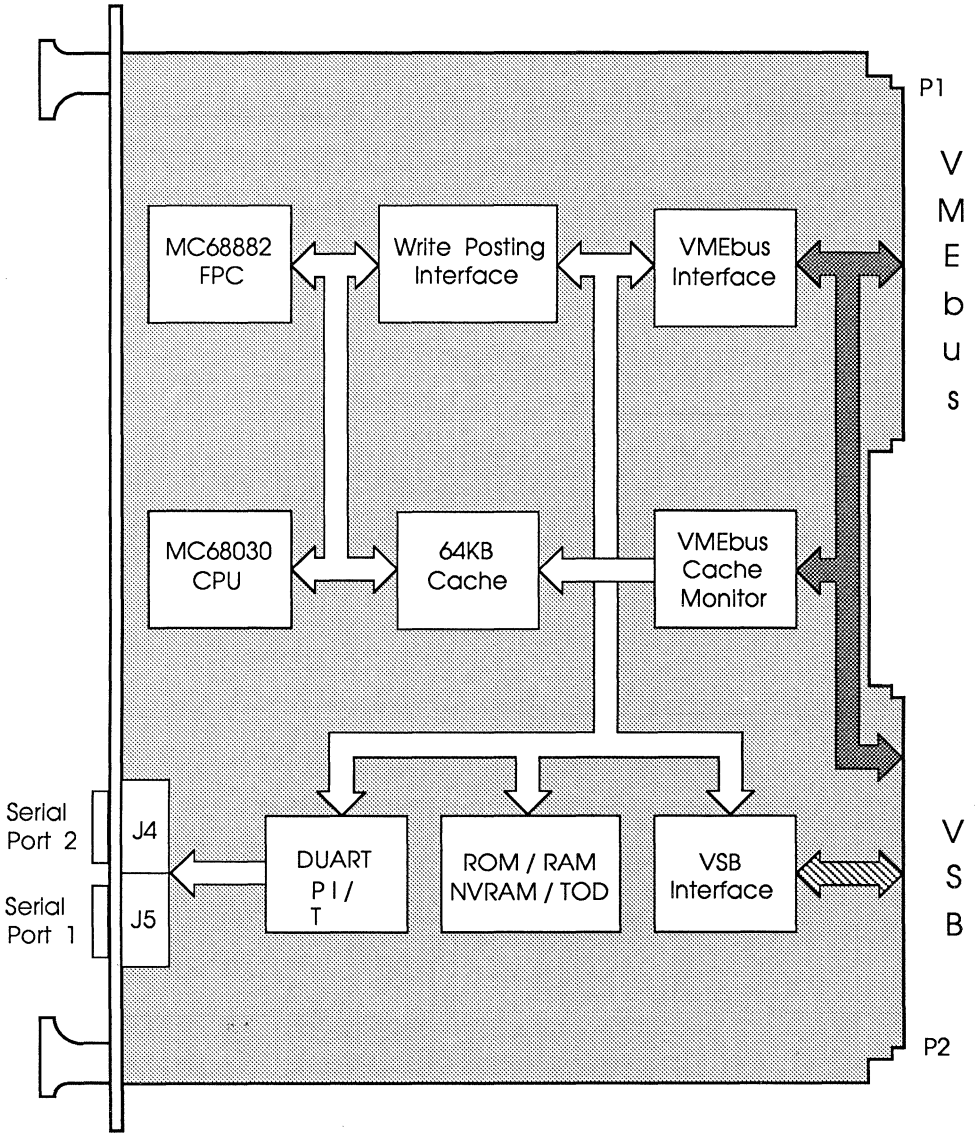


FIGURE 1-1. MVME141 BLOCK DIAGRAM

The MVME141 includes the MC68882 floating-point coprocessor, the MC68681 DUART for serial I/O and software timing, the MC6823Ø PI/T for local CSR and software counter/timer, two 32-pin JEDEC standard sockets for EPROMs, one 24-pin JEDEC socket for 2K x 8 Non-Volatile RAM/Time-Of-Day Clock, and one 28-pin JEDEC socket for 32K x 8 Static RAM. The static RAM is provided for non-performance critical, private storage of data for applications such as a resident debugger/diagnostic firmware package.

1.5 REFERENCE DOCUMENTATION

The following publications provide additional helpful information. They describe the VLSI devices, the I/O interfaces, and the firmware used on the MVME141. If not shipped with this product, they may be purchased from the Motorola Literature Distribution Center, 616 West 24th Street, Tempe Arizona 85282; telephone (6Ø2) 994-6561.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
MC68Ø3Ø User's Manual	MC68Ø3ØUM
MC68882 User's Manual	MC68882UM
MC68681 DUART	ADI-988-R1
MC6823Ø Parallel Interface/Timer (PI/T)	ADI-86Ø-R2
VMEbus Specification (Rev C.1)	HB212/D
VME Subsystem Bus (VSB) Specification	MVMESB
VSBchip User's Manual	MVSB24ØØ
141BUG User's Manual	MVME141BUG

An additional publication that may provide helpful information is the EIA RS-232-C Serial Interface Specification, which is available from the Electronic Industries Association, Washington, D.C.

1.6 MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides the unpacking, hardware preparation, and installation instructions for the MVME141 microcomputer. It also describes the system support requirements and the start-up procedures.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request that the carrier's agent be present during unpacking/inspection of equipment.

Carefully unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the shipping carton and packing materials for storing or reshipping of the equipment.

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

Inspect for any shipping damage. If no damage exists, then the module can be prepared for operation according to the following sections of this chapter.

2.3 HARDWARE PREPARATION

This section describes the hardware preparation of the MVME141 prior to installation. Observance of this description will ensure the user that all components are properly configured for operation.

Jumper blocks are used to select various hardware and software functions on the MVME141. They must be properly configured before installation according to the hardware parameters of the board, and according to the user's application of the board in the system. The jumper blocks are illustrated in Figure 2-1 with their factory jumper settings (asterisks indicate the factory settings). The

factory settings configure the board for one common mode of operation. The user should verify and change these jumper settings as required to configure the module for the target application. The jumper functions and settings are summarized in Table 2-1 and described in the following sections.

TABLE 2-1. MVME141 JUMPER SUMMARY

Jumper: Function	Position	Configuration
J1: VMEchip Control	J1(1-2)	* Installed - System Controller Enabled
	J1(3-4)	* Installed - (Not Used)
	J1(5-6)	* Installed - Decodes GCSR A8 = Ø
	J1(7-8)	* Installed - Decodes GCSR A9 = Ø
	J1(9-1Ø)	* Installed - Decodes GCSR A1Ø = Ø
	J1(11-12)	* Installed - Decodes GCSR A11 = Ø
	J1(13-14)	* Installed - Decodes GCSR A12 = Ø
	J1(15-16)	* Installed - Decodes GCSR A13 = Ø
	J1(17-18)	* Installed - Decodes GCSR A14 = Ø
	J1(19-2Ø)	* Installed - Decodes GCSR A15 = Ø
J2: VMEchip Clock	J2(1-2)	Installed - 16 MHz clock source
	J2(2-3)	* Installed - 8 MHz clock source
J3: VMEbus Lock	J3(1-2)	Installed - VMEbus Lock Enabled
	J3(2-3)	* Installed - VMEbus Lock Disabled
J6: General Purpose	J6(1-2)	* Installed - CSR bit GPSW1 = Ø
	J6(3-4)	* Installed - CSR bit GPSW2 = Ø
	J6(5-6)	* Installed - CSR bit GPSW3 = Ø
	J6(7-8)	* Installed - CSR bit GPSW4 = Ø
J7: VSB chip	J7(1-2)	* No Jumper - Normal operation
	J7(1-2)	Installed - Factory test only

Notes: Asterisks indicate factory configuration.
Designators J4 and J5 are assigned to the DB-9 connectors.

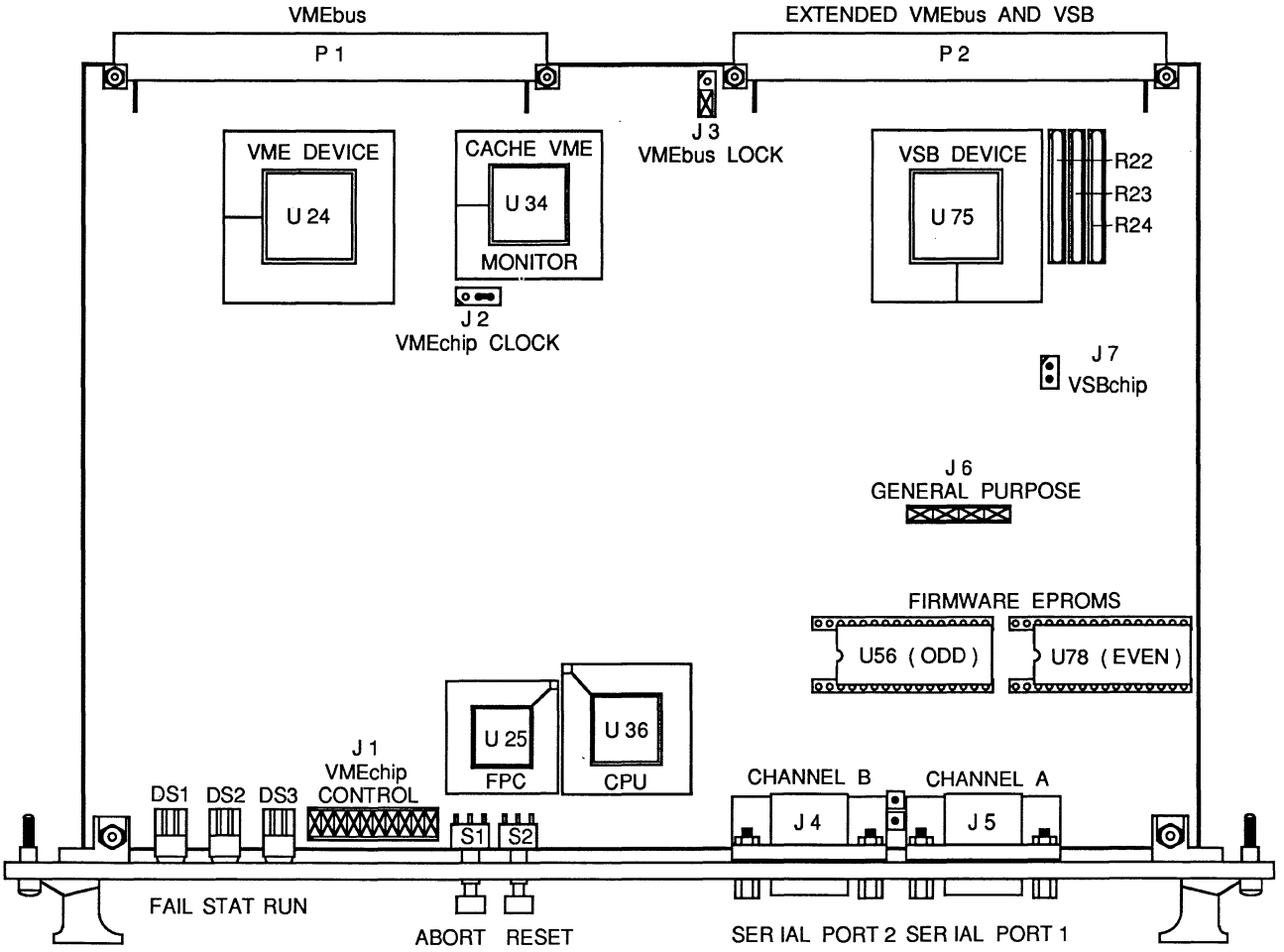
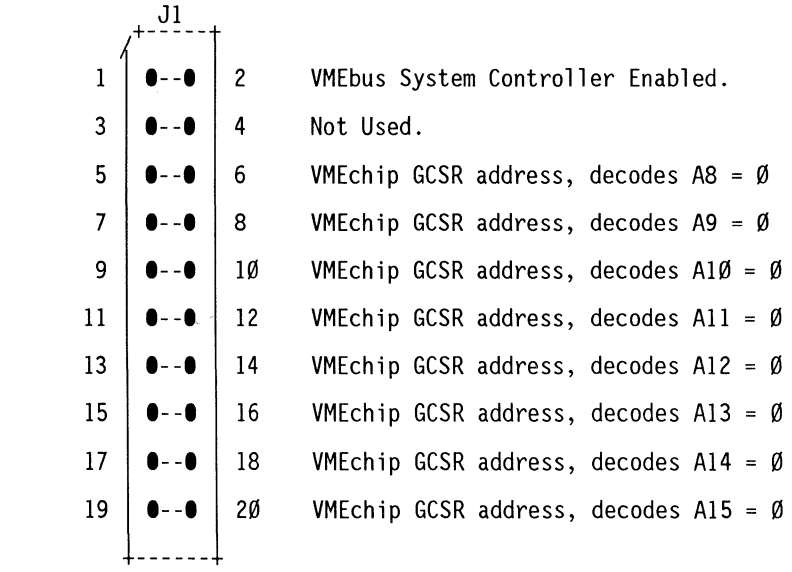


FIGURE 2-1. CONFIGURATION REFERENCE DRAWING

2.3.1 VMEchip Control (J1)

Jumper block J1 selects the VMEbus System Controller function and the group address of the global CSR (GCSR) for the VMEchip. Installing a jumper cap at position J1(1-2) will select the MVME141 as the VMEbus system controller. The state of this jumper can be read by the processor through the local CSR (LCSR) in the VMEchip. When selected as system controller, the MVME141 should be installed in the chassis in the left-most card slot relative to the other VMEbus bus masters in the system. Jumper position J1(3-4) is not used. The remaining eight jumper positions on J1 are used to select the group address of the GCSR. The group address of the GCSR is selected for a VMEbus Short I/O access with a match on the eight VMEbus address lines A8 through A15. Each of the jumper positions is assigned to the corresponding VMEbus address line given in Table 2-1 and compared with that address line for a match condition. An installed jumper causes a match for a logic zero on its corresponding VMEbus address line, and a removed jumper causes a match for a logic one. Note that the base address of the GCSR is further decoded within the group by the VMEchip. Refer to the VMEchip User's Manual for a description of the GCSR.

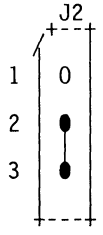
Jumper Block J1
VMEchip Control
(Factory Setting)



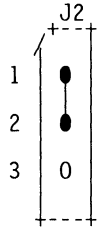
2.3.2 VMEchip Clock Select (J2)

Jumper block J2 selects the clock source for the VMEchip. A jumper at setting J2(2-3) will select 8 MHz operation. This jumper is implemented as a soldered-in staple, and it is not recommended for modification by the user. Note that at initial release, the VMEchip is not specified for operation at 16 MHz on the MVME141. If 16 MHz operation (setting J2(1-2)) is selected and in question, contact a factory representative for verification of the jumper configuration.

Jumper Block J2
VMEchip Clock
8 MHz Clock Source
(Factory Setting)



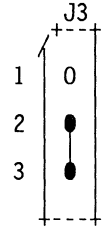
Jumper Block J2
VMEchip Clock
16 MHz Clock Source



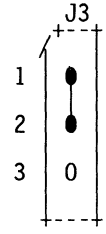
2.3.3 VMEbus Lock Select (J3)

Jumper block J3 selects the resource lock control for VMEbus RMC (Read Modify Cycle) operations. The resource lock on VMEbus is a unique feature supported on certain Motorola VMEmodules that contain dual-port memory resources. It is used to support the CAS and CAS2 instructions of the MC68Ø2Ø and MC68Ø3Ø microprocessors. For these instructions, multiple memory cycles to different addresses may be executed during a single indivisible RMC operation. The resource lock control is provided to ensure the indivisibility of these cycles to the dual-port boards. The resource lock is implemented by driving the RMC* signal from the processor onto the VMEbus reserved pin P2-B3 during VMEbus operations. The supporting dual-port boards use this signal when asserted as a port lock control to prevent the alternate memory port from gaining access to the memory resource during the indivisible block of cycles. Jumper J3 should only be set to the lock-enabled position (setting J3(1-2)) if a dual-port memory resource on VMEbus supports the resource lock control, and if the VMEbus reserved pin is not otherwise used in the system. With jumper block J3 set to the lock-disabled position (setting J3(2-3)), no connection is made to the VMEbus reserved pin. Jumper block J3 is factory configured for the lock-disabled function.

Jumper Block J3
VMEbus Lock Select Disable
(Factory Setting)



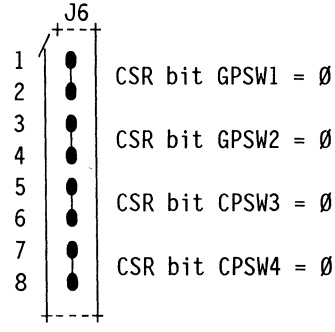
Jumper Block J3
VMEbus Lock Select Enable



2.3.4 General Purpose Jumpers (J6)

Jumper block J6 provides four general purpose jumpers that are readable by software and perform no hardware functions directly. They can be used as software switches by the software or firmware running on the board to select various program-controlled functions. The jumper positions are readable through the GPSW1 through GPSW4 bits of the PI/T CSR. An installed jumper reads as a logic zero from its corresponding CSR bit, and a removed jumper reads as a logic one. The PI/T CSR bits are described in section 4.2.5.1. If the 141Bug firmware EPROMs are installed, refer to the 141Bug User's Manual for the functional assignments for these jumpers.

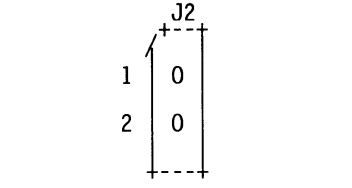
Jumper Block J6
General Purpose Jumpers
(Factory Setting)



2.3.5 VSBchip Jumper (J7)

Jumper block J7 is provided for factory test purposes only. No jumper cap should be installed at this location.

Jumper Block J2
VSBchip Jumper
No Jumper Installed
(Factory Setting)



2.3.6 Firmware EPROMs

Two firmware EPROMs are required on the MVME141 to provide the start-up program for the MC68Ø3Ø after a power-up or reset condition. The EPROMs should be installed at chip locations U56 and U78 on the MVME141. These chip locations are implemented as two 32-pin, raised DIP sockets that can accept either two JEDEC compatible, 28-pin, 64K x 8 EPROMs, or two JEDEC compatible, 32-pin, 128K x 8 EPROMs. Both EPROMs should be of the same type, and either type can be used without any jumper modifications. If 28-pin EPROMs are used, they should be bottom justified in the 32-pin sockets (closer to the board edge) as illustrated in Figure 2-1. EPROMs with a speed of 25Ø nanoseconds or faster can be used.

The 141Bug firmware product from Motorola is optionally supplied for the MVME141. When installed on the board, the 141Bug uses the general purpose jumpers at jumper location J6 for system configuration. These jumpers must be properly configured before installation. Generally, these jumpers are used as software switches to enable or disable the major features of the MVME141, and they should normally be installed to select the preferred enabled states. For a further description of the configuration controls and operating instructions for the 141Bug firmware, refer to the 141Bug User's Manual.

2.3.7 VSB Bus Termination

Resistor terminations are used on the VSB bus to optimize the electrical characteristics of the VSB signal lines. They may be located either on the processor board or on the VSB backplane. The MVME141 provides three 33Ø/47Ø ohm, 1Ø-pin SIP resistor networks at

component locations R22, R23, and R24 (by the P2 connector) for the VSB signal terminations. These resistor networks may require removal from the board depending upon the type of VSB backplane used and the number of MVME141s installed on the same VSB bus. The resister networks are socketed on the MVME141 for easy removal.

The resister networks should be configured on the MVME141 so that there is only one set of terminators on the VSB bus, and so that the terminators are located at the left or rightmost card slot of the bus. If a VSB backplane with integral termination resistors is used, then the three resistor networks on the MVME141 should be unplugged from the board. If a VSB backplane without termination resistors is used (such as a ribbon cable and connector backplane), then the three resistor networks on the MVME141 should remain installed on the board if it is the only VSB master or if it is the correct left or rightmost board.

2.4 SYSTEM SUPPORT

The MVME141 is designed to operate in a VMEmodule system. To support the module in the system, the VMEbus P2 connector should be fully supported for power, for the extended VMEbus, and for the VSB bus. For optimum performance, the VSB memory modules in the system should be jumpered for "cycle start" on address strobe if supportable. In addition, the RS-232 cables must be supplied for the front panel serial ports. Compatible chassis, VME/VSB memory modules, and serial port distribution boards that support the MVME141 are available from Motorola.

2.4.1 Power Distribution

The MVME141 draws electrical power from both the P1 and the P2 connectors. Both connectors must be fully supported for +5 Volt power distribution. If the power connections for the P2 connector are not supported on the backplane, then the MVME141 will be unable to draw enough power from the P1 connector only to operate reliably, and the excessive power draw through P1 only may damage the P1 connector on the board or on the backplane. For optimum reliability, the power distribution for the P1 and P2 connectors should be integrated into a single, monolithic, multilayer backplane utilizing individual power and ground planes.

2.4.2 Extended VMEbus

The MVME141 uses the P2 connector to connect to the extended address and data sections of VMEbus. The extended address bus contains the VMEbus address lines A24 through A31, and provides for system expandability. The extended data bus contains the VMEbus data lines D16 through D31, and provides for increased data throughput and system performance. The extended buses may or may not be supported

in the system depending on the backplane configuration and the VMEmodules installed. The use of the extended buses by the MVME141 may be enabled or disabled through the CSR bits in the MVME6ØØØ VMEchip, through the VA24 bit in the PI/T CSR, and through certain predefined ranges of the MVME141 address map. The extended data bus, however, **must** be supported in the system to any memory module residing in the MVME141 cacheable address space. The MVME141 only supports caching to 32-bit wide data ports, and it performs all read accesses to its cacheable address space as 4-byte, longword-aligned data transfers. If a D16 module is located in the cacheable address space, the MVME141 will not be able to access the odd-word addresses on the module. Refer to section 4.5.1 on the definition of cacheablity. The extended address and data sections of the VMEbus occupy the center row of the P2 connector. They should be integrated into the PCB backplane of the chassis for optimum electrical characteristics. Refer to the VMEbus Specification for a description of the VMEbus signals and backplane requirements.

2.4.3 VSB Cabling

The MVME141 uses the P2 connector to connect to the VSB bus. The VSB (VME Subsystem Bus) is an independent data transfer bus that provides an alternate port to system memory for increased performance in a DMA or multiprocessor VMEbus system. The VSB bus may or may not be supported in the system depending on the backplane interconnection and the memory modules installed. The use of the VSB bus by the MVME141 may be enabled or disabled through the CSR bits in the MVSB24ØØ VSB chip. The VSB bus occupies the two outer rows of the P2 connector. These outer rows are provided in the VMEbus specification for user applications, and they are normally unconnected on the VMEbus backplane. These outer rows must be bussed on the backplane from the MVME141 card slot to the card slots of the memory modules or other modules in the chassis that support the VSB bus.

The VSB bus interconnection is typically implemented with a ribbon cable and connectors (or a monolithic PCB with connectors) that presses onto the P2 connector pins which extend out from the back of the VMEmodule backplane. A ribbon cable backplane will not support the proper bus grant daisy-chain for VSB. It will be suitable, however, for one to two VSB bus masters as long as the bus grant in and bus grant out lines are shorted together by at least one module on the bus. The memory module will typically serve this function. If three or more VSB masters are required on the same bus, then a PCB VSB backplane must be used that implements the bus grant daisy-chain properly. The VSB bus physical length is limited to 6 card slots. Refer to the VSB Specification for a description of the VSB bus signals and backplane requirements. Refer also to section 2.3.7 for the VSB bus termination requirements.

2.4.4 VSB Cycle Start

Some VSB memory modules provide a jumper to select the start-of-cycle condition either on the assertion of the VSB address strobe, or on the assertion of the VSB data strobe. The jumper selection depends on whether the VSB master performs address-only cycles in which a VSB resource is selected by an address but no data transfer is performed to it. Note that "bounce" cycles on VSB are address-only cycles, but that they do not select a target resource on VSB so they do not fall into this category of cycles. The MVME141 does not perform address-only cycles to target resources, so the VSB slave modules can be configured for start-of-cycle on VSB address strobe provided that other VSB masters on the bus, if any, do the same. Generally, start-of-cycle on address strobe for the slave modules will allow for higher performance operation with the MVME141. Refer to the user's manuals of the VSB memory modules in the system for their start-of-cycle jumper configurations.

2.4.5 RS-232 Cables

The RS-232 cables must be supplied to connect to the two front panel serial ports. Each serial port uses a 9-pin, female "D" connector with the pin assignments listed in the leftmost column of Table 2-2. Each port provides the standard RS-232C handshake signals RTS, CTS, DTR, DCD, and DSR. The input handshake signals CTS and DCD are pulled-up at each connector to support basic 3-wire operation using only TXD, RXD, and GND. Refer to section 4.2.6.1 for a description of the handshake signals.

TABLE 2-2. SERIAL PORT CABLING

MVME141 Connector DB-9	SIGNAL I/O	Connector to DTE/TERM DB-9 (DB-25)	Connector to DCE/MODEM DB-9 (DB-25)
TXD, 3	-->	RXD, 2 (3)	TXD, 3 (2)
RXD, 2	<--	TXD, 3 (2)	RXD, 2 (3)
RTS, 7	-->	CTS, 8 (5)	RTS, 7 (4)
CTS, 8	<--	RTS, 7 (4)	CTS, 8 (5)
DTR, 4	-->	DCD, 1 (8)	DTR, 4 (2Ø)
DCD, 1	<--	DTR, 4 (2Ø)	DCD, 1 (8)
DSR, 6	---	DSR, 6 (6)	DSR, 6 (6)
GND, 5	---	GND, 5 (7)	GND, 5 (7)

Notes: Signal names on the left are at the MVME141 connector.
Signal names on the right are on the cable.
DSR on the MVME141 is a pull-up resistor to +12V.
DB-9, pin 9 (DB-25, pin 1) is not connected.

Both serial ports on the MVME141 are configured at the DUART controller chip as DTEs (Data Terminal Equipment), so null-modem cables will generally be required to connect to other terminal equipment. The recommended cabling configurations are given in Table 2-2 for connecting to other computer equipment using either DB-9 or DB-25 connectors. Note that the connector pinouts or the use of the handshake signals may vary with other computer equipment, so other cabling configurations may be required than those given in the table. The use of shielded cables is recommended to reduce the generation and susceptibility of EMI (Electro Magnetic Interference).

2.4.6 Serial Distribution Boards

Serial distribution boards are available from Motorola for the front panel serial ports on the MVME141. The MVME714 from Motorola can be used to translate the front panel DB-9 connectors to DB-25 connectors, to allow the serial ports to be individually reconfigured from DTEs (Data Terminal Equipment) to DCEs (Data Computer Equipment), and to enable the routing of the serial port cables to the rear of the chassis. The MVME714M from Motorola is a similar product that includes a modem interface for a direct telephone hook-up. Note that the use of a serial transition board may alter the cabling requirements described in section 2.6.5.

2.5 INSTALLATION INSTRUCTIONS

After the MVME141 has been properly configured for operation, it is ready for installation in a VMEmodule chassis.

CAUTION

INSERTING OR REMOVING THE MODULE WHILE POWER IS APPLIED CAN DAMAGE THE MODULE CIRCUITRY. AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

Ensure that power is turned off to the chassis, and that the card ejector handles are in their non-eject positions. Slide the board into the board slides of the selected slot until the P1/P2 connectors align and seat into their backplane sockets. Press firmly on the top and bottom sections of the front panel until the connectors seat fully into their backplane sockets. Avoid pressing against the card ejector handles as they may slide into their card eject positions. Also avoid pressing against the pushbutton switches or other projections from the front panel as they can be physically damaged. When installing, check the position of the two

captive screws at the top and bottom ends of the front panel. They may jam against the chassis frame and prevent the board from seating fully.

Once installed, screw in the two captive screws to secure the board in place. Avoid over-tightening the screws as they may strip out the screw sockets. The screws also serve to electrically connect the front panel to the frame of the chassis by pressing the conductive top and bottom sections of the front panel against the conductive frame of the chassis. This integrates the front panel into the EMI (Electro Magnetic Interference) shield of the chassis. This also completes the termination for the cable shield if shielded serial port cables are used, and it reduces the susceptibility of the board to static discharge that can result from touching the front panel. These EMI protections rely on the use of a chassis that is properly designed to control the susceptibility and emission of EMI.

2.6 START-UP

After the MVME141 has been properly configured and installed in a VMEmodule chassis, it is ready for power-up. Connect a console terminal to serial port 1 of the MVME141, and turn power on to the chassis. The front panel **FAIL** and **STAT** LEDs should illuminate during the power-up reset period (or after any reset condition). The power-up reset period should typically last less than a second. After the reset period is complete, the **FAIL** LED should remain illuminated to indicate that the board is in a start-up "non-ready" mode of operation, the **STAT** LED should go dim or out, and the **RUN** LED should illuminate to indicate that the processor is operating. The **RUN** and **STAT** LEDs together give a rough indication of how the processor is operating. Refer to section 3.2 for a description of the LED indicators.

After any power-up or reset condition, the processor will begin executing the firmware supplied in the EPROMs. If the 141Bug firmware EPROMs are installed, the processor will perform a self-test and initialization sequence. Upon successful completion, it will turn the **FAIL** LED off, search for system memory and controller boards installed (if directed by its configuration parameters), output a start-up message to the console screen, and wait for user input (or begin booting if directed).

CHAPTER 3 - OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter describes the operating controls and indicators on the MVME141 microcomputer.

3.2 LED INDICATORS

The MVME141 has three LED indicators (**FAIL**, **STAT**, and **RUN**) located on the front panel. These indicators help to indicate the operation of the processor.

3.2.1 FAIL Indicator (DS1)

The **FAIL** LED indicator illuminates red while the BRDFAIL (Board Fail) bit of the System Controller Configuration Register in the LCSR of the VMEchip is asserted. It indicates that the MVME141 is driving the SYSFAIL signal on the VMEbus (provided the ISF bit in the GCSR of the VMEchip is not asserted). Refer to the VMEchip User's Manual for a description of the LCSR and GCSR control bits.

The BRDFAIL bit of the VMEchip is asserted after any power-up or reset condition. Generally, the processor should turn off the BRDFAIL bit (thereby turning off the FAIL LED and releasing the SYSFAIL signal on the VMEbus) to indicate that it has successfully passed a self-test procedure and is ready for normal operation. The processor should re-assert the BRDFAIL bit (thereby illuminating the **FAIL** LED and asserting the SYSFAIL signal on VMEbus) whenever a significant error has occurred as defined by the user's application of the board.

3.2.2 STAT Indicator (DS2)

The **STAT** LED indicator illuminates yellow while the STATUS signal from the processor is asserted. The STATUS signal indicates several states of the processor. It asserts statically to indicate that the processor is halted or reset. It also asserts dynamically (pulses) while the processor is operating to indicate various states of the operation of the internal execution unit of the processor. As such, the **STATUS** LED will illuminate brightly while the processor is reset or halted, and it will also illuminate dimly or brightly while the processor is operating normally. In general, the following operations can be roughly interpreted from the **RUN** and **STATUS** LEDs.

RUN LED	STATUS LED	Indication
Off	Off	Stopped (no program activity)
Off	On	Halted or Reset
On	Off	Bus Locked
On	Dim/Bright	Normal Operation

3.2.3 RUN Indicator (DS3)

The **RUN** LED illuminates green while the AS* (address strobe) or the ECS* (Early Cycle Start) signal from the processor is asserted. It indicates that the processor is performing accesses to off-chip resources or to its on-chip cache.

3.3 PUSHBUTTON CONTROLS

The MVME141 has two pushbutton-type switches (**RESET** and **ABORT**) located on the front panel. These switches can be used to restart or abort the operation of the processor.

3.3.1 ABORT Switch (S1)

The **ABORT** switch, when pressed, generates a falling-edge signal transition on the H2S pin of the PI/T chip. The PI/T should be properly configured to generate a level 7 interrupt to the processor on this signal transition.

3.3.2 RESET Switch (S2)

The **RESET** switch, when pressed, asserts the BRDRESET (Board Reset) signal to the VMEchip. The VMEchip then resets all devices on the MVME141, and if jumpered as a system controller, it asserts the SYSRESET signal on VMEbus to reset all the boards in the system. The VMEchip is also reset by this switch. The **RESET** switch is debounced but not timed on the MVME141. It should be held pressed momentarily before releasing. The resulting reset generated by the VMEchip is timed for a minimum assertion of 200 milliseconds.

CHAPTER 4 - FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides the operating and programming information for the MVME141 microcomputer.

4.2 ADDRESS MAP

The address map for the MVME141 is given in Table 4-1. The address map is also illustrated in Figure 4-1 for the VSB operating in "bounce" mode, and in Figure 4-2 for the VSB operating in "non-bounce" mode. Refer to section 4.2.9 for a description of bounce operation.

The bottom half of the address map (ØØØØØØØØ to 7FFFFFFF) is decoded for cacheable resources, and the top half of the address map (8ØØØØØØØ to FFFFFFFF) is decoded for noncacheable resources. The top 256Kb of the address map (Fxxxxxxx) are further decoded for special VMEbus (A24,A16,D16) resources and for local (on-board) resources. The local resources and VMEbus Short I/O (A16) resources are decoded in the top megabyte (FFFxxxxx) of this address space. Some of the resources in the address map appear replicated throughout a larger address space. For these cases, the recommended address range to use is given in Table 4-1, and the replicated address ranges should not be used. All of the address references are given as physical addresses outside the MC68Ø3Ø chip (output side of the PMMU). The resources of the address map are described in the following sections.

4.2.1 Function Codes

The three function code signals on the MC68Ø3Ø specify the type of cycle being run. They specify User Data (FC=1), User Program (FC=2), Supervisor Data (FC=5), and Supervisor Program (FC=6) cycle types, as well as three reserved cycle types (FC=Ø,3,4) and CPU Space cycles (FC=7). Processor cycles using any of the non-CPU Space cycle function codes (FC=Ø-6) will select the resources of the address map illustrated on the left in Figure 4-1 and Figure 4-2. Processor cycles using the CPU Space cycle function code (FC=7) will select an alternate address map containing the MC68882 coprocessor and the interrupt acknowledge vectors as shown on the right in Figure 4-1 and Figure 4-2.

The function codes are usually generated automatically by the MC68Ø3Ø, and not directly specified by the user. However, the user can directly specify the function codes for data accesses with the MOVES instruction. Caution should be used if doing this to a device over VMEbus as the lower three bits of the VMEbus address modifiers

TABLE 4-1. ADDRESS MAP

Address	Resource	Size	Comments
FFFFØØØØ-FFFFFFFF	VSB/VMEbus-SHIO	64K	A16, D16, CI
FFFCØØØØ-FFFEFFFF	(Reserved)	-	VSB/VMESHIO replicated
FFFBØØ3Ø-FFFBFFFF	(Reserved)	-	VMEchip CSR replicated
FFFBØØØØ-FFFBØØ2F	VMEchip CSR	48	D16 (odd byte only), CI
FFFAØØØ8-FFFAFFFF	(Reserved)	-	VSB/VME
FFFAØØØØ-FFFAØØØ7	VSBchip CSR	8	D32, CI
FFF9ØØØØ-FFF9FFFF	(Reserved)	-	Local Timeout
FFF8ØØØØ-FFF8FFFF	(Reserved)	-	VSB/VME
FFF7ØØ1Ø-FFF7FFFF	(Reserved)	-	DUART replicated
FFF7ØØØØ-FFF7ØØØF	DUART	16	D8, CI
FFF6ØØ2Ø-FFF6FFFF	(Reserved)	-	PI/T replicated
FFF6ØØØØ-FFF6ØØ1F	PI/T-Local CSR	32	D8,CI
FFF5Ø8ØØ-FFF5FFFF	(Reserved)	-	NVRAM/TOD replicated
FFF5Ø7F8-FFF5Ø7FF	Time-Of-Day Clock	8	D8, CI
FFF5ØØØØ-FFF5Ø7F7	NV Static RAM	2Ø4Ø	D8, CI
FFF48ØØØ-FFF4FFFF	(Reserved)	-	SRAM replicated
FFF4ØØØØ-FFF47FFF	Static RAM	32K	D8, CI
FFF2ØØØØ-FFF3FFFF	(EPROM Expansion)	128K	1M bit EPROM option
FFFØØØØØ-FFF1FFFF	EPROM	128K	D16, CI, LTO on writes
F1ØØØØØØ-FFEFFFFF	VSB/VMEbus	239M	A32, D16, CI
FØØØØØØØ-FØFFFFFF	VSB/VMEbus	16M	A24, D16, CI
8ØØØØØØØ-EFFFFFFF	VSB/VMEbus	1792M	A32, D32, CI
Ø1ØØØØØØ-7FFFFFFF	VSB/VMEbus	2Ø32M	A32, D32, CCB
ØØØØØØØØ-ØØFFFFFF	VSB/VMEbus	16M	A32, D32, CCB or A24, D32, CCB

Notes: CCB = Cacheable, CI = Cache Inhibited
A24 option at ADR = Ø is selected by the PI/T CSR bit VA24.
All VSB references are A32.

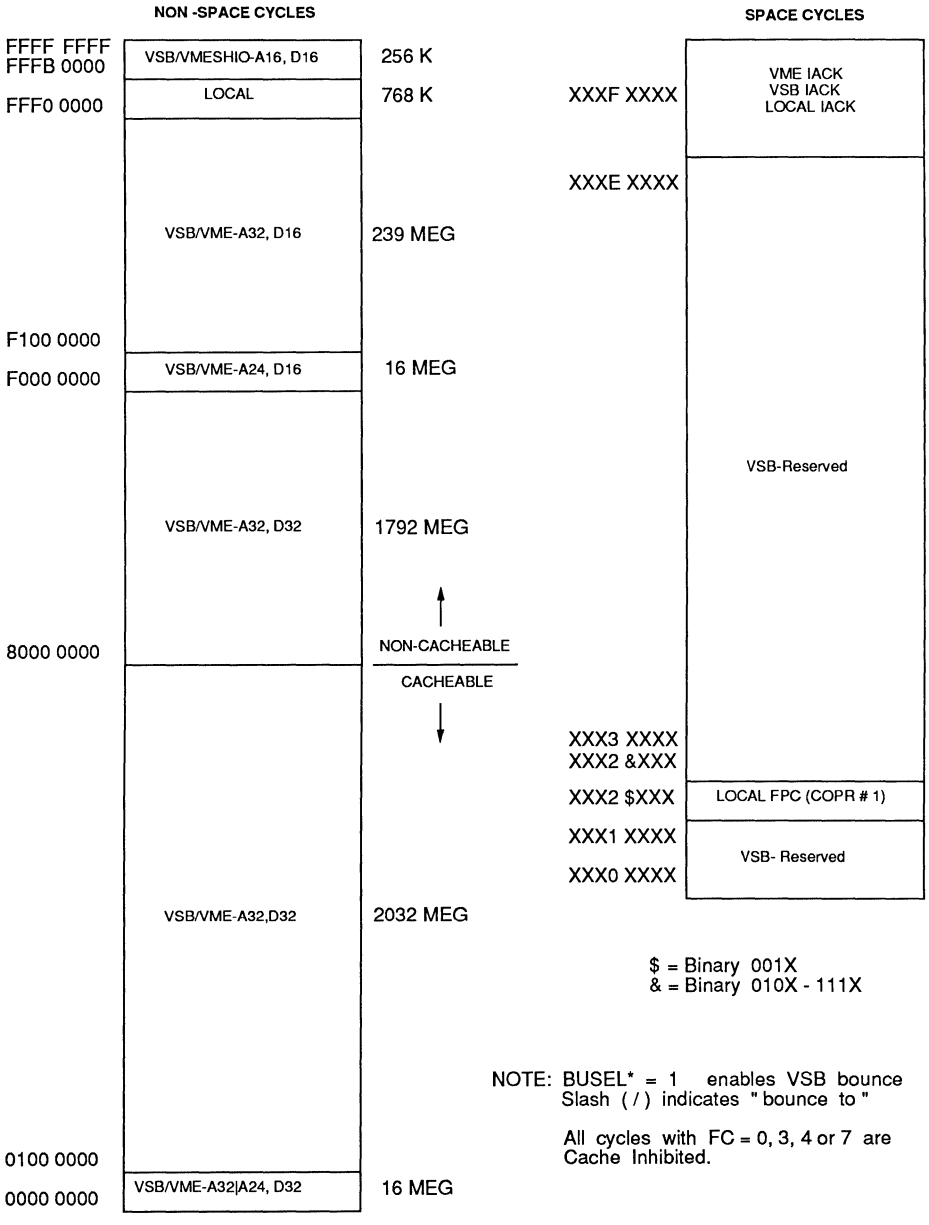


FIGURE 4-1. MVME141 SYSTEM ADDRESS MAP (WITH VSB BOUNCE ENABLED)

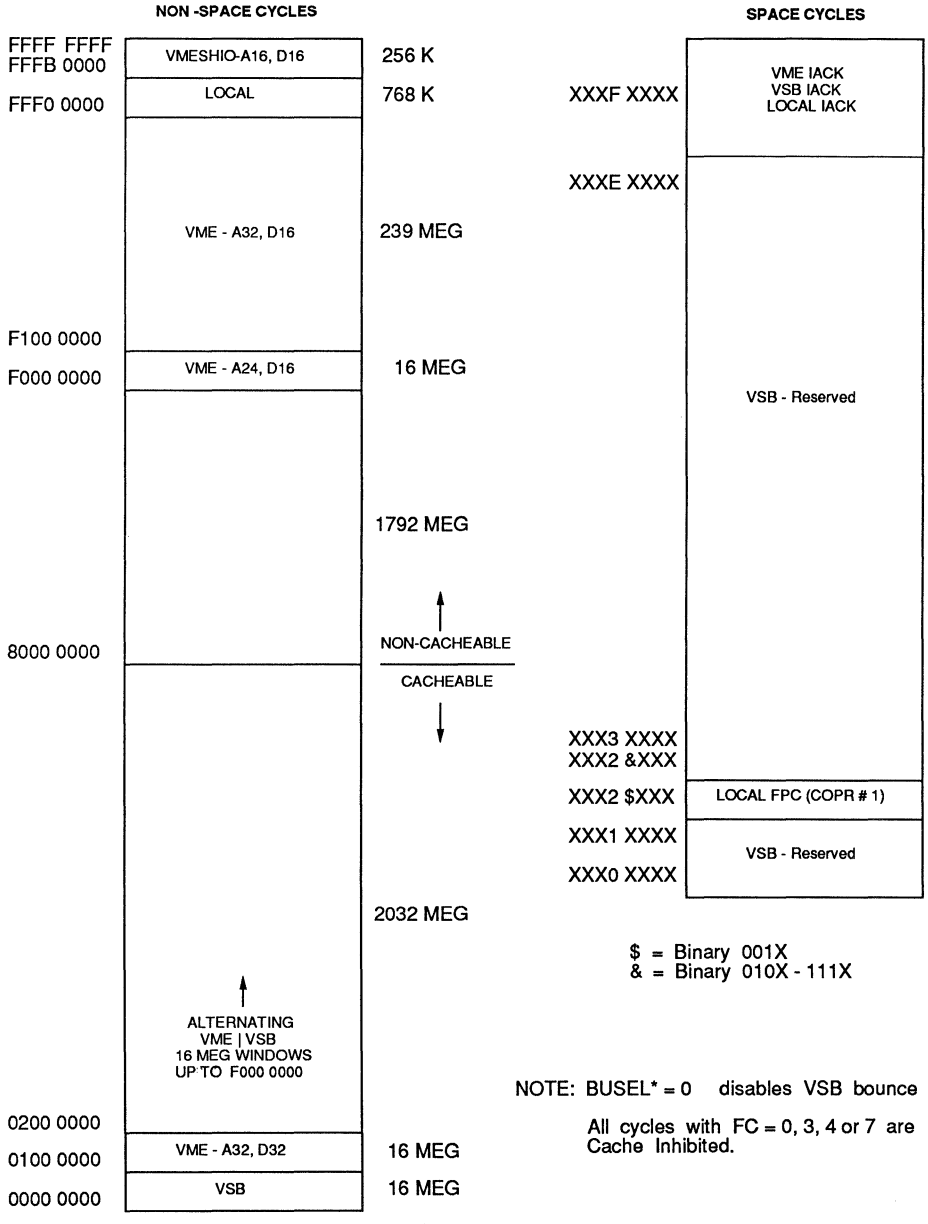


FIGURE 4-2. MVME141 SYSTEM ADDRESS MAP (WITH VSB BOUNCE DISABLED)

are generated directly from the function codes through the VMEchip. This may generate a reserved address modifier on VMEbus that the target device may not respond to. Refer to the VMEbus Specification for address modifier usage.

4.2.1.1 CPU Space Address Map

Processor cycles using the CPU Space function code (FC=7) will select an alternate address map containing the MC68882 Floating Point Coprocessor (FPC) and the interrupt acknowledge vectors. The FPC is decoded as coprocessor #1 and is selected automatically by the processor when CPID equals 1 in the coprocessor instructions. The interrupt acknowledge vectors are accessed automatically by the processor during interrupt acknowledge cycles. The CPU Space address map is illustrated in Figure 4-1 and Figure 4-2. Only certain address bits are decoded to select the CPU Space resources. The FPC appears normally at space addresses 22ØØØ through 22Ø1F, and the interrupt acknowledge vectors appear normally at space addresses FFFFFFF3 through FFFFFFFF (odd addresses only). A space address that does not select the FPC or interrupt vectors will be routed to the VSB bus but not to VMEbus. The CPU Space addresses are usually generated automatically by the processor, and not directly specified by the user. Refer to the MC68Ø3Ø User's Manual for CPU space addressing.

4.2.2 EPROM

The EPROM is decoded starting at address FFFØØØØØ. It is either 128Kb or 256Kb in size depending on whether 64K x 8 or 128K x 8 EPROMs are installed. The EPROM is configured as a 16-bit wide (D16), cache inhibited (CI) data port for the processor. It is a read-only resource, and any write access to the EPROM address space will be terminated with a local bus timeout (LTO). The EPROM is automatically selected after any power-up or reset condition to supply the initial stack pointer and program counter to the processor. It will subsequently remain selected until an access to any on-board address is performed.

4.2.3 Static RAM

The local static RAM (SRAM) is decoded at addresses FFF4ØØØØ through FFF47FFF. It is 32Kb in size, and it is configured as an 8-bit wide (D8), cache inhibited (CI) data port for the processor. The static RAM is decoded at sequential byte addresses, and it is accessible with byte, word, or longword operations. The static RAM is not accessible from VSB or VMEbus.

4.2.4 NVRAM/Time-Of Day Clock

The combination nonvolatile RAM and Time-Of-Day clock (NVRAM/TOD) chip is decoded at addresses FFF5ØØØØ through FFF5Ø7FF. It is 2Kb in size, and it is configured as an 8-bit wide (D8), cache inhibited (CI) data port for the processor. The NVRAM/TOD is decoded at sequential byte addresses, and it can be accessed with byte, word, or longword operations. The NVRAM and time-of-day clock are battery backed-up for continuous data retention and clock operation. After power-up, the first write operation to the NVRAM must be used to test the condition of the battery. If the first write is unsuccessful, then the battery voltage is low and the NVRAM/TOD chip should be replaced to ensure nonvolatile operation.

The registers for the time-of-day clock are accessed through the top 8 bytes of the 2Kb NVRAM/TOD address space. The registers are summarized in Table 4-2.

TABLE 4-2. NVRAM/TOD CLOCK REGISTER MAP

Address	Data								Function
	D7	D6	D5	D4	D3	D2	D1	DØ	
FFF5Ø7F8	W	R	S	Ca	Ca	Ca	Ca	Ca	Control
FFF5Ø7F9	ST	-	-	-	-	-	-	-	Seconds (ØØ-59)
FFF5Ø7FA	Ø	-	-	-	-	-	-	-	Minutes (ØØ-59)
FFF5Ø7FB	KS	Ø	-	-	-	-	-	-	Hour (ØØ-23)
FFF5Ø7FC	Ø	FT	Ø	Ø	Ø	-	-	-	Day (Ø1-Ø7)
FFF5Ø7FD	Ø	Ø	-	-	-	-	-	-	Date (Ø1-31)
FFF5Ø7FE	Ø	Ø	Ø	-	-	-	-	-	Month (Ø1-12)
FFF5Ø7FF	-	-	-	-	-	-	-	-	Year (ØØ-99)

Notes: W = Write bit, R = Read bit
S = Calibration Sign bit, Ca = Calibration value (5 bits)
ST = Stop bit, KS = Kick Start, FT = Frequency Test

Setting the "R" bit (R=1) in the TOD control register will latch the current time from the clock in the other TOD registers for reading. Clearing the "R" bit (R=Ø) will enable the continual updating of the TOD registers by the clock with the current time. Setting the "W" bit (W=1) in the TOD control register will enable writing of the other TOD registers by the processor to change the current time. Clearing the "W" bit (W=Ø) will set the clock to the time that was written in the registers. The KS, FT, and zero (Ø) bits in the TOD registers must be written as zero to allow normal clock operation. The 5-bit calibration value (Ca) and the calibration sign bit (S)

can be used to speed up or slow down the clock at a linear rate of approximately 5.35 seconds per month per increment. The time values are encoded in BCD format. Refer to the Thomson/Mostek MK48TØ2 data sheet for a detailed operating description of the NVRAM/TOD clock chip.

4.2.5 Parallel Interface/Timer (PI/T)

The PI/T (MC6823Ø) is decoded at addresses FFF6ØØØØ through FFF6ØØ1F. It is 32 bytes in size, and it is configured as an 8-bit wide (D8), cache inhibited (CI) data port for the processor. The registers of the PI/T are decoded at sequential byte addresses, and they can be accessed with byte, word, or longword operations (with the exception of certain board-defined control bits in the Port A and Port B data registers). The register assignments are summarized in Table 4-3.

The PI/T consists of two logically independent sections: the parallel ports and the counter/timer. The parallel ports are dedicated to the MVME141 hardware, and they must must be properly configured by the user to operate the board. The parallel ports are described in the following section. The counter/timer is not dedicated by the hardware and is available for general user applications. The counter/timer can be operated from the 8MHz clock source of the PI/T chip, or from the counter/timer output pin OP3 of the DUART chip. The PI/T is reset by any power-up or reset condition. Refer to the PI/T User's Manual for a detailed operating description of the PI/T chip.

4.2.5.1 PI/T Port Configuration

The parallel port section of the PI/T is used on the MVME141 for control and status registers (CSRs) and for interrupt control. It must be properly configured to support the board.

The parallel port section consists of Ports A and B, four interrupt/handshake pins (H1, H2, H3, and H4), and Port C which contains two general I/O pins and six dual-function pins. Ports A and B and the Hx pins must be programmed in the PI/T for MODE Ø - SUBMODE 1X operation. The upper six pins of Ports A and B must be programmed as outputs for use as read/write control bits, and the lower two bits of Ports A and B must be programmed as inputs for use as read-only status bits. The H1 and H3 pins should be programmed as edge-activated interrupt sources with an active low asserted pin sense. The H2 and H4 pins should be programmed as edge-activated status inputs with an active low asserted pin sense on H4, and an active high asserted pin sense on H2. The dual-function pins on port C must be programmed in the PI/T for the "non-port" functions except for the DMA pin. The DMA pin and the two general I/O pins on Port C are not used and should be programmed as outputs. The recommended

TABLE 4-3. PI/T ADDRESS MAP

Address	Register	Comments
FFF60000	Port General Control Register	R/W, IV = 32
FFF60001	Port Service Request Register	R/W, IV = 18
FFF60002	Port A Data Direction Register	R/W, IV = FC
FFF60003	Port B Data Direction Register	R/W, IV = FC
FFF60004	Port C Data Direction Register	R/W, IV = 13
FFF60005	Port Interrupt Vector Register	R/W, IV = 40
FFF60006	Port A Control Register	R/W, IV = 82
FFF60007	Port B Control Register	R/W, IV = 82
FFF60008	Port A Data Register	R/W, CSR bits
FFF60009	Port B Data Register	R/W, CSR bits
FFF6000A	Port A Alternate Register	Read-only of Port A pins
FFF6000B	Port B Alternate Register	Read-only of Port A pins
FFF6000C	Port C Data Register	R/W, IV = EC
FFF6000D	Port Status Register (PSR)	R/W, IV = 0F
FFF6000E	Null	Read as zero
FFF6000F	Null	Read as zero
FFF60010	Timer Control Register	R/W, IV = 101xxxx0 (binary)
FFF60011	Timer Interrupt Vector Register	R/W, IV = 45
FFF60012	Null	Read as zero
FFF60013	Counter Preload Register(High)	R/W
FFF60014	Counter Preload Register(Mid)	R/W
FFF60015	Counter Preload Register(Low)	R/W
FFF60016	Null	Read as zero
FFF60017	Count Register(High)	Read-only of count state
FFF60018	Count Register(Mid)	Read-only of count state
FFF60019	Count Register(Low)	Read-only of count state
FFF6001A	Timer Status Register	R/W
FFF6001B	Null	Read as zero
FFF6001C	Null	Read as zero
FFF6001D	Null	Read as zero
FFF6001E	Null	Read as zero
FFF6001F	Null	Read as zero

Notes: IV = Recommended initialization values.
Interrupt vector assignments are for 141Bug.
Timer initialization values are user defined.

configuration values for the PI/T ports are given in Table 4-3. The final configuration values may vary depending on the interrupt requirements of the application.

4.2.5.2 PI/T Port (CSR) Assignments

The MVME141 port assignments for the parallel port section of the PI/T are illustrated in Figure 4-3.

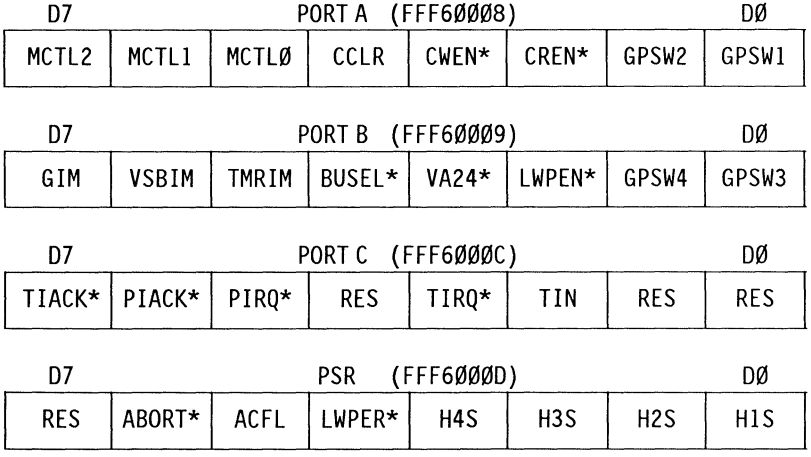


FIGURE 4-3. PI/T PORT (CSR) ASSIGNMENTS

The upper six CSR bits of Ports A and B are used to control the circuitry on the MVME141. There is a timing delay, however, between the writing of the CSR bits and before the bits change at the port pins of the PI/T chip where they become effective on the board. As a result, the following software constraint must be imposed on how the CSR bits are modified to prevent the port pins from changing in the middle of a subsequent processor cycle that they may be controlling.

The CSR bits CCLR, CWEN*, and CREN* of Port A must not be modified with a byte write operation. They should be modified with a word or longword operation performed to the Port A byte address FFF6ØØØ8. The CSR bits BUSEL*, VA24*, and LWPEN* of Port B also must not be modified with a byte write operation. They should be modified with a word operation performed to the Port B byte address FFF6ØØØ9, or with a longword operation performed to the Port A byte address FFF6ØØØ8. A word or longword operation by the software will cause the processor to perform two or four byte operations to the PI/T chip (D8 port) thus protecting the subsequent processor cycles from the

CSR bit changes. If a word operation is used to modify Port A, then the critical bits of Port B must not be changed by the same instruction. If a longword operation is used, then the critical bits of both Ports A and B can be changed by the same instruction.

The bit assignments for the port registers are described below.

MCTLØ-2 < Monitor Control Ø-2>

The Monitor Control bits (MCTLØ-2) select the operating mode of the VMEbus monitor gate-array (cache snooper). They are encoded to select one of eight modes of operation. The operating modes are summarized in the following chart.

MTCL2	MCTL1	MCTLØ	VMEbus Monitor Operating Mode
1	1	1	Normal, Enabled
1	1	Ø	Normal, Disabled
1	Ø	1	Reserved
1	Ø	Ø	Reserved
Ø	1	1	Loopback, Enabled, Fill
Ø	1	Ø	Loopback, Disabled
Ø	Ø	1	Loopback, Enabled, Fill, CC, CI override
Ø	Ø	Ø	Loopback, Enabled, Fill, CC

Note: CC = Continuous Count, CI = Carry-In

The VMEbus monitor gate-array should always be selected for the "Normal, Enabled" mode of operation (MCTLØ-2 = 111) even if the on-board cache is disabled to ensure cache coherency. The "Loopback" modes are provided for diagnostic use only. The VMEbus monitor gate-array is a four level FIFO that captures the addresses of memory locations modified by VMEbus masters in the system and presents them to the cache for processing. During the Normal, Enabled mode of operation, the monitor captures the addresses of memory locations modified by other VMEbus masters in the system. During the Loopback modes of operation, the monitor captures only those VMEbus addresses modified by this MVME141 to allow testing of the monitor independent of the system environment.

CCLR < Cache Clear>

The Cache Clear control bit (CCLR) clears the on-board cache and the VMEbus monitor gate-array. While this bit is asserted (CCLR = 1), the cache and the monitor are held in a cleared and disabled state. When this bit is negated (CCLR = Ø), the cache and the monitor are enabled for the operating modes selected by the cache control bits (CREN*, CWEN*) and the monitor control bits (MCTLØ-2) described in this section.

CWEN* **< Cache Write Enable>**
CREN* **< Cache Read Enable>**

The Cache Write Enable (CWEN*) and Cache Read Enable (CREN*) control bits select the operating mode of the on-board cache. They are encoded to select one of four modes of operation. The operating modes are summarized in the following chart.

CWEN*	CREN*	Cache Operating Mode
Ø	Ø	Enabled (hits/updates allowed)
Ø	1	Virtual Write (test mode)
1	Ø	Virtual Read (test mode)
1	1	Disabled (no hits/updates allowed)

The on-board cache should normally be selected for the "Enabled" mode of operation (CWEN*,CREN* = Ø,Ø) for maximum processor performance. The "Virtual" modes are provided for diagnostic purposes only. Asserting the Cache Write Enable bit (CWEN* = Ø) enables memory accesses by the processor to be stored in the cache. Asserting the Cache Read Enable bit (CREN* = Ø) enables valid data in the cache to hit for the processor. Asserting either control bit but not both selects a Virtual Read or Virtual Write mode of operation for the cache. In the Virtual modes, a read or write cycle that misses or "exits" the cache will be automatically acknowledged to the processor without selecting a target memory device over the VSB or VMEbus. This enables the processor to store any address in the cache and read it back for testing purposes independent of the system memory configuration.

GPSW1-GPSW4 < General Purpose Switches 1-4>

GPSW1 through GPSW4 are read-only status bits that indicate the state of the four general purpose jumpers at jumper block J6 on the board. They can be used as general purpose switches by the firmware or software running on the board to select various program-controlled functions. A GPSWx bit will read as a logic zero for an installed jumper, and as a logic one for a removed jumper. The jumper location assignments for the GPSWx bits are given in Table 2-1. If the 141Bug firmware is installed, refer to the 141Bug User's Manual for the functional assignments for these bits.

GIM **< Global Interrupt Mask>**

GIM is the global interrupt mask bit for all interrupt request signals to the processor (except for the the AC-FAIL interrupt). Asserting GIM (GIM = 1) will unconditionally mask all interrupt requests to the processor except for AC-FAIL. Negating GIM (GIM = Ø) will enable all interrupt requests to the processor that are not otherwise masked in the system.

VSBIM **< VSB Interrupt Mask>**

VSBIM is the interrupt mask bit for the interrupt request signal from the VSB bus. Asserting VSBIM (VSBIM = 1) will mask a VSB interrupt request from generating an interrupt to the processor. Negating VSBIM (VSBIM = Ø) will enable a VSB interrupt request to generate an interrupt to the processor.

TMRIM **< Timer Interrupt Mask>**

TMRIM is the interrupt mask bit for the timer interrupt request signal generated from the counter/timer of the MC68681 DUART. Asserting TMRIM (TMRIM = 1) will mask a timer interrupt request from generating an interrupt to the processor. Negating TMRIM (TMRIM = Ø) will enable a timer interrupt request to generate an interrupt to the processor.

BUSEL* **< Bus Select>**

The Bus Select bit (BUSEL*) controls the routing of off-board accesses to VSB and VMEbus. Negating BUSEL* (BUSEL* = 1) selects the "bounce" mode operation in which an off-board address is first broadcast on VSB and then re-routed to VMEbus if no device is selected by the address. In this mode, the VSB resources effectively select the target bus. Asserting BUSEL* (BUSEL* = Ø) selects "non-bounce" mode operation in which the MVME141 selects the target bus at the start of the access and no "bouncing" is performed. The resulting system address map for bounce mode and non-bounce mode operation is illustrated in Figure 4-1 and Figure 4-2.

VA24* **< VME 24-Bit Address mode>**

The VA24* control bit selects the address mode for VMEbus accesses in the lower 16 megabytes of the address map. Negating VA24* (VA24* = 1) selects the A32 address mode in which one of the extended VMEbus address modifiers ØE, ØD, ØA, or Ø9 will be generated on the bus. These address modifiers specify that the address bits A1 through A31 on the bus contain valid address information. Asserting VA24* (VA24* = Ø) selects the A24 address mode in which one of the standard VMEbus address modifiers 3E, 3D, 3A, or 39 will be generated instead. These address modifiers specify that only the address bits A1 through A23 on the bus contain valid address information, and that the VMEbus address bits A24 through A31 should be ignored by the slave when decoding the address. The specific one of four address modifiers used is determined by the function codes of the processor during the bus access. Any VMEbus access above the lower 16 megabyte boundary of the address map will be performed in A32 mode.

The VA24 control bit allows for mix-mode operation in which A24 and A32 VMEmodules can be used in the same system. There is a similar bit in the VMEchip LCSR called MAS24 which can override the VA24*

control bit and configure the entire VMEbus for A24 (16 megabytes) operation only. Generally, the use of the VA24* control bit is preferred over the MAS24 bit where A24 operation is desired in an A32-capable system.

LWPEN* **< Local Write-Posting Enable>**

LWPEN* is the enable control for the local write-posting interface on the MVME141. Asserting LWPEN* (LWPEN* = Ø) enables the local write-posting interface, and negating LWPEN* (LWPEN* = 1) disables the local write-posting interface. When enabled, the local write-posting interface latches the address and data information for a write cycle to the VSB or VMEbus memory; and it acknowledges the cycle to the processor so that the processor can continue to operate out of cache. The local write-posting interface then continues and completes the write cycle to the target memory independently of the processor. Generally, the local write-posting interface should always be enabled for maximum processor performance.

The local write-posting interface is implemented as discrete circuitry on the MVME141. It is effective for both VSB and VMEbus operations. There is a similar write-posting interface in the VMEchip which is only effective for VMEbus operations. The VMEchip write-posting interface must not be enabled if the VSB bus is operated on the MVME141.

RES/H4S **< Reserved>**

The RES and H4S bits of the Port Status Register (PSR) are reserved. These bits reflect the status of the H4 pin of the PI/T chip which is connected on the board but not used. The H4 pin must be programmed in the PI/T as an input status pin with interrupt generation disabled. The RES bit will always read high by the processor, and the H4S bit may read either high or low.

ABORT*/H3S **< Abort Status>**

The ABORT* and H3S bits of the Port Status Register (PSR) reflect the status of the front panel, **ABORT** pushbutton switch. The ABORT* bit is a read-only status bit that will read high (ABORT* = 1) while the **ABORT** pushbutton is in the released position, and read low (ABORT* = Ø) while the **ABORT** pushbutton is pressed. The H3S bit is an edge-activated, read/clearable status bit that will set to one (H3S = 1) when the **ABORT** pushbutton is pressed. It must subsequently be written with a logic one to clear to a zero. The H3S bit should be programmed in the PI/T to generate an interrupt on the falling-edge assertion of the ABORT* signal on the H3 pin. Generally, the ABORT* bit does not have to be read since the interrupt is edge-activated and uniquely vectored. The H3S bit should be written during interrupt processing to clear the interrupt condition.

ACFL/H2S **< AC Fail Status>**

The ACFL and H2S bits of the Port Status Register (PSR) reflect the status of the AC-FAIL signal on VMEbus. The ACFL bit is a read-only status bit that will read high (ACFL = 1) while the AC-FAIL signal is asserted indicating that power is about to be lost to the system. It will read low (ACFL = Ø) while the AC-FAIL signal is negated. The H2S bit is an edge-activated, read/clearable status bit that will set to one (ACFL = 1) when the AC-FAIL signal asserts. It must subsequently be written with a logic one to clear to a zero. The H2 pin should be programmed in the PI/T as an active high asserted, input status pin with interrupt generation disabled. The AC-FAIL interrupt is already generated and uniquely vectored by other circuitry on the board. As such, the use of the ACFL and H2S bits may be optional.

LWPER*/H1S **< Local Write-Posting Error Status>**

The LWPER* and H1S bits of the Port Status Register (PSR) reflect the status of the bus error signal from the local write-posting interface. The LWPER* bit is a read-only status bit that will always read high (LWPER* = 1) because of the timing of the bus error signal. The H1S bit is an edge-activated, read/clearable status bit that will set to one (H1S = 1) when a local write-posted cycle is terminated with a bus error condition. It must subsequently be written with a logic one to clear to a zero. The H1S bit should be programmed in the PI/T to generate an interrupt on the falling-edge assertion of the LWPER* signal on the H1 pin. The H1S bit should be written during interrupt processing to clear the interrupt condition.

TIACK* **< Timer Interrupt Acknowledge>**
PIACK* **< Port Interrupt Acknowledge>**
PIRQ* **< Port Interrupt Request>**
TIRQ **< Timer Interrupt Request>**
TIN **< Timer Input>**

These signals are the alternate function pins on Port C of the PI/T that are dedicated for the MVME141. They are not control or status bits, but are control signals used by the PI/T for interrupt and timer operation. These signals are shown in Figure 4-3 for reference to show the bit positions in Port C that are dedicated for non-port operation. They are programmed through the Port Service Request Register (PSRR) and Timer Control Register (TCR) of the PI/T. The bit positions of Port C corresponding to these alternate signal functions should be programmed as inputs. The remaining bit positions of Port C are not used and should be programmed as outputs. The TIN signal can be programmed as an optional clock source for the PI/T timer. It is generated by the OP3* output pin of the MC68681 DUART. Note that the TIN clock is rising-edge activated, but that the OP3* pin is falling-edge asserted. Generally, the OP3* signal from the DUART should be programmed as a continuous square wave output when used as the PI/T timer clock.

4.2.6 DUART

The MC68681 DUART is decoded at addresses FFF7ØØØØ through FFF7ØØØF. It is 16 bytes in size, and it is configured as an 8-bit wide (D8), cache inhibited (CI) data port for the processor. The registers of the DUART are decoded at sequential byte addresses, and they can be accessed with byte, word, or longword operations. The register assignments are summarized in Table 4-4.

TABLE 4-4. DUART ADDRESS MAP

Address	Read Cycle	Write Cycle
FFF7ØØØØ	Serial Port A - MODE REG.	Serial Port A - MODE REG.
FFF7ØØØ1	Serial Port A - STATUS REG.	Serial Port A - CLOCK SELECT REG.
FFF7ØØØ2	(Do Not Access)	Serial Port A - COMMAND REG.
FFF7ØØØ3	Serial Port A - RECEIVER REG.	Serial Port A - TRANSMITTER REG.
FFF7ØØØ4	Input Port - CHANGE REG.	AUXILIARY CONTROL REG.
FFF7ØØØ5	Interrupt - STATUS REG.	Interrupt - MASK REG.
FFF7ØØØ6	Counter - CURRENT MSB REG.	Counter/Timer - MSB LOAD REG.
FFF7ØØØ7	Counter - CURRENT LSB REG.	Counter/Timer - LSB LOAD REG.
FFF7ØØØ8	Serial Port B - MODE REG.	Serial Port B - MODE REG.
FFF7ØØØ9	Serial Port B - STATUS REG.	Serial Port B - CLOCK SELECT REG.
FFF7ØØØA	(Do Not Access)	Serial Port B - COMMAND REG.
FFF7ØØØB	Serial Port B - RECEIVER REG.	Serial Port B - TRANSMITTER REG.
FFF7ØØØC	Interrupt - VECTOR REG.	Interrupt - VECTOR REG.
FFF7ØØØD	Input Port - STATUS BUFFER	Output Port - CONFIGURATION REG.
FFF7ØØØE	Counter - Start Command	Output Port - Bit Set Command
FFF7ØØØF	Counter - Stop Command	Output Port - Bit Clear Command

The DUART consists of two serial ports, a 6-bit parallel input port, and an 8-bit parallel output port. Serial port A operates through serial port connector #1 on the front panel (SP1, lower connector), and serial port B operates through serial port connector #2 (SP2, upper connector). The input port and output port on the DUART are reserved for the serial port handshake signals and the timer interrupt clock. They are described in the following section. The crystal frequency used to operate the DUART is the recommended 3.6864 MHz. The DUART is reset by any power-up or reset condition. Refer to the DUART User's Manual for a detailed operating description of the DUART chip.

4.2.6.1 DUART Port Assignments

The bit assignments for the input and output port on the DUART are given in Table 4-5. The port pins are reserved for the serial port handshake signals and the timer interrupt clock. The handshake signals are defined by the RS-232C guidelines for interfacing data terminal equipment. The signal pair RTS/CTS is typically used for hardware flow control between two serial ports. This signal function is automatically managed by the DUART circuitry after appropriately programming the chip. The signal pair DTR/DCD is typically used to indicate the state of presence or readiness between two serial ports. This signal function must be managed by the firmware or software running on the board. Note that the use of these handshake signals may vary with different computer products. The handshake signal DSR is not used by the MVME141. It is pulled up to +12V for both serial ports. The DUART supports change of state detection for the input port pins assigned to CTS and DCD for both serial ports.

TABLE 4-5. DUART PARALLEL PORT ASSIGNMENTS

Register Bit	I/O	Assignment	Comments
OPØ	->	RTS for channel A	1 sets RTS ON for SP1
OP1	->	RTS for channel B	1 sets RTS ON for SP2
OP2	->	DTR for channel A	1 sets DTR ON for SP1
OP3	->	Timer Interrupt Clock	Active low clock
OP4	->	-	not used
OP5	->	DTR for channel B	1 sets DTR ON for SP2
OP6	->	-	not used
OP7	->	-	not used
IPØ	< -	CTS* for channel A	Ø = CTS ON for SP1
IP1	< -	CTS* for channel B	Ø = CTS ON for SP2
IP2	< -	DCD* for channel A	Ø = DCD ON for SP1
IP3	< -	DCD* for channel B	Ø = DCD ON for SP2
IP4	< -	DCD* for channel A	(IP2 replicated)
IP5	< -	DCD* for channel B	(IP3 replicated)

Notes: Channel A uses serial port connector 1 (SP1).
Channel B uses serial port connector 2 (SP2).
IP4 and IP5 do not provide change-of-state detection.

The output port pin OP3 on the DUART is used for the tick-timer clock. A high-to-low signal transition on this pin will generate a timer interrupt to the processor. The timer interrupt is generated by external circuitry on the board, so no DUART processing is

required to handle the interrupt. A tick timer can be implemented by programming a continuous, square wave output on OP3. A counter load value of 48ØØ hex or 78ØØ hex will generate a 1ØØ Hz or 6Ø Hz timer interrupt when the counter/timer is programmed for the timer mode using the 1x clock source. The OP3 pin also connects to the Timer-In (TIN) pin of the MC6823Ø PI/T where it can optional be used as the clock source for the counter/timer in the PI/T.

4.2.7 VSBchip CSR

The MVSB24ØØ VSBchip contains two registers to configure and control the VSB interface on the MVME141. The registers are decoded in the VSBchip at the two longword addresses FFFAØØØØ and FFFAØØØ4. They are configured as a 32-bit wide (D32), cache inhibited (CI) data port for the processor. Table 4-6 lists the VSBchip registers.

TABLE 4-6. VSBchip REGISTERS

Address	Register	Comments
FFFAØØØØ	Control and Status Register (CSR)	16 bits, DØØ-D15
FFFAØØØ4	Block-Transfer Byte-Count Reg.	32 bits
-	Address-Decode Register	not supported

The Control and Status Register (CSR) is used to configure, control, and monitor the operation of the VSB interface. It is 16 bits wide, and it is accessed at the lower 16 bits (DØØ through D15) of longword address FFFAØØØØ. The Block-Transfer Byte Count register is used to control the length of block transfer cycles. A third register in the VSBchip (the Address Decode Register) is not supported on the MVME141 and cannot be accessed by the processor. The VSBchip registers do not decode transfer size information from the processor, so they should be modified with longword operations only. The VSBchip CSR is initialized to FFFF on the MVME141 by a power-up or reset condition to disable the VSB interface. The CSR should be configured after reset to select the desired VSB mode of operation. Refer to the MVSB24ØØ User's Manual for a detailed description of the VSBchip registers and operation.

4.2.7.1 VSBchip Configuration

When configuring the VSBchip for the MVME141, the master interface should generally be enabled if the VSB bus is supported for the board. The system controller function should be enabled if the MVME141 is the left-most bus master on the VSB bus. The bounce mode should always be enabled in the VSBchip and controlled instead through the BUSEL* bit of the PI/T CSR. Bounce mode operation is generally preferred as it provides for the transparent selection of

resources between VSB and VMEbus. The memory map for the MVME141 operating in VSB bounce mode is illustrated in Figure 4-1. Non-bounce mode can be selected to provide a faster access time to VMEbus resources; however, it reconfigures the memory map as illustrated in Figure 4-2. The read-only mode is provided for multiprocessor applications to support cache coherency. The read-only mode forces all write cycles to VMEbus so that other MVME141s in the system can monitor the write operations. (The MVME141 only performs cache monitoring on VMEbus). The read-only mode is generally not required in single processor applications. The block transfer capability of the VSBchip is not readily supported on the MVME141 and is not recommended for use.

The VSBchip CSR is initialized to FFFF by any power-up or reset condition to disable the VSB interface on the MVME141. A CSR value of FEBE can be used to enable the VSB interface for system controller (DØØ) and master operation (DØ6), with bounce mode enabled (DØ4), read-only mode disabled (DØ5), and bus timeout set for 256 microseconds (DØ8, DØ9). Other VSB configurations can also be selected through the VSBchip CSR depending on the application.

4.2.8 VMEchip CSR

The MVME6ØØØ VMEchip contains twenty two registers to configure and control the VMEbus interface on the MVME141. The registers are decoded on the MVME141 at addresses FFFBØØØØ through FFFBØØ2F. They are configured as a 16-bit wide (D16), cache inhibited (CI) data port for the processor. The VMEchip registers are listed in Table 4-7 and Table 4-8.

TABLE 4-7. VMEchip LOCAL CONTROL AND STATUS REGISTERS

Local Address	Register
FFFBØØØ1	System Controller Configuration Register
FFFBØØØ3	Requester Configuration Register
FFFBØØØ5	Master Configuration Register
FFFBØØØ7	Slave Configuration Register
FFFBØØØ9	Timer Configuration Register
FFFBØØØB	Slave Address Modifier Register
FFFBØØØD	Master Address Modifier Register
FFFBØØØF	Interrupt Handler Mask Register
FFFBØØ11	Utility Interrupt Mask Register
FFFBØØ13	Utility Interrupt Vector Register
FFFBØØ15	Interrupt Request Register
FFFBØØ17	Status/ID Register
FFFBØØ19	Bus Error Status Register
FFFBØØ1B	GCSR Base Address Register

TABLE 4-8. VMEchip GLOBAL CONTROL AND STATUS REGISTERS

Local Address	Global Offset	Register
FFFBØØ21	Ø1	Global Register Ø
FFFBØØ23	Ø3	Global Register 1
FFFBØØ25	Ø5	Board Identification Register
FFFBØØ27	Ø7	General Purpose Register Ø
FFFBØØ29	Ø9	General Purpose Register 1
FFFBØØ2B	ØB	General Purpose Register 2
FFFBØØ2D	ØD	General Purpose Register 3
FFFBØØ2F	ØF	General Purpose Register 4

Notes: Global Offset is selected by VMEbus A1-A3
Global address = SHIO/Header J1/LCSR Reg 1B/A1-A3

The VMEchip registers are divided into two sets: the Local Control and Status Registers (LCSR) and the Global Control and Status Registers (GCSR). The LCSR registers are used to configure, control, and monitor the operation of the VME interface. These registers are only accessible by the local processor. The GCSR registers are used in multiprocessor applications for communication and control. These registers are accessible by the local processor through the local address map, and also by other processors in the system through the VMEbus Short I/O address space. The global address of the GCSR in the VMEbus Short I/O space is determined by the jumper settings of jumper block J1 and the contents of the GCSR Base Address Register in the LCSR (register 1B).

The VMEchip registers are organized as 8-bit registers on the odd byte section (DØ through D7) of the word port (DØ through D15). They should be accessed by the processor with byte operations at odd byte addresses or with word operations at aligned word addresses. The VMEchip registers are initialized by a power-up or reset condition to select a minimum operating configuration for the VMEbus interface. They should be reconfigured after reset as necessary to select the desired VMEbus mode of operation. Refer to the VMEchip User's Manual for a detailed description of the VMEchip registers and operation.

4.2.8.1 VMEchip Configuration

The four LCSR registers $Ø5, $Ø7, $ØB, $ØD of the VMEchip control functions that are either not supported on the MVME141, or are controlled dynamically through other circuitry on the board. These registers are initialized to their desired state after reset, and they generally should not be modified by the processor. The following exceptions or clarifications should be noted.

The write-posting interface in the VMEchip must not be used if the VSB bus is supported, but it can be used in a VMEbus-only environment. Unaligned transfers by the master interface can be enabled if supported by the slave modules on VMEbus. A24 operation should generally be controlled through the PI/T CSR bit VA24 instead of through the VMEchip. The VA24 bit of the PI/T allows for mix-mode operation in which A32 and A24 resources can still be accessed over VMEbus. D16 operation must not be selected if caching is performed over VMEbus. The MVME141 on-board cache only supports caching from D32 data ports. If D16 mode is selected, the on-board cache will not operate properly. Note that the MVME141 provides a pre-decoded D16 address space in the noncacheable section of the address space for D16 resources. Cache-filling may or may not to be selected. It is automatically performed on the MVME141 for cacheable addresses before either the VSB or VMEbus interface is selected. The address modifiers should not be overridden by the LCSR registers. They are dynamically configured by the circuitry on the board on a cycle by cycle basis. No CSR bits concerning the slave interface should be enabled. The slave interface is not supported on the MVME141 (except for accesses to the GCSR).

The remaining functions of the VMEchip should be configured through the LCSR as required according to the application of the board. These functions include the interrupt controls, the arbiter mode, the requester level and request/release mode, the GCSR base address, and the cycle timeout parameters. The interrupt control bits power-up masking the VMEchip and VMEbus interrupt sources. The arbiter powers-up selecting priority mode arbitration. It is automatically enabled or disabled for operation by the system controller jumper at jumper block J1 on the board. The requester powers-up configured for request level 3 and Release-On-Request (ROR) operation. The local timeout timer is initially disabled. It should be enabled by the processor after start-up. The MVME141 uses the local timeout timer of the VMEchip to perform the watchdog timer function for processor cycles to the local resources except for the cache and FPC. The GCSR should be configured as required for multiprocessor applications.

4.2.9 VSB/VMEbus

The VSB and VMEbus interfaces are selected for any processor address that does not decode a local (on-board) resource. The address ranges for the bus interfaces are listed in Table 4-1. The selection between the VSB and VMEbus interface is controlled by the bus select bit BUSEL* of the PI/T CSR. For BUSEL* = 1, the VSB interface is operating in "bounce" mode in which a processor address is first broadcast on VSB. If a resource is selected by the address, then that resource completes the cycle for the processor. If all the resources acknowledge that they are not selected by the address, then the cycle is re-routed or "bounced" to VMEbus. The resources

on VSB effectively select the target bus interface for the processor thus allowing for the transparent selection of system resources. The address map for bounce mode operation is illustrated in Figure 4-1. For BUSEL* = Ø, the VSB interface is operating in "non-bounce" mode in which the MVME141 selects the target bus at the start of the processor cycle, and no bouncing from VSB to VMEbus is performed. In this mode, the MVME141 uses an on-board address decoder to determine which bus interface is selected. The MVME141 alternates the decoding of the bus interfaces for each 16 megabytes of address space up to FØØØØØØØ. Above this address, VMEbus is decoded. The address map for non-bounce mode operation is illustrated in Figure 4-2.

4.2.9.1 VSB

The VSB interface is always configured for an address size of 32 bits (A32). The VSB address space code 11 (system address space) is used for non-CPU Space accesses by the processor (FC = Ø-6). The VSB Space Code ØØ is used for interrupt acknowledge cycles by the processor, and the code Ø1 (alternate address space) is used for non-IACK CPU space cycles. The data size is configured dynamically by the responding slave resource. Only D32 resources should be located in the cacheable address space to support the MVME141 on-board cache. Noncacheable resources on VSB should be located in the noncacheable areas of the MVME141 address map, or they should be configured as noncacheable through the cache inhibit (CI) bit of the PMMU page descriptors. The cache inhibit signal on VSB is not supported by the MVME141. The VSB interface is controlled by the MVSB24ØØ VSBchip. Refer to sections 4.2.7 and 4.2.7.1 for a description of the VSBchip registers and configuration.

4.2.9.2 VMEbus

The VMEbus interface is configurable for A32, A24, and A16 operation, and for D32 and D16 operation. The address and data size used is hard-decoded on the MVME141 according to the processor address. The address ranges of the MVME141 for the various VMEbus configurations are given in Table 4-1 and illustrated in Figure 4-1 and Figure 4-2. The hard-decoded address ranges enable different address and data size VMEmodules to be used in the same system without having to configure the entire VMEbus system to suit the smallest module. The VMEbus Address Modifiers are generated dynamically by the MVME141 based on the hard-decoded VMEbus address size for each cycle. The lower three bits of the address modifiers are buffered from the function codes of the processor. Only D32 resources should be located in the cacheable address space of the MVME141 to support the on-board cache. Noncacheable resources on VMEbus should be located in the noncacheable areas of the MVME141 address map, or they should be configured as noncacheable through the cache inhibit (CI) bit of the PMMU page descriptors. Certain

limitations apply for D16 resources on VMEbus (refer to section 4.5.2). The VMEbus interface is controlled by the MVME6ØØØ VMEchip and by the VA24* bit of the PI/T CSR. Refer to sections 4.2.8 and 4.2.8.1 for a description of the VMEchip registers and configuration.

4.2.9.3 VMEbus Short I/O

The VMEbus Short I/O (SHIO) space is selected in the processor address range FFFFØØØØ through FFFFFFFF. It is an alternate 64Kb space on VMEbus that uses only the lower 16 bits of the address bus to simplify decoding. This space is typically used for CSRs and other I/O devices on VMEbus that can occupy small address ranges. During Short I/O accesses, the MVME141 generates one of the two VMEbus short address modifiers 2D or 29. The particular address modifier used is determined by the function codes of the processor. The Short I/O space is configured as a 16-bit wide (D16), cache inhibited (CI) data port for the processor.

4.3 INTERRUPT HANDLING

The MVME141 supports 21 interrupt requests to the processor. The interrupt requests are prioritized by the interrupt handler circuitry on the board into seven interrupt request levels with three prioritized groups per level. The interrupt prioritization is such that any higher level interrupt will take precedence over any lower level interrupt, and any higher group interrupt on a given level will take precedence over any lower group interrupt on the same level. The interrupt sources and their prioritizations are given in Table 4-9.

TABLE 4-9. MVME141 INTERRUPT ASSIGNMENTS

Level		(Highest) Group 3	Group 2	(Lowest) Group 1
7	-	ACFAIL (1F)	PITPRT (4Ø,42)	WPERR (67), VIRQ7
6	-	TCKTMR (1E)	PITTMR (45)	SYSFAIL (66), VIRQ6
5	-	VSBIRQ (1D)	DUART (44)	SIGHP (65), VIRQ5
4	-			LOCMON1 (64), VIRQ4
3	-			VMEIACK (63), VIRQ3
2	-			LOCMONØ (62), VIRQ2
1	-			SIGLP (61), VIRQ1

Notes: PITPRT contains LWPER and ABORT.
() specify vector assignments for 141Bug.

Interrupt level 7 is the highest priority interrupt level, and interrupt group 3 is the highest priority group on each level. The group 3 interrupts are handled by the interrupt handler circuitry on the board. Their associated interrupt vectors are auto-vectored in the processor. The group 2 interrupts are generated by the PI/T and DUART chips. Their associated interrupt vectors are supplied by the respective chips. The group 1 interrupts are either generated by the VMEchip, or they are passed through the VMEchip to the processor from VMEbus. Their associated interrupt vectors are either supplied by the VMEchip, or they are accessed over VMEbus from the interrupting VMEmodule. All interrupt requests except ACFAIL have an associated interrupt mask bit on the board that can be used to mask the interrupt to the processor. In addition, all interrupt requests except ACFAIL can be simultaneously masked with the global interrupt mask bit GIM in the PI/T CSR. The interrupts are described in the following sections.

4.3.1 AC-Fail Interrupt (ACFAIL)

The AC-Fail interrupt (ACFAIL, level 7, group 3) is generated by the ACFAIL* signal on VMEbus. This signal asserts when AC power has been lost at the system power supply. It indicates that a minimum of 2 milliseconds of operating time is left before DC power will be lost to the system. The AC-Fail interrupt will remain asserted to the processor for as long as the ACFAIL* signal is asserted on the bus. It is not maskable by any CSR bit on the board. The state of the ACFAIL* signal on VMEbus can be read during interrupt processing through the PI/T CSR if required. The AC-Fail interrupt is generated and uniquely vectored by discrete circuitry on the board. The AC-Fail interrupt is auto-vectored to the processor with interrupt vector 1F hex (vector table offset Ø7C).

4.3.2 Tick-Timer Interrupt (TCKTMR)

The Tick-Timer interrupt (TCKTMR, level 6, group 3) is triggered by a high-to-low signal transition on output port pin OP3 of the DUART. The signal transition is latched-up by discrete interrupt circuitry on the board to generate an interrupt to the processor. The interrupt is automatically cleared during the interrupt acknowledge vector fetch by the processor. As such, no interrupt processing is required by the processor to identify and handle the tick-timer interrupt. The tick-timer interrupt may already be asserted after a power-up or reset condition. The firmware should clear it if necessary during the power-up initialization of the board, or keep it masked until ready for use. The tick-timer interrupt can be individually masked with the TMRIM bit of the PI/T CSR. When this external tick-timer interrupt source is used, the internal counter/timer interrupt source in the DUART chip should be masked. The tick-timer interrupt is auto-vectored to the processor with interrupt vector 1E hex (vector table offset Ø78).

Note that the tick-timer interrupt is separate from the DUART interrupts, although it is triggered by the counter/timer in the DUART chip. If the tick-timer and serial port interrupts were handled through the same interrupt request signal of the DUART, then it is possible that a tick-timer interrupt could be missed while servicing the serial ports. Generally, the reverse is not true since the receiver data registers of the serial ports are multiply buffered. It is generally recommended that the external tick-timer interrupt (TCKTMR) be used, and that the internal counter/timer interrupt source in the DUART chip remain masked if tick-timer operation is required.

Note that the counter/timer in the DUART could be used for counter/time applications other than a tick-timer if desired. Also, the counter/timer interrupt source in the DUART could be used instead of the external tick-timer (TCKTMR) interrupt if desired. For this mode, the external tick-timer interrupt should remain masked, and the internal counter/timer interrupt in the DUART should be enabled.

4.3.3 VSB Interrupt (VSBIRQ)

The VSB Interrupt Request (VSBIRQ, level 5, group 3) is generated by the IRQ* signal from VSB bus. It can be individually masked with the VSBIM bit of the PI/T CSR. During the interrupt acknowledge cycle by the processor, an interrupt acknowledge cycle is first broadcast on VSB bus to read the interrupt vector from the interrupting module. If there is no responding module to supply the interrupt vector, then the interrupt acknowledge cycle is auto-vectored to the processor with interrupt vector 1D hex (vector table offset Ø74).

4.3.4 PI/T Port Interrupt (PITPRT)

The PI/T Port Interrupt (PITPRT, level 7, group 2) is generated by the programmable interrupt sources of the port section of the PI/T chip. The PI/T port interrupt should be programmed to assert for local write-post bus errors through the port handshake pin H1, and for the ABORT pushbutton switch through the port handshake pin H3. The programming requirements for the port handshake pins are described in section 4.2.5.1 and section 4.2.5.2. Each of the interrupt sources for the port interrupt are individually maskable in the PI/T. The interrupt vectors for the port interrupt are supplied by the PI/T. The 141Bug firmware, if installed, will initialize the base interrupt vector for the port to 4Ø hex to generate an interrupt vector of 4Ø hex (vector table offset 1ØØ) for the local write-post bus error interrupt, and 42 hex (vector table offset 1Ø8) for the abort interrupt. The two interrupt vectors 41 hex and 43 hex would be reserved for the two handshake pins that are not programmed as interrupt sources.

The local write-post bus error interrupt (LWPER) is generated when a write-posted cycle to VSB or VMEbus is terminated with a bus error condition. This bus error condition must be treated as an interrupt since the processor is not interlocked to the write-posted cycle, and will be executing further down the program stream when the bus error occurs. Generally, the software should treat the write-post bus error interrupt with the same significance as a true bus error exception, with the exception that the software may not be able to determine the actual address that caused the bus error. (The bus error address will always be the previous write cycle from where the interrupt was asserted to the processor). During interrupt processing, the H1S bit of the PI/T PSR register should be written with a one to clear the interrupt condition. The abort interrupt is generated by the **ABORT** pushbutton switch located on the front panel of the MVME141. It is an edge-activated event that is triggered when the **ABORT** pushbutton is pressed. During interrupt processing, the H3S bit of the PI/T PSR register should be written with a one to clear the interrupt condition.

4.3.5 PI/T Timer Interrupt (PITTMR)

The PI/T Timer Interrupt (PITTMR, level 6, group 2) is generated by the programmable counter/timer in the the PI/T chip. The counter/timer is a 24-bit, synchronous down counter that can be programmed to generate an interrupt for each count to state zero. The timer interrupt can be individually masked in the PI/T. The interrupt vector for the timer interrupt is supplied by the PI/T. The 141Bug firmware, if installed, will initialize the timer interrupt vector to 45 hex (vector table offset 114 hex). Refer to the MC68230 User's Manual for a detailed description of the counter/timer of the PI/T.

4.3.6 DUART Interrupt (DUART)

The DUART interrupt (DUART, level 5, group 2) is generated by the various programmable interrupt sources of the DUART chip. The interrupt sources are associated with the two serial ports, the input port, and the counter/timer. The input port signals are connected to the CTS and DCD signals of the two front-panel serial ports. They can be programmed to generate a change-of-state interrupt on the serial port's flow control or connect/disconnect status. The interrupt sources for the DUART interrupt can be individually masked in the DUART. The on-chip counter/timer interrupt should generally remain masked when the off-chip tick-timer interrupt is used (refer to section 4.3.2). The interrupt vector for the DUART interrupt is supplied by the DUART. The 141Bug firmware, if installed, will initialize the interrupt vector to 44 hex (vector table offset 110 hex). Refer to the DUART User's Manual for a detailed description of the DUART, and to section 4.2.6.1 for the DUART port assignments.

4.3.7 VMEchip/VMEbus Interrupts

All of the group 1 interrupts are generated by the VMEchip or by the VMEbus interrupt request lines. The VMEchip can generate a utility interrupt request for a VMEchip write-post bus error condition (WPERR), the SYSFAIL signal on VMEbus, either of two location monitors (LOCMON1, LOCMONØ), a high and low priority attention interrupt from the GCSR (SIGHP, SIGLP), and to indicate the acknowledging of an interrupt acknowledge cycle (VMEIACK). The VMEchip will also pass the interrupt request lines from VMEbus (VIRQ1 through VIRQ7) to the processor at the same interrupt request levels as they are on VMEbus. Each of the interrupt sources can be individually masked in the VMEchip. The interrupt vectors for the VMEbus interrupts are accessed from the interrupting VMEmodule over VMEbus. The interrupt vectors for the VMEchip utility interrupts are supplied by the VMEchip. The 141Bug firmware, if installed, will initialize the base vector register for the utility interrupts to 6Ø hex (vector table offset starting at 184 for SIGLP). The corresponding utility interrupt vectors are given in Table 4-9. Refer to the VMEchip User's Manual for a detailed description of the VMEchip utility interrupts.

4.4 INTERRUPT GENERATION

The MVME141 supports a programmable, 7-level, VMEbus Interrupter through the VMEchip. The VMEbus Interrupter is programmed through the LCSR of the VMEchip. Refer to the VMEchip User's Manual for a detailed description of interrupter operation and the LCSR.

4.5 CACHE/WRITE-POSTING MANAGEMENT

The local cache and write-posting interface on the MVME141 are hardware modules designed to maximize the performance of the processor. They are software transparent to the operation of the processor in that no software interaction is required to control the cache and write-posting interface during normal operation. The cache and write-posting interface, however, do constrain where resources can be addressed in the memory map, and affect bus error exception handling and certain memory sizing routines or other routines that rely on bus error exceptions during write operations. These constraints are described in the following sections.

4.5.1 Resource Addressing

The MVME141 performs three functions associated with the cache architecture of the board that affect where resources can be addressed on VSB and VMEbus. The functions are caching, write-posting, and longword-filling. These functions are only enabled in the cacheable sections of the MVME141 address map.

The cacheable sections of the MVME141 address map are those addresses in the bottom half of the address map (ØØØØØØØØ through 7FFFFFF) that are not cache-inhibited by the cache-inhibit bit (CI) of the PMMU page descriptor tables. Only those resources that are correct for caching, write-posting, and longword-filling should be located in these cacheable areas. Any resource that should not be cached from, write-posted to, or longword-filled from should be located in the top half of the address map (8ØØØØØØØ through FFFFFFFF), or they should be decoded as noncacheable through the CI bit of the PMMU page descriptor tables.

Caching, write-posting, and longword-filling are disabled in the noncacheable sections of the MVME141 address map irregardless of the CSR bits that control their functions. Caching and write-posting can be disabled in the cacheable sections of the map through the control bits of the PI/T CSR if required. (Generally they should always be enabled for maximum processor performance.) Longword-filling is always enabled in the cacheable sections of the address map, and it cannot be disabled through the PI/T CSR. Longword-filling is the reading of a longword-aligned, 4-byte unit of data irregardless of how few bytes the processor is requesting. It is used to guarantee that all four bytes are supplied for each longword entry of the cache.

Caching, write-posting, and longword-filling are also controlled by the type of cycle being run by the processor. Caching is enabled for program and data accesses only. Write-posting is enabled for data accesses only (FC1=Ø), but not for certain misaligned transfers. Longword-filling is enabled for all cycle types except for CPU-space cycles. Caching, write-posting, and longword-filling are all disabled for RMC cycles.

The on-chip cache of the processor is enabled for caching by the same parameters as the on-board cache provided the on-chip data cache is not operated in write allocate mode. If write allocate mode is used, caching by the on-chip data cache must be controlled by the CI bit of the PMMU page descriptor tables. The on-chip cache is also controlled through the CSR control bits in the MC68Ø3Ø register set.

4.5.2 Data Port Restrictions

The on-board cache and write-posting interface only supports 32-bit size (D32) data ports. As such, only D32 size data ports should be located in the cacheable sections of the address map. D16 and D8 size data ports must be located in the noncacheable sections of the address map (refer to section 4.5.1) with the following restriction.

D16 resources on VMEbus are treated differently than those on VSB. The MVME141 must decode where the D16 resources can be located on VMEbus to generate the proper acknowledge to the processor.

Generally, a D16 resource should only be located in the pre-decoded D16 address space of the noncacheable section of the address map for proper operation (refer to section 4.2.9.2). A D16 resource on VMEbus could be located in a D32 address space; however, all accesses to it will be acknowledged to the processor as a D32 (longword) port. For this configuration, the software would have to restrict all accesses to the D16 resource to aligned word and byte operations. Within this constraint, a D16 resource could be located in the lower half of the address map (ØØØØØØØØ through 8ØØØØØØØ) if it is declared noncacheable through the CI bit of the PMMU page descriptors.

4.5.3 Dual-Port and I/O Resources

Dual-port memory resources must be evaluated as to whether they can be located in the cacheable section of the MVME141 address map. The MVME141 only provides cache monitoring over VMEbus. If a dual-port resource has a port through which another device can modify the memory resource without the MVME141 being able to monitor this over VMEbus, then that resource must be located in the noncacheable section of the MVME141 address map.

An example of this is another VMEmodule which contains a processor and on-board memory which is shared with VMEbus. If the MVME141 were to cache data from this memory through the VMEbus port, then the other processor could modify that memory at a later time through its own "private" port. The MVME141 cache would now contain "stale" data, and a system software error could result. The solution is to address the memory resource on VMEbus in the top half of the MVME141 address map (8ØØØØØØØ through FFFFFFFF), or to decode the memory resource as noncacheable through the cache-inhibit bit (CI) of the PMMU page descriptor tables.

A dual-port VSB/VMEbus memory resource, however, is correct in the cacheable section of the address map if the MVME141 is the only master that can modify the memory over the VSB bus. Any other device that modifies the memory will do so over VMEbus which is monitored for the cache. An example of such a device might be a disk controller that could write a new page from disk to memory over VMEbus at memory locations that had been previously cached. The cache monitor would be able to capture all of the addresses that are modified over VMEbus, and so present them to the cache for comparison and invalidation if any match.

Note that the cache monitor on the MVME141 allows for software transparent operation of the on-board cache by continually monitoring the addresses modified by other devices on VMEbus. The on-chip data cache on the processor, however, is not monitored. It must be managed by the software to prevent stale data from being generated in the cacheable sections of the MVME141 address space.

The on-chip cache is protected from stale data in the noncacheable sections of the MVME141 address map. Any address that is noncacheable for the on-board cache is automatically decoded as noncacheable for the on-chip cache by the circuitry on the board.

An I/O device must never be cached by the MVME141. The data read from an I/O device such as a serial I/O chip or a disk controller chip may change in real-time on each read. If that data were cached, then stale data would result. I/O devices should always be located in the noncacheable sections of the MVME141 address map.

4.5.4 Bus Error Handling

The cache and write-posting interface must be properly managed for bus error handling and for cases where bus error conditions may be expected. The on-board cache does not log the fact that a bus error occurred. If a bus error occurs on an access, that access is stored in the on-board cache as valid data. A subsequent read from that errant address will hit in the on-board cache and complete successfully for the processor. During bus error processing, the processor should clear the on-board cache (or invalidate the known cache entry by replacement) to remove the stale data.

The on-chip data cache in the processor also does not log bus-error conditions during write operations. The on-chip data cache should be handled similarly.

There are certain applications that look for bus error conditions during write operations. A memory sizing routine, for example, may combine memory sizing with memory initialization when sizing a parity memory system. It could continually write to incrementing memory addresses until a bus error is encountered indicating the end of memory. Another example is a routine that writes to a device to determine if it is installed in the system. For these applications, the write-posting interface may affect the operation of the program.

A bus error condition that occurs for a write-posted cycle is reported to the processor as a level 7 interrupt, and not as a bus error exception. When the processor takes the interrupt, it will generally not be able to determine the address that caused the bus error. For applications where bus error conditions are expected, it is recommended that the write-posting interface be disabled so that the actual bus-errored address can be determined. These types of applications generally occur only during the initialization of a system, and not during the normal operation of a system.

The bus error exception taken because of a PMMU page-fault is not detected outside of the processor chip. These bus error conditions will not affect the cache or write-posting interface.

4.6 BUS ERROR STATUS

A bus error exception can be asserted to the processor on the MVME141 for a local bus timeout, a VSB timeout, a VMEbus timeout, or for a bus error exception asserted by a VSB or VMEbus resource. The bus error exceptions are asserted to the processor by the VSBchip and the VMEchip. The source of a bus error can be determined by the processor through the CSR of the VSBchip and the bus error status register in the VMEchip.

In the VSBchip CSR (address FFFAØØØØ), bit D15 will clear to zero for any VSB bus error condition asserted to the processor, and bit D12 will clear to zero for a VSB timeout only. These bits should be written with a one if asserted during bus error processing to reset the bus error status. In the VMEchip bus error status register (address FFFBØØ19), bit D2 will set to one for any VMEbus bus error condition asserted to the processor, bit D1 will set to one for a VMEbus access timeout, and bit DØ will set to one for a local bus timeout condition. The VMEchip local timout also operates for VSB accesses. These bits are updated to indicate the status of the last bus error condition only, and any read from this VMEchip register will automatically clear the bus error status. Refer to the VSBchip and VMEchip User's Manuals for a detailed description of their respective bus error controls. A bus error exception taken by the processor for a PMMU page fault is not detected outside of the processor chip. This exception will not set any of the bus error status bits on the board.

4.7 RMC OPERATION

RMC operations are sequences of read and write cycles by the processor that should complete without interruption from other devices in the system. The processor will signal an RMC operation during the TAS, CAS, and CAS2 instructions, and during all PMMU tablewalk operations.

To ensure uninterrupted RMC operation over VMEbus, the VMEchip will perform all byte RMC operations (TAS and byte-size CAS) as single address, single address strobe cycles. Word and longword CAS and CAS2 operations are performed as multiple address, multiple address strobe cycles, and are not protected against interruption over VMEbus.

To ensure uninterrupted RMC operation over VSB, the VSBchip will maintain ownership of the VSB bus for any RMC operation by the processor. The MVME141 also asserts the LOCK* signal on VSB during RMC operations to lock a dual-port resource from being accessed by another device through a "hidden" or private port on the other board. For VSB operating in bounce mode, all RMC operations are automatically routed to VMEbus to prevent a lock-up condition that

would occur if the VSB interface were also operating in read-only mode.

4.8 RESET OPERATION

The MVME141 has five sources of reset. They are the SYSRESET* signal on the VMEbus, the reset bit in the LCSR in the VMEchip, the **RESET** pushbutton on the front panel, the RESET instruction of the processor, and the Reset and Hold bit (R&H) of the GCSR in the VMEchip. All of the resets are integrated through the VMEchip to reset the local devices, the devices on the VMEbus, or both.

The SYSRESET* signal on the VMEbus, when asserted, will reset all devices on the MVME141 including the processor and the VMEchip. This signal will also reset all devices in the VMEbus system. The reset bit in the LCSR (bit D1 at FFFBØØØ1), when set, will assert the SYSRESET* signal on the VMEbus which will reset the MVME141 and all devices on the VMEbus. This bit is effective whether or not the MVME141 is jumpered as the VMEbus system controller. The **RESET** pushbutton, when pressed, will reset all devices on the MVME141; and if the MVME141 is jumpered as the VMEbus system controller, it will assert the SYSRESET* signal to reset all devices on the VMEbus. The RESET instruction, when executed, will reset the devices on the MVME141 except for the processor. The RESET instruction will not assert the SYSRESET* signal on the VMEbus. The Reset and Hold bit in the GCSR (bit D7 at GCSR register offset $Ø1), while set, will hold the local devices on the MVME141 in reset. The R&H bit can be set and cleared by other bus masters on the VMEbus for multiprocessor applications. It is also clearable by the SYSRESET* signal. Refer to the VMEchip User's Manual for a detailed description of the VMEchip reset controls.

Any reset condition that asserts a reset to the local devices on the MVME141 will cause the VSB and VMEbus interfaces to be disabled for subsequent processor cycles. The local resources will be decoded instead for any processor address so that the local EPROM can supply the initial program counter and stack pointer for post-reset operation of the processor. Any subsequent processor access that specifically addresses a local resource will clear the local "ghost" decode function and re-enable the system busses. As such, a reset instruction must only be executed from local memory (EPROM or SRAM) since the subsequent program instructions will not be immediately accessible from off-board memory.

CHAPTER 5 - SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the connector signal descriptions, parts list, parts location diagram, and schematic diagram for the MVME141.

5.2 INTERCONNECT SIGNALS

The MVME141 uses the P1 and P2 backplane DIN connectors to interconnect with the VMEbus and VSB, and to power the board. The MVME141 uses the J4 and J5 front panel DB-9 connectors to interconnect with serial I/O equipment. The locations of the connectors on the MVME141 are illustrated in Figure 5-1. The connectors are described in the following sections.

5.2.1 P1/P2 Connectors

The P1 and P2 connectors are used to interconnect the the VMEbus and VSB bus, and to power the module. Both connectors are standard DIN, triple row, 96-pin male connectors. The VMEbus signals occupy the P1 connector and the center row of the P2 connector. The VSB signals occupy the two outer rows of the P2 connector. The pin assignments, signal mnemonics, and signal descriptions for the two connectors are provided in Tables 5-1 through 5-4. Refer to the VMEbus Specification and the VSB Specification for a complete description of the interconnect signals.

5.2.2 J4/J5 Connectors

The J4 and J5 connectors are used to interconnect to the two serial ports of the MC68681 DUART. Both connectors are standard DB-9 female connectors that are located on the front panel of the MVME141. Connector J5 (Serial Port 1) connects to serial port A of the MC68681, and connector J4 (Serial Port 2) connects to serial port B. The signals on J4 and J5 are RS-232 compatible. The pin assignments, signal mnemonics, and signal descriptions for the two connectors are provided in Tables 5-5 and 5-6. Refer to the RS-232-C EIA Standard specification and the MC68681 User's Manual for a detailed description of the serial port signals. The parallel port assignments for the MC68681 are described in section 4.2.6.1. The cabling information for the connectors is provided in section 2.6.5.

TABLE 5-1. CONNECTOR P1 PIN ASSIGNMENTS

Pin Number	Row A Signals	Row B Signals	Row C Signals
1	DØØ	BBSY*	DØ8
2	DØ1	BCLR*	DØ9
3	DØ2	ACFAIL*	D1Ø
4	DØ3	BGØIN*	D11
5	DØ4	BGØOUT*	D12
6	DØ5	BG1IN*	D13
7	DØ6	BG1OUT*	D14
8	DØ7	BG2IN*	D15
9	GND	BG2OUT*	GND
1Ø	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BRØ*	SYSRESET*
13	DSØ*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AMØ	A22
17	GND	AM1	A21
18	AS*	AM2	A2Ø
19	GND	AM3	A19
2Ø	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	AØ7	IRQ7*	A14
25	AØ6	IRQ6*	A13
26	AØ5	IRQ5*	A12
27	AØ4	IRQ4*	A11
28	AØ3	IRQ3*	A1Ø
29	AØ2	IRQ2*	AØ9
3Ø	AØ1	IRQ1*	AØ8
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

Note: The MVME141 does not connect to SERCLK, SERDAT, or +5VSTDBY.

TABLE 5-2. CONNECTOR P1 SIGNAL DESCRIPTIONS

Pin Number	Signal Mnemonic	Signal Name and Description
A1-A8	DØØ-DØ7	DATA BUS (bits Ø-7) - Eight of 16 three-state, bidirectional data bus signals on P1. (The expanded 16 signals of the data bus are found on connector P2).
A9	GND	GROUND
A1Ø	SYSCLOCK	SYSTEM CLOCK - A free-running, 16 MHz clock signal driven by the system controller.
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - A three-state signal driven by the master whose falling-edge initiates a data transfer with the slave. A low level indicates for byte/word transfers that the data transfer will occur on data bus signals DØ8 through D15.
A13	DSØ*	DATA STROBE Ø - A three-state signal driven by the master whose falling-edge initiates a data transfer with the slave. A low level indicates for byte/word transfers that the data transfer will occur on data bus signals DØØ through DØ7.
A14	WRITE*	WRITE - A three-state signal driven by the master that indicates the data transfer is a write cycle to the slave when low, or a read cycle from the slave when high.
A15	GND	GROUND
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - An open-collector signal driven by the slave. A falling edge indicates that the slave has driven valid data on the data bus during a read cycle, or that the slave has received valid data from the data bus during a write cycle. A low level indicates the slave may be active on the data bus.
A17	GND	GROUND

TABLE 5-2. CONNECTOR P1 SIGNAL DESCRIPTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A18	AS*	ADDRESS STROBE - A three-state signal driven by the master whose falling-edge indicates a valid address is on the address bus. A low level indicates ownership of VMEbus and the slave resource.
A19	GND	GROUND
A2Ø	IACK*	INTERRUPT ACKNOWLEDGE - A three-state signal driven by the master that indicates an interrupt acknowledge cycle.
A21	ACKIN*	(INTERRUPT) ACKNOWLEDGE INPUT - The ACKIN* and ACKOUT* signals form an interrupt acknowledge daisy-chain to select the interrupting device to supply an interrupt vector.
A22	ACKOUT*	(INTERRUPT) ACKNOWLEDGE OUTPUT - The ACKIN* and ACKOUT* signals form an interrupt acknowledge daisy-chain to select the interrupting device to supply an interrupt vector.
A23	AM4	ADDRESS MODIFIER (bit 4) - One of six three-state signals driven by the master that specify information about the bus cycle including address size and cycle type.
A24-A3Ø	AØ7-AØ1	ADDRESS BUS (bits 7-1, reverse ordered) - Seven of 23 three-state driven address bus signals on P1. (The extended 8 signals of the address bus are found on connector P2).
A31	-12V	-12 Vdc POWER
A32	+5V	+5 Vdc POWER
B1	BBSY*	BUS BUSY - An open-collector signal driven by the bus master to indicate ownership of VMEbus.
B2	BCLR	BUS CLEAR - A totem-pole signal driven by the bus arbiter to request the current bus master to relinquish the bus.

TABLE 5-2. CONNECTOR P1 SIGNAL DESCRIPTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B3	ACFAIL	AC FAIL - An open-collector signal driven by the power monitor to indicate a power failure at the AC input of the power supply.
B4	BGØIN*	BUS GRANT Ø IN - The BGØIN* and BGØOUT* signals form a bus grant daisy-chain to select a bus requester on level Ø to become the next bus master.
B5	BGØOUT*	BUS GRANT Ø OUT - The BGØIN* and BGØOUT* signals form a bus grant daisy-chain to select a bus requester on level Ø to become the next bus master.
B6	BG1IN*	BUS GRANT 1 IN - Same as BGØIN* on pin B4.
B7	BG1OUT*	BUS GRANT 1 OUT - Same as BGØOUT* on pin B5.
B8	BG2IN*	BUS GRANT 2 IN - Same as BGØIN* on pin B4.
B9	BG2OUT*	BUS GRANT 2 OUT - Same as BGØOUT* on pin B5.
B1Ø	BG3IN*	BUS GRANT 3 IN - Same as BGØIN* on pin B4.
B11	BG3OUT*	BUS GRANT 3 OUT - Same as BGØOUT* on pin B5.
B12-B15	BRØ*-BR3*	BUS REQUEST (bits Ø-3) - Four open-collector signals that are driven by the bus requesters to request access to VMEbus.
B16-B19	AMØ-AM3	ADDRESS MODIFIER (bits Ø-3) - Same as pin A23.
B2Ø	GND	GROUND
B21	SERCLK	SERIAL CLOCK - Not connected on the MVME141.
B22	SERDAT	SERIAL DATA - Not connected on the MVME141.
B23	GND	GROUND
B24-B3Ø	IRQ7*-IRQ1*	INTERRUPT REQUEST (bits 7-1, reverse ordered) - Seven open-collector signals used to request interrupt servicing.

TABLE 5-2. CONNECTOR P1 SIGNAL DESCRIPTIONS(cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B31	+5VSTDBY	+5 Vdc STANDBY POWER - Not connected on the MVME141.
B32	+5V	+5 Vdc POWER
C1-C8	DØ8-D15	DATA BUS (bits 8-15) - Same as pins AØ-A8.
C9	GND	GROUND
C1Ø	SYSFAIL	SYSTEM FAILURE - An open-collector signal that can be driven by any module to indicate a failure.
C11	BERR*	BUS ERROR - An open-collector signal driven by the slave or the bus timer. A falling-edge indicates that an error has been encountered during the data transfer cycle. A low level indicates the slave may be active on the data bus.
C12	SYSRESET	SYSTEM RESET - An open-collector signal which will reset all modules in the system.
C13	LWORD*	LONGWORD - A three-state signal driven by the master that, when combined with signals DS1*, DSØ*, and A1, indicates the size of the data transfer.
C14	AM5	ADDRESS MODIFIER 5 - Same as AM4 on pin A23.
C15-C3Ø	A23-AØ8	ADDRESS BUS (bits 23-Ø8, reverse ordered) - Sixteen of 23 three-state driven address bus signals on P1. (The extended 8 signals of the address bus are found on connector P2).
C31	+12V	+12 Vdc POWER
C32	+5V	+5 Vdc POWER

TABLE 5-3. CONNECTOR P2 PIN ASSIGNMENTS

Pin Number	Row A Signals	Row B Signals	Row C Signals
1	ADØØ	+5V	ADØ1
2	ADØ2	GND	ADØ3
3	ADØ4	RESERVED	ADØ5
4	ADØ6	A24	ADØ7
5	ADØ8	A25	ADØ9
6	AD1Ø	A26	AD11
7	AD12	A27	AD13
8	AD14	A28	AD15
9	AD16	A29	AD17
1Ø	AD18	A3Ø	AD19
11	AD2Ø	A31	AD21
12	AD22	GND	AD23
13	AD24	+5V	AD25
14	AD26	D16	AD27
15	AD28	D17	AD29
16	AD3Ø	D18	AD31
17	GND	D19	GND
18	IRQ*	D2Ø	GND
19	DS*	D21	GND
2Ø	WR*	D22	GND
21	SPACEØ	D23	SIZEØ
22	SPACE1	GND	PAS*
23	LOCK*	D24	SIZE1
24	ERR*	D25	GND
25	GND	D26	ACK*
26	GND	D27	AC
27	GND	D28	ASACK1*
28	GAØ	D29	ASACKØ*
29	GA1	D3Ø	CACHE*
3Ø	GA2	D31	WAIT*
31	BGIN*	GND	BUSY*
32	BREQ*	+5V	BGOUT*

Note: VMEbus occupies Row B, VSB occupies Rows A and C.

TABLE 5-4. CONNECTOR P2 SIGNAL DESCRIPTIONS

Pin Number	Signal Mnemonic	Signal Name and Description
A1-A16	ADØØ-AD3Ø	(VSB) MULTIPLEXED ADDRESS/DATA (bits ØØ-3Ø, even-numbered) - Sixteen of 32 three-state, multiplexed address/data signals that specify the address during the address broadcast phase of the cycle, and specify the data during the data transfer phase of the cycle.
A17	GND	(VSB) GROUND
A18	IRQ*	(VSB) INTERRUPT REQUEST - An open-collector signal used to request interrupt servicing.
A19	DS*	(VSB) DATA STROBE - A three-state signal driven by the master whose falling-edge initiates the data transfer phase of the cycle.
A2Ø	WR*	(VSB) WRITE - A three-state signal driven by the master that indicates the data transfer is a write cycle to the responding slave when low, or a read cycle from the responding slave when high.
A21	SPACEØ	(VSB) SPACE Ø - One of two three-state signals driven by the master to select the address space for the cycle, or to specify an interrupt acknowledge or arbitration cycle. The address spaces defined for VSB are System Address Space, I/O Address Space, and Alternate Address Space.
A22	SPACE1	(VSB) SPACE 1 - Same as SPACEØ on pin A21.
A23	LOCK*	(VSB) LOCK - A three-state signal driven by the master to specify indivisible-access cycles. A low level locks VSB and the responding slave resource from being accessed by another master.
A24	ERR*	(VSB) ERROR - An open-collector signal driven by the responding slave or bus timer. A falling-edge indicates an that error has been encountered during the data transfer phase of the cycle, and that the data transfer phase can be terminated.

TABLE 5-4. CONNECTOR P2 SIGNAL DESCRIPTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A25-A27	GND	(VSB) GROUND
A28-A3Ø	GAØ-GA2	(VSB) GEOGRAPHICAL ADDRESS (bits Ø-2) - Not connected on the MVME141.
A31	BGIN*	(VSB) BUS GRANT IN - The BGIN* and BGOUT* signals form a daisy-chain to select a bus requester to become the next bus master on VSB.
A32	BREQ*	(VSB) BUS REQUEST - An open-collector signal driven by the bus requesters to request access to VSB.
B1	+5V	+5 Vdc POWER
B2	GND	GROUND
B3	RESERVED	RESERVED - This signal is jumper configurable on the MVME141. Refer to section 2.3.3.
B4-B11	A24-A31	ADDRESS BUS (bits 24-31) - Eight three-state driven address bus signals on P2 that form the extended section of the VMEbus address bus. (The address bus signals A1 through A23 for VMEbus are found on connector P1).
B12	GND	GROUND
B13	+5V	+5 Vdc POWER
B14-B21	D16-D23	DATA BUS (bits 16-23) - Eight of 16 three-state, bidirectional data bus signals on P2 that form the expanded section of the VMEbus data bus. (The 16 data bus signals DØØ through D15 for VMEbus are found on connector P1).
B22	GND	GROUND
B23-B3Ø	D24-D31	DATA BUS (bits 24-31) - Eight of 16 three-state, bidirectional data bus signals on P2 that form the expanded section of the VMEbus data bus. (The 16 data bus signals DØØ through D15 for VMEbus are found on connector P1).
B31	GND	GROUND

TABLE 5-4. CONNECTOR P2 SIGNAL DESCRIPTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B32	+5V	+5 Vdc POWER
C1-C16	ADØ1-AD31	(VSB) MULTIPLEXED ADDRESS/DATA (bits Ø1-31, odd-numbered) - Same as ADØØ through AD3Ø on pins A1 through A16.
C17-C2Ø	GND	(VSB) GROUND
C21	SIZEØ	(VSB) SIZE Ø - One of two three-state signals driven by the master that indicate the number of bytes to be transferred during the data transfer phase of the cycle.
C22	PAS*	(VSB) ADDRESS STROBE - A three-state signal driven by the master. A falling-edge indicates the start of the address broadcast phase of the cycle, and that a valid address has been driven by the master on the AD bus. A low level indicates ownership of VSB and the responding slave resource.
C23	SIZE1	(VSB) SIZE 1 - Same as SIZEØ on pin C21.
C24	GND	(VSB) GROUND
C25	ACK*	(VSB) ACKNOWLEDGE - An open-collector signal driven by the responding slave. A falling-edge indicates that the responding slave has completed its participation in the data transfer phase of the cycle; and that it has driven valid data on the AD bus during a read cycle, or received valid data from the AD bus during a write cycle.
C26	AC	(VSB) ADDRESS COMPLETE - An open-collector signal released by each slave. A rising-edge on AC indicates that all slaves have finished participating in the address broadcast phase of the cycle. A low level on AC during the falling-edge of ACK* or ERR* indicates that the slave will require an address broadcast phase for the next cycle.

TABLE 5-4. CONNECTOR P2 SIGNAL DESCRIPTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C27	ASACK1*	(VSB) ADDRESS SIZE ACKNOWLEDGE 1 - One of two open-collector signals driven by a responding slave to indicate that it has completed its participation in the address broadcast phase of the cycle and has been selected as the responding slave; and to indicate its data port size to the master.
C28	ASACKØ*	(VSB) ADDRESS SIZE ACKNOWLEDGE Ø - Same as ASACK1* on pin C27.
C29	CACHE*	(VSB) CACHE - An open-collector signal driven by the responding slave during the cycle to indicate that the data can be cached by the master. This signal is not supported by the MVME141.
C3Ø	WAIT*	(VSB) WAIT - An open-collector signal driven by any slave to extend the address broadcast phase or the data transfer phase of the cycle. The master can terminate the address broadcast phase and begin the data transfer phase on the falling-edge of ASACKØ* or ASACK1* if WAIT* is high, or on the rising-edge of AC if WAIT* is low. The master will not terminate the data transfer phase of the cycle until ACK* or ERR* is low, and WAIT* is high.
C31	BUSY*	(VSB) BUSY - An open-collector signal driven by the bus master to indicate ownership of VSB.
C32	BGOUT*	(VSB) BUS GRANT OUT - The BGIN* and BGOUT* signals form a daisy-chain to select a bus requester to become the next bus master on VSB.

TABLE 5-5. CONNECTOR J4 SIGNAL DESCRIPTION

Pin Number	Signal Mnemonic	Signal Name and Description
1	DCDA	DATA CARRIER DETECT (channel A) - An input RS-232 signal to Serial Port 2 that indicates a valid carrier is being received when ON. DCDA is a software-monitored signal on the MVME141. (It usually indicates that a communication channel has been connected).
2	RXDA	RECEIVE DATA (channel A) - An input RS-232 signal to Serial Port 2 that provides the received data.
3	TXDA	TRANSMIT DATA (channel A) - An output RS-232 signal from Serial Port 2 that provides the transmitted data.
4	DTRA	DATA TERMINAL READY (channel A) - An output RS-232 signal from Serial Port 2 that indicates the port is ready to transmit and receive data when ON. DTRA is a software-controlled signal on the MVME141.
5	GND	SIGNAL GROUND
6	DSRA	DATA SET READY (channel A) - Not used on the MVME141. DSRA is connected to +12 Volts through a pull-up resistor.
7	RTSA	REQUEST TO SEND (channel A) - An output RS-232 signal from Serial Port 2 that indicates the port is ready to receive data when ON. RTSA is a hardware-controlled signal on the MVME141.
8	CTSA	CLEAR TO SEND (channel A) - An input RS-232 signal to Serial Port 2 that enables the port to transmit data when ON. CTSA is a hardware-controlled signal on the MVME141.
9	RES	RESERVED - Not connected on the MVME141.

Notes: J4 (Serial Port 2) is connected to port B of the MC68681.
ON = SPACE = +3V to +12V, OFF = MARK = -3V to -12V.

TABLE 5-6. CONNECTOR J5 SIGNAL DESCRIPTIONS

Pin Number	Signal Mnemonic	Signal Name and Description
1	DCDA	DATA CARRIER DETECT (channel A) - An input RS-232 signal to Serial Port 1 that indicates a valid carrier is being received when ON. DCDA is a software-monitored signal on the MVME141. (It usually indicates that a communication channel has been connected).
2	RXDA	RECEIVE DATA (channel A) - An input RS-232 signal to Serial Port 1 that provides the received data.
3	TXDA	TRANSMIT DATA (channel A) - An output RS-232 signal from Serial Port 1 that provides the transmitted data.
4	DTRA	DATA TERMINAL READY (channel A) - An output RS-232 signal from Serial Port 1 that indicates the port is ready to transmit and receive data when ON. DTRA is a software-controlled signal on the MVME141.
5	GND	SIGNAL GROUND
6	DSRA	DATA SET READY (channel A) - Not used on the MVME141. DSRA is connected to +12 Volts through a pull-up resistor.
7	RTSA	REQUEST TO SEND (channel A) - An output RS-232 signal from Serial Port 1 that indicates the port is ready to receive data when ON. RTSA is a hardware-controlled signal on the MVME141.
8	CTSA	CLEAR TO SEND (channel A) - An input RS-232 signal to Serial Port 1 that enables the port to transmit data when ON. CTSA is a hardware-controlled signal on the MVME141.
9	RES	RESERVED - Not connected on the MVME141.

Notes: J5 (Serial Port 1) is connected to port A of the MC68681.
ON = SPACE = +3V to +12V, OFF = MARK = -3V to -12V.

5.3 PARTS LIST

The parts location diagram for the MVME141 is provided in Figure 5-1. The reference designation, part number, and description for each component are listed in Table 5-7. This parts list reflects the latest issue of the MVME141 hardware at the time of the release of this user's manual.

TABLE 5-7. MVME141 PARTS LIST

Reference Designation	Motorola Part Number	Description
--	84-W8528BØ1B	Printed wiring board assembly, MVME141
C1-32, C35-44, C46-6Ø, C62,C64, C65-94, C99,C1ØØ	21NW9711AØ2	Capacitor, ceramic, SMD, .1MF, 2Ø%
C33,C34, C45,C61, C63,C95 C98	23NW9618A71	Capacitor, electrolytic, radial, 47MF, 1Ø Vdc
C96	21NW96Ø4A4Ø	Capacitor, ceramic, 1ØPF, 5Ø Vdc
C97	21NW9629AØ1	Capacitor, mica, radial, 5PF, 5ØØ Vdc
CR1	48NW9616AØ3	Diode, 1N4148/1N914
CR2	48NW96Ø7A2Ø	Rectifier, Schottky
DL1	51NW9615Y14	IC, DS1Ø13M-25
DS1	48NW9612A49	LED, red, right-angle
DS2	48NW9612A74	LED, yellow, right-angle
DS3	48NW9612A59	LED, green, right-angle
J1,J3,J6	29NW98Ø5CØ7	Pin, Ø.Ø25-inch square, gold, autoinsert (31 req'd)[used on J1(1-2Ø),J3(1-3),J6(1-8)]
--	29NW98Ø5B17	Jumper, insulated, shorting (15 req'd)[used at J1(1-2,3-4,5-6,7-8,9-1Ø, 11-12,13-14,15-16,17-18,19-2Ø),J3(2-3), J6(1-2,3-4,5-6,7-8)]

TABLE 5-7. MVME141 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
J2	29NW98Ø5B44	Jumper, 2-pin male (1 req'd)[used on J2(2-3)]
J4,J5	28NW98Ø2G79	Connector, 9-pin, socket, right-angle
--	47NW94Ø5A28	Jackpost assembly, D-subminiature (2 req'd)(used with J4 and J5)
P1,P2	28NW98Ø2E51	Connector, 96-pin, plug, PWB
--	Ø5NW9ØØ7A26	Eyelet, Ø.Ø89-inch OD x Ø.344-inch long (4 req'd)(used with P1 and P2)
R1,R3,R5, R7,R9,R12, R14,R15, R17,R19	51NW9626B56	Resistor network, SIP, nine 1ØK ohms
R2,R4, R8,R1Ø	51NW9626B55	Resistor network, SIP, nine 4.7K ohms
R6,R18	51NW9626A31	Resistor network, SIP, seven 51Ø ohms
R11	51NW9626CØ5	Resistor network, SIP, nine 22K ohms
R13	Ø6SW-124AØ9	Resistor, film, 1/4W, 5%, 22 ohms
R16	51NW9626A56	Resistor network, SIP, four 22 ohms
R2Ø,R21	51NW9626B57	Resistor network, SIP, nine 1.ØK ohms
R22-24	51NW9626A75	Resistor network, eight 33Ø/47Ø ohms
--	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (3 req'd)(used at R22, R23, R24)
S1,S2	4ØNW98Ø1B7Ø	Switch, push, SPDT, momentary, right-angle
--	38NW94Ø4C11	Cap, switch, black (used with S1)
--	38NW94Ø4C12	Cap, switch, red (used with S2)

TABLE 5-7. MVME141 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U1-4, U14-17	51NW9615Y12	IC, MCM629ØP25
U5,U6,U1Ø, U18,U19, U85,U86	51NW9615R36	IC, 74F543SPC
--	Ø9-W4659B12	Socket, IC, SIL, 12-pin (8 req'd)(used at U5, U6, U18, and U19)
U7,U2Ø, U21,U31, U33,U73	51NW9615Y45	IC, N74F841N
U8	(NOTE)	IC, programmed PAL11
--	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U8)
U9,U11, U12,U22, U66,U83	51NW9615M9Ø	IC, 74F245PC
U13	51NW9615E93	IC, SN74LS14N
U23,U65	51NW9615R3Ø	IC, SN74AS373N
U24	51NW9615W69	IC, ULA6ØDSAØ14R
--	Ø9NW9811B33	Socket, IC, PGA, 132-pin (1 req'd)(used at U24)
U25	51NW9615W47	IC, MC68882RC25A **(For version MVME141-1 only)**
U25	51NW9615Y98	IC, XC68882RC33A **(For version MVME141-2 only)**
--	Ø9NW9811A71	Socket, IC, PGA, 68-pin (1 req'd)(used at U25)
U26	(NOTE)	IC, programmed PAL1Ø
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U26)

TABLE 5-7. MVME141 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U27	(NOTE)	IC, programmed PAL9
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U27)
U28-3Ø, U39-42, U62	51NW9615YØ5	IC, SN74AS258N
U32	51NW9615WØ7	IC, IDT74FCT521AP
U34	51NW9615YØ6	MB67Ø3Ø9U
--	Ø9NW9811A73	Socket, IC, PGA, 89-pin (1 req'd)(used at U34)
U35	(NOTE)	IC, programmed PAL2Ø
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U35)
U36	51NW9615W66	IC, MC68Ø3ØRC25
--	Ø9NW9811B14	Socket, IC, PGA, 144-pin (1 req'd)(used at U36)
U37	(NOTE)	IC, programmed PAL12
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U37)
U38,U47, U48-5Ø	51NW9615ZØ1	IC, MK41H8ØN-2Ø
U43	(NOTE)	IC, programmed PAL14
--	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U43)
U44	51NW9615R43	IC, 74F161APC
U45	(NOTE)	IC, programmed PAL2
U46	(NOTE)	IC, programmed PAL3

TABLE 5-7. MVME141 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U46)
U51,U59	51NW9615J39	IC, 74F74PC
U52	(NOTE)	IC, programmed PAL13
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U52)
U53	(NOTE)	IC, programmed PAL16
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U53)
U54	51NW9615T47	IC, UPD43256C-12
--	Ø9-W4659B14	Socket, IC, SIL, 14-pin (2 req'd)(used at U54)
U55	(NOTE)	IC, programmed PAL7
U56	(NOTE)	IC, 141 BUG ODD
--	Ø9-W4659B16	Socket, IC, SIL, 16-pin (2 req'd)(used at U56)
U57,U61	51NW9615K99	IC, 74F374PC
U58	51NW9615K64	IC, 74F86PC
U6Ø	51NW9615N61	IC, 74F534PC
U63	(NOTE)	IC, programmed PAL1
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U63)
U64	51NW9615N32	IC, 74F164PC
U67,U77	51NW9615S83	IC, MC1454Ø6P
U68	(NOTE)	IC, programmed PAL8
U69	51NW9615R69	IC, MC6823ØP8

TABLE 5-7. MVME141 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
--	Ø9-W4659B24	Socket, IC, SIL, 24-pin (2 req'd)(used at U69)
U7Ø	(NOTE)	IC, programmed PAL4
U71	(NOTE)	IC, programmed PAL6
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U71)
U72	(NOTE)	IC, programmed PAL5
--	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U72)
U74	(NOTE)	IC, programmed PAL17
--	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U74)
U75	51NW9615W77	IC, XVSB24ØØ
--	Ø9NW9811B33	Socket, IC, PGA, 132-pin (1 req'd)(used at U75)
U76	51NW9615P22	IC, MC68681P
--	Ø9-W4659B2Ø	Socket, IC, SIL, 2Ø-pin (2 req'd)(used at U76)
U78	(NOTE)	IC, 141 BUG EVEN
--	Ø9-W4659B16	Socket, IC, SIL, 16-pin (2 req'd)(used at U78)
U79	(NOTE)	IC, programmed PAL18
U8Ø	(NOTE)	IC, programmed PAL19
U81	51NW9615U6Ø	IC, MK48TØ2B-25
U82	(NOTE)	IC, programmed PAL15
--	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U82)

TABLE 5-7. MVME141 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U84	51NW9615K47	IC, 74F244PC
Y1	48-W5558BØ5	Crystal oscillator, 16.Ø MHz
Y2	48-W5558BØ2	Crystal oscillator, 25.Ø MHz **(For version MVME141-1 only)**
Y2	48-W5558BØ8	Crystal oscillator, 33.33 MHz **(For version MVME141-2 only)**
Y3	48NW96Ø6A54	Quartz crystal, 3.6864 MHz
--	67NW9415A17	Kit, ejector handle, 6U component
--	64-W5742BØ1A	Panel, front, MVME141
--	33-W5Ø89BØ1	Nameplate, Scanbe, logo
--	33-W5787BØ1A	Nameplate, MVME141-1
--	42NW94Ø1B14	Captive collar screw (2 req'd)
--	Ø3NW9ØØ4B48	Screw, captive, M2.5 (2 req'd)

NOTE: When ordering, use number labeled on part.

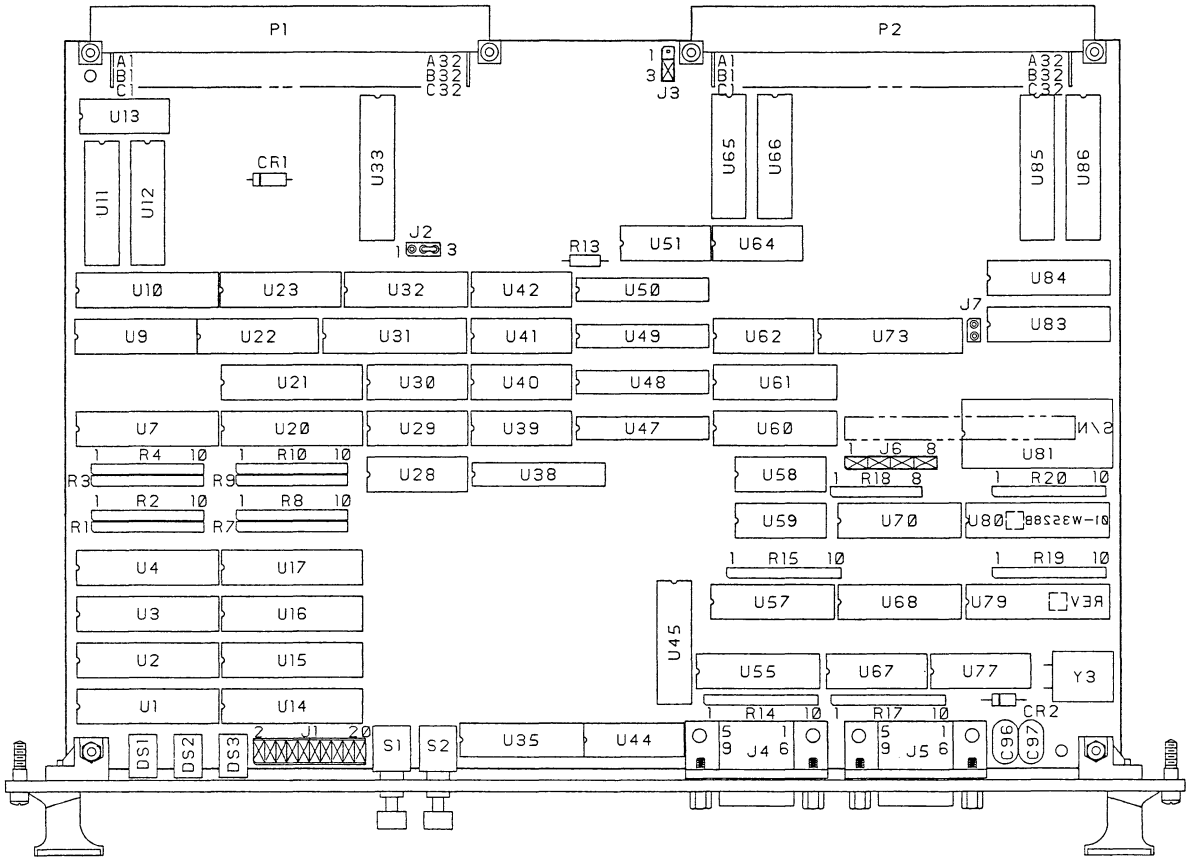


FIGURE 5-1. MVME141 PARTS LOCATION DIAGRAM
(SHEET 1 OF 3)

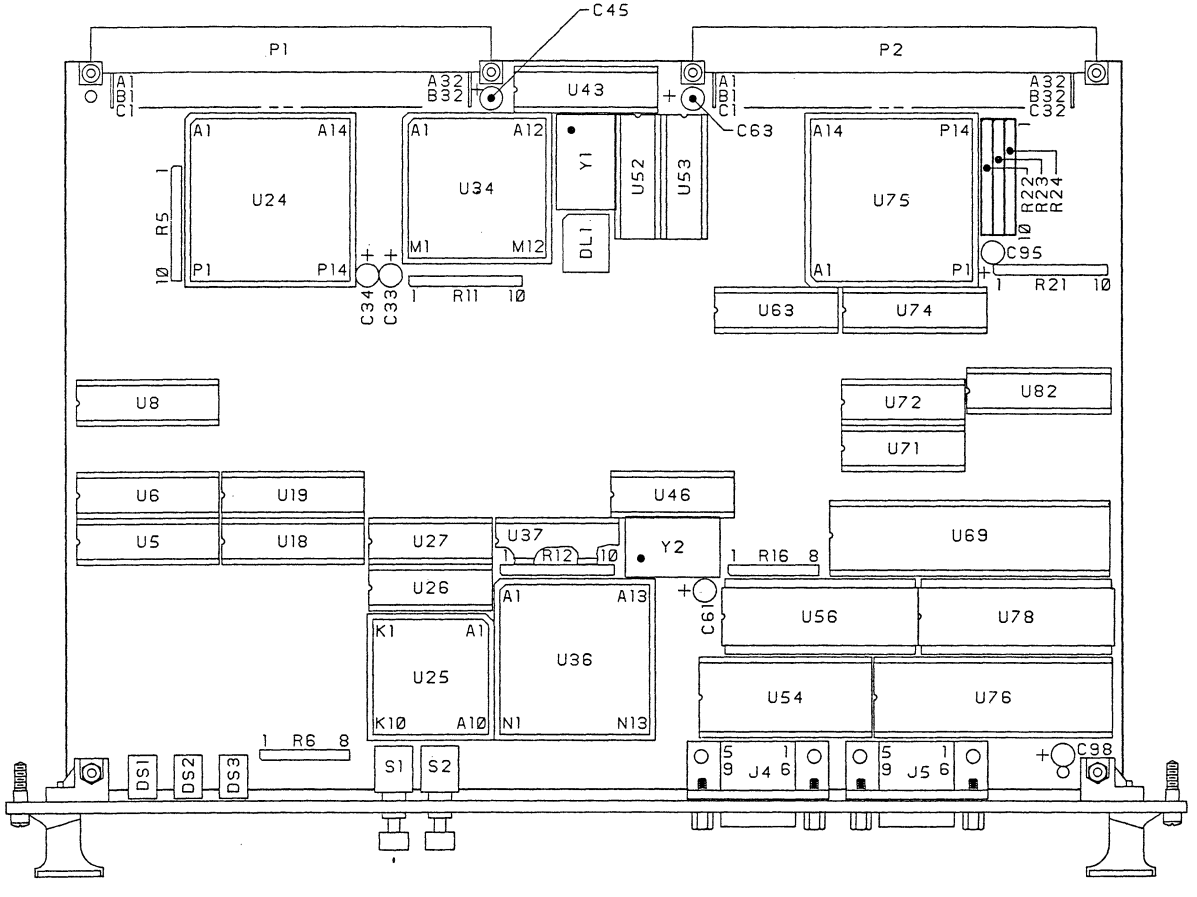
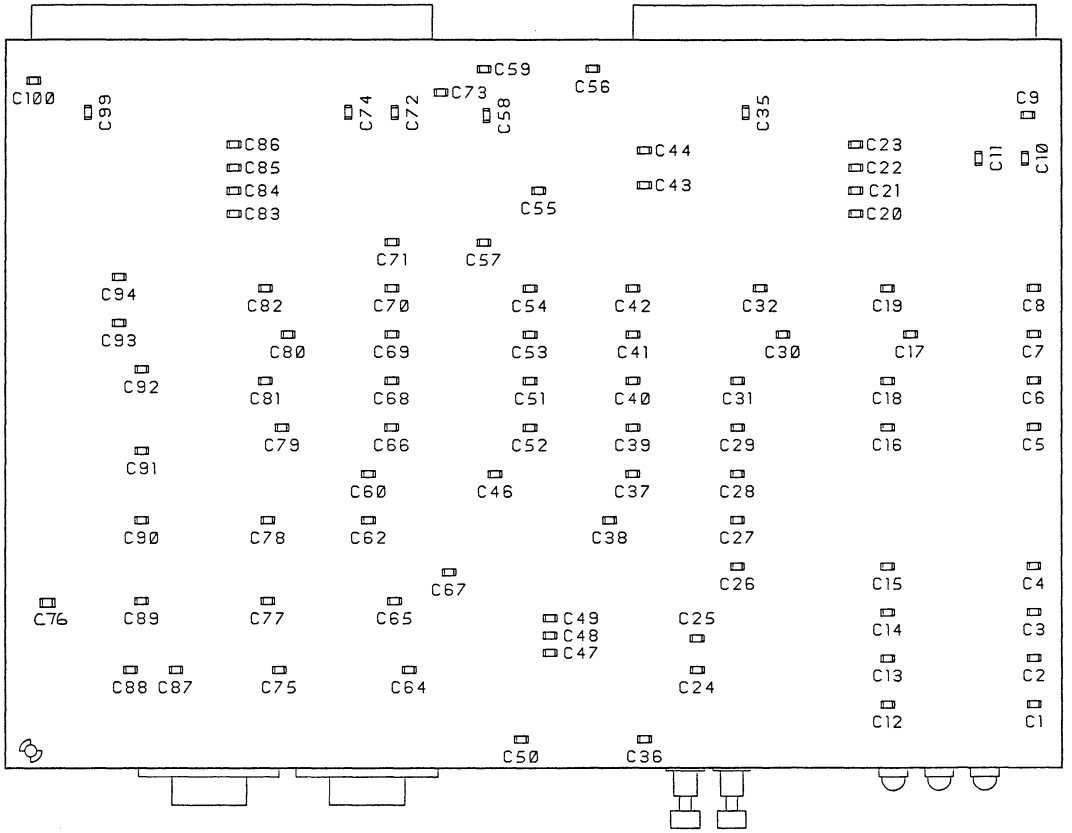


FIGURE 5-1. MVME141 PARTS LOCATION DIAGRAM (cont.)
(SHEET 2 OF 3)



NOTES: 1) SECONDARY SIDE SHOWN WITHOUT FRONT PANEL.
2) CAPACITORS FOR SURFACE MOUNT APPLICATION AS SHOWN.

FIGURE 5-1. MVME141 PARTS LOCATION DIAGRAM (cont.)
(SHEET 3 OF 3)

5.4 SCHEMATIC DIAGRAMS

Figure 5-2 (3Ø sheets) contains detailed schematic diagrams of the internal circuitry comprising the MVME141. These schematic diagrams represent the lastest design. Occasionally, minor component changes are made at the factory. Therefore, when replacing a component, always use the same value as the defective component even though the schematic diagram may indicate a different value or type.

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL Ø1-W3528B__, CURRENT REVISION/CONFIGURATION APPLIES.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   <> DENOTES - VECTORED SIGNALS.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
7. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS: (SHEET) 5 C7 (ZONE)

REF DES	TYPE △4	GND	+5V
DL1	DLY2PM	4	8
U1	MCM6290	12	24
U2	MCM6290	12	24
U3	MCM6290	12	24
U4	MCM6290	12	24
U5	F543	12	24
U6	F543	12	24
U7	F841	12	24
U8	PAL20L8	12	24
U9	F245	10	20
U10	F543	12	24
U11	F245	10	20
U12	F245	10	20
U13	LS14	7	14
U14	MCM6290	12	24
U15	MCM6290	12	24
U16	MCM6290	12	24
U17	MCM6290	12	24
U18	F543	12	24
U19	F543	12	24
U20	F841	12	24
U21	F841	12	24
U22	F245	10	20
U23	AS373	10	20

REF DES	TYPE △4	GND	+5V
U24	MVME6000	C3	D1
		C8	K1
		G3	E14
		M7	L14
		N2	
		B13	
		H12	
		M12	
U25	MC68882	A2	A1
		B2	B1
		B3	B8
		B7	E2
		C1	E9
		C3	H8
		D2	J2
		F2	
		H9	
		J8	
		K3	
		A10	
		E10	
U26	PAL16L8	10	20
U27	PAL16L8	10	20
U28	AS258	8	16
U29	AS258	8	16
U30	AS258	8	16
U31	F841	12	24
U32	FCT521	10	20
U33	F841	12	24
U34	VMEMON	C6	C7
		F3	G3
		K7	K6
		G10	F10
U35	PAL16L8	10	20
U36	MC68030	C5	C6
		C7	D4
		C9	F2
		E3	H3
		F3	K4
		G3	L6
		J3	D10
		L5	F11
		L7	H11
		L8	K10
		L9	
		E11	
		G11	
		J11	
U37	PAL16L8	10	20
U38	4180	11	22
U39	AS258	8	16
U40	AS258	8	16
U41	AS258	8	16
U42	AS258	8	16
U43	PAL14	12	24
U44	F161	8	16
U45	PAL16L8	10	20
U46	PAL16L8	10	20
U47	4180	11	22
U48	4180	11	22

REF DES	TYPE △4	GND	+5V	+12V	-12V
U49	4180	11	22		
U50	4180	11	22		
U51	F74	7	14		
U52	PAL16L8	10	20		
U53	PAL16L8	10	20		
U54	MCM60256	14	28		
U55	PAL16L8	10	20		
U56	27C1001	16	32		
U57	F374	10	20		
U58	F86	7	14		
U59	F74	7	14		
U60	F534	10	20		
U61	F374	10	20		
U62	AS258	8	16		
U63	PAL16R4	10	20		
U64	F164	7	14		
U65	AS373	10	20		
U66	F245	10	20		
U67	MC145406	9	16	1	8
U68	PAL16L8	10	20		
U69	MC68230	38	12		
U70	PAL16L8	10	20		
U71	PAL16L8	10	20		
U72	PAL16L8	10	20		
U73	F841	12	24		
U74	PAL20L8	12	24		
U75	MVSB2400	C3	D1		
		C8	K2		
		G3	E14		
		M7	L13		
		N2			
		B13			
		H12			
		M12			
U76	MC68681	20	40		
U77	MC145406	9	16	1	8
U78	27C1001	16	32		
U79	PAL20L8	12	24		
U80	PAL20RA10	12	24		
U81	MK48T02	12	24		
U82	PAL20L8	12	24		
U83	F245	10	20		
U84	F244	10	20		
U85	F543	12	24		
U86	F543	12	24		
Y1	16MHZ	7	14		
Y2	25MHZ	7	14		

REF DES	SH
CR2	2
CR1	22
C1	2
C2	2
C3	2
C4	2
C5	2
C6	2
C7	2
C8	2
C9	2
C10	2
C11	2
C12	2
C13	2
C14	2
C15	2
C16	2
C17	2
C18	2
C19	2
C20	2
C21	2
C22	2
C23	2
C24	2
C25	2
C26	2
C27	2
C28	2
C29	2
C30	2
C31	2
C32	2
C33	2
C34	22
C35	2
C36	2
C37	2
C38	2
C39	2
C40	2
C41	2
C42	2
C43	2
C44	2
C45	2
C46	2
C47	2
C48	2
C49	2
C50	2
C51	2
C52	2
C53	2
C54	2
C55	2
C56	2
C57	2
C58	2

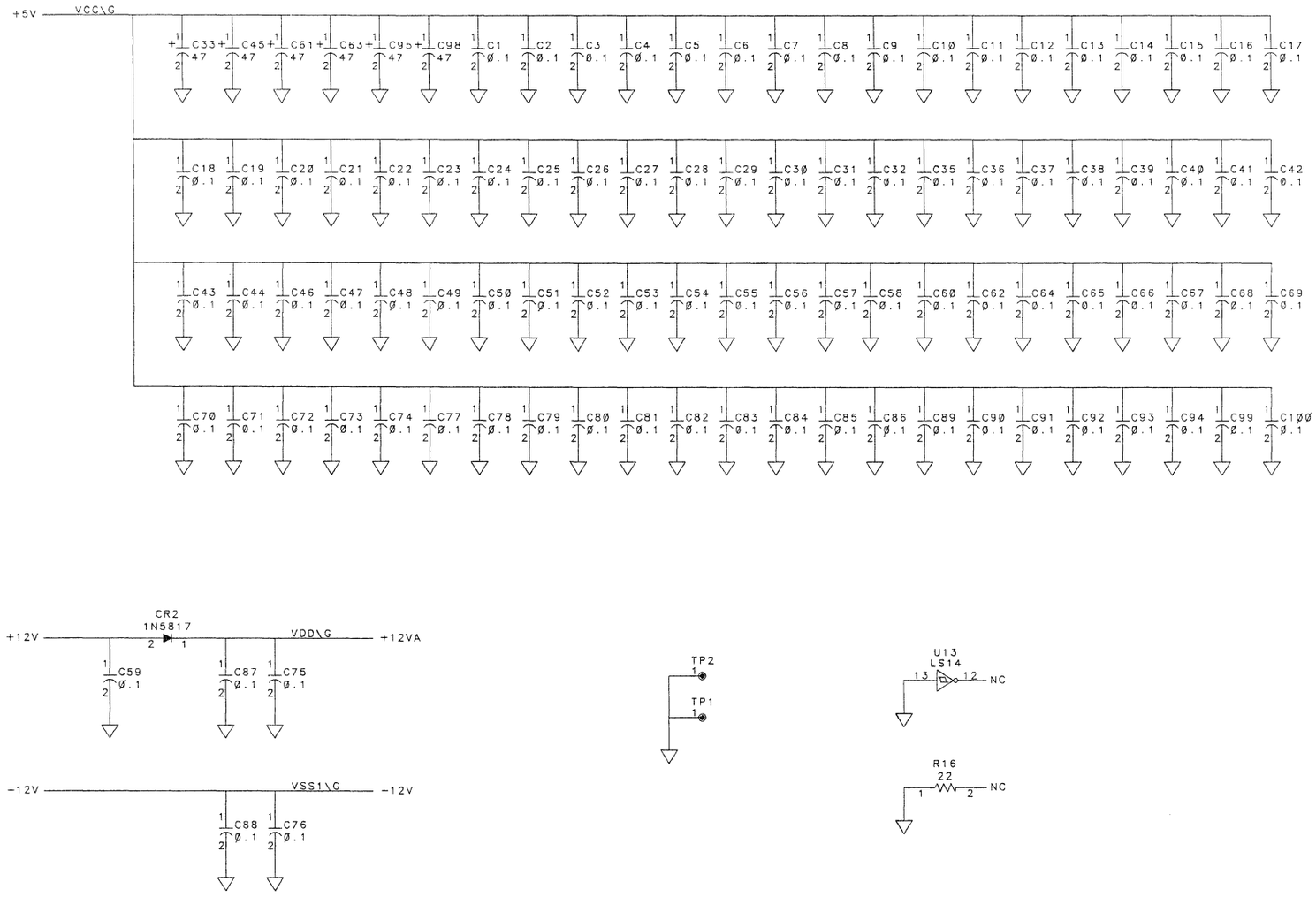
REF DES	SH
C59	2
C60	2
C61	2
C62	2
C63	2
C64	2
C65	2
C66	2
C67	2
C68	2
C69	2
C70	2
C71	2
C72	2
C73	2
C74	2
C75	2
C76	2
C77	2
C78	2
C79	2
C80	2
C81	2
C82	2
C83	2
C84	2
C85	2
C86	2
C87	2
C88	2
C89	2
C90	2
C91	2
C92	2
C93	2
C94	2
C95	2
C96	28
C97	28
C98	2
C99	2
C100	2
DL1	17
DL1	19
DS1	30
DS2	30
DS3	30
J1	22
J2	20
J3	22
J4	4
J5	4
J6	27
J7	19
P1	3
P2	4
R1	16
R2	16
R3	16
R4	16

REF DES	SH
R5	20
R6	30
R7	16
R8	16
R9	16
R10	16
R11	22
R12	6
R13	27
R14	28
R15	25
R16	2
R16	6
R17	28
R18	30
R19	25
R20	20
R21	19
R22	18
R23	19
R24	18
S1	30
S2	30
TP1	2
TP2	2
U1	7
U2	7
U3	7
U4	7
U5	16
U6	16
U7	14
U8	14
U9	21
U10	21
U11	21
U12	21
U13	2
U13	19
U13	22
U13	30
U14	7
U15	7
U16	7
U17	7
U18	16
U19	16
U20	15
U21	15
U22	21
U23	22
U24	20
U25	6
U26	13
U27	13
U28	8
U29	8
U30	8
U31	15
U32	22

REF DES	SH
U33	22
U34	23
U35	30
U36	6
U37	14
U38	10
U39	8
U40	8
U41	8
U42	8
U43	17
U44	30
U45	11
U46	11
U47	9
U48	9
U49	9
U50	9
U51	17
U51	27
U52	17
U53	24
U54	26
U55	13
U56	26
U57	11
U58	6
U58	22
U59	6
U59	12
U60	12
U61	12
U62	10
U63	10
U64	24
U65	22
U66	25
U67	28
U68	13
U69	27
U70	11
U71	12
U72	12
U73	15
U74	24
U75	18
U76	28
U77	28
U78	26
U79	29
U80	29
U81	26
U82	19
U83	25
U84	19
U85	21
U86	21
Y1	27
Y2	6
Y3	28

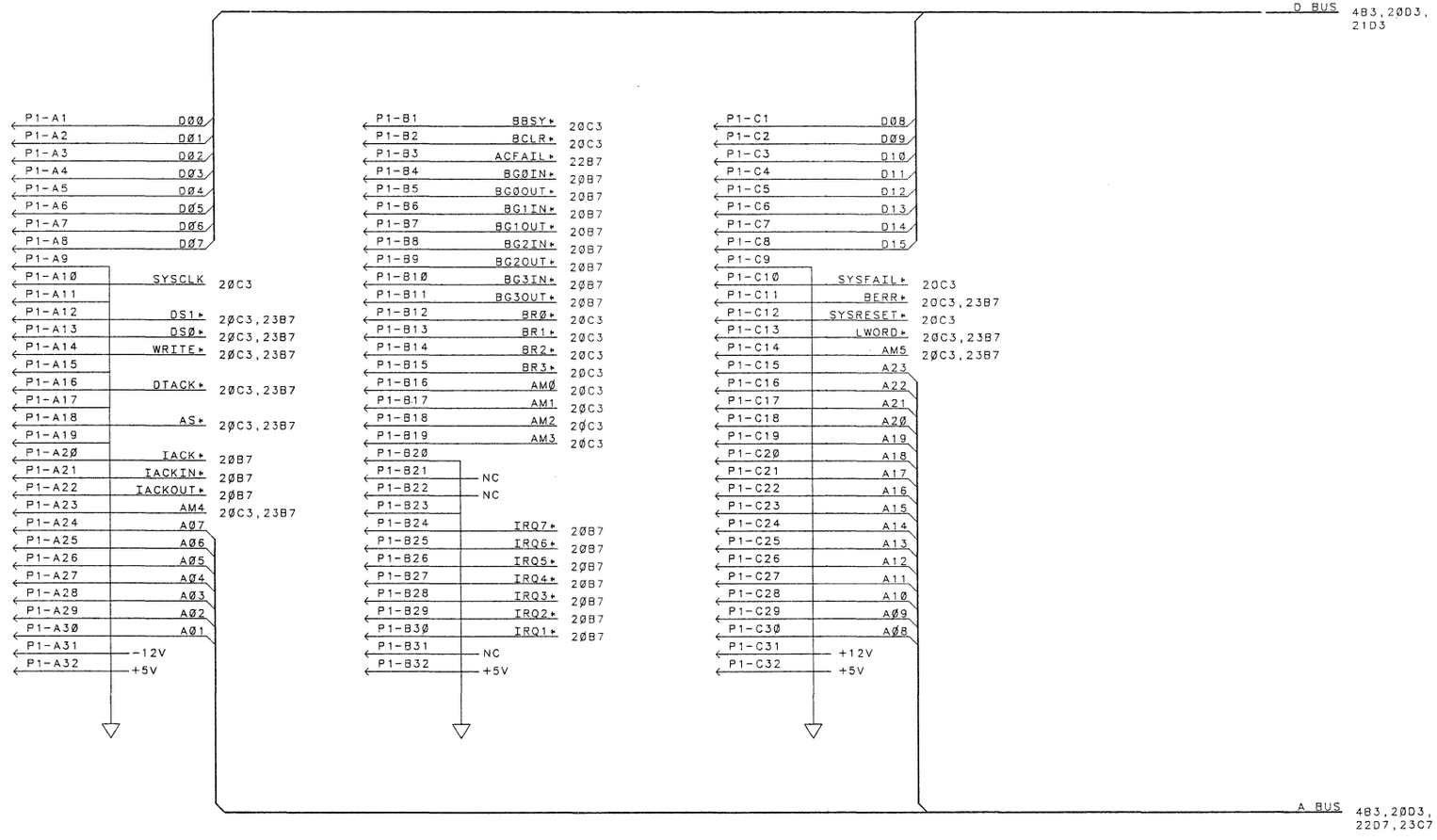
63DW3528B0B REV A SH 1 OF 30
JUN 22 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 1 OF 30)



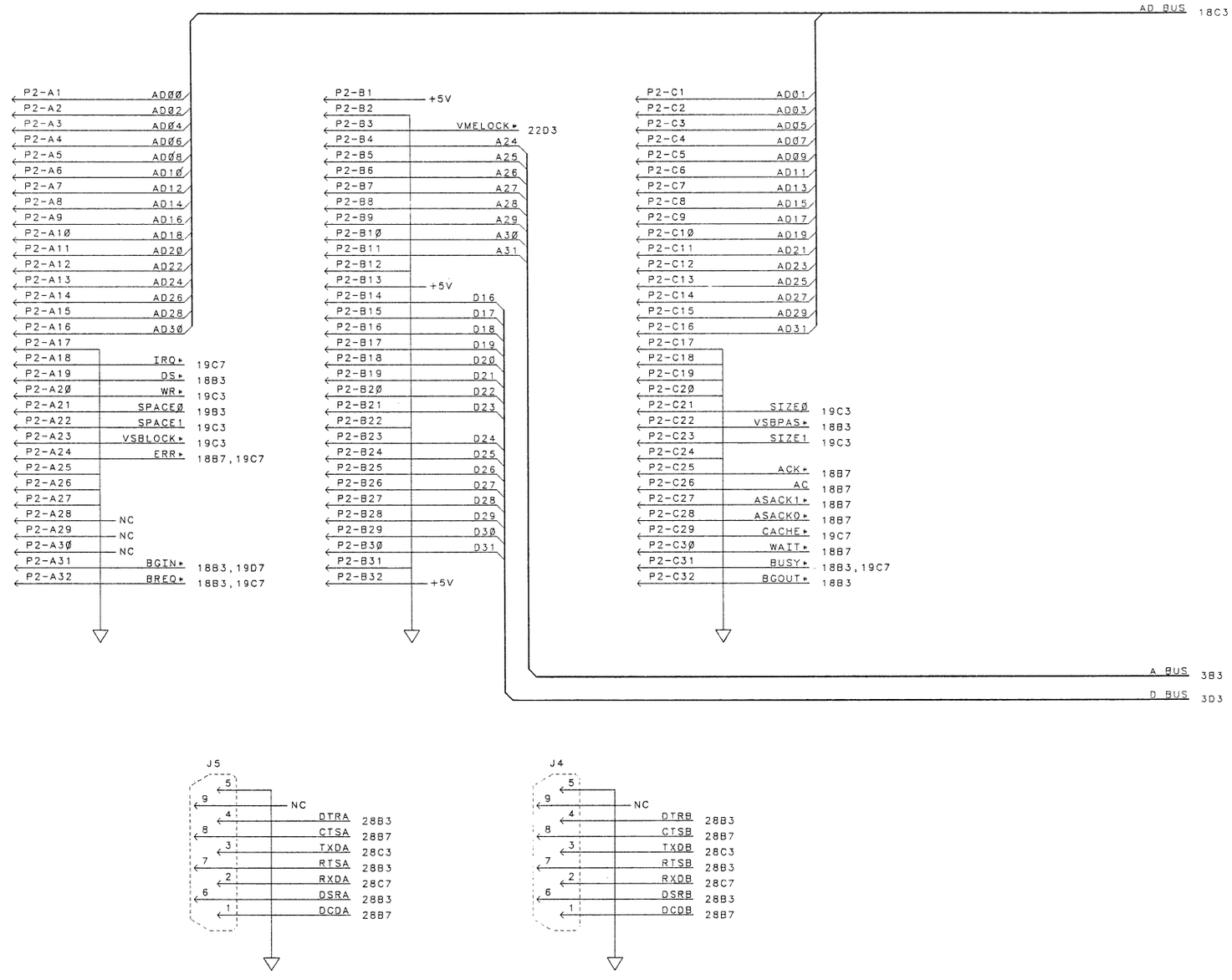
63DW3528BØB REV A SH 2 OF 3Ø
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 2 OF 3Ø)



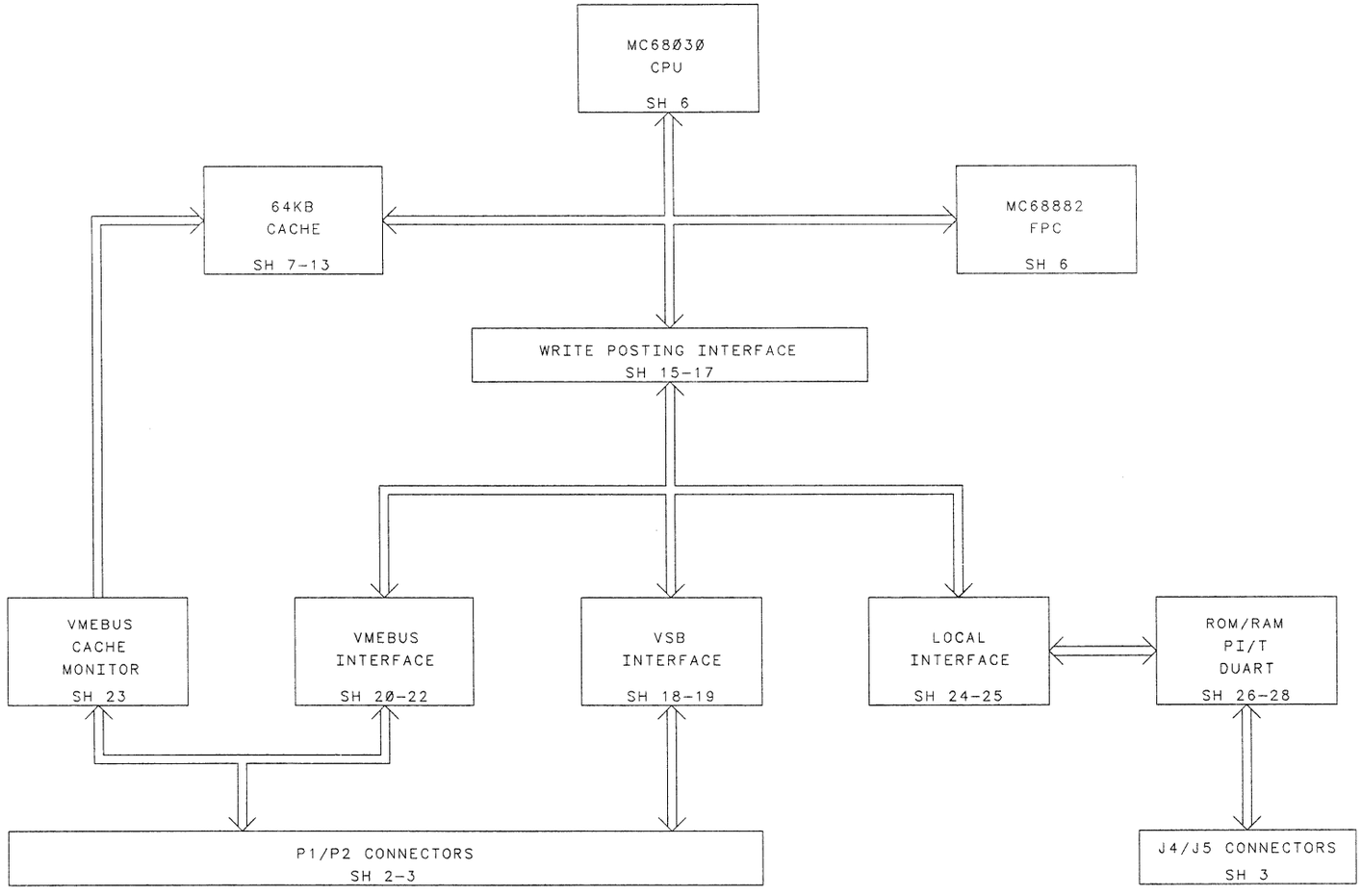
63DW3528B0B REV A SH 3 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 3 OF 30)



63DW3528B0B REV A SH 4 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 4 OF 30)



BLOCK DIAGRAM
63DW3528BØB REV A SH 5 OF 3Ø
APP 11 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 5 OF 3Ø)

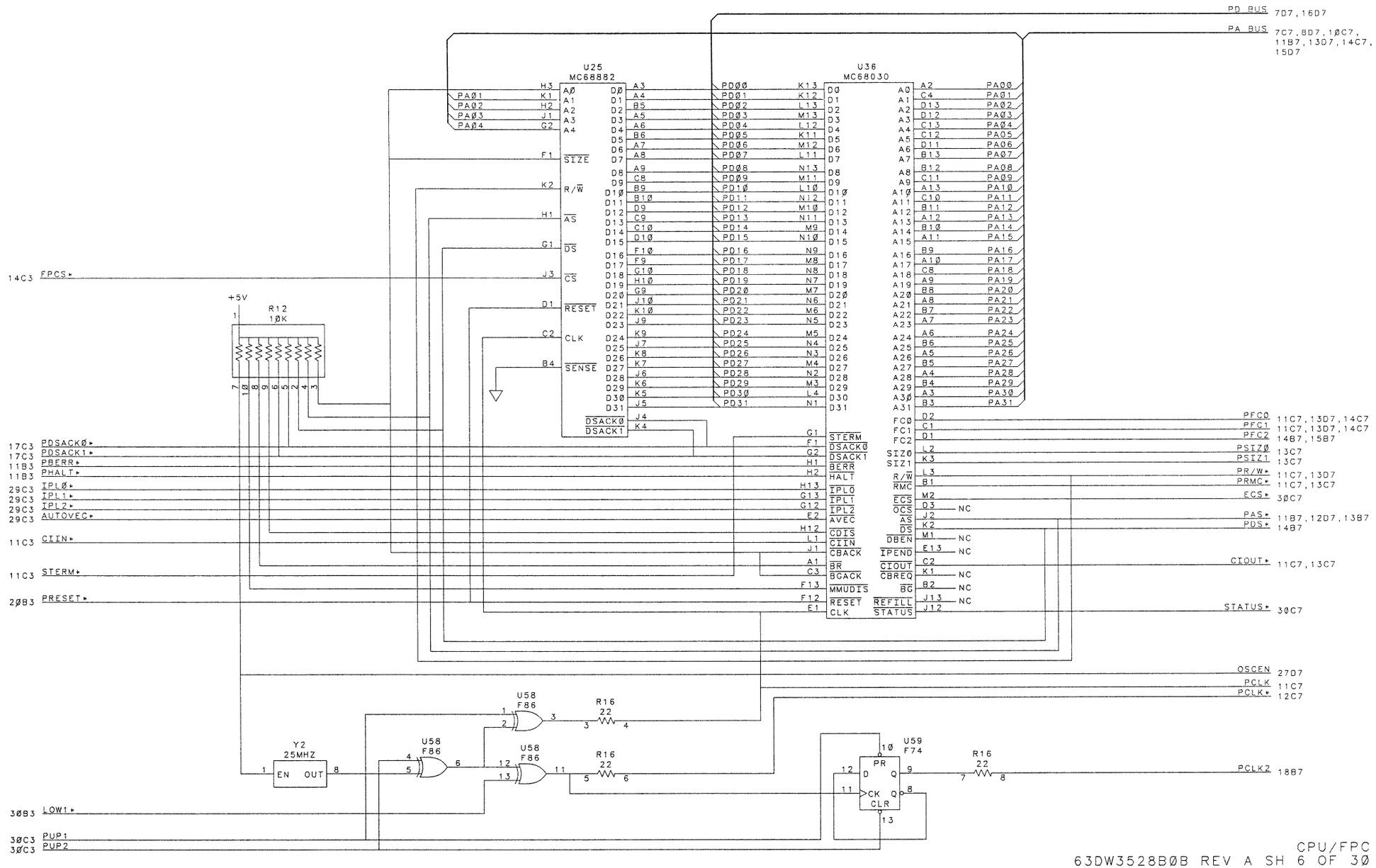
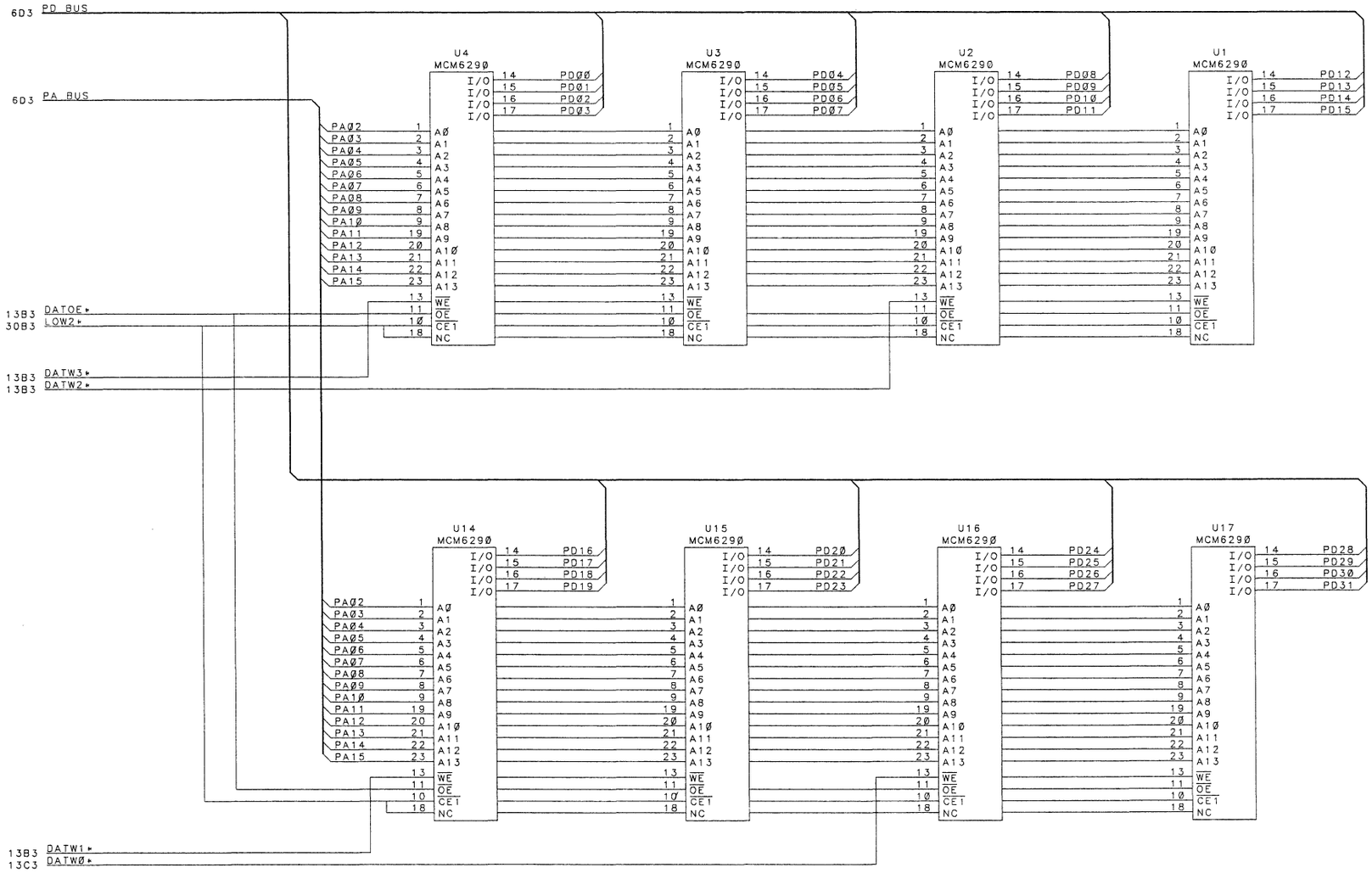
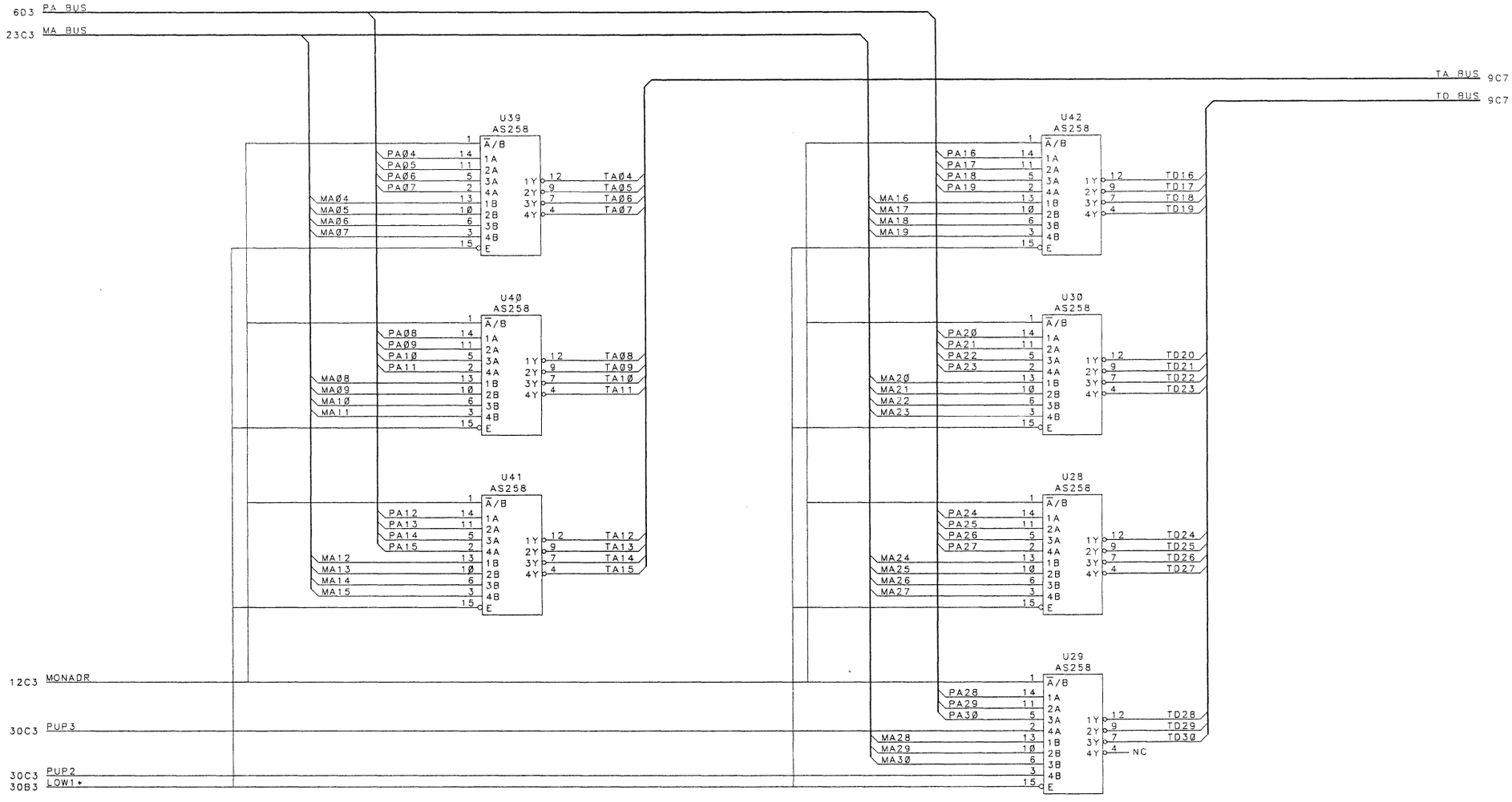


FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 6 OF 30)



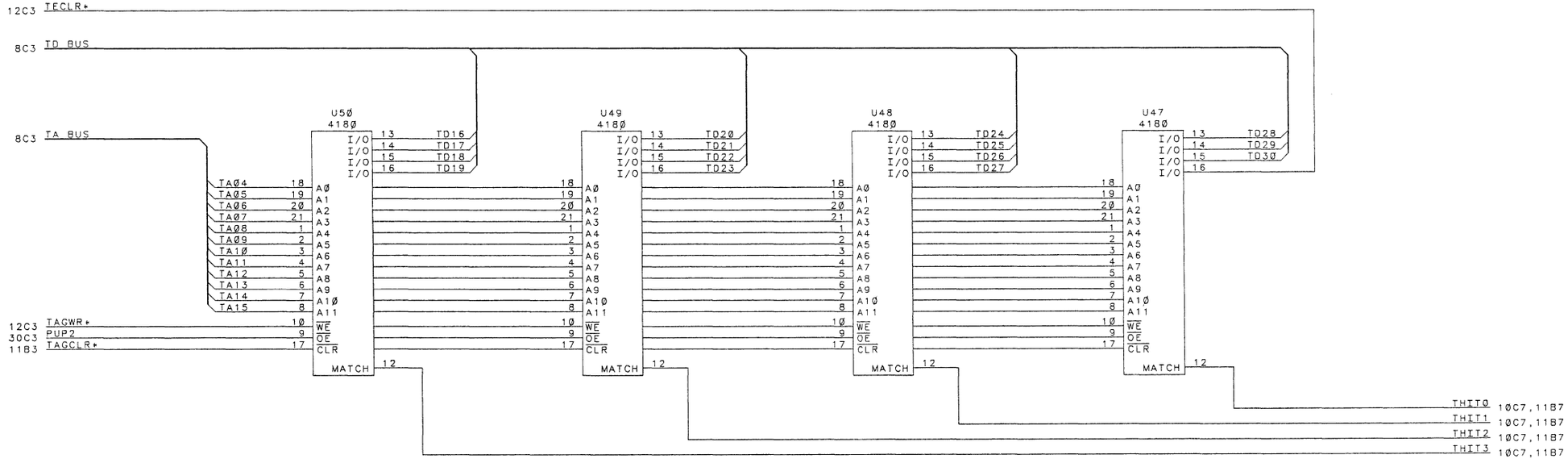
CACHE DATA RAM
63DW3528B0B REV A SH 7 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 7 OF 30)



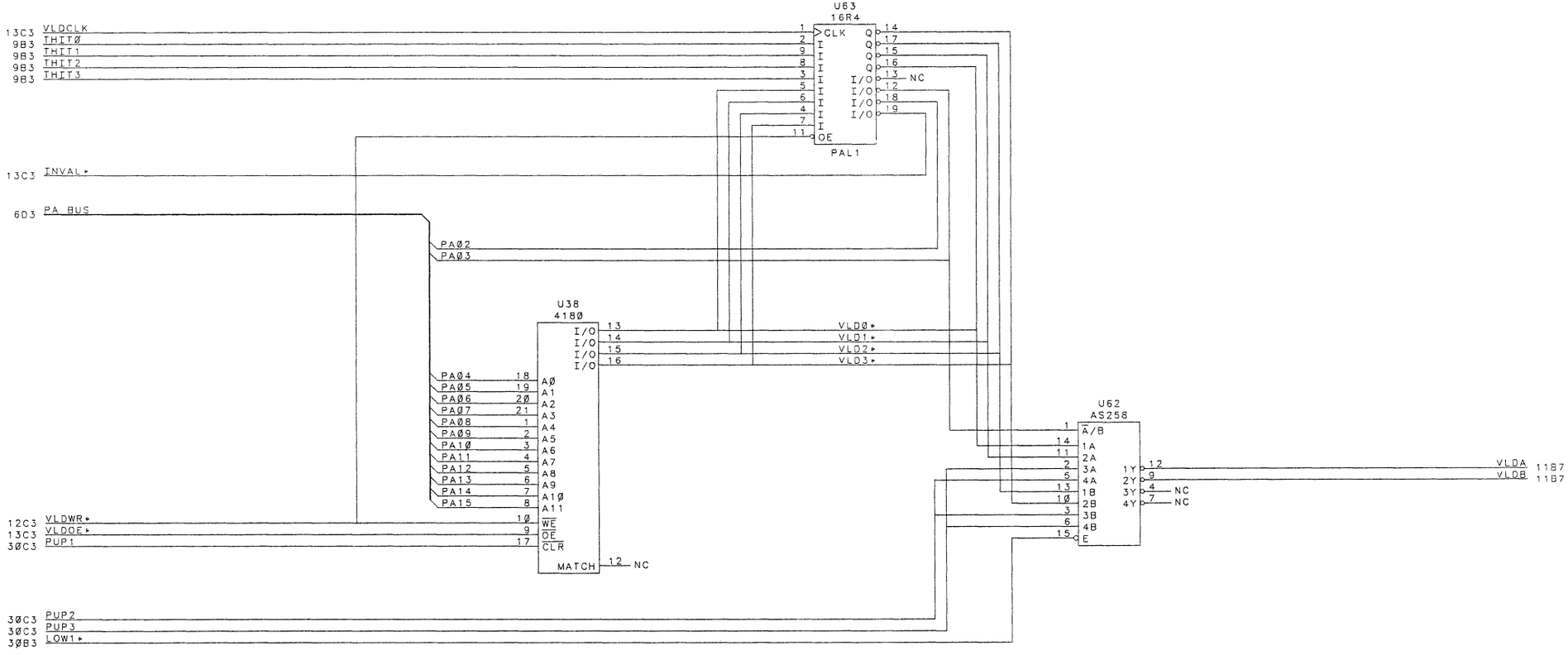
CACHE TAG MUX
63DW3528BØB REV A SH 8 OF 3Ø
JUN 2Ø 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 8 OF 3Ø)



CACHE TAG MUX
63DW3528B0B REV A SH 9 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 9 OF 30)



CACHE VALID RAM
63DW3528B0B REV A SH 10 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 10 OF 30)

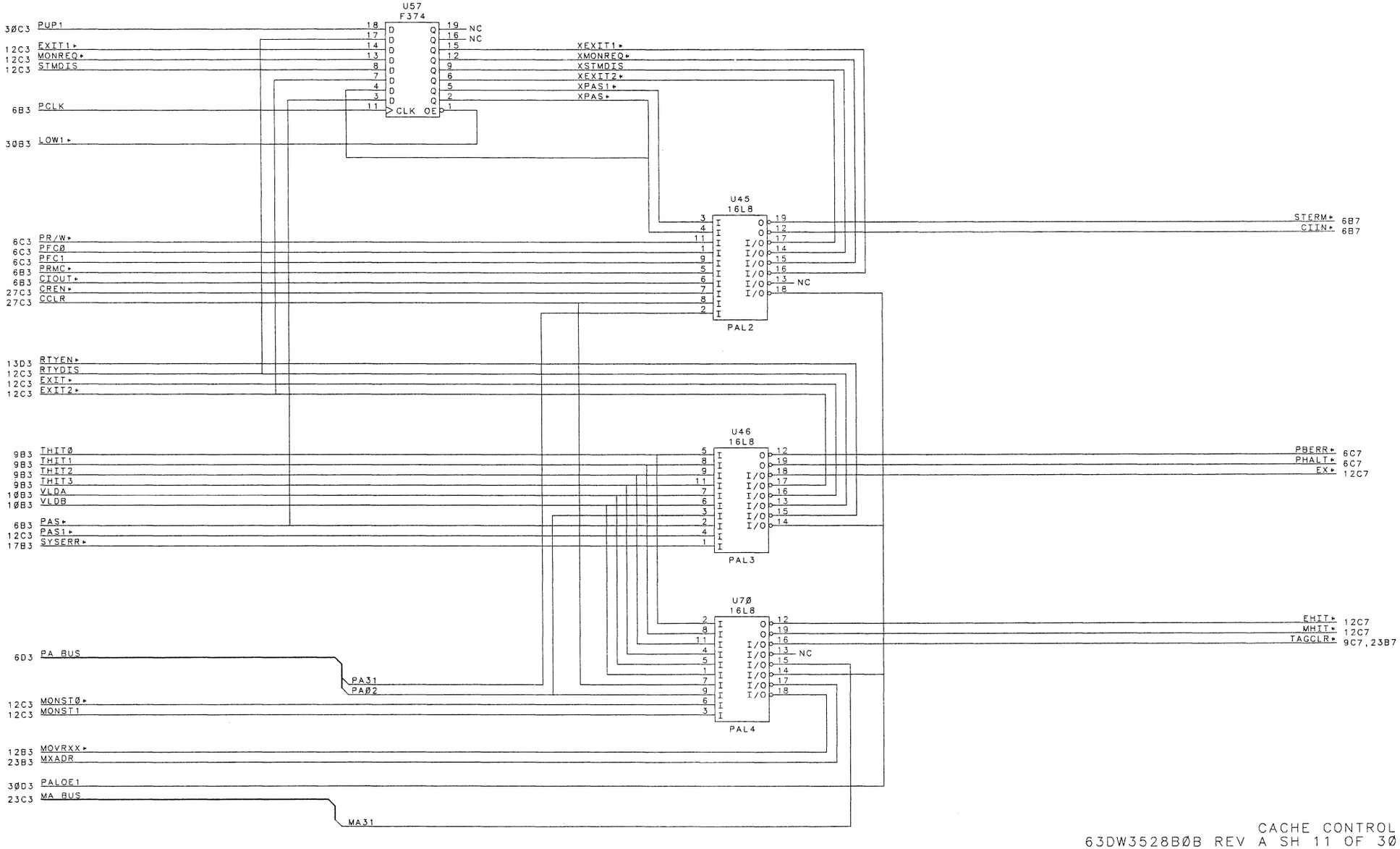
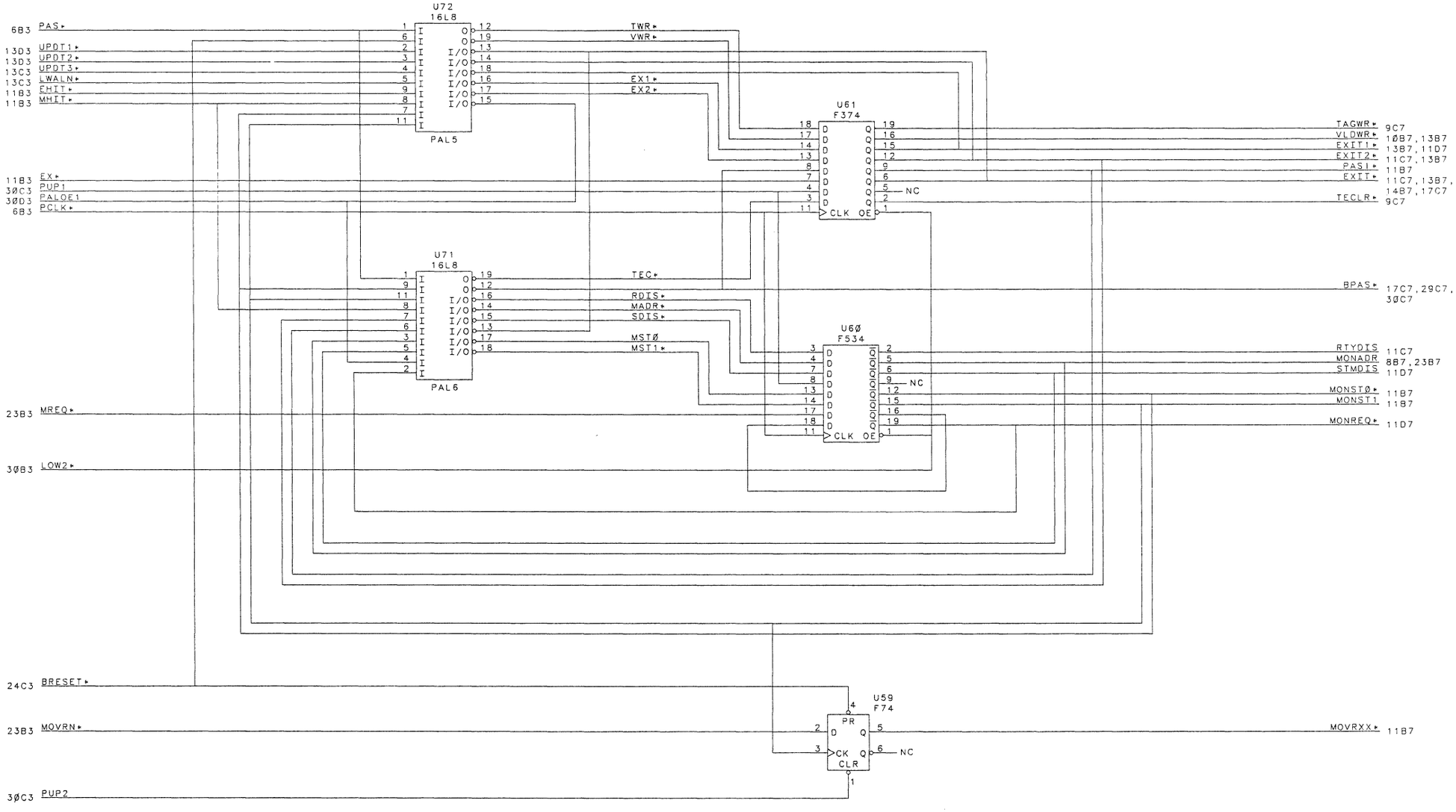
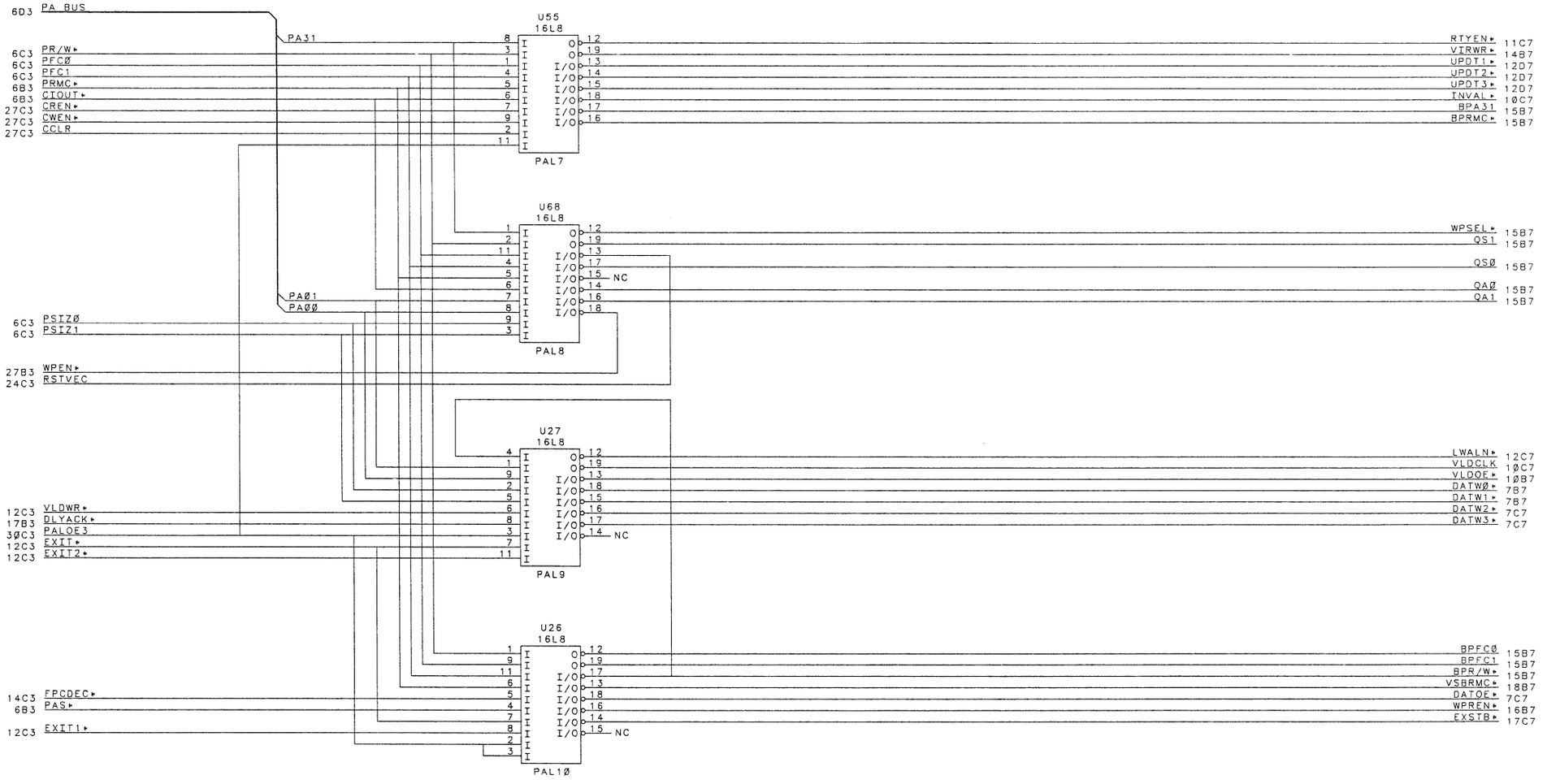


FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 11 OF 30)



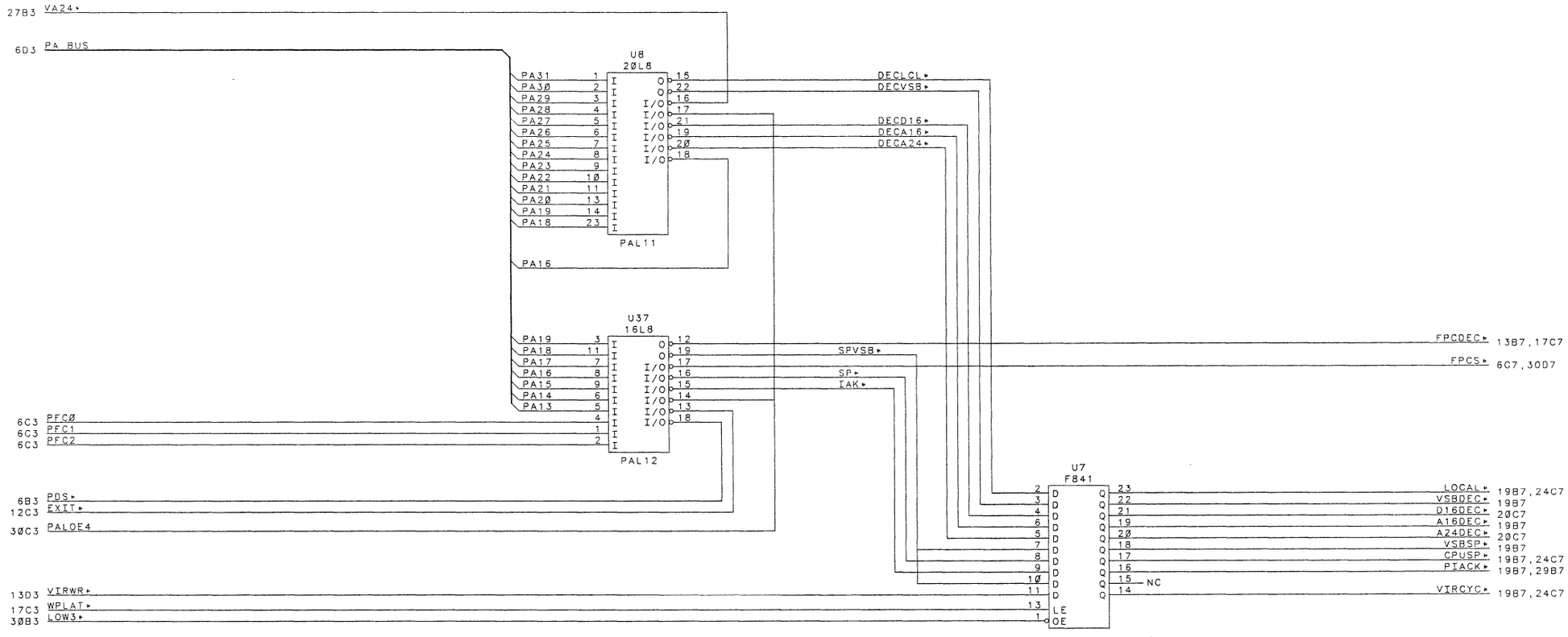
CACHE CONTROL
63DW3528BØB REV A SH 12 OF 3Ø
JUN 2Ø 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 12 OF 3Ø)



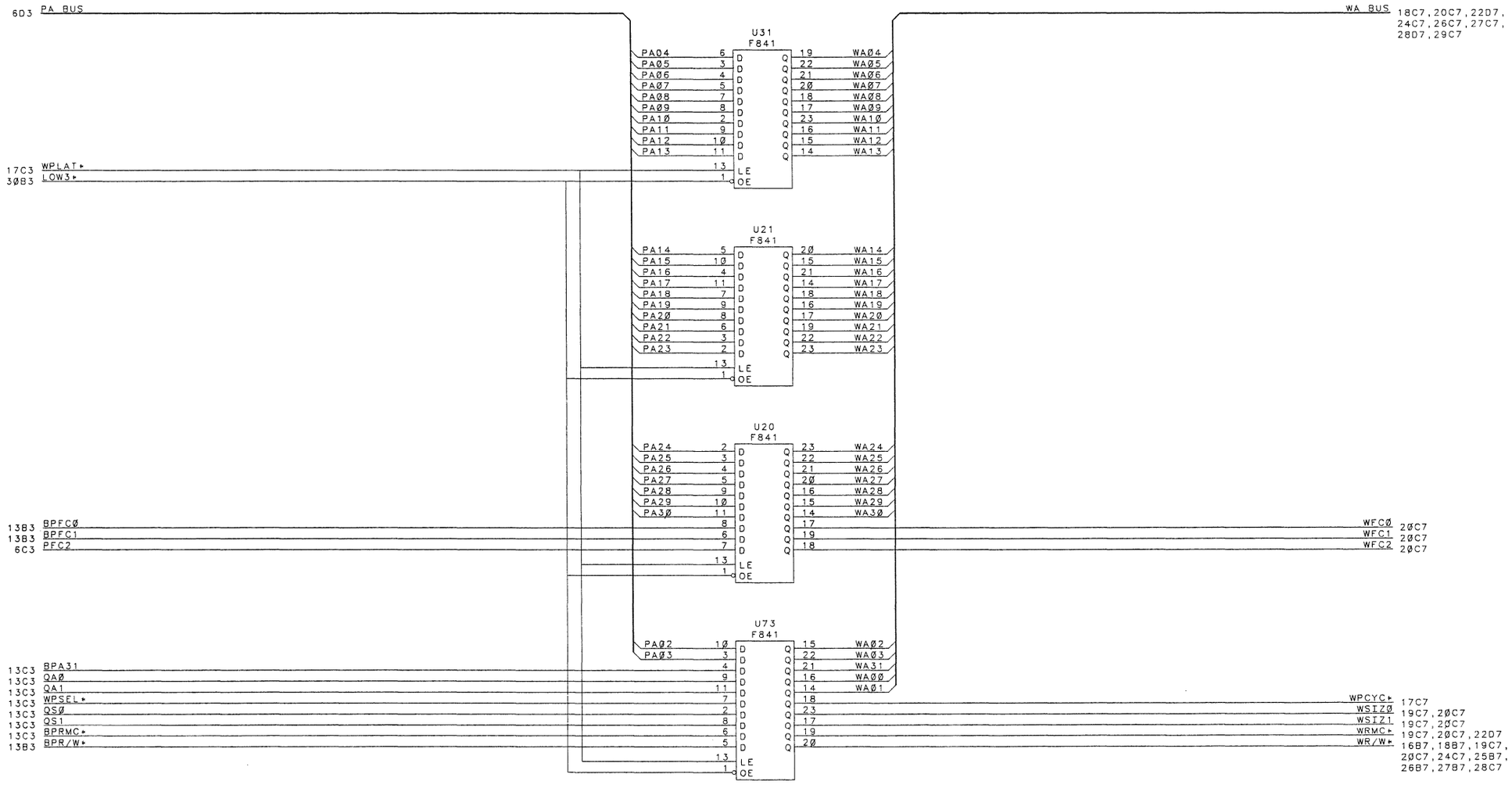
CACHE CONTROL
63DW3528BØB REV A SH 13 OF 3Ø
JUN 2Ø 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 13 OF 3Ø)



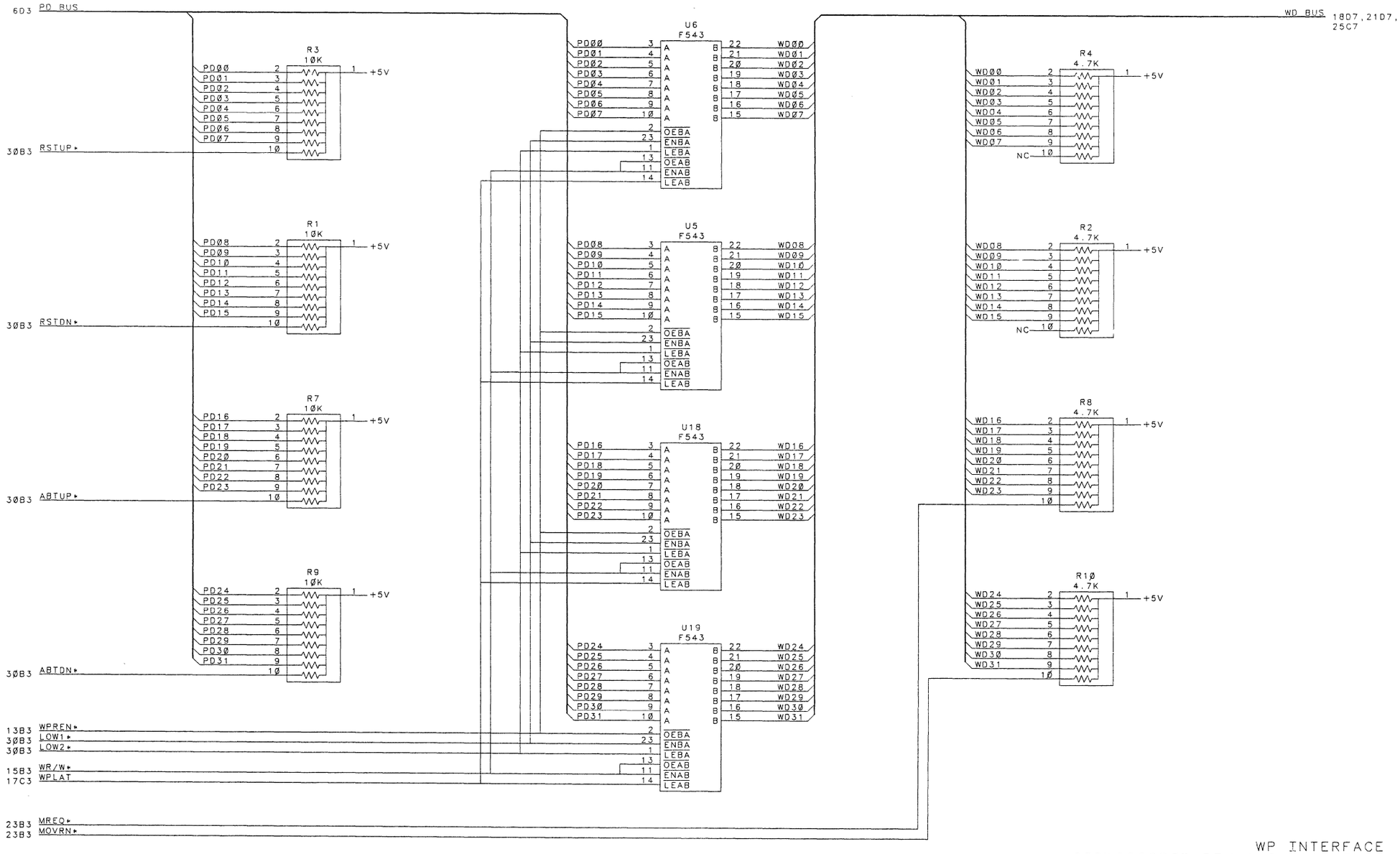
PRIMARY DECODE
63DW3528B0B REV A SH 14 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 14 OF 30)



WP INTERFACE
63DW3528B0B REV A SH 15 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 15 OF 30)



WP INTERFACE
63DW3528B0B REV A SH 16 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 16 OF 30)

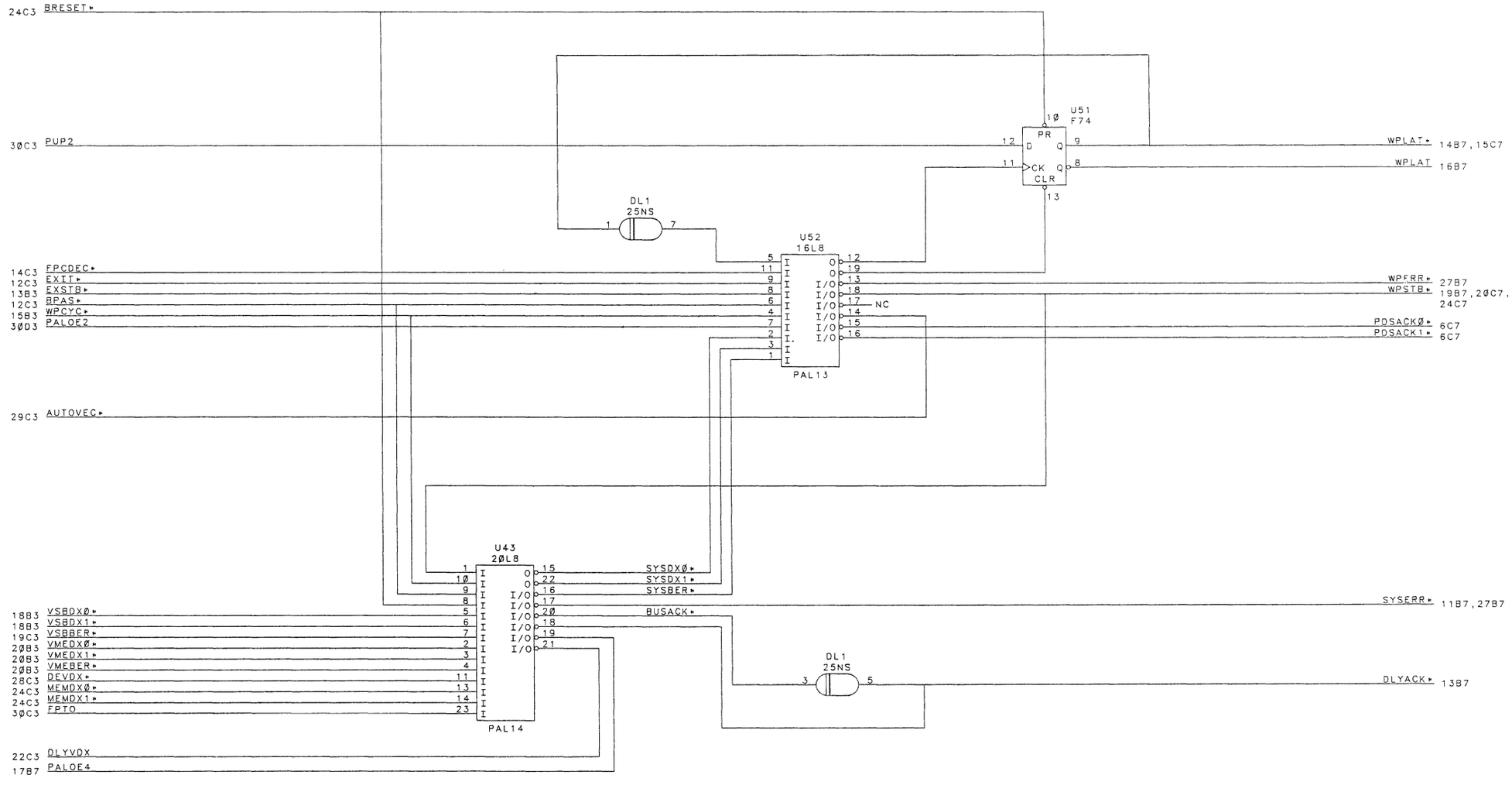
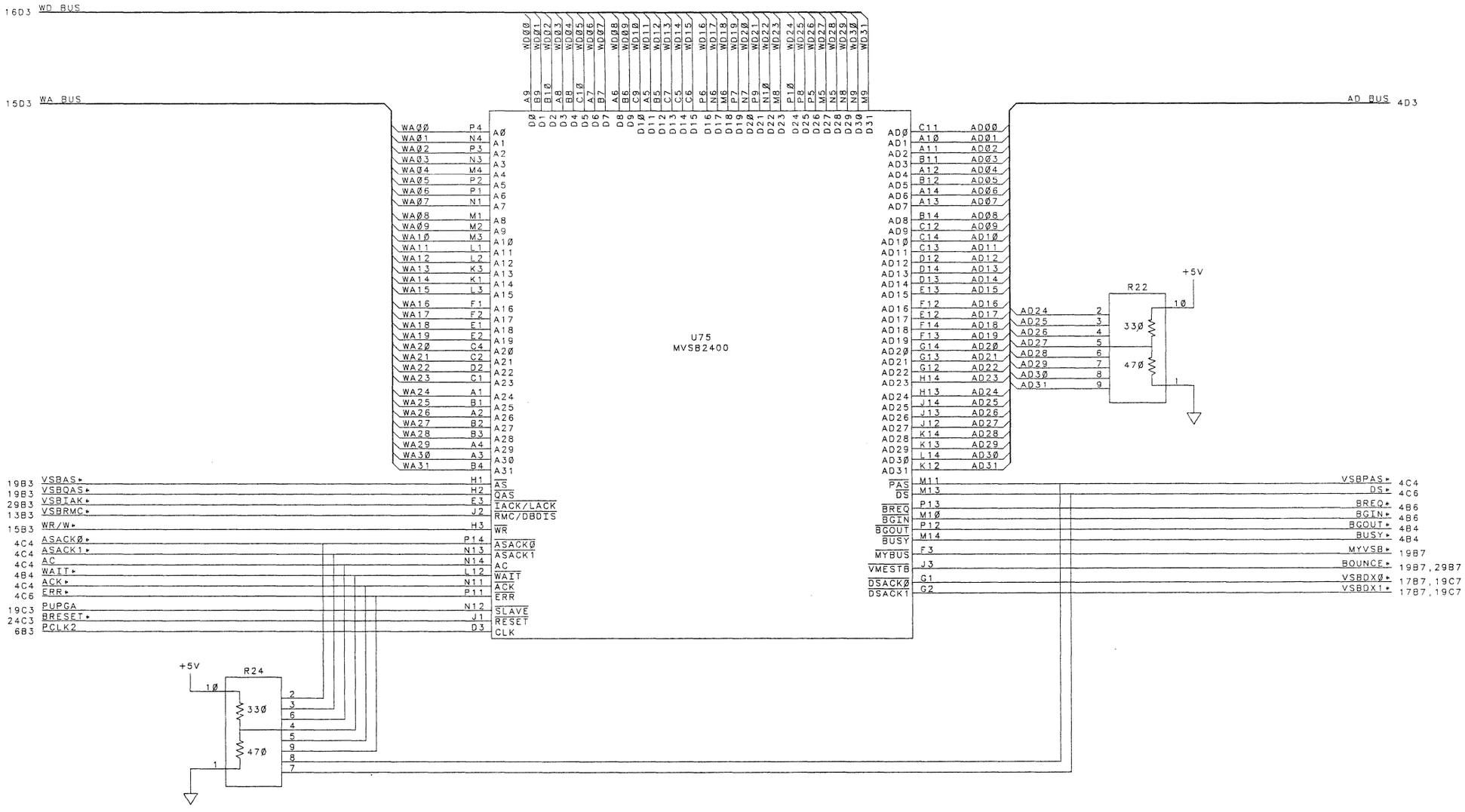
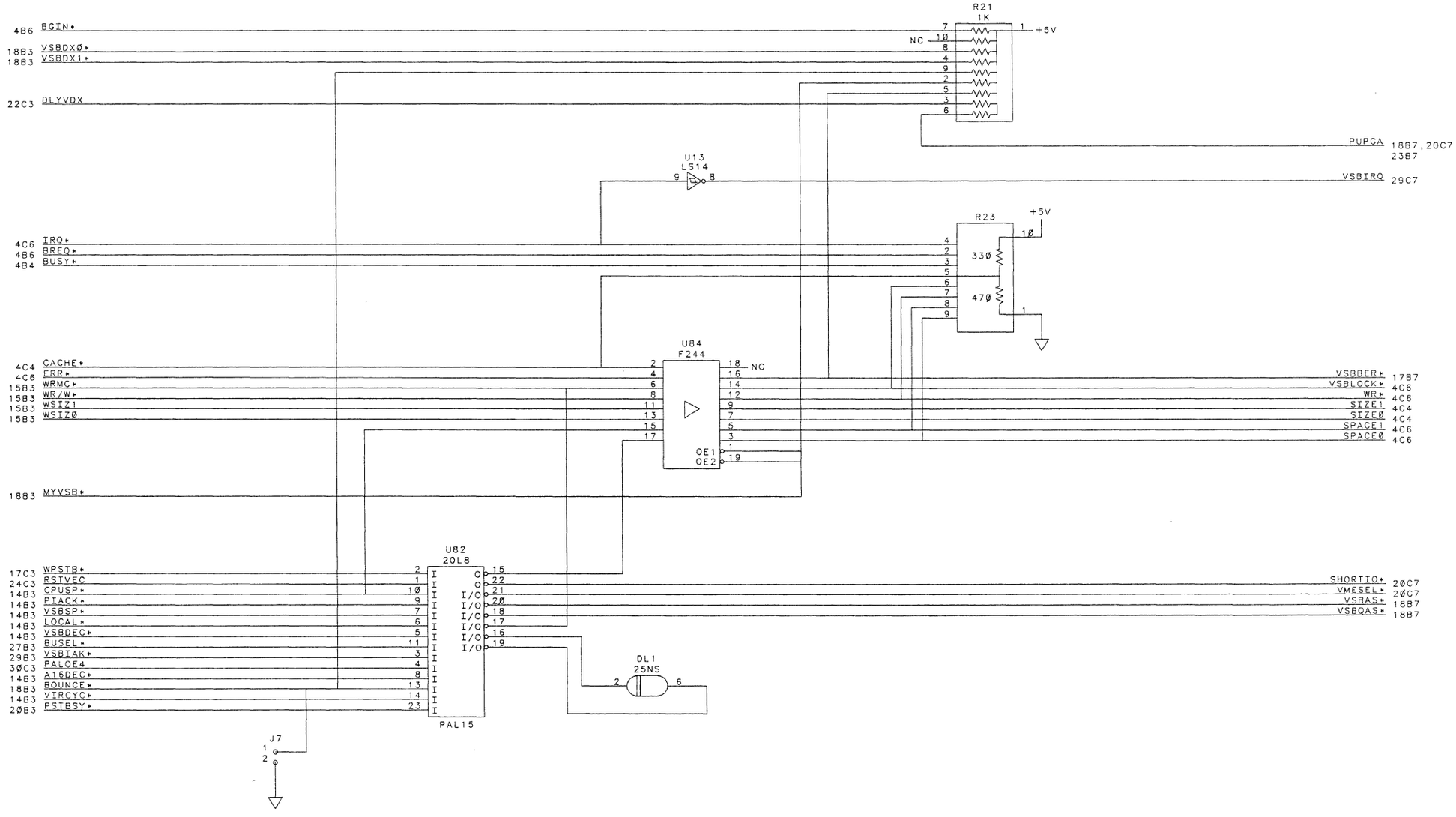


FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 17 OF 30)



VSB INTERFACE
63DW3528BØB REV A SH 18 OF 3Ø
JUN 2Ø 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 18 OF 3Ø)



VSB INTERFACE
63DW3528B0B REV A SH 19 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 19 OF 30)

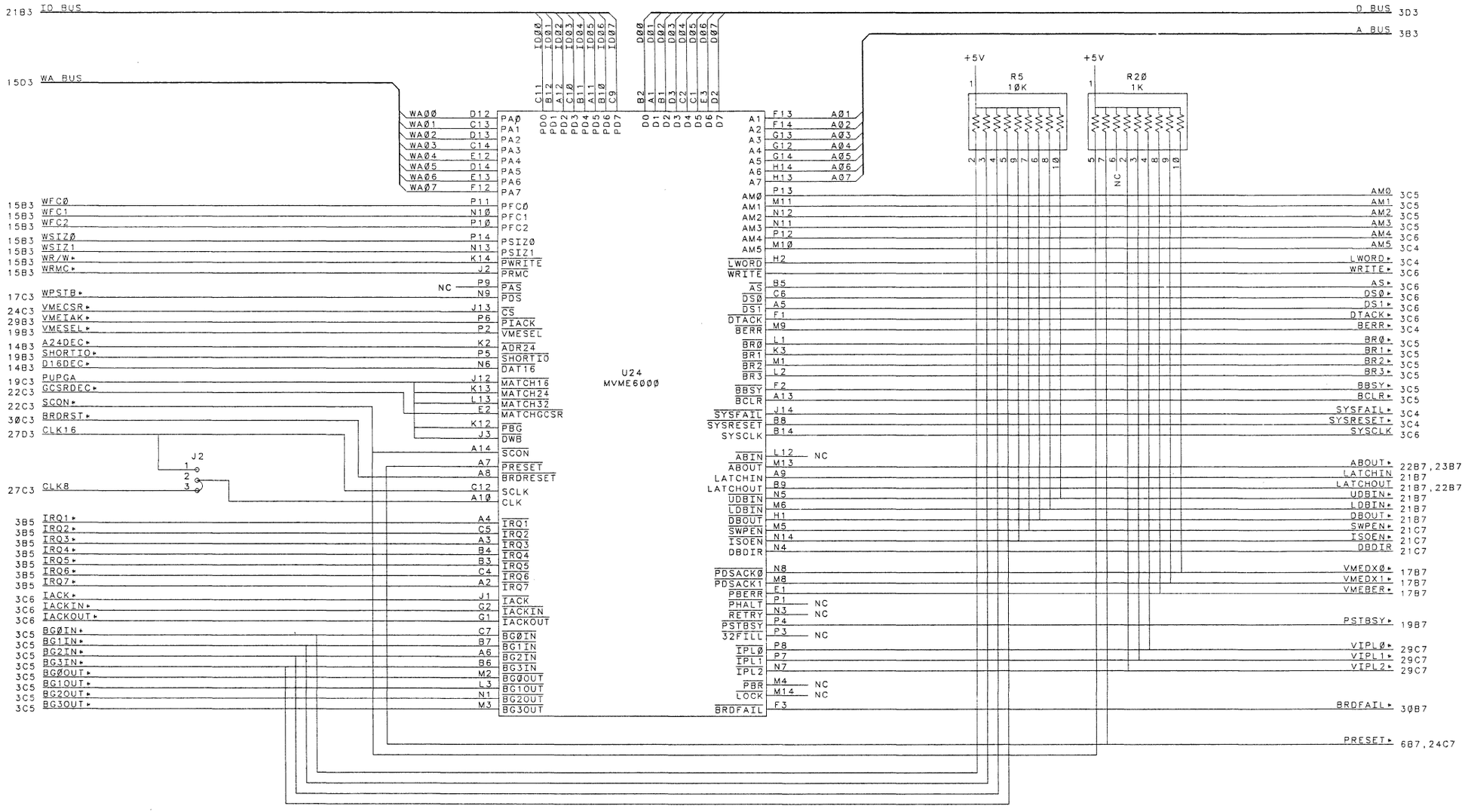
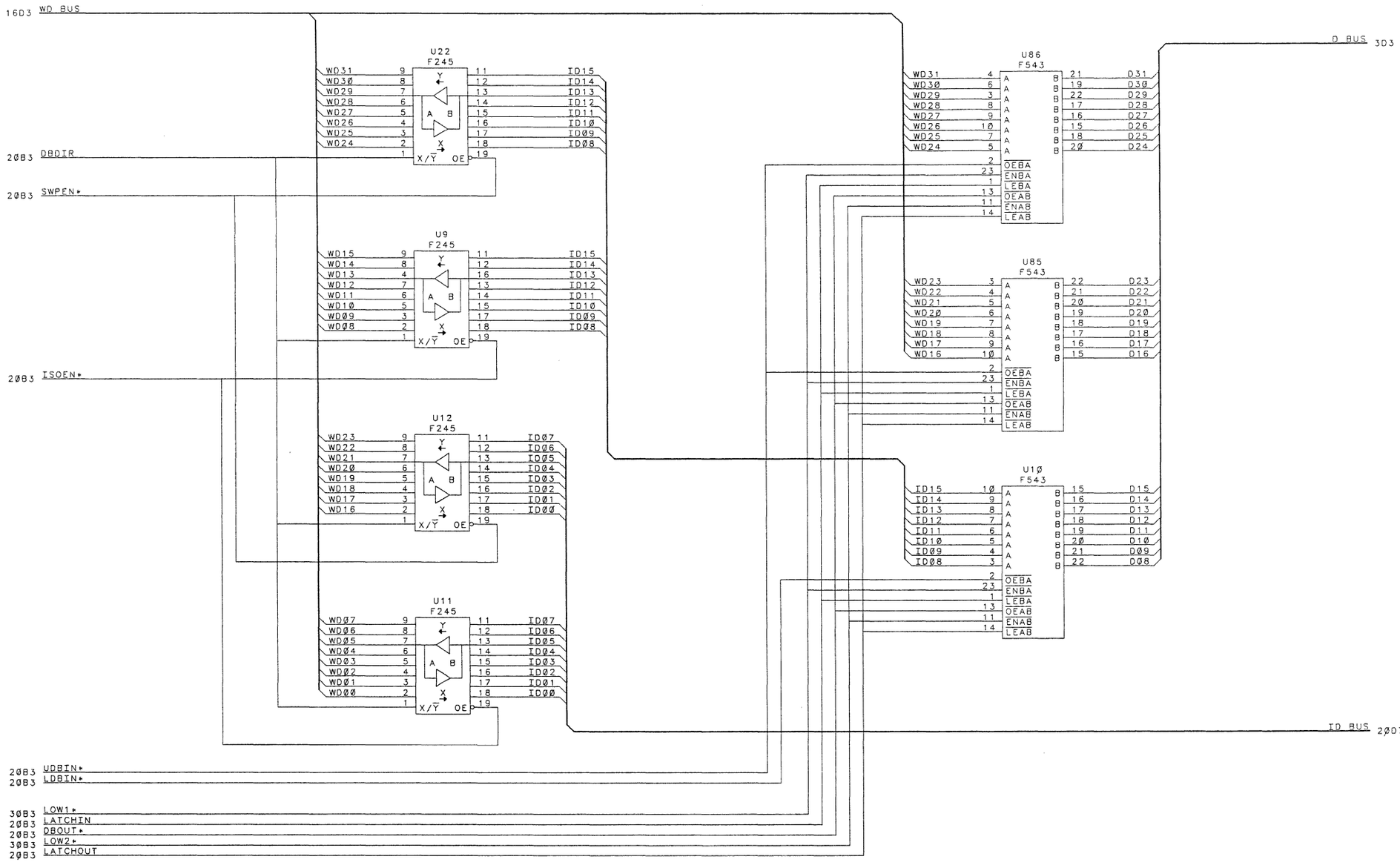
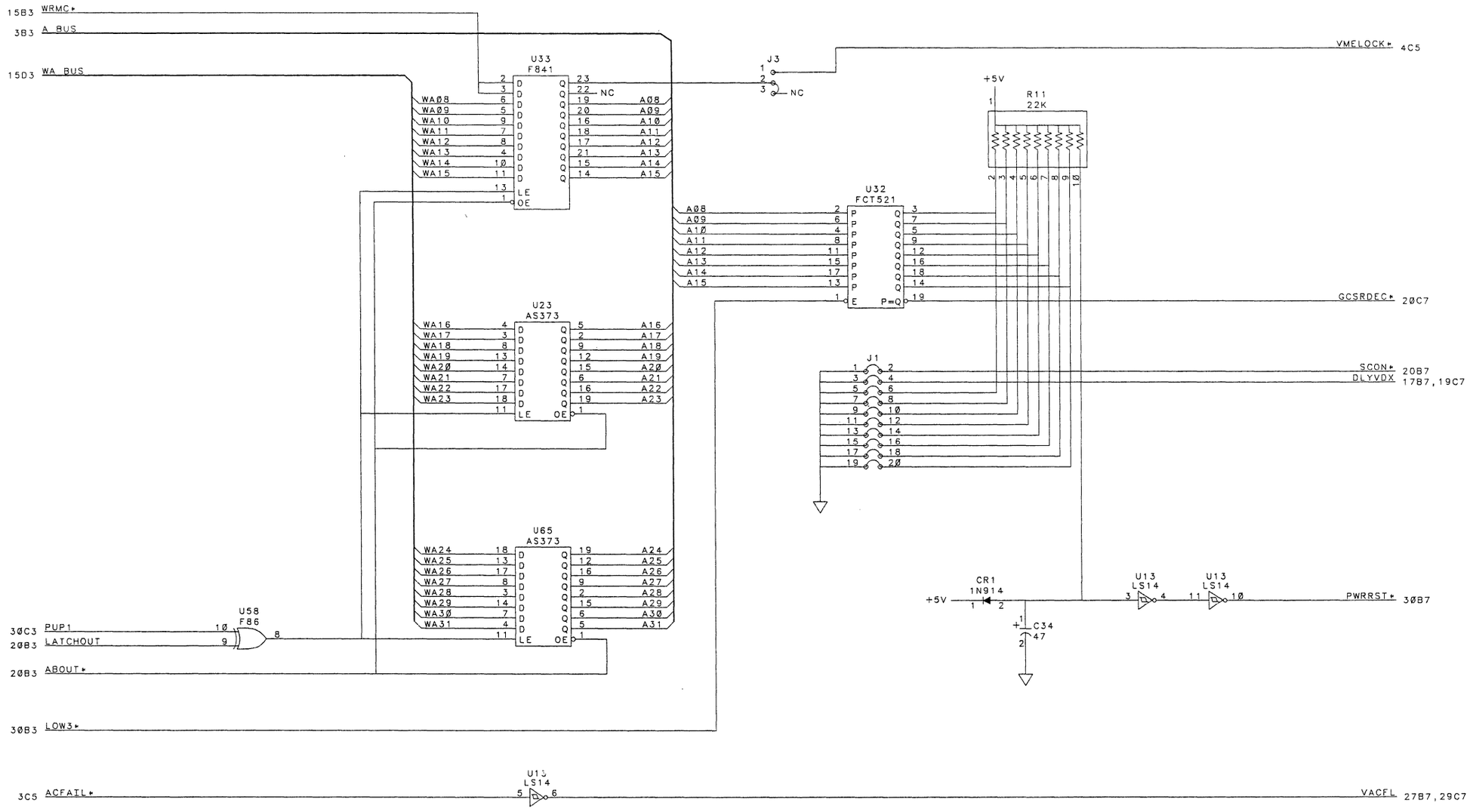


FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 20 OF 30)



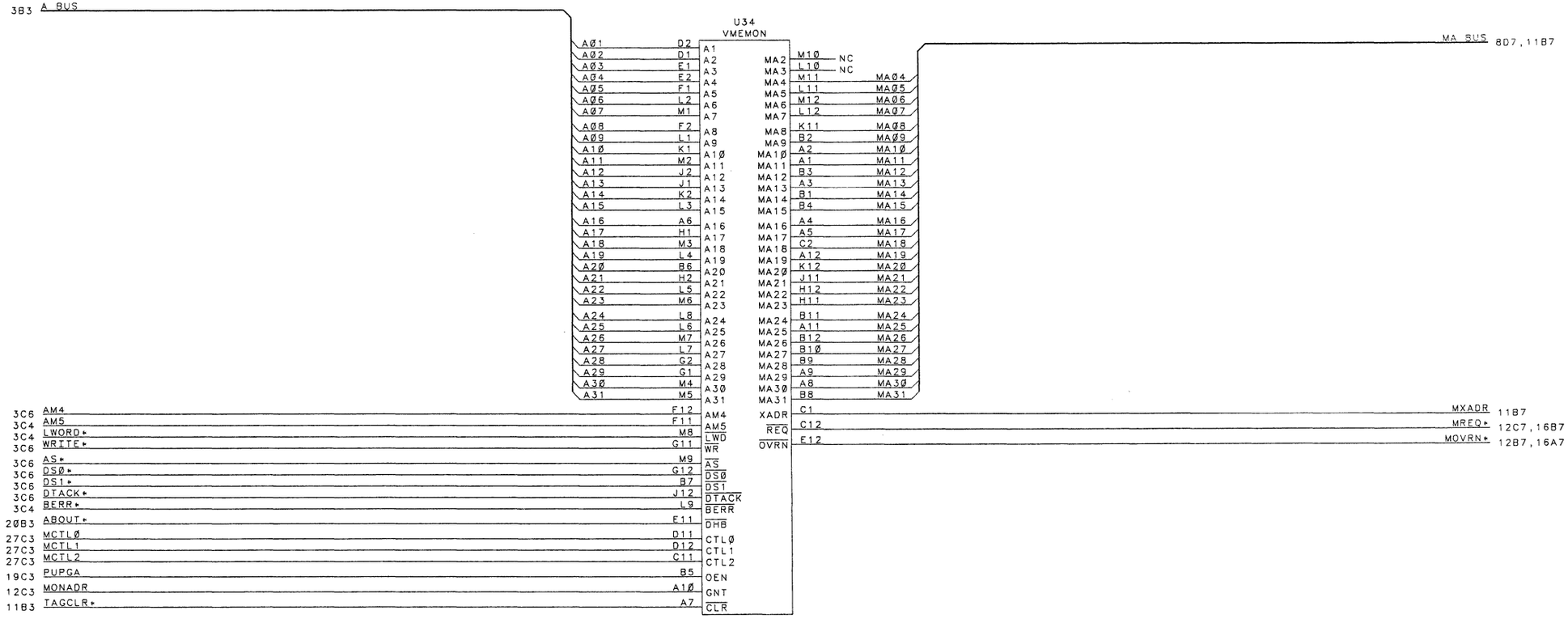
VME INTERFACE
63DW3528B0B REV A SH 21 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 21 OF 30)



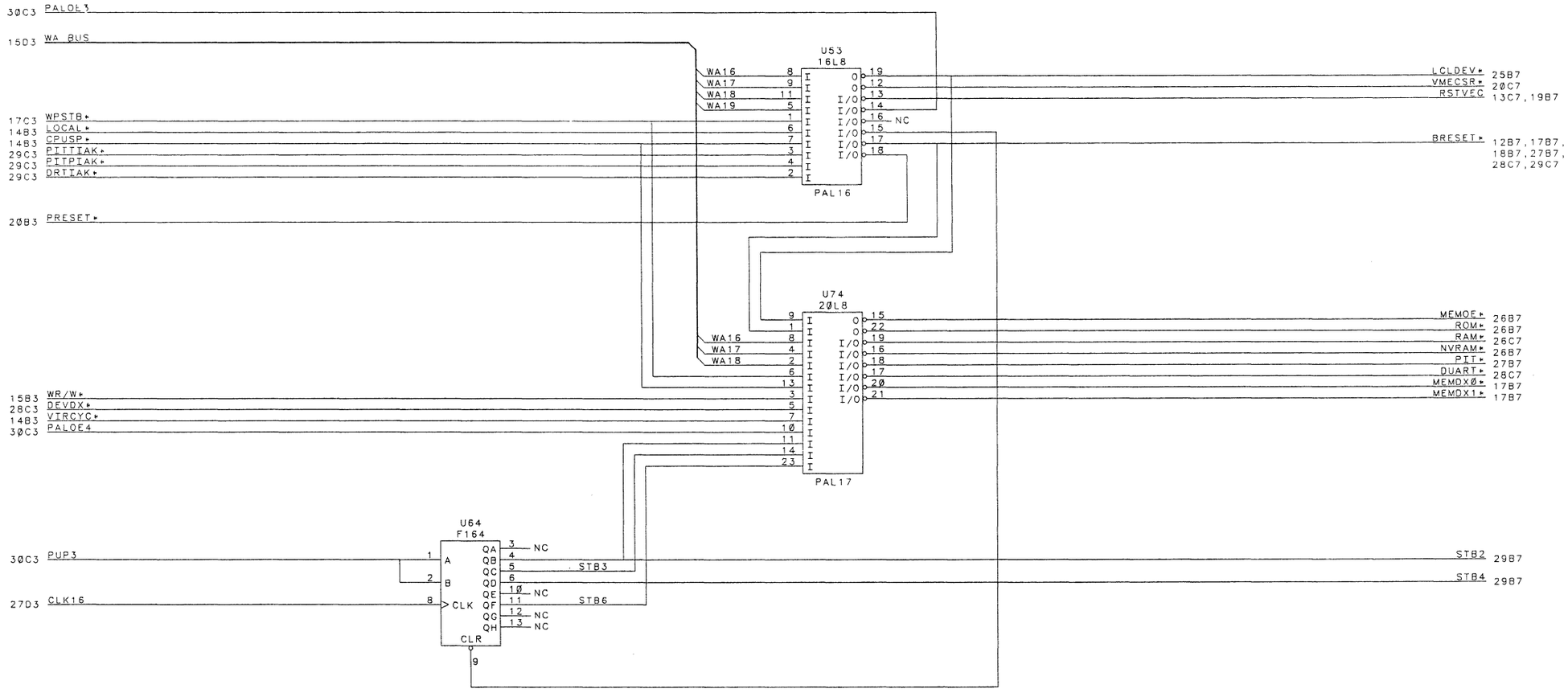
VME INTERFACE
63DW3528B0B REV A SH 22 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 22 OF 30)



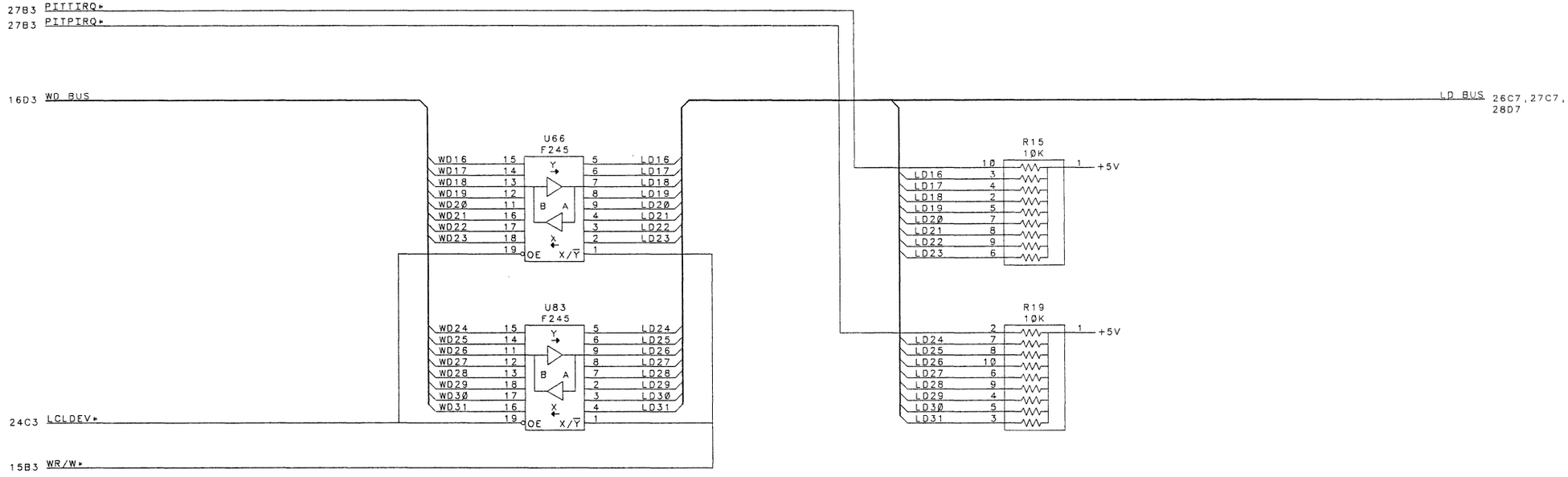
VME CACHE MONITOR
63DW3528B0B REV A SH 23 OF 30
~~JUN 20~~ ~~1988~~ VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 23 OF 30)



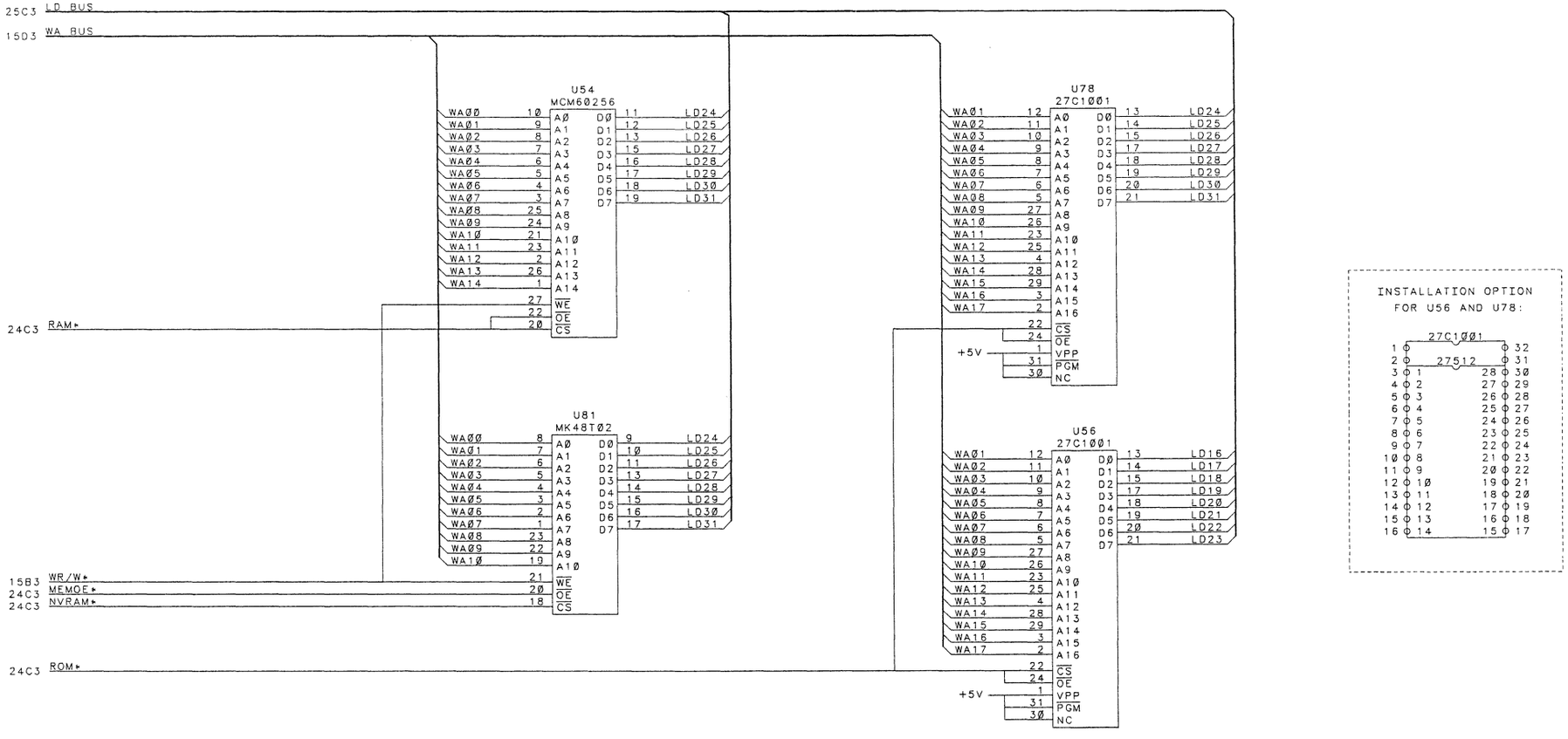
LOCAL INTERFACE
63DW3528B0B REV A SH 24 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 24 OF 30)



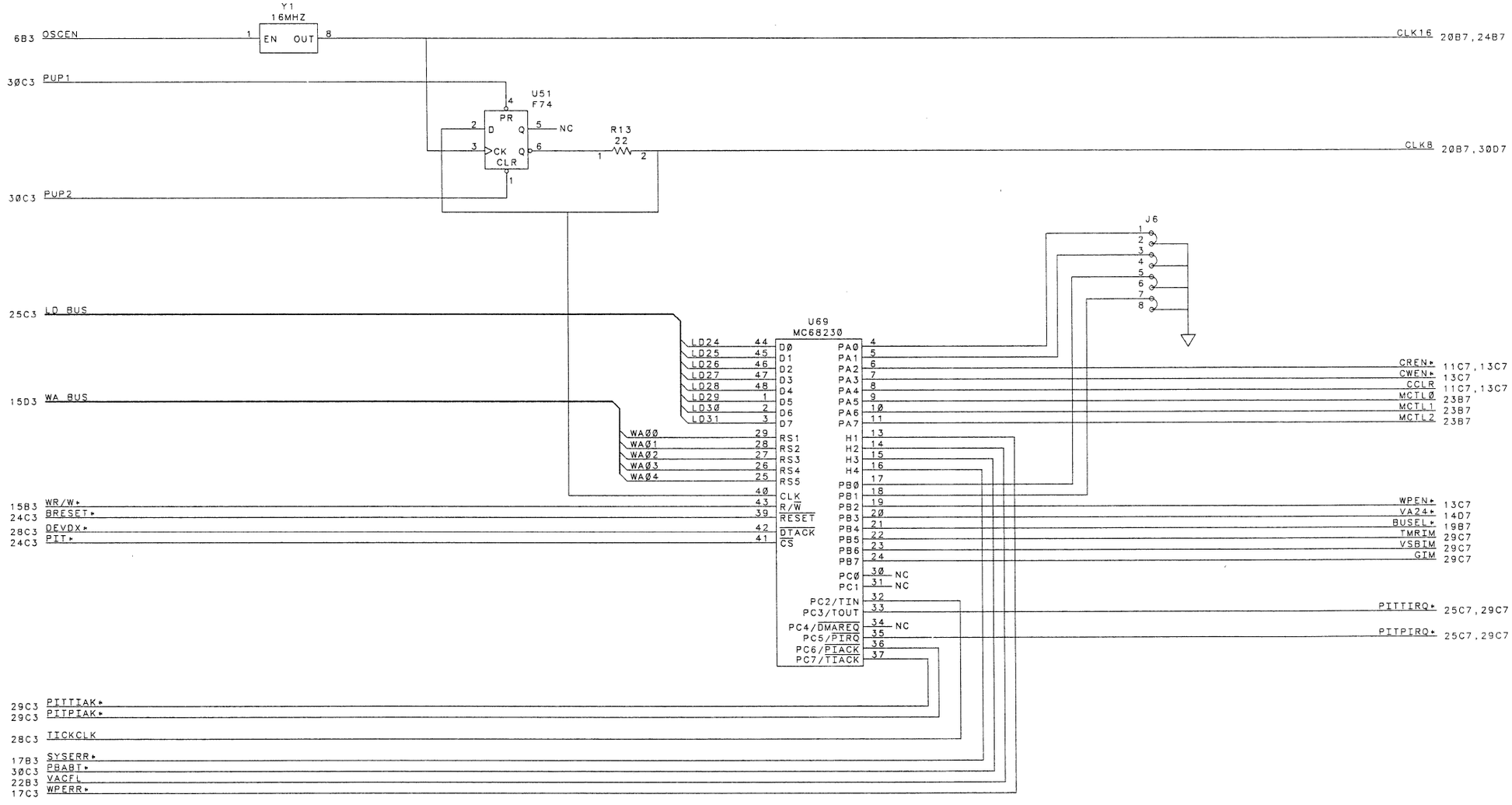
LOCAL INTERFACE
63DW3528B0B REV A SH 25 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 25 OF 30)



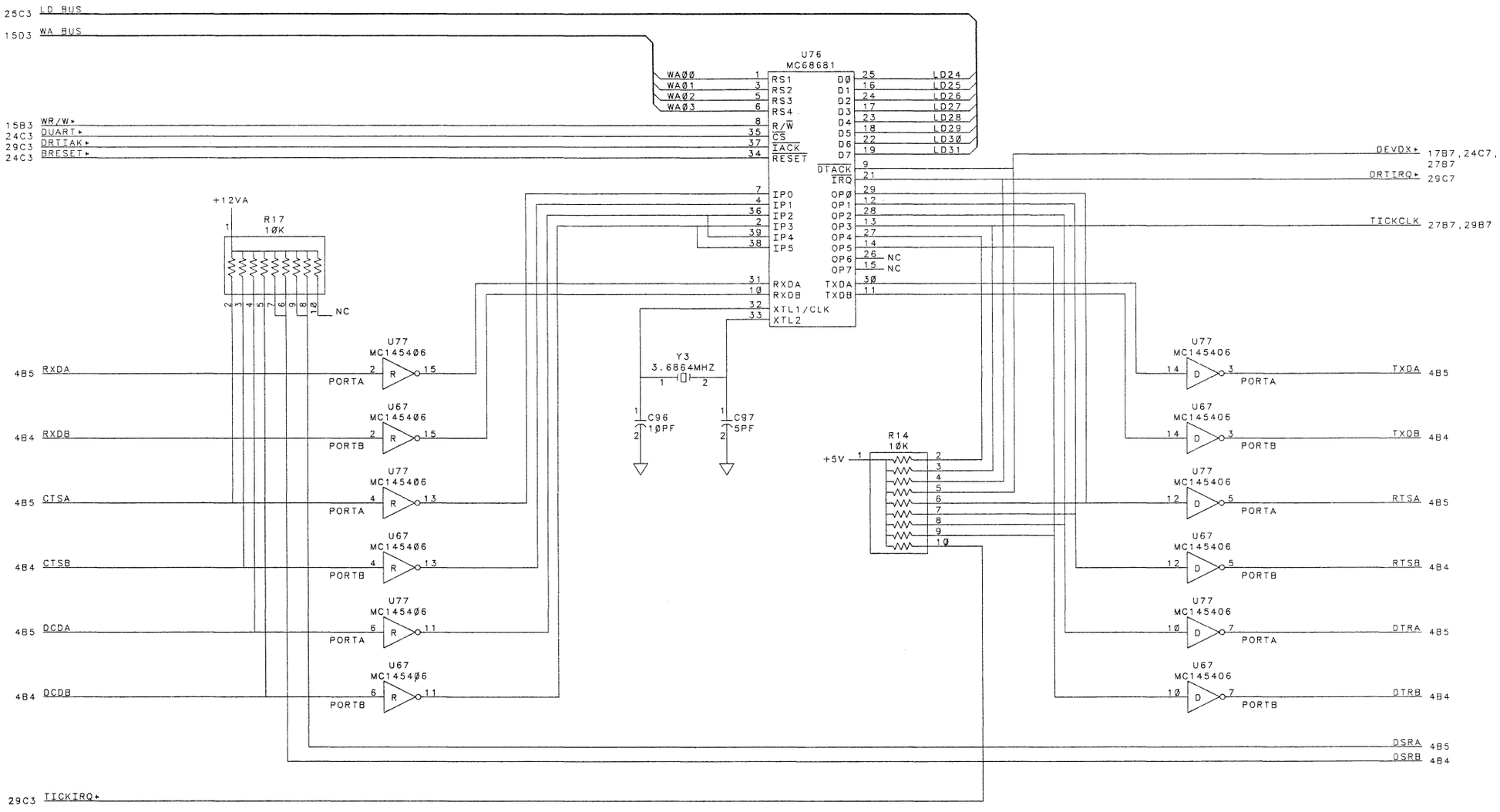
ROM/RAM
63DW3528B0B REV A SH 26 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 26 OF 30)



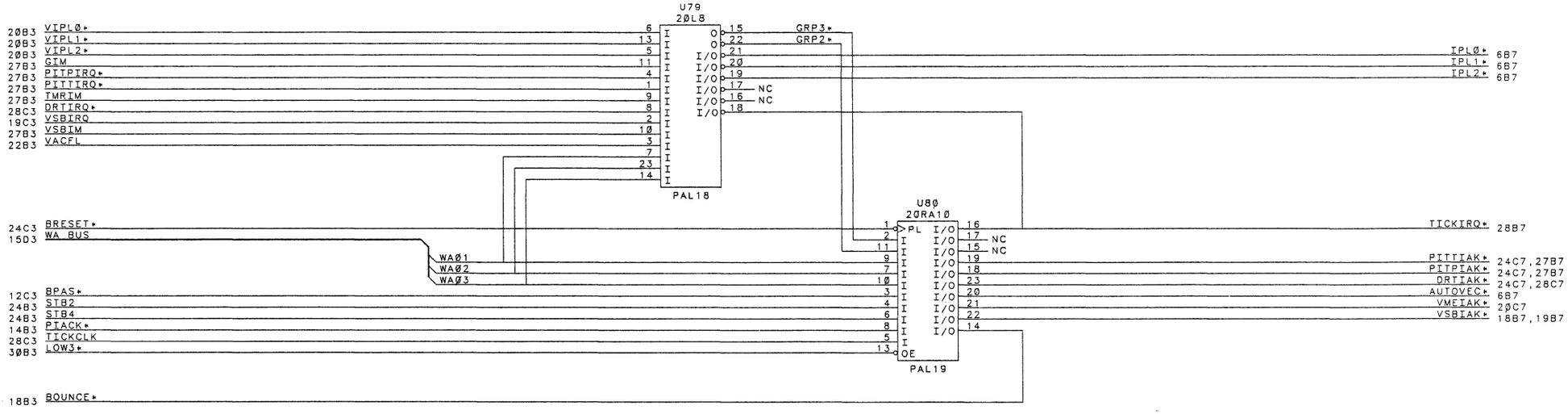
PI/T
63DW3528B0B REV A SH 27 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 27 OF 30)



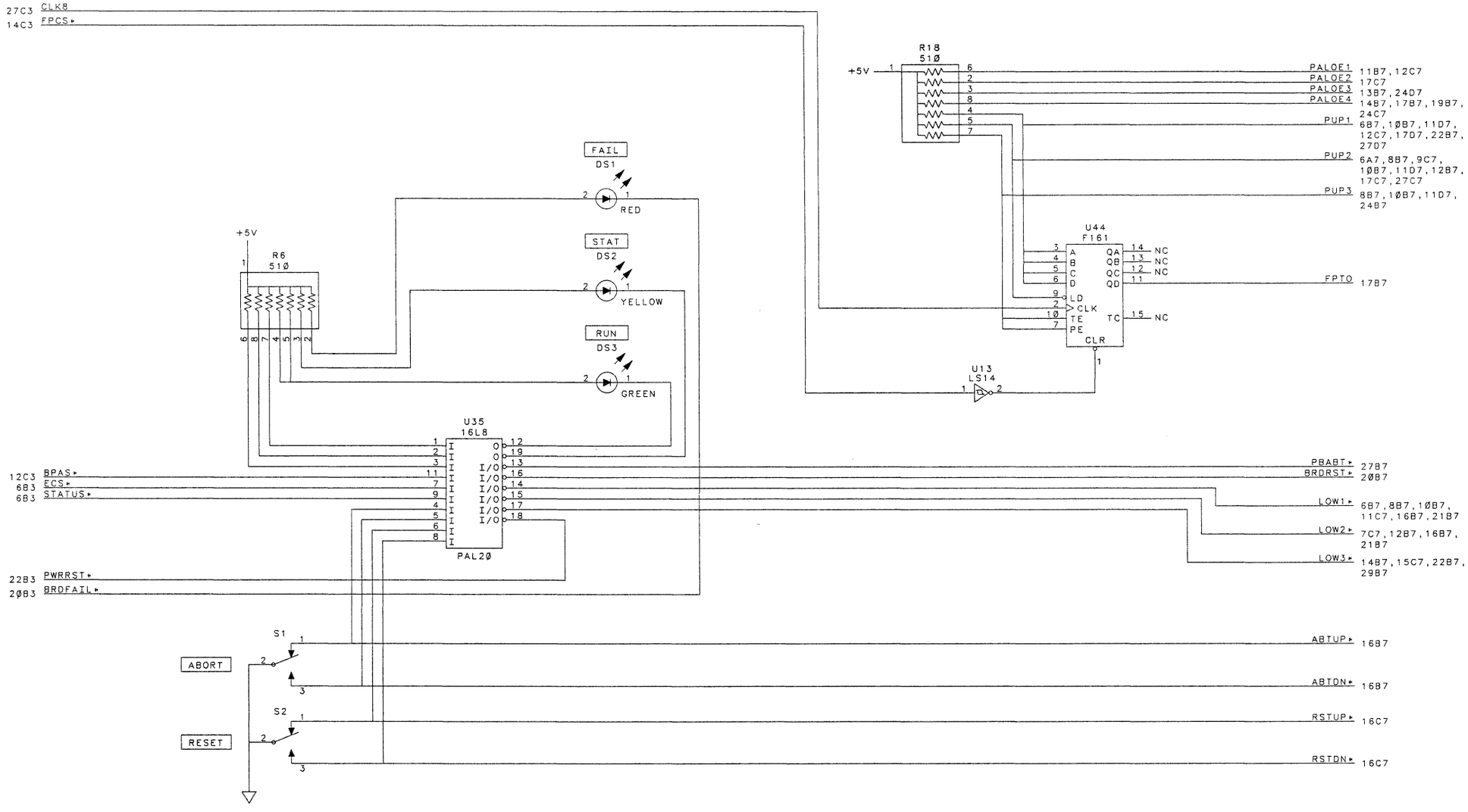
SERIAL PORTS
63DW3528B0B REV A SH 28 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 28 OF 30)



INTERRUPT HANDLER
63DW3528B0B REV A SH 29 OF 30
~~JUN 20 1988~~ VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 29 OF 30)



MISC
63DW3528B00B REV A SH 30 OF 30
JUN 20 1988 VME141

FIGURE 5-2. MVME141 SCHEMATIC DIAGRAM (SHEET 30 OF 30)

APPENDIX A - VMEchip LCSR BIT ASSIGNMENTS

	D7	D6	D5	D4	D3	D2	D1	DØ
$Ø1	-	-	-	-	ROBIN	BDFAIL	SRESET	SCON
$Ø3	DWB	DHB	RONR	RWD	RNEVER	-	RQLEV1	RQLEVØ
$Ø5	-	-	MASWP	CFILL	MASUAT	MASA16	MASA24	MASD16
$Ø7	SLVEN	-	SLVWP	-	-	-	-	SLVD16
$Ø9	-	ARBTO	VBTO1	VBTOØ	ACTO1	ACTOØ	LBTO1	LBTOØ
$ØB	SUPER	USER	EXTED	STND	SHORT	BLOCK	PROGRM	DATA
$ØD	AMSEL	-	AM5	AM4	AM3	AM2	AM1	AMØ
$ØF	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	-
$11	WPEREN	SFIEN	SIGHEN	LM1EN	IACKEN	LMØEN	SIGLEN	-
$13	UVB7	UVB6	UVB5	UVB4	UVB3	UVB2	UVB1	UVBØ
$15	-	-	-	-	-	IL2	IL1	ILØ
$17	DØ7	DØ6	DØ5	DØ4	DØ3	DØ2	DØ1	DØØ
$19	-	-	-	-	RMCERR	VBERR	ACTO	LBTO
$1B	-	-	-	-	GCSRA7	GCSRA6	GCSRA5	GCSRA4

A

VMEchip LCSR BIT ASSIGNMENTS

APPENDIX B - VMEchip GCSR BIT ASSIGNMENTS

	D7	D6	D5	D4	D3	D2	D1	DØ
$Ø1	LM3	LM2	LM1	LMØ	CHPID3	CHPID2	CHPID1	CHPIDØ
$Ø3	R&H	SCON	ISF	BDFAIL	-	-	SIGHP	SIGLP
$Ø5	BRDID7	BRDID6	BRDID5	BRDID4	BRDID3	BRDID2	BRDID1	BRDIDØ
$Ø7	GENERAL PURPOSE CSR Ø							
$Ø9	GENERAL PURPOSE CSR 1							
$ØB	GENERAL PURPOSE CSR 2							
$ØD	GENERAL PURPOSE CSR 3							
$ØF	GENERAL PURPOSE CSR 4							

VMEchip GCSR BIT ASSIGNMENTS

B

APPENDIX C - VSB CSR BIT ASSIGNMENTS

FFFAØØØ2

D15							D8
ERR*	ASACK1*	ASACKØ*	TIMOUT	WRERR*	FAIR*	ENTOØ	ENTO1

FFFAØØØ3

D7							DØ
-	MASEN*	RDONLY*	BOUNCE	TEN*	BLKEN*	-	SCON*

VSB CSR BIT ASSIGNMENTS

C

SUGGESTION/PROBLEM REPORT

Motorola welcomes your comments on its products and publications. Please use this form.

To: Motorola Inc.
Microcomputer Division
2900 S. Diablo Way
Tempe, Arizona 85282
Attention: Publications Manager
Maildrop DW164

Product: _____ Manual: _____

COMMENTS: _____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

(For additional comments use other side)

Please Print

Name _____ Title _____

Company _____ Division _____

Street _____ Mail Drop _____

City _____ Phone _____

State _____ Zip _____ Country _____

For Additional Motorola Publications
Literature Distribution Center
616 West 24th Street
Tempe, AZ 85282
(602) 994-6561

Motorola Field Service Division/Customer Support
(800) 528-1908
(602) 438-3100

COMMENTS: _____

MOTOROLA INC.

Microcomputer Division
2900 South Diablo Way
Tempe, Arizona 85282
P.O. Box 2953
Phoenix, Arizona 85062

Motorola is an Equal Employment
Opportunity/Affirmative Action Employer

10367 PRINTED IN USA (10/88) MPS 1500

68NW9209E94A