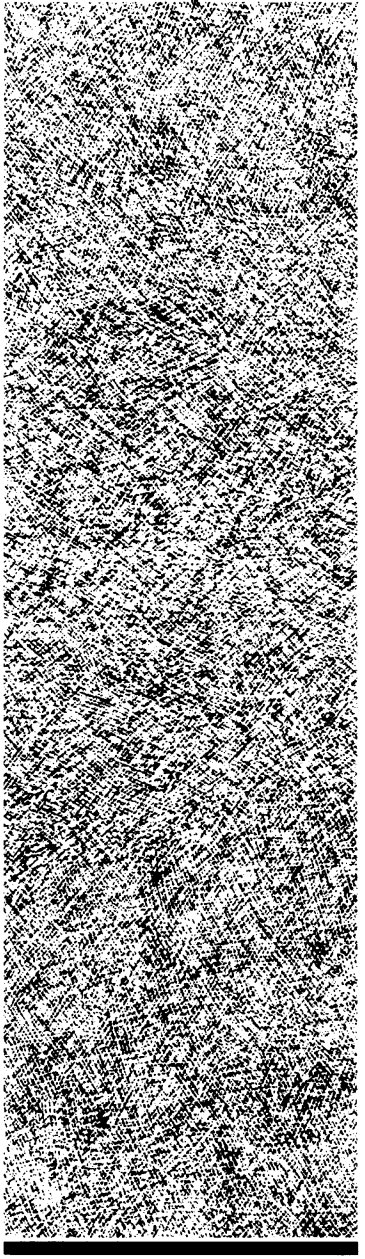
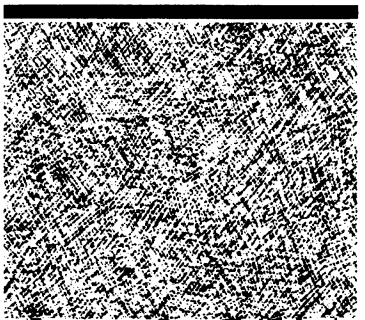


MOTOROLA



MVME117/D3

MVME117
MPU VMEmodule
User's Manual

MVME117

MPU VMEmodule

USER'S MANUAL

(MVME117/D3)

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, Motorola reserves the right to make changes to any products herein to improve reliability, function, or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights or the rights of the others.

PREFACE

This manual provides general information, hardware preparation, installation instructions, operating instructions, functional description, and support information for the MVME117 MPU VMEmodule.

This revision (D3) corrects minor errors and eliminates the MVME708–1 Transition Module information from this manual. The MVME708–1 is presented in a separate manual.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

Throughout this manual the paragraph headings conform to the following convention:

DETAILED DESCRIPTION	(this is a main topic heading)
MC68010 Microprocessor Unit (MPU)	(this is a subordinate topic heading under a main topic)
Local Accesses	(this is a subordinate topic heading under the subordinate topic)

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WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

Third Edition January 1989

Second Edition May 1987

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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CHAPTER 3 - OPERATING INSTRUCTIONS

CHAPTER 4 - FUNCTIONAL DESCRIPTION

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CHAPTER 1 – GENERAL INFORMATION

INTRODUCTION

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the MVME117 MPU VMEmodule.

MODEL DESIGNATIONS

The MVME117 is available in several configurations which are summarized in the following table. The main differences between the versions is incorporation of the MC68881 device and SCSI availability.

MVME117 Model Designations

PRODUCT NUMBER	RAM CHIP SIZE (BITS)	ONBOARD MEMORY (BYTES)	SCSI (Y/N)	MC68881
MVME117-03	256K x 1	512K	Y	N
MVME117-04	256K x 1	512K	N	N
MVME117-3FP	256K x 1	512K	Y	Y

FEATURES

The features of the MVME117 include:

- MC68010 10 MHz microprocessor
- Socket for MC68881 floating point processor (chip is provided onboard for MVME117-3FP only; user may supply chip for MVME117-3 or -4)
- Zero wait state dynamic RAM (512K) with parity disabled; one wait cycle with byte parity enabled
- One multiprotocol RS-232C serial port through P2 connector
- One asynchronous front panel debug serial port J6 (to terminal only)

- Two independent 8-bit input or output parallel ports with two handshake lines each through P2 connector (may be configured together as a Centronics printer port)
- Small Computer Systems Interface (SCSI) bus interface through P2 connector (for firmware details refer to the *SCSI Firmware User's Manual*, MVMESCSIFW) (no SCSI chip on MVME117-4 module)
- Time-of-day clock/calendar with battery backup
- Battery backed up 2K by 8 (or user-substituted 8K by 8) CMOS RAM
- MC68B40 triple 16-bit timers: tick timer, watchdog timer, user timer
- Interrupt handler for onboard and offboard interrupt sources
- System controller functions (can be jumper disabled) include SYSCLK, Bus Time-Out (BTO), single-level bus arbiter, and system reset generator
- Four 28-pin JEDEC-standard ROM/EPROM sockets for 8K x 8 to 64K x 8 parts
- Bus requester, with Release-On-Request or Release-When-Done
- Status LEDs for HALT, RUN and FAIL
- RESET and ABORT switches
- Remote reset connection through P2 connector
- Eight bits of software-readable board configuration number (in PROM U93)
- Eight-position software-readable front panel switch
- The MVME117 can be run stand-alone (without VMEbus chassis) using only terminal, power supply, and optional SCSI disk

SPECIFICATIONS

The MVME117 specifications are given in Table 1-1.

TABLE 1-1. MVME117 Module Specifications

CHARACTERISTICS	SPECIFICATIONS
Power requirements (MVME117 with full set of ROM/EPROM and RAM)	+5 Vdc, 4.4 A max. (4.1 A typical) +12 Vdc, 50 mA max. (10 mA typical) -12 Vdc, 50 mA max. (10 mA typical)
Microprocessor	MC68010
Clock signal	10 MHz to MPU
Addressing	
Total address range (on and offboard)	16Mb
ROM/EPROM	Four ROM/EPROM sockets for 8K x 8, 16K x 8, 32K x 8, or 64K x 8 devices
Dynamic RAM	512Kb
I/O ports	
Serial	One multiprotocol serial port connected through P2 One asynchronous debug serial port (J6 on front panel) DCE (to terminal) interface only
Parallel	Parallel I/O/Centronics printer port connected through P2
Timers	4 total
Time-of-day clock	4 bit (with 0.1 second resolution)
Watchdog timer	16 bit (tick timer output is watchdog timer input)
User timer	16 bit
Tick timer	16 bit
Bus configuration	Data Transfer Bus (DTB) master, with 24-bit address (A24) and 16-bit data (D16)

TABLE 1-1. MVME117 Module Specifications (cont'd)

CHARACTERISTICS	SPECIFICATIONS
Interrupt handler	Any or all onboard plus up to seven VMEbus interrupts
Bus arbitration	When the MVME117 is the system controller, it arbitrates bus requests and bus grants on level 3 only
Reset	RESET switch or remote reset input resets the MC68010. If the MVME117 is the system controller, it also activates SYSRESET* (system reset) on the VMEbus
Operating temperature	0 degrees to 55 degrees C at point of entry of forced air (approximately 5 CFM)
Storage temperature	-40 degrees to 85 degrees C
Relative humidity	5% to 90% (non-condensing)
Physical characteristics (excluding front panel)	
Height	9.187 inches (233.35 mm)
Width	6.299 inches (160.0 mm
Thickness	0.063 inches (1.6 mm)

Cooling Requirements

Motorola VMEmodules are specified, designed, and tested to operate reliably with an incoming air temperature range from 0 degrees C to 55 degrees C (32 degrees F to 131 degrees F) with forced air cooling. Temperature qualification is performed in a standard Motorola VMEsystem 1000 chassis. Twenty-five watt load boards are inserted in the two card slots, one on each side, adjacent to the board under test to simulate a high power density system configuration. An assembly of three axial fans, rated at 71 CFM per fan, is placed directly under the MVME card cage. The incoming air temperature is measured between the fan assembly and the card cage where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to

ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 5 CFM flowing over the module. Less air flow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions it may be possible to operate the module reliably at higher than 55 degrees C with increased air flow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume of air flowing over a module.

FCC Compliance

This VMEmodule (MVME117) was tested in an FCC-compliant chassis, and meet the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

a. Shielded cables on all external I/O ports.

b. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.

c. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.

d. Front panels screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the modules.

GENERAL DESCRIPTION

The MVME117 is a double-high VMEmodule. The module has high functionality with large onboard RAM (512Kb), serial ports, parallel/printer port, SCSI bus controller (MVME117-3, -3FP), floating point processor (MVME117-3FP), tick timer, watchdog timer, time-of-day clock/calendar with battery backup, and VMEbus interface with system controller functions.

The MVME117 can be operated in stand-alone mode without being part of a VMEbus system with other VMEmodules such as RAM modules, CPU modules, graphics modules, and analog I/O modules.

RELATED DOCUMENTATION

The following manuals are applicable to the MVME117. If these manuals are not shipped with this product, they may be purchased from the Motorola Literature Distribution Center, 616 West 24th Street, Tempe, AZ 85282; telephone (602) 994-6561. Non-Motorola documents may be obtained from the sources listed.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
MVME117 Firmware Debug Monitor User's Manual	MVME117BUG
Small Computer Systems Interface (SCSI) Firmware User's Manual	MVMESCSIFW
MVME708 Transition Module and MVME117/MVME117A P2 Adapter Board User's Manual	MVME708
MC6840 Programmable Timer Fundamentals and Applications	MC6840UM
MC68010 16-Bit Virtual Memory Microprocessor Data Book	MC68010
M68000 16/32-Bit Microprocessor Programmer's Reference Manual	M68000UM
Software Links Math Chip to 68000-Family uPs	AR233
MC68881/MC68882 Floating-Point Coprocessor User's Manual	MC68881UM

NOTE: Although not shown in the above list, each Motorola MCD manual publication number is suffixed with characters which represent the revision level of the document, such as "/D2" (the second revision of a manual); a supplement bears the same number as the manual but has a suffix such as "/A1" (the first supplement to the manual).

The following publications are available from the sources indicated.

MM58274 Real-Time Clock; data sheet and application note 365; National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, CA 95051

Z8530 Serial Communications Controller; data sheet; Zilog, Inc., Corporate Communications, Building A, 1315 Dell Ave, Campbell, California 95008

NCR 5380 SCSI Interface Chip; data sheet; NCR Microelectronics Division, 1635 Aeroplaza Drive, Colorado Springs, Colorado 80916

SCSI Small Computer System Interface; draft X3T9.2/82-2 - Revision 14; Computer and Business Equipment Manufacturers Association, 311 First Street, N.W., Suite 500, Washington, D.C. 20001

MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2 – HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

INTRODUCTION

This chapter provides the unpacking, hardware preparation, and installation instructions for the MVME117.

UNPACKING INSTRUCTIONS

NOTE

If the carton is damaged upon receipt, request carrier's agent be present during unpacking/inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

HARDWARE PREPARATION

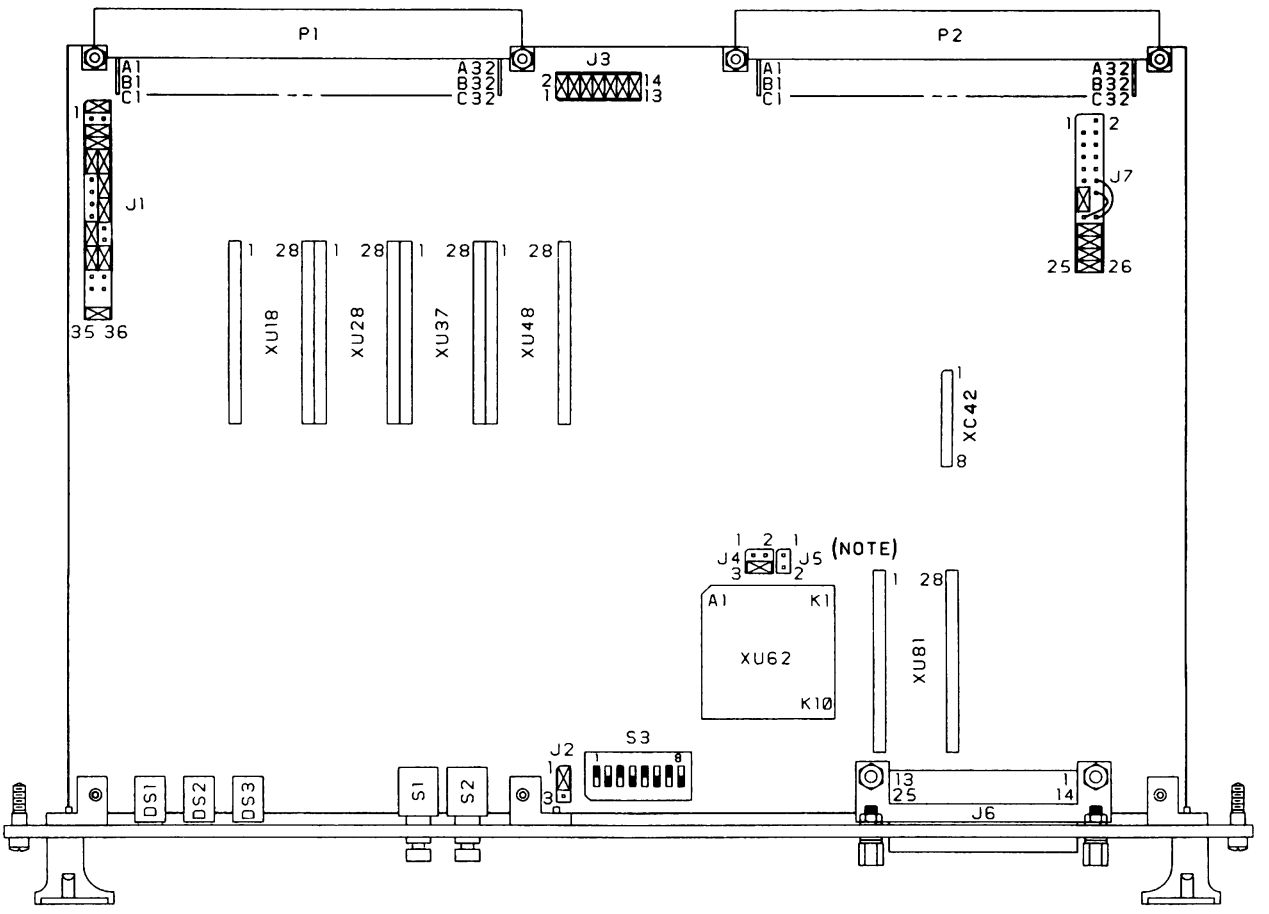
To select the desired configuration and ensure proper operation of the MVME117, certain modifications may be made before installation. These changes are made through jumper or wire wrap arrangements on the headers, switch settings, and terminator resistor installation/removal. The location of the headers, switches, LEDs, and connectors on the MVME117 is illustrated in Figure 2–1. The module has been factory tested and is shipped with factory–installed jumper configurations that are described in the following paragraphs with each header description. The module is operational with factory–installed jumper configurations. Headers J1 through J5, and J7, and switch S3 are factory–configured as shown below.

• Bus request and bus grant levels	J1-21 to 23, 1 to 2, 5 to 6, 7 to 8, 9 to 11, 10 to 12	BR3*, BG3IN*, and BG3OUT* enabled
• ROM/EPROM pinout address select	J1-14 to 16, 18 to 20, 26 to 28	64K x 8 chips for XU18, XU28, XU37, and XU48
• ROM/EPROM access time (speed) select	J1-25 to 27	fast chips (less than 250 ns, one wait cycle)
• ROM/EPROM size select	no jumpers J1-29 through 32	64K x 8 chips
• System controller enable	J1-35 to 36	MVME117 module is system controller
• Factory header (RAM size)	J2-1 to 2 (NOTE 1)	512Kb (256K-bit chips)
• VMEbus interrupt requests (IRQ) enable	J3-1 to 2, 3 to 4, 5 to 6, 7 to 8, 9 to 10, 11 to 12, 13 to 14	IRQ1* through IRQ7* enabled for offboard interrupts
• Floating point processor clock select	J4-3 to 4	10 MHz clock to the floating point processor
• Battery backup connection	no jumper from J5-1 to 2 (NOTE 2)	disables backup battery
• Serial port jumpers	no jumpers J7-3 through 10; but J7-12 to 18, 14 to 17	asynchronous P2 port; DTRA & RTSA connected
• CMOS RAM pinout select	J7-13 to 15	2K x 8 CMOS RAM U81 in socket XU81
• Parallel port jumpers	J7-19 to 20, 21 to 22	ports 0 & 1 interrupt on low level pulses
• ABORT switch enable	J7-23 to 24	ABORT switch S1 enabled

• RESET switch enable	J7–25 to 26	RESET switch S2 enabled
• Readable switch S3	S3–1, –3, –5, –7 up (open); –2, –4, –6, –8 down (closed)	SRSW register reads alternating 1's and 0's

NOTES: 1. Jumper at J2 is soldered trace. Do not cut this trace.

2. The jumper at J5 is shipped in kit 67–W2287B01 and may be installed by the user.



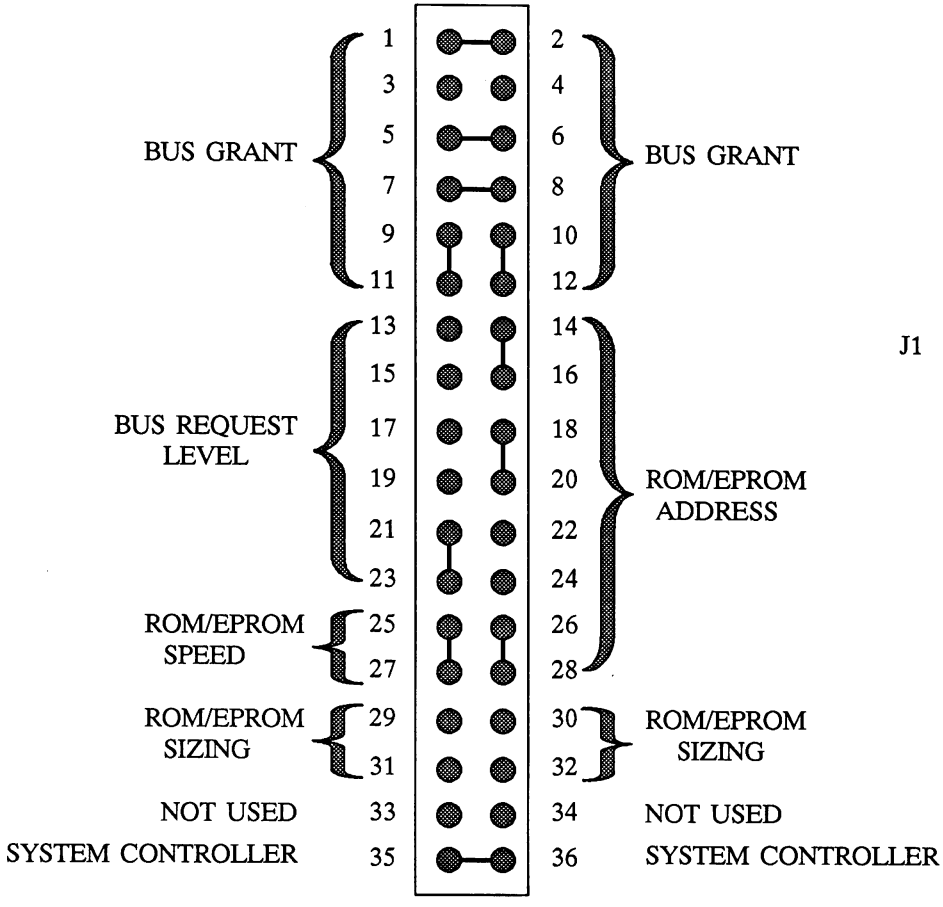
NOTE: THE JUMPER AT J5 IS SHIPPED IN KIT 67-W2287B01 AND INSTALLED BY THE USER.

FIGURE 2-1. MVME117 Header Locations

Bus Request Level (Part of J1)

Pins J1–13, 15, 17, 19, 21, and 23 are used to select the proper bus request level. Only one level may be enabled on the module at one time. The module is shipped with pin J1–21 connected to J1–23, enabling Bus Request level 3 (BR3*), the highest possible level. The jumpers for all levels are:

BR3*	J1–21 to J1–23
BR2*	J1–19 to J1–21
BR1*	J1–15 to J1–17
BR0*	J1–13 to J1–15



If the MVME117 is enabled as the system controller, the bus requester must be set for level 3 to correspond to the arbiter, which is level 3 only. If the MVME117 is used with an external arbiter, the onboard system controller functions must be disabled per the *System Controller Enable* paragraph in this chapter. In either case, the bus request level must match the bus grant level selected per the *Bus Grant Level* paragraph in this chapter.

Bus Grant Level (Part of J1)

The bus grant pins are J1-1 through J1-12. The as-shipped configuration is J1-1 to J1-2, J1-5 to J1-6, J1-7 to J1-8, J1-9 to J1-11, and J1-10 to J12. This enables Bus Grant 3 In (BG3IN*) and Bus Grant 3 Out (BG3OUT*), the highest level. The jumpers for each level are:

BG3IN*, BG3OUT*	J1-1 to J1-2, 5 to 6, 7 to 8, 9 to 11, 10 to 12
BG2IN*, BG2OUT*	J1-1 to J1-2, 5 to 6, 7 to 9, 8 to 10, 11 to 12
BG1IN*, BG1OUT*	J1-1 to J1-2, 3 to 5, 4 to 6, 7 to 8, 11 to 12
BG0IN*, BG0OUT*	J1-1 to J1-3, 2 to 4, 5 to 6, 7 to 8, 11 to 12

ROM/EPROM Pinout Address Select (Part of J1)

The ROM or EPROM address is selected using four combinations of jumpers on pins J1-14, 16, 18, 20, 22, 24, 26, and 28 to route the MPU address lines to the proper pins on the ROM/EPROM sockets XU18, XU28, XU37, and XU48. (Select same size devices per the *ROM/EPROM Size Select* paragraph in this chapter.) Standard factory configuration for J1 is as follows: J1-14 to J1-16, J1-18 to J1-20, J1-24 to J1-26; for use with 64K x 8 ROMs/EPROMs. The jumpers for each possible size are:

64K x 8	J1-14 to J1-16, J1-18 to J1-20, J1-26 to J1-28
32K x 8	J1-14 to J1-16, J1-18 to J1-20, J1-24 to J1-26
16K x 8	J1-14 to J1-16, J1-20 to J1-22, J1-24 to J1-26
8K x 8	J1-20 to J1-22, J1-24 to J1-26

NOTE

The MVME117bug debug monitor, version 1.1 or later, is available in two fast 64K x 8 EPROMs. (Version 1.0 was in two fast 32K x 8 EPROMs.) These are to be installed in sockets XU18 and XU28, with power removed from the module. All the as-shipped jumper configurations are designed to work with MVME117bug, version 1.1 or later. Refer to the *MVME117 Firmware Debug Monitor User's Manual* for details.

ROM/EPROM Access Time (Speed) Select (Part of J1)

Select ROM or EPROM speed using pins J1-25 and J1-27. The as-shipped configuration has a jumper between these pins, for fast chips with access times less than 250 nsec (run with one wait cycle). For slower chips, with access times greater than 250 nsec but less than 450 nsec (run with three wait cycles), remove the jumper between J1-25 and J1-27.

NOTE

All four ROMs or EPROMs installed in the sockets XU18, XU28, XU37, and XU48, must be devices of the same size and type, meet the 28-pin JEDEC-standard pinout, and have the same access time (speed). The two 64K x 8 EPROMs for the MVME117bug debug monitor, version 1.1 or later, are fast.

ROM/EPROM Size Select (Part of J1)

Four combinations of jumpers establish the memory map according to the size of the ROMs or EPROMs used in sockets XU18, XU28, XU37, and XU48. (ROM/EPROM size may be 8K x 8, 16K x 8, 32K x 8, or 64K x 8.) This allows the second pair of ROMs/ EPROMs to immediately follow the first pair on the memory map. For socket pair 1, U18 = even bytes and U28 = odd bytes. For socket pair 2, U37 = even bytes and U48 = odd bytes. Refer to the *ROM/EPROM Socket Interface* paragraph in Chapter 4. The module is factory-configured with jumpers between pins J1-29, 30, 31, and 32 for 64K x 8 devices. The possible size configurations are:

64K x 8	no jumpers on J1 pins 29, 30, 31, and 32
32K x 8	J1-29 to J1-30
16K x 8	J1-31 to J1-32
8K x 8	J1-29 to J1-30, and J1-31 to J1-32

NOTE

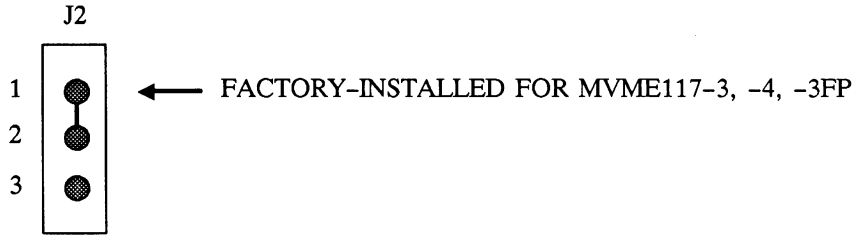
Set the jumpers per the above paragraph for the same size devices selected per the *ROM/EPROM Pinout Address Select* paragraph in this chapter for the devices to work properly.

System Controller Enable (Part of J1)

The jumper installed at the factory between pins J1-35 and J1-36 enables the system controller functions (system clock, VMEbus time-out generator, single level VMEbus arbiter, and system reset generator) on the MVME117. If this jumper is removed, the MVME117 cannot perform as system controller, but some other module in the system can.

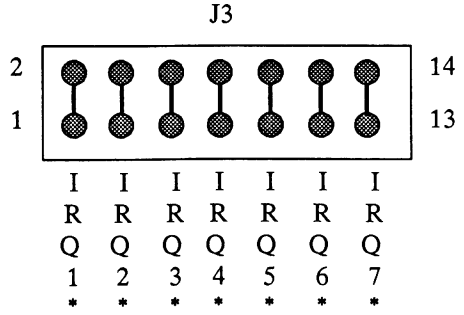
Factory Header (J2)

Header J2 is for factory use only. A wire trace is built at the factory between pins J2-1 and J2-2 for the MVME117-3, -4, and -3FP with 512Kb of RAM using 256K-bit chips. Do not move or remove this jumper.



VMEbus Interrupt Requests (IRQ) Enable (J3)

Header J3 is used for VMEbus interrupt enable. There are seven possible jumper locations; each one enables servicing one of the seven offboard interrupt levels. The factory as-shipped header configuration enables all these levels and is as follows:



NOTE

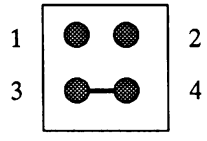
Interrupt handlers are identified in a system by the number and range of interrupt request lines they service. Option notation is IH(a-b), where "a" is the lowest line serviced and "b" is the highest. The interrupt handler on MVME117 is IH(0-7). It is a VMEbus requirement that an interrupt handler may only service a contiguous sequence of interrupt levels.

Floating Point Processor Clock Select (J4)

Header J4 is used to select the following clock speeds:

The clock speed is factory set for 10 MHz (J4-3 to J4-4). The clock speed selected must be slower than or equal to the MC68881 processor chip rated speed. For an MC68881 with its part number ending in "RC12" (it runs at 12.5 MHz), use the 10 MHz clock; for an MC68881 with its part number ending in "RC16" (it runs at 16.7 MHz), use the 16 MHz clock. The MVME117-3FP contains a 12.5 MHz MC68881 chip. The MVME117-3 and MVME117-4 do not contain an MC68881 chip.

CLOCK SPEED	J4 JUMPER
10 MHz	3-4
16 MHz	3-2 (WIRE WRAP)
20 MHz	3-1

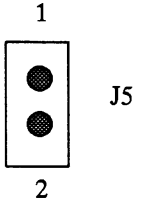


Battery Backup Connection (J5)

A jumper on J5 pins 1-2 connects the backup battery to the module. The MVME117 is shipped with no jumper here, thus disabling any battery backup power and maximizing battery life. If the jumper is installed, +3.5 Vdc from the battery preserves whatever data are in the MM58274 Real-Time Clock and the CMOS RAM (U81) in socket XU81. Note that this is byte wide and not executable memory. (Refer to the *CMOS RAM Pinout Select* paragraph in this Chapter.)

NOTE

The jumper for J5 is shipped in kit 67-W2287B01, and may be installed by the user. It is recommended that this be installed if using the MVME117bug debug monitor.



Serial Port Jumpers (Part of J7)

Header pins J7-3 through J7-10 are used to configure the multiprotocol serial port (port 2 = channel B) at P2 as "to modem" (DTE) or "to terminal" (DCE) operating synchronously. The factory configuration is with no jumpers on these pins, that is, for asynchronous operation. The possible configurations are:

asynchronous operation	no jumpers on J7-3 through J7-10
synchronous "to modem"(DTE)	J7-5 to J7-6, J7-7 to J7-9 (both clocks received from modem)
synchronous "to terminal"(DCE)	J7-3 to J7-4, J7-5 to J7-7, J7-8 to J7-10 (both clocks driven from Z8530 TXC output: Z8530 must be programmed to output TXC clock)

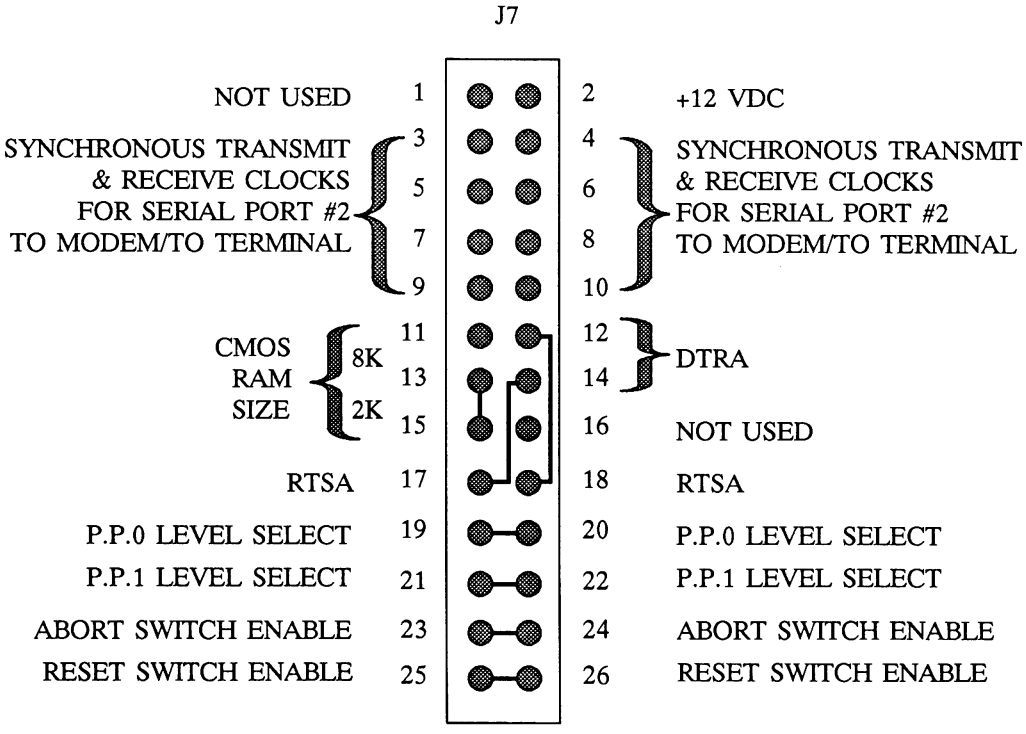
For the onboard asynchronous serial port (port 1 = channel A) at J6, the factory configuration is with a wire wrap jumper between J7-12 and J7-18, and a wire wrap jumper between J7-14 and J7-17. These jumpers connect DTRA and RTSA from a terminal to the modem control logic through J6. If J6 is connected to a terminal which doesn't drive DTR and/or RTS signals, these signals can be disconnected from J6 and wire wrapped to J7-2 (+12 Vdc) to permanently hold the signals true. Remove the applicable wire wrap jumper(s), and connect the "chip-side" pin(s) (J7-14 and/or J7-18) to J7-2. This holds these lines true to serial I/O controller chip Z8530 at U86.

NOTE

When operating in a noisy environment, at a baud rate (less than 19,200 baud), glitches may appear on the serial port lines. This can be corrected by installing a seven-segment, eight-pin SIP, 470 pF per segment capacitor on the MVME117 at location XC42. For the proper location see Figure 2-1. Use Sprague part number 470C7C0G471K5DG, or equivalent. Solder this capacitor network into the holes on the board. The "serial port" sheet of the schematic in Chapter 5 shows the circuits involved.

NOTE

If the MVME708A/MVME708-1 transition module is used, the jumpers on it must be set to the corresponding configuration (DEC or DTE) set on J7 on the MVME117. If the MVME117 is operated asynchronously, the MVME708A/MVME708-1 must **still** be set for DCE or DTE. Refer to the *MVME708A Transition Module and MVME117MVME117A P2 Adapter Board User's Manual*. If the transition module is not used, the P2 connector wiring must be equivalent to the MVME708A/MVME708-1 configuration.



CMOS RAM Pinout Select (Part of J7)

Header J7 pins 11, 13, and 15 configure socket XU81 for the required size of CMOS RAM U81 that is installed. (This RAM can be protected by the battery backup power. Refer to the *Battery Backup Connection* paragraph in this chapter.) The as-shipped configuration is with a jumper installed between J7-13 and J7-15, which connects a write signal to XU81 pin 23, so it is used with the factory-installed 2K x 8 RAM. If that jumper is removed and one is connected between J7-11 and J7-13, this connects an address line to XU81 pin 23, so it can be used with a user-substituted 8K x 8 RAM. No other size RAMs can be used in XU81. The RAM will receive only odd bytes through data lines D0 through D7. This is non-executable memory.

The factory-installed 2K x 8 chip is the Toshiba TC5517APL-2, which is in a 24-pin package, and is installed at the bottom of socket XU81, that is, in pin sockets 3 through

26. A recommended 8K x 8 chip that the user may substitute is the Toshiba TC5564P-2, which is in a compatible 28-pin package.

NOTE

The battery life is a function of the RAM standby current. Toshiba TC5517APL-2 parts were selected because of their low current and low data retention minimum voltage. The battery BT1 should last for 3 years when used with these parts.

Parallel Port Jumpers (Part of J7)

Header J7 pins 19 through 22 configure the input handshake lines on the parallel ports. The factory as-shipped configuration is with jumpers between J7-19 and J7-20 and between J7-21 and J7-22. This programs the input handshake lines on port 0 and port 1, respectively, to interrupt on low level pulses on their acknowledge lines. Removing either jumper changes that port so that the handshake line interrupts on a high level pulse on the acknowledge line.

ABORT Switch Enable (Part of J7)

Header pins J7-23 and J7-24 are jumpered in the factory to enable the ABORT switch S1. If this jumper is removed, the switch is disabled. (All interrupts, including the level 7 one from the ABORT switch, can be disabled through bit D7 of the Module Control Register (MCR) at address F44007. Refer to Chapter 3.)

RESET Switch Enable (Part of J7)

Header pins J7-25 and J7-26 are jumpered in the factory to enable the RESET switch S2. If this jumper is removed, this front panel RESET switch is disabled (but the remote reset and the watchdog reset still function).

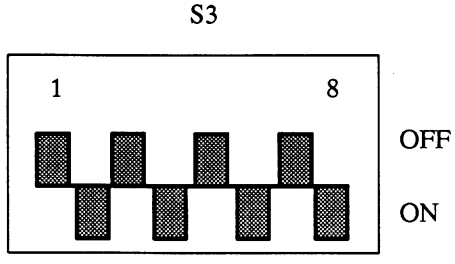
Readable Switch (S3)

Switch S3 has eight segments, which are set to up (open = high) or down (closed = low) on data lines D0 through D7 on the module. The leftmost segment (labeled 1) affects line D0; the rightmost (labeled 8) affects D7. Segment positions form a software readable switch register (SRSW) with an address of F4400B. Refer to the memory map in Chapter 3. The factory configuration is with segments alternating up (open) and down (closed).

2

NOTE

When the MVME117bug debug monitor is used with the module, data in the 2K x 8 CMOS RAM (U81) enables the debug monitor self-test. If U81 is not installed, self-test does not run. (On earlier versions of the MVME117, this function was performed by switch S3 segment 8 down (on).)



INSTALLATION INSTRUCTIONS

When the MVME117 has been configured as desired by the user, it can be installed in the system as follows:

a. Turn all equipment power OFF and disconnect power cable from ac power source.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS EQUIPMENT. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

b. Remove chassis cover as instructed in the equipment user's manual.

c. Remove the filler panel from the appropriate card slot at the front of the chassis. If the MVME143 is configured as the system controller, it must be installed in the left most card slot (slot 1) to correctly initiate the bus grant daisy-chain and the IACK daisy-chain.

d. Insert the MVME117 into the selected card slot. Be sure module is seated properly into the connectors on the backplane. Fasten the module in the chassis with the screws provided.

e. If the P2 adapter module is to be used, connect the P2 adapter module in accordance with the instructions in the *MVME708A Transition Module and MVME117/MVME117A P2 Adapter Board User's Manual.*

f. If a MVME708A/MVME708-1 transition module is used with the MVME117, install the MVME708A/MVME708-1 in accordance with the instructions in the *MVME708A Transition Module and MVME117/MVME117A P2 Adapter Board User's Manual.* See Figure 2-2.

g. Replace cover and turn equipment power ON.

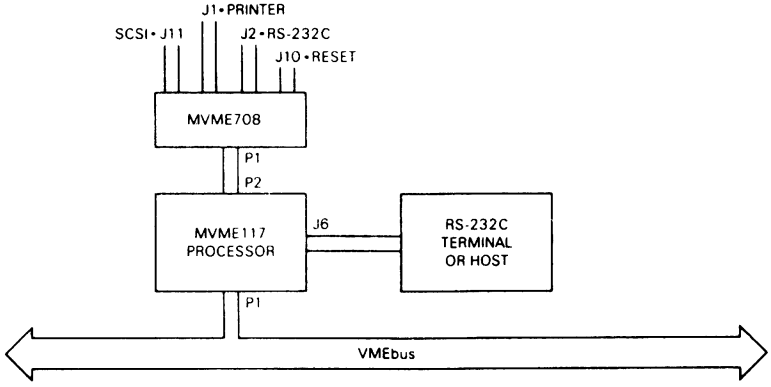


FIGURE 2-2. Typical MVME117 Stand-alone Installation

Terminal Connection

The RS-232C serial port on the front panel is configured for DCE (to terminal) operation only. A 25-pin RS-232C cable may be connected to the front panel connector J6 with the other end connected to a compatible terminal. This cable is not provided with the MVME117 module, and must be made or provided by the user. Refer to Chapter 5 for detailed information on signals supported.

NOTE

The user may change J6 to a "to modem" configuration by providing a "null-modem" cable that switches certain signals.

System Considerations

The MVME117 may be used as a stand-alone controller, as shown in Figure 2-2., or with other SCSI controllers, as shown in Figure 2-3. When it operates stand-alone, onboard pullup resistors hold certain VMEbus lines in a known state. If the MPU tries to make an offboard access, the onboard system controller grants the bus, but because there are no devices on the bus, a bus time-out occurs.

To use the MVME117 as an Intelligent SCSI bus Peripheral Controller (IPC), additional resources are required. A VMEbus IPC needs a bus interrupter, which may be supplied by the global interrupter on the MVME050. Use of the MVME117 in this mode is further limited by its lack of shared memory, requiring global memory such as provided by the MVME202.

Note that the SCSI bus specification allows for a maximum of eight devices (controllers and hosts) communicating to each other on the bus, so that an MVME117 is capable of connecting to a maximum of seven controllers (including other MVME117's). See Figure 2-3. Each device can have up to eight logical units (drives or channels) associated with it. Many SCSI controllers support disconnection and reselection, which allows parallel execution of commands. The SCSI bus currently supports interfacing to disk controllers, tape controllers, printers, LAN interfaces, and other processors.

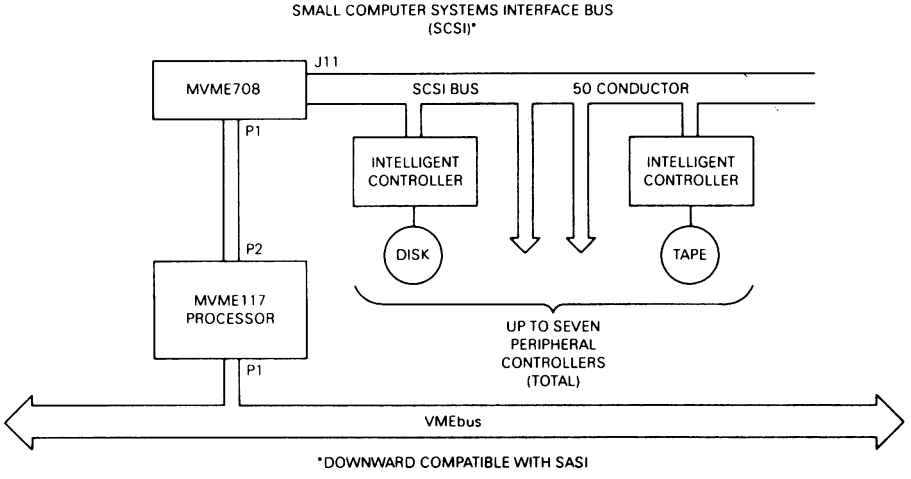


FIGURE 2-3. MVME117 Used with Other SCSI Controllers

CHAPTER 3 – OPERATING INSTRUCTIONS

INTRODUCTION

This chapter provides the necessary information to use the MVME117 module in a system configuration.

CONTROLS AND INDICATORS

The MVME117 module has RESET, ABORT, and readable switches, and HALT, RUN, and FAIL indicators, all of which are located on the front panel of the module.

RESET Switch (S2)

A front panel RESET switch (S2) (if enabled) generates a local reset and (if system controller) also generates a VMEbus system reset. A jumper on J7 is provided to allow the RESET switch to generate a local reset. The system controller jumper (on J1) allows the system reset to be asserted by the local reset. Removing the jumper from J7 disables the RESET switch.

The MPU is not immediately reset when the RESET switch is pressed, but instead, waits for current access of the MPU to be completed before entering the reset state. This prevents short cycling onboard and VMEbus accesses.

ABORT Switch (S1)

A software ABORT switch (S1) is located on the front panel. Programs may be aborted (if enabled by a jumper on J7 and by the interrupt enable bit in the Module Control Register (MCR), bit D7 at address F44007) with this switch. Pressing this switch causes a level 7 interrupt to the MPU through vector $1F with an offset of $7C from the Vector Base Register (VBR).

Readable Switch (S3)

The front panel 8-position software-readable switch (S3) is a piano-type switch accessible through the front panel. An open switch is read as high, a closed switch is read as low on data lines D7 through D0. Switch position 8 corresponds to data line D7, etc.

HALT Indicator (DS2)

The red LED HALT indicator (DS2), located on the front panel, is lit whenever the MPU enters a halted state (usually the result of a double bus fault). The indicator is also lit whenever the MPU is being reset.

RUN Indicator (DS3)

The green LED RUN indicator (DS3), located on the front panel, is connected to the MPU's address strobe signal and indicates that the MPU is executing a bus cycle.

FAIL Indicator (DS1)

The red LED FAIL indicator DS1, located on the front panel, indicates the status of the fail bit in the control register. Also, if the module is configured as the system controller (by a jumper on J1), the FAIL LED indicates the status of the SYSFAIL* signal on the VMEbus.

MVME117 MEMORY MAP

Memory mapping of various devices of the MVME117 is provided in Table 3-1.

TABLE 3-1. MVME117 Memory Map

DEVICE(S)	ADDRESS	COMMENTS	ATTRIBUTES
Local RAM	000000 - 07FFFF	512Kb	(R/W)
VMEbus	080000 - EFFFFF		AM=$3E, $3D, $3A, or $39
ROM/EPROM sockets	F00000 - F3FFFF	Four sockets with maximum size of 64K x 8 each; details in Table 4-2.	(R)
Battery-backed RAM	F40001 - F43FFF	8K x 8 max. (odd bytes only). non-executable. factory-installed 2K x 8 part repeats four times.	(R/W)

TABLE 3-1. MVME117 Memory Map (cont'd)

DEVICE(S)	ADDRESS	COMMENTS	ATTRIBUTES
Registers	F44001 - F47FFF	(odd bytes only)	
Parallel ports register detail:		'ALS652	
PIO #0	F44001	Byte #1	(R/W)
PIO #1	F44003	Byte #2	(R/W)
Parallel Port Control		'LS794	
Register detail:			
PPCR	F44005	at reset=$FF	(R/W)

Bit assignments for the PCCR are listed below.

DATA BIT	FUNCTION	COMMENTS
D7	Port #1 Direction	(0=output, 1=input)
D6	Port #1 Strobe	(0=low, 1=high output level)
D5	Port #1 Input Latch Enable	(0=enabled)
D4	Port #1 Interrupt Enable	(0=enabled)
D3	Port #0 Direction	(0=output, 1=input)
D2	Port #0 Strobe	(0=low, 1=high output level)
D1	Port #0 Input Latch Enable	(0=enabled)
D0	Port #0 Interrupt Enable	(0=enabled)

Module Control		'LS794	
Register detail:			
MCR	F44007	(odd byte only) after reset=$FF	(R/W)

Bit assignments for MCR are listed below.

DATA BIT	FUNCTION	COMMENTS
D7	Interrupt Enable	(0=enabled)
D6	SCSI Chip Reset	(1=reset)

TABLE 3-1. MVME117 Memory Map (cont'd)

DEVICE(S)	ADDRESS	COMMENTS	ATTRIBUTES
D5	Board Fail	(1=fail)	
D4	Write Incorrect Parity	(0=enabled)	
D3	Parity Enable	(0=enabled)	
D2	Enable Fail Interrupt	(0=disabled, 1=enabled)	
D1	SCSI Interrupt Enable	(0=enabled)	
D0	Requester Mode	(1=ROR, 0=RWD)	
Module Status Register		'LS244	(R)
MSR	F44009	(odd byte only)	

The assignments for MSR are listed below.

DATA BIT	FUNCTION	COMMENTS
D7	Parallel Port #1 Acknowledge Flag	(0=interrupt pending)
D6	Parallel Port #0 Acknowledge Flag	(0=interrupt pending)
D5	Parity Error	(0=error)
D4	Power On Reset	(0=cold start)
D3	System Controller	(1=system controller)
D2	VMESFAIL	status of SYSFAIL signal
D1	Onboard Time-out Flag	(0=time-out)
D0	SCSI Interrupt Flag	(1=interrupted)

CP0FLAG	F44009	(odd byte only) Clears parallel port #0 acknowledge flag	(W)
Software-Readable	Switch S3	'LS244	(R)
Register detail:			
SRSW	F4400B	(odd byte only)	

TABLE 3-1. MVME117 Memory Map (cont'd)

DEVICE(S)	ADDRESS	COMMENTS	ATTRIBUTES

The SRSW bit assignments are listed below.

DATA BIT	FUNCTION	COMMENTS
D7	Switch S3 Segment 8	(1=up=open, 0=down=closed)
D6	Switch S3 Segment 7	(1=up=open, 0=down=closed)
D5	Switch S3 Segment 6	(1=up=open, 0=down=closed)
D4	Switch S3 Segment 5	(1=up=open, 0=down=closed)
D3	Switch S3 Segment 4	(1=up=open, 0=down=closed)
D2	Switch S3 Segment 3	(1=up=open, 0=down=closed)
D1	Switch S3 Segment 2	(1=up=open, 0=down=closed)
D0	Switch S3 Segment 1	(1=up=open, 0=down=closed)

CP1FLAG	F4400B	(odd byte only) Clears parallel port #1 acknowledge flag	(W)
CONFIG. NUMBER		82S123	(R)

Register detail:

CONFIG	F4400D	(odd byte only)	(R)

PRODUCT NUMBER	RAM CHIP SIZE (BITS)	ONBOARD MEMORY (BYTES)	SCSI (Y/N)	MC68881	CONFIG. NUMBER
MVME117-03	256K x 1	512K	Y	N	02
MVME117-04	256K x 1	512K	N	N	03
MVME117-3FP	256K x 1	512K	Y	Y	06

ERROR CLEAR		(dummy location)	(R)

Register detail:

ERRCLR	F4400F	(odd byte only) clears parity error, local bus error, and power on reset flag.	(R)

TABLE 3-1. MVME117 Memory Map (cont'd)

DEVICE(S)	ADDRESS	COMMENTS	ATTRIBUTES
Serial Ports	F48001 - F4BFFF	Z8530A (odd bytes only)	(W)
Register details:			
SIOB WR0	F48001	ch. B Write Reg. 0	(W)
SIOB RR0	F48001	ch. B Read Reg. 0	(R)
SIOB DR0	F48003	ch. B Data Reg.	(R/W)
SIOA WR0	F48005	ch. A Write Reg. 0	(W)
SIOA RR0	F48005	ch. A Read Reg. 0	(R)
SIOA DR0	F48007	ch. A Data Reg.	(R/W)
Real-Time clock	F4C001 - F4FFFF	(odd byte, D3-D0 only)	
Register detail:			
RTC 00	F4C001	Control Register	(Split R/W)
RTC 01	F4C003	Tenths of Seconds	(R)
RTC 02	F4C005	Units Seconds	(R/W)
RTC 03	F4C007	Tens Seconds	(R/W)
RTC 04	F4C009	Units Minutes	(R/W)
RTC 05	F4C00B	Tens Minutes	(R/W)
RTC 06	F4C00D	Units Hours	(R/W)
RTC 07	F4C00F	Tens Hours	(R/W)
RTC 08	F4C011	Units Days	(R/W)
RTC 09	F4C013	Tens Days	(R/W)
RTC 10	F4C015	Units Months	(R/W)
RTC 11	F4C017	Tens Months	(R/W)
RTC 12	F4C019	Units Years	(R/W)
RTC 13	F4C01B	Tens Years	(R/W)
RTC 14	F4C01D	Day of Week	(R/W)
RTC 15	F4C01F	Clock setting or interrupt registers	(R/W)
Programmable Timer	F50001 - F53FFF	MC68B40 (odd bytes only)	

TABLE 3-1. MVME117 Memory Map (cont'd)

DEVICE(S)	ADDRESS	COMMENTS	ATTRIBUTES
Register detail:			
PTM 00	F50001	Control Register 1/3	(W)
PTM 00	F50001	No operation	(R)
PTM 01	F50003	Control Register 2	(W)
PTM 01	F50003	Status Register	(R)
PTM 02	F50005	MSB Buffer Register	(W)
PTM 02	F50005	Timer #1 Counter	(R)
PTM 03	F50007	Timer #1 Latches	(W)
PTM 03	F50007	LSB Buffer Register	(R)
PTM 04	F50009	MSB Buffer Register	(W)
PTM 04	F50009	Timer # 2 Counter	(R)
PTM 05	F5000B	Timer #2 Latches	(W)
PTM 05	F5000B	LSB Buffer Register	(R)
PTM 06	F5000D	MSB Buffer Register	(W)
PTM 06	F5000D	Timer #3 Counter	(R)
PTM 07	F5000F	Timer #3 Latches	(W)
PTM 07	F5000F	LSB Buffer Register	(R)
RESERVED	F54001 - F57FFF		
SCSI Controller	F58001 - F5BFFF	NCR 5380 (odd bytes only)	
Register detail:			
SCSI 00	F58001	Current SCSI Data	(R)
SCSI 00	F58001	Output Data Reg.	(W)
SCSI 01	F58003	Initiator Command Reg.	(R/W)
SCSI 02	F58005	Mode Register	(R/W)
SCSI 03	F58007	Target Command Reg.	(R/W)
SCSI 04	F58009	SCSI Bus Status	(R)
SCSI 04	F58009	Select Enable Reg.	(W)
SCSI 05	F5800B	Bus & Status Reg.	(R)
SCSI 05	F5800B	Start DMA Send	(W)
SCSI 06	F5800D	Input Data Register	(R)
SCSI 06	F5800D	Start Target Rec. DMA	(W)

TABLE 3-1. MVME117 Memory Map (cont'd)

DEVICE(S)	ADDRESS	COMMENTS	ATTRIBUTES
SCSI 07	F5800F	Reset Parity/Interrupts	(R)
SCSI 07	F5800F	Start Init. Rec. DMA	(W)
FSCSI	F5C001 - F5FFFF	NCR 5380 (odd bytes only) pseudo-DMA only	
Register detail:			
FSCSI 00	F5C001	Output Data Reg.	(W)
FSCSI 06	F5C00D	Input Data Register (Only output and input registers should be used in pseudo-DMA addresses.)	(R)
Floating Point Peripheral	F60000 - F6FFFF	MC68881	(R/W)
Register detail:			
CPRESP	F60000	Response Register	(R:16)
CPCONT	F60002	Control Register	(W:16)
CPSAVE	F60004	Save Register	(R:16)
CPREST	F60006	Restore Register	(R/W:16)
Reserved	F60008	Reserved	---
CPCOMM	F6000A	Command word	(W:16)
Reserved	F6000C	Reserved	---
CPCOND	F6000E	Condition word	(W:16)
CPOPER	F60010	32 bit operand	(R/W:32)
CPREGS	F60014	Register Selector	(R:16)
Reserved	F60016	Reserved	---
CPINADD	F60018	Instruction Address	(R/W:32)
Reserved	F6001C	Reserved (32 bits)	---

TABLE 3-1. MVME117 Memory Map (cont'd)

DEVICE(S)	ADDRESS	COMMENTS	ATTRIBUTES
VMEbus	F70000 - FEFFFF	VMEbus	(R/W) AM=$3E, $3D, $3A, or $39
VMEbus	FF0000 - FFFFFF	Short I/O Space	Address Modifier =$29, $2D

CHAPTER 4 - FUNCTIONAL DESCRIPTION

INTRODUCTION

This chapter provides the overall block diagram level description for the MVME117. The general description provides an overview of the modules, followed by a detailed description of each section of the modules. The simplified block diagram of the MVME117 is shown in Figure 4-3.

GENERAL DESCRIPTION

The MVME117 is a complete microcomputer system. The module contains MPU, memory, and input/output, as well as numerous control functions.

For most applications, the MPU fetches and executes instructions from the onboard RAM or ROM/EPROM. If the address is not within the onboard range, the onboard requester requests the VMEbus if it does not already have it. Upon receiving a grant, the cycle is completed via the VMEbus. The address modifiers are driven according to the following codes.

CODE NO.	DESCRIPTION
3E	Standard supervisory program access
3D	Standard supervisory data access
3A	Standard non-privileged program access
39	Standard non-privileged data access
2D	Short supervisory I/O access
29	Short non-privileged I/O access

Two serial ports with programmable baud rates are provided for communication: one multiprotocol serial port (port 2 = channel B) on P2 with either DCE "to terminal" or DTE "to modem" interface, and one asynchronous only serial port (port 1 = channel A) on J6 configured DCE "to terminal" for a debug port or for general serial I/O.

A parallel I/O/Centronics printer port on connector P2 can be connected directly to a Centronics-type printer through the MVME708A/MVME708-1 transition module or it can be used for general purpose parallel I/O.

The mass storage interface consists of a SCSI bus controller to interface to external SCSI controller modules for peripherals such as hard and floppy disks and tape drives.

Three timers are provided, each capable of generating an interrupt. The third timer is used by the VERSAdos operating system as a tick timer for task switching. The first timer is cascaded with the tick timer to provide a watchdog time-out which resets the module. The second timer is unused by VERSAdos and is available to the user.

VMEbus system controller functions are provided including the 16 MHz system clock, single level VMEbus arbiter, VMEbus time-out generator, and a system reset generator. These functions can be disabled if a system controller already exists in the system. The MVME117 can also be run stand-alone, without a VMEbus.

The software readable front panel switch function is determined by the user.

The ABORT switch on the front panel generates a level 7 interrupt to the MPU.

A battery-backed time-of-day clock provides time (tenths of seconds, seconds, minutes, hours), day, month, and year information and can be programmed for periodic interrupts.

The module and generally the entire VME system may be reset from the front panel RESET switch or through the remote reset line on the P2 connector. The 9-pin remote reset connector on the MVME708-1 transition module is used for resetting the MVME117 module from a remote location.

NOTE

If the MVME117 is the system controller, the entire system is reset; if not, only onboard functions will be affected by a local reset.

The module configuration code is used by the debug monitor and operating system to indicate available resources.

A 2K x 8 (or user-substituted 8K x 8) CMOS RAM is provided with a battery backup for data retention during power-down.

DETAILED DESCRIPTION

The MVME117 consists of the following circuitry.

Microprocessor Unit (MPU)

The MC68010 MPU is used in the MVME117 circuitry. The MPU is contained in a dual-inline package and its associated circuitry operates at 10 MHz. Timing for the MPU and other logic is derived from a 40 MHz oscillator. For further information concerning the MC68010 MPU, refer to Motorola data book for the MC68010.

RAM

The MVME117 module has 18 RAM chips that are factory-configured with 256K x 1 chips. Onboard RAM is 512Kb (on MVME117-3,-4,-3FP).

The RAM array consists of one bank for odd bytes and another bank for even bytes. Dynamic RAMs (150ns access time) are used with 256-row four milliseconds refresh. Parity on a byte boundary is updated on every write cycle to the onboard RAM. On a read cycle, parity is checked (if enabled) for odd parity. When parity is enabled, the onboard RAM access time is automatically increased to accommodate the additional time required for the parity check. This results in one wait cycle operation from onboard RAM when parity is enabled and zero wait cycle operation when parity is disabled. Parity check is performed on both the lower byte and the upper byte of a word in onboard dynamic RAM whether either byte or both bytes are read. Refer to bit D3 in the module control register at address $F44007 in the memory map in Chapter 3.

Refresh

The RAM is refreshed once every 30 us with two RAS-only refresh cycles. During refresh all onboard processing stops.

Local Accesses

The local dynamic RAM starting address is 0. The upper address lines are decoded to decide if the cycle is for the onboard RAM. If the RAM is selected, the RAM sequencer is started.

Bus Requester

The bus requester requests the VMEbus mastership on any one of four bus request levels (user configurable by jumpers on header J1) and supports the daisy-chain on bus grant. The bus requester operates in the Release-On-Request (ROR) mode or in the Release-When-Done (RWD) mode and requests bus mastership only if the MPU attempts a VMEbus access and does not already have the bus mastership. The bus mastership is

released when a bus request is received on any level or if an onboard refresh sequence is started (ROR), or is released when the MVME117 is done with the current cycle (RWD). The mode of the bus requester is selectable through bit D0 of the module control register at address $F44007. Refer to the memory map in Chapter 3. The default power-up mode is ROR.

Interrupt Handler

The interrupt handler receives interrupt requests from the serial ports, timer, SCSI interface, parallel/printer port, ABORT switch, real-time clock, SYSFAIL, AC fail, and the seven VMEbus interrupt requests. If the user wants to ignore any VMEbus interrupt level, the seven VMEbus interrupt requests can be individually disabled by removing a jumper on header J3. (Refer to Chapter 2.)

Also, some of the eight onboard interrupt sources can be individually enabled in the peripheral chip or by the module control register. All interrupts are disabled at reset until software sets the interrupt enable bit in the control register. On an interrupt acknowledge cycle, the interrupt handler will supply a vector number from a PROM for an onboard interrupt source (except the serial port interface chip which supplies its own vector number), or receive the vector number from the VMEbus for a VMEbus acknowledge cycle.

The various interrupt sources and interrupt levels are listed in Table 4-1.

TABLE 4-1. Interrupt Sources

INTERRUPT SOURCE	INTERRUPT LEVEL	VECTOR SOURCE	VECTOR NUMBER	OFFSET FROM VBR
ABORT switch	7	PROM	$1F (NOTE)	$7C
AC-Fail	7	PROM	$40 (NOTE)	$100
Serial Ports	6	SIO Chip	programmable	
Timer	5	PROM	$41 (NOTE)	$104
Parallel Port	4	PROM	$42 (NOTE)	$108
Time-of-day clock	3	PROM	$43 (NOTE)	$10C
SCSI Interface	2	PROM	$44 (NOTE)	$110
SYSFAIL	1	PROM	$45 (NOTE)	$114
Reserved for SCSI firmware	--	--	$46	$118

TABLE 4-1. Interrupt Sources (cont'd)

INTERRUPT SOURCE	INTERRUPT LEVEL	VECTOR SOURCE	VECTOR NUMBER	OFFSET FROM VBR
VMEbus IRQ 7	7	VMEbus	supplied	
VMEbus IRQ 7	7	VMEbus	supplied	
VMEbus IRQ 6	6	VMEbus	supplied	
VMEbus IRQ 5	5	VMEbus	supplied	
VMEbus IRQ 4	4	VMEbus	supplied	
VMEbus IRQ 3	3	VMEbus	supplied	
VMEbus IRQ 2	2	VMEbus	supplied	
VMEbus IRQ 1	1	VMEbus	supplied	

NOTE: Vector number may be modified by a user-supplied programmed PROM, U93. Refer to Appendix B for contents of the factory-supplied U93 PROM.

Serial Ports

Two serial ports are provided by the Z8530A SIO. One provides a multiprotocol port (port 2 = channel B) to the user, accessible through the P2 connector. The other (port 1 = channel A) is asynchronous and DCE "to terminal" only; and is accessible on the front panel at J6. Both ports are RS-232C levels. For asynchronous protocols, the baud rates are software programmable from 50 to 19.2K baud. For synchronous protocols, the baud rates are software programmable up to 1M Bits/Second (although the Z8530A software controller will be the limiting factor). Flow control of data into this board is handled by RTS in the "to modem" configuration, and by CTS in the "to terminal" configuration. Flow control of data coming from the board can be CTS "to modem", or DTR "to terminal", or preferably by X-on/X-off. For the "to terminal" (DCE) configuration, DSR and CTS are driven (pulled up to the true level). For the "to modem" (DTE) configuration, the DTR signal is driven (pulled up to the true level).

If this module interfaces to a three wire terminal (TXD, RXD, GND), the inputs CTS and DCD for "to modem" interface, or DTR and RTS for "to terminal" interface can be disconnected from the connector and held true by wire wrapping or jumpering the inputs to pull-up resistors. (Refer to Chapter 2.)

For synchronous protocols (port 2 = channel B only), both TXC and RXC signals are driven from the TXC output of the interface chip for "to terminal" (DCE) configuration. For "to modem" (DTE) configuration, TXC and RXC signals both are received by the interface chip. See Figure 4-2.

Refer to the *Serial Port Setup Example* paragraph in this chapter for an example of setting up the serial port.

Timers

Three independent 16-bit timers are provided by the MC68B40 programmable timer. Two of these are chained through hardware to provide the tick/watchdog functions. Timer #3 uses a 1 MHz or 125 kHz internal reference and was chosen as the "tick" timer for a task switching operating system such as VERSAdos; timer #1 (watchdog timer) shares a control register with timer #3. The second timer is left free for the user. Refer to the *MC68B40 Timer Setup Example* paragraph in this chapter for an example of setting up the MC68B40 timer.

SCSI Controller

The NCR 5380 SCSI controller implements the small computer systems interface as defined by the ANSI X3T9.2 committee (Rev. 14 of the SCSI specification). The single-ended, open collector version of the SCSI bus is implemented. The controller supports arbitration, including reselection, and operates in both the initiator and target mode (in the same system) in a multi-target system (or simpler one). The SCSI bus device ID is software controlled by the user.

All command/status interfacing and data transfer are performed through the NCR 5380. When data is to be transferred, or the SCSI bus is to be acquired, the information is sent to the interface chip which interrupts when processor intervention is required. When the module has been selected by another SCSI bus device, or data is received, an interrupt occurs allowing the MPU to transfer data to RAM or act on being selected. The data path is single-buffered on chip.

The SCSI interrupt to the processor can be disabled through bit D1 of the module control register at address $F44007. Refer to the memory map in Chapter 3.

High level SCSI routines are included in the EPROMs that contain the MVME117bug debug monitor. Refer to the *MVME117 Firmware Debug Monitor User's Manual* and the *Small Computer Systems Interface (SCSI) Firmware User's Manual.*

ROM/EPROM Sockets

Four 28-pin ROM/EPROM sockets are provided. The sockets accommodate 8K x 8, 16K x 8, 32K x 8, or 64K x 8 devices. No mixing of ROM/EPROM sizes is allowed. The ROMs/EPROMs are mapped in one contiguous block starting at F00000. However, when the module is reset, the ROMs/EPROMs are accessed on the first four MPU cycles (the MPU fetches its stack pointer and program counter) from the first four ROM/EPROM locations.

Time-of-Day Clock

The National MM58274 Real-Time Clock provides timekeeping from tenths of seconds to tens of years. It may be programmed to interrupt in the following intervals: 0.1 second, 0.5 second, 1 second, 5 seconds, 10 seconds, 30 seconds, and 60 seconds. Battery backup is provided to maintain timer operation while power is off.

The real-time clock chip has a 4-bit data bus and uses MPU data lines D03-D00.

To ensure the clock has not been automatically updated while reading the current time (causing an erroneous reading), the following algorithm is used to read the time:

Entry

1.0 Read time-of-day control register (clears data changed flag).
2.0 Read all of the time and date registers. Store results in RAM.
3.0 Read time-of-day control register.
4.0 If "data changed" flag set, go to 1.0.

Exit

The *Real-Time Clock* paragraph in this chapter details initializing, setting, and reading the real-time clock.

Non-Volatile RAM

The module provides a battery backed up CMOS RAM socket, XU81. The factory supplies U81 as a 2K x 8 CMOS RAM, but the user may substitute an 8K x 8 CMOS RAM. (Refer to Chapter 2.) The non-volatile RAM is interfaced only to data lines D0 through D7 (odd bytes). This is non-executable memory.

Battery Backup System

A Lithium battery keeps the Real-Time Clock (RTC) and Non-Volatile RAM (NVRAM) active while power is off. Circuitry is provided to isolate the RTC and NVRAM from false writes during power-down and power-up. Shelf life (battery not connected by jumper on J5) is estimated at five years, and typical operating life of the battery is estimated at three years. Refer to the parts list in Chapter 5 for a part number and electrical characteristics.

Parallel/Printer Port

Twenty parallel I/O lines with four of these as handshake lines are provided. These lines may be configured as a Centronics printer port. The two input handshake lines are level-sensitive and may be programmed to interrupt on low or high pulses on the corresponding acknowledge lines. These levels are individually programmed by external jumpers on header J7. The two output handshake lines are strobes and do not interrupt the MPU. The Centronics port signals are available on the P2 connector. The parallel ports are implemented with two 74ALS652s and a 74LS794 used as a control register.

The parallel I/O lines are configured in two 8-bit groups, each group having two associated handshake lines. Each group may be programmed (through a control register) as input, latched input, or latched output. The control register is byte-wide and each 4-bit nibble affects one 8-bit port. The four control bits are: DIR (direction, 0=output, 1=input), STB (strobe, 0=low, 1=high), LEN* (latch enable, 0=enabled, 1=disabled), and INTEN* (interrupt enable, 0=enabled, 1=disabled). The most and least significant nibbles control parallel I/O bytes #1 and #0, respectively. Power-up status is $FF (refer to Table 3-2). Two bits of the Module Status Register tell the MPU of pending interrupts -- one bit each for I/O bytes #1 and #0 (refer to the memory map in Chapter 3.

The *Parallel Port* paragraph gives parallel port operation, including printer port information.

MC68881 Socket and Chip

The MVME117 provides a socket XU62 for an optional user-supplied MC68881 Floating Point Coprocessor (FPC). The 68-pin grid array socket allows the user to provide mathematical enhancements to the 16-bit system. The MC68881 provides an IEEE-compatible floating point format and math functions such as add, subtract, multiply, divide, sine, cosine, tangent, square root, power, and others. The MC68881 chip is present as U62 on the MVME117-3FP version of the module. Macros for using the MC68881 are included with the MVME117-3FP module, as part number 8211XS881MAC. Refer to AR233, applications, listed in Chapter 1.

System Controller Functions

The system controller functions include a 16 MHz system clock, single level VMEbus arbiter, system reset (switch and power-up), and a VMEbus time-out generator. Note that all of these functions must be disabled by a jumper on header J1 if there is another VMEbus system controller active in the system.

Bus Arbiter

The single level arbiter receives level 3 (only) bus requests from the VMEbus and issues a level 3 (only) bus grant when the bus busy signal is negated. The bus arbiter is enabled when the MVME117 is the system controller.

Reset Generator, Power-Up Reset

The power-up reset generates a local and a system reset for approximately 300 milliseconds. The RESET switch has the same function as the power-up reset except it is initiated by the front panel button. A disable jumper is provided on J7 to disconnect the front panel RESET switch. Reset can also be generated by the remote reset line on the P2 connector. A bit in the module status register is set during a power-up reset. This software flag can be used to distinguish between a power-up reset and a user reset for cold restart or warm restart. The module status register at address $F44009 is reset when the ERRCLR location at $F4400F is accessed. (Refer to the memory map in Chapter 3.) System reset is enabled by the system controller jumper on J1.

System Clock

If the monoboard microcomputer is the system controller, the 16 MHz SYSCLK signal for the VMEbus is provided by the MVME117. The timing reference is an onboard crystal oscillator, Y2.

VMEbus Time-Out

If the MVME117 is the system controller, the bus time-out function asserts bus error if a VMEbus cycle exceeds approximately 120 microseconds.

HARDWARE INTERFACE

The hardware interface consists of the following circuitry.

Timer Interface

The MC68B40 Programmable Timer Module provides the "tick" timer for timing events, and for periodic interrupts for time-slicing. The module contains three 16-bit timers.

Timer #3 has the capability of using an internal time reference of 1 MHz or a pre-scaled internal reference of 125 kHz; this timer is used as the "tick" timer for Operating Systems. Timer #3 external clock is left as a no connection. The watchdog timer is implemented with Timer #1; its input clock is the output of Timer #3. The output of Timer #1 is buffered and logically ORed with the local RESET of the MVME117 to provide the watchdog function. The choice of chaining timers #3 and #1 was based on the fact that these two timers share a control register. Timer #2 is left open for the user. Its external clock is left unconnected; the 1 MHz internal clock is used for a timer reference.

The MC68B40 interfaces to the MC68010 as an MC6800 peripheral. It uses the VPA* signal to tell the MC68010 that it acknowledges an access. The other peripherals use the standard MC68000 interface, that is, they acknowledge an access by responding with DTACK*.

Serial Interface

The serial interface buffers the TTL signals from the Z8530A chip to RS-232C levels and provides the switching of the P2 second serial port (port 2 = channel B) "to terminal", "to modem" configurations for the serial port on the MVME708A/MVME708-1 transition module. The port at J6 on the front panel (port 1 = channel A) is hardwired in the "to terminal" configuration; the user may change it to a "to modem" configuration by providing an external cable that switches certain signals.

When configured as "to terminal", the DCD and DSR signals are held true with pullup resistors. Flow control is accomplished with CTS or with the RTS input. For synchronous protocols, the TXC signal comes from the Z8530A chip and is connected to the Z8530A RXC and driven out to both TXC and RXC RS-232C lines.

NOTE

Port 1 (= channel A) at J6 on the front panel is "to terminal", asynchronous protocols only. Its intended use is a debug port, although it may be used as a general purpose asynchronous port. (It may be configured for the "to modem" configuration by the use of a "null-modem" cable that switches some signals.)

When port 2 is configured as "to modem", DTR is held true. Flow control is accomplished with RTS, or with the CTS input. For synchronous protocols, the TXC and RXC signals are input from the RS-232C lines.

NOTE

The limiting factor for synchronous bit rate is the Z8530A software controller with a limit of 1M bits/second.

For details of serial port connections for port 1 see Figure 4-1. For details of serial port connections for port 2 see Figure 4-2.

Floating Point Coprocessor Interface

Floating point operations are accomplished using the Motorola MC68881 device. Although the MC68881 is designed with a 32-bit data bus and although it was designed to interface to an MC68020, it is easily interfaced to a 16-bit processor like the MC68010. By programming the SIZE and A0 pins of the MC68881 for a 16-bit bus, it is interfaced directly to the MC68010 with a simple address decode scheme and proper timing. All floating point operations are treated like memory reads and writes to the proper MC68881 registers. Refer to the documentation listed in Chapter 1.

ROM/EPROM Socket Interface

After a RESET, ROM/EPROM socket pair #1 is selected for the first four word accesses. A logic device senses the RESET condition and signals the map decoder that a RESET VECTOR fetch is under way. At this time, the MPU fetches the initial stack pointer value and the initial program counter value. These two long words are located in the first four word locations of the ROM/EPROM. The above condition necessitates a minimum of two ROM/EPROM devices on the module. A 1 x 8 header (J1, pins 14, 16, 18, 20, 22, 24, 26, 28) is provided to switch address signals to the ROMs/EPROMs depending on device size. Since there are two socket pairs, the map decoder needs information to select the second pair instead of the first pair. This device size information is provided by two jumpers (J1, pins 29 and 30, 31 and 32). The jumper information is summarized in Table 4-2. The 1 x 8 header must be set up to match the size programmed for the map decoder, otherwise, incorrect accesses occur. If devices smaller than 64K x 8 are used, the memory space allocated for ROM is not entirely populated. If accesses are attempted beyond the space populated by the ROMs/EPROMs, a bus error occurs. If a write attempt is made to the ROMs/EPROMs, a bus error occurs.

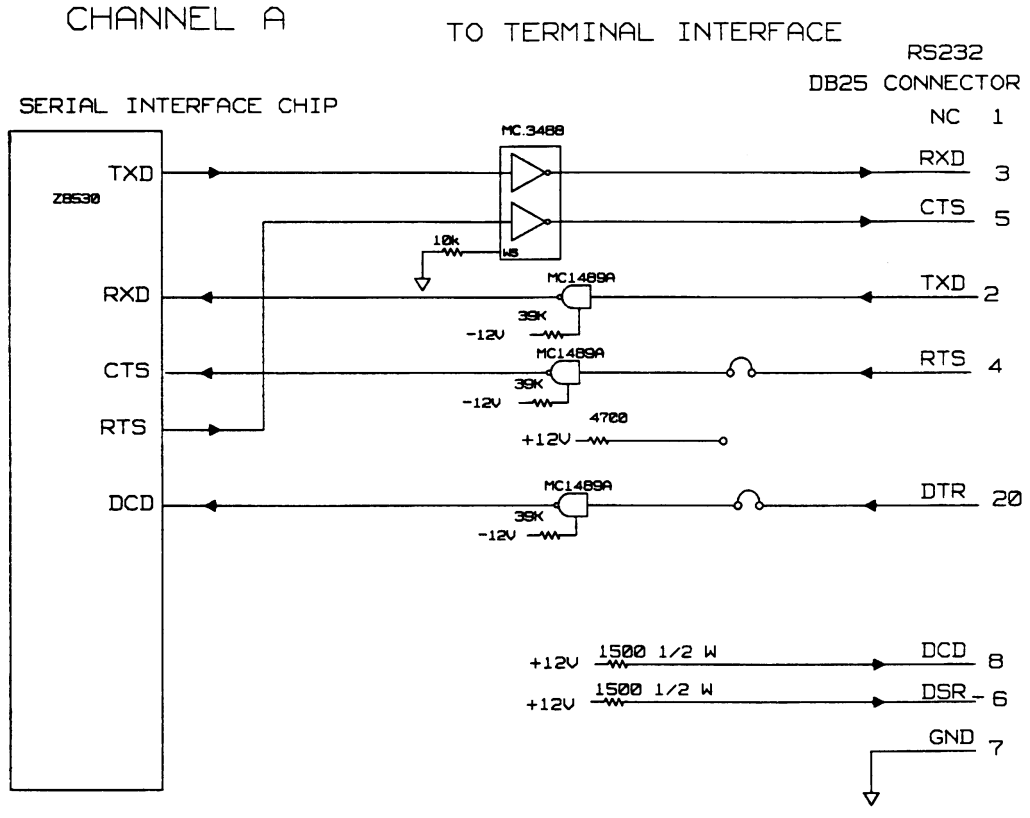
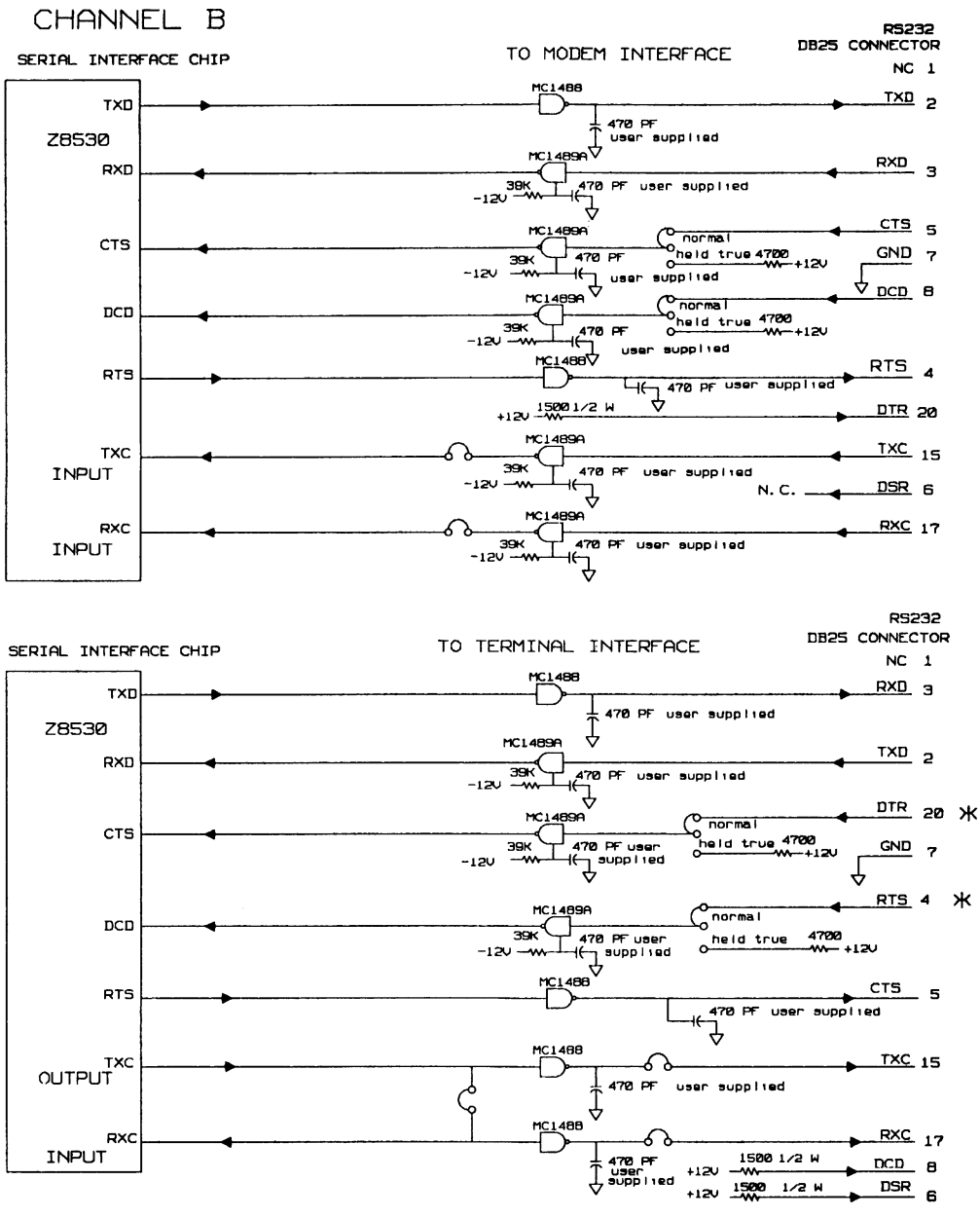


FIGURE 4-1. MVME117 Serial Interface (Port 1 = Channel A)



* DTR(20) and RTS(4) are reversed when jumpered for VERSAdos version 4.5

FIGURE 4-2. MVME117 Serial Interface (Port 2 = Channel B)

TABLE 4-2. ROM/EPROM Socket Jumper Information

JUMPER 1 (NOTE 1)	JUMPER 0 (NOTE 2)	PART SIZE	SOCKET PAIR #1 (NOTE 4)	SOCKET PAIR #2 (NOTE 5)
IN	IN	8K x 8	F00000 - F03FFF	F04000 - F07FFF
IN	OUT	16K x 8	F00000 - F07FFF	F08000 - F0FFFF
OUT	IN	32K x 8	F00000 - F0FFFF	F10000 - F1FFFF
OUT (NOTE 3)	OUT	64K x 8	F00000 - F1FFFF	F20000 - F3FFFF

NOTES: 1. JUMPER 1 is part of the 2 x 18 header (J1, pins 31 and 32).
2. JUMPER 0 is part of the 2 x 18 header (J1, pins 29 and 30).
3. Factory configuration.
4. For socket pair #1, U18 = even bytes and U28 = odd bytes.
5. For socket pair #2, U37 = even bytes and U48 = odd bytes.

Parallel/Printer Interface

The parallel/printer interface is implemented with two 74ALS652s, octal bus transceivers/registers. A 74LS794 and a PAL are used to control the ALS652's. These devices set up the signals necessary to control the direction of data transfer and also provide two of the handshake outputs. The STROBE* handshake signals are generated by writing a 0 to the correct bit position and then writing a 1 to the same bit. Two independent 8-bit ports are provided for general I/O or for a Centronics printer port. (A minimum current sink of 24 mA is sufficient for the printer port.) Each port has an associated DIRECTION control bit that programs it as latched output (DIRECTION=0) or a buffered input (DIRECTION=1). The two input handshake lines (ACK) are buffered and provide interrupt capability. These lines are level sensitive and may be programmed to interrupt the processor on either positive or negative pulses. To program the ACK line to interrupt on a positive pulse, the corresponding jumper on header J7 should be left off (EDGE=1 into the PAL). When a port is programmed as an input (DIRECTION=1), the user has a choice of latching the 8 bits with the same ACK pulse that is used to request an interrupt from the MPU (if enabled), or just buffering the 8 input bits. This choice is programmed by the bit INPUT LATCH ENABLE signal of the Parallel Port Control Register (PPCR) at address $F44005. If this bit is a 0, the input is latched on the selected pulse of the ACK signal; if this bit is a 1, the input is sampled when the MPU reads the corresponding port. Two bits

of a status register are used as interrupt flags for the two individual 8-bit ports. In the polled mode, these flags signal pending events of the ACK signal. If those bits are a logic 1, interrupts (or ACKs) are pending for the ports. A write to location CP1FLAG clears the port #1 ACK/interrupt flag. Similarly, a write to location CP0FLAG clears the port #0 ACK/interrupt flag. For PPCR bit assignments refer to Table 4-3. After a reset, the PPCR = $FF. (Refer also to port pin assignments in Chapter 5.)

TABLE 4-3. Parallel/Printer Port Control Register Bit Assignments

DATA BIT	PORT NUMBER	DESCRIPTION
D7	Port #1	Direction (0=output, 1=input)
D6	Port #1	Strobe (0=low, 1=high output level)
D5	Port #1	Input Latch Enable (0=enabled)
D4	Port #1	Interrupt Enable (0=enabled)
D3	Port #0	Direction (0=output, 1=input)
D2	Port #0	Strobe (0=low, 1=high output level)
D1	Port #0	Input Latch Enable (0=enabled)
D0	Port #0	Interrupt Enable (0=enabled)

SCSI Interface

The SCSI bus is defined by the ANSI X3T9.2 committee. It is a superset of the SASI interface and is downward compatible with SASI peripheral controllers. The single-ended, open collector version is implemented. The bus is composed of 18 lines (8 data, one parity, and 9 control lines). Communication is achieved through eight bus phases. These phases are used to establish communication between two devices (initiator is usually this module, target is the I/O device, but this module has the ability to be both initiator and target in the same system), and to pass control, status, and data.

SCSI interfacing is implemented through the NCR 5380 SCSI bus controller (on MVME117-3 or -3FP only). The transition module has socketed terminators for the SCSI bus. This bus is available on the P2 connector. (Refer to the pin assignments table in Chapter 5.)

Each device on the SCSI bus is given an ID number (between 7 and 0, highest priority being 7). The MVME117 can be used with any ID number. The ID number is configured by the user through software.

The NCR 5380 SCSI interface chip is set up to run in a non-DMA mode. The registers on the chip can be used to directly control the SCSI bus lines. In the Programmed I/O mode, the bus handshake lines must be individually manipulated through software to transfer data, greatly slowing down transfer speeds. To improve performance, the MPU can access the NCR 5380 in a pseudo-DMA mode where bus handshake lines are automatically controlled (through the FSCSI, fast SCSI memory locations at $F5C001 and $F5C00D). This pseudo-DMA mode more than doubles data transfer speed.

In this configuration, the processor speed and the opcode fetch time limit the performance. With code run out of RAM (0 wait state), the effective data transfer rate is about 470Kb/sec. If slower controllers are used, then the limiting factor is the controller transfer rate. Furthermore, an extremely slow SCSI or SASI controller may cause a bus time-out error if the controller does not provide data within 120 microseconds. The FSCSI channel waits for the data to become available to finish its bus cycle. If a bus cycle exceeds 120 microseconds, a bus time-out will occur. Software should retry the access in these cases.

SOFTWARE INTERFACE

The following paragraphs contain overviews of the RS-232C and SCSI interfaces.

RS-232C Interface

The Z8530A serial communications controller is capable of both synchronous and asynchronous protocols. The P2 serial port of the MVME117 is multiprotocol and may be wired to a terminal or to a modem. The J6 debug monitor and the VERSAdos port for the MVME117 support only asynchronous communication.

SCSI Interface

The following overview of the SCSI software interface describes general protocol (excluding error recovery) for a few of the performed functions.

To relieve the user of having to follow SCSI bus protocol, the SCSI firmware allows the user to pass commands to the bus through high level command packets. With this method, the firmware interface can greatly speed up the user software development cycle.

When using the SCSI firmware, the user has two mode options. Interrupt mode is the most processor-efficient mode of operation. Multitasking is allowed in this mode for targets that support Arbitration, Reselection, and the Message Out Phase. The MC68010 processor is returned to the user whenever the SCSI bus is slowed down (in between phases), or whenever the target disconnects with a pending reselection; this allows commands on the bus to be overlapped.

A general TRAP #15 interface using polled mode is also provided for the user who cannot tolerate interrupts. The processor stays inside the SCSI firmware until the command is finished or until user interaction is required.

Examples of SCSI operation are as follows.

Writing to Magnetic Memory

This consists of the following steps.

a. The SCSI interface is commanded to arbitrate for the bus. When arbitration is won and the proper SCSI controller has been selected, proceed to step b.

b. Identify message is sent to SCSI controller, selecting proper disk drive. Command description block is sent to controller specifying write operation, disk location and length of data block.

c. Data is transferred to controller. If all the data is transferred, or if the controller buffer fills, or if a time-consuming seek is required, the controller may send a disconnect to the host.

d. After the data in the controller buffer has been written onto disk, the controller arbitrates for the bus, wins and reselects the host. If more data is to be written, go to step c. Otherwise, the controller sends ending status to the host, followed by a command complete message. The controller considers the write complete and disconnects from the bus.

The media has been written to.

Reading from Magnetic Memory

This consists of the following steps.

a. The SCSI interface is commanded to arbitrate for the bus. When arbitration is won and the SCSI controller has been selected, proceed to step b.

b. The Identify message is sent to the controller, specifying disk drive and ability for reselection. The command description block is then sent to the controller, specifying a read operation, starting address, and length.

c. The disk controller may disconnect from the bus for the seek/read operation. When the data buffer is full, or all data has been read, the disk controller reselects the host.

d. Data is transferred to the host until the controller buffer is empty. If all the data has not been transferred, go to step c.

e. The disk controller sends ending status to the host followed by a command complete message. The controller now disconnects from the bus.

The read operation is now complete.

Other Uses

In addition to the above uses, the SCSI interface can be used to interface with printer controllers, to pass messages between hosts, and to interface to a LAN controller.

MODULE CONFIGURATION NUMBER

An eight bit register at address $F4400D is provided to indicate to the software the module configuration such as RAM size, and depopulation options. (Refer to the memory map in Chapter 3.) The module product numbers and their corresponding configuration numbers are listed in the table below.

MVME117 Configuration Number

PRODUCT NUMBER	RAM CHIP SIZE (BITS)	ONBOARD MEMORY (BYTES)	SCSI (Y/N)	MC68881	CONFIG. NUMBER
MVME117-03	256K x 1	512K	Y	N	02
MVME117-04	256K x 1	512K	N	N	03
MVME117-3FP	256K x 1	512K	Y	Y	06

SOURCES OF BUS ERROR

There are three sources of bus error:

- Parity error from onboard RAM
- VMEbus bus error
- Onboard time-out (an access to a non-existent device or a write access to EPROM space) or a local time-out (MPU did not obtain VMEbus mastership within 120 microseconds)

The onboard status register at address $F44009 has two status bits to indicate the bus error source. One bit is for onboard parity error and the other bit indicates a local time-out bus error or onboard time-out. (Refer to the memory map in Chapter 3.)

PARALLEL PORT

The following paragraphs cover first time initialization, interrupt handling, strobe handshake, data movement, and operation as a Centronics printer port.

First Time Initialization

After a reset, the PPCR at address $F44005 is initialized by hardware to $FF. This configuration leaves the interrupts disabled. The ports are configured for input. To change them to output mode, a 0 should be written to the Direction bits of the control register. After the Direction bits are programmed, the user may wish to have the ACK lines interrupt the MPU. The interrupts are enabled by writing a 0 to the Interrupt Enable bits of the parallel port control register. If the parallel port is programmed as input, the user may wish to latch the inputs on a particular edge of the ACK* signal. The edge selection is done through the EDGE (level) jumpers at header J7 on the MVME117. The latching of inputs is accomplished through the Input Latch Enable bits of the parallel port control register. (Refer to the memory map in Chapter 3.)

Interrupt Handling

If the interrupts were enabled as described above, they would use level 4 to vector a service routine. Both 8-bit ports use the same interrupt level on the MVME117. To distinguish between the two sources, two bits in the status register determine which of the two ports (which handshake, in reality) have an interrupt pending. The service routine must first decide which port to service, and then act accordingly. In the case where both ports have simultaneous interrupts, a priority selection is necessitated. Next, the user's service routine would probably clear the latched interrupt. This is accomplished by writing to either the dummy location CP0FLAG ($F44009) for parallel port #0 or by writing to the dummy location CP1FLAG ($F4400B) for parallel port #1.

In a polled environment, the reception of ACK strobe is signaled by the corresponding PPXFLAG (X=0, 1) in the Module Status Register (MSR) at address $F44009. Writing to the dummy location CPXFLAG (X=0, 1) clears the PPXFLAG (X=0, 1).

Strobe Handshake

This output signals to an external device that either the associated port has an output ready or that the port has read the external byte. Two consecutive bit writes (e.g., if STROBE=1, a 1-0 store) to the parallel port control register by the MPU causes the STROBE output to follow the level last written to the control register.

Data Movement

The movement of data to or from the ports is accomplished by a MOVE instruction to or from the addressed port. If the port is programmed as an output, the contents of the port may also be read. If the port is programmed as an input, writing to it has no effect. The two ports may be addressed as a 16-bit port by the use of the MOVEP.W instruction. (Note: the parallel ports are on the lower half of the data bus, so they do not form a word in the memory map; they are just two consecutive odd bytes.)

Operation as a Centronics Printer Port

The two 8-bit parallel ports are wired for a Centronics printer port on the MVME708A/ MVME708-1 transition module. In order to use the connector, parallel port #1 is the output port; port #1 STB* is the printer DATA STROBE*, parallel port #0 is the status port, and port #1 ACK* is the printer acknowledge. The signals wired for the printer port and parallel port are listed in Table 4-4. (Refer to Chapter 5 for the printer and parallel port pinouts.)

TABLE 4-4. Printer Signals and Corresponding Parallel Port Signals

PRINTER SIGNAL	CORRESPONDING PARALLEL PORT SIGNAL
DATA STROBE*	PORT #1 STB (PPCR)
DATA 1	PORT #1 D0
DATA 2	PORT #1 D1
DATA 3	PORT #1 D2
DATA 4	PORT #1 D3
DATA 5	PORT #1 D4
DATA 6	PORT #1 D5
DATA 7	PORT #1 D6
DATA 8	PORT #1 D7
PACK*	PORT #1 ACK*
PRINTER BUSY	PORT #0 D7
PE (out of paper)	PORT #0 D6
SLCT	PORT #0 D5
IN PRIME*	PORT #0 STB (PPCR)

TABLE 4-4. Printer Signals and Corresponding Parallel Port Signals (cont'd)

PRINTER SIGNAL	CORRESPONDING PARALLEL PORT SIGNAL
FAULT*	PORT #0 ACK*
LIGHT DETECT* (video error)	PORT #0 D4

NOTE: Some printers use pin 14 as an auto line feed enable when low. On this interface, pin 14 is logic ground which may cause extra line feeds (double spacing).

The following is an example of how to print a character.

Port 1 output (data)
Port 0 input (status)

Move $6E into PPCR	(F44005)	Configure the parallel port: port 1 as output, port 0 as input, both strobes high, interrupts enabled.
Write to CP0FLAG	(F44009)	Clears any interrupt flag for port 0 (fault flag).
Write to CP1FLAG	(F4400B)	Clears any interrupt flag for port 1 (acknowledge flag).
Check MSR	(F44009)	Read Module Status Register. Check to be sure the acknowledge flag is false (D7 = 0). If flag is true (D7 = 1), branch back to "Write to CP1FLAG" step to clear acknowledge flag. This is for printers with long acknowledge pulse width.
Write character into PIO #1	(F44003)	Put character into port 1 register.
Clear bit 6 in PPCR	(F44005)	Strobe line low.
Set bit 6 in PPCR	(F44005)	Strobe line high.

Read MSR	(F44009)	Read Module Status Register.Check for interrupt flags (D7 = printer acknowledge flag, D6 = printer fault status).

NOTES: 1. If enabled, an interrupt will result from a printer acknowledge, or a printer fault.

2. Printer interrupt level = 4, vector number = $42, and VBR offset = $108.

After receipt of an acknowledge, clear any interrupt flags and repeat above procedure.

REAL-TIME CLOCK

The following sections explain first time initialization, time setting, and reading the time correctly.

First Time Initialization

When the RTC chip is first installed and power applied, the device will need to be properly initialized. The following procedure should be followed:

a. Disable the interrupt from the RTC to the MPU to allow oscillator setting. Write $7 into the control register. The clock and interrupt start/stop bits are now set to 1, ensuring that the clock and interrupt timers are both halted. The interrupt register is selected.

b. Write 0 to the interrupt register. Ensure that there are no interrupts programmed.

c. Set the clock to the proper time as described in the next section.

Setting the Time

Follow these steps upon installation and any time the clock has to be reset.

a. Write $5 to the control register. The clock is now halted (not in test mode). The clock setting register is now selected by the interrupt select bit.

b. Set the 12/24 hours mode (write to the clock setting register to select the hours counting mode required).

c. Load real-time registers. All registers (AM/PM and leap year included) may now be loaded in any order.

NOTE

In writing the leap year and AM/PM bit, the 12/24 hours mode must be loaded with the same value as in step b.

d. Write 0 to the control register. This finishes the clock setting by starting the clock again. This final control register write should be synchronized to an external time source.

NOTE

Oscillator Y3 for the real-time clock chip has an accuracy of 6 seconds per day or less, over the operating temperature range of the MVME117.

Reading the Time Correctly

In order to ensure the clock has not been automatically updated while reading the current time (causing an erroneous reading), the following algorithm should be used to read the time.

Entry

a. Read RTC control register. This clears the data changed flag.

b. Read all time registers, store results in RAM.

c. Read RTC control register. If "data changed" is set, go to step a. above.

Exit

SERIAL PORT SETUP EXAMPLE

This example of serial port setup has:
9600 baud, asynchronous only;
Interrupt on Received Character, Transmitter Ready, External Status;
Interrupt level = 6, interrupt vector is programmable via vector register.

SETUP:

Move $30 into SCCWRO	(F48001)	Clear receiver error status.
Move $10 into SCCWRO	(F48001)	Clear external status interrupts.
Move $09 into SCCWRO	(F48001)	Write the register pointer.
Move $80 into SCCWRO	(F48001)	Reset Channel A.

Move $09 into SCCWRO	(F48001)	Write the register pointer.
Move $40 into SCCWRO	(F48001)	Reset Channel B.
Move $0A into SCCWRO	(F48001)	Write the register pointer.
Move $00 into SCCWRO	(F48001)	Make sure NRZ format is set.
Move $0E into SCCWRO	(F48001)	Write the register pointer.
Move $82 into SCCWRO	(F48001)	Disable the baud rate generator.
Move $04 into SCCWRO	(F48001)	Write the register pointer.
Move $44 into SCCWRO	(F48001)	Divide by 16, no parity, one stop bit.
Move $03 into SCCWRO	(F48001)	Write the register pointer.
Move $C1 into SCCWRO	(F48001)	Receiver: eight bits, receiver enabled.
Move $05 into SCCWRO	(F48001)	Write the register pointer.
Move $EA into SCCWRO	(F48001)	Transmitter: eight bits, transmitter enabled, DTR on, RTS on.

BAUD RATE TABLE

BAUD RATE	VALUE	ERROR
50	$0C33	
75	$0821	
110	$05A4	
134.5	$0488	
150	$0410	
300	$0207	
600	$0102	+0.2%
1200	$0080	+0.2%
1800	$0055	-0.2%
2000	$004C	+0.2%
2400	$003F	+0.2%
3600	$0029	+0.9%
4800	$001F	-1.4%
7200	$0014	-1.4%
9600	$000E	+1.7%
19200	$0006	+1.7%

Move $0C into SCCWRO	(F48001)	Write the register pointer.
Move $0E into SCCWRO	(F48001)	Write lower byte of baud rate.
Move $0D into SCCWRO	(F48001)	Write the register pointer.
Move $00 into SCCWRO	(F48001)	Write upper byte of baud rate.
Move $0B into SCCWRO	(F48001)	Write the register pointer.
Move $56 into SCCWRO	(F48001)	RX clock = TRXC pin, TX clock = TRXC pin, TRXC = output, TRXC = baud rate generator output.
Move $0E into SCCWRO	(F48001)	Write the register pointer.
Move $83 into SCCWRO	(F48001)	Clock source = baud rate generator.
Move $01 into SCCWRO	(F48001)	Write the register pointer.
Move $11 into SCCWRO	(F48001)	Interrupt on Receive Character, external interrupt enable.
Move $0F into SCCWRO	(F48001)	Write the register pointer.
Move $80 into SCCWRO	(F48001)	Enable break interrupts.
Move $09 into SCCWRO	(F48001)	Write the register pointer.
Move $08 into SCCWRO	(F48001)	Master interrupt enable.
Move $02 into SCCWRO	(F48001)	Write the register pointer.
Move $80 into SCCWRO	(F48001)	Interrupt Vector number ($80 = offset $200).

Put interrupt handler starting address into interrupt vector table at offset $200.

INTERRUPT HANDLER:

Move $03 into SCCWRO	(F48001)	Write the register pointer.
Read status from RR3	(F48001)	Read RR3 for interrupt cause.

Check the interrupt pending bits for each channel and cause.
Branch to the appropriate handler routine.

TRANSMIT A CHARACTER:

Transmitter interrupts must be enabled before outputting a character or else an interrupt will never occur.

Move $01 into SCCWRO	(F48001)	Write the register pointer.
Move $13 into SCCWRO	(F48001)	Enable transmitter interrupts.
Move output char. into SCCDR	(F48003)	Write char. into data register.
Move $38 into SCCWRO	(F48001)	Reset interrupt-under-service flag.

TRANSMITTER READY INTERRUPT HANDLER:

Move $01 into SCCWRO	(F48001)	Write the register pointer.
Move $11 into SCCWRO	(F48001)	Disable transmitter interrupts.

Do we have more characters to transmit?
If Yes, go do TRANSMIT A CHARACTER.
If No, return.

Move $38 into SCCWRO	(F48001)	Reset interrupt-under-service flag.

RECEIVED CHARACTER INTERRUPT HANDLER:

Move $01 into SCCWRO	(F48001)	Write the register pointer.
Read status from RR0	(F48001)	Read RR0 to check for status.

Check for framing errors, receiver overrun, parity errors.

Read data from SCCDR	(F48003)	Read character.
Move $38 into SCCWRO	(F48001)	Reset interrupt-under-service flag.

Return.

EXTERNAL STATUS INTERRUPT HANDLER:

Break -- either start of break or end of break.
CTS -- a transition has occurred on the CTS input pin.
DCD -- a transition has occurred on the DCD input pin.

Move $01 into SCCWRO	(F48001)	Write the register pointer.
Read status from RR0	(F48001)	Read RR0 to check for status.
Move $10 into SCCWRO	(F48001)	Reset external status interrupt.

Do action necessary.

If break bit is low, which is the end of a break, a null character is still in the receive buffer.

Read data from SCCDR	(F48003)	Read null from data register.
Move $38 into SCCWRO	(F48001)	Reset interrupt-under-service flag.

MC68B40 TIMER SETUP EXAMPLE

This example of the MC68B40 timer setup has:
Interrupt every 10 msec by timer 3; and
Watchdog (reset after 10 sec) by timer 1.

Move $01 into CRX2	(F50003)	Allow writes to control reg. 1.
Move $01 into CRX1	(F50001)	All timers held in present state. Set timer 1.
Move $00 into CRX2	(F50003)	Allow writes to control reg. 3.
Move $C6 into CRX1	(F50001)	Configure timer 3 for internal clock, interrupt enabled, output enabled, 8-bit mode.
Move $03 into T1MSB	(F50005)	Set timer 1 ($03E8 = 1000).
Move $E8 into T1LSB	(F50007)	Set timer 1.
Move $30 into T3MSB	(F5000D)	Set timer 3 ($30CB = 12491).
Move $CB into T3LSB	(F5000F)	Set timer 3.
Move $01 into CRX2	(F50003)	Allow writes to control reg. 1.
Move $C0 into CRX1	(F50001)	Configure timer 1 for external clock, interrupt enabled, output enabled,enable all timers.

Timer 3 will now interrupt every 10 msec.
Timer 1 will now assert RESET* in 10 seconds unless cleared.

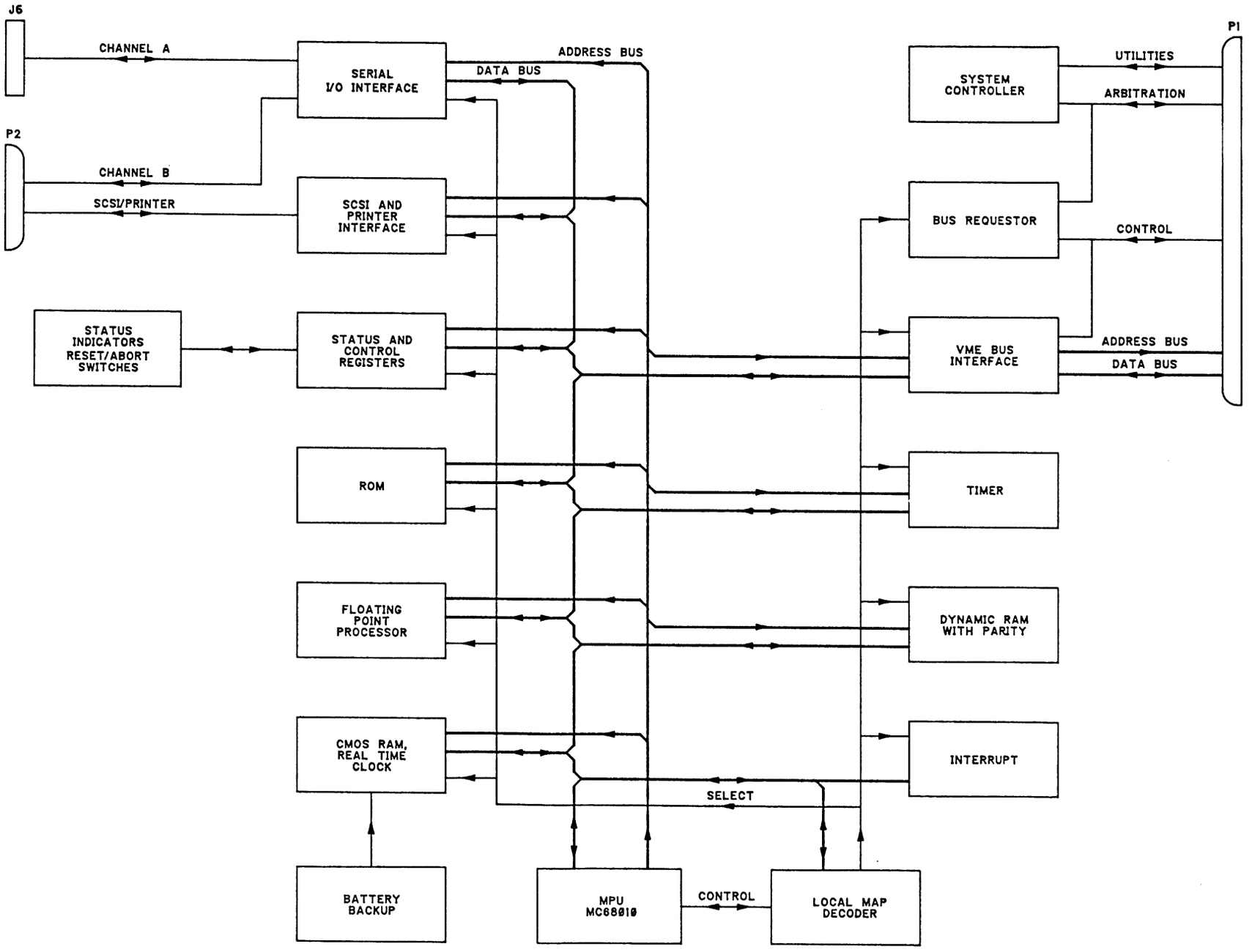
Timer interrupt level = 5, timer interrupt vector number = $41, offset = $104.

To clear timer interrupts:

Read status register	(F50003)	Status register has flags indicating which timer is interrupting.
Read timer 1 counter	(F50005) and (F50007)	
Read timer 3 counter	(F5000D) and (F5000F)	
Read control register	(F50001)	Clears interrupt from timer 1.

NOTE

Timer 3 is still running. If not reinitialized a watchdog reset occurs in 10 seconds.



BLOCK DIAGRAM
63DW3393B REV C SH 3 OF 19

FIGURE 4-3. MVME117 Block Diagram

CHAPTER 5 - SUPPORT INFORMATION

INTRODUCTION

This chapter provides the interconnection signals, parts list with parts location illustration, and schematic diagram for the MVME117 module.

INTERCONNECT SIGNALS

The MVME117 module interconnects with the VMEbus through connector P1, with P2 adapter board and transition module MVME708A/MVME708-1 through connector P2, and with an RS-232C device through J6.

Connector P1 Interconnect Signals

Connector P1 is a standard DIN 41612 triple-row, 96-pin male connector. All Motorola VMEbus specifications are met by the MVME117 module. Each pin connection, signal mnemonic, and signal characteristic for the connector are listed in Table 5-1.

TABLE 5-1. Connector P1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A8	D00-D07	DATA bus (bits 0-7) - eight of 16 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
A9	GND	GROUND
A10	SYSCLK	SYSTEM CLOCK - a 16 MHz input signal used as a timing reference. This signal is provided by the VMEbus system controller.
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - input signal that indicates a data transfer on data bus lines D08-D15.
A13	DS0*	DATA STROBE 0 - input signal that indicates a data transfer on data bus lines D00-D07.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A14	WRITE*	WRITE - input signal that specifies the direction of data transfers.
A15	GND	GROUND
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - this output signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
A17	GND	GROUND
A18	AS*	ADDRESS STROBE - the falling edge of this input signal indicates a valid address is present on the address bus.
A19	GND	GROUND
A20	IACK*	INTERRUPT ACKNOWLEDGE - input signal that indicates a VME interrupt acknowledge cycle. The VME system controller has been interrupted on one of seven levels and is now acknowledging the specific interrupt with a service routine.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - IACKIN* and IACKOUT* form a daisy-chained acknowledge. The standard Motorola VMEbus backplane must have jumpers installed to continue the daisy-chained interrupt acknowledge beyond vacant card slots. This input signal is used when the controller module forms part of the daisy-chained interrupt acknowledge sequence.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - IACKIN* and IACKOUT* form a daisy-chained acknowledge. The standard Motorola VMEbus backplane must have jumpers installed to continue the daisy-chained interrupt acknowledge beyond vacant card slots. This input signal is used when the controller module forms part of the daisy-chained interrupt acknowledge sequence.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A23	AM4	ADDRESS MODIFIER (bit 4) - one of the three-state input lines that provide additional information about the address bus, such as size, cycle type, and/or data transfer bus master identification.
A24	A07	ADDRESS bus (bit 7) - one of 16 three-state input lines that specify an address in the memory map. Only the least significant 16 bits of the 23 associated VMEbus address lines are employed on the controller module.
A25	A06	ADDRESS bus (bit 6) - same as A07 on pin A24.
A26	A05	ADDRESS bus (bit 5) - same as A07 on pin A24.
A27	A04	ADDRESS bus (bit 4) - same as A07 on pin A24.
A28	A03	ADDRESS bus (bit 3) - one of 16 three-state input lines that specify an address in the memory map. During an interrupt acknowledge cycle, address bus lines A01-A03 are used to indicate the interrupt level that is being acknowledged.
A29	A02	ADDRESS bus (bit 2) - same as A03 on pin A28.
A30	A01	ADDRESS bus (bit 1) - same as A03 on pin A28.
A31	-12 VDC	-12 Vdc Power - used by the logic circuits on the controller module.
A32	+5 VDC	+5 Vdc Power - used by the logic circuits on the controller module.
B1	BBSY*	BUS BUSY - This signal is driven low when the controller module is the bus master. This signal is an input to the arbiter to indicate that the bus may be arbitrated.
B2		Not used.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B3	ACFAIL*	AC FAILURE - Input signal that indicates a power failure has occurred and generates a level seven interrupt request.
B4	BG0IN*	BUS GRANT 0 IN - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. A grant received at the jumpered level indicates the MVME117 may become the bus master. The remaining three bus-grant-in lines are connected directly to their respective bus-grant-out lines.
B5	BG0OUT*	BUS GRANT 0 OUT - bus-grant-in and bus-grant-out form a daisy-chained bus grant. When a bus- grant-in is received at the jumpered level and the MPU is not awaiting bus mastership, the bus-grant-out signal is true on the respective level.
B6	BG1IN*	BUS GRANT 1 IN - same as BG0IN on pin B4.
B7	BG1OUT*	BUS GRANT 1 OUT - same as BG0OUT on pin B5.
B8	BG2IN*	BUS GRANT 2 IN - same as BG0IN on pin B4.
B9	BG2OUT*	BUS GRANT 2 OUT - same as BG0OUT on pin B5.
B10	BG3IN*	BUS GRANT 3 IN - same as BG0IN on pin B4.
B11	BG3OUT*	BUS GRANT 3 OUT - same as BG0OUT on pin B5.
B12-B15	BR0*-BR3*	BUS REQUEST (0-3) - the bus request at the jumpered level is true when the MPU requires bus mastership. When one or more bus request lines is true in the ROR mode, bus mastership is released. When the controller module is the system controller, bus request level three is monitored by the arbiter.
B16-B19	AM0-AM3	ADDRESS MODIFIER (bits 0-3) - same as AM4 on pin A23.
B20	GND	GROUND
B21,B22		Not used.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B23	GND	GROUND
B24-B30	IRQ7*- IRQ1*	INTERRUPT REQUEST (7-1) - seven prioritized interrupt request inputs. Jumper enabled, level seven is the highest priority.
B31		Not used.
B32	+5 VDC	+5 Vdc Power - same as +5 VDC on pin A32.
C1-C8	D08-D015	DATA bus (bits 8-15) - eight of 16 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
C9	GND	GROUND
C10	SYSFAIL*	SYSTEM FAIL - reflects state of FAIL bit in MCR and fail indicator. When enabled in MCR, this bidirectional signal generates an interrupt request.
C11	BERR*	BUS ERROR - an active low output signal that indicates an error has occurred during a data transfer cycle.
C12	SYSRESET*	SYSTEM RESET - the system controller provides this input signal that causes a board level reset on the controller module.
C13	LWORD*	LONGWORD - three-state driven signal to indicate that the current transfer is a 32-bit transfer.
C14	AM5	ADDRESS MODIFIER (bit 5) - same as AM4 on pin A23.
C15	A23	ADDRESS bus (bit 23) - same as A07 on pin A24.
C16	A22	ADDRESS bus (bit 22) - same as A07 on pin A24.
C17	A21	ADDRESS bus (bit 21) - same as A07 on pin A24.
C18	A20	ADDRESS bus (bit 20) - same as A07 on pin A24.
C19	A19	ADDRESS bus (bit 19) - same as A07 on pin A24.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C20	A18	ADDRESS bus (bit 18) - same as A07 on pin A24.
C21	A17	ADDRESS bus (bit 17) - same as A07 on pin A24.
C22	A16	ADDRESS bus (bit 16) - same as A07 on pin A24.
C23	A15	ADDRESS bus (bit 15) - same as A07 on pin A24.
C24	A14	ADDRESS bus (bit 14) - same as A07 on pin A24.
C25	A13	ADDRESS bus (bit 13) - same as A07 on pin A24.
C26	A12	ADDRESS bus (bit 12) - same as A07 on pin A24.
C27	A11	ADDRESS bus (bit 11) - same as A07 on pin A24.
C28	A10	ADDRESS bus (bit 10) - same as A07 on pin A24.
C29	A09	ADDRESS bus (bit 9) - same as A07 on pin A24.
C30	A08	ADDRESS bus (bit 8) - same as A07 on pin A24.
C31	+12 VDC	+12 Vdc Power - used by the logic circuits on the controller module.
C32	+5 VDC	+5 Vdc Power - same as +5 Vdc on pin A32.

Connector P2 Interconnect Signals

Connector P2 is a standard DIN 41612 triple-row, 96-pin male connector. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-2. (SIO) = serial I/O, (PARALLEL) = parallel port, (SCSI) = SCSI interface.

TABLE 5-2. Connector P2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1,A2	GND	GROUND
A3	SEL*	SELECT (SCSI) - signal used by an initiator to select a target or by a target to reselect an initiator.
A4	RST*	RESET (SCSI) - OR-tied signal that indicates the RESET condition.
A5	ACK*	ACKNOWLEDGE (SCSI) - signal driven by an initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.
A6	BSY*	BUS BUSY (SCSI) - OR-tied signal that indicates that the bus is being used.
A7	GND	GROUND
A8	DB(7)*	DATA BUS BIT 7 (SCSI) - most significant bit and the highest priority during the Arbitration phase.
A9	DB(5)*	DATA BUS BIT 5 (SCSI)
A10	DB(3)*	DATA BUS BIT 3 (SCSI)
A11	DB(1)*	DATA BUS BIT 1 (SCSI)
A12	GND	GROUND
A13	TXDB	TRANSMIT DATA (channel B) (SIO) - data to be transmitted is furnished on this line to the modem from the terminal.

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A14	RXDB	RECEIVE DATA (channel B) (SIO) - data that is demodulated from the receive line is presented to the terminal by the modem.
A15	CTSB	CLEAR TO SEND (channel B) (SIO) - CTS is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of a message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
A16-A18	GND	GROUND
A19	P0-D0	Port 0, data bit 0 (PARALLEL)
A20	P0-D2	Port 0, data bit 2 (PARALLEL)
A21	P0-D4	Port 0, data bit 4 (PARALLEL) (LIGHT DETECT, a level that indicates the video circuit is not functioning. On some printers, this pin is a ground - when configured for Centronics printer.)
A22	P0-ACK*	Port 0, ACKNOWLEDGE signal (PARALLEL) (FAULT - an input signal that indicates a printer fault condition - when configured for Centronics printer.)
A23	P0-STB*	Port 0, STROBE signal (PARALLEL) (IN PRIME - INPUT PRIME, an output signal that clears the printer buffer and initializes the logic - when configured for Centronics printer.)
A24	P0-D5	Port 0, data bit 5 (PARALLEL) (SLCT - SELECT, an input signal indicating that the printer is selected - when configured for Centronics printer.)
A25	PO-D7	Port 0, data bit 7 (PARALLEL) (PRINTER BUSY - an input signal indicating that the printer cannot receive data - when configured for Centronics printer.)

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A26	P1-ACK*	Port 1, ACKNOWLEDGE signal (PARALLEL) (PACK - PRINTER ACKNOWLEDGE, a low level input pulse indicating that the next character may be sent - when configured for Centronics printer.)
A27	P1-D7	Port 1, data bit 7 (PARALLEL) (DATA 8 when configured for Centronics printer.)
A28	P1-D5	Port 1, data bit 5 (PARALLEL) (DATA 6 when configured for Centronics printer.)
A29	P1-D3	Port 1, data bit 3 (PARALLEL) (DATA 4 when configured for Centronics printer.)
A30	P1-D1	Port 1, data bit 1 (PARALLEL) (DATA 2 when configured for Centronics printer.)
A31	GND	GROUND
A32	REMRESET*	REMOTE RESET* - a remote reset connection for a normally open switch.
B1,B13, B32	+5V	+5 VDC POWER - used by the logic circuits on the MPU module.
B2,B12, B22,B31	GND	GROUND
B3-B11		Not used.
B14-B21		Not used.
B23-B30		Not used.

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C1	I/O*	INPUT/OUTPUT (SCSI) - signal driven by a target which controls the direction of data movement on the bus. True (low) indicates input to the initiator. False (high) indicates output from the initiator. This signal is also used to distinguish between Selection and Reselection phases.
C2	REQ*	REQUEST (SCSI) - signal driven by a target to indicate a request for a REQ/ACK data transfer handshake.
C3	C/D*	CONTROL/DATA (SCSI) - signal driven by the target. It indicates whether control or data information is on the data bus. True (low) indicates CONTROL.
C4	MSG*	MESSAGE (SCSI) - signal driven by the target during the Message phase.
C5,C6	GND	GROUND
C7	ATN*	ATTENTION (SCSI) - signal driven by the initiator. Indicates the attention condition.
C8	DB(P)*	DATA BUS PARITY (SCSI) - data parity is odd. Use of parity is a system option. Parity is not valid during the Arbitration phase.
C9	DB(6)*	DATA BUS BIT 6 (SCSI)
C10	DB(4)*	DATA BUS BIT 4 (SCSI)
C11	DB(2)*	DATA BUS BIT 2 (SCSI)
C12	DB(0)*	DATA BUS BIT 0 (LSB) (SCSI)
C13,C14	GND	GROUND

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C15	RTSB	REQUEST TO SEND (channel B) (SIO) - RTS is supplied by the terminal to the modem when it is required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.
C16	RES1	RESISTOR 1 (SIO) - line wired high through pullup resistor on module.
C17	RXCB	RECEIVE CLOCK (channel B) (SIO) - this line clocks input data from a terminal to a modem.
C18	TXCB	TRANSMIT CLOCK (channel B) (SIO) - this line clocks output data to the modem from the terminal.
C19	DCDB	DATA CARRIER DETECT (channel B) (SIO) - sent by the modem to the terminal to indicate that a valid carrier is being received.
C20	P0-D1	Port 0, data bit 1 (PARALLEL)
C21	P0-D3	Port 0, data bit 3 (PARALLEL)
C22	RES2	RESISTOR 2 (SIO) - line wired high through pullup resistor on module.
C23	RES3	RESISTOR 3 (SIO) - line wired high through pullup resistor on module.
C24	TERMPWR	TERMINATOR POWER (SCSI)
C25	P0-D6	Port 0, data bit 6 (PARALLEL)(PE - PAPER EMPTY, out of paper - when configured for Centronics printer.)
C26	TERMPWR	TERMINATOR POWER (SCSI)
C27	GND	GROUND

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C28	P1-D6	Port 1, data bit 6 (PARALLEL) (DATA 7 when configured for Centronics printer.)
C29	P1-D4	Port 1, data bit 4 (PARALLEL) (DATA 5 when configured for Centronics printer.)
C30	P1-D2	Port 1, data bit 2 (PARALLEL) (DATA 3 when configured for Centronics printer.)
C31	P1-D0	Port 1, data bit 0 (PARALLEL) (DATA 1 when configured for Centronics printer.)
C32	P1-STB*	Port 1, STROBE signal (PARALLEL) (DATA STROBE - an active low output pulse used to clock data from the system to the printer - when configured for Centronics printer.)

Connector J6 Interconnect Signals

Connector J6 is a standard RS-232C DB25 25-pin female connector. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-3. Note that J6 mates with a 25-pin cable to connect to a terminal. For further details, refer to Appendix A.

TABLE 5-3. RS-232C Connector J6 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1		Not used.
2	TXDA	TRANSMIT DATA (channel A) - data to be transmitted is furnished on this line to the modem from the terminal.
3	RXDA	RECEIVE DATA (channel A) - data that is demodulated from the receive line is presented to the terminal by the modem.
4	RTSA	REQUEST TO SEND (channel A) - RTS is supplied by the terminal to the modem when it is required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.
5	CTS	CLEAR TO SEND - CTS is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of a message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
6	DSR	DATA SET READY - DSR is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
7	SIG-GND	SIGNAL GROUND - Common return line for all signals at the modem interface.

TABLE 5-3. RS-232C Connector J6 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
8	DCD	DATA CARRIER DETECT - Sent by the modem to the terminal to indicate that a valid carrier is being received.
9-19		Not used.
20	DTRA	DATA TERMINAL READY - A signal from the terminal to the modem indicating that the terminal is ready to send or receive data.
21-25		Not used.

PARTS LISTS

The components of the MVME117 are listed in Table 5-4. The parts locations are illustrated in Figure 5-1. These parts reflect the latest issue of hardware at the time of printing.

TABLE 5-4. MVME117 Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
--	84-W8393B01	Printed wiring board
BT1	60NW9701A12	Battery, lithium, 3.5 V, 750 mAh, DIP
C1-C12, C14-C27,C29, C31-C35,C37 C40,C41, C43-C45, C47-C48	21NW9632A03	Capacitor, ceramic, axial lead, 0.1 uF + 20% @ 50 Vdc
C13	23NW9704A99	Capacitor, tantalum, radial lead, 33 uF + 20% @ 15 Vdc
C28 --	Not used	
C30,C36	23NW9618A71	Capacitor, electrolytic, radial lead, 47 uF + 20% @ 10 Vdc
C38,C39	21SW992C043	Capacitor, ceramic, 20 pF + 5% @ 50 Vdc
C42	--	Optional, customer-installed
C46	23NW9618A79	Capacitor, electrolytic, radial lead, 100 uF + 20% @ 25 Vdc
CR1,CR2	48NW9616A03	Diode, silicon, 1N4148/1N914
DL1	01NW9804C34	Delay module, triple, 70 ns
DL2	01NW9804C33	Delay module, triple, 40 ns
DS1,DS2	48NW9612A49	LED, red, right angle

TABLE 5-4. MVME117 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
DS3	48NW9612A59	LED, green, right angle
F1	65NW9622A26	Fuse, axial, micro, 1 A, 125 Vdc
--	28NW9802E08	Connector, single socket (2 req'd) (used with F1)
J1,J3-J5,J7	29NW9805C07	Pind, auto-insert (78 required)
--	29NW9805B17	Jumper, insulated, shorting (36 req'd) (used with J1, J3 through J5, J7)
J2	--	Header pad, 3-pin, with trace at pins 1-2
J6	28NW9802G42	Connector, 25-pin, right-angle, D-subminiature, socket
L1	76NW9810A04	Ferrite bead, 0.146 inch by 0.126 inch (at connector P1 pin B1)
P1,P2	28NW9802E51	Connector, 96-pin
Q1,Q3	48NW9610A22	Transistor, NPN, MPS2222, in TO-92 package
Q2	48NW9611A15	Transistor, PNP, 2N3906
R1,R2	06SW-124A23	Resistor, fixed, film, 82 ohms, 5%, 1/4 W
R3	06SW-124A18	Resistor, fixed, film, 51 ohms, 5%, 1/4 W
~~RFR~~4,R7	51NW9626B67	Resistor network, 9/27k ohm
R5,R8,R15, R17,R25,R27, R30,R32,R41, R46	51NW9626B56	Resistor network, 9/10k ohm
R6,R37	06SW-124A97	Resistor, fixed, film, 100k ohms, 5%, 1/4 W

TABLE 5-4. MVME117 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R9,R26	51NW9626B55	Resistor network, 9/4.7k ohm
R10,R11, R34,R35	51NW9626B48	Resistor network, 5/47 ohm
R12	51NW9626A56	Resistor network, 4/22 ohm
R13,R14	51NW9626B64	Resistor network, 4/47 ohm
R16	06SW-124A25	Resistor, fixed, film, 100 ohms, 5%, 1/4 W
R18	06SW-962A83	Resistor, fixed, film, 27k ohms, 5%, 1/8 W
R19	06SW-962A59	Resistor, fixed, film, 2.7k ohms, 5%, 1/8 W
R20	51NW9626B51	Resistor network, 5/1K ohm
R21,R22	06SW-124A17	Resistor, fixed, film, 47 ohm, 5%, 1/4 W
R23	51NW9626A77	Resistor network, 7/22k ohm
R24	06SW-960D47	Resistor, fixed, film, 30.1k ohms, 1%, 1/8 W
R28	06SW-124A96	Resistor, fixed, film, 91k ohms, 5%, 1/4 W
R29	06SW-124A61	Resistor, fixed, film, 3.3k ohms, 5%, 1/4 W
R31	51NW9626B63	Resistor network, 9/39k ohm
R33,R40, R42,R43	06SW-125A53	Resistor, fixed, film, 1.5k ohms, 5%, 1/2 W
R36,R44	06SW-124A73	Resistor, fixed, film, 10k ohms, 5%, 1/4 W
R38,R45	06SW-124A65	Resistor, fixed, film, 4.7k ohms, 5%, 1/4 W
R39	51NW9626B57	Resistor network, 9/1.0k ohm
S1,S2	40NW9801B70	Switch, push, SPDT, momentary

TABLE 5-4. MVME117 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
S3	40NW9801B35	Switch, DIP, SPST, 8-position, piano
U1	(NOTE)	I.C. programmed
--	09NW9811A78	Socket, I.C., DIL, 20-pin (used at U1)
U2-U4, U8-U10, U13-U15, U20-U22, U24-U26, U30-U32	51NW9615P38	I.C. MCM6256P15
U5,U16,U43, U56,U57,U61, U88,U89,U95	51NW9615J39	I.C. 74F74PC
U6,U55,U70	51NW9615F85	I.C. SN74S38N
U7,U12	51NW9615R26	I.C. SN74ALS645-1N
U11	(NOTE)	I.C. programmed
--	09NW9811B01	Socket, I.C., DIL, 24-pin (used at U11)
U17,U64	51NW9615K67	I.C. 74F20PC
U18,U28 U37,U48	--	Customer-supplied
XU18,XU28, XU37,XU48	09-W4659B14	Socket, I.C., SIL, 14-pin (2 each req'd)
U19,U23,U29, U33,U36,U38	51NW9615G07	I.C. SN74S244N
U27	51NW9615E95	I.C.SN74LS240N

TABLE 5-4. MVME117 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U34	(NOTE)	I.C. programmed
--	09-W4659B10	Socket, I.C., SIL, 10-pin (2 req'd) (used at U34)
U35	(NOTE)	I.C. programmed
--	09-W4659B10	Socket, I.C., SIL, 10-pin (2 req'd) (used at U35)
U39,U66	51NW9615K66	I.C. 74F32PC
U40,U90	51NW9615K71	I.C. 74F04PC
U41,U45,U51	51NW9615N45	I.C. 74F257PC
U42	(NOTE)	I.C. Programmed PAL
--	09NW9811A78	Socket, I.C., DIL, 20-pin (used at U42)
U44	51NW9615L74	I.C. 74F163APC
U46,U58	51NW9615K72	I.C. 74F02PC
U47	51NW9615C22	I.C. SN74LS08N
U49	51NW9615K18	I.C. 74F373PC
U50,U87	51NW9615K70	I.C. 74F08PC
U52,U53	51NW9615K98	I.C. 74F280PC
U54	(NOTE)	I.C. programmed
--	09NW9811A78	Socket, I.C., DIL, 20-pin (used at U54)
U59,U69	51NW9615K73	I.C. 74F00PC
U60	51NW9615M11	I.C. MC68010L10
--	09-W4659B32	Socket, I.C., SIL, 32-pin (2 req'd) (used at U60)
U62	51NW9615N72	I.C. MC68881RC12 (for MVME117-3FP only)

TABLE 5-4. MVME117 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
XU62	09NW9811A71	Socket, I.C., PGA, 68-pin (used at U62)
U63	51NW9615F30	I.C. DM74S05N
U65	51NW9615K65	I.C. 74F64PC
U67	51NW9615E91	I.C. SN74LS00N
U68,U73	51NW9615F02	I.C. SN74LS244N
U71,U104	51NW9615K69	I.C. 74F10PC
U72	51NW9615N47	I.C. MC3488AP1
U74	51NW9615F59	I.C. MC68B40P
--	09-W4659B14	Socket, I.C., SIL, 14-pin (2 req'd) (used at U74)
U75,U96	51NW9615R38	I.C. SN74LS794N
U76	51NW9615P52	I.C. SN74ALS245N
U77	51NW9615R67	I.C. NCR/5380 (for MVME117-3,-3FP only)
--	09-W4659B20	Socket, I.C., SIL, 20-pin (2 req'd) (used at U77) (for MVME117-3, -3FP only)
U78	51NW9615S50	I.C. ICL8212CPA
U79	51NW9615R66	I.C. MM58274N
U80	51NW9615P58	I.C. MC74HC32N
U81	51NW9615R62	I.C. TC5517APL-2
XU81	09-W4659B14	Socket, I.C., SIL, 14-pin (2 req'd) (used at U81)
U82,U83	51NW9615B30	I.C. MC1489AP
U84	51NW9615B29	I.C. MC1488P

TABLE 5-4. MVME117 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U85	51NW9615F38	I.C. SN74LS393N
U86	51NW9615R68	I.C. Z8530APC
--	09-W4659B20	Socket, I.C., SIL, 20-pin (2 req'd) (used at U86)
U91	51NW9615E93	I.C. SN74LS14N
U92	(NOTE)	I.C. programmed
--	09-W4659B12	Socket, I.C., SIL, 12-pin (2 req'd) (used at U92)
U93	(NOTE)	I.C. programmed
--	09-W4659B08	Socket, I.C., SIL, 8-pin, (2 req'd) (used at U93)
U94	(NOTE)	I.C. programmed
--	09-W4659B10	Socket, I.C., SIL, 10-pin (2 req'd) (used at U94)
U97,U106	51NW9615S03	I.C. SN74ALS652NT
U98	(NOTE)	I.C. programmed
--	09-W4659B10	Socket, I.C., SIL, 10-pin (2 req'd) (used at U98)
U99	(NOTE)	I.C. programmed
--	09-W4659B10	Socket, I.C., SIL, 10-pin (2 req'd) (used at U99)
U100	51NW9615N32	I.C. 74F164PC
U101	51NW9615C30	I.C. SN74LS193N
U102	(NOTE)	I.C. programmed
--	09-W4659B10	Socket, I.C., SIL, 10-pin (2 req'd) (used at U102)
U103,U105	51NW9615C69	I.C. SN74LS138N

TABLE 5-4. MVME117 Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
VR1	48NW9608A47	Zener diode, 1N4685, 3.6 Vdc + 5%, DO204 package
Y1	48AW1015B13	Crystal oscillator, 40 MHz + 0.01%
Y2	48AW1015B07	Crystal oscillator, 16.0 MHz + 0.01%
Y3	48NW9606A55	Quartz crystal, 32.768 kHz + 0.002%
--	64-W4896B01	Panel, front

NOTE: When ordering, use number labeled on part.

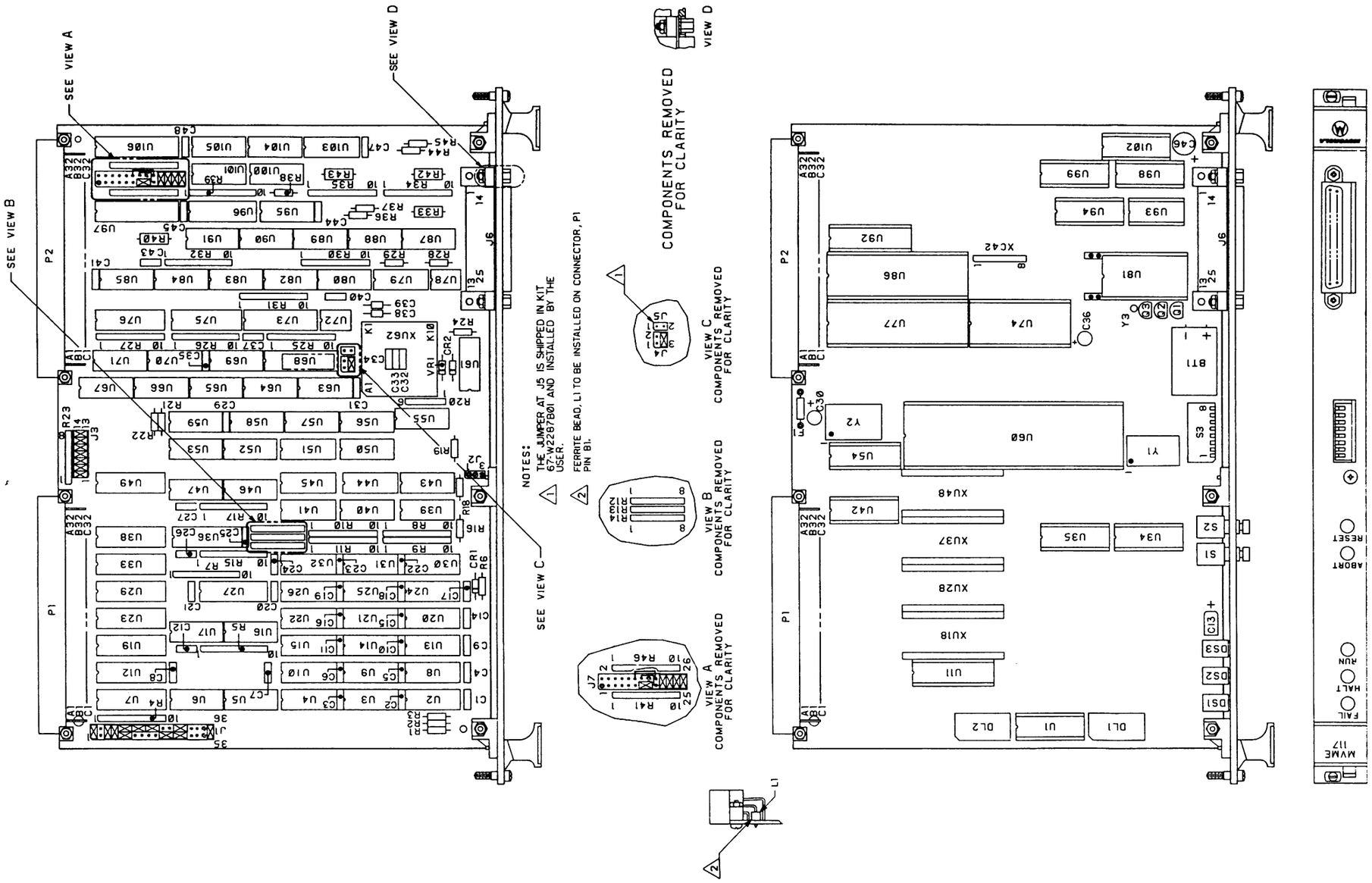


FIGURE 5-1. MVME117 Module Parts Location

SCHEMATIC DIAGRAM

The schematic diagram for the MVME117 module is illustrated in Figure 5-2.

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3393B01.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   [] DENOTES - ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING, FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:

   SHEET — 6 A6 — ZONE

9. PARTS LOCATED AT U79 AND U80 ARE GROUNDED TO [CG] (CMOS GROUND).
10. THE JUMPER AT J5 IS SHIPPED IN KIT 67-W2287B01 AND INSTALLED BY THE USER.

Y3	
VR1	
XU81	XU1-17,19-27 29-36,38-47 49-61,63-80
XC42	XC1-XC41
U106	U18,28,37 48,62,81
S3	
R46	
Q3	
P2	
J7	
F1	
DS3	
CR2	
C49	C42
BT1	
HIGHEST NUMBER USED	NOT USED

REFERENCE DESIGNATIONS

TABLE 1 ⚠4

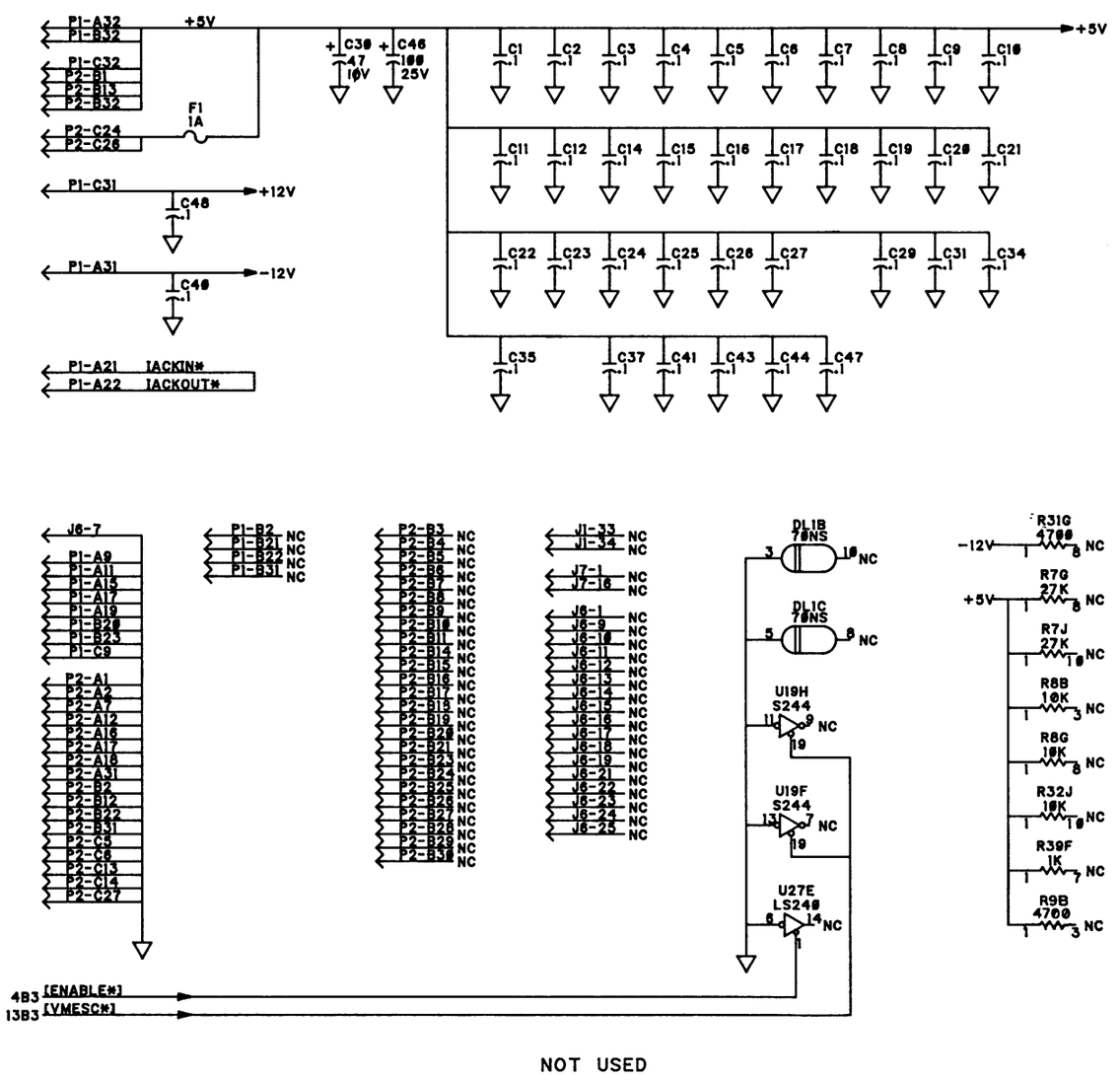
REF DES	TYPE ⚠4	GND	+5V	SH
DL1	70NS	7	14	2,11
DL2	40NS	7	14	10,11
U1	PAL16L8A	10	20	10
U2	MCM6256	16	8	8
U3	MCM6256	16	8	8
U4	MCM6256	16	8	8
U5	74F74	7	14	11
U6	74S38	7	14	9,11
U7	74ALS645-1	10	20	10
U8	MCM6256	16	8	8
U9	MCM6256	16	8	8
U10	MCM6256	16	8	8
U11	PAL20L8A	12	24	11
U12	74ALS645-1	10	20	10
U13	MCM6256	16	8	8
U14	MCM6256	16	8	8
U15	MCM6256	16	8	8
U16	74F74	7	14	9,11
U17	74F20	7	14	6,11
U19	74S244	10	20	10,11,13
U20	MCM6256	16	8	8
U21	MCM6256	16	8	8
U22	MCM6256	16	8	8
U23	74S244	10	20	9
U24	MCM6256	16	8	8
U25	MCM6256	16	8	8
U26	MCM6256	16	8	8
U27	74LS240	10	20	4,10,11,13,16,18
U29	74S244	10	20	10
U30	MCM6256	16	8	8
U31	MCM6256	16	8	8
U32	MCM6256	16	8	8
U33	74S244	10	20	10
U34	PAL16L8	10	20	7
U35	PAL16R8	10	20	8
U36	74S244	10	20	4,6,10,11,12,13
U38	74S244	10	20	10
U39	74F32	7	14	7,10
U40	74F04	7	14	4
U41	74F257	8	16	8
U42	82S153A	10	20	12
U43	74F74	7	14	7
U44	74F163	8	16	4
U45	74F257	8	16	8
U46	74F02	7	14	6,7,11
U47	74LS08	7	14	11,12,17
U49	74F373	10	20	12
U50	74F08	7	14	4,5,6,15
U51	74F257	8	16	8
U52	74F280	7	14	9
U53	74F280	7	14	9
U54	82S153A	10	20	12
U55	74S38	7	14	4
U56	74F74	7	14	7
U57	74F74	7	14	5,7
U58	74F02	7	14	7,9
U59	74F00	7	14	2,7,9
U60	MC68010	53	14	4
U60	MC68010	16	49	4
U61	74F74	7	14	6

TABLE 1 CONT ⚠4

REF DES	TYPE ⚠4	GND	[CG]	+5V	+12V	-12V	SH
U63	74S05	7		14			4,9
U64	74F20	7		14			13
U65	74F64	7		14			13
U66	74F32	7		14			6,7,9,13
U67	74LS00	7		14			5,12,13
U68	74LS244	10		20			13
U69	74F00	7		14			4,5,6,16
U70	74S38	7		14			4,6,12,16
U71	74F10	7		14			5,10,12
U72	MC3486	4			8	5	15
U73	74LS244	10		20			13
U74	MC68B40	1		14			12
U75	74LS794	10		20			13
U76	74ALS645	10		20			13
U77	NCR5380	11		31			16
U78	ICL8212	5		8			18
U79	MM58274		8	16			18
U80	74HC32		7	14			18
U82	MC1489A	7		14			15
U83	MC1489A	7		14			15
U84	MC1488	7			14	1	15
U85	74LS393	7		14			6
U86	Z8530	31		9			15
U87	74F08	7		14			6,13,15
U88	74F74	7		14			6
U89	74F74	7		14			6
U90	74F04	7		14			4,5,8,9,19
U91	74LS14	7		14			4,13,17
U92	PAL20L10	12		24			17
U93	82S123	8		16			12
U94	82S153A	10		20			5
U95	74F74	7		14			4
U96	74LS794	10		20			17
U97	74ALS652	12		24			17
U98	PAL16L8B	10		20			5
U99	PAL16L8A	10		20			5
U100	74F164	7		14			5
U101	74LS193	8		16			6
U102	PAL16R4A	10		20			5
U103	74LS138	8		16			5
U104	74F10	7		14			6
U105	74LS138	8		16			5
U106	74ALS652	12		24			17
XU18	SOCKET						14
XU28	SOCKET						14
XU37	SOCKET						14
XU48	SOCKET						14
XU62	MC68881	B7		B8			19
XU62	MC68881	J8		E2			19
XU62	MC68881	C3		E9			19
XU62	MC68881	E10		H8			19
XU81	SOCKET						18
Y1	K1100A	7		14			4
Y2	K1148	7		14			13

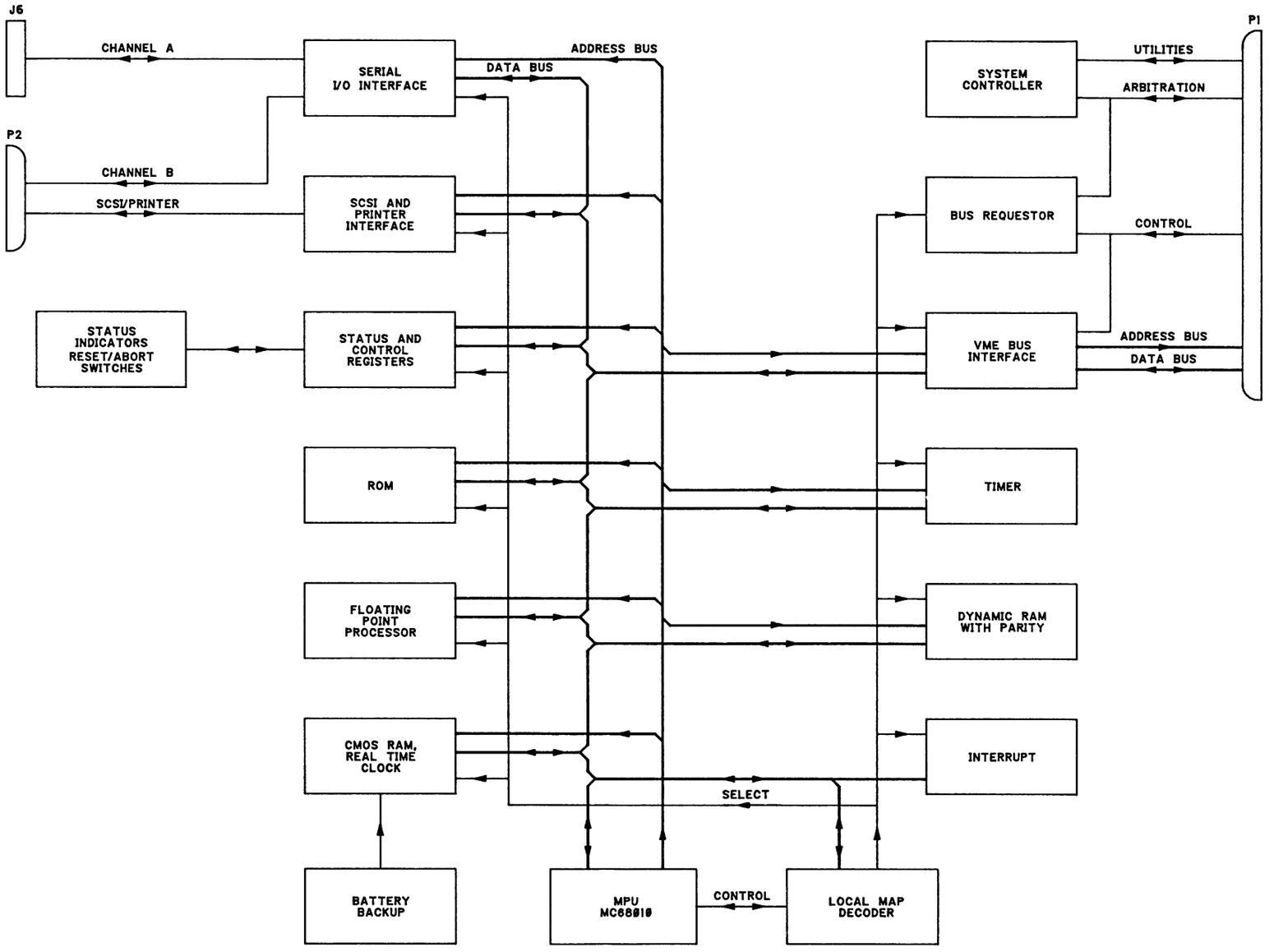
63DW3393B REV H SH 1 OF 19

FIGURE 5-2. MVME117 Schematic Diagram 5-27/5-28



63DW3393B REV F SH 2 OF 19

FIGURE 5-2. MVME117 Schematic Diagram 5-29/5-30



BLOCK DIAGRAM
63DW3393B REV C SH 3 OF 19

FIGURE 5-2. MVME117 Schematic Diagram

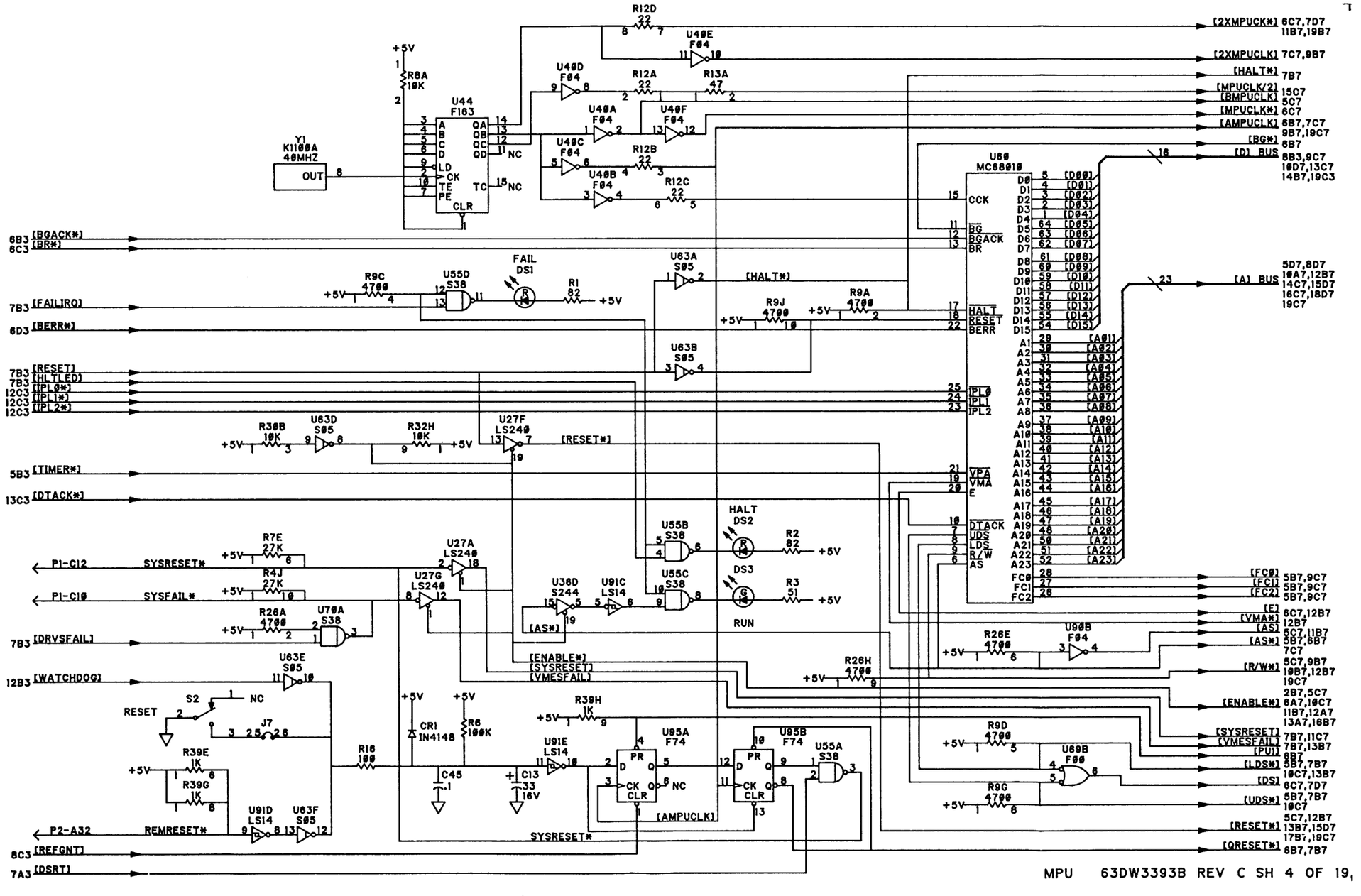


FIGURE 5-2. MVME117 Schematic Diagram

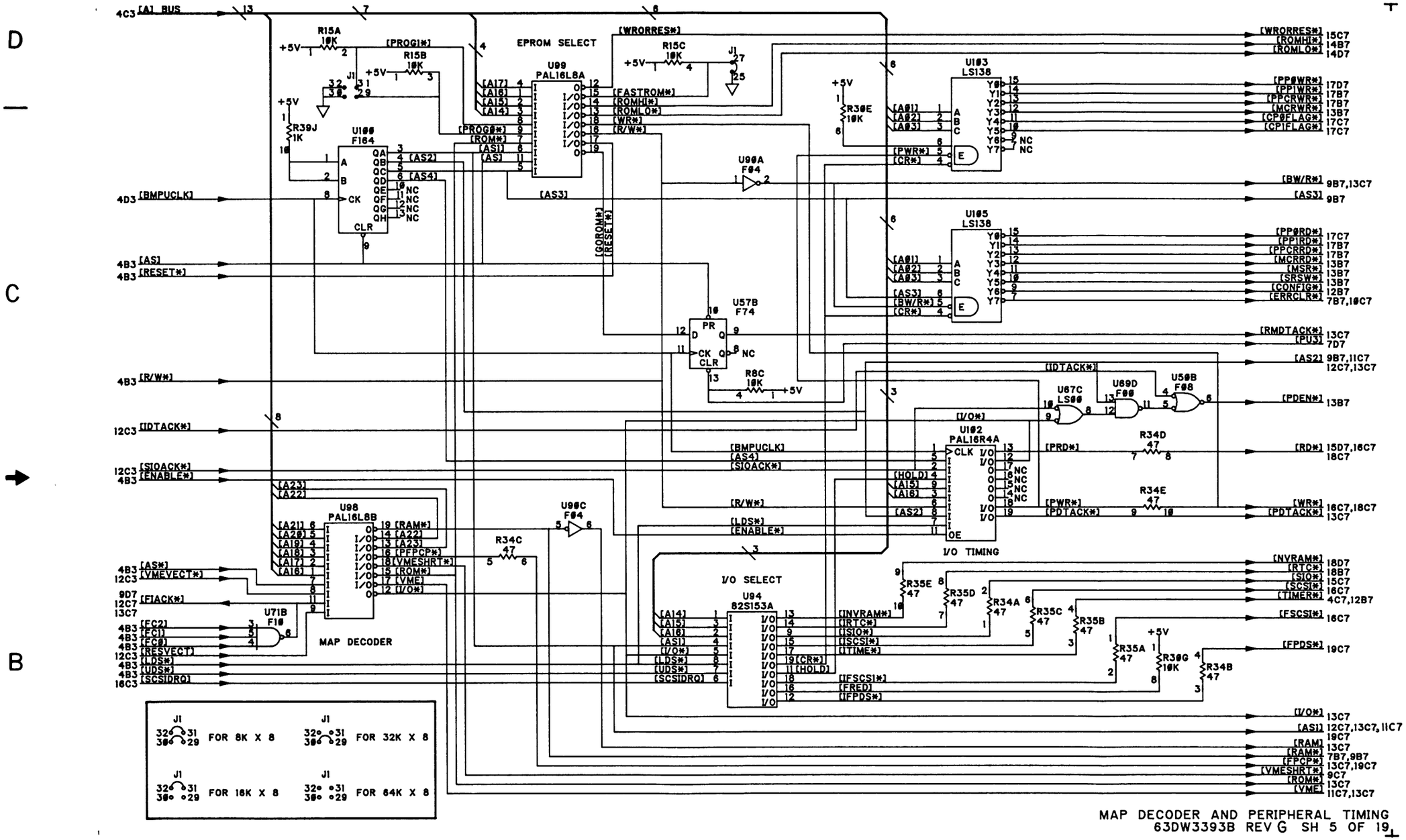
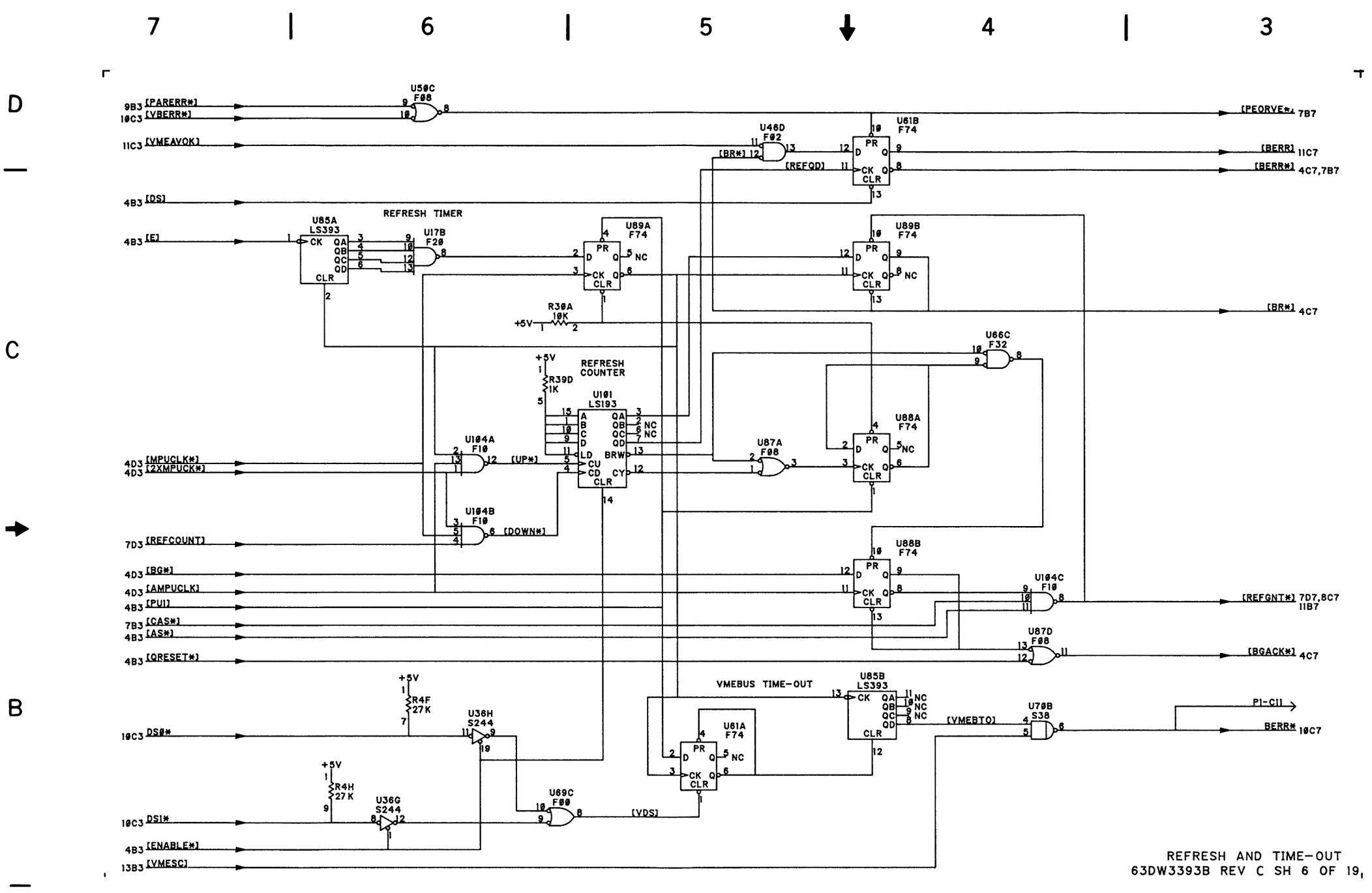


FIGURE 5-2. MVME117 Schematic Diagram 5-35/5-36



REFRESH AND TIME-OUT
63DW3393B REV C SH 6 OF 19

FIGURE 5-2. MVME117 Schematic Diagram 5-37/5-38

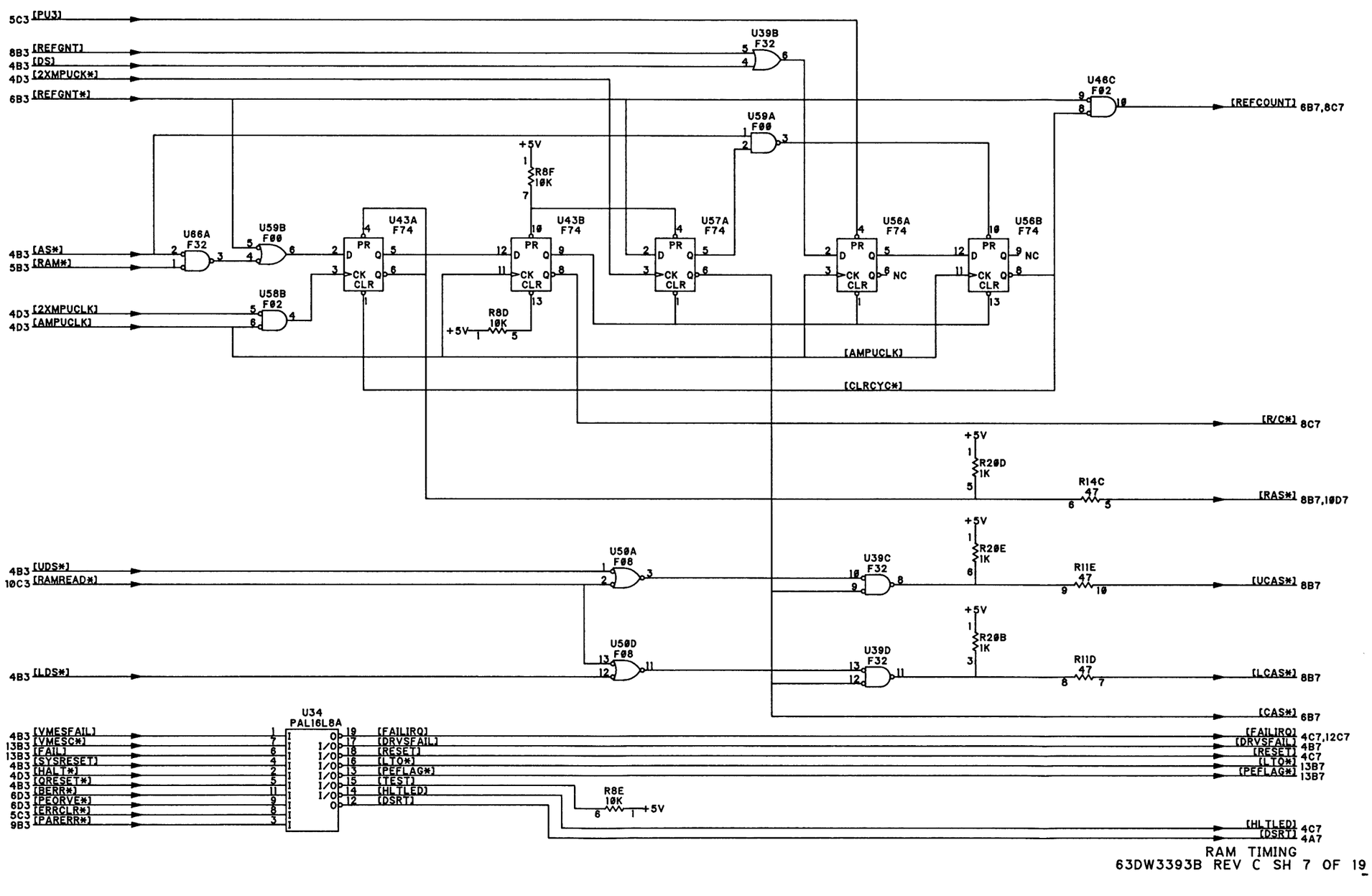


FIGURE 5-2. MVME117 Schematic Diagram

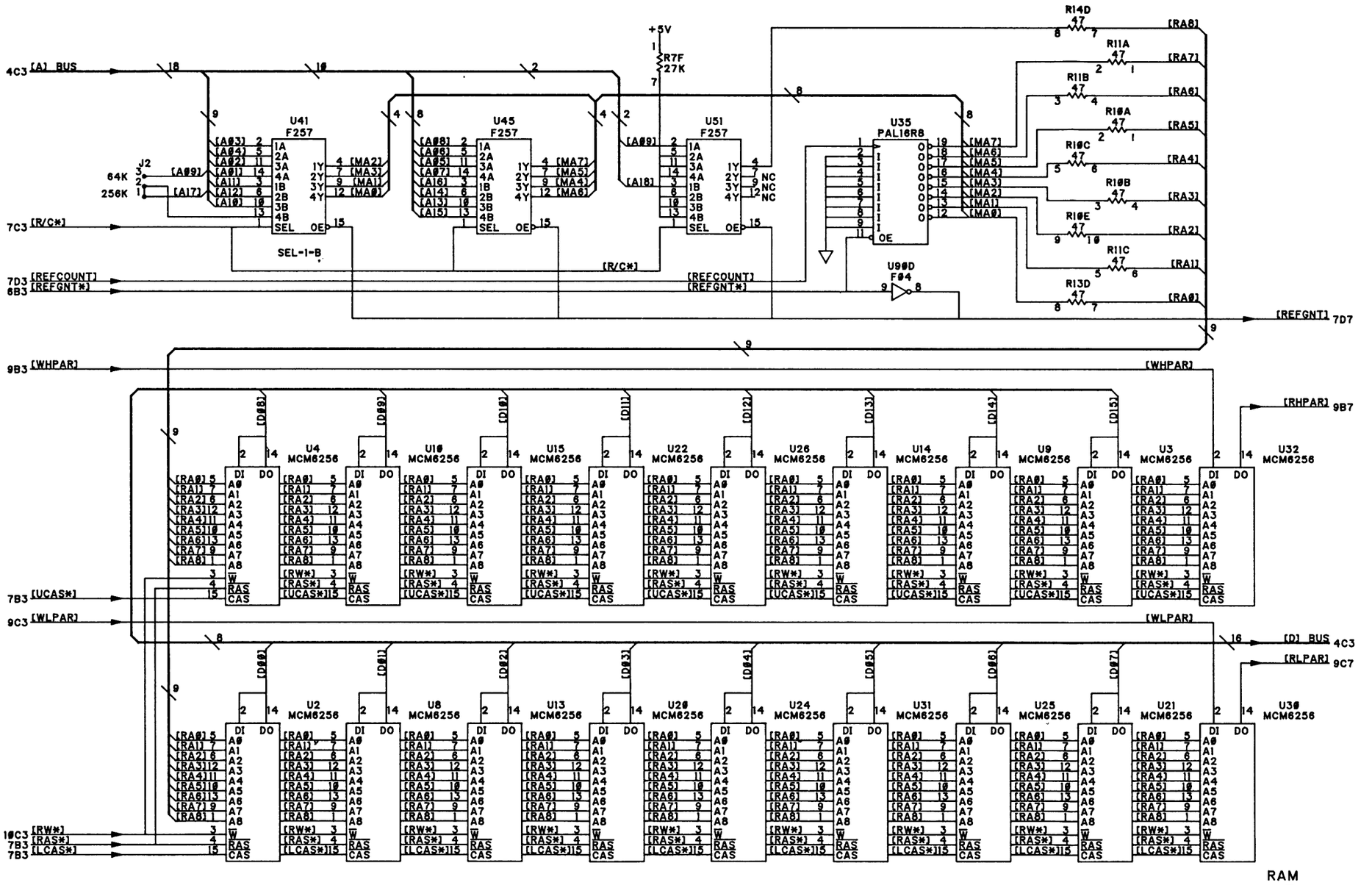
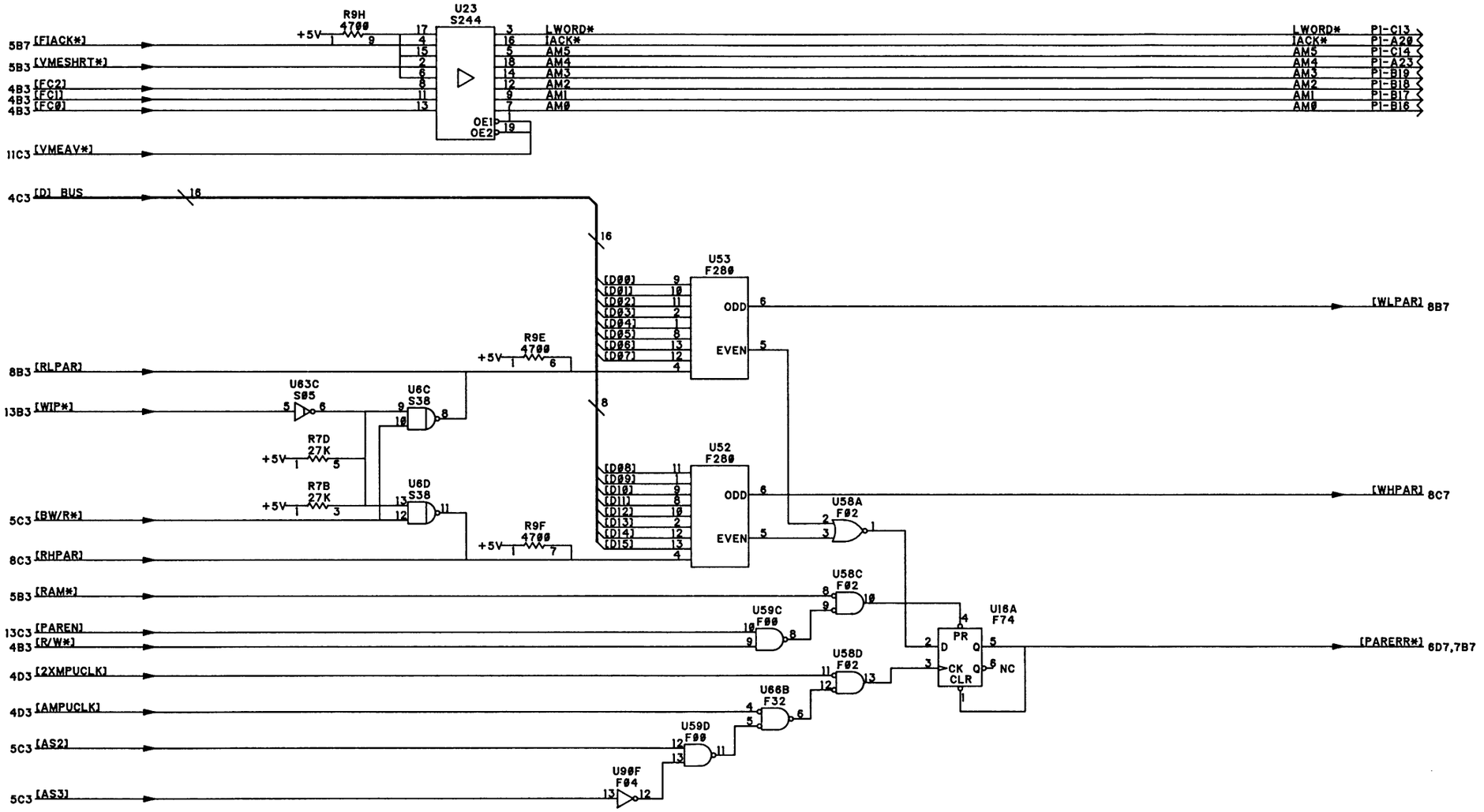


FIGURE 5-2. MVME117 Schematic Diagram



PARITY
63DW3393B REV C SH 9 OF 19

FIGURE 5-2. MVME117 Schematic Diagram 5-43/5-44

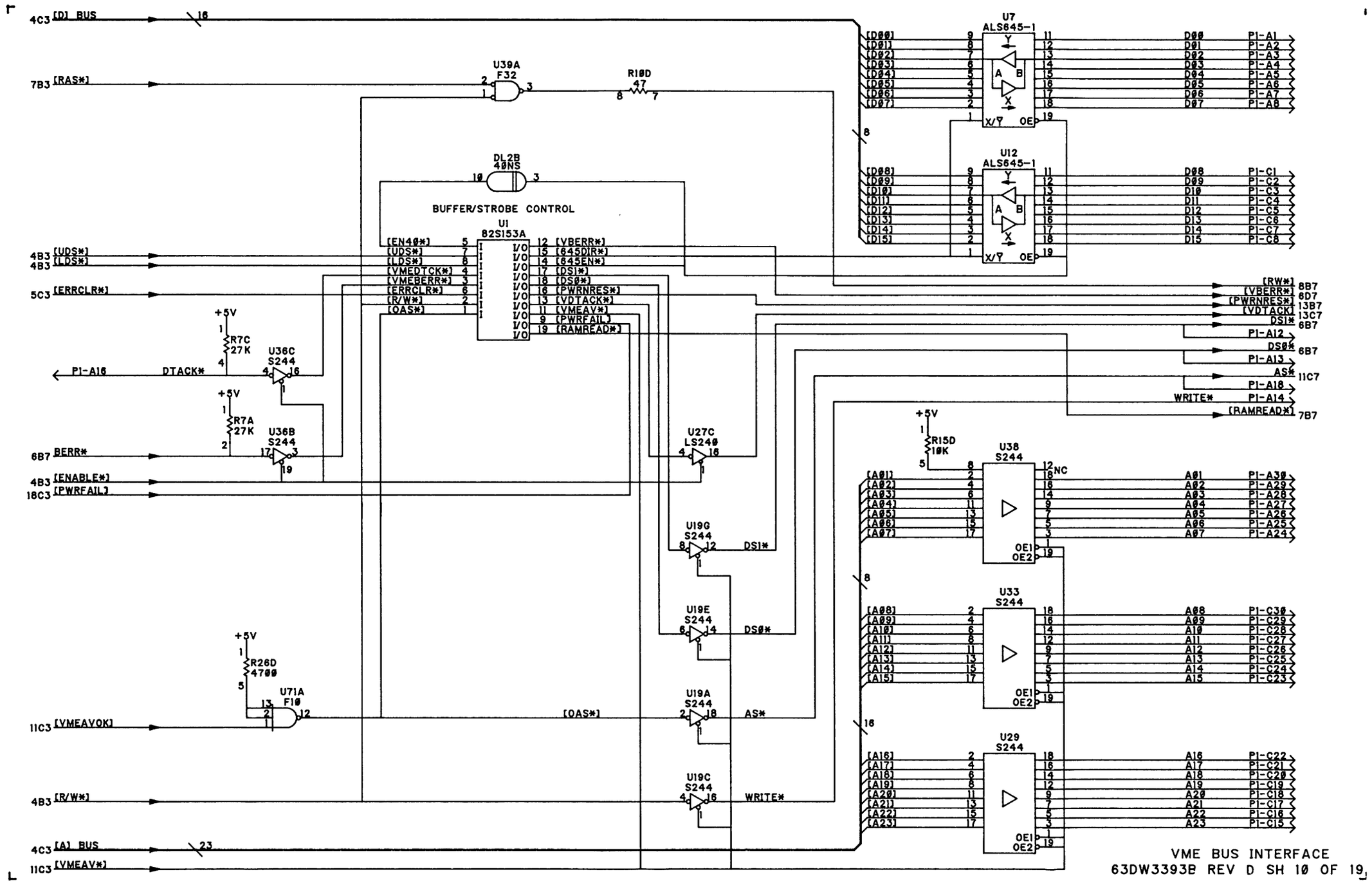


FIGURE 5-2. MVME117 Schematic Diagram

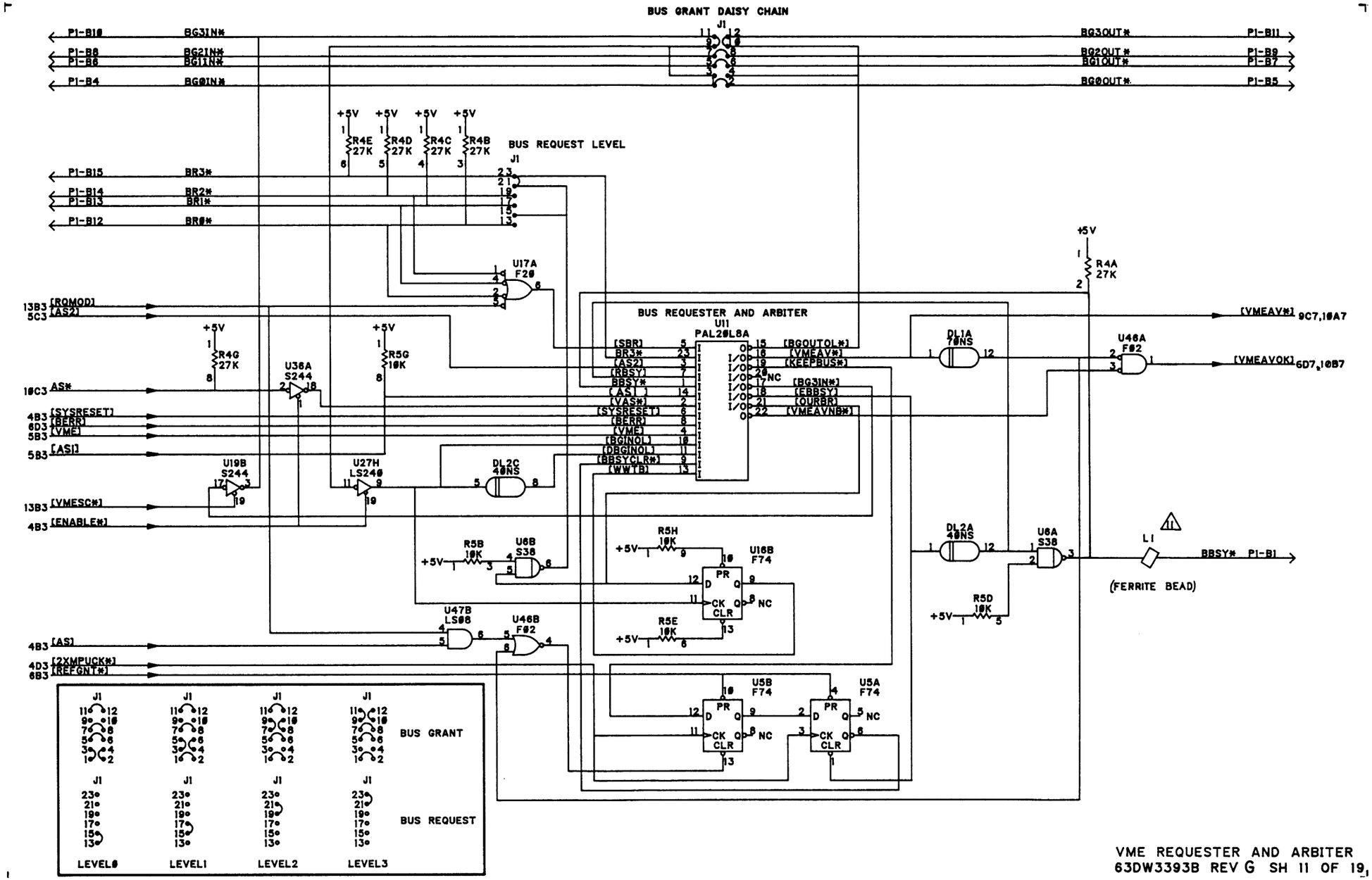
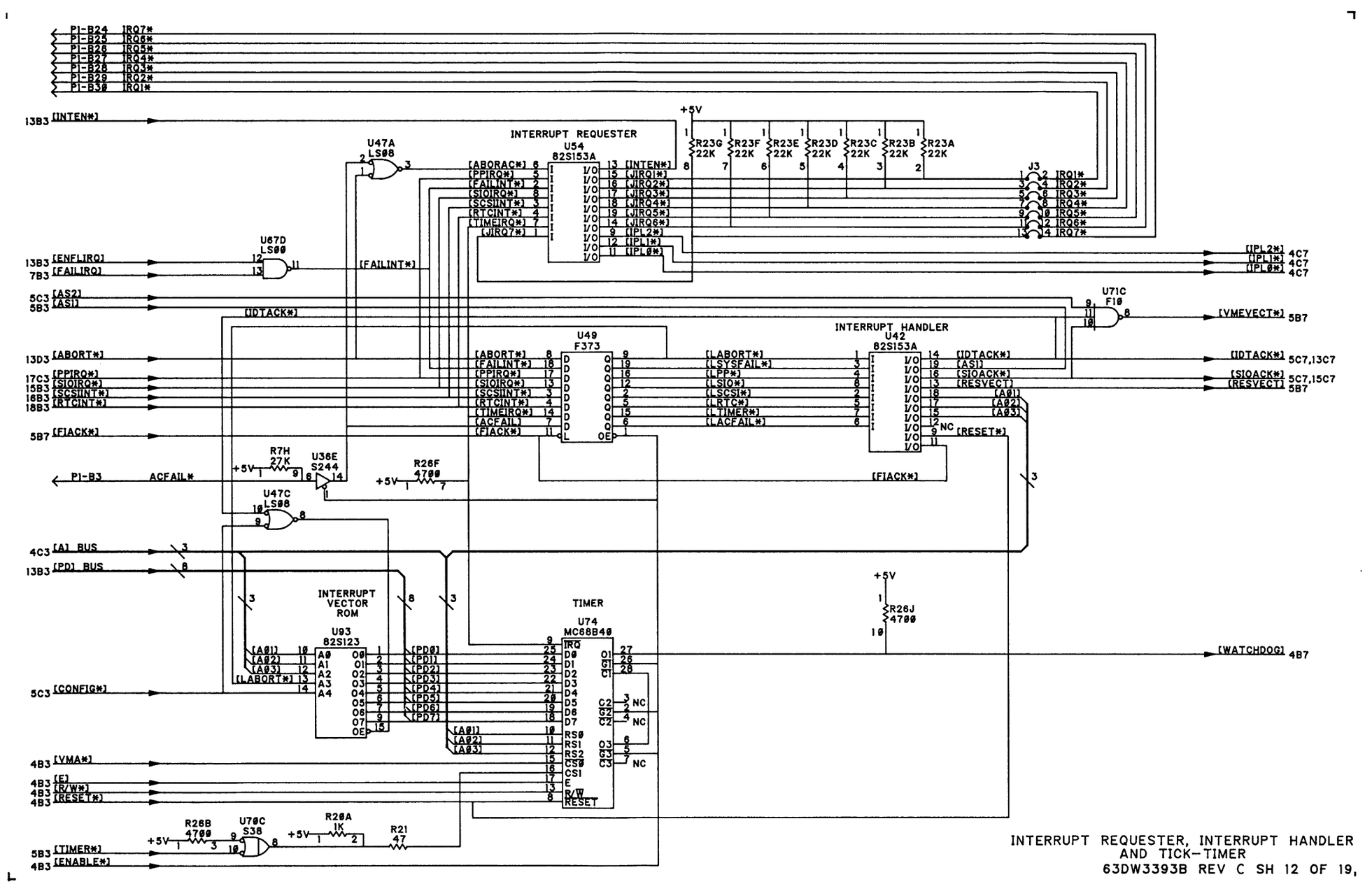


FIGURE 5-2. MVME117 Schematic Diagram



INTERRUPT REQUESTER, INTERRUPT HANDLER AND TICK-TIMER
63DW3393B REV C SH 12 OF 19,

FIGURE 5-2. MVME117 Schematic Diagram 5-49/5-50

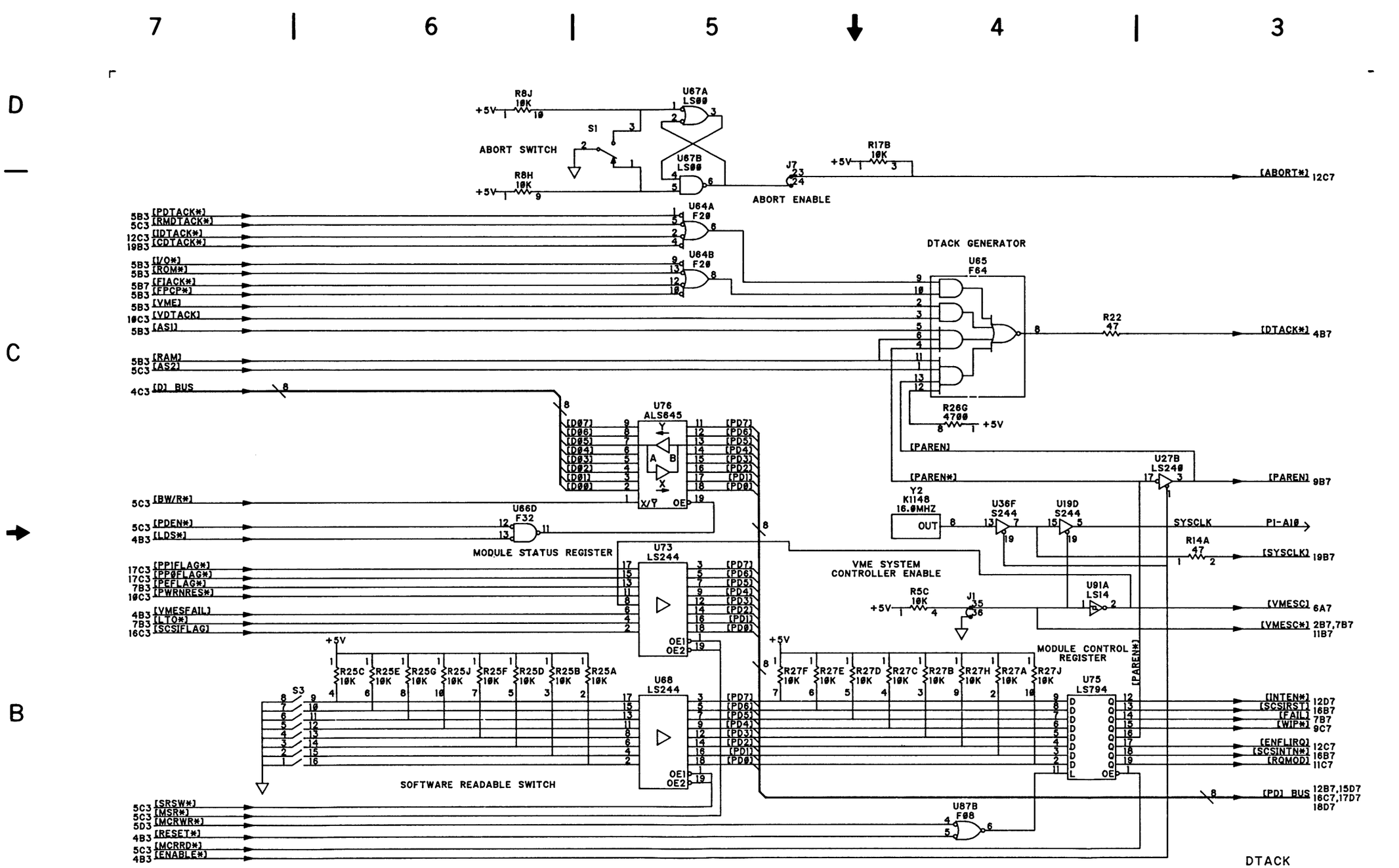


FIGURE 5-2. MVME117 Schematic Diagram 5-51/5-52

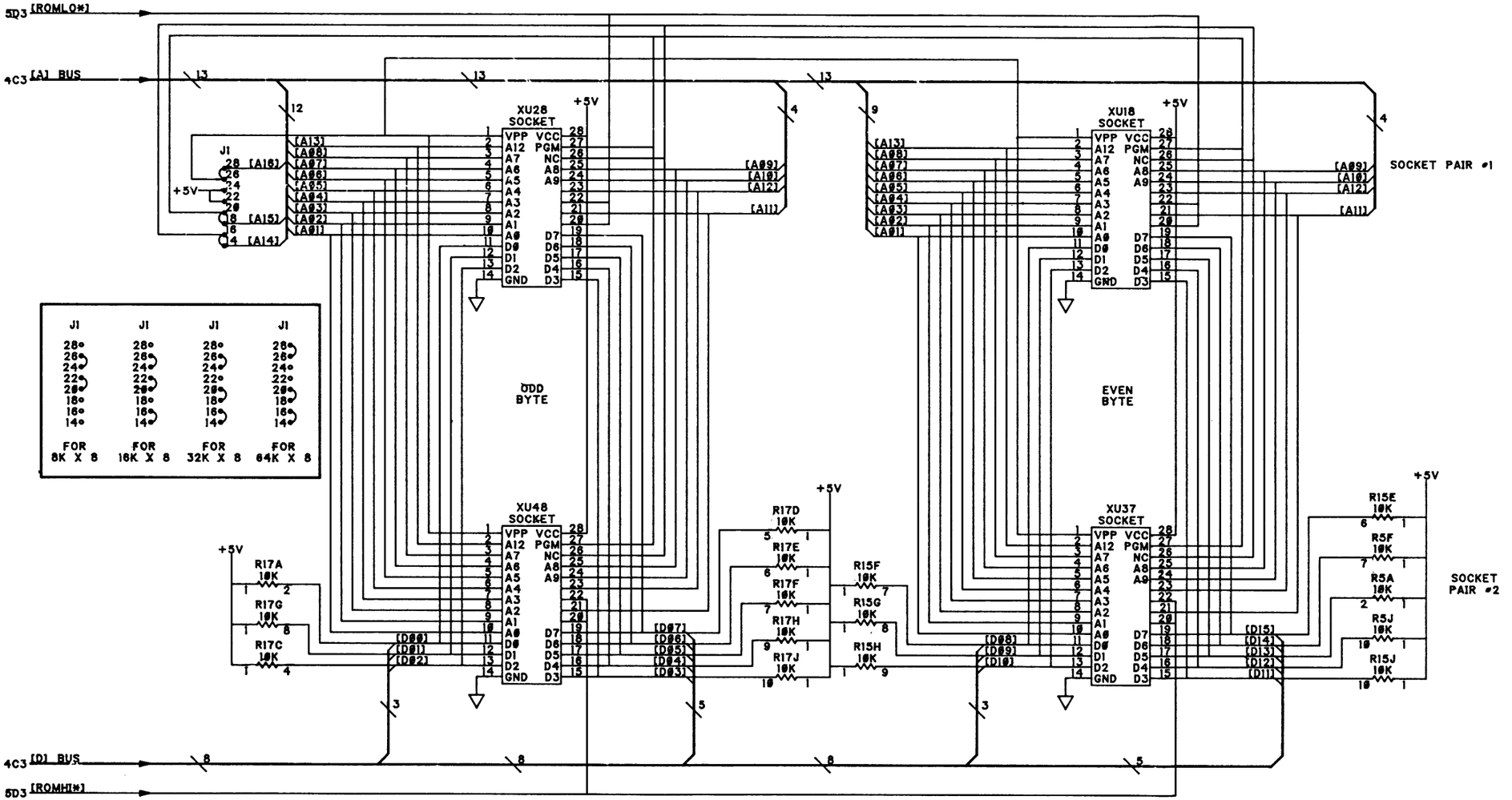


FIGURE 5-2. MVME117 Schematic Diagram 5-53/5-54

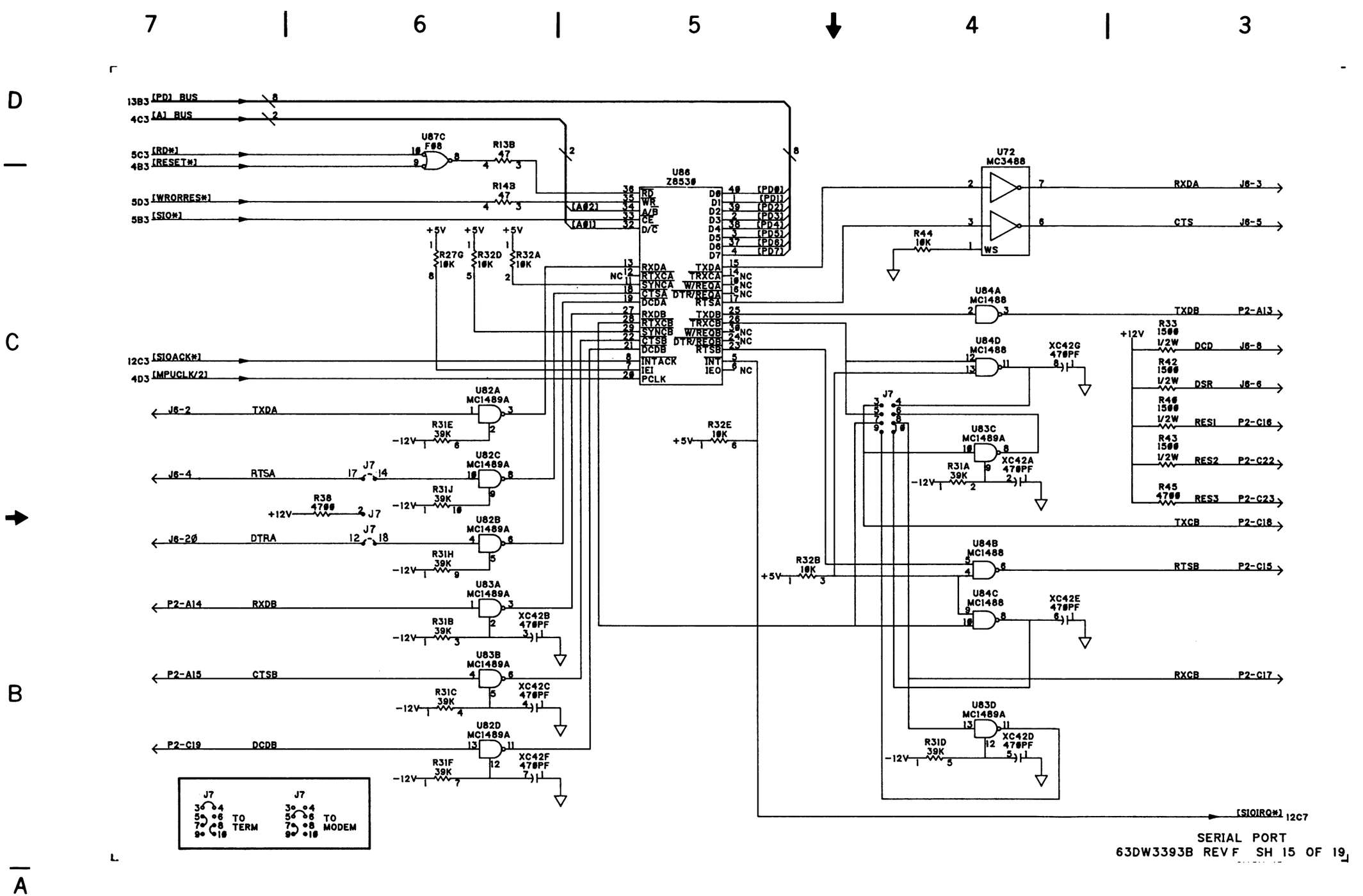
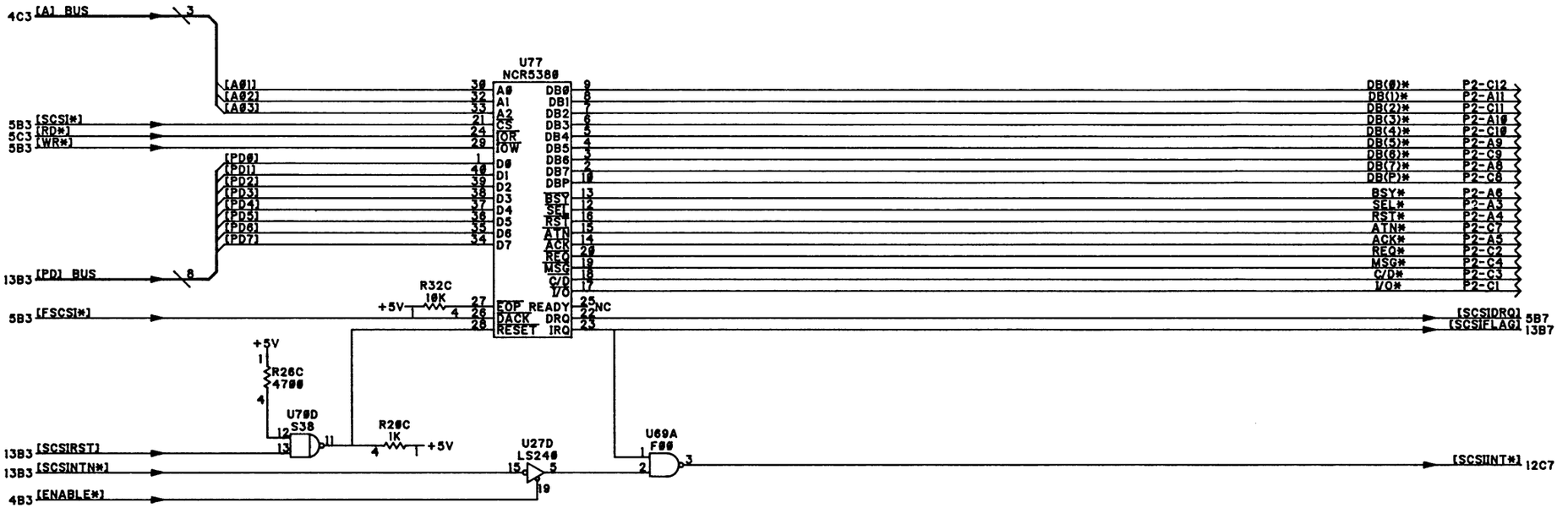


FIGURE 5-2. MVME117 Schematic Diagram 5-55/5-56



SCSI CONTROLLER
63DW3393B REV A SH 16 OF 19

FIGURE 5-2. MVME117 Schematic Diagram 5-57/5-58

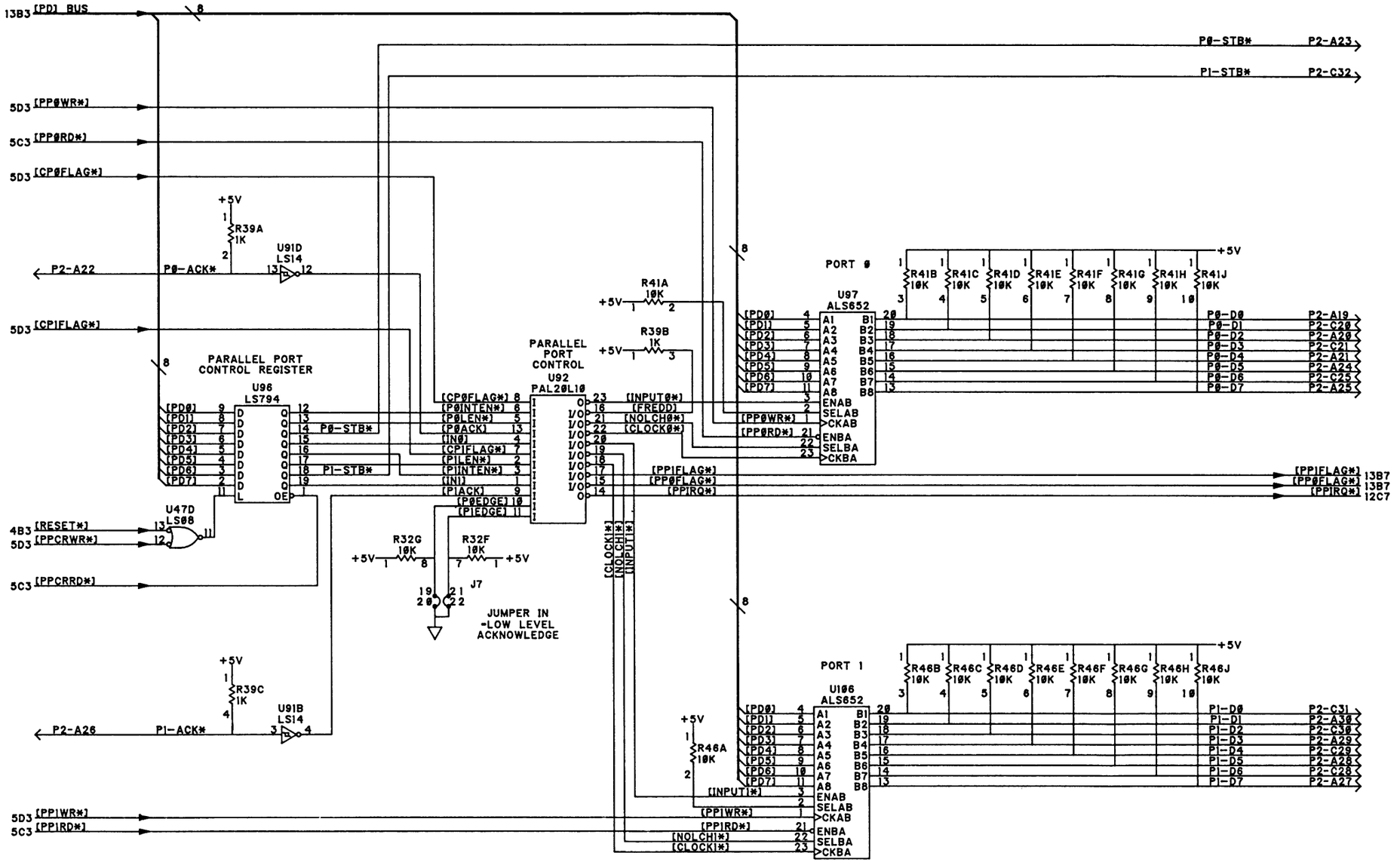


FIGURE 5-2. MVME117 Schematic Diagram 5-59/5-60

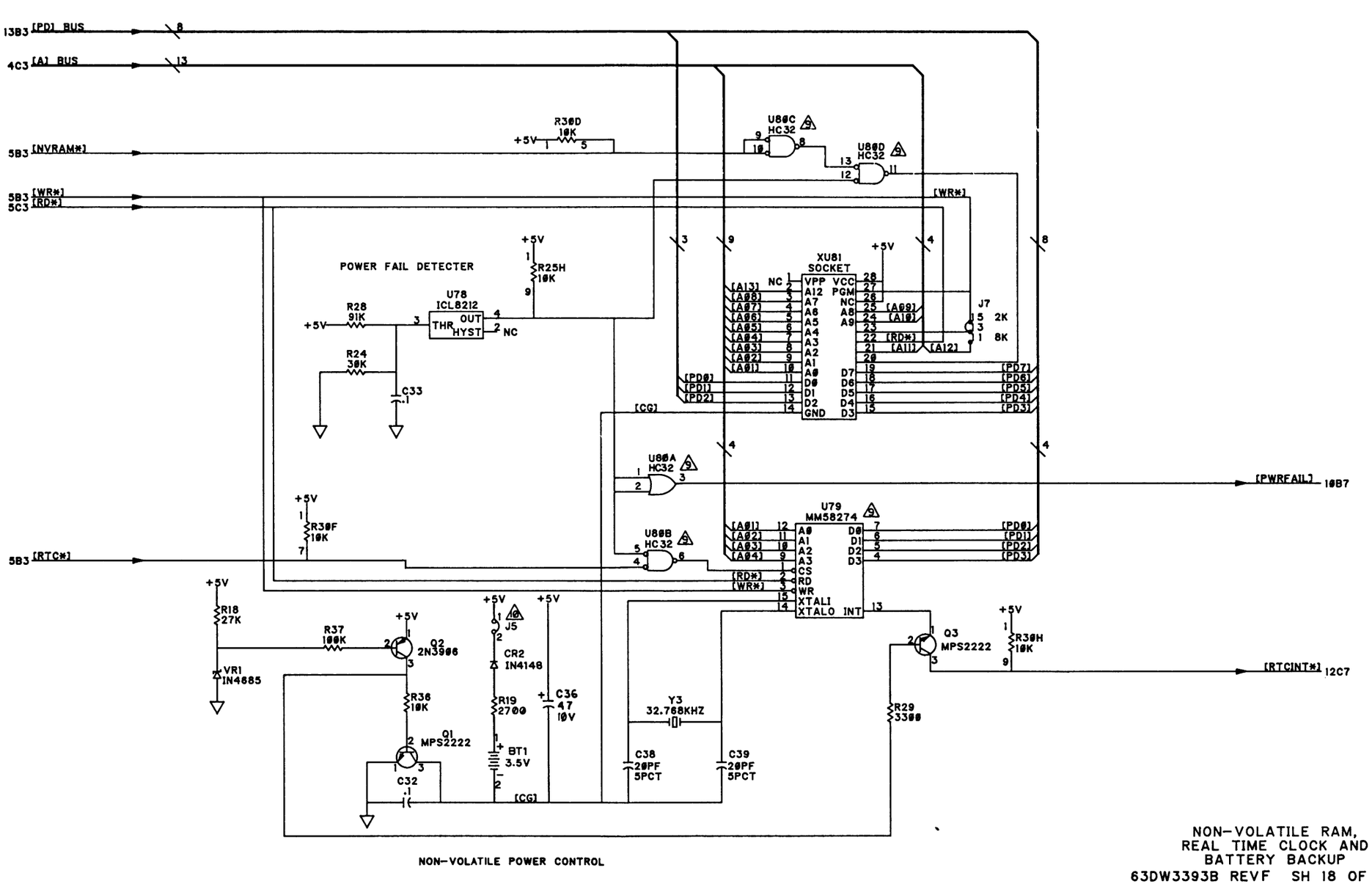
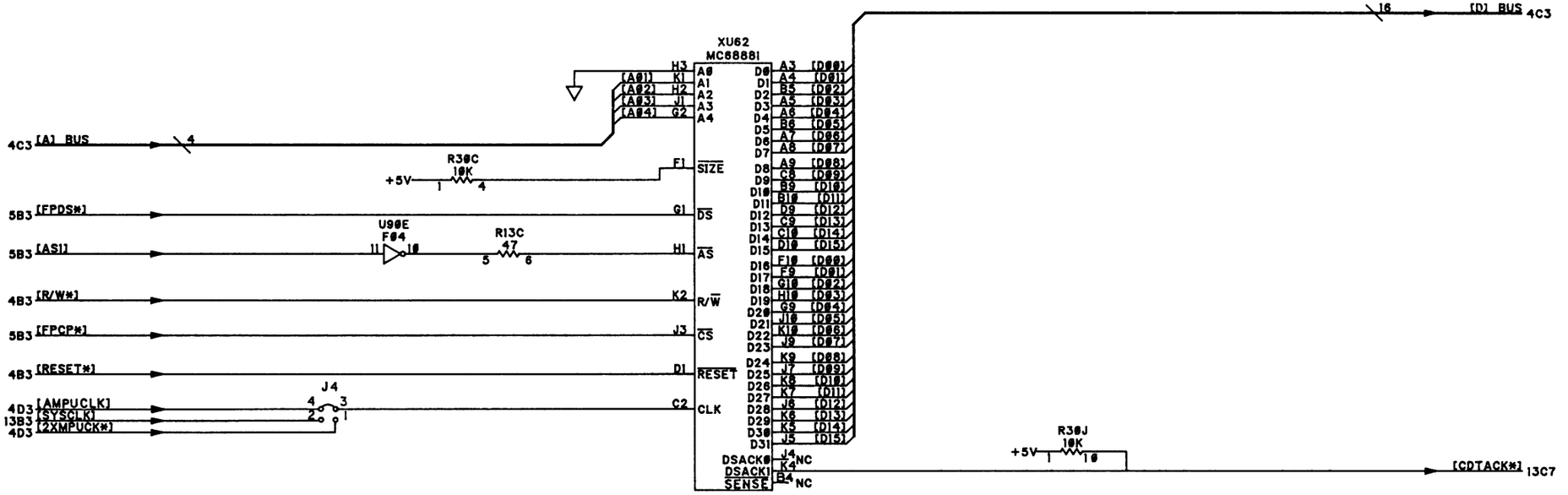
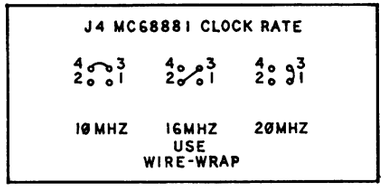


FIGURE 5-2. MVME117 Schematic Diagram





FLOATING POINT PROCESSOR
(PERIPHERAL)
63DW3393B REV F SH 19 OF 19

FIGURE 5-2. MVME117 Schematic Diagram 5-63/5-64

APPENDIX A – RS-232C INTERCONNECTIONS

The RS-232C standard is the most widely used interface between terminals and computers or modems, and yet it is not fully understood. This is because all the lines are not clearly defined, and many users do not see the need to conform for their applications. A system should easily connect to any other. Many times designers think only of their own equipment, but the state-of-the-art is computer-to-computer or computer-to-modem operation.

The RS-232C standard was originally developed by the Bell System to connect terminals via modems. Therefore, several handshaking lines were included. In many applications these are not needed, but since they permit diagnosis of problems, they are included in many applications.

The standard RS-232C interconnections are listed in Table To interpret this information correctly it is necessary to know that RS-232C is intended to connect a terminal to a modem. When computers are connected to computers without modems, one of them must be configured as a terminal and the other as a modem. Because computers are normally configured to work with terminals, they are said to be configured as a modem. Also, the signal levels must be between +3 and +15 volts for a high level, and between -3 and -15 volts for a low level. Any attempt to connect units in parallel may result in out of range voltages and is not allowed by the RS-232C specification.

TABLE A-1. RS-232C Interconnections

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1		Not used.
2	TxD	TRANSMIT DATA - data to be transmitted is furnished on this line to the modem from the terminal.
3	RxD	RECEIVE DATA - data which is demodulated from the receive line is presented to the terminal by the modem.

TABLE A-1. RS-232C Interconnections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
4	RTS	REQUEST TO SEND - RTS is supplied by the terminal to the modem when required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.
5	CTS	CLEAR TO SEND - CTS is a function supplied to the terminal by the modem which indicates that it is permissible to begin transmission of a message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
6	DSR	DATA SET READY - data set ready is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
7	SIG-GND	SIGNAL GROUND - common return line for all signals at the modem interface.
8	DCD	DATA CARRIER DETECT - sent by the modem to the terminal to indicate that a valid carrier is being received.
9-14		Not used.
15	TxC	TRANSMIT CLOCK - this line clocks output data to the modem from the terminal.
16		Not used.
17	RxC	RECEIVE CLOCK - this line clocks input data from a terminal to a modem.
18,19		Not used.
20	DTR	DATA TERMINAL READY - a signal from the terminal to the modem indicating that the terminal is ready to send or receive data.

TABLE A-1. RS-232C Interconnections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
21		Not used.
22	RI	RING INDICATOR - RI is sent by the modem to the terminal. This line indicates to the terminal that an incoming call is present. The terminal causes the modem to answer the phone by carrying DTR true while RI is active.
23		Not used.
24	TxC	TRANSMIT CLOCK - Same as TxC on pin 15.
25	BSY	BUSY - A positive EIA signal applied to this pin causes the modem to go off-hook and make the associated phone busy.

NOTES: 1. High level = +3 to +15 volts. Low level = -3 to -15 volts.
2. RS-232C is intended to connect a terminal to a modem. When computers are connected to computers without modems, one of the computers must be configured as a modem and the other as a terminal.

There are several levels of conformance that are appropriate for typical RS-232C interconnections. The bare minimum requirement is the two data lines and a ground . The full version of RS-232C requires 12 lines and accommodates automatic dialing, automatic answering, and synchronous transmission. A middle-of-the-road approach is illustrated in Figure A-1.

One set of handshaking signals frequently implemented are RTS and CTS. CTS is used in many systems to inhibit transmission until the signal is high. In the modem application, RTS is turned around and returned as CTS after 150 microseconds. RTS is programmable in some systems to work with the older type 202 modem (half duplex). CTS is used in some systems to provide flow control to avoid buffer overflow. This is not possible if modems are used. It is usually necessary to make CTS high by connecting it to RTS or to some source of +12 volts such as the resistors shown in Figure A-1. It is also frequently

jumpered to an MC1488 gate which has its inputs grounded (the gate is provided for this purpose). Another signal used in many systems is DCD. The original purpose of this signal was to tell the system that the carrier tone from the distant modem was being received. This signal is frequently used by the software to display a message like CARRIER NOT PRESENT to help the user to diagnose failure to communicate. Obviously, if the system is designed properly to use this signal, and it is not connected to a modem, the signal must be provided by a pullup resistor or gate as described before (see Figure A-1). Many modems expect a DTR high signal and issue a DSR. These signals are used by software to help prompt the operator about possible causes of trouble. The DTR signal is used sometimes to disconnect the phone circuit in preparation for another automatic call. It is necessary to provide these signals in order to talk to all possible modems (see Figure A-1). Figure A-2 is a good minimum configuration that almost always works. If the CTS and DCD signals are not received from the modem, the jumpers can be moved to artificially provide the needed signal. A way that an RS-232C connector can be wired to enable a computer to connect to a basic terminal with only three wires is shown in Figure A-2. This is because most terminals have a DTR signal that is ON, and that can be used to pullup the CTS, DCD, and DSR signals. Two of these connectors wired back-to-back can be used. It must be realized that all the handshaking has been bypassed and possible diagnostic messages do not occur. Also the Tx and Rx lines may have to be crossed since Tx from a terminal is outgoing but the Tx line on a modem is an incoming signal.

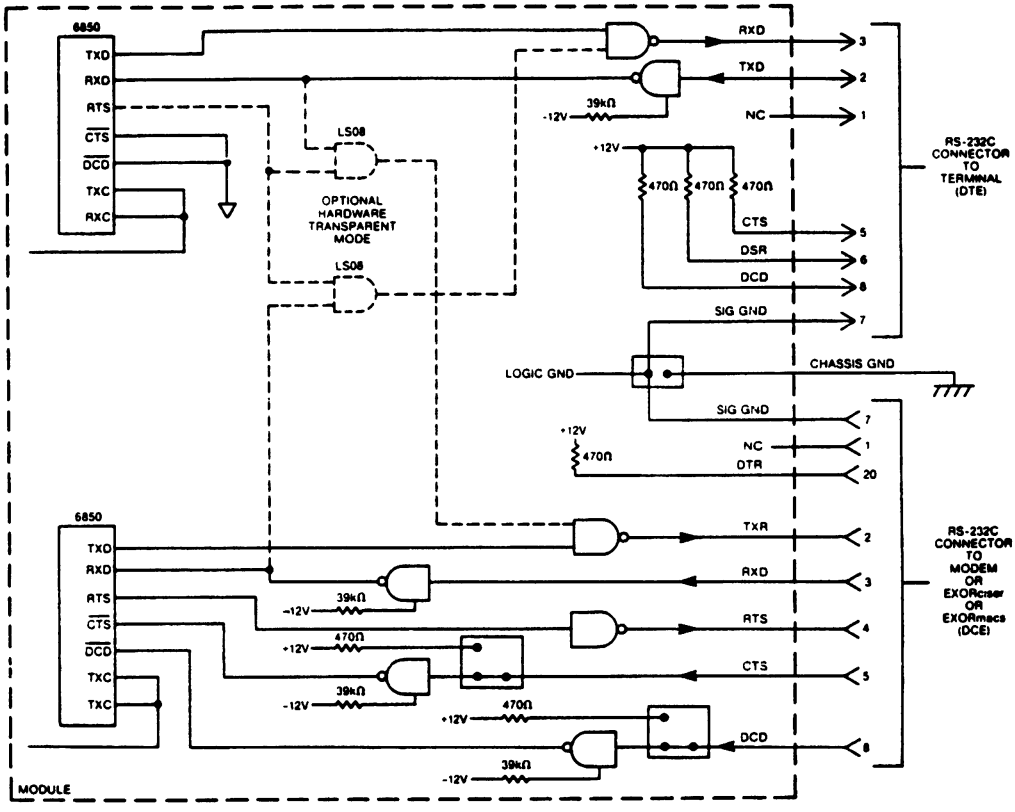


FIGURE A-1. Middle-of-the-Road RS-232C Configuration

Another subject that needs to be considered is the use of ground pins. There are two pins labeled GND. Pin 7 is the SIGNAL GROUND and must be connected to the distant device to complete the circuit. Pin 1 is the CHASSIS GROUND, but it must be used with care. The chassis is connected to the power ground through the green wire in the power cord and must be connected to the chassis to be in compliance with the electrical code. The problem is that when units are connected to different electrical outlets, there may be several volts difference in ground potential. If pin 1 of the devices are interconnected with a cable, several amperes of current could result. This not only may be dangerous for the small wires in a typical cable, but could result in electrical noise that could cause errors. That is the reason that Figure A-1 shows no connection for pin 1. Normally, pin 7 should only be connected to the CHASSIS GROUND at one point, and if several terminals are

used with one computer, the logical place for that point is at the computer. The terminals should not have a connection between the logic ground return and the chassis.

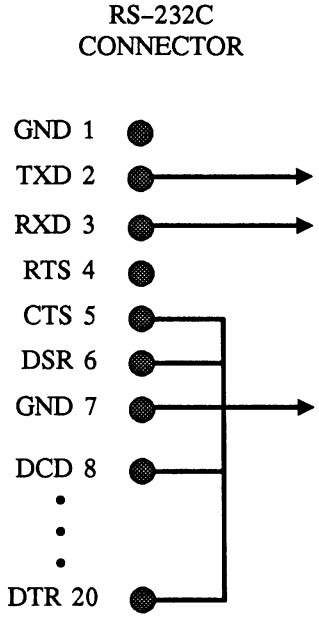


FIGURE A-2. Minimum RS-232C Connection

APPENDIX B – INTERRUPT VECTOR AND CONFIGURATION NUMBER PROM U93

This PROM is made from an 83S123 and contains the code for the interrupt vectors and the configuration number. Users may program their own PROM with different vectors.

The configuration number in location E is the number given as "bit pattern" in this appendix, and must be correct for the model of the MVME117 module used. Refer to the *Module Configuration Number* paragraph in Chapter 4. The example shown below is pattern 02 for "module part number" B03, which is part number 01-W3393B03, for the MVME117-3.

U93

51AW1086X17

ADDRESS	CONTENTS	ADDRESS	CONTENTS
0	UNUSED	10	BREAKPOINT VECTOR (DC)
1	UNUSED	11	SYSFAIL VECTOR (45)
2	UNUSED	12	SCSI VECTOR (44)
3	UNUSED	13	REAL-TIME-CLOCK VECTOR (43)
4	UNUSED	14	PARALLEL PORT VECTOR (42)
5	UNUSED	15	TICK-TIMER VECTOR (41)
6	UNUSED	16	UNUSED (UNPROGRAMMED)
7	UNUSED	17	ABORT VECTOR (1F)
8	UNUSED	18	BREAKPOINT VECTOR (DC)
9	UNUSED	19	SYSFAIL VECTOR (45)
A	UNUSED	1A	SCSI VECTOR (44)
B	UNUSED	1B	REAL-TIME-CLOCK VECTOR (43)
C	UNUSED	1C	PARALLEL PORT VECTOR (42)
D	UNUSED	1D	TICK-TIMER VECTOR (41)
E	CONFIGURATION NUMBER	1E	UNUSED (UNPROGRAMMED)
F	UNUSED	1F	ACFAIL VECTOR (40)

BIT PATTERN	MODULE PART NUMBER	PROGRAMMED PART NUMBER	CHECKSUM
00	B01	51AW1086X14	02FD
01	B02	51AW1086X16	02FE
02	B03	51AW1086X17	02FF
03	B04	51AW1086X18	0300
06	B07	51AW1086X19	0303

BIT MAP (XX= FACTORY DEFINABLE)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0-	00	00	00	00	00	00	00	00	00	00	00	00	00	00	XX	00
1-	00	45	44	43	42	41	00	1F	00	45	44	43	42	41	00	40

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