MVME10X/D1

MVME10X (MVME104/105/106/107) Series of Single Board Computers User's Manual

MVME10X/D1

JUNE 1987

MVME10X (MVME104/105/106/107) SERIES

OF

SINGLE BOARD COMPUTERS

USER'S MANUAL

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

First Edition

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Microsystems Warranty and Repair for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this user's manual.

An asterisk (*) following a signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following a signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the MVME1Ø4, MVME1Ø5, MVME1Ø6, and MVME1Ø7 series of 24-bit address and 16-bit data Single-Board Computers (SBC). Unless otherwise specified, these VMEmodules are referred to as the SBC units throughout this manual.

1.2 FEATURES

The features of the SBC include:

- MC68Ø1Ø (1Ø MHz) Virtual Memory Microprocessor.
- Standard VMEbus interface with 24-bit address and 16-bit data.
- 512K bytes of zero wait state DRAM shared with VMEbus.
- Memory mappable on 512K-byte boundaries (from $ØØØØØØ to $EFFFFF) on VMEbus.
- Memory mappable at either $ØØØØØØ or $E8ØØØØ locally.
- One multi-protocol serial port with multi-drop capabilities on connector P2.
- One RS-232 synchronous/asynchronous serial port on front panel.
- Parallel Input/Output Centronics printer port.
- 24-bit programmable timer.
- Local watchdog timer.
- Local bus timer.
- System controller functions, including system clock, single level arbiter, bus timer, and reset generator.
- Two on-board EPROM sockets to support 32K x 8 or 64K x 8 EPROMs (configured for Industry Standard JEDEC 28-pin devices; user-provided).
- Two on-board RAM/EPROM sockets to support either 2K x 8, 8K x 8, 32K x 8 static RAMs, 2K x 8, 8K x 8 EEPROMs, 32K x 8 or 64K x 8 EPROMs (configured for Industry Standard JEDEC 28-pin devices; user-provided). Powered by +5V or +5V standby, jumper selectable.
- Bus requester with Release-On-Request (ROR) and early release.
- Status LEDs for HALT, RUN, and FAIL on front panel.

- RESET and ABORT switches on front panel with jumper disable.
- 8-Bit software readable switch.
- 16-bit Control/Status Register (16 bits read/writable locally, 16 bits readable from VMEbus, 8 bits writable from VMEbus).
- Stand-alone operation (without chassis or backplane) with addition of power supply and terminal.
- I/O channel interface (VME1Ø4 version only).
- Disk Controller supports four 5-1/4 inch floppy disk drives (on VME1Ø6 version only).
- Full Small Computer Systems Interface (SCSI) bus interface with pseudo Direct Memory Access (DMA) capabilities (on VME1Ø7 version only).

1.3 SPECIFICATIONS

The specifications for the SBC are given in Table 1-1.

TABLE 1-1. SBC SPECIFICATIONS

Characteristic	Specification
Microprocessor	MC68Ø1Ø (refer to Motorola Publication ADI-942)
Clock signal	1Ø MHz CPU clock frequency
Power requirements:	
VME1Ø4	+5 Vdc, 4.2Ø A maximum (3.5 A typical) +12 Vdc, 5.Ø mA maximum (Ø mA typical) -12 Vdc, 8.Ø mA maximum (Ø mA typical)
VME1Ø5	+5 Vdc, 3.84 A maximum (3.2 A typical) +12 Vdc, 5.Ø mA maximum (Ø mA typical) -12 Vdc, 8.Ø mA maximum (Ø mA typical)

TABLE 1-1. SBC SPECIFICATIONS (cont.)

Characteristic	Specification
VME1Ø6	+5 Vdc, 4.2Ø A maximum (3.5 A typical) +12 Vdc, 5.Ø mA maximum (Ø mA typical) -12 Vdc, 8.Ø mA maximum (Ø mA typical)
VME1Ø7	+5 Vdc, 4.32 A maximum (3.6 A typical) +12 Vdc, 5.Ø mA maximum (Ø mA typical) -12 Vdc, 8.Ø mA maximum (Ø mA typical)
NOTE:	+12V and -12V need not be provided, unless the front panel RS-232 terminal port is used.
Addressing:	
Total on-board	24-bit addressing (shared with VMEbus)
Dynamic RAM	512K bytes, no parity, zero wait cycles, read, one wait state write.
RAM/EPROM/EEPROM	Two on-board EPROM sockets for 32K x 8 or 64K x 8 devices using +5 Vdc only (JEDEC standard 28-pin devices). Two on-board RAM/EPROM sockets for 2K x 8, 8K x 8, 32K x 8 RAMs; 2K x8 or 8k x 8 EEPROMs; or 32K x 8 or 64K x 8 EPROMs (JEDEC standard 28-pin devices). Powered by +5V or +5V standby, jumper selectable.
I/O ports:	
Serial	One RS-232 port (on the SBC front panel) to support sync/async DCE or DTE operation. One RS-485 port (on connector P2) to support multi-protocol capabilities.
Parallel	Bidirectional I/O Centronics printer port (connection through the front panel).
Timers:	
Local bus timer	115 microseconds
Watchdog timer	15 milliseconds
MC6823Ø	24-bit programmable timer

TABLE 1-1. SBC SPECIFICATIONS (cont.)

Characteristic	Specification
VMEbus requester	Release-On-Request with early bus busy release.
Interrupt handler	Up to 9 interrupt requests from VMEbus. (IRQ1 through IRQ7, SYSFAIL, AC FAIL)
Temperatures:	
Operating	Ø to 5Ø degrees C
Storage	-4Ø to 85 degrees C
Relative humidity	5% to 9Ø% (non-condensing)
Physical size (PCB):	
Height x width	6.3Ø inches (16.ØØ cm) x 9.19 inches (23.34 cm)
Thickness	Ø.Ø62 inch (Ø.157 cm)
Part projections:	
Component side	Ø.5Ø inch (1.27 cm) maximum
Solder side	Ø.Ø67 inch (Ø.17 cm) maximum

1.3.1 FCC Compliance

The SBC units (VME1Ø4, VME1Ø5, VME1Ø6, and VME1Ø7) were tested in an FCC-compliant chassis, and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

1. Shielded cables on all external I/O ports.

2. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.

3. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.

4. Front panels screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the modules.

1.4 GENERAL DESCRIPTION

The SBC units are 24-bit address and 16-bit data Single-Board Computers. All SBC units incorporate the MC68Ø1Ø (1Ø MHz) 24-bit address and 16-bit data microprocessor. The units interface with the VMEbus, and includes 512K bytes of on-board DRAM memory (shared with VMEbus), two serial ports, one parallel/printer port, and four on-board sockets supporting various RAM and EPROM devices. The SBC units incorporate system controller functions, an interrupt handler, and a level 3 bus arbitor. In the VME1Ø4, the SBC supports the I/O channel interface. In the VME1Ø6, the SBC supports four 5-1/4 inch floppy disk drives. In the VME1Ø7, the SBC supports the full SCSI bus as defined by specification ANSI X3T9.2/82-2. All four SBC units are capable of stand-alone operation with the addition of a power supply and terminal.

1.5 REFERENCE DOCUMENTATION

The following publications may provide additional information. If not shipped with this product, they may be purchased from Motorola's Literature Distribution Center, 616 West 24th Street, Tempe, Arizona 85282; telephone (6Ø2) 994-6561.

Document Title	Motorola Publication
VMEbus Specification Manual	HB212/D
I/O Modules Input/Output Channel Specification Manual	M68RIOCS
MC68Ø1Ø 16 Bit Virtual Memory Data Sheet	ADI-942

The Z8Ø3Ø/Z853Ø SCC Serial Communications Controller Technical Manual may be obtained from Zilog, Inc., Corporate Communications, Building A, 1315 Dell Ave., Campbell, California 95ØØ8.

The NCR 538Ø SCSI Interface Chip Data Sheet may be obtained from NCR Microelectronic Division, 1635 Aeroplaza Drive, Colorado Springs, Colorado 8Ø916.

The SCSI Small Computer System Interface Specification Draft X3T9.2/82-2 may be obtained from Computer and Business Equipment Manufacturers Association, 311 First Street, N. W., Suite 5ØØ, Washington, D.C. 2ØØØ1.

The Centronics Specification may be obtained from Centronics Data Computer Corporation, 1 Wall Street, Hudson, New Hampshire Ø3Ø52.

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CHAPTER 2
HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides the unpacking, hardware preparation, and installation instructions for the SBC units.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request that the carrier's agent be present during unpacking/inspection of equipment.

Unpack and remove the SBC unit(s) from its shipping carton. Refer to the packing list and verify that all items are present. Care should be taken during the unpacking of the module. Save the original shipping container and packing material for storing or reshipping of the equipment.

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

Inspect for any shipping damage. If no damage exists, the module can then be prepared (jumpers configured) and readied for installation.

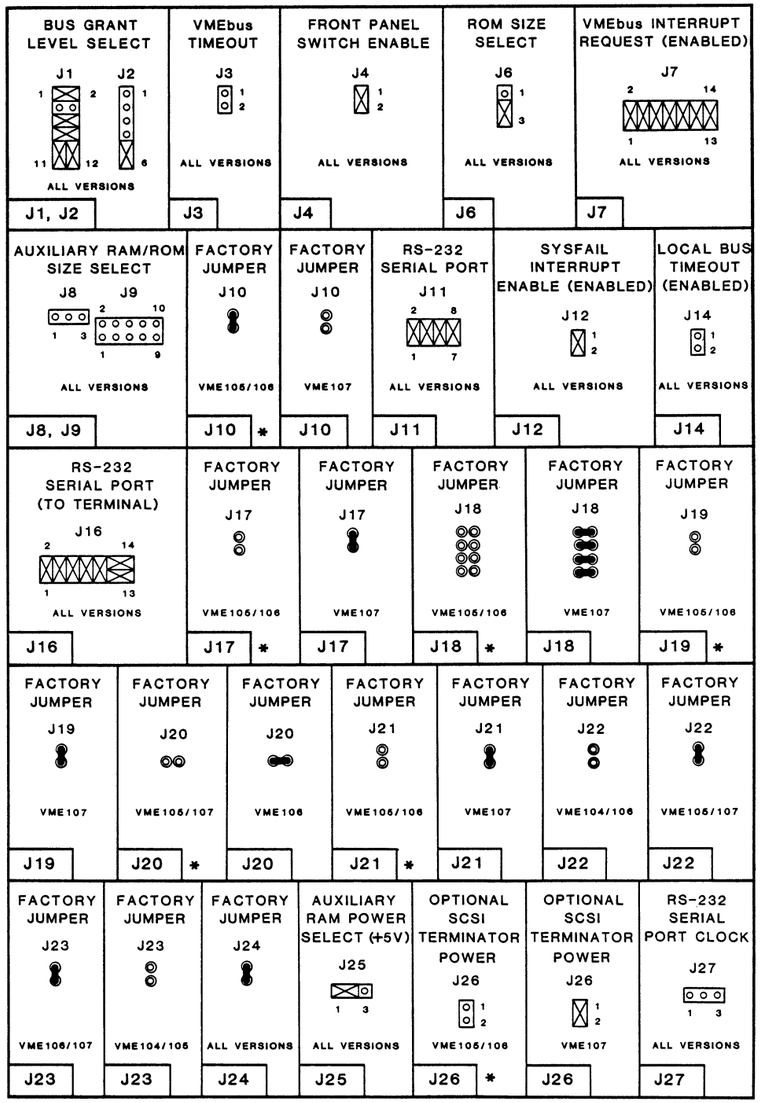
2.3 HARDWARE PREPARATION

This section describes the hardware preparation for the SBC prior to installation. Observance of this description will ensure the user that all unit components are properly configured for operation.

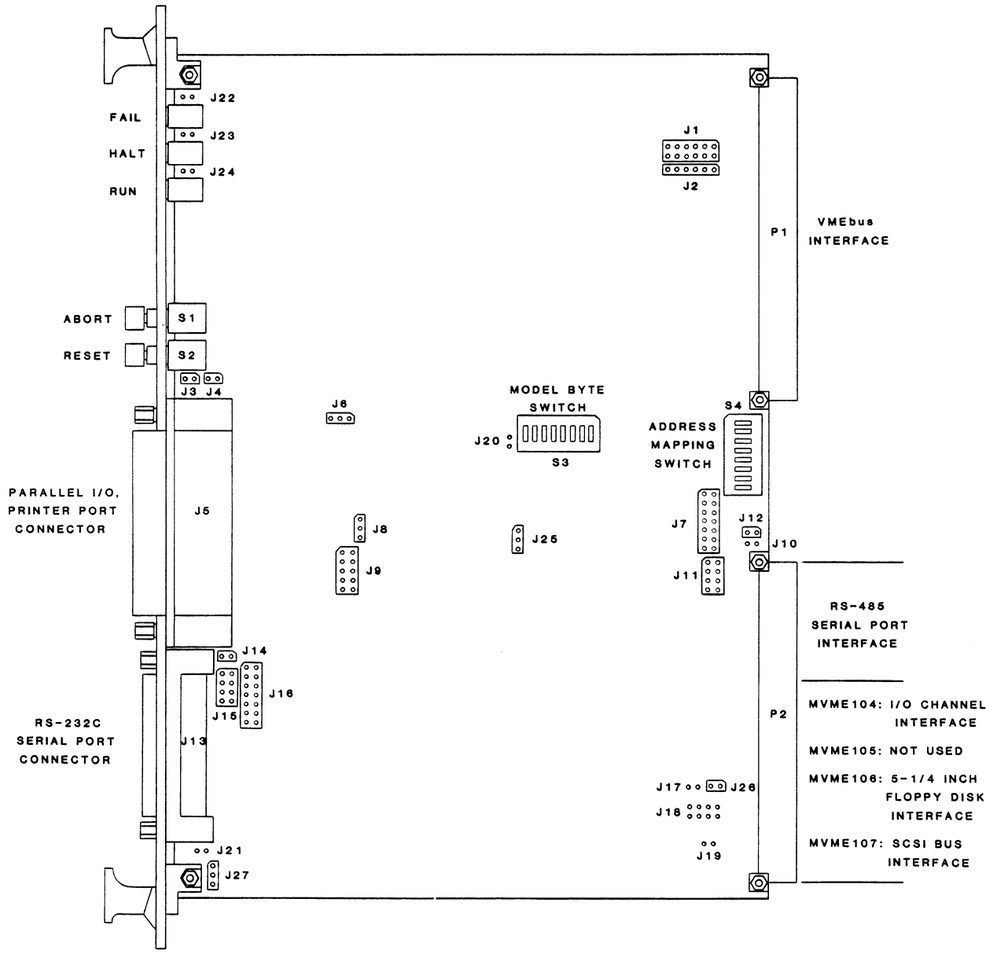
Jumper blocks are used to select the various functions and options of the SBC. Before the SBC is installed, the user should verify the jumper block configurations and alter the jumpers, as required, for the user's particular system operation. The SBC has been factory tested and is shipped with factory-installed jumper configurations that are illustrated in Figure 2-1. The SBC is operational with

these factory-installed jumpers. Table 2-1 lists the jumper blocks by designation, function, and factory configuration. A more detailed description of these jumper blocks is provided in the following sections.

Two DIP-type switches (S3 and S4) are located on the SBC. For detailed information regarding the use of these two switches, refer to Chapter 3.



* NOTE: JUMPERS J10, J17, J18, J19, J20, J21, AND J26 DO NOT EXIST ON THE VME104.



NOTE: Figure above depicts a composite module and illustrates jumper locations only. Refer to adjacent chart and Table 2-1 for jumper population and configuration.

FIGURE 2-1. SBC JUMPER, CONNECTOR, AND SWITCH LOCATION DIAGRAM

2.3.1 SBC Jumper Block Settings

The following table lists and describes the SBC jumper blocks.

TABLE 2-1. SBC JUMPER BLOCK PLACEMENTS

Jumper	Function	Factory Configuration
J1	Bus Grant Level Select	J1 (1-2)(5-6)(7-8)(9-11)(1Ø-12)
J2	Bus Request Level Select	J2 (5-6)
J3	VMEbus Timeout	No jumper installed.
J4	Front Panel Switch Enable (Enabled)	J4 (1-2)
J5	Printer Port Connector	--------
J6	ROM Size Select (64K x 8 devices)	J6 (2-3)
J7	VMEbus Interrupt Requests (Enabled)	J7 (1-2)(3-4)(5-6)(7-8)(9-1Ø) (11-12)(13-14)
J8	Auxiliary RAM/ROM Size Select	No jumper(s) installed.
J9	Auxiliary RAM/ROM Size Select	No jumper(s) installed.
J1Ø	Factory Jumper (For factory use only)	Does not exist on VME1Ø4. J1Ø (1-2) stapled closed on VME1Ø5 and VME1Ø6. J1Ø (1-2) soldered closed on VME1Ø7.
J11	RS-485 Serial Port	J11 (1-2)(3-4)(5-6)(7-8)
J12	SYSFAIL Interrupt Enable (Enabled)	J12 (1-2)
J13	RS-232 Serial Port Connector	--------

2

TABLE 2-1. SBC JUMPER BLOCK PLACEMENTS (cont.)

Jumper	Function	Factory Configuration
J14	Local Bus Timeout (Enabled)	No jumper(s) installed.
J15	RS-232 Serial Port Clocks	No jumper(s) installed.
J16	RS-232 Serial Port (To Terminal)	J16 (1-2)(3-4)(5-6)(7-8)(9-1Ø) (11-13)(12-14)
J17	Factory Jumper (For factory use only)	Does not exist on VME1Ø4. No jumper irstalled on VME1Ø5 and VME1Ø6. J17 (1-2) stapled closed on VME1Ø7.
J18	Factory Jumper (For factory use only)	Does not exist on VME1Ø4. No jumpers installed on VME1Ø5 and VME1Ø6. J18 (1-2)(3-4)(5-6)(7-8) stapled closed on VME1Ø7.
J19	Factory Jumper (For factory use only)	Does not exist on VME1Ø4. No jumper installed on VME1Ø5 and VME1Ø6. J19 (1-2) stapled closed on VME1Ø7.
J2Ø	Factory Jumper (For factory use only)	Does not exist on VME1Ø4. No jumper installed on VME1Ø5 and VME1Ø7. J2Ø (1-2) stapled closed on VME1Ø6.
J21	Factory Jumper (For factory use only)	Does not exist on VME1Ø4. No jumper installed on VME1Ø5 and VME1Ø6. J21 (1-2) stapled closed on VME1Ø7.

TABLE 2-1. SBC JUMPER BLOCK PLACEMENTS (cont.)

Jumper	Function	Factory Configuration
J22	Factory Jumper (For factory use only)	No jumper installed on VME1Ø4 and VME1Ø6. J22 (1-2) stapled closed on VME1Ø5 and VME1Ø7.
J23	Factory Jumper (For factory use only)	No jumper installed on VME1Ø4 and VME1Ø5. J23 (1-2) stapled closed on VME1Ø6 and VME1Ø7.
J24	Factory Jumper (For factory use only)	J24 (1-2) stapled closed on all versions.
J25	Auxiliary RAM Power Select (+5 Vdc)	J25 (1-2) installed on all versions.
J26	Optional SCSI Terminator Power	Does not exist on VME1Ø4. No jumper installed on VME1Ø5 and VME1Ø6. J26 (1-2) installed on VME1Ø7.
J27	RS-232 Serial Port Clock	No jumpers installed

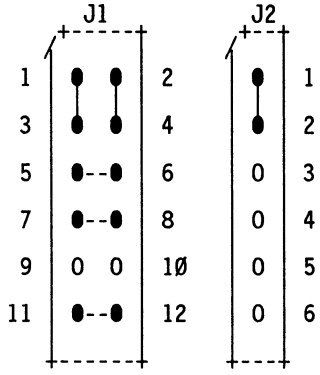
2.3.1.1 Bus Grant/Request Level Select (J1,J2)

The VMEbus has four bus request levels (BGØIN*/OUT* through BG3IN*/OUT*), each having an associated bus grant daisy-chain. Level 3 has the highest priority while level Ø has the lowest. Jumper block J1, in conjunction with jumper block J2, allow the user to select the desired priority level for VMEbus accesses. When the SBC is configured as the System Controller, Bus Grant/Request Level 3 must be set. The following configurations illustrate the proper jumpering for each bus arbitration level.

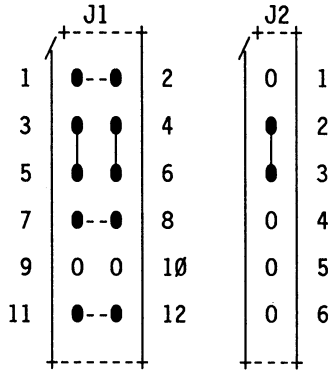
NOTE: No other configurations will work properly.

2

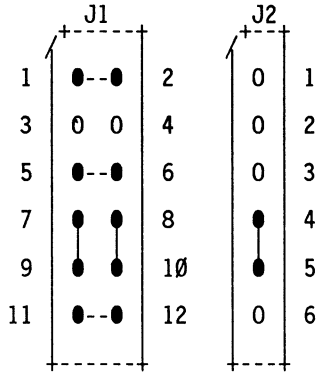
Jumper Blocks J1 and J2
Bus Grant/Request Level
Bus Level Ø



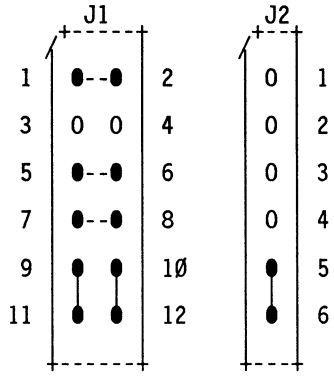
Jumper Blocks J1 and J2
Bus Grant/Request Level
Bus Level 1



Jumper Blocks J1 and J2
Bus Grant/Request Level
Bus Level 2



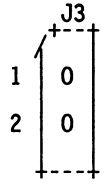
Jumper Blocks J1 and J2
Bus Grant/Request Level
Bus Level 3
(Factory Setting)



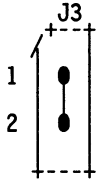
2.3.1.2 VMEbus Timeout (Enabled)(J3)

Jumper block J3 is used to disable the VMEbus timer. Installing a jumper pin at J3 will disable the timer and allow infinite VMEbus cycles when the SBC is the System Controller.

Jumper Block J3
VMEbus Timeout (Enabled)
No Jumper Installed
(Factory Setting)



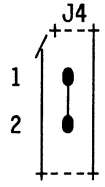
Jumper Block J3
VMEbus Timeout (Disabled)
Jumper Installed



2.3.1.3 Front Panel Enable (J4)

Jumper block J4 is used to enable/disable the front panel switches.

Jumper Block J4
Front Panel Enable
(Factory Setting)

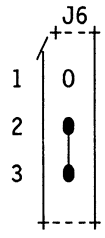


2.3.1.4 ROM Size Select (J6)

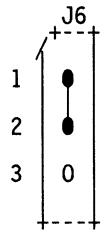
Jumper block J6 selects the size of ROMs used at sockets U56 and U63. The SBC is factory-configured with a jumper pin between J6-2 and J6-3 for 64K x 8 devices. Should the user need to use 32K x 8 devices, then set the jumper pin between J6-1 and J6-2.

2

Jumper Block J6
ROM Size Select
64K x 8 Devices
(Factory Setting)



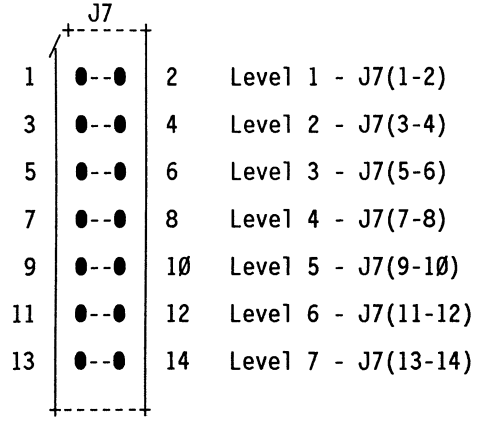
Jumper Block J6
ROM Size Select
32K x 8 Devices



2.3.1.5 VMEbus Interrupt Requests Enable (J7)

Jumper block J7 is used for VMEbus interrupt enable. There are seven possible jumper locations; each one enables servicing one of the seven off-board interrupt levels. The factory setting configuration enables all these levels. Thus, a jumper pin installed allows the SBC to handle that level interrupt on VMEbus.

Jumper Block J7
VMEbus Interrupt Request Enable
(Factory Setting)

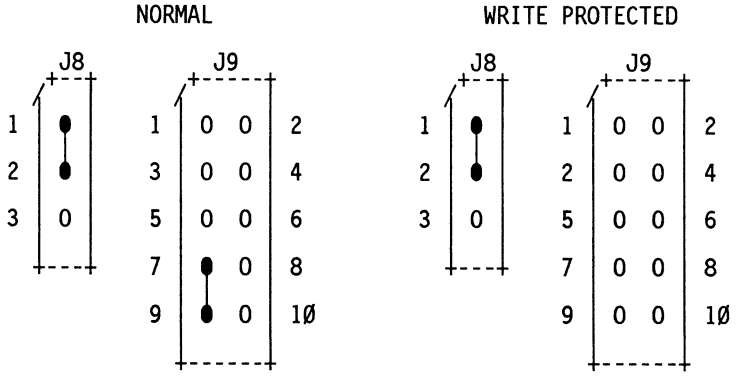


2.3.1.6 Auxiliary RAM/ROM Device Size Select (J8,J9)

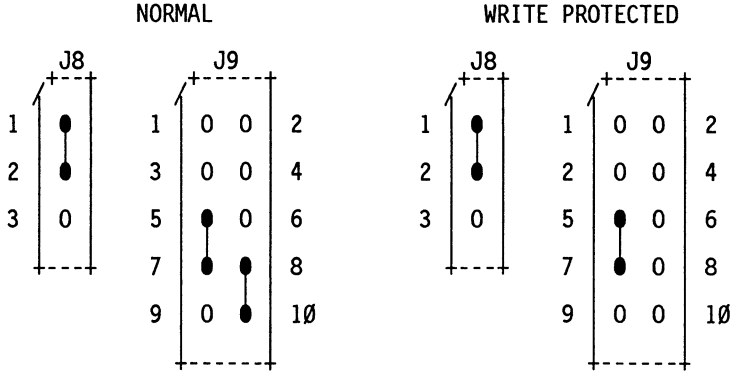
Jumper blocks J8 and J9 are used to select the size of the different devices used for the auxiliary RAM located at sockets XU48 and XU7Ø. Refer to Appendix A for suggested devices.

NOTE: 24-pin devices are inserted with pins 1 through 24 of the device matching pins 3 through 26 of RAM sockets XU48 and XU7Ø.

a) 2K x 8 Static RAM:

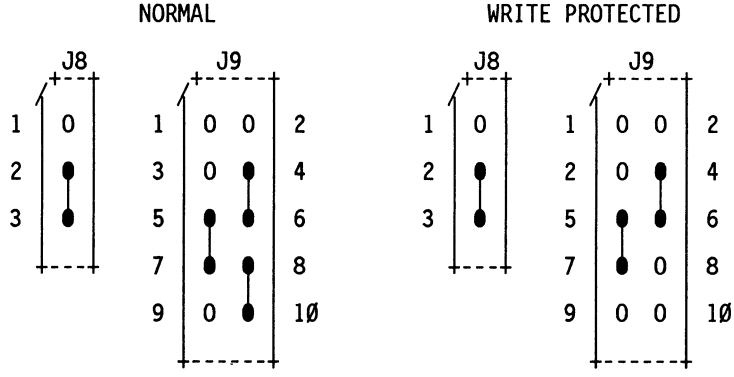


b) 8K x 8 Static RAM:

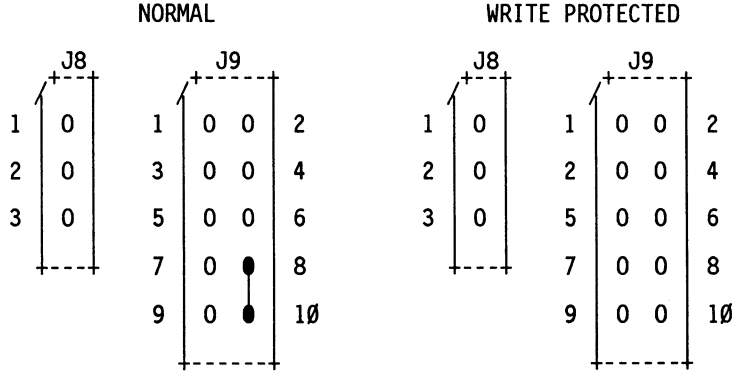


2

c) 32K x 8 Static RAM:

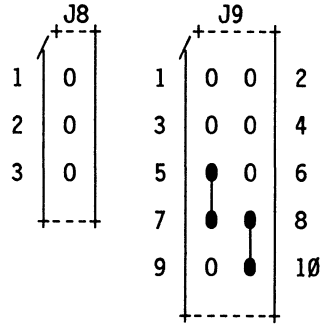


d) 2K x 8 EEPROM:

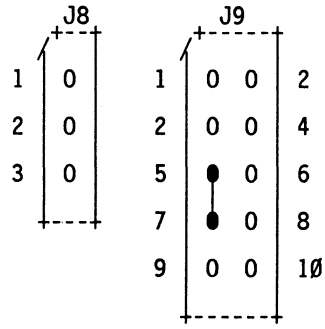


e) 8K x 8 EEPROM:

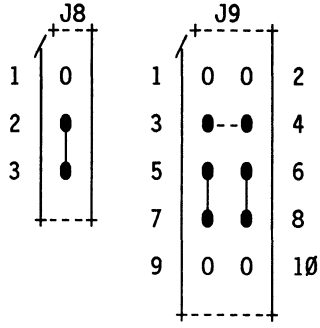
NORMAL



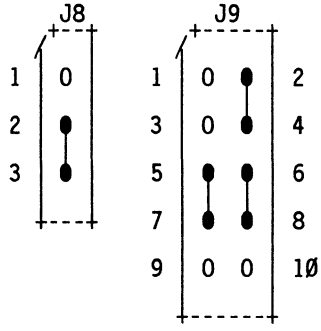
WRITE PROTECTED



f) 32K x 8 EPROM:



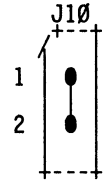
g) 64K x 8 EPROM:



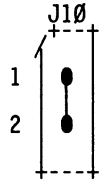
2.3.1.7 Factory Jumper (J1Ø)

Jumper J1Ø is a two-pin jumper for factory use only. Jumper J1Ø does not exist on the VME1Ø4 version of the SBC. Jumper J1Ø has a jumper staple installed on the VME1Ø5 and VME1Ø6, while it is soldered closed on the VME1Ø7.

Jumper Block J1Ø
Factory Jumper
(Jumper Stapled on VME1Ø5/1Ø6)



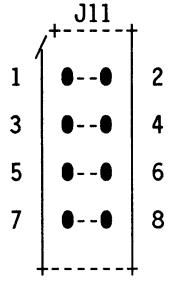
Jumper Block J1Ø
Factory Jumper
(Soldered Closed on VME1Ø7)



2.3.1.8 RS-485 Serial Port (J11)

Jumper block J11 is used to configure the SBC of master/slave operation and 8/4/2 wire operation.

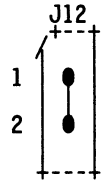
Jumper Block J11
RS-485 Serial Port



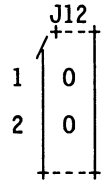
2.3.1.9 SYSFAIL Interrupt Enable (J12)

Jumper block J12 is used to enable the SYSFAIL interrupt.

Jumper Block J12
SYSFAIL Enabled
Jumper Installed
(Factory Setting)



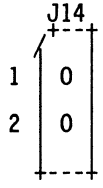
Jumper Block J12
SYSFAIL Disabled
No Jumper Installed



2.3.1.1Ø Local Bus Timeout (Enable)(J14)

Jumper block J14 is used to disable the local bus timer. As shipped from the factory (no jumper installed), the setting is 115 microseconds. Installing a jumper pin across J14-1 and J14-2 provides an infinite time limit on the local bus cycles.

Jumper Block J14
Local Bus Timeout
(Factory Setting)

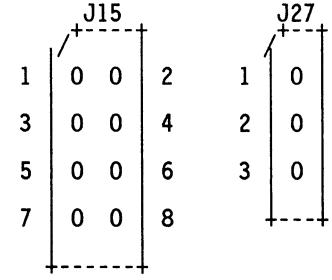


2

2.3.1.11 RS-232 Serial Port Clock (J15,J27)

Jumper block J15 is used in conjunction with jumper block J27 to configure the SBC's RS-232 serial port synchronous clocks.

Jumper Block J15 and J27
RS-232 Serial Port Clock
No Jumpers Installed
(Factory Setting)



The following charts illustrate several configurations to configure the serial port synchronous clock.

SBC (configured as a modem)	Jumper Blocks J15	J27
Transmit Clock (pin 26 of Z853Ø) to pin 17 of RS-232 cable*	(5-7)	(1-2)
Transmit Clock (pin 26 of Z853Ø) to pin 15 of RS-232 cable	(5-6)	(1-2)
Transmit Clock (pin 26 of Z853Ø) to pin 24 of RS-232 cable	(5-3)	(1-2)

* Recommended method to connect two SBCs without a modem.

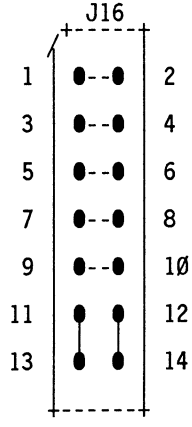
SBC (configured as a terminal)	Jumper Blocks J15	J27
Receive Clock (pin 28 of Z853Ø) from pin 17 of RS-232 cable*	(1-2)	---
Transmit Clock as input (pin 26 of Z853Ø) from pin 15 of RS-232 cable	(4-6)	(2-3)
Transmit Clock as input (pin 26 of Z853Ø) from pin 24 of RS-232 cable	(3-4)	(2-3)

* Recommended method to connect two SBCs without a modem.

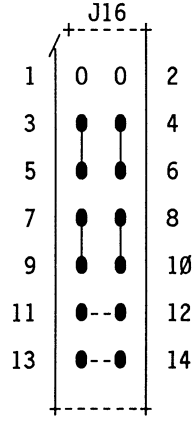
2.3.1.12 RS-232 Serial Port Data and Handshake (J16)

Jumper block J16 is used to configure the data and handshake lines on the RS-232 serial port.

Jumper Block J16
RS-232 Serial Port
Data and Handshake
Configured as a Modem
(Factory Setting)



Jumper Block J16
RS-232 Serial Port
Data and Handshake
Configured as a Terminal



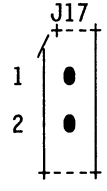
If a different configuration is desired, the following chart can be used. If connections must be made to other than adjacent pins, it can be accomplished by wire-wrapping the pins.

J16 Pin	Signal	Connection
1	DSR	RS-232, pin 6.
2	+12 V	+12V pull-up resistor to terminate any signal into RS-232.
3	DCD	Receiver into DCD input of Z853Ø, pin 21.
4	DTR	RS-232, pin 2Ø.
5	DCD	RS-232, pin 8.
6	DTR	Driven from DTR output of Z853Ø, pin 24.
7	CTS	Receiver into CTS input of Z853Ø, pin 22.
8	RTS	RS-232, pin 4.
9	CTS	RS-232, pin 5.
1Ø	RTS	Driven from RTS output of Z853Ø, pin 23.
11	RXD	Receiver into RXD input of Z853Ø, pin 27.
12	TXD	RS-232, pin 3.
13	RXD	RS-232, pin 2.
14	TXD	Driven from TXD output of Z853Ø, pin 25.

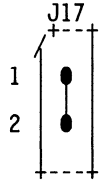
2.3.1.13 Factory Jumper (J17)

Jumper J17 is a two-pin jumper for factory use only. Jumper J17 does not exist on the VME1Ø4 version of the SBC. Jumper J17 is soldered closed on the VME1Ø5 and VME1Ø6, while on the VME1Ø7, a jumper staple is installed.

Jumper Block J17
Factory Jumper
(Soldered Closed on VME1Ø5/1Ø6)



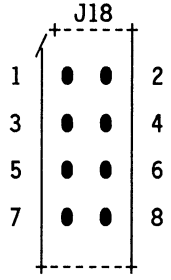
Jumper Block J17
Factory Jumper
(Jumper Stapled on VME1Ø7)



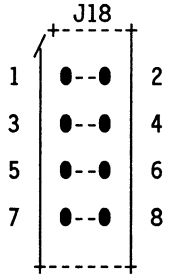
2.3.1.14 Factory Jumper (J18)

Jumper block J18 is for factory use only. Jumper block J18 does not exist on the VME1Ø4. In the VME1Ø5 and VME1Ø6 version of the SBC, jumper block J18 is soldered closed, while on the VME1Ø7, jumper staples are installed.

Jumper Blocks J18
Factory Jumper
(Soldered Closed on VME1Ø5/1Ø6)



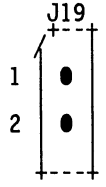
Jumper Blocks J18
Factory Jumper
(Jumper Stapled on VME1Ø7)



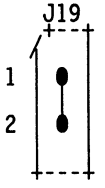
2.3.1.15 Factory Jumper (J19)

Jumper J19 is a two-pin jumper for factory use only. Jumper J19 does not exist on the VME1Ø4 version of the SBC. Jumper J19 is soldered closed on the VME1Ø5 and VME1Ø6, while on the VME1Ø7, a jumper staple is installed.

Jumper Block J19
Factory Jumper
(Soldered Closed on VME1Ø5/1Ø6)



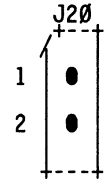
Jumper Block J19
Factory Jumper
(Jumper Stapled on VME1Ø7)



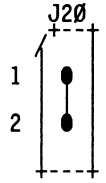
2.3.1.16 Factory Jumper (J2Ø)

Jumper J2Ø is a two-pin jumper for factory use only. Jumper J2Ø does not exist on the VME1Ø4 version of the SBC. Jumper J2Ø is soldered closed on the VME1Ø5 and VME1Ø7, while on the VME1Ø6, a jumper staple is installed.

Jumper Block J2Ø
Factory Jumper
(Soldered Closed on VME1Ø5/1Ø7)



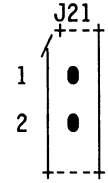
Jumper Block J2Ø
Factory Jumper
(Jumper Stapled on VME1Ø6)



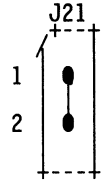
2.3.1.17 Factory Jumper (J21)

Jumper J21 is a two-pin jumper for factory use only. Jumper J21 does not exist on the VME1Ø4 version of the SBC. Jumper J21 is soldered closed on the VME1Ø5 and VME1Ø6, while on the VME1Ø7, a jumper staple is installed.

Jumper Block J21
Factory Jumper
(Soldered Closed on VME1Ø5/1Ø6)



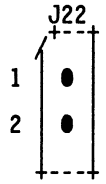
Jumper Block J21
Factory Jumper
(Jumper Stapled on VME1Ø7)



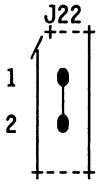
2.3.1.18 Factory Jumper (J22)

Jumper J22 is a two-pin jumper for factory use only. Jumper J22 is soldered closed on the VME1Ø4 and VME1Ø6, while on the VME1Ø5 and VME1Ø7, a jumper staple is installed.

Jumper Block J22
Factory Jumper
(Soldered Closed on VME1Ø4/1Ø6)



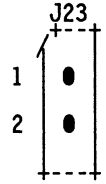
Jumper Block J22
Factory Jumper
(Jumper Stapled on VME1Ø5/1Ø7)



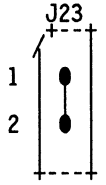
2.3.1.19 Factory Jumper (J23)

Jumper J23 is a two-pin jumper for factory use only. Jumper J23 is soldered closed on the VME1Ø4 and VME1Ø5, while on the VME1Ø6 and VME1Ø7, a jumper staple is installed.

Jumper Block J23
Factory Jumper
(Soldered Closed on VME1Ø4/1Ø5)



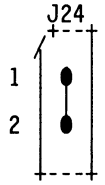
Jumper Block J23
Factory Jumper
(Jumper Stapled on VME1Ø6/1Ø7)



2.3.1.2Ø Factory Jumper (J24)

Jumper J24 is a two-pin jumper for factory use only. A jumper staple is installed at jumper J24 on all versions of the SBC.

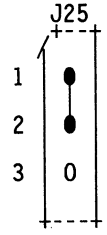
Jumper Block J24
Factory Jumper
(Jumper Stapled on all versions)



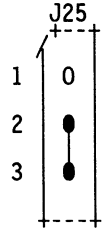
2.3.1.21 Auxiliary RAM Power Select (J25)

Jumper block J25 selects the power source for the auxiliary RAM sockets XU48 and XU7Ø. A jumper pin installed across pins J25-1 and J25-2 supplies +5V power, while a jumper pin across pins J25-2 and J25-3 supplies +5V stand-by power from the VMEbus.

Jumper Block J25
Auxiliary RAM Power
Select (+5V)
(Factory Setting)



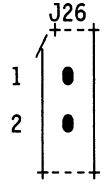
Jumper Block J25
Auxiliary RAM Power
Select (+5V Stand-by)



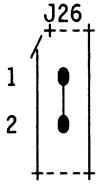
2.3.1.22 Optional SCSI Terminator Power (J26)

Jumper block J26 is used to supply +5 Vdc optional terminator power to the SCSI bus. Jumper J26 does not exist on the VME1Ø4 version of the SBC. Jumper J26 is soldered closed on the VME1Ø5 and VME1Ø6, while on the VME1Ø7, a jumper pin is installed.

Jumper Block J26
Optional SCSI Terminator Power
(Soldered Closed on VME1Ø5/1Ø6)
(Factory Setting)



Jumper Block J26
Optional SCSI Terminator Power
(Jumper pin installed on VME1Ø7)



2.3.1.23 RS-232 Serial Port Clock (J27)

Jumper block J27 is used in conjunction with J15 to configure the RS-232 port serial clock. Refer to section 2.3.1.11 for jumper settings and possible configurations for jumper block J27.

2.4 INSTALLATION INSTRUCTIONS FOR VME CHASSIS OPERATION

When the SBC has been prepared (configured by the user) as desired, it is ready for system use and can then be installed in a VMEmodule chassis. The following general procedure is recommended for installation of the SBC.

a. Turn all equipment OFF.

CAUTION

INSERTING OR REMOVING THE MODULE WHILE POWER IS APPLIED COULD RESULT IN DAMAGE TO MODULE PARTS. AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

b. The SBC may be installed into any ususued double-high slot on a VMEmodule chassis. Using a firm grip on the module, slide the unit into the card slide until the P1 and P2 connectors of the SBC align and seat into the backplane sockets. Use a firm, steady pushing motion to install the unit snuggly into the backplane.

c. Turn chassis power ON.

2.5 INSTALLATION INSTRUCTIONS FOR STAND-ALONE OPERATION

Stand-alone operation is similar to operation in a chassis, except that the SBC must be connected to a power source and must always be the system controller (refer to section 4.17). In addition, the SBC must be placed or mounted in such a way that the pins on the module are in no danger of being shorted.

Connectors must be attached to P1 and P2 with power supplied through the following pins.

+5V	-- P1 pins: A32, B32, C32	P2 pins: B1, B13, B32
GND	-- P1 pins: A9, A11, A15, A17, A19, B2Ø, B23, C9	P2 pins: B2, B12, B22, B31
+12V	-- P1 pins: C31	
-12V	-- P1 pins: A31	

NOTE: +12 V and -12V need not be supplied unless the front panel RS-232 port is to be used.

CHAPTER 3
OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter describes the switches, operating controls, and indicators found on the front panel of the SBC unit.

3.2 CONTROLS AND INDICATORS

The SBC has two control switches (RESET and ABORT) and three LED indicators (HALT, RUN, and FAIL) located on the front panel of the SBC. The SBC also has two eight-position readable switches (S3 and S4) which provide control over the Model Byte Register (MBR) and the address mapping and system configuration.

3.2.1 FAIL Indicator DS1

The red LED FAIL indicator, located on the front panel, indicates the status of the fail bit in the control register.

3.2.2 HALT Indicator DS2

The red LED HALT indicator, located on the front panel, is lit when the MC68Ø1Ø microprocessor enters a halted state (usually the result of a double bus fault). The indicator is also lit whenever the MC68Ø1Ø is being reset.

3.2.3 RUN Indicator DS3

The green LED RUN indicator, located on the front panel, is connected to the MC68Ø1Ø's address strobe signal (AS*) and indicates that the MC68Ø1Ø is executing a bus cycle.

3.2.4 ABORT Switch S1

The ABORT switch is a momentary type switch located on the front panel. Pressing the ABORT switch causes a local level 7 interrupt to the MC68Ø1Ø. Bit 14 of the Address Status Register (ASR) is set to a "1" when this switch is pressed. It is cleared when the ASR is read.

3.2.5 RESET Switch S2

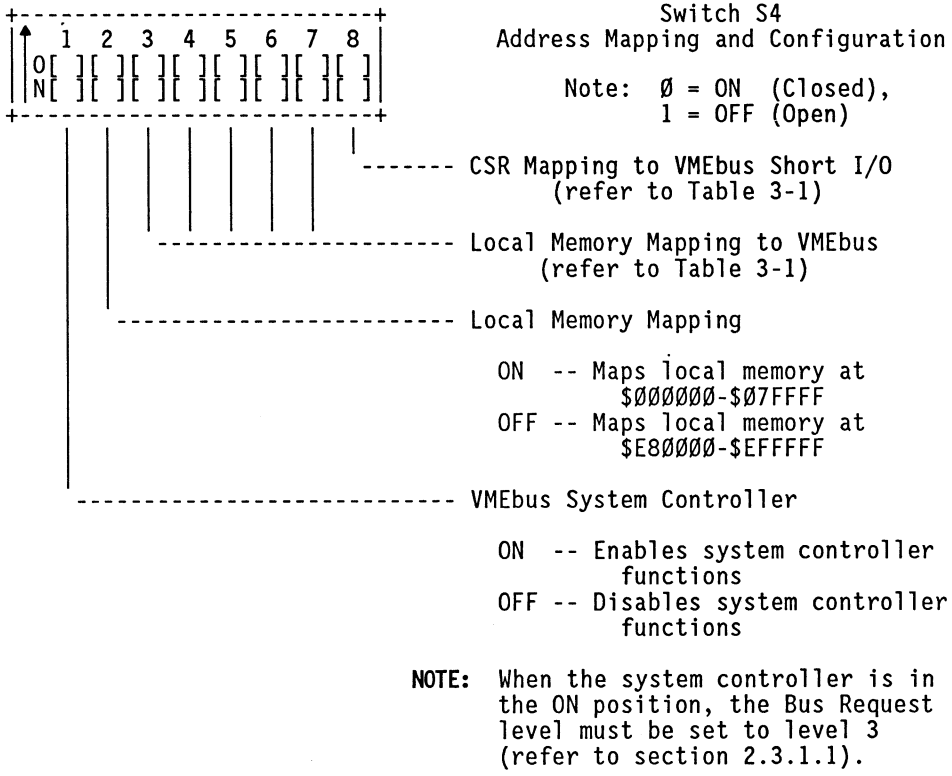
The RESET switch is a momentary type switch located on the front panel. When pressed, the RESET switch generates a local reset and (if the SBC is system controller) also generates a VMEbus system reset.

3.2.6 Model Byte Switch S3

Switch S3 is a software-accessible board status register on the VME1Øx. It is implemented in hardware as an an eight-position DIP switch and does not perform any hardware control directly. The function of switch S3 is completely dependent on the system software. For more detailed information on the 1ØxBug operation for switch S3, refer to the 1ØxBug user's manual.

3.2.7 Address Mapping and Configuration Switch S4

Switch S4 is an eight-position DIP switch which is used to map the local memory and the CSR to the VMEbus. It selects local memory to reside at either $ØØØØØØ or $E8ØØØØ and selects whether the SBC will be the system controller.



NOTE: When the system controller is in the ON position, the Bus Request level must be set to level 3 (refer to section 2.3.1.1).

TABLE 3-1. SWITCH S4 VME ADDRESS MAPPING

Binary Switch Position 7	6	5	4	3	Local RAM appears on VMEbus at VME Hex Address			Short I/O Map Address in Hex Switch Position 8 (Closed = ON)	(OPEN = OFF)
Ø	Ø	Ø	Ø	Ø	ØØØØØØ	to	Ø7FFFF	ØØØØ - ØØ7F	8ØØØ - 8Ø7F
Ø	Ø	Ø	Ø	1	Ø8ØØØØ	to	ØFFFFF	ØØ8Ø - ØØFF	8Ø8Ø - 8ØFF
Ø	Ø	Ø	1	Ø	1ØØØØØ	to	17FFFF	Ø1ØØ - Ø17F	81ØØ - 817F
Ø	Ø	Ø	1	1	18ØØØØ	to	1FFFFF	Ø18Ø - Ø1FF	818Ø - 81FF
Ø	Ø	1	Ø	Ø	2ØØØØØ	to	27FFFF	Ø2ØØ - Ø27F	82ØØ - 827F
Ø	Ø	1	Ø	1	28ØØØØ	to	2FFFFF	Ø28Ø - Ø2FF	828Ø - 82FF
Ø	Ø	1	1	Ø	3ØØØØØ	to	37FFFF	Ø3ØØ - Ø37F	83ØØ - 837F
Ø	Ø	1	1	1	38ØØØØ	to	3FFFFF	Ø38Ø - Ø3FF	838Ø - 83FF
Ø	1	Ø	Ø	Ø	4ØØØØØ	to	47FFFF	Ø4ØØ - Ø47F	84ØØ - 847F
Ø	1	Ø	Ø	1	48ØØØØ	to	4FFFFF	Ø48Ø - Ø4FF	848Ø - 84FF
Ø	1	Ø	1	Ø	5ØØØØØ	to	57FFFF	Ø5ØØ - Ø57F	85ØØ - 857F
Ø	1	Ø	1	1	58ØØØØ	to	5FFFFF	Ø58Ø - Ø5FF	858Ø - 85FF
Ø	1	1	Ø	Ø	6ØØØØØ	to	67FFFF	Ø6ØØ - Ø67F	86ØØ - 867F
Ø	1	1	Ø	1	68ØØØØ	to	6FFFFF	Ø68Ø - Ø6FF	868Ø - 86FF
Ø	1	1	1	Ø	7ØØØØØ	to	77FFFF	Ø7ØØ - Ø77F	87ØØ - 877F
Ø	1	1	1	1	78ØØØØ	to	7FFFFF	Ø78Ø - Ø7FF	878Ø - 87FF
1	Ø	Ø	Ø	Ø	8ØØØØØ	to	87FFFF	Ø8ØØ - Ø87F	88ØØ - 887F
1	Ø	Ø	Ø	1	88ØØØØ	to	8FFFFF	Ø88Ø - Ø8FF	888Ø - 88FF
1	Ø	Ø	1	Ø	9ØØØØØ	to	97FFFF	Ø9ØØ - Ø97F	89ØØ - 897F
1	Ø	Ø	1	1	98ØØØØ	to	9FFFFF	Ø98Ø - Ø9FF	898Ø - 89FF
1	Ø	1	Ø	Ø	AØØØØØ	to	A7FFFF	ØAØØ - ØA7F	8AØØ - 8A7F
1	Ø	1	Ø	1	A8ØØØØ	to	AFFFFF	ØA8Ø - ØAFF	8A8Ø - 8AFF
1	Ø	1	1	Ø	BØØØØØ	to	B7FFFF	ØBØØ - ØB7F	8BØØ - 8B7F
1	Ø	1	1	1	B8ØØØØ	to	BFFFFF	ØB8Ø - ØBFF	8B8Ø - 8BFF
1	1	Ø	Ø	Ø	CØØØØØ	to	C7FFFF	ØCØØ - ØC7F	8CØØ - 8C7F
1	1	Ø	Ø	1	C8ØØØØ	to	CFFFFF	ØC8Ø - ØCFF	8C8Ø - 8CFF
1	1	Ø	1	Ø	DØØØØØ	to	D7FFFF	ØDØØ - ØD7F	8DØØ - 8D7F
1	1	Ø	1	1	D8ØØØØ	to	DFFFFF	ØD8Ø - ØDFF	8D8Ø - 8DFF
1	1	1	Ø	Ø	EØØØØØ	to	E7FFFF	ØEØØ - ØE7F	8EØØ - 8E7F
1	1	1	Ø	1	E8ØØØØ	to	EFFFFF	ØE8Ø - ØEFF	8E8Ø - 8EFF

NOTE: Switch position S4-8 maps the Short I/O in the low range when ON (Closed) and in the high range when OFF (Open).

The CSR appears in the Short I/O address space on the VMEbus. It is multiple decoded in 128 locations. VMEbus accesses are not allowed by the SBC in the Short I/O space mapped for that module. Example: An SBC mapped with switch positions S4-3 to S4-7 set to ØØØØØ could not access the short I/O addresses from $ØØØØ through to $ØØ7F (S4-8 = Closed) or $8ØØØ through $807F (S4-8 = Open). To do so would cause a bus error. Software can read the contents in the ASR and disallow

access to the SBC's own I/O range. Switch positions S4-2 through S4-8 can be read through the ASR.

3.3 LOCAL MEMORY MAP

3

Table 3-2 provides the memory mapping ranges for the various devices used on the SBC.

TABLE 3-2. LOCAL MEMORY MAP

Devices	Address	Comments
Short I/O	$FFØØØØ-$FFFFFF	Causes lower 16 address bits to be presented on VMEbus with short I/O address modifiers.
Address Switch Register	$FE8ØØØ	
I/O Channel VME1Ø4	$FE6ØØ1-$FE7FFF	
Disk VME1Ø6 Floppy	$FE6ØØ1-$FE6ØØ5	
Disk VME1Ø7 SCSI	$FE6ØØ1-$FE61F	
Serial Port	$FE4ØØ1-$FE4ØØ7	
Model Byte Register	$FE2ØØ1	Read only.
I/O Channel Interrupt Vector Register	$FE2ØØ1-$FE2ØØ7	Write only (VME1Ø4 only).
MC6823Ø	$FEØØØ1-$FEØØ3F	
Control Status Register	$FDØØØØ	
Auxiliary RAM/ROM	$F2ØØØØ-$F3FFFF	
ROM	$FØØØØØ-$F1FFFF	
Alternate Local RAM	$E8ØØØØ-$EFFFFF	When S4-2 = OFF (open).
VMEbus	$Ø8ØØØØ-$EFFFFF $ØØØØØØ-$E7FFFF	If local RAM is mapped at Ø, S4-2 = ON. If local RAM is mapped at E8ØØØØØ, S4-2 = OFF.
Local RAM	$ØØØØØØ-$Ø7FFFF	When S4-2 = ON (closed).

TABLE 3-2. LOCAL MEMORY MAP (cont.)

Devices	Address	Comments
Control Status Register	$FDØØØØ	
Auxiliary RAM/ROM	$F2ØØØØ - $F3FFFF	
ROM	$FØØØØØ - $F1FFFF	
Alternate Local RAM	$E8ØØØØ - $EFFFFF	When bit 2 of the address mapping switch is open.
VMEbus	$Ø8ØØØØ - $EFFFFF	If local RAM is mapped at Ø, switch S4-2 = ON.
	$ØØØØØØ - $E7FFFF	If local RAM is mapped at E8ØØØØØ, switch S4-2 = OFF.
Local RAM	$ØØØØØØ - $Ø7FFFF	When bit 2 of the address mapping switch is closed.

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CHAPTER 4
FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides the overall block diagram level description for the SBC.

4.2 GENERAL DESCRIPTION

The SBC is a single board computer based on a double-high VME board. It is a medium performance, low cost CPU with 512K bytes of on-board RAM shared with the VMEbus, two serial ports, a parallel/printer port, VMEbus interface, two sockets to support 32K x 8 or 64K x 8 EPROMs, and two additional sockets which can support either 2K x 8 or 8K x 8 EEPROMs; 2K x 8, 8K x 8, or 32K x 8 static RAMs; or 32K x 8 or 64K x 8 EPROMs. The SBC has system controller functions, an interrupt handler, and a level 3 bus arbitrator. In the VME1Ø4 version, the SBC supports the I/O channel interface. In the VME1Ø6 version, the SBC supports four 5-1/4 inch floppy disk drives. In the VME1Ø7 version, the SBC supports the full SCSI bus as defined by ANSI Specification X3T9.2. The SBC is capable of stand-alone operation with the addition of a power supply and a terminal.

4.3 MPU

The MC68Ø1Ø microprocessor and the supporting circuitry are designed to operate at 1Ø MHz.

4.4 RAM

The SBC has 16 ZIP package 256K x 1 DRAM devices to provide 512K bytes of RAM. Read operations are done with zero wait cycles. Write operations are done at one wait cycle maximum.

4.5 REFRESH

CAS before RAS refresh cycles are utilized, employing the refresh address counters internal to the DRAM devices. Every 15 microseconds a refresh cycle is run, supplying a CAS pulse, followed by a RAS pulse. In this mode, all other pins on the RAM devices are ignored.

4.6 LOCAL RAM ACCESSES

Local RAM can be user selected to reside at either address $ØØØØØØ or $E8ØØØØ by setting switch position 2 of the address mapping and configuration switch to closed or open.

4.7 VMEbus RAM ACCESSES

The RAM is also mapped to the VMEbus anywhere from $ØØØØØØ to $EFFFFF in 512K-byte increments. It responds to address modifier codes for:

1. Standard Supervisory Program Accesses (3E).
2. Standard Supervisory Data Accesses (3D).
3. Standard Non-Privileged Program Accesses (3A).
4. Standard Non-Privileged Data Accesses (39).

It will also appear in the local map at the same address.

4.8 EPROM SOCKETS

There are two industry standard JEDEC 28-pin sockets to support either 32K x 8 or 64K x 8 EPROMs, selectable by setting one jumper. Accesses are with "Ø" wait cycle using 25Ø nanosecond or faster devices.

4.9 AUXILIARY SOCKETS

There are two industry standard JEDEC 28-pin sockets that can be jumpered to support 2K x 8, 8K x 8, or 32K x 8 static RAMs. This includes the static RAM devices available with the internal battery and real time clock. They also support 2K x 8, 8K x 8 EEPROMs and 32K x 8 or 64K x 8 EPROMs.

NOTE: When using EEPROMS, re-access times must be software controlled.

When using EEPROMS or battery back-up static RAMs, they can be write protected after the code has been loaded by removing the jumper pin between J9(7-9) or J9(8-1Ø). With these jumpers pins removed, the RAMS cannot be changed by a software runaway. This feature is implemented in PCB Revision C VME1Ø5/1Ø6/1Ø7 and PCB Revision B VME1Ø4 modules.

4.1Ø TIMERS

There are three timers locally on the SBC.

4.1Ø.1 MC6823Ø Timer

There is a 24-bit timer provided by the MC6823Ø. The source for it's clock is pin 4Ø, which is 8 MHz. Refer to Motorola Publication ADI-86Ø for more details on this part and its operation.

4.1Ø.2 Local Bus Timer

There is a local bus timer. It is a timer used to time local bus events. It runs freely any time the local address strobe signal is in the true (low) state. It is disabled when a local to VMEbus access is detected or when address strobe again goes false. The time duration is fixed and is approximately 115 microseconds. The timer may be disabled by installing a jumper. Refer to section 2.3.1.1Ø for jumper details.

4.1Ø.3 Watchdog Timer

There is a watchdog timer which, when enabled through software, runs freely until reset by software. The timer's purpose is to restore the system when running away on a software problem, or when the VMEbus is not granted for extremely long periods of time. The watchdog timer is enabled by writing a "Ø" to CSR bit Ø and is reset by writing CSR bit Ø to a "1", then returning it to a "Ø". To disable the timer, CSR bit Ø is written to a "1" and left a "1". The default on power up is the timer disabled. The watchdog timer's timing interval is 15 milliseconds. If it should timeout, then it causes System Reset to be driven.

4.11 ADDRESS SWITCH REGISTER (ASR)

This is a 16-bit read only register which contains setup and status information. The two following charts provide the bit definitions.

Bit	Definition
Ø	Address Mapping and Configuration Switch Position 3.
1	Address Mapping and Configuration Switch Position 4.
2	Address Mapping and Configuration Switch Position 5.
3	Address Mapping and Configuration Switch Position 6.
4	Address Mapping and Configuration Switch Position 7.
5	Address Mapping and Configuration Switch Position 8.
6	Conflict Bit - Low True.
7	Local Timeout Bit - Low True.
8	VMEbus Error Bit (Local accesses only) - Low True.
9	Address Mapping and Configuration Switch Position 2.
1Ø	Board ID Bit (see below).
11	Board ID Bit (see below).
12	Board ID Bit (see below).
13	SCSI Interrupt - Low True (VME1Ø7 only).
14	Abort Flag - High True.
15	Arbitration Flag - High True (VME1Ø7 only).

ASR Bit	Board ID Bits 12	11	1Ø	Device (SBC)
Level	1	Ø	Ø	VME1Ø4
	1	Ø	1	VME1Ø5
	1	1	Ø	VME1Ø6
	1	1	1	VME1Ø7

Bits 6, 7, 8, and 14 are reset to the untrue state when the ASR is read. Bit 15 is reset by setting the Busy Interrupt Enable bit (PB2 of the MC6823Ø) to low (VME1Ø7 only). All other bits may be read without disturbing the contents.

4.12 CONTROL STATUS REGISTER

All bits are readable and writable locally and readable from the VMEbus. The lower eight bits cannot be written from the VMEbus. The bits are all defaulted to a "1" on power up or reset. The following chart defines the bit usage.

Bit	Usage	Comments
Ø	Watchdog Timer Control	" Ø" = Enable, " 1" = Reset/Disable
1	User Defined	VME1Ø5, VME1Ø6, VME1Ø7
1	I/O Channel Reset	VME1Ø4 " Ø" = Reset I/O Channel
2	Address Modifier 3	Address modifiers 3 and 5 are driven
3	Address Modifier 5	by these two bits.
4	User Defined	
5	System Fail	A " 1" drives SYSFAIL on VMEbus.
6	Disable Interrupts	This bit, when a " 1" disables all interrupts.
7	User Defined	
8	CSR IRQ 2, bit Ø	A " Ø" written to CSR bits 8, 9,
9	CSR IRQ 2, bit 1	or 1Ø causes a level 2 local
1Ø	CSR IRQ 2, bit 2	interrupt to be generated if interrupts are enabled.
11	CSR IRQ 7	A " Ø" written causes local level 7 IRQ.
12	VME Override	Refer to section 4.12.1.
13	User Defined	
14	User Defined	
15	User Defined	

4.12.1 VME Override Bit

Another bus master may make fast transfers of blocks of data to the local RAM by resetting the VME override bit (bit 12 in the CSR) to a "Ø". At this point, the local processor is suspended and held off the local bus for an unlimited time (until bit 12 is set back to a "1"). The local processor will then resume exactly where it stopped. Interrupts will not be serviced during this time.

This option allows minimum time transfers to the local RAM by removing arbitration time and the time the local processor normally would use to finish the instruction in process. In normal operation, a first off-board access would take approximately 65Ø to 12ØØ nanoseconds and possibly longer if certain instructions were being executed at the time. Very fast occurring sequential accesses would each take 12ØØ nanoseconds, because the local processor will always take a cycle for itself.

With the VME override bit reset to "Ø", each off-board access will be approximately 65Ø nanoseconds. This bit must never be written to a "Ø" by the local processor.

4.13 SERIAL PORTS

Two serial ports are provided by the Z853Ø Serial I/O device. The Z853Ø has a recharge/stabilization time needed between accesses. This must be accounted for in software. Consecutive accesses to the part must be separated by 16ØØ nanoseconds. This can be accomplished by inserting 5 NOP instructions or calculating the time the instructions between accesses will use and assuring they will leave 16ØØ nanoseconds recharge time. The following chart provides the pin definitions of the Z853Ø.

Pin	Mnemonic	Usage
5	INT	Serial Port IRQ
6	IEO	Unused, No Connection
7	IEI	Unused, Pulled High
8	INTACK	Unused, Pulled High
1Ø	W/REQA	Unused, No Connection
11	SYNCA	Unused, Pulled High
12	RTXDA	Receive Clock, Input, Port A
13	RXDA	Receive Data Input, Port A
14	TRXCA	Transmit Clock Output, Port A
15	TXDA	Transmit Data Output, Port A
16	DTR/REQA	Output, High Three-state Master and Slave Drivers
17	RTSA	Output, High Selects Master, Low Selects Slave Drivers
18	CTSA	Unused, Pulled High

19	DCDA	Unused, Pulled High
2Ø	PCLK	Clock Input, 4 MHz Clock Signal
21	DCDB	DCD Input, Port B
22	CTSB	CTS Input, Port B
23	RTSB	RTS Output, Port B (Must be Low to Output Data on Pin 25)
24	DTR/REQB	DTR Output, Port B
25	TXDB	Transmit Data Output, Port B
26	TRXCB	Transmit Clock, Port B, Input or Output
27	RXDB	Receive Data Input, Port B
28	RTXCB	Receive Clock Input, Port B
29	SYNCB	Unused, Pulled High
3Ø	W/REQB	Unused, No Connection

The following chart provides the memory map of the serial port registers.

Channel A	$FE4ØØ7	Data Register 8
	$FE4ØØ5	Command Register Ø
Channel B	$FE4ØØ3	Data Register 8
	$FE4ØØ1	Command Register Ø

4.13.1 RS-485 Port

Port A of the Z853Ø uses RS-485 drivers and receivers. The RS-485 signals are routed to P2. An external cable may be connected to P2 and the user must make a crossover cable to convert from the cable pinout of P2 on the SBC unit to the pinout of the user's serial network. The connector that is used to interface to the RS-485 network should take shielding into consideration.

The RS-485 port can be configured by software to be either master or slave, with the RTSA bit. Also, the DTR/REQA bit may be used to enable/disable the RS-485 drivers. Table 4-1 provides the possible configurations for the RS-485 port.

TABLE 4-1. RS-485 PORT CONFIGURATIONS

DRT/REQA	RTSA	Signal	Usage
Ø	Ø	S1+/-	TXDA drives S1+/-
		S2+/-	S2+/- drives RXDA
		S3+/-	TRXCA drives S3+/-
		S4+/-	S4+/- drives RTXCA
Ø	1	S1+/-	S1+/- drives RTXCA
		S2+/-	TXDA drives S2+/-
		S3+/-	RXDA drives S3+/-
		S4+/-	TRXCA drives S4+/-
1	Ø	S1+/-	OFF
		S2+/-	S2+/- drives RXDA
		S3+/-	OFF
		S4+/-	S4+/- drives RTXCA
1	1	S1+/-	S1+/- drives RTXCA
		S2+/-	OFF
		S3+/-	S3+/- drives RXDA
		S4+/-	OFF

Resistor XR1 is used for termination. It should be installed in the RS-485 units at the ends of the net. Any units in the middle of the net should have XR1 removed.

4.13.2 RS-232 Port

Port B is a synchronous/asynchronous RS-232C port accessed through a DB-25 connector on the front panel of the SBC. It supports asynchronous baud rates from 5Ø to 96ØØ baud. It supports synchronous baud rates from 5Ø to 64K baud. It is jumper configurable to appear as a DTE (to terminal) or DCE (to modem) device with the use of on-board jumpers.

4.14 PARALLEL/PRINTER PORT

The Parallel/Printer Port is implemented with a MC6823Ø. It provides all the necessary signals to support the Centronics printer interface. It is accessed from the front panel through a Centronics 36-pin connector. It also has a bit to allow it to be bidirectional and used as a parallel I/O port. The clock source for the MC6823Ø is on pin 4Ø, clock input, and is 8 MHz. The following charts show the bit definitions in the MC6823Ø.

Bit	Usage (VME1Ø4/1Ø5/1Ø6/1Ø7)
PAØ	Printer Data Bit 1
PA1	Printer Data Bit 2
PA2	Printer Data Bit 3
PA3	Printer Data Bit 4
PA4	Printer Data Bit 5
PA5	Printer Data Bit 6
PA6	Printer Data Bit 7
PA7	Printer Data Bit 8

The above bits are bidirectional. They are driven to the connector by an F24Ø, whose direction is controlled by bit PC4. Care must be taken to never have PC4 in the low state while PAØ through PA7 are configured as outputs.

When changing direction from output to input, first change the direction of PAØ through PA7 from output to input, and then change PC4 from high to low. When changing from input to output, first change PC4 from low to high, then change PAØ through PA7 from inputs to outputs.

Bit	Usage (VME1Ø4/1Ø5/1Ø6/1Ø7)
H1	Printer Acknowledge
H2	Printer Data Strobe
H3	Printer Fault
H4	Printer Input Prime
PCØ	Printer Busy
PC1	Printer Out
PC2	Printer Select
PC3	Timer Interrupt
PC4	Parallel Port Direction
PC5	Printer Interrupt
PC6	Printer Interrupt Acknowledge
PC7	Timer Interrupt Acknowledge

Bit	Usage VME1Ø4/1Ø5	Usage VME1Ø6	Usage VME1Ø7
PBØ	Not Used	Door Open	Not Used
PB1	Not Used	double Density	Busy Interrupt Enable
PB2	Not Used	SSO	SCSI Interrupt Enable
PB3	Not Used	Drive Select 3	Not Used
PB4	Not Used	Drive Select 2	Not Used
PB5	Not Used	Drive Select 1	Not Used
PB6	Not Used	Drive Select Ø	Not Used
PB7	Not Used	Motor On	Not Used

4.15 BUS REQUESTER

The Bus Requester requests VMEbus mastership on any one of the four bus request levels (user configurable by jumpers), and supports the daisy-chain on bus grant. The bus requester operates in the Release-On-Request (ROR) mode with early release and request bus mastership only if the MC68Ø1Ø microprocessor attempts a VMEbus access and does not already have the bus mastership. The bus mastership is released when a bus request is received on any level and (1) there is no cycle in process, or (2) if the current cycle has passed an initial threshold of its current cycle. If the SBC is also the System Controller, the Bus Requester must be set to level 3.

4.16 INTERRUPT HANDLER

The Interrupt Handler receives up to nine interrupt requests from the VMEbus on IRQ1 through IRQ7, SYSFAIL, and AC FAIL. IRQ1 through IRQ7 and SYSFAIL may be selectively disabled by removing the jumper for the interrupt not desired. AC FAIL is always monitored, however SYSFAIL is only enabled if the SBC is the System Controller.

Local interrupts are monitored for CSR, Printer Port, Floppy Disk, Serial Port, Timer, I/O Channel, SCSI, and ABORT.

The Printer Port, Timer, and VMEbus IRQ1 through IRQ7 use an IACK cycle to get the interrupt vector from the interrupting device. All other use the auto vector feature of the MC68Ø1Ø.

All interrupts are disabled when CSR bit 6 is a "1". The default on power up is to disable all interrupts.

The following chart provides the interrupt source, its level, vector source, and vector number.

Interrupt Source	Level	Vector Source	Vector Number
CSR	7	Auto Vector	
ABORT	7	Auto Vector	
AC FAIL	7	Auto Vector	
Timer	6	Timer Device	Programmable
I/O Channel	5	I/O Channel Vector RAM	Programmable
Serial Port	5	Auto Vector	
I/O Channel	4	I/O Channel Vector RAM	Programmable
Printer Port	3	Timer Device	Programmable
Floppy Disk	2	Auto Vector (VME1Ø6 only)	
SCSI	2	Auto Vector (VME1Ø7 only)	
CSR	2	Auto Vector	
SYS FAIL	2	Auto Vector	
I/O Channel	2	I/O Channel Vector RAM	Programmable
I/O Channel	1	I/O Channel Vector RAM	Programmable
VMEbus IRQ7	7	VMEbus	Supplied
VMEbus IRQ6	6	VMEbus	Supplied
VMEbus IRQ5	5	VMEbus	Supplied
VMEbus IRQ4	4	VMEbus	Supplied
VMEbus IRQ3	3	VMEbus	Supplied
VMEbus IRQ2	2	VMEbus	Supplied
VMEbus IRQ1	1	VMEbus	Supplied

Upon receipt of a level 7 local (auto vector) interrupt, there are three possible causes. The ASR and CSR must be read to determine what action to take.

1. Abort bit set: The ABORT pushbutton has been pressed. Handle accordingly, monitor the bit until it is cleared. When cleared, return from interrupt handler.
2. CSR bit 11 is set to "Ø": Interrupt caused by CSR being written to, handle according to operating system definition.
3. Neither of the above bits were set: This is an AC FAIL, process accordingly.

Upon receipt of a level 2 local (auto vector) interrupt, there are two possible causes. The CSR must be read to determine what action to take.

1. CSR bits 8, 9, or 1Ø are set to a "Ø": This is a CSR interrupt, handle according to the operating system definition.

2. CSR bits 8, 9, and 1Ø are all set to "1: This is a SYSFAIL interrupt.

4.17 SYSTEM CONTROLLER FUNCTIONS

4.17.1 Bus Arbitrator

A single level bus arbitrator is incorporated. Any time a level 3 bus request is present and bus busy is inactive, a bus grant will issued. If the SBC is System Controller, this arbitrator is used and all modules in the system must be on Bus Request Level 3.

4.17.2 Reset Generator

On power up or upon pressing the reset button, system reset is driven on the VMEbus.

4.17.3 System clock

A symmetrical 16 MHz system clock is provided.

4.17.4 VMEbus Timeout

The bus timeout timer asserts BERR* if a VMEbus cycle exceeds 1Ø5 microseconds. This function can be disabled by installing jumper J4.

4.18 BUS ERROR

There are three possible causes of a Bus Error. First, read the ASR and check the following.

1. Local timeout bit set: The processor was attempting to access a local resource on the SBC and DTACK was not asserted in 115 microseconds.
2. VMEbus error bit set: The processor was attempting to access a location on VMEbus and received a BERR instead of a DTACK.
3. If neither of the above bits were set, read the status register on the stack. If the TAS bit is set, a TAS instruction was attempted to a VME address at the same time another master was attempting to access a local on-board resource. A hardware rerun sequence was attempted, but on a TAS instruction, and the bus error was taken instead. Rerun the TAS instruction in software.

4.19 I/O CHANNEL INTERFACE (VME1Ø4 ONLY)

The I/O Channel Interface provides an eight-bit asynchronous data communication path between the MPU and up to 16 I/O channel modules. The I/O Channel interface signals are located on connector P2. The

user can connect a 5Ø-pin cable from P2 to these I/O modules to provide a private I/O for the VME1Ø4. Note that power for the I/O Channel boards is not supplied by the VME1Ø4.

Twelve address lines provide 4K bytes of memory mapped I/O for address placement on the I/O Channel. This I/O is mapped at odd bytes starting at address $FE6ØØ1. The following equation may be used to determine the VME1Ø4 address of an I/O Channel device.

VME1Ø4 Address = $FE6ØØ1 + 2 x (I/O Channel address)

A 4 MHz free running clock provides a time base for general use.

There are four interrupts provided on open-collector lines to allow I/O modules to interrupt the MPU. These are serviced as vectored interrupts by the MPU. The following chart shows the I/O Channel interrupt levels at the MPU and the address of the corresponding vector. This write only vector address register must be loaded during initialization.

I/O Channel Interrupt Signal	I/O Channel Interrupt Level	Vector Register Address	MPU Interrupt Level
INT1*	1	$FE2ØØ3	1
INT2*	2	$FE2ØØ5	2
INT3*	3	$FE2ØØ9	4
INT4*	4	$FE2ØØB	5

Reset on the I/O Channel is driven by board reset and at any time CSR bit 1 is in the low (Ø) state.

For further I/O Channel information, refer to the I/O Channel Specification M68RIOCS.

4.2Ø FLOPPY DISK CONTROLLER (VME1Ø6 ONLY)

The Floppy Disk Controller supports FM and MFM data on four 5-1/4 inch floppy disk drives, using the Western Digital WD177Ø Floppy Disk Controller Chip.

4.2Ø.1 Register Map

All registers are byte wide and are mapped on odd bytes.

$FEØØØ1 - Status Register

$FEØØØ3 - Track Register

$FE0005 - Sector Register

$FE0007 - Data Register

4.21 SCSI CONTROLLER (VME107 ONLY)

The NCR5380 SCSI controller accommodates the Small Computer Systems Interface as defined by ANSI X3T9.2 committee (Revision 16 of the SCSI specification). The single ended, open-collector version of the SCSI bus is implemented. The controller supports arbitration, including reselection, and can operate in both the Initiator and Target mode. The bus device ID is software controlled.

All command/status interfacing and data transfers are performed through the NCR5380. When data is to be transferred or the SCSI bus is to be acquired, the information is sent to the protocol controller and it interrupts when processor intervention is required. When the SBC has been selected by another SCSI device (or data received) an interrupt occurs allowing the microprocessor to transfer data to RAM or act on being selected. The data is single buffered on the device.

The SBC also supports a pseudo DMA channel from the SCSI controller. In this mode the Z5380 is programmed to operate in the DMA mode and the processor then does either reads or writes to the Z5380 as fast as the SCSI bus is able to handle the transfers, or as fast as the MC68010 is able to provide or take data. Basically, the processor does the first half of a move instruction (for a write to SCSI) and waits for the SCSI to take the data to complete the move instruction. The processor then returns in it's software loop and does another move. Reads from the SCSI are similar. Interrupts or polling times are avoided.

4.21.1 Interrupts

The normal interrupts created by the NCR5380 are enabled by setting the MC68230 PB2 bit to a "1".

Additional provisions are made to allow interrupts of the processor when the SCSI bus has a bus free condition. This interrupt is enabled by setting the MC68230 PB1 bit to a "1". The MC68230 PB2 bit must also by a "1".

4.21.2 Register Map

All access to the SCSI are byte wide and on odd boundaries.

$FE6001 - Pseudo DMA Output Data Register (Write Only).

The Pseudo DMA Output Data Register is used to transfer data to the SCSI bus from the local bus in the Pseudo DMA mode. The DMA mode bit (FEØØ15, bit 1) must be set (1) and the Start DMA Send Register ($FE6Ø1B) must be written to before writing to this register.

$FE6ØØ3 - Unused.

$FE6ØØ5 - Unused.

$FE6ØØ7 - Unused.

$FE6ØØ8 - Unused.

$FE6ØØD - Input Data Register (Read Only).

The Input Data Register is a read only register that is used to read latched data from the SCSI bus. Data is latched either during a Pseudo DMA Target receive operation or during a Pseudo DMA Initiator receive operation. The DMA mode bit ($FE6Ø15, bit 1Ø must be set (1) before data can be latched in the Input Data Register. Parity checking is optional depending on the status of the Enable Parity Checking bit ($FE6Ø15, bit 5). Bit assignment in the Input Data Register is with SCSI DBØ at Data bit Ø up to SCSI DB7 at Data bit 7.

$FE6Ø11 - Normal Mode Output Data Register (Write Only).

The Output Data Register is a write only register that is used to send data to the SCSI bus in the normal mode (Non-Pseudo DMA). It is also used to assert the proper ID bits on the SCSI bus during the arbitration and selection phases.

$FE6Ø11 - Current SCSI Data Register (Read Only).

The Current SCSI Data Register is a read only register which allows the MPU to read the active SCSI data bus. This register is used for normal (Non-Pseudo DMA) reads of the SCSI bus.

Bit definition -- bit Ø = DBØ* through bit 7 = DB7*.

$FE6Ø13 - Initiator Command Register (Read or Write).

The Initiator Command Register is a read/write register which is used to assert certain SCSI bus signals, to monitor those signals, and to monitor the progress of bus arbitration.

Bit	Read	Write
Ø	Assert Data Bus	Same
1	Assert Attention	Same
2	Assert Select	Same
3	Assert Busy	Same
4	Assert Acknowledge	Same
5	LA	Different Enable (not used)
6	Arbitration in Progress	Test Mode
7	Assert Reset	Same

$FE6Ø15 - Mode Register (Read or Write).

The Mode Register is used to control the operation of the chip. It determines whether the SCSI Controller operates an an initiator or a target, whether parity is checked, and whether interrupts are generated on various conditions. It may be read to check the value of the internal control bits.

Bit	Usage
Ø	Arbitrate
1	DMA Mode
2	Monitor Busy
3	Enable EOP Interrupt
4	Enable Parity Interrupt
5	Enable Parity Checking
6	Target Mode
7	Block DMA Mode (not used)

$FE6Ø17 - Target Command Register (Read or Write).

When connected as a target device, the Target Command Register allows the MPU to control the SCSI bus information transfer phase and/or to assert REQ* (pin 2Ø) simply by writing to this register. The Target Mode bit ($FE6Ø15, bit 6) must be set (1) for bus assertion to occur. When connected as an initiator with DMA Mode true, $FE6Ø15 (bit 2) is set = 1. If the phase lines (I/O, C/D, and MSG) do not match the phase bits in the Target Command Register, a phase mismatch interrupt is generated when REQ* goes active. In order to send data as an initiator, the ASSERT I/O, ASSERT C/D, and ASSERT MSG bits must match the corresponding bits in the current SCSI Bus Status Register ($FE6Ø19). The ASSERT REQ bit (bit 3) has no meaning when operating as an initiator.

Bit	Usage
Ø	Assert I/O
1	Assert C/D
2	Assert MSG
3	Assert REQ
4	Unused
5	Unused
6	Unused
7	Unused

$FE6Ø19 - Select Enable Register (Write Only).

The Select Enable Register is a write only register which is used as a mask to monitor a single ID during a selection attempt. The simultaneous occurrence of the correct ID bit, BSYU false, and SEL true will cause an interrupt. This interrupt can be disabled by resetting all bits in this register. If the ENABLE PARITY CHECKING bit ($FE6Ø15, bit 5) is set (1), parity will checked during selection.

Bit definition -- Bit Ø = DB* through Bit 7 = DB7*.

$FE6Ø19 - Current SCSI Bus Status (Read Only).

The Current SCSI Bus Status Register is a read only register which is used to monitor seven SCSI bus control signals plus the data parity bit.

Bit	Usage
Ø	DBP*
1	SEL*
2	I/O*
3	C/D*
4	MSG*
5	REQ*
6	BSY*
7	RST*

$FE6Ø1B - Start DMA Send (Write Only).

This register is written to initiate a DMA send, from the local bus in the Pseudo DMA mode, to the SCSI bus, for either initiator or target role operation. The DMA mode bit must be set (1) prior to writing this register.

$FE6Ø1B - Bus and Status Register (Read Only).

The Bus and Status Register is a read only register which can be used to monitor the SCSI bus control signals not found in the Current SCSI Bus Status Register and six other status bits.

Bit	Usage
Ø	ACK*
1	ATN*
2	Busy Error
3	Phase Match
4	Interrupt Request Active
5	Parity Error
6	DMA Request
7	End of DMA

$FE6Ø1D - Start DMA Receive (Write Only).

This register is written to initiate a DMA receive, from the SCSI bus to the local bus in the Pseudo DMA mode, for target operation only. The DMA mode bit must be set (1) prior to writing this register.

$FE6Ø1D - Unused.

$FE6Ø1F - Start DMA Initiator Receive (Write Only).

This register is written to initiate a DMA receive, from the SCSI bus to the local bus in the Pseudo DMA mode for initiator operation only. The DMA mode bit must be set (1Ø and the Target Mode bit must be clear (Ø) prior to writing this register.

$FE6Ø1F - Reset Parity/Interrupt (Read Only).

Reading this register resets the Parity Error bit (bit 5), the Interrupt Request bit (bit 4), and the Busy Error bit (bit 2) in the Bus and Status Register (Read only, $FE6ØØB).

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CHAPTER 5
SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the connector pin signal descriptions, parts list with associated parts location diagram, and the schematic diagrams for the different versions of the SBC units.

5.2 INTERCONNECTION SIGNALS

The SBC interconnects with VMEbus through connector P1. Connector P2 interconnects the SBC with the RS-485 serial port interface and the floppy disk drive signals.

5.2.1 Connector P1

Connector P1 is a standard DIN triple row, 96-pin male connector. all Motorola VMEbus specifications are met by the SBC. Table 5-1 lists each pin connection, signal mnemonic, and signal characteristic for edge connector P1.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
A1-A8	DØØ-DØ7	DATA BUS (bits Ø-7) - Eight of 16 three-state bidirectional data lines that provide the data path between the data transfer bus master and slave.
A9	GND	GROUND
A1Ø	SYSCLOCK	SYSTEM CLOCK - A constant 16 MHz clock signal that is independent of processor speed or timing and is used as a timing reference.
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - A three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines DØ8 through D15.
A13	DSØ*	DATA STROBE Ø - A three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines DØØ through DØ7.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A14	WRITE*	WRITE ENABLE - Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation and a low level indicates a write operation.
A15	GND	GROUND
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - An open-collector driven signal generated by a data transfer bus slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
A17	GND	GROUND
A18	AS*	ADDRESS STROBE - This signal's falling edge is used to indicate that a valid address is on the address bus. AS* is an active low, TTL three-state signal.
A19	GND	GROUND
A2Ø	IACK*	INTERRUPT ACKNOWLEDGE - An open-collector driven input signal that indicates a VME interrupt acknowledge cycle. The VME system controller has been interrupted on one of seven levels and is now acknowledging the interrupt.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - IACKIN* and IACKOUT* form a daisy-chained acknowledge. IACKIN* input signal is connected directly to IACKOUT*.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - IACKIN* and IACKOUT* form a daisy-chained acknowledge. IACKOUT* output signal is connected directly to IACKIN*.
A23	AM4	ADDRESS MODIFIER (bit 4) - One of four input lines that provide additional information about the address bus, such as size, cycle type, and/or data transfer bus master identification.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A24	AØ7	ADDRESS BUS (bit 7) - One of 16 three-state input lines that specify an address in the memory map.
A25	AØ6	ADDRESS BUS (bit 6) - Same as AØ7 on pin A24.
A26	AØ5	ADDRESS BUS (bit 5) - Same as AØ7 on pin A24.
A27	AØ4	ADDRESS BUS (bit 4) - Same as AØ7 on pin A24.
A28	AØ3	ADDRESS BUS (bit 3) - One of 16 three-state input lines that specify an address in the memory map. During an interrupt acknowledge cycle, address bus lines AØ1 through AØ3 are used to indicate the interrupt level that is being acknowledged.
A29	AØ2	ADDRESS BUS (bit 2) - Same as AØ3 on pin A28.
A3Ø	AØ1	ADDRESS BUS (bit 1) - Same as AØ3 on pin A28.
A31	-12V	-12 Vdc POWER - Used by system logic circuits.
A32	+5V	+5 Vdc POWER - Used by system logic circuits.
B1	BBSY*	VMEbus BUSY - Open-collector driven signal generated by the current Data Transfer Bus (DTB) master to indicate that it is using the bus.
B2	NC	NOT CONNECTED.
B3	ACFAIL*	SYSTEM AC POWER FAIL - An open-collector driven signal which indicates that the AC input to the power supply is not being provided or the required input voltage level is not being met.
B4	BGØIN*	BUS GRANT Ø IN - The "bus grant in" and "bus grant out" form a daisy-chained bus grant. A grant received at the jumpered level indicates the module may become the bus master. The remaining three "bus grant in" lines are connected directly to their respective "bus grant out" lines.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B5	BGØOUT*	BUS GRANT Ø OUT - The "bus grant in" and "bus grant out" form a daisy-chained bus grant. When a "bus grant in" is received at the jumpered level and the MPU is not awaiting bus mastership, the "bus grant out" signal is true on the respective level.
B6	BG1IN*	BUS GRANT 1 IN - Same as BGØIN on pin B4.
B7	BG1OUT*	BUS GRANT 1 OUT - Same as BGØOUT on pin B5.
B8	BG2IN*	BUS GRANT 2 IN - Same as BGØIN on pin B4.
B9	BG2OUT*	BUS GRANT 2 OUT - Same as BGØOUT on pin B5.
B1Ø	BG3IN*	BUS GRANT 3 IN - Same as BGØIN on pin B4.
B11	BG3OUT*	BUS GRANT 3 OUT - Same as BGØOUT on pin B5.
B12-B15	BRØ*-BR3*	BUS REQUEST (bits Ø - 3) - These open-collector driven signals that are generated by requesters. These signals indicate that a data transfer bus master in the daisy-chain requires access to the bus.
B16-B19	AMØ-AM3	ADDRESS MODIFIER (bits Ø-3) - Same as AM4 on pin A23.
B2Ø	GND	GROUND
B21, B22	NC	NOT CONNECTED
B23	GND	GROUND
B24-B3Ø	IRQ7*-IRQ1*	INTERRUPT REQUEST (bits 7-1)- These signals are generated by an interrupter and carry the prioritized interrupt requests. Level 7 is the highest priority and level 1 the lowest.
B31	+5VSTBY	+5Vdc STANDBY - This line supplies +5 Vdc to devices requiring battery backup.
B32	+5V	+5 Vdc POWER - Used by system logic circuits.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C1-C8	DØ8-D15	DATA BUS (bits 8-15) - Eight of 16 three-state bidirectional data lines that provide the data path between the data transfer bus master and slave.
C9	GND	GROUND
C1Ø	SYSFAIL*	SYSTEM FAILURE - An open-collector driven signal that indicates a failure has occurred in the system. SYSFAIL* may be generated by any module on the VMEbus.
C11	BERR*	BUS ERROR - Open-collector driven signal generated by a slave. BERR* indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
C12	SYSRESET*	SYSTEM RESET - Open-collector driven signal which, when low, will cause the system to be reset.
C13	LWORD*	LONGWORD - A three-state driven signal specifying that the cycle is a byte/word transfer (when high) or a longword transfer (when low).
C14	AM5	ADDRESS MODIFIER (bit 5) - Same as AM4 on pin A23.
C15	A23	ADDRESS BUS (bit 23) - Same as AØ7 on pin A24.
C16	A22	ADDRESS BUS (bit 22) - Same as AØ7 on pin A24.
C17	A21	ADDRESS BUS (bit 21) - Same as AØ7 on pin A24.
C18	A2Ø	ADDRESS BUS (bit 2Ø) - Same as AØ7 on pin A24.
C19	A19	ADDRESS BUS (bit 19) - Same as AØ7 on pin A24.
C2Ø	A18	ADDRESS BUS (bit 18) - Same as AØ7 on pin A24.
C21	A17	ADDRESS BUS (bit 17) - Same as AØ7 on pin A24.
C22	A16	ADDRESS BUS (bit 16) - Same as AØ7 on pin A24.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C23	A15	ADDRESS BUS (bit 15) - Same as AØ7 on pin A24.
C24	A14	ADDRESS BUS (bit 14) - Same as AØ7 on pin A24.
C25	A13	ADDRESS BUS (bit 13) - Same as AØ7 on pin A24.
C26	A12	ADDRESS BUS (bit 12) - Same as AØ7 on pin A24.
C27	A11	ADDRESS BUS (bit 11) - Same as AØ7 on pin A24.
C28	A1Ø	ADDRESS BUS (bit 1Ø) - Same as AØ7 on pin A24.
C29	AØ9	ADDRESS BUS (bit Ø9) - Same as AØ7 on pin A24.
C3Ø	AØ8	ADDRESS BUS (bit Ø8) - Same as AØ7 on pin A24.
C31	+12V	+12 Vdc POWER - Used by system logic circuits.
C32	+5V	+5 Vdc POWER - Used by system logic circuits.

5.2.2 Connector P2

Connector P2 is a standard DIN triple row, 96-pin male connector. Table 5-2 lists the RS-485 serial port interface and floppy disk drive signals.

NOTE: Table 5-2 has multiple entries for certain pin numbers. In these cases, the appropriate version of the SBC (VME1Ø4, VME1Ø5, VME1Ø6, or VME1Ø7) is listed with the description.

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
A1	GND	GROUND **(VME1Ø4)**
A1	S1+	RS-485 TRANSMIT DATA (+) - This line is half of the balanced differential pair that includes S1+ and S1-. The pair is buffered to the RXDA pin of the Z853Ø when port A is configured as a slave, and it is buffered from the TXDA pin of the Z853Ø when port A is configured as a master. **(VME1Ø5/1Ø6/1Ø7)**
A2	GND	GROUND **(VME1Ø4)**
A2	S2+	RS-485 RECEIVE DATA (+) - This line is half of the balanced differential pair that includes S2+ and S2-. The pair is buffered from the TXDA pin of the Z853Ø when port A is configured as a slave, and it is buffered to the RXDA pin of the Z853Ø when port A is configured as a master. **(VME1Ø5/1Ø6/1Ø7)**
A3	GND	GROUND **(VME1Ø4)**
A3	S3+	RS-485 TRANSMIT CLOCK (+) - This line is half of the balanced differential pair that includes S3+ and S3-. The pair is buffered to the RTXCA pin of the Z853Ø (depends on J11) when port A is configured as a slave, and it is buffered from the TRXCA pin of the Z853Ø when port A is configured as a master. **(VME1Ø5/1Ø6/1Ø7)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A4	GND	GROUND **(VME1Ø4)**
A4	S4+	RS-485 RECEIVE CLOCK (+) - This line is half of the balanced differential pair that includes S4+ and S4-. The pair is buffered from the TRXCA pin of the Z853Ø when port A is configured as a slave, and it is buffered to the RTXCA pin of the Z853Ø (depends on J11) when port A is configured as a master. **(VME1Ø5/1Ø6/1Ø7)**
A5	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
A6	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
A7	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
A8	GND	GROUND **(VME1Ø4)**
A8	----	NOT USED. **(VME1Ø5/1Ø6)**
A8	DBØ*	DATA BUS BIT Ø (SCSI) - Least significant bit (LSB) of eight bidirectional data bus signals. This bit has the lowest priority during the Arbitration phase. **(VME1Ø7)**
A9	GND	GROUND **(VME1Ø4)**
A9	----	NOT USED. **(VME1Ø5/1Ø6)**
A9	DB1*	DATA BUS BIT 1 (SCSI) - One of eight bidirectional data bus signals. **(VME1Ø7)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A1Ø	GND	GROUND **(VME1Ø4)**
A1Ø	----	NOT USED. **(VME1Ø5/1Ø6)**
A1Ø	DB2*	DATA BUS BIT 2 (SCSI) - Same as DB1* on pin A9. **(VME1Ø7)**
A11	IOA11	I/O CHANNEL ADDRESS (bit 11) - One of 12 address lines from the SBC to the I/O Channel bus. **(VME1Ø4)**
A11	----	NOT USED. **(VME1Ø5/1Ø6)**
A11	DB3*	DATA BUS BIT 3 (SCSI) - Same as DB1* on pin A9. **(VME1Ø7)**
A12	IOA1Ø	I/O CHANNEL ADDRESS (bit 1Ø) - Same as IOA11 on pin A11. **(VME1Ø4)**
A12	----	NOT USED. **(VME1Ø5/1Ø6)**
A12	DB4*	DATA BUS BIT 4 (SCSI) - Same as DB1* on pin A9. **(VME1Ø7)**
A13	IOAØ8	I/O CHANNEL ADDRESS (bit Ø8) - Same as IOA11 on pin A11. **(VME1Ø4)**
A13	----	NOT USED. **(VME1Ø5/1Ø6)**
A13	DB5*	DATA BUS BIT 5 (SCSI) - Same as DB1* on pin A9. **(VME1Ø7)**
A14	IOAØ6	I/O CHANNEL ADDRESS (bit Ø6) - Same as IOA11 on pin A11. **(VME1Ø4)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A14	----	NOT USED. **(VME1Ø5/1Ø6)**
A14	DB6*	DATA BUS BIT 6 (SCSI) - Same as DB1* on pin A9. **(VME1Ø7)**
A15	IOAØ4	I/O CHANNEL ADDRESS (bit Ø4) - Same as IOA11 on pin A11. **(VME1Ø4)**
A15	----	NOT USED. **(VME1Ø5/1Ø6)**
A15	DB7*	DATA BUS BIT 7 (SCSI) - Most significant bit (MSB) of eight bidirectional data bus signals. This bit has the highest priority during the Arbitration phase. **(VME1Ø7)**
A16	IOAØ2	I/O CHANNEL ADDRESS (bit Ø2) - Same as IOA11 on pin A11. **(VME1Ø4)**
A16	----	NOT USED. **(VME1Ø5/1Ø6)**
A16	DBP*	DATA BUS PARITY (SCSI) - Data parity is odd. Use of parity is a system option. Parity is not valid during the Arbitration phase. **(VME1Ø7)**
A17	GND	GROUND **(VME1Ø4)**
A17	----	NOT USED. **(VME1Ø5/1Ø6)**
A17	SCSIGND*	SCSI GROUND - This line is a specified ground pin for the SCSI bus interface. **(VME1Ø7)**
A18	GND	GROUND **(VME1Ø4/1Ø7)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A18	----	NOT USED. **(VME1Ø5)**
A18	FDCSEL3*	FLOPPY DISK DRIVE SELECT (bit 3) - One of four signals used to indicate which floppy disk has been selected. **(VME1Ø6)**
A19	GND	GROUND **(VME1Ø4/1Ø7)**
A19	----	NOT USED. **(VME1Ø5)**
A19	INDEX*	INDEX - This signal indicates that the floppy disk has encountered an index hole on the disk. **(VME1Ø6)**
A2Ø	IOD7	I/O CHANNEL DATA (bit 7) - Most signification bit (MSB) of eight bidirectional data bus signals to the I/O Channel bus. **(VME1Ø4)**
A2Ø	----	NOT USED. **(VME1Ø5)**
A2Ø	FDCSELØ*	FLOPPY DISK DRIVE (bit Ø) - Same as FDCSEL3* on pin A18. **(VME1Ø6)**
A2Ø	TPWR	TERMINATOR POWER (SCSI) - +5 Vdc for external SCSI device terminators (when jumper J26 is installed). **(VME1Ø7)**
A21	IOD6	I/O CHANNEL DATA (bit 6) - One of eight bidirectional data bus signals to the I/O Channel bus. **(VME1Ø4)**
A21	----	NOT USED. **(VME1Ø5)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A21	FDCSEL1*	FLOPPY DISK DRIVE (bit 1) - Same as FDCSEL3* on pin A18. **(VME1Ø6)**
A21	GND	GROUND **(VME1Ø7)**
A22	IOD4	I/O CHANNEL DATA (bit 4) - Same as IOD6 on A21. **(VME1Ø4)**
A22	----	NOT USED. **(VME1Ø5)**
A22	FDCSEL2*	FLOPPY DISK DRIVE (bit 2) - Same as FDCSEL3* on pin A18. **(VME1Ø6)**
A22	GND	GROUND **(VME1Ø7)**
A23	IOD2	I/O CHANNEL DATA (bit 2) - Same as IOD6 on A21. **(VME1Ø4)**
A23	----	NOT USED. **(VME1Ø5)**
A23	MOTORON*	MOTOR ON - This signal commands the floppy disk motors to turn. **(VME1Ø6)**
A23	ATTN	ATTENTION (SCSI) - This signal is driven by the initiator that indicates the attention condition. **(VME1Ø7)**
A24	GND	GROUND **(VME1Ø4/1Ø7)**
A24	----	NOT USED. **(VME1Ø5)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A24	DIR*	DIRECTION - This signal indicates the direction of the next step on the floppy disk. **(VME106)**
A25	GND	GROUND **(VME104)**
A25	----	NOT USED. **(VME105)**
A25	FSTEP*	FLOPPY STEP - This pulse signal indicates to the selected floppy drive to advance to the next track. **(VME106)**
A25	BSY*	BUS BUSY (SCSI) - OR-tied signal that indicates that the bus is being used. **(VME107)**
A26	NC	NOT CONNECTED. **(VME104)**
A26	----	NOT USED. **(VME105)**
A26	WRITEDATA*	WRITE DATA - This signal indicates that write data is being written to the floppy disk drive selected. **(VME106)**
A26	ACK*	ACKNOWLEDGE (SCSI) - This signal is driven by an initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake. **(VME107)**
A27	NC	NOT CONNECTED. **(VME104)**
A27	----	NOT USED. **(VME105)**
A27	WRITEGATE*	WRITE GATE - Signal indicates that the floppy disk drive is being written to. **(VME106)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A27	RST*	RESET (SCSI) - OR-tied signal that indicates the reset condition. **(VME1Ø7)**
A28	S1+	RS-485 TRANSMIT DATA (+) - Same as S1+ on pin A1. **(VME1Ø4)**
A28	----	NOT USED. **(VME1Ø5)**
A28	TRØØ*	TRACK Ø - This signal indicates that the floppy disk drive selected is on track Ø. **(VME1Ø6)**
A28	MSG*	MESSAGE (SCSI) - Signal driven by the target during the Message phase. **(VME1Ø7)**
A29	S2+	RS-485 RECEIVE DATA (+) - Same as S2+ on pin A2. **(VME1Ø4)**
A29	----	NOT USED. **(VME1Ø5)**
A29	WPRT*	WRITE PROTECT - This signal indicates that the floppy disk has the write protect notch engaged. **(VME1Ø6)**
A29	SEL*	SELECT (SCSI) - Signal used by an initiator to select a target or by a target to reselect an initiator. **(VME1Ø7)**
A3Ø	S3+	RS-485 TRANSMIT CLOCK (+) - Same as S3+ on pin A3. **(VME1Ø4)**
A3Ø	----	NOT USED. **(VME1Ø5)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A3Ø	RAWDRDATA*	RAW DRIVE DATA - This signal indicates read data from the floppy disk drive in MFM or FM format. **(VME1Ø6)**
A3Ø	C/D*	CONTROL/DATA (SCSI) - This signal is driven by the target. It indicates whether control or data information is on the data bus. True (low) indicates CONTROL. **(VME1Ø7)**
A31	S4+	RS-485 RECEIVE CLOCK (+) - Same as S4+ on pin A4. **(VME1Ø4)**
A31	----	NOT USED. **(VME1Ø5)**
A31	SSØ	SIDE SELECT - This signal indicates which side of the floppy disk is selected. **(VME1Ø6)**
A31	REQ*	REQUEST (SCSI) - Signal driven by a target to indicate a request for a REQ/ACK data transfer handshake. **(VME1Ø7)**
A32	NC	NOT CONNECTED. **(VME1Ø4)**
A32	----	NOT USED. **(VME1Ø5)**
A32	DOPEN	DOOR OPEN - Signal indicates that the floppy disk door has been opened since last selected. **(VME1Ø6)**
A32	I/O*	INPUT/OUTPUT (SCSI) - Signal driven by a target which controls the direction of data movement on the bus. True (low) indicates input to; false (high) indicates output from the initiator. This signal is also used to distinguish between Selection and Reselection phase. **(VME1Ø7)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B1	+5V	+5 Vdc POWER - Used by system logic circuits. **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B2	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B3-B11	NC	NOT CONNECTED. **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B12	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B13	+5V	+5 Vdc POWER - Used by system logic circuits. **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B14-B21	NC	NOT CONNECTED. **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B22	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B23-B3Ø	NC	NOT CONNECTED. **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B31	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
B32	+5V	+5 Vdc POWER - Used by system logic circuits. **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
C1	INT4*	I/O CHANNEL INTERRUPT LEVEL 4 (Level 5 at MPU) - Input signal line from the I/O Channel bus. **(VME1Ø4)**
C1	S1-	RS-485 TRANSMIT DATA (-) - Return, refer to S1+ on pin A1. **(VME1Ø5/1Ø6/1Ø7)**
C2	INT3*	I/O CHANNEL INTERRUPT LEVEL 3 (Level 4 at MRU) - Input signal line from the I/O Channel bus. **(VME1Ø4)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C2	S2-	RS-485 RECEIVE DATA (-) - Return, refer to S2+ on pin A2. **(VME1Ø5/1Ø6/1Ø7)**
C3	INT2*	I/O CHANNEL INTERRUPT LEVEL 2 (Level 2 at MPU) - Input signal line from the I/O Channel bus. **(VME1Ø4)**
C3	S3-	RS-485 TRANSMIT CLOCK (-) - Return, refer to S3+ on pin A3. **(VME1Ø5/1Ø6/1Ø7)**
C4	INT1*	I/O CHANNEL INTERRUPT LEVEL 1 (Level 1 at MPU) - Input signal line from the I/O Channel bus. **(VME1Ø4)**
C4	S4-	RS-485 TRANSMIT CLOCK (-) - Return, refer to S4+ on pin A4. **(VME1Ø5/1Ø6/1Ø7)**
C5	IORES*	I/O CHANNEL RESET - Low true output signal to the I/O Channel bus. **(VME1Ø4)**
C5	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C6	XACK*	I/O CHANNEL ACKNOWLEDGE - Low true input signal from the I/O Channel bus. **(VME1Ø4)**
C6	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C7	CLK	4MHZ FREE RUNNING CLOCK - Output signal to the I/O Channel bus. **(VME1Ø4)**
C7	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C8	NC	NOT CONNECTED. **(VME1Ø4)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C8	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C9	NC	NOT CONNECTED. **(VME1Ø4)**
C9	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C1Ø	NC	NOT CONNECTED. **(VME1Ø4)**
C1Ø	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C11	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
C12	IOAØ9	I/O CHANNEL ADDRESS (bit Ø9) - Same as IOA11 on pin A11. **(VME1Ø4)**
C12	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C13	IOAØ7	I/O CHANNEL ADDRESS (bit Ø7) - Same as IOA11 on pin A11. **(VME1Ø4)**
C13	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C14	IOAØ5	I/O CHANNEL ADDRESS (bit Ø5) - Same as IOA11 on pin A11. **(VME1Ø4)**
C14	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C15	IOAØ3	I/O CHANNEL ADDRESS (bit Ø3) - Same as IOA11 on pin A11. **(VME1Ø4)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C15	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C16	IOAØ1	I/O CHANNEL ADDRESS (bit Ø1) - Same as IOA11 on pin A11. **(VME1Ø4)**
C16	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C17	IOAØØ	I/O CHANNEL ADDRESS (bit ØØ) - Same as IOA11 on pin A11. **(VME1Ø4)**
C17	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C18	STB*	I/O CHANNEL ADDRESS STROBE - Output signal to I/O Channel bus indicating addresses IOAØØ through IOA11 are valid. **(VME1Ø4)**
C18	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C19	WT*	I/O CHANNEL WRITE LINE - Output signal to the I/O Channel bus. **(VME1Ø4)**
C19	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C2Ø	GND	GROUND **(VME1Ø4)**
C2Ø	NC	NOT CONNECTED. **(VME1Ø5/1Ø6/1Ø7)**
C21	IOD5	I/O CHANNEL DATA (bit 5) - Same as IOD6 on pin A21. **(VME1Ø4)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C21	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C22	IOD3	I/O CHANNEL DATA (bit 3) - Same as IOD6 on pin A21. **(VME1Ø4)**
C22	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C23	IOD1	I/O CHANNEL DATA (bit 1) - Same as IOD6 on pin A21. **(VME1Ø4)**
C23	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C24	IODØØ	I/O CHANNEL DATA (bit ØØ) - Least signification bit (LSB) of eight bidirectional data bus signals to the I/O Channel bus. **(VME1Ø4)**
C24	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C25	GND	GROUND **(VME1Ø4/1Ø5/1Ø6/1Ø7)**
C26	NC	NOT CONNECTED. **(VME1Ø4)**
C26	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C27	NC	NOT CONNECTED. **(VME1Ø4)**
C27	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C28	S1-	RS-485 TRANSMIT DATA (-) - Return, refer to S1+ on pin A1. **(VME1Ø4)**

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C28	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C29	S2-	RS-485 RECEIVE DATA (-) - Return, refer to S2+ on pin A1. **(VME1Ø4)**
C29	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C3Ø	S3-	RS-485 TRANSMIT CLOCK (-) - Return, refer to S3+ on pin A1. **(VME1Ø4)**
C3Ø	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C31	S4-	RS-485 RECEIVE CLOCK (-) - Return, refer to S4+ on pin A1. **(VME1Ø4)**
C31	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**
C32	NC	NOT CONNECTED. **(VME1Ø4)**
C32	GND	GROUND **(VME1Ø5/1Ø6/1Ø7)**

5.2.3 Centronics Printer Connector J5 Interconnect Signals

Connector J5 is a 36-pin, right-angle connector used for connecting the SBC to the Centronics printer. Table 5-3 list the pin connection, signal mnemonic, and signal description for the connector.

TABLE 5-3. CONNECTOR J5 PRINTER CONNECTIONS

Pin Number	Signal Mnemonic	Signal Name and Description
1	DATSTB*	DATA STROBE - An active low output pulse used to clock data from the system to the printer.
2	PD1	PRINTER DATA (bit 1) - Output data to the printer.
3	PD2	PRINTER DATA (bit 2) - Output data to the printer.
4	PD3	PRINTER DATA (bit 3) - Output data to the printer.
5	PD4	PRINTER DATA (bit 4) - Output data to the printer.
6	PD5	PRINTER DATA (bit 5) - Output data to the printer.
7	PD6	PRINTER DATA (bit 6) - Output data to the printer.
8	PD7	PRINTER DATA (bit 7) - Output data to the printer.
9	PD8	PRINTER DATA (bit 8) - Output data to the printer.
1Ø	ACKNLG*	(PRINTER) ACKNOWLEDGE - A low level input signal that indicates that the next character may be sent.
11	BUSY	(PRINTER) BUSY - An input signal that indicates that the printer cannot receive data.
12	PAPOUT	PAPER OUT - Signal that indicates out of paper.
13	SELECT	SELECT - An input signal that indicates that the printer is selected.

TABLE 5-3. CONNECTOR J5 CENTRONICS PRINTER CONNECTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
14-18	NC	NOT CONNECTED.
19-3Ø	GND	GROUND
31	INPRIM*	INPUT PRIME - An output signal that clears the printer buffer and initializes the logic.
32	FAULT*	FAULT - An input signal that indicates a printer fault condition.
33-36	NC	NOT CONNECTED.

5.2.4 RS-232C Connector J13 Interconnect Signals

Connector J13 is a standard RS-232C DB-25 25-pin female connector. Table 5-4 list the pin connection, signal mnemonic, and signal description for the connector.

TABLE 5-4. CONNECTOR J13 RS-232C SERIAL PORT CONNECTIONS

Pin Number	Signal Mnemonic	Signal Name and Description
1	NC	NOT CONNECTED.
2	RXDB	RECEIVE DATA (channel B) - Data to be transmitted is furnished on this line to the modem from the terminal.
3	TXDB	TRANSMIT DATA (channel B) - Data that is demodulated from the receiver line is presented to the terminal by the modem.
4	RTSB	REQUEST TO SEND (channel B) - RTSB is supplied by the terminal to the modem when it is required to transmit a message. With RTSB off, the modem carrier remains off. When RTSB is turned on, the modem immediately turns on the carrier.
5	NC	NOT CONNECTED.
6	DSRB	DATA SET READY (channel B) - DSRB is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
7	GND	GROUND
8	DCDB	DATA CARRIER DETECT (channel B) - DCDB is sent by the modem to the terminal to indicate that a valid carrier is being received.
9-14	NC	NOT CONNECTED.
15	TXCB	TRANSMIT CLOCK (channel B) - This line clocks output data to the modem from the terminal.
16	NC	NOT CONNECTED.
17	RXCB	RECEIVE CLOCK (channel B) - This line clocks input data from a terminal to a modem.

TABLE 5-4. CONNECTOR J13 RS-232C SERIAL PORT CONNECTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
18-19	NC	NOT CONNECTED.
2Ø	DTRB	DATA TERMINAL READY (channel B) - This signal from the terminal to the modem indicates that the terminal is ready to send or receive data.
21-23	NC	NOT CONNECTED.
24	SYNCLKB	RS-232 SYSTEM CLOCK - This signal is used in some systems as a clock.
25	NC	NOT CONNECTED.

5.3 PARTS LIST

The parts location diagrams for the four versions of the SBC (VME1Ø4, VME1Ø5, VME1Ø6, and VME1Ø7) are illustrated in Figures 5-1 through 5-4, respectively. The reference designation, part number, and description for each component of the different versions of the SBC are listed in Tables 5-5 through 5-8, respectively. These lists reflect the latest issue of all SBC hardware at the time of the printing of this user's manual.

TABLE 5-5. VME1Ø4 PARTS LIST

Reference Designation	Motorola Part Number	Description
---	84-W845ØBØ1	Printed wiring board assembly, MVME1Ø4
C1,C2, C4-13, C16,C17, C19,C21, C22,C24, C26-29, C3Ø,C32, C34-46, C48-55, C57-61, C64-67	21NW9632AØ3	Capacitor, ceramic, Ø.1 MFD, 5Ø Vdc
C3,C23, C33	23NW9618A82	Capacitor, electrolytic, 22 MFD, 25 Vdc
C14	21NW97Ø9AØ8	Capacitor, ceramic, .1 MFD, 5Ø Vdc
C15,C25, C63	21SW992CØ14	Capacitor, ceramic, .Ø1Ø FD, 5Ø Vdc
C18,C2Ø, C56,C62	23NW9618A79	Capacitor, electrolytic, 1ØØ MFD, 25 Vdc
C31	21NW96Ø4A58	Capacitor, ceramic, 33Ø PFD, 5Ø Vdc
CR1	48NW9616AØ3	Diode, 1N4148/1N914
DL1	Ø1NW98Ø4C35	Delay module, 25Ø nsec
DL2	Ø1NW98Ø4C33	Delay module, 4Ø nsec
DL3	51NW9615T55	IC, DS1ØØØ-1ØØ

TABLE 5-5. VME1Ø4 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
DL5	Ø1NW9615U58	IC, DS1ØØØ-125
DL6	Ø1NW98Ø4C32	Delay module, 3Ø nsec
DS1,DS2	48NW9612A49	LED, red
DS3	48NW9612A59	LED, green
J5	28NW98Ø2G48	Connector, right-angle, 36-pin
---	Ø3SW993D3Ø8	Screw, PhFil, M3.Ø x Ø.5 x 8 (2 req'd)(use at J5)
J13	28NW98Ø2G8Ø	Connector, right-angle, 25-pin
P1,P2	28NW98Ø2E51	Connector, PWB, 3-row, 96-pin
---	Ø5NW9ØØ7A26	Eyelet, .Ø89 OD x .344 L (8 req'd)(used with P1 and P2)
R2,R5, R1Ø,R13, R18,R3Ø	51NW9626B56	Resistor network, nine 1ØK ohm
R3,R4	51NW9626BØ1	Resistor network, four 33 ohm
R6	51NW9626B42	Resistor network, five 33 ohm
R7	51NW9626A4Ø	Resistor network, five 1K ohm
R8	51NW9626A46	Resistor network, five 4.7K ohm
R9,R14	51NW9626B47	Resistor network, nine 22K ohm
R11	Ø6SW-124A89	Resistor, film, 1/4W, 5%, 47K ohm
R12	Ø6SW-124A81	Resistor, film, 1/4W, 5%, 22K ohm
R15	51NW9626A76	Resistor network, six 33Ø/47Ø ohm
R19	51NW9626A41	Resistor network, nine 4.7K ohm
R2Ø-22	51NW9626A49	Resistor network, seven 1ØK ohm

TABLE 5-5. VME1Ø4 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
R24	Ø6SW-124A53	Resistor, fixed, film, 1/2W, 5%, 1.5K ohm
R29,R33, R34	Ø6SW-124A37	Resistor, film, 1/4W, 5%, 33Ø ohm
R31	Ø6SW-96ØE18	Resistor, film, 1/8W, 1%, 15ØK ohm
R32	Ø6SW-962B22	Resistor, film, 1/8W, 5%, 1.ØM ohm
S1,S2	4ØNW98Ø1B7Ø	Switch, pushbutton, SPDT
---	38NW94Ø4C11	Cap, switch, black (1 req'd)(user at S1)
---	38NW94Ø4C12	Cap, switch, red (1 req'd)(user at S2)
S3,S4	4ØNW98Ø1A34	Switch, DIP, SPST, 8-position
U1-U8, U15-22	51NW9615S68	IC, MB81256-12PZ
U9,U12, U67	51NW9615M9Ø	IC, 74F245PC
U1Ø,U13	51NW9615R38	IC, SN74LS794N
U11,U14	51NW9615R36	IC, 74F543SPC
U23,U26	51NW9615K61	IC, 74F157PC
U24	51NW9615F79	IC, SN74S24ØN
U25,U42	51NW9615F85	IC, SN74S38N
U27	51AW5185BØ1	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U27)
U28	51AW4697B53	IC, Programmed

TABLE 5-5. VME1Ø4 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U28)
U29,U37, U38,U65	51NW9615GØ7	IC, SN74S244N
U3Ø	51AW4697B54	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U3Ø)
U31	51AW5185BØ3	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U31)
U32,U33, U92	51NW9615K73	IC, 74FØØPC
U34	51NW9615B59	IC, MC74Ø7P
U35,U66	51NW9615E93	IC, SN74LS14N
U36	51NW9615M11	IC, MC68Ø1ØL1Ø
---	Ø9-W4659B32	Socket, IC, SIL, 32-pin (2 req'd)(used at U36)
U39	51NW9615F31	IC, SN74S51N
U4Ø,U54, U62,U95	51NW9615J39	IC, 74F74PC
U41	51NW9615F38	IC, SN74LS393N
U43,U64	51NW9615FØ2	IC, SN74LS244N
U44,U49, U57	51NW9615R26	IC, SN74ALS645-1N
U45	51AW512ØB12	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U45)

TABLE 5-5. VME1Ø4 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U46,U94, U97	51NW9615C25	IC, SN74LS74AN
U47	51NW9615C24	IC, SN74LS32N
U5Ø,U52, U59	51NW9615H41	IC, SN74LS682N
U51	51NW9615E95	IC, SN74LS24ØN
U53	51AW512ØB25	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U53)
U55,U61, U79,U88	51NW9615K7Ø	IC, 74FØ8PC
U58	51AW4591C63	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U58)
U6Ø	51NW9615B65	IC, MC1455P1
U68	51NW9615K65	IC, 74F64PC
U69,U83	51NW9615K66	IC, 74F32PC
U71,U8Ø, U87,U1Ø2	51NW9615C22	IC, SN74LSØ8N
U72	51AW5185BØ4	IC, Programmed PROM
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U72)
U73	51NW9615R69	IC, MC6823ØP8
---	Ø9NW9811A26	Socket, IC, DIL, 48-pin (1 req'd)(used at U73)
U74	51NW9615C6Ø	IC, MC3456P

TABLE 5-5. VME1Ø4 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U75	51NW9615H38	IC, SN75175N
U81	51NW9615H37	IC, SN75174N
U82,U91	51NW9615K71	IC, 74FØ4PC
U84	51NW9615R68	IC, Z853ØAPC
---	Ø9-W4659B2Ø	Socket, IC, SIL, 2Ø-pin (2 req'd)(used at U84)
U85	51NW9615C21	IC, SN74LSØ4N
U86	51NW9615D93	IC, SN74S3ØN
U9Ø,U96	51NW9615S83	IC, MC1454Ø6P
U93	51NW9615K69	IC, 74F1ØPC
U98	51AW4591C64	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U98)
U99,U1Ø4	51NW9615KØ9	IC, SN74ALS244AN
U1ØØ	51NW9615F35	IC, SN74LS21N
U1Ø1	51NW9615K72	IC, 74FØ2PC
U1Ø3	51NW9615N8Ø	IC, MCM2Ø16HN-7Ø
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U1Ø3)
U1Ø5	51AW512ØB24	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U1Ø5)
U1Ø6	51AW4591C65	IC, Programmed

TABLE 5-5. VME1Ø4 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	Ø9NW9811A27	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U1Ø6)
U1Ø7	51AW4697B67	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U1Ø7)
U1Ø8	51NW9615E96	IC, SN74LS245
XR1	51NW9626A94	Resistor network, four 12Ø ohm
---	Ø9NW9811A9Ø	Socket, IC, SIL, 8-pin (1 req'd)(use at XR1)
Y1	48AW1Ø15BØ7	Crystal oscillator, 16.Ø MHz
Y2	48AW1Ø15BØ3	Crystal oscillator, 2Ø.Ø MHz
---	Ø9NW9811A46	Socket, crystal oscillator (2 req'd)(use at Y1 and Y2)
---	47NW94Ø5A28	Jackpost, assembly
---	29NW98Ø5B17	Jumper, insulated, shorting (28 req'd)[use at J1(1-2)(5-6)(7-8) (9-11)(1Ø-12),J2(5-6),J4(1-2),J6(2-3), J7(1-2)(3-4)(5-6)(7-8)(9-1Ø)(11-12) (13-14),J11(1-2)(3-4)(5-6)(7-8), J12(1-2),J16(1-2)(3-4)(5-6)(7-8)(9-1Ø) (11-13)(12-14),J25(1-2)]
---	29NW98Ø5B44	Jumper, 2-pin (1 req'd)[use at J24(1-2)]
---	67NW9415A17	Kit, 6 component, ejector handle
---	64-W5111BØ1	Panel, front, VME1Ø4/1Ø5/1Ø6/1Ø7
---	29NW98Ø5CØ7	Pin, Ø.Ø25-inch square, auto-insert (92 req'd)[use at J1(1-12),J2(1-6),J3 (1-2),J4(1-2),J6(1-3),J7(1-14),J8(1-3), J9(1-1Ø),J11(1-8),J12(1-2),J14(1-2), J15(1-8),J16(1-14),J25(1-3),J27(1-3)]

TABLE 5-5. VME1Ø4 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	33-W5Ø89B46	Nameplate, MVME1Ø4 (1 req'd)
---	33-W5Ø89BØ1	Nameplate, Motorola logo (1 req'd)
---	Ø9-W4659B14	Socket, IC, SIL, 14-pin (8 req'd)(use at XU48, XU56, XU63, XU7Ø)
---	42NW94Ø1B14	Screw, captive collar (2 req'd)
---	Ø3NW9ØØ4B48	Screw, captive, M2.5 (2 req'd)

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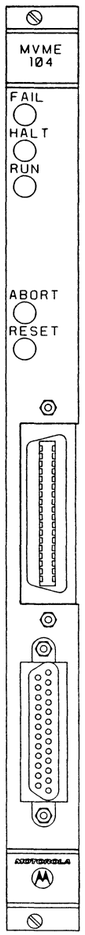
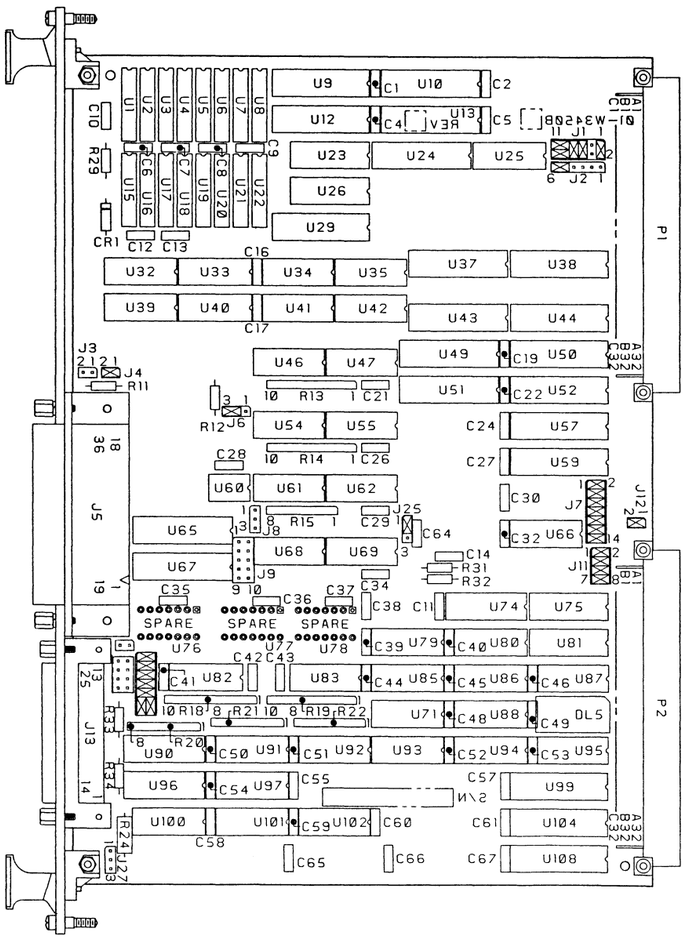
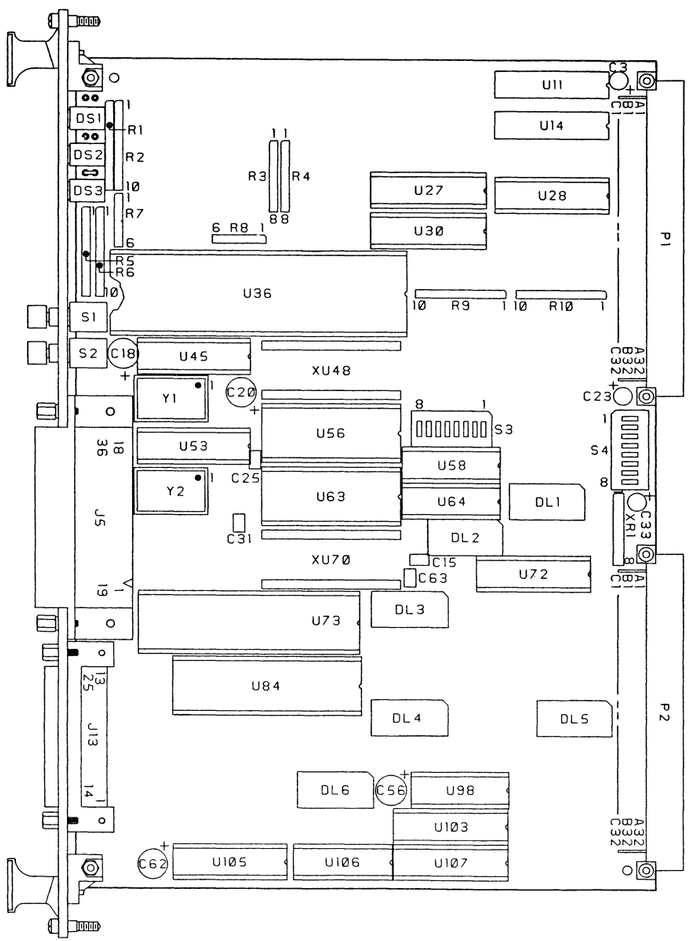


Front
Panel



VME1Ø4 with components removed for clarity.



VME1Ø4 with components removed for clarity.

FIGURE 5-1. MVME1Ø4 PARTS LOCATION DIAGRAM

TABLE 5-6. VME1Ø5 PARTS LIST

Reference Designation	Motorola Part Number	Description
---	84-W8438BØ1	Printed wiring board assembly, MVME1Ø5/1Ø6/1Ø7
C1,C2, C4-13, C16,C17, C19,C21, C24,C26, C27-3Ø, C32,C34, C38-56, C58-61, C64	21NW9632AØ3	Capacitor, ceramic, Ø.1 MFD, 5Ø Vdc
C3,C23, C33	23NW9618A82	Capacitor, electrolytic, 22 MFD, 25 Vdc
C14	21NW97Ø9AØ8	Capacitor, ceramic, .1 MFD, 5Ø Vdc
C15,C25, C63	21SW992CØ14	Capacitor, ceramic, .Ø1Ø FD, 5Ø Vdc
C18,C2Ø, C62	23NW9618A79	Capacitor, electrolytic, 1ØØ MFD, 25 Vdc
C31	21NW96Ø4A58	Capacitor, ceramic, 33Ø PFD, 5Ø Vdc
CR1	48NW9616AØ3	Diode, 1N4148/1N914
DL1	51NW9615UØ4	IC, DS1ØØØ-25Ø
DL2,DL6	Ø1NW98Ø4C32	Delay module, 3Ø nsec
DL3	51NW9615T55	IC, DS1ØØØ-1ØØ
DS1,DS2	48NW9612A49	LED, red
DS3	48NW9612A59	LED, green
J5	28NW98Ø2G48	Connector, right-angle, 36-pin
---	Ø3SW993D3Ø8	Screw, PhFil M3.Ø x Ø.5 x 8 (2 req'd)(use at J5)

TABLE 5-6. VME1Ø5 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
J13	28NW98Ø2G8Ø	Connector, right-angle, 25-pin
P1,P2	28NW98Ø2E51	Connector, PWB, 3-row, 96-pin
---	Ø5NW9ØØ7A26	Eyelet, .Ø89 OD x .344 L (4 req'd)(use with P1 and P2)
R2,R5, R1Ø,R13, R15,R18, R22,R3Ø	51NW9626B56	Resistor network, nine 1ØK ohm
R3,R4	51NW9626BØ1	Resistor network, four 33 ohm
R6	51NW9626B42	Resistor network, five 33 ohm
R7	51NW9626A4Ø	Resistor network, five 1K ohm
R8	51NW9626A46	Resistor network, five 4.7K ohm
R9,R14	51NW9626B47	Resistor network, nine 22K ohm
R11	Ø6SW-124A89	Resistor, film, 1/4W, 5%, 47K ohm
R12	Ø6SW-124A81	Resistor, film, 1/4W, 5%, 22K ohm
R19	51NW9626A41	Resistor network, nine 4.7K ohm
R21	51NW9626A49	Resistor network, seven 1ØK ohm
R24	Ø6SW-125A53	Resistor, fixed, film, 1/2W, 5%, 1.5K ohm
R29,R33, R34	Ø6SW-123A37	Resistor, film, 1/4W, 5%, 33Ø ohm
R31	Ø6SW-96ØE18	Resistor, film, 1/8W, 1%, 15ØK ohm
R32	Ø6SW-962B22	Resistor, film, 1/8W, 5%, 1.ØM ohm
S1,S2	4ØNW98Ø1B7Ø	Switch, pushbutton, SPDT
---	38NW94Ø4C11	Cap, switch, black (1 req'd)(user at S1)

TABLE 5-6. VME1Ø5 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	38NW94Ø4C12	Cap, switch, red (1 req'd)(user at S2)
S3,S4	4ØNW98Ø1A34	Switch, DIP, SPST, 8-position
U1-U8, U15-22	51NW9615S68	IC, MB81256-12PZ
U9,U12, U67	51NW9615M9Ø	IC, 74F245PC
U1Ø,U13	51NW9615R38	IC, SN74LS794N
U11,U14	51NW9615R36	IC, 74F543SPC
U23,U26	51NW9615K61	IC, 74F157PC
U24	51NW9615F79	IC, SN74S24ØN
U25,U42	51NW9615F85	IC, SN74S38N
U27	51AW5185BØ1	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U27)
U28	51AW4697B53	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U28)
U29,U37, U38,U65	51NW9615GØ7	IC, SN74S244N
U3Ø	51AW4697B54	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U3Ø)
U31	51AW5185BØ3	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U31)

TABLE 5-6. VME105 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U32,U33, U92	51NW9615K73	IC, 74F00PC
U34	51NW9615B59	IC, MC7407P
U35,U66	51NW9615E93	IC, SN74LS14N
U36	51NW9615M11	IC, MC68010L10
---	09-W4659B32	Socket, IC, SIL, 32-pin (2 req'd)(used at U36)
U39	51NW9615F31	IC, SN74S51N
U40,U54, U62,U105	51NW9615J39	IC, 74F74PC
U41	51NW9615F38	IC, SN74LS393N
U43,U107	51NW9615F02	IC, SN74LS244N
U44,U49, U57	51NW9615R26	IC, SN74ALS645-1N
U45	51AW5120B12	IC, Programmed
---	09NW9811B01	Socket, IC, DIL, 24-pin (1 req'd)(used at U45)
U46,U94, U97	51NW9615C25	IC, SN74LS74AN
U47	51NW9615C24	IC, SN74LS32N
U50,U52, U59	51NW9615H41	IC, SN74LS682N
U51	51NW9615E95	IC, SN74LS240N
U53	51AW5120B08	IC, Programmed
---	09NW9811B01	Socket, IC, DIL, 24-pin (1 req'd)(used at U53)

TABLE 5-6. VME1Ø5 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U55,U61, U79,U88	51NW9615K7Ø	IC, 74FØ8PC
U58	51AW4591C34	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U58)
U6Ø	51NW9615B65	IC, MC1455P1
U64	51AW4591C69	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(user at U64)
U68	51NW9615K65	IC, 74F64PC
U69,U83	51NW9615K66	IC, 74F32PC
U71,U8Ø, U87,U1Ø3	51NW9615C22	IC, SN74LSØ8N
U72	51AW5185BØ4	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U72)
U73	51NW9615R69	IC, MC6823ØP8
---	Ø9NW9811A26	Socket, IC, DIL, 48-pin (1 req'd)(used at U73)
U74	51NW9615C6Ø	IC, MC3456P
U75	51NW9615H38	IC, SN75175N
U81	51NW9615H37	IC, SN17574N
U82,U91	51NW9615K71	IC, 74FØ4PC
U84	51NW9615R68	IC, Z853ØAPC
---	Ø9-W4659B2Ø	Socket, IC, SIL, 2Ø-pin (2 req'd)(used at U84)

TABLE 5-6. VME1Ø5 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U85	51NW9615C21	IC, SN74LSØ4N
U86	51NW9615D93	IC, SN74S3ØN
U9Ø,U96	51NW9615S83	IC, MC1454Ø6P
U93	51NW9615K69	IC, 74F1ØPC
U1Ø1	51NW9615F35	IC, SN74LS21N
U1Ø2	51NW9615K72	IC, 74FØ2PC
U1Ø4	51NW9615C69	IC, SN74LS138N
XR1	51NW9626A94	Resistor network, four 12Ø ohm
---	Ø9NW9811A9Ø	Socket, IC, SIL, 8-pin (1 req'd)(use at XR1)
Y1	48AW1Ø15BØ7	Crystal oscillator, 16.Ø MHz
Y2	48AW1Ø15BØ3	Crystal oscillator, 2Ø.Ø MHz
---	Ø9NW9811A46	Socket, crystal oscillator (2 req'd)(use at Y1 and Y2)
---	47NW94Ø5A28	Jackpost, assembly (2 req'd)
---	29NW98Ø5B17	Jumper, insulated, shorting (28 req'd)[use at J1(1-2)(5-6)(7-8) (9-11)(1Ø-12),J2(5-6),J4(1-2),J6(2-3), J7(1-2)(3-4)(5-6)(7-8)(9-1Ø)(11-12) (13-14),J11(1-2)(3-4)(5-6)(7-8), J12(1-2),J16(1-2)(3-4)(5-6)(7-8)(9-1Ø) 11-13)(12-14),J25(1-2)]
---	29NW98Ø5B44	Jumper, 2-pin (3 req'd)[use at J1Ø(1-2), J22(1-2), and J24(1-2)]
---	67NW9415A17	Kit, 6 component, ejector handle

TABLE 5-6. VME1Ø5 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	64-W5111BØ1	Panel, front, VME1Ø4/1Ø5/1Ø6/1Ø7
---	29NW98Ø5CØ7	Pin, Ø.Ø25-inch square, auto-insert (92 req'd)[use at J1(1-12), J2(1-6), J3(1-2), J4(1-2), J6(1-3), J7(1-14), J8(1-3), J9(1-1Ø), J11(1-8), J12(1-2), J14(1-2), J15(1-8), J16(1-14), J25(1-3), and J27(1-3)]
---	33-W5Ø89B32	Nameplate, MVME1Ø5 (1 req'd)
---	33-W5Ø89BØ1	Nameplate, Motorola logo (1 req'd)
---	Ø9-W4659B14	Socket, IC, SIL, 14-pin (8 req'd)(use at XU48, XU56, XU63, XU7Ø)
---	42NW94Ø1B14	Screw, captive collar (2 req'd)
---	Ø3NW9ØØ4B48	Screw, captive, M2.5 (2 req'd)

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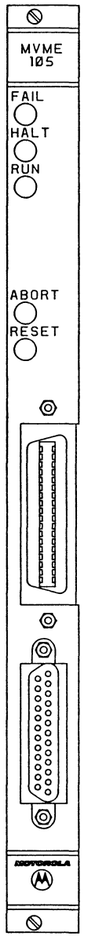
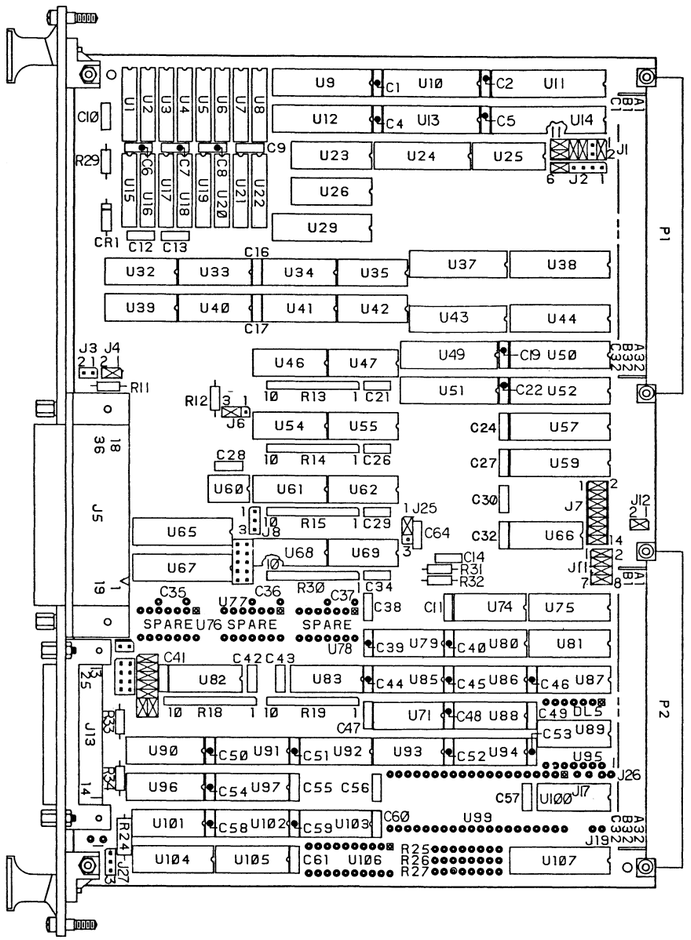
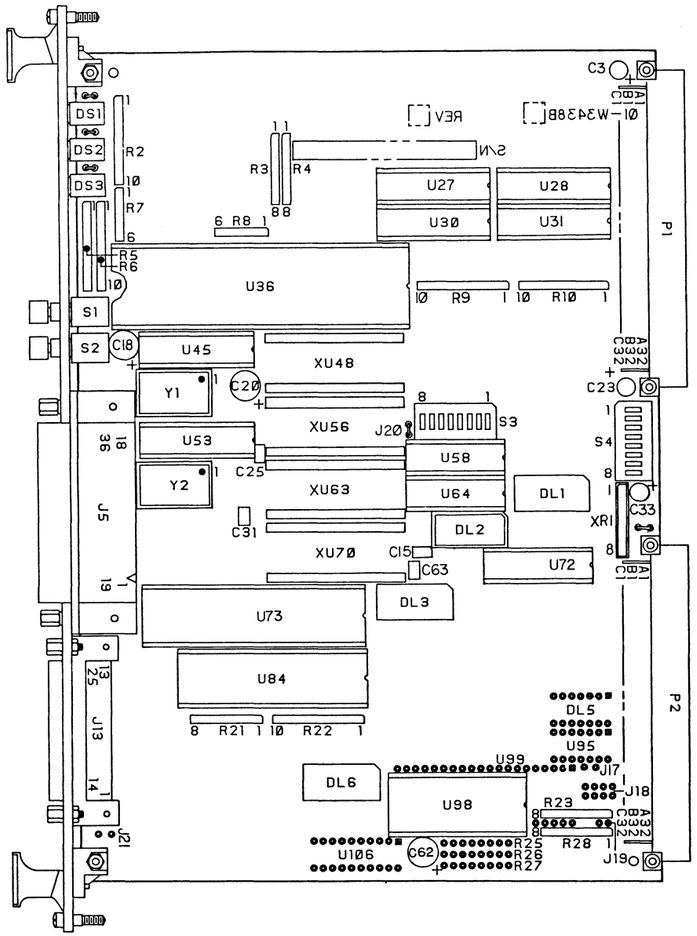


Front
Panel



VME105 with components removed for clarity.



VME105 with components removed for clarity.

FIGURE 5-2. MVME105 PARTS LOCATION DIAGRAM

TABLE 5-7. VME1Ø6 PARTS LIST

Reference Designation	Motorola Part Number	Description
---	84-W8438BØ1	Printed wiring board assembly, MVME1Ø5/1Ø6/1Ø7
C1,C2, C4-13, C16,C17, C19,C21, C22,C24, C26-3Ø, C32,C34, C38-61, C64	21NW9632AØ3	Capacitor, ceramic, Ø.1 MFD, 5Ø Vdc
C3,C23, C33	23NW9618A82	Capacitor, electrolytic, 22 MFD, 25 Vdc
C14	21NW97Ø9AØ8	Capacitor, ceramic, .1 MFD, 5Ø Vdc
C15,C25, C63	21SW992CØ14	Capacitor, ceramic, .ØlØ FD, 5Ø Vdc
C18,C2Ø, C62	23NW9618A79	Capacitor, electrolytic, 1ØØ MFD, 25 Vdc
C31	21NW96Ø4A58	Capacitor, ceramic, 33Ø PFD, 5Ø Vdc
CR1	48NW9616AØ3	Diode, 1N4148/1N914
DL1	51NW9615UØ4	IC, DS1ØØØ-25Ø
DL2,DL6	ØlNW98Ø4C32	Delay module, 3Ø nsec
DL3	51NW9615T55	IC, DS1ØØØ-1ØØ
DS1,DS2	48NW9612A49	LED, red
DS3	48NW9612A59	LED, green
J5	28NW98Ø2G48	Connector, right-angle, 36-pin
---	Ø3SW993D3Ø8	Screw, PhFil, M3.Ø x Ø.5 x 8 (2 req'd)(use at J5)
J13	28NW98Ø2G8Ø	Connector, right-angle, 25-pin

TABLE 5-7. VME1Ø6 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
P1,P2	28NW98Ø2E51	Connector, PWB, 3-row, 96-pin
---	Ø5NW9ØØ7A26	Eyelet, .Ø89 OD x .344 L (4 req'd)(use with P1 and P2)
R2,R5, R1Ø,R13, R15,R18, R22,R3Ø	51NW9626B56	Resistor network, nine 1ØK ohm
R3,R4	51NW9626BØ1	Resistor network, four 33 ohm
R6	51NW9626B42	Resistor network, five 33 ohm
R7	51NW9626A4Ø	Resistor network, five 1K ohm
R8	51NW9626A46	Resistor network, five 4.7K ohm
R9,R14	51NW9626B47	Resistor network, nine 22K ohm
R11	Ø6SW-124A89	Resistor, film, 1/4W, 5%, 47K ohm
R12	Ø6SW-124A81	Resistor, film, 1/4W, 5%, 22K ohm
R19	51NW9626A41	Resistor network, nine 4.7K ohm
R21,R23	51NW9626A49	Resistor network, seven 1ØK ohm
R24	Ø6SW-124A53	Resistor, fixed, film, 1/2W, 5%, 1.5K ohm
R28	51NW9626A6Ø	Resistor network, six 22Ø/33Ø ohm
R29,R33, R34	Ø6SW-124A37	Resistor, film, 1/4W, 5%, 33Ø ohm
R31	Ø6SW-96ØE18	Resistor, film, 1/8W, 1%, 15ØK ohm
R32	Ø6SW-962B22	Resistor, film, 1/8W, 5%, 1.ØM ohm
S1,S2	4ØNW98Ø1B7Ø	Switch, pushbutton, SPDT
---	38NW94Ø4C11	Cap, switch, black (1 req'd)(user at S1)

TABLE 5-7. VME1Ø6 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	38NW94Ø4C12	Cap, switch, red (1 req'd)(user at S2)
S3,S4	4ØNW98Ø1A34	Switch, DIP, SPST, 8-position
U1-U8, U15-22	51NW9615S68	IC, MB81256-12PZ
U9,U12, U67	51NW9615M9Ø	IC, 74F245PC
U1Ø,U13	51NW9615R38	IC, SN74LS794N
U11,U14	51NW9615R36	IC, 74F543SPC
U23,U26	51NW9615K61	IC, 74F157PC
U24	51NW9615F79	IC, SN74S24ØN
U25,U42	51NW9615F85	IC, SN74S38N
U27	51AW5185BØ1	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U27)
U28	51AW4697B53	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U28)
U29,U37, U38,U65	51NW9615GØ7	IC, SN74S244N
U3Ø	51AW4697B54	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U3Ø)
U31	51AW5185BØ3	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U31)

TABLE 5-7. VME1Ø6 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U32,U33, U92	51NW9615K73	IC, 74FØØPC
U34,U1ØØ	51NW9615B59	IC, MC74Ø7P
U35,U66	51NW9615E93	IC, SN74LS14N
U36	51NW9615M11	IC, MC68Ø1ØL1Ø
---	Ø9-W4659B32	Socket, IC, SIL, 32-pin (2 req'd)(used at U36)
U39	51NW9615F31	IC, SN74S51N
U4Ø,U54, U62,U1Ø5	51NW9615J39	IC, 74F74PC
U41	51NW9615F38	IC, SN74LS393N
U43,U1Ø7	51NW9615FØ2	IC, SN74LS244N
U44,U49, U57	51NW9615R26	IC, SN74ALS645-1N
U45	51AW512ØB12	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U45)
U46,U94, U97	51NW9615C25	IC, SN74LS74AN
U47	51NW9615C24	IC, SN74LS32N
U5Ø,U52, U59	51NW9615H41	IC, SN74LS682N
U51	51NW9615E95	IC, SN74LS24ØN
U53	51AW512ØBØ8	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U53)

TABLE 5-7. VME1Ø6 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U55,U61, U79,U88	51NW9615K7Ø	IC, 74FØ8PC
U58	51AW4591C34	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (2 req'd)(used at U58)
U6Ø	51NW9615B65	IC, MC1455P1
U64	51AW4591C69	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (2 req'd)(user at U64)
U68	51NW9615K65	IC, 74F64PC
U69,U83	51NW9615K66	IC, 74F32PC
U71,U8Ø, U87,U1Ø3	51NW9615C22	IC, SN74LSØ8N
U72	51AW5185BØ4	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U72)
U73	51NW9615R69	IC, MC6823ØP8
---	Ø9NW9811A26	Socket, IC, DIL, 48-pin (1 req'd)(used at U73)
U74	51NW9615C6Ø	IC, MC3456P
U75	51NW9615H38	IC, SN75175N
U81	51NW9615H37	IC, SN75174N
U82,U91	51NW9615K71	IC, 74FØ4PC
U84	51NW9615R68	IC, Z853ØAPC
---	Ø9-W4659B2Ø	Socket, IC, SIL, 2Ø-pin (2 req'd)(used at U84)

TABLE 5-7. VME1Ø6 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U85	51NW9615C21	IC, SN74LSØ4N
U86	51NW9615D93	IC, SN74S3ØN
U89	51NW9615D25	IC, SN7416N
U9Ø,U96	51NW9615S83	IC, MC1454Ø6P
U93	51NW9615K69	IC, 74F1ØPC
U98	51NW9615P43	IC, WD177ØPH
---	Ø9NW9811A64	Socket, IC, DIL, 28-pin (use at U98)
U1Ø1	51NW9615F35	IC, SN74LS21N
U1Ø2	51NW9615K72	IC, 74FØ2PC
U1Ø4	51NW9615C69	IC, SN74LS138N
XR1	51NW9626A94	Resistor network, four 12Ø ohm
---	Ø9NW9811A9Ø	Socket, IC, SIL, 8-pin (1 req'd)(use at XR1)
Y1	48AW1Ø15BØ7	Crystal oscillator, 16.Ø MHz
Y2	48AW1Ø15BØ3	Crystal oscillator, 2Ø.Ø MHz
---	Ø9NW9811A46	Socket, crystal oscillator (2 req'd)(use at Y1 and Y2)
---	47NW94Ø5A28	Jackpost, assembly
---	29NW98Ø5B17	Jumper, insulated, shorting (28 req'd)[use at J1(1-2)(5-6)(7-8) (9-11)(1Ø-12),J2(5-6),J4(1-2),J6(2-3), J7(1-2)(3-4)(5-6)(7-8)(9-1Ø)(11-12) (13-14),J11(1-2)(3-4)(5-6)(7-8), J12(1-2),J16(1-2)(3-4)(5-6)(7-8)(9-1Ø) 11-13)(12-14),J25(1-2)]

TABLE 5-7. VME10Ø PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	29NW98Ø5B44	Jumper, 2-pin (4 req'd)[use at J1Ø(1-2), J2Ø(1-2), J23(1-2), and J24(1-2)]
---	67NW9415A17	Kit, 6 component, ejector handle
---	64-W5111BØ1	Panel, front, VME1Ø4/1Ø5/1Ø6/1Ø7
---	29NW98Ø5CØ7	Pin, Ø.Ø25-inch square, auto-insert (92 req'd)[use at J1(1-12), J2(1-6), J3(1-2), J4(1-2), J6(1-3), J7(1-14), J8(1-3), J9(1-1Ø), J11(1-8), J12(1-2), J14(1-2), J15(1-8), J16(1-14), J25(1-3), and J27(1-3)]
---	33-W5Ø89B33	Nameplate, MVME1Ø6 (1 req'd)
---	33-W5Ø89BØ1	Nameplate, Motorola logo (1 req'd)
---	Ø9-W4659B14	Socket, IC, SIL, 14-pin (8 req'd)(use at XU48, XU56, XU63, XU7Ø)
---	42NW94Ø1B14	Screw, captive collar (2 req'd)
---	Ø3NW9ØØ4B48	Screw, captive, M2.5 (2 req'd)
---	Ø3SW993D3Ø8	Screw, PhFil, M3.Ø x Ø.5 x 8 (2 req'd)(use at J5)

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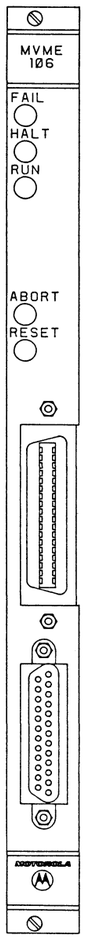
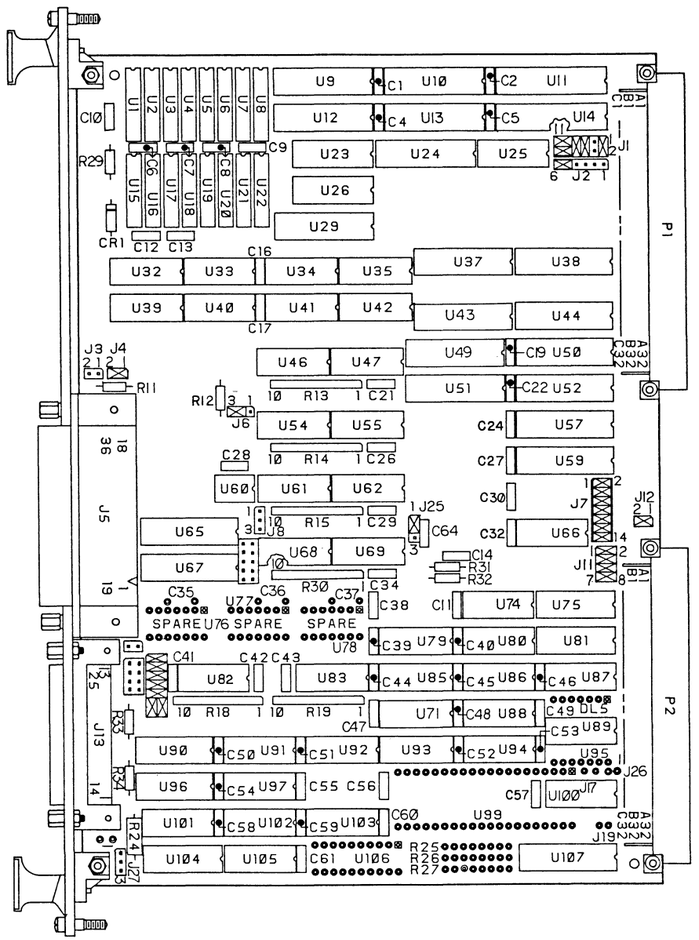
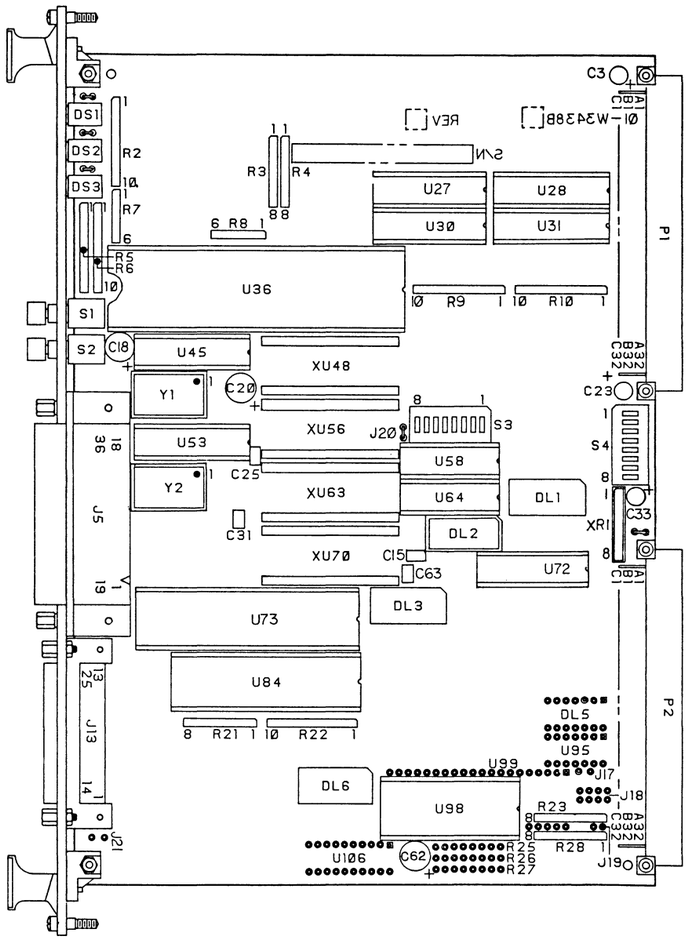


Front Panel



VME1Ø6 with components removed for clarity.



VME1Ø6 with components removed for clarity.

FIGURE 5-3. MVME1Ø6 PARTS LOCATION DIAGRAM

TABLE 5-8. VME1Ø7 PARTS LIST

Reference Designation	Motorola Part Number	Description
---	84-W8438BØ1	Printed wiring board assembly, MVME1Ø5/1Ø6/1Ø7
C1,C2, C4-13, C16,C17, C19,C21, C22,C24, C26-3Ø, C32,C34, C38-56, C58-61, C64	21NW9632AØ3	Capacitor, ceramic, Ø.1 MFD, 5Ø Vdc
C3,C23, C33	23NW9618A82	Capacitor, electrolytic, 22 MFD, 25 Vdc
C14	21NW97Ø9AØ8	Capacitor, ceramic, .1 MFD, 5Ø Vdc
C15,C25, C63	21SW992CØ14	Capacitor, ceramic, .ØlØ FD, 5Ø Vdc
C18,C2Ø, C62	23NW9618A79	Capacitor, electrolytic, 1ØØ MFD, 25 Vdc
C31	21NW96Ø4A58	Capacitor, ceramic, 33Ø PFD, 5Ø Vdc
CR1	48NW9616AØ3	Diode, 1N4148/1N914
DL1	51NW9615UØ4	IC, DS1ØØØ-25Ø
DL2,DL6	Ø1NW98Ø4C32	Delay module, 3Ø nsec
DL3	51NW9615T55	IC, DS1ØØØ-1ØØ
DL5	51NW9615U65	IC, DS1ØØØ-5ØØ
DS1,DS2	48NW9612A49	LED, red
DS3	48NW9612A59	LED, green
J5	28NW98Ø2G48	Connector, right-angle, 36-pin
---	Ø3SW993D3Ø8	Screw, PhFil, M3.Ø x Ø.5 x 8

TABLE 5-8. VME1Ø7 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
J13	28NW98Ø2G8Ø	Connector, right-angle, 25-pin
P1,P2	28NW98Ø2E51	Connector, PWB, 3-row, 96-pin
---	Ø5NW9ØØ7A26	Eyelet, .Ø89 OD x .344 L (4 req'd)(use with P1 and P2)
R2,R5, R1Ø,R13, R15,R18, R22,R3Ø	51NW9626B56	Resistor network, nine 1ØK ohm
R3,R4	51NW9626BØ1	Resistor network, four 33 ohm
R6	51NW9626B42	Resistor network, five 33 ohm
R7	51NW9626A4Ø	Resistor network, five 1K ohm
R8	51NW9626A46	Resistor network, five 4.7K ohm
R9,R14	51NW9626B47	Resistor network, nine 22K ohm
R11	Ø6SW-124A89	Resistor, film, 1/4W, 5%, 47K ohm
R12	Ø6SW-124A81	Resistor, film, 1/4W, 5%, 22K ohm
R19	51NW9626A41	Resistor network, nine 4.7K ohm
R21	51NW9626A49	Resistor network, seven 1ØK ohm
R24	Ø6SW-124A53	Resistor, fixed, film, 1/2W, 5%, 1.5K ohm
R25-27	51NW9626A6Ø	Resistor network, six 22Ø/33Ø ohm
---	Ø9NW9811A9Ø	Socket, IC, SIL, 8-pin (use at R25-27)
R29,R33, R34	Ø6SW-124A37	Resistor, film, 1/4W, 5%, 33Ø ohm
R31	Ø6SW-96ØE18	Resistor, film, 1/8W, 1%, 15ØK ohm
R32	Ø6SW-962B22	Resistor, film, 1/8W, 5%, 1.ØM ohm

TABLE 5-8. VME1Ø7 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
S1,S2	4ØNW98Ø1B7Ø	Switch, pushbutton, SPDT
---	38NW94Ø4C11	Cap, switch, black (1 req'd)(user at S1)
---	38NW94Ø4C12	Cap, switch, red (1 req'd)(user at S2)
S3,S4	4ØNW98Ø1A34	Switch, DIP, SPST, 8-position
U1-U8, U15-22	51NW9615S68	IC, MB81256-12PZ
U9,U12, U67	51NW9615M9Ø	IC, 74F245PC
U1Ø,U13	51NW9615R38	IC, SN74LS794N
U11,U14	51NW9615R36	IC, 74F543SPC
U23,U26	51NW9615K61	IC, 74F157PC
U24	51NW9615F79	IC, SN74S24ØN
U25,U42	51NW9615F85	IC, SN74S38N
U27	51AW5185BØ1	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U27)
U28	51AW4697B53	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U28)
U29,U37, U38,U65	51NW9615GØ7	IC, SN74S244N
U3Ø	51AW4697B54	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U3Ø)

TABLE 5-8. VME1Ø7 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U31	51AW5185BØ3	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U31)
U32,U33, U92	51NW9615K73	IC, 74FØØPC
U34	51NW9615B59	IC, MC74Ø7P
U35,U66	51NW9615E93	IC, SN74LS14N
U36	51NW9615M11	IC, MC68Ø1ØL1Ø
---	Ø9-W4659B32	Socket, IC, SIL, 32-pin (2 req'd)(used at U36)
U39	51NW9615F31	IC, SN74S51N
U4Ø,U54, U62,U1Ø5	51NW9615J39	IC, 74F74PC
U41	51NW9615F38	IC, SN74LS393N
U43,U1Ø7	51NW9615FØ2	IC, SN74LS244N
U44,U49, U57	51NW9615R26	IC, SN74ALS645-1N
U45	51AW512ØB12	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U45)
U46,U94, U97	51NW9615C25	IC, SN74LS74AN
U47	51NW9615C24	IC, SN74LS32N
U5Ø,U52, U59	51NW9615H41	IC, SN74LS682N
U51	51NW9615E95	IC, SN74LS24ØN

TABLE 5-8. VME1Ø7 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U53	51AW512ØBØ8	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U53)
U55,U61, U79,U88	51NW9615K7Ø	IC, 74FØ8PC
U58	51AW4591C41	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (2 req'd)(used at U58)
U6Ø	51NW9615B65	IC, MC1455P1
U64	51AW4591C67	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (2 req'd)(user at U64)
U68	51NW9615K65	IC, 74F64PC
U69,U83	51NW9615K66	IC, 74F32PC
U71,U8Ø, U87,U1Ø3	51NW9615C22	IC, SN74LSØ8N
U72	51AW5185BØ4	IC, Programmed
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U72)
U73	51NW9615R69	IC, MC6823ØP8
---	Ø9NW9811A26	Socket, IC, DIL, 48-pin (1 req'd)(used at U73)
U74	51NW9615C6Ø	IC, MC3456P
U75	51NW9615H38	IC, SN75175N
U81	51NW9615H37	IC, SN75174N

TABLE 5-8. VME1Ø7 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U82,U91	51NW9615K71	IC, 74FØ4PC
U84	51NW9615R68	IC, Z853ØAPC
---	Ø9-W4659B2Ø	Socket, IC, SIL, 2Ø-pin (2 req'd)(used at U84)
U85	51NW9615C21	IC, SN74LSØ4N
U86,U95	51NW9615D93	IC, SN74S3ØN
U9Ø,U96	51NW9615S83	IC, MC145406P
U93	51NW9615K69	IC, 74F1ØPC
U99	51NW9615R67	IC, NCR/538Ø
---	Ø9NW9811A37	Socket, IC, DIL, 4Ø-pin (use at U99)
U1Ø1	51NW9615F35	IC, SN74LS21N
U1Ø2	51NW9615K72	IC, 74FØ2PC
U1Ø4	51NW9615C69	IC, SN74LS138N
U1Ø6	51AW4699B22	IC, Programmed
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (use at U1Ø6)
XR1	51NW9626A94	Resistor network, four 12Ø ohm
---	Ø9NW9811A9Ø	Socket, IC, SIL, 8-pin (1 req'd)(use at XR1)
Y1	48AW1Ø15BØ7	Crystal oscillator, 16.Ø MHz
Y2	48AW1Ø15BØ3	Crystal oscillator, 2Ø.Ø MHz
---	Ø9NW9811A46	Socket, crystal oscillator (2 req'd)(use at Y1 and Y2)
---	47NW94Ø5A28	Jackpost, assembly

TABLE 5-8. VME1Ø7 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	29NW98Ø5B17	Jumper, insulated, shorting (28 req'd)[use at J1(1-2)(5-6)(7-8) (9-11)(1Ø-12),J2(5-6),J4(1-2),J6(2-3), J7(1-2)(3-4)(5-6)(7-8)(9-1Ø)(11-12) (13-14),J11(1-2)(3-4)(5-6)(7-8), J12(1-2),J16(1-2)(3-4)(5-6)(7-8)(9-1Ø) (11-13)(12-14),J25(1-2)]
---	29NW98Ø5B44	Jumper, 2-pin (11 req'd)[use at J17(1-2), J18(1-2) (3-4)(5-6)(7-8), J19(1-2), J21(1-2), J22(1-2), J23(1-2), and J24(1-2)]
---	67NW9415A17	Kit, 6 component, ejector handle
---	64-W5111BØ1	Panel, front, VME1Ø4/1Ø5/1Ø6/1Ø7
---	29NW98Ø5CØ7	Pin, Ø.Ø25-inch square, auto-insert (94 req'd)[use at J1(1-12), J2(1-6), J3(1-2), J4(1-2), J6(1-3), J7(1-14), J8(1-3), J9(1-1Ø), J11(1-8), J12(1-2), J14(1-2), J15(1-8), J16(1-14), J25(1-3), J26(1-2), and J27(1-3)]
---	33-W5Ø89B34	Nameplate, MVME1Ø7 (1 req'd)
---	33-W5Ø89BØ1	Nameplate, Motorola logo (1 req'd)
---	Ø9-W4659B14	Socket, IC, SIL, 14-pin (8 req'd)(use at XU48, XU56, XU63, XU7Ø)
---	42NW94Ø1B14	Screw, captive collar (2 req'd)
---	Ø3NW9ØØ4B48	Screw, captive, M2.5 (2 req'd)

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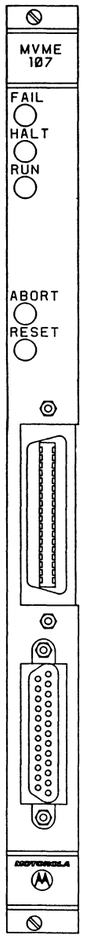
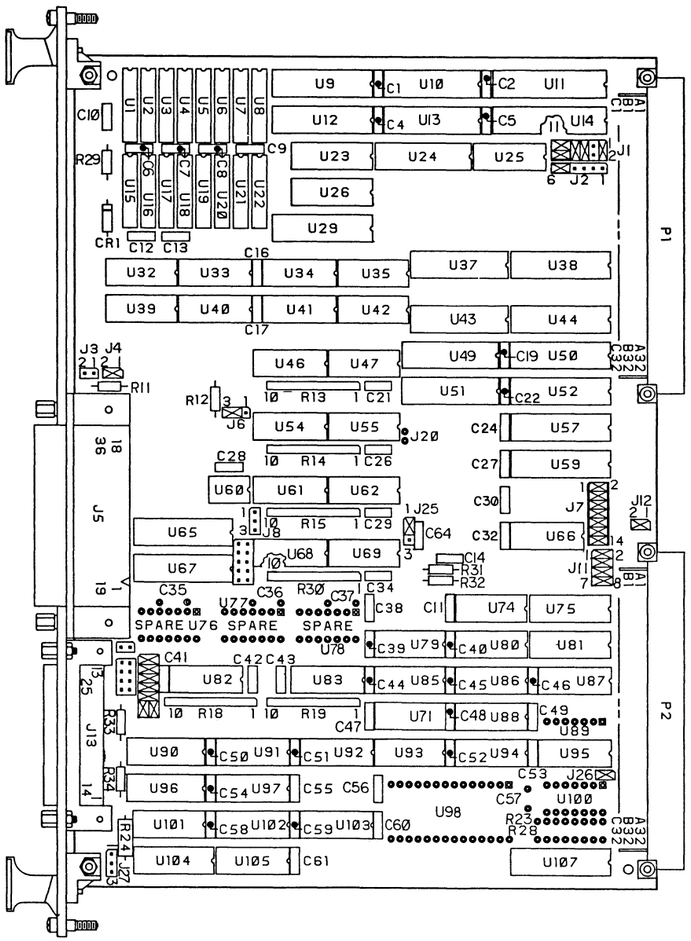
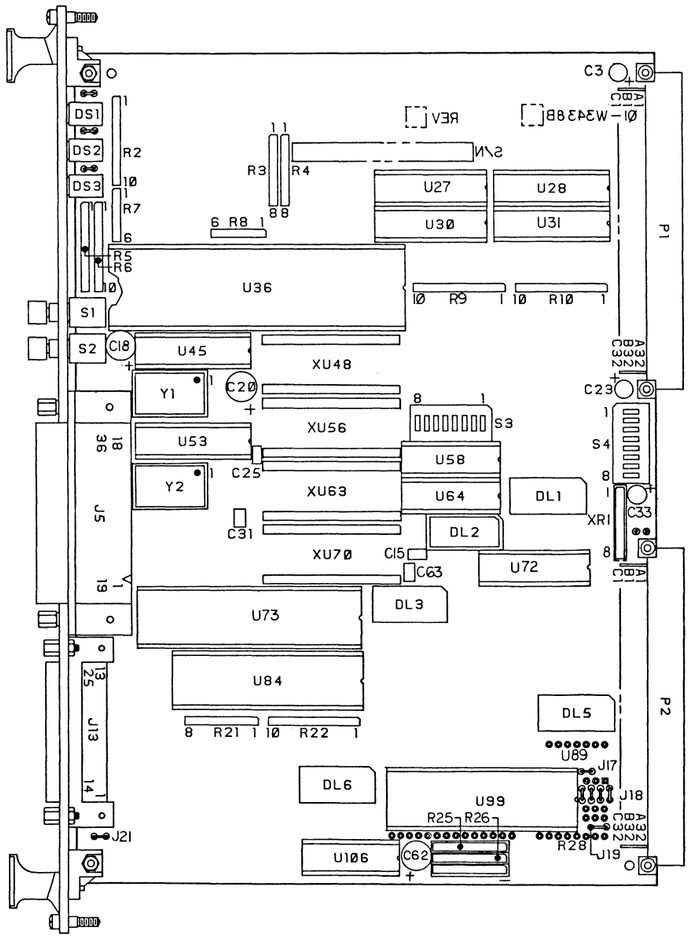


Front
Panel



VME1Ø7 with components removed for clarity.



VME1Ø7 with components removed for clarity.

FIGURE 5-4. MVME1Ø7 PARTS LOCATION DIAGRAM

5.4 SCHEMATIC DIAGRAMS

Figure 5-5 (MVME1Ø4, 22 sheets) and Figure 5-6 (MVME1Ø5/1Ø6/1Ø7, 23 sheets) contain detailed schematic diagrams of the internal circuitry comprising the four versions of the SBC. These schematic diagrams represent the latest design. Occasionally, minor component changes are made at the factory. Therefore, when replacing a component, always use the same value as the defective component even though the schematic diagram may indicate a different value or type.

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NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3450B01.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   () DENOTES - ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING. FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS.

   6 A6
   SHEET — ZONE

REFERENCE DESIGNATIONS	
Y2	
XU70	XU1-47,49-55 57-62,64-69
XR1	
U108	U48,56,63,70 89
S4	
RJ4	R1,16,17,23,25, 26,27,28
P2	
J27	J10,17,18,19,20 21,26
DSJ	
DL6	DL4
CR1	
C67	C47
HIGHEST NUMBER USED	NOT USED

TABLE 1

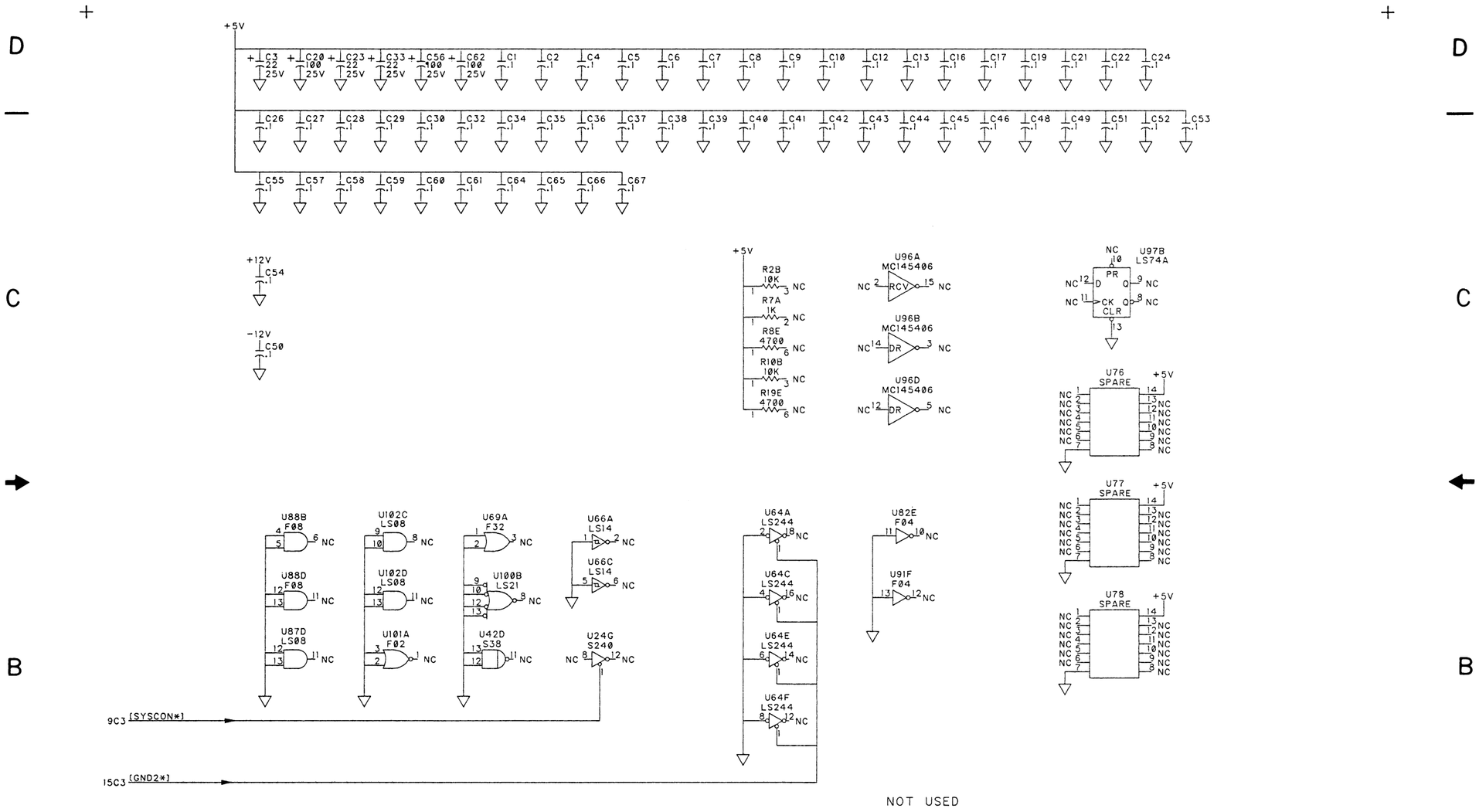
REF DES	TYPE (4)	GND	+5V	SH
DL1	250NS	7	14	15
DL2	40NS	7	14	14,18,21
DL3	100NS	7	14	6
DL5	125NS	7	14	19
DL6	30NS	7	14	6,9,18
U1	M5K4256L	4	12	8
U2	M5K4256L	4	12	8
U3	M5K4256L	4	12	8
U4	M5K4256L	4	12	8
U5	M5K4256L	4	12	8
U6	M5K4256L	4	12	8
U7	M5K4256L	4	12	8
U8	M5K4256L	4	12	8
U9	74F245	10	20	10
U10	74LS794	10	20	22
U11	74F543	12	24	14
U12	74F245	10	20	10
U13	74LS794	10	20	22
U14	74F543	12	24	14
U15	M5K4256L	4	12	8
U16	M5K4256L	4	12	8
U17	M5K4256L	4	12	8
U18	M5K4256L	4	12	8
U19	M5K4256L	4	12	8
U20	M5K4256L	4	12	8
U21	M5K4256L	4	12	8
U22	M5K4256L	4	12	8
U23	74F157	8	16	11
U24	74S240	10	20	2,9,18
U25	74S38	7	14	18
U26	74F157	8	16	11
U27	PAL20R4	12	24	17
U28	PAL20L8A	12	24	14
U29	74S244	10	20	7
U30	PAL20L8A	12	24	9
U31	PAL20R4	12	24	17
U32	74F00	7	14	6
U33	74F00	7	14	6,7
U34	7407	7	14	17
U35	74LS14	7	14	6,7,17
U36	MC68010	53	14	7
U36	MC68010	16	49	7
U37	74S244	10	20	14
U38	74S244	10	20	20
U39	74S51	7	14	6,11
U40	74F74	7	14	6,7
U41	74LS393	7	14	15
U42	74S38	7	14	2,15,18,22
U43	74LS244	10	20	9
U44	74ALS645	10	20	14
U45	PAL20L8B	12	24	9
U46	74LS74A	7	14	15
U47	74LS32	7	14	16,18
XU48	SOCKET			16
U49	74ALS645	10	20	14
U50	74LS682	10	20	9
U51	74LS240	10	20	20
U52	74LS682	10	20	9
U53	PAL20L8B	12	24	21

TABLE 1 CONT.

REF DES	TYPE (4)	GND	+5V	+12V	-12V	SH
U54	74F74	7	14			6,7
U55	74F08	7	14			22
XU56	27512	14	28			10
U57	74ALS645	10	20			14
U58	PAL16L8A	10	20			9
U59	74LS682	10	20			9
U60	MC1455	1	8			6
U61	74F08	7	14			6,15
U62	74F74	7	14			7,18
XU63	27512	14	28			10
U64	74LS244	10	20			2,9
U65	74S244	10	20			12
U66	74LS14	7	14			15,18
U67	74F245	10	20			12
U68	74F64	7	14			6
U69	74F32	7	14			2,6,9,17
XU70	SOCKET					16
U71	74LS08	7	14			13,15,22
U72	PAL20R4	12	24			18
U73	MC68230	38	12			12
U74	MC3456	7	14			15
U75	SN75175	8	16			13
U76	SPARE					2
U77	SPARE					2
U78	SPARE					2
U79	74F08	7	14			6,14,18
U80	74LS08	7	14			6,18
U81	SN75174	8	16			13
U82	74F04	7	14			2,6,11,12,13,20
U83	74F32	7	14			7,14,16
U84	Z8530	31	9			13
U85	74LS04	7	14			13,15,18,21
U86	74S30	7	14			7
U87	74LS08	7	14			2,9,10,21
U88	74F08	7	14			2,10,21
U90	MC145406	9	16	1	8	13
U91	74F04	7	14			2,6,7,9,15
U92	74F00	7	14			9,18
U93	74F10	7	14			18,20,21
U94	74LS74A	7	14			10,22
U95	74F74	7	14			20,21
U96	MC145406	9	16	1	8	2,13
U97	74LS74A	7	14			2,6
U98	PAL16L8	10	20			19
U99	74ALS244A	10	20			19
U100	74LS21	7	14			2,20
U101	74F02	7	14			2,6,21
U102	74LS08	7	14			2,13,21
U103	MCM2016	12	24			19
U104	74ALS244A	10	20			19
U105	PAL20L8B	12	24			21
U106	PAL16L8A	10	20			21
U107	PAL20L8	12	24			15
U108	74LS245	10	20			19
Y1	K1100	7	14			7
Y2	K1100	7	14			7

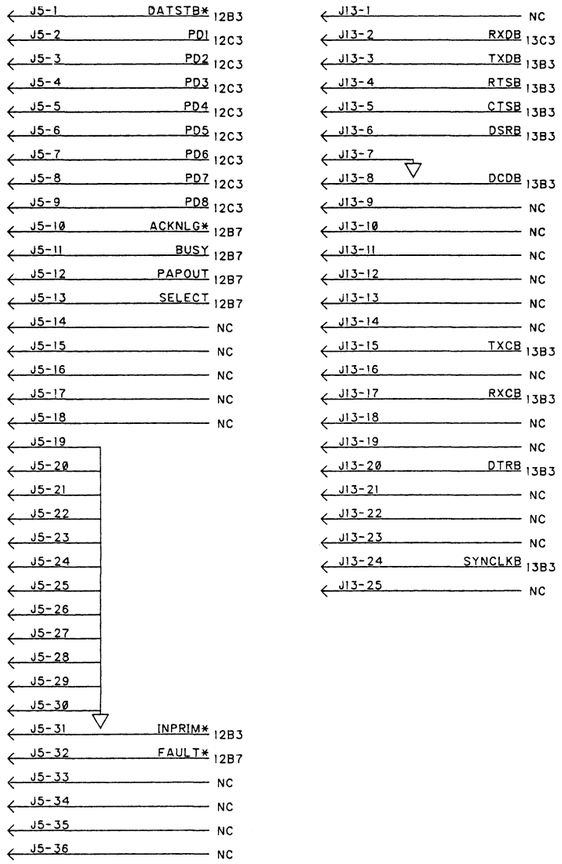
63DW3450B REV B SH 1 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 1 OF 22)



63DW3450B REV B SH 2 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 2 OF 22)



CONNECTORS

63DW3450B REV A SH 3 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 3 OF 22)

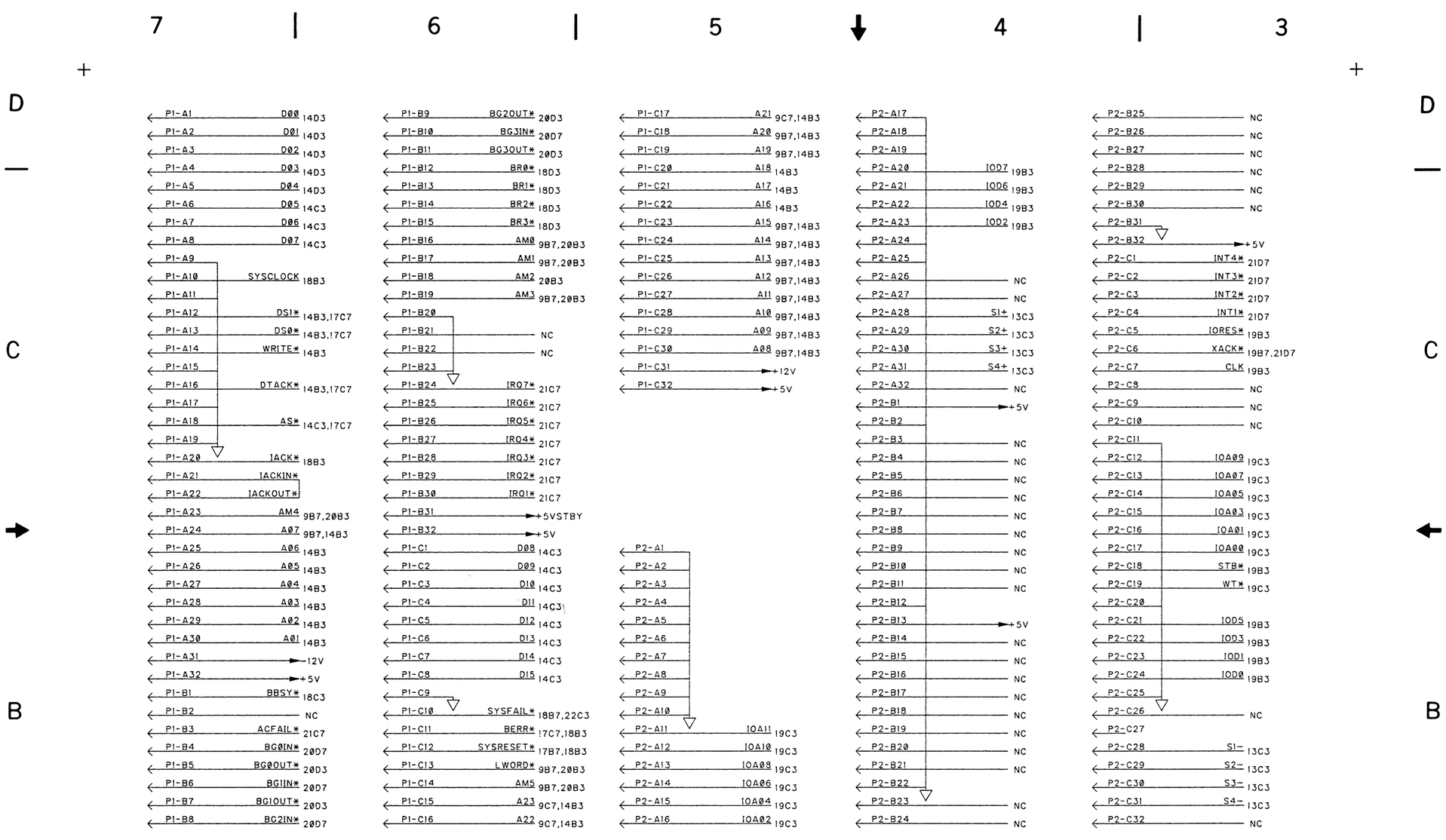
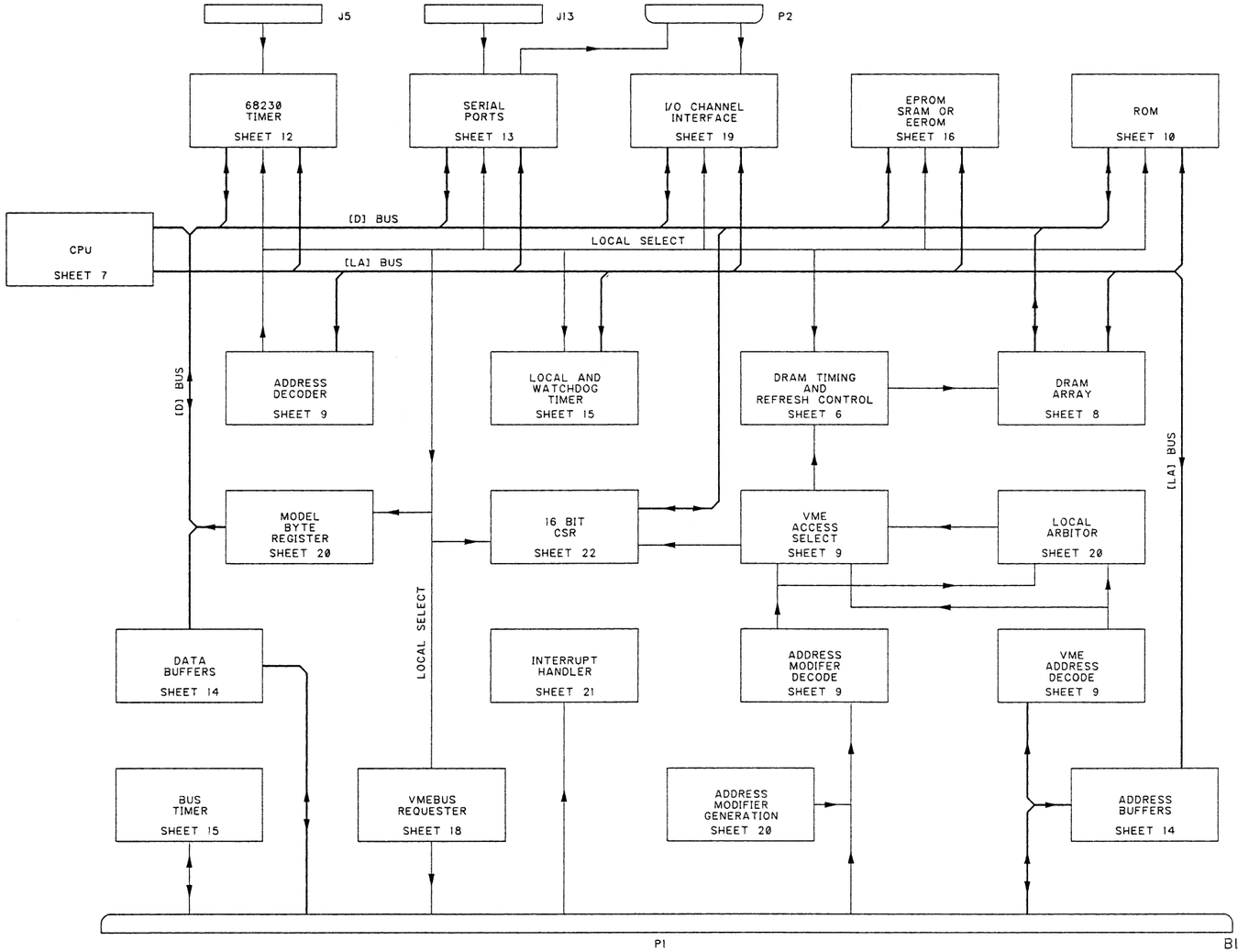
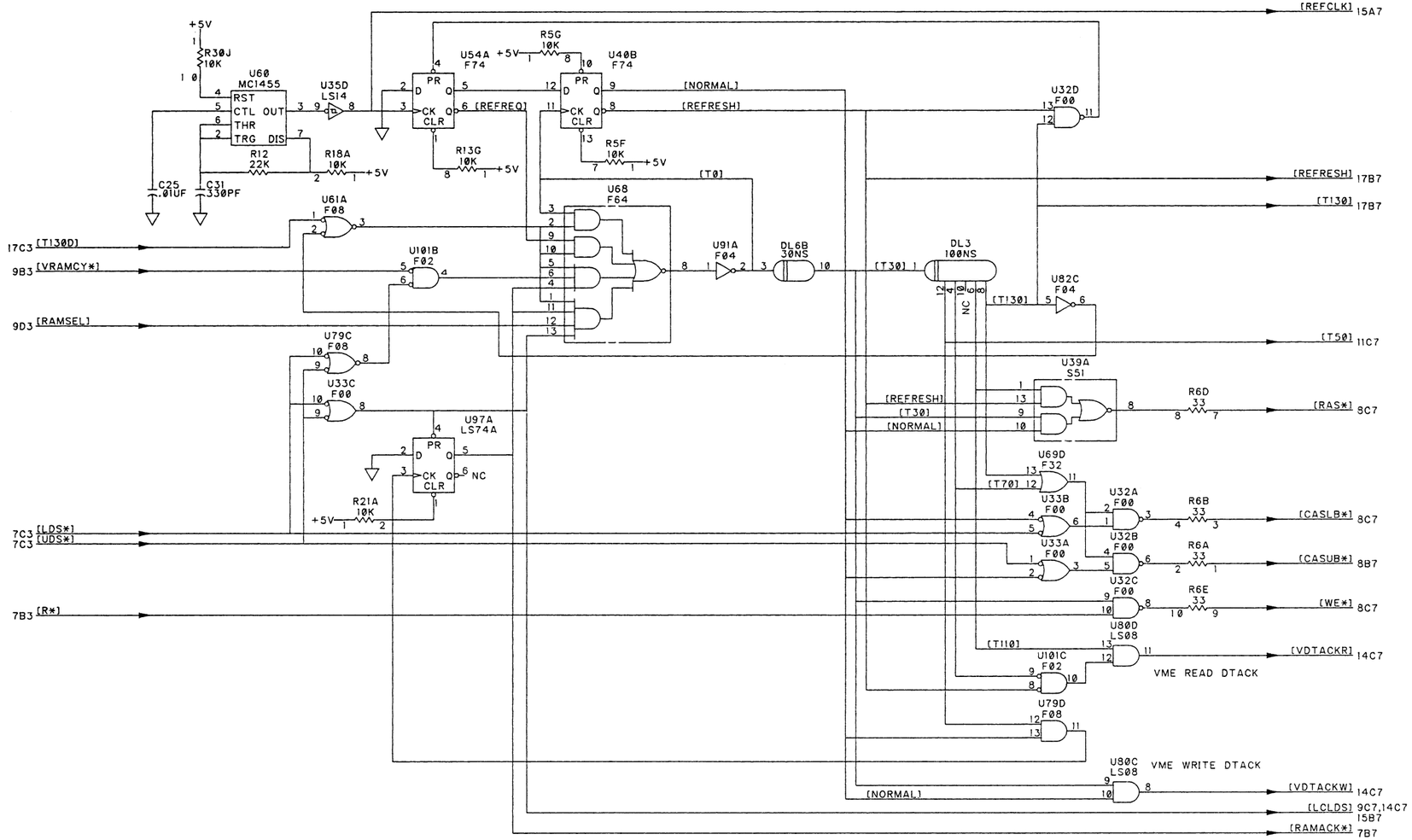


FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 4 OF 22)



BLOCK DIAGRAM
63DW3450B REV A SH 5 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 5 OF 22)



MEMORY TIMING
63DW3450B REV B SH 6 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 6 OF 22)

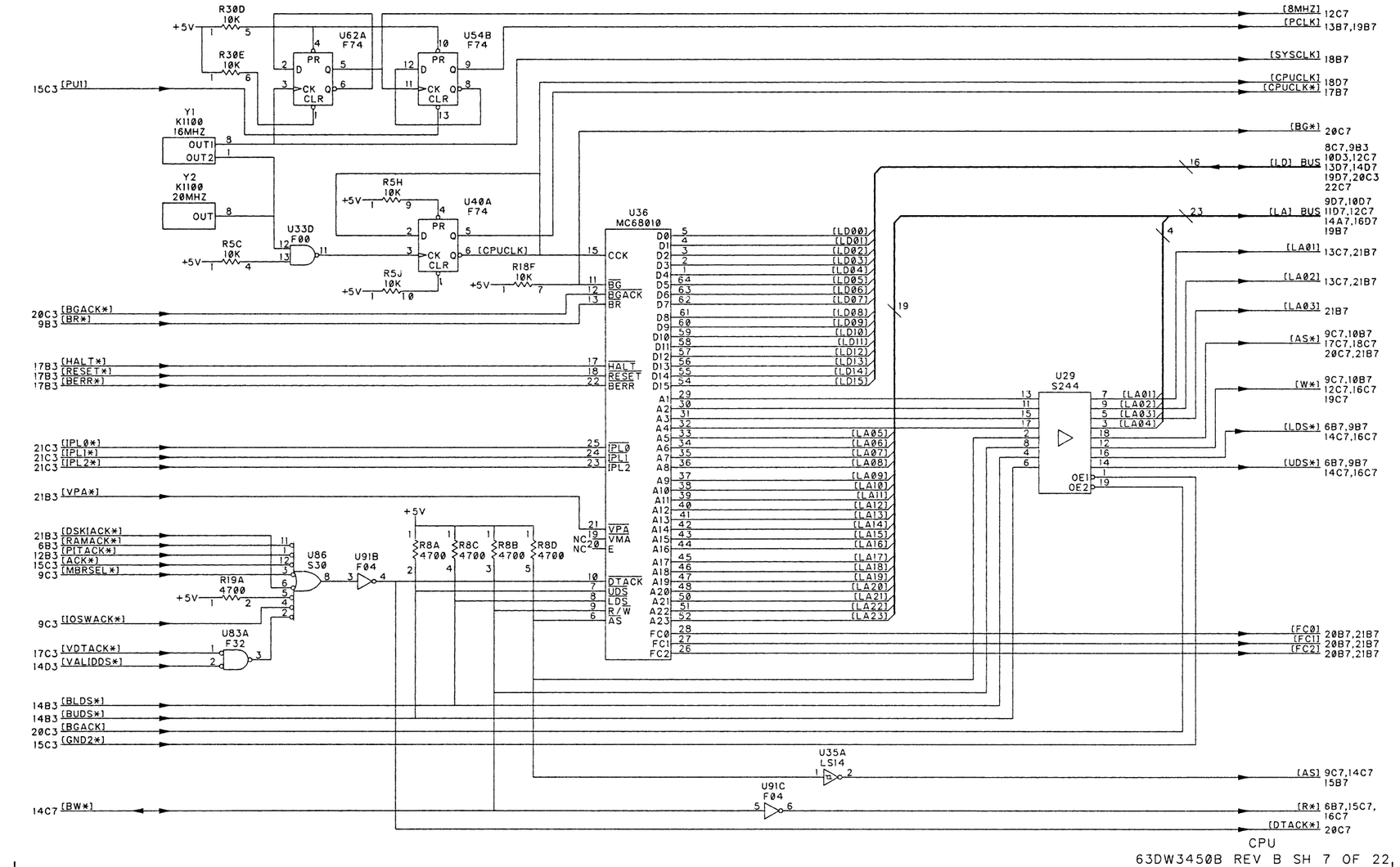
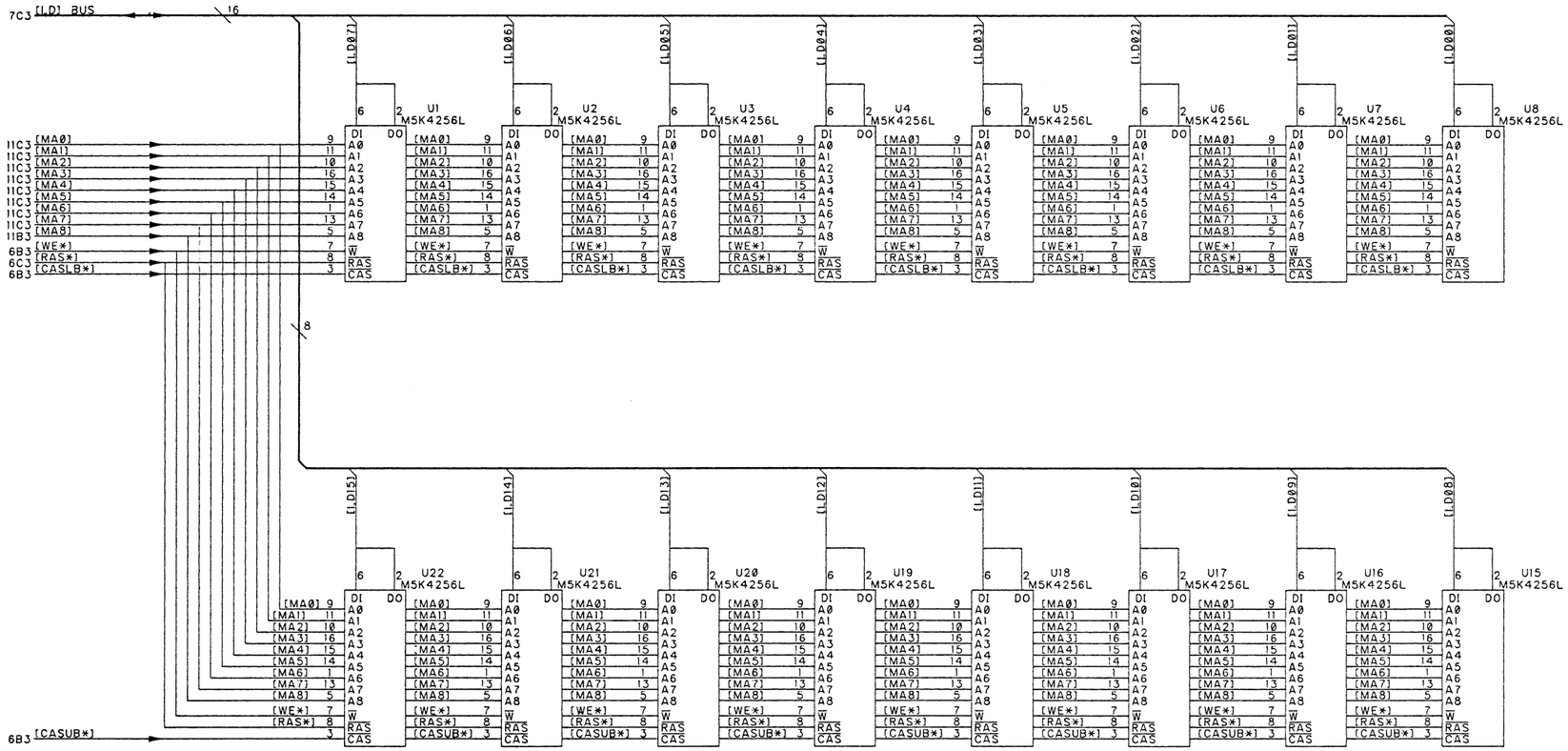


FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 7 OF 22)



RAM ARRAY
63DW3450B REV A SH 8 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 8 OF 22)

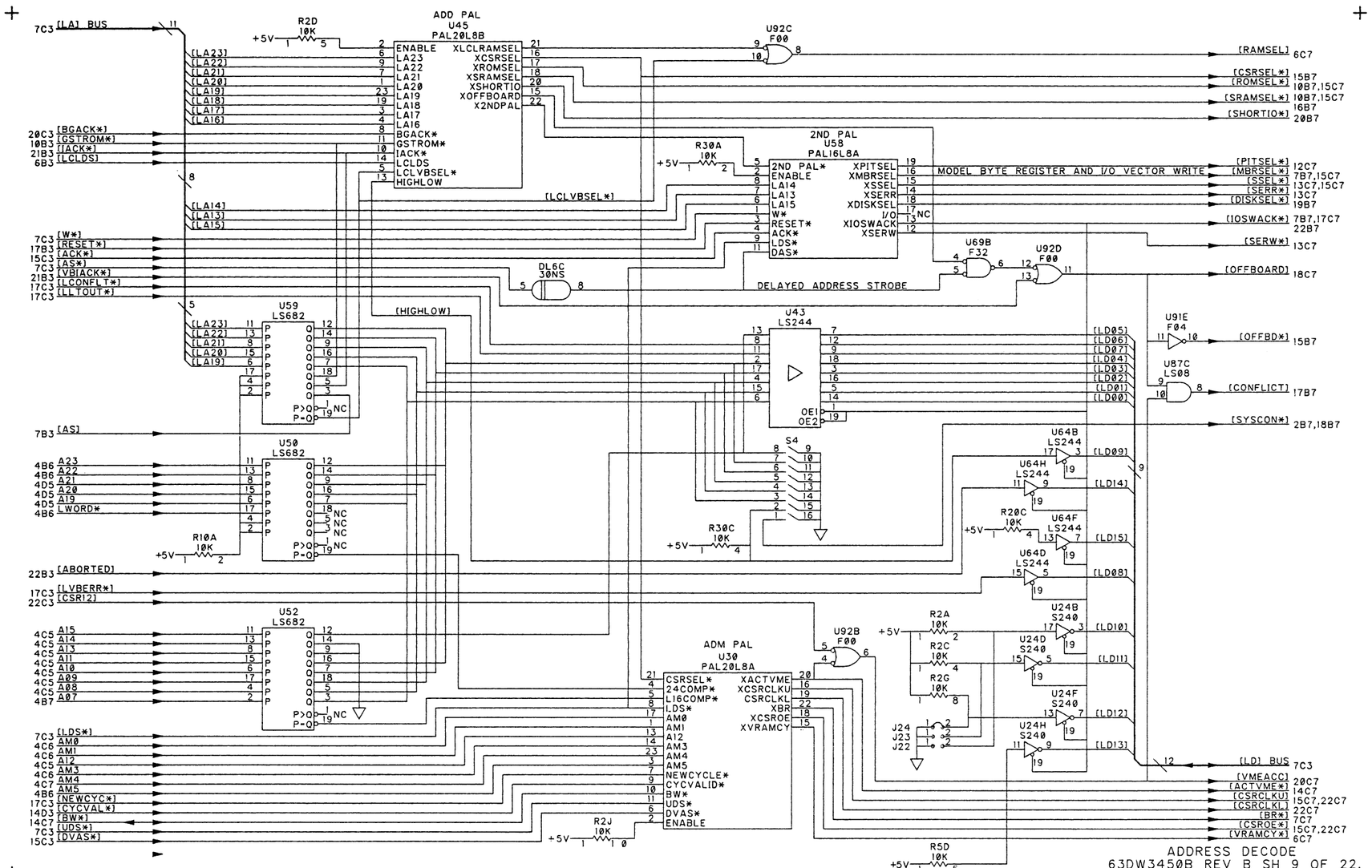
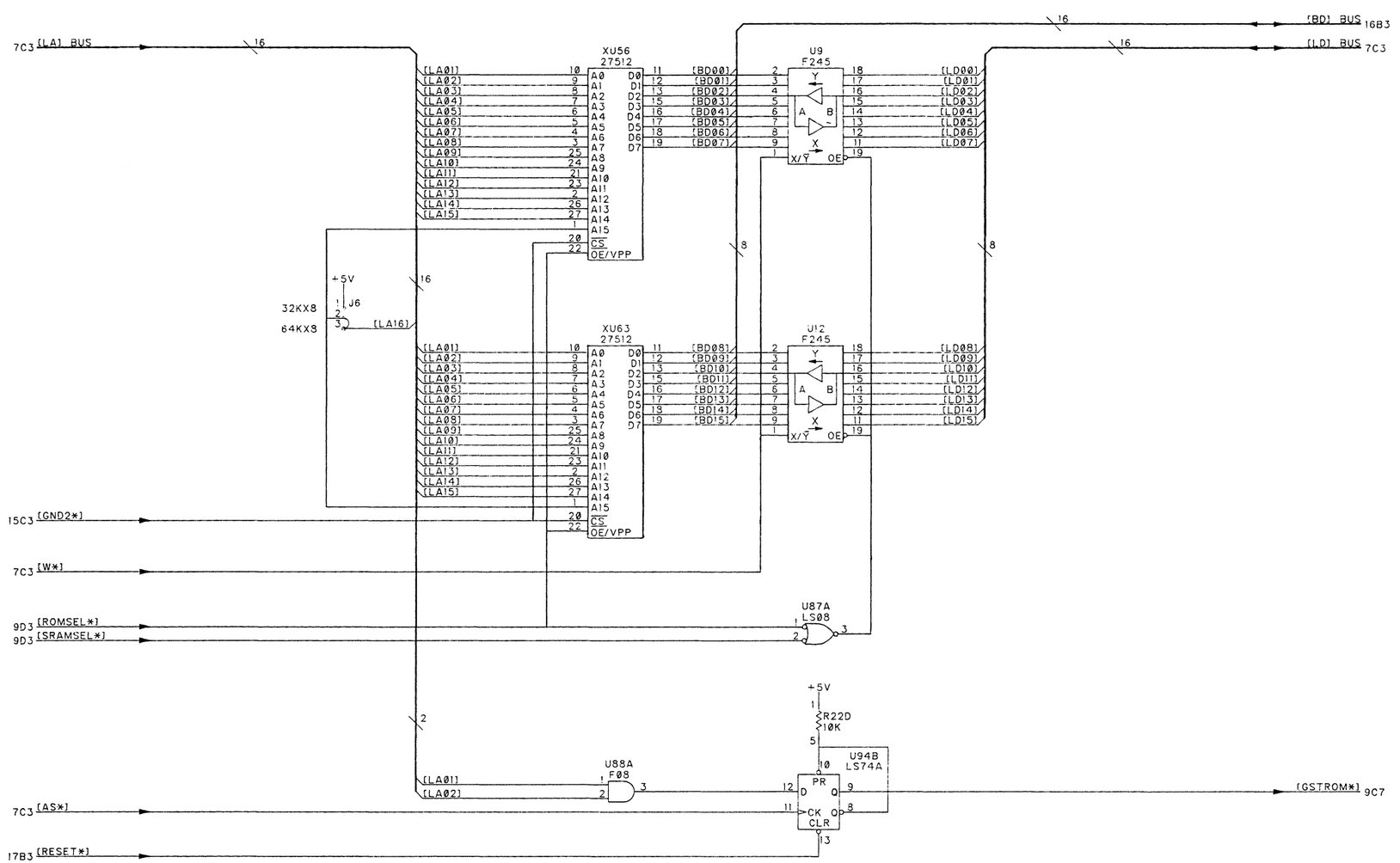


FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 9 OF 22)



EPROM
63DW3450B REV B SH 10 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 10 OF 22)

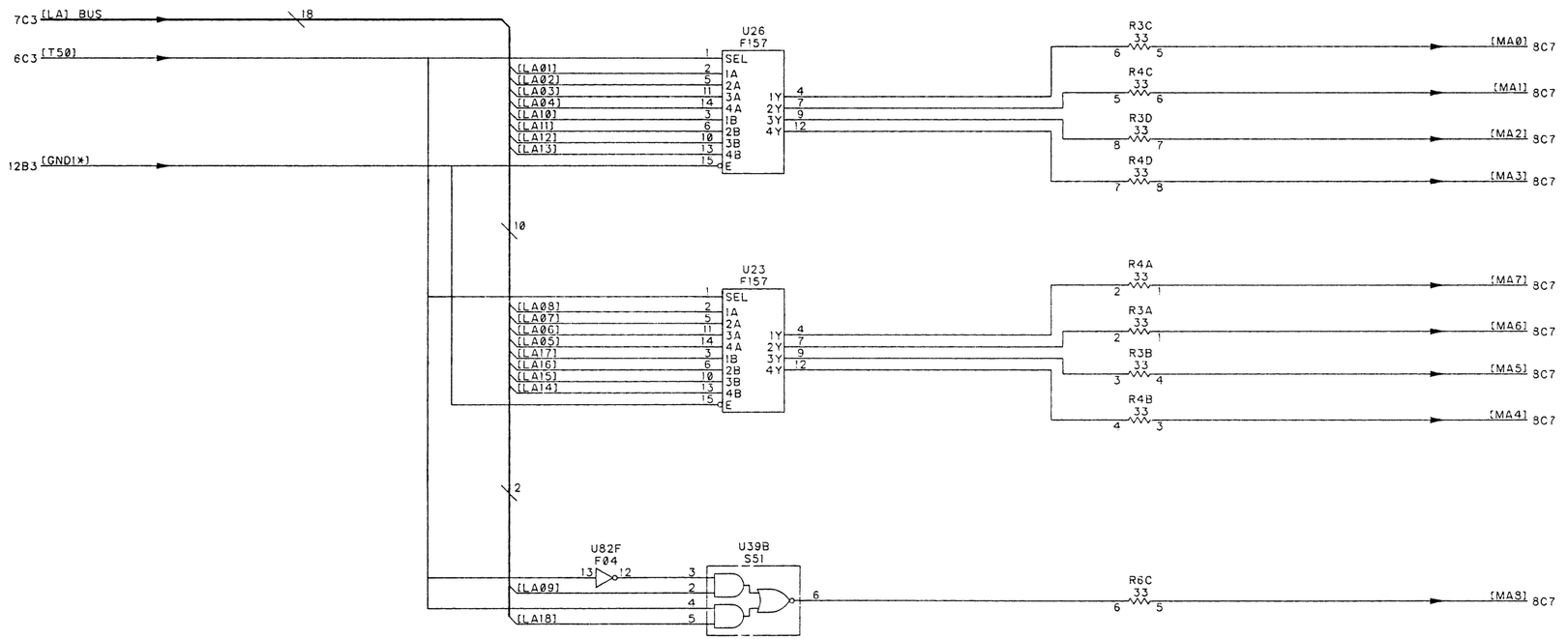
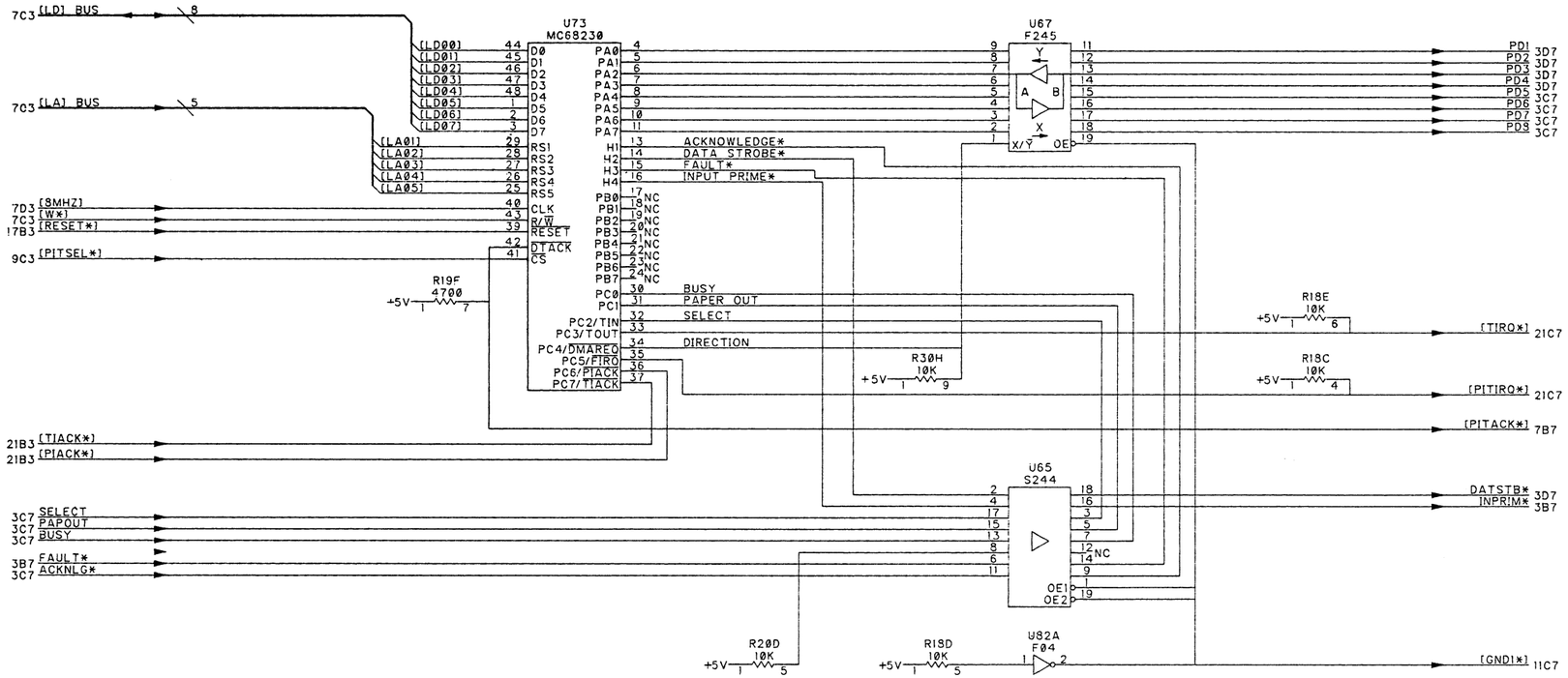


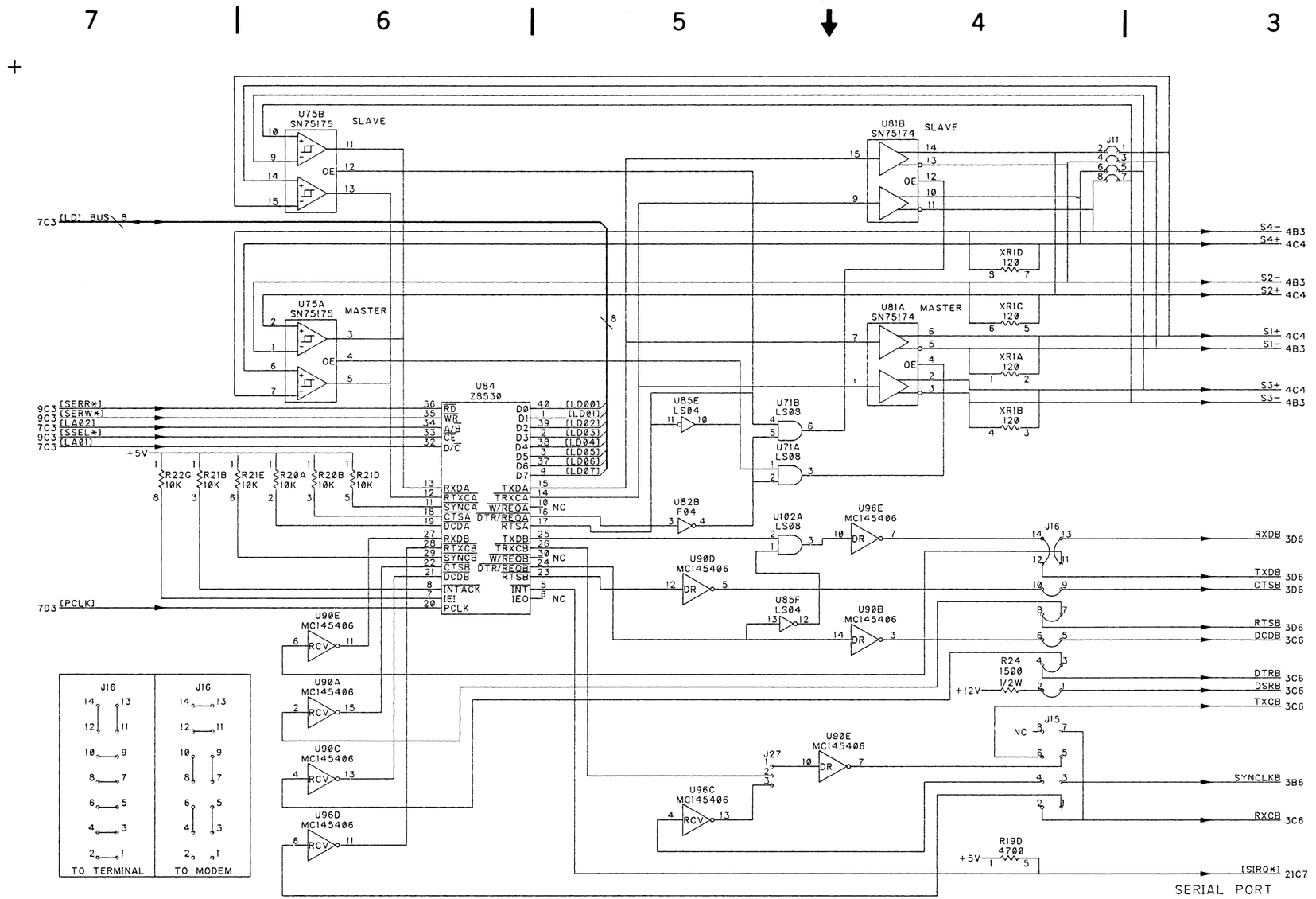
FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 11 OF 22)



TIMER

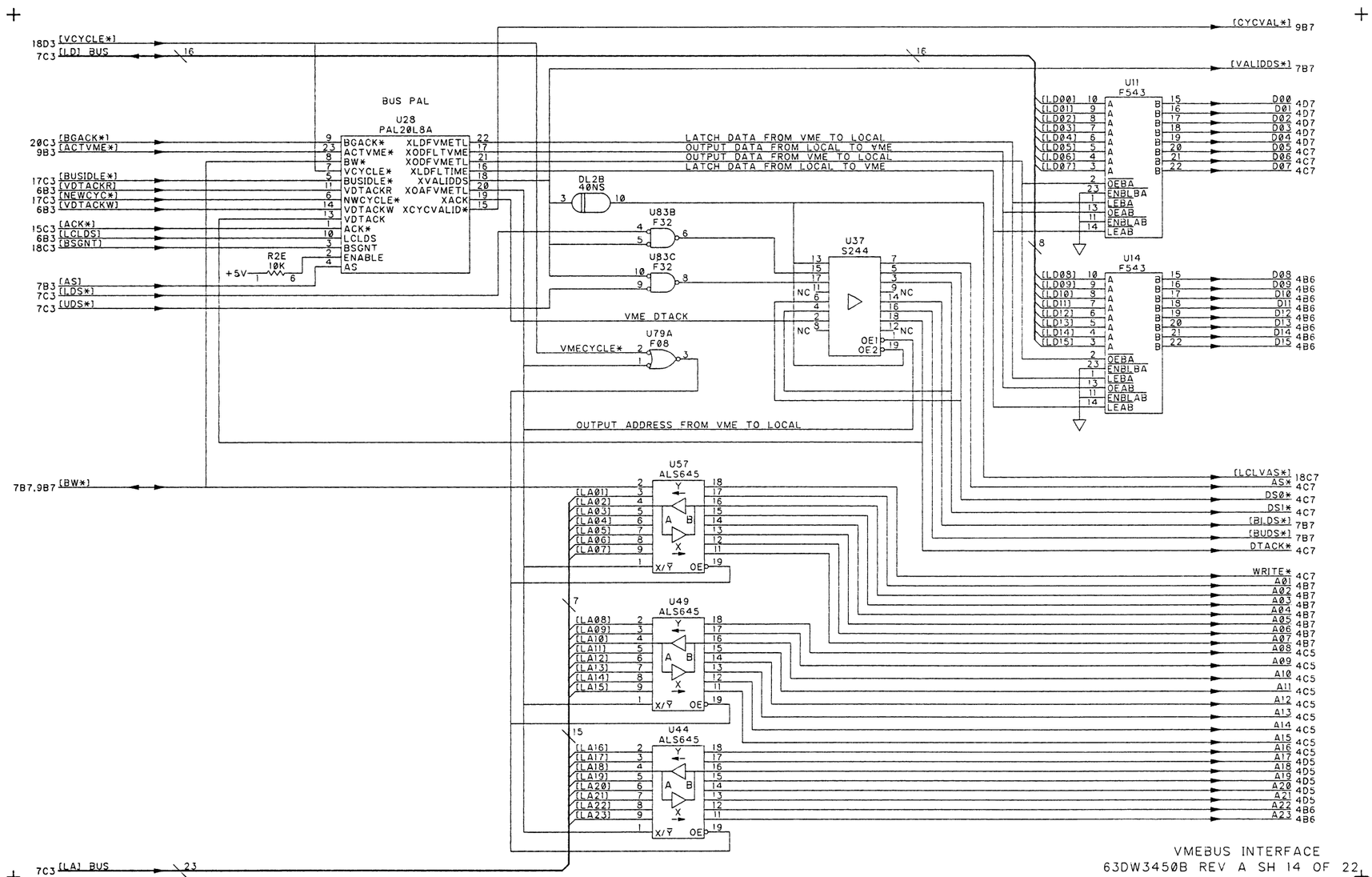
63DW3450B REV B SH 12 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 12 OF 22)



63DW3450B REV B SH 13 OF 22

FIGURE 5-5. MVME1Ø4 SCHEMATIC DIAGRAM (SHEET 13 OF 22)



VMEBUS INTERFACE
63DW3450B REV A SH 14 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 14 OF 22)

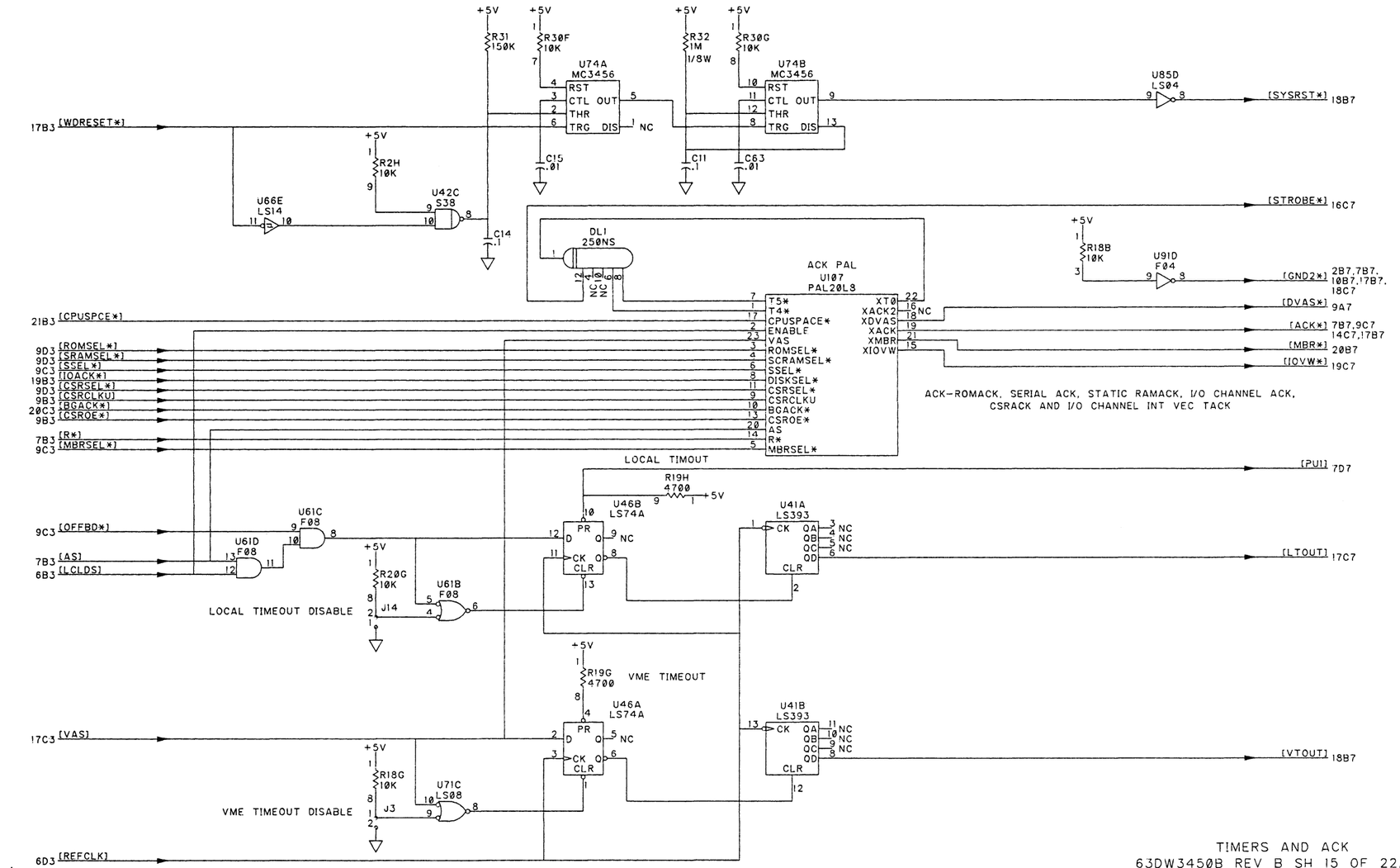
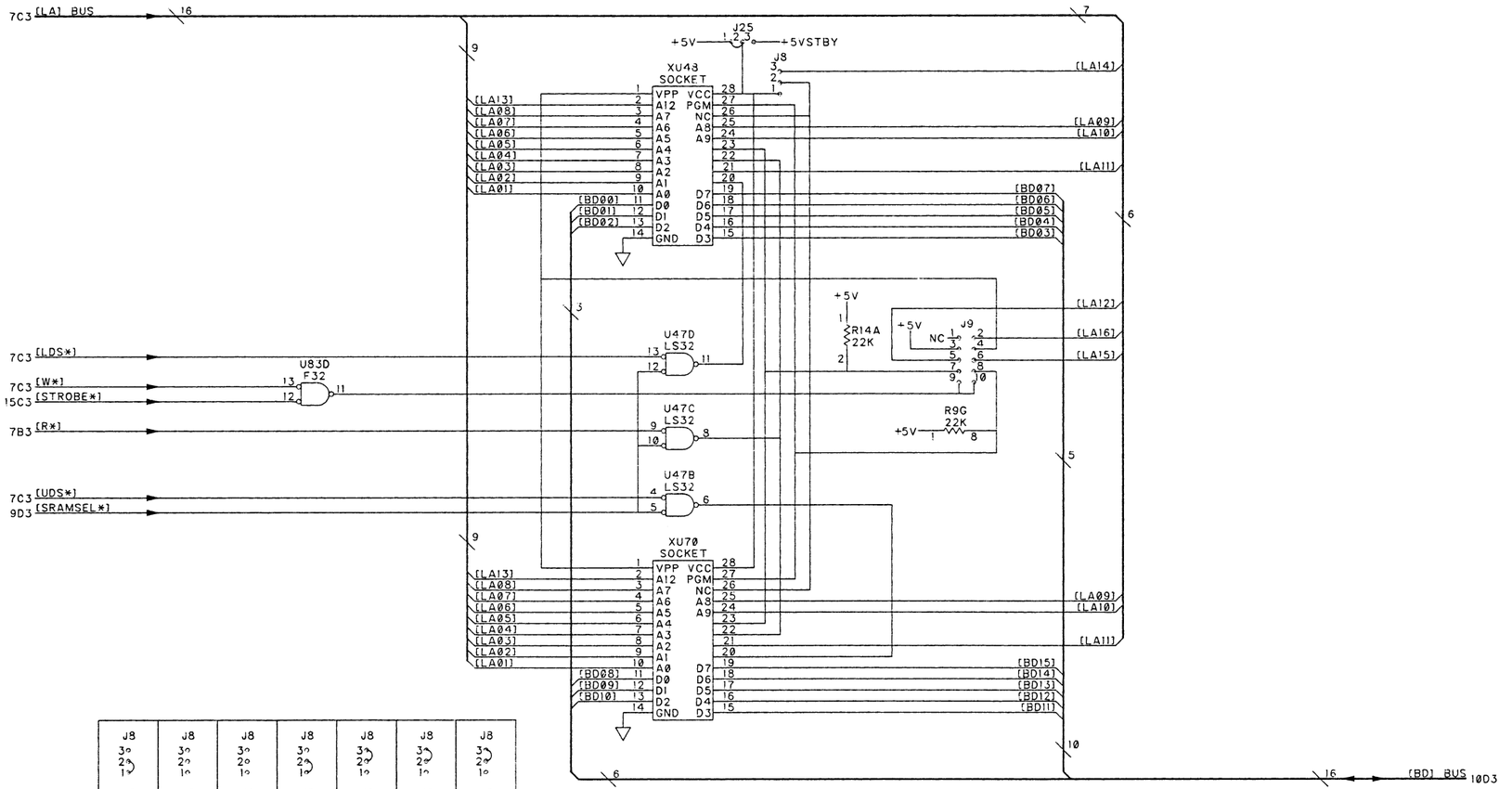


FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 15 OF 22)



ROM/RAM SOCKETS

63DW3450B REV B SH 16 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 16 OF 22)

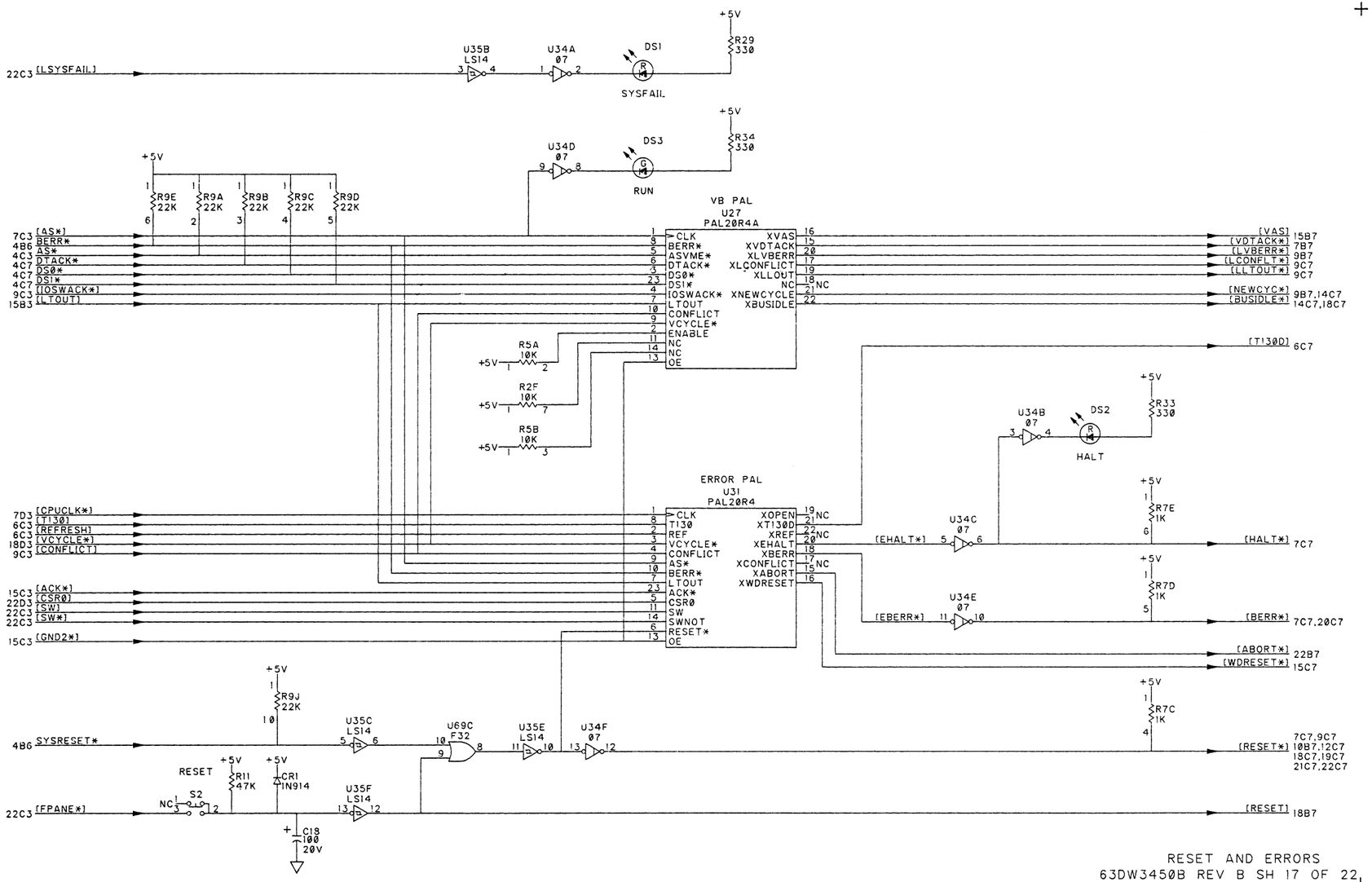
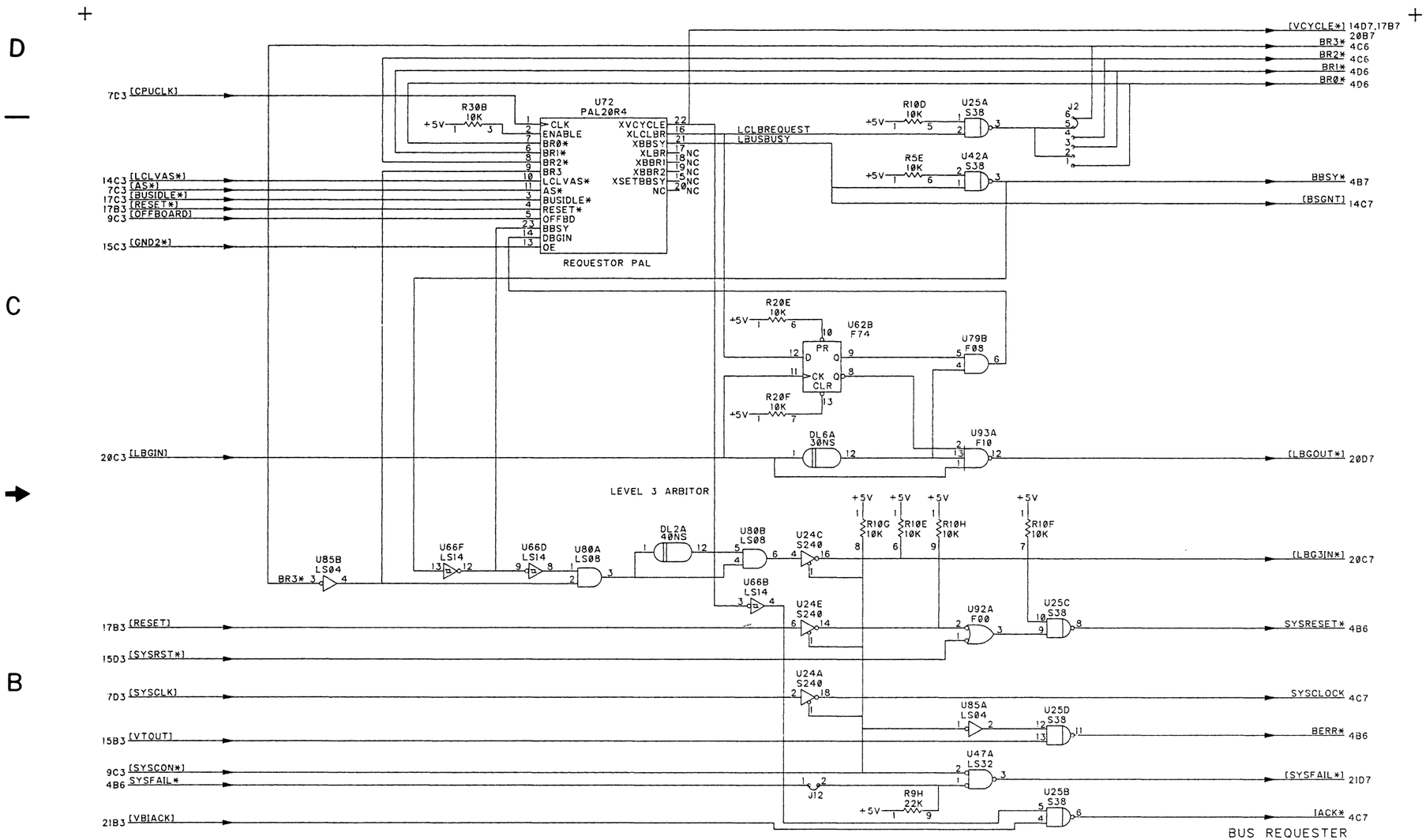
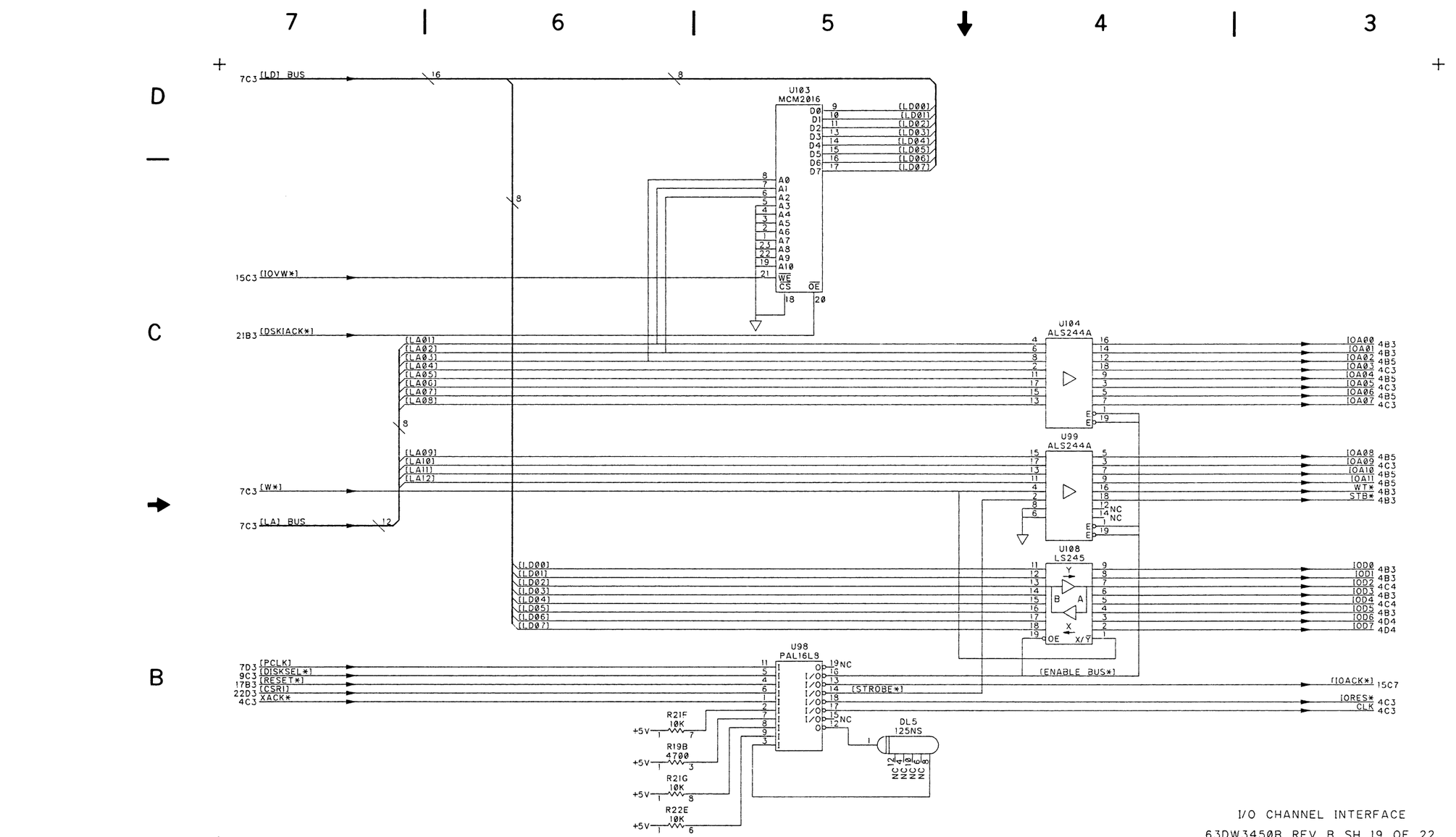


FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 17 OF 22)



63DW3450B REV B SH 18 OF 22

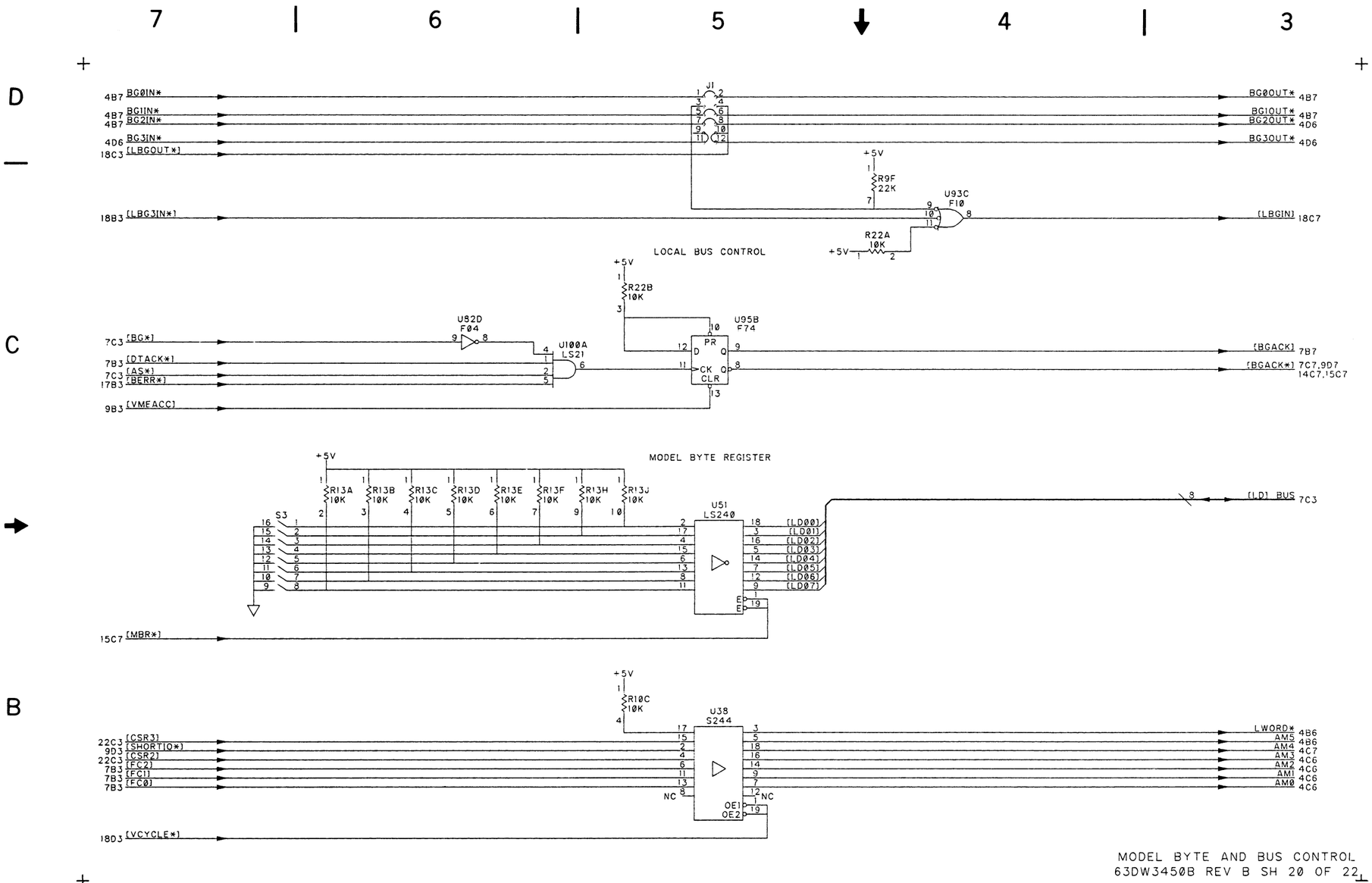
FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 18 OF 22)



I/O CHANNEL INTERFACE

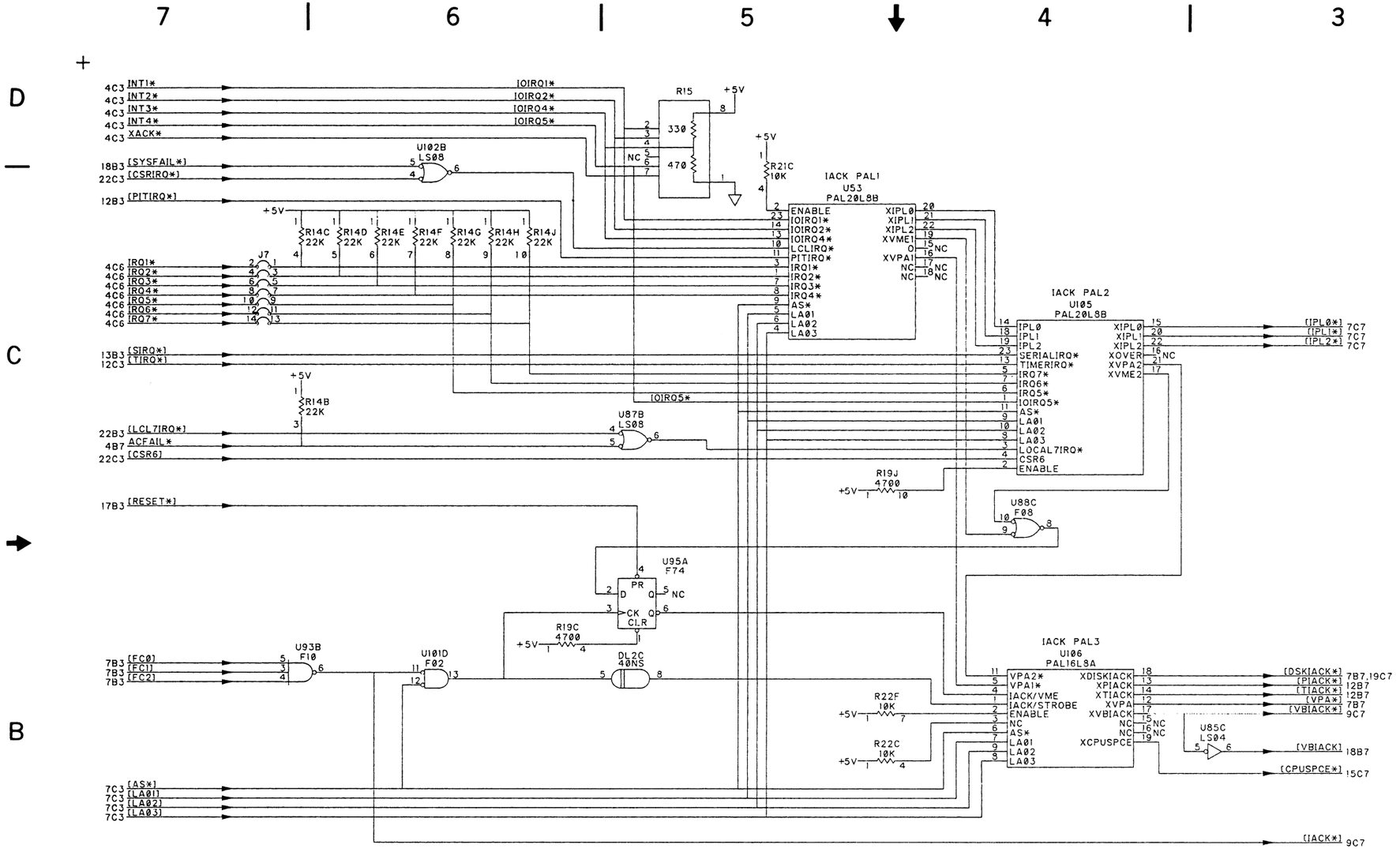
63DW3450B REV B SH 19 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 19 OF 22)



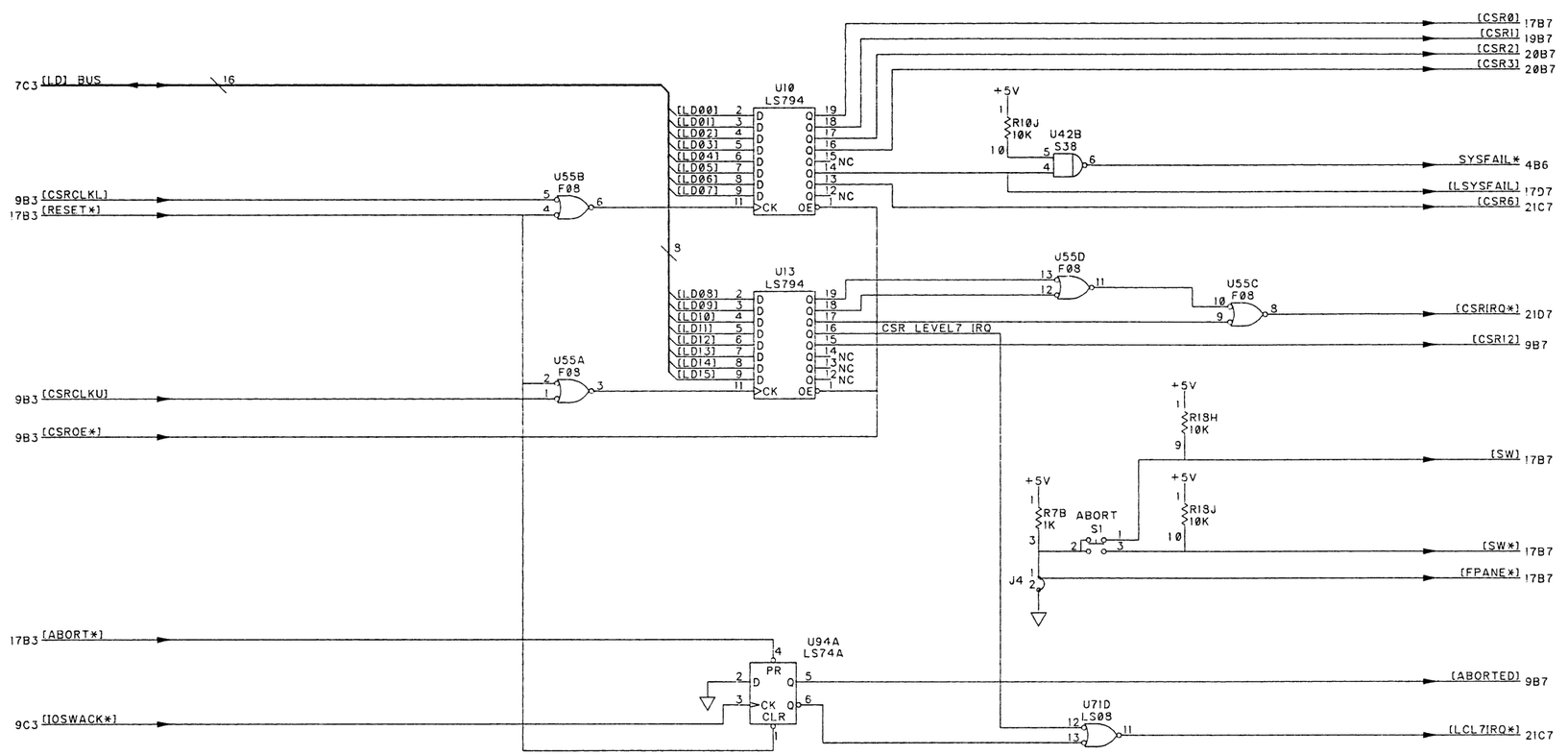
MODEL BYTE AND BUS CONTROL
63DW3450B REV B SH 20 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 20 OF 22)



INTERRUPT HANDLER
63DW3450B REV B SH 21 OF 22

FIGURE 5-5. MVME1Ø4 SCHEMATIC DIAGRAM (SHEET 21 OF 22)



CSR
63DW3450B REV A SH 22 OF 22

FIGURE 5-5. MVME104 SCHEMATIC DIAGRAM (SHEET 22 OF 22)

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL Ø1-W3438BØ1,BØ2 AND BØ3.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   □ DENOTES - ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING, FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:
   6 A6
   SHEET — ZONE
9. INSTALL ON MVME1Ø7 (Ø1-W3438BØ3), ONLY.
10. INSTALL ON MVME1Ø6 (Ø1-W3438BØ2), ONLY.
11. INSTALL ON MVME1Ø5 (Ø1-W3438BØ1), ONLY.
12. INSTALL JUMPERS J22,J23,AND J24 PER CHART:

REF DES	MVME1Ø5	MVME1Ø6	MVME1Ø7
J22	INSTALLED	OPEN	INSTALLED
J23	OPEN	INSTALLED	INSTALLED
J24	INSTALLED	INSTALLED	INSTALLED

Y2	
XR1	
U107	
S4	
R34	R1,16,17,20
P2	
J27	
DS3	
DL6	DL4
CR1	
C64	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	

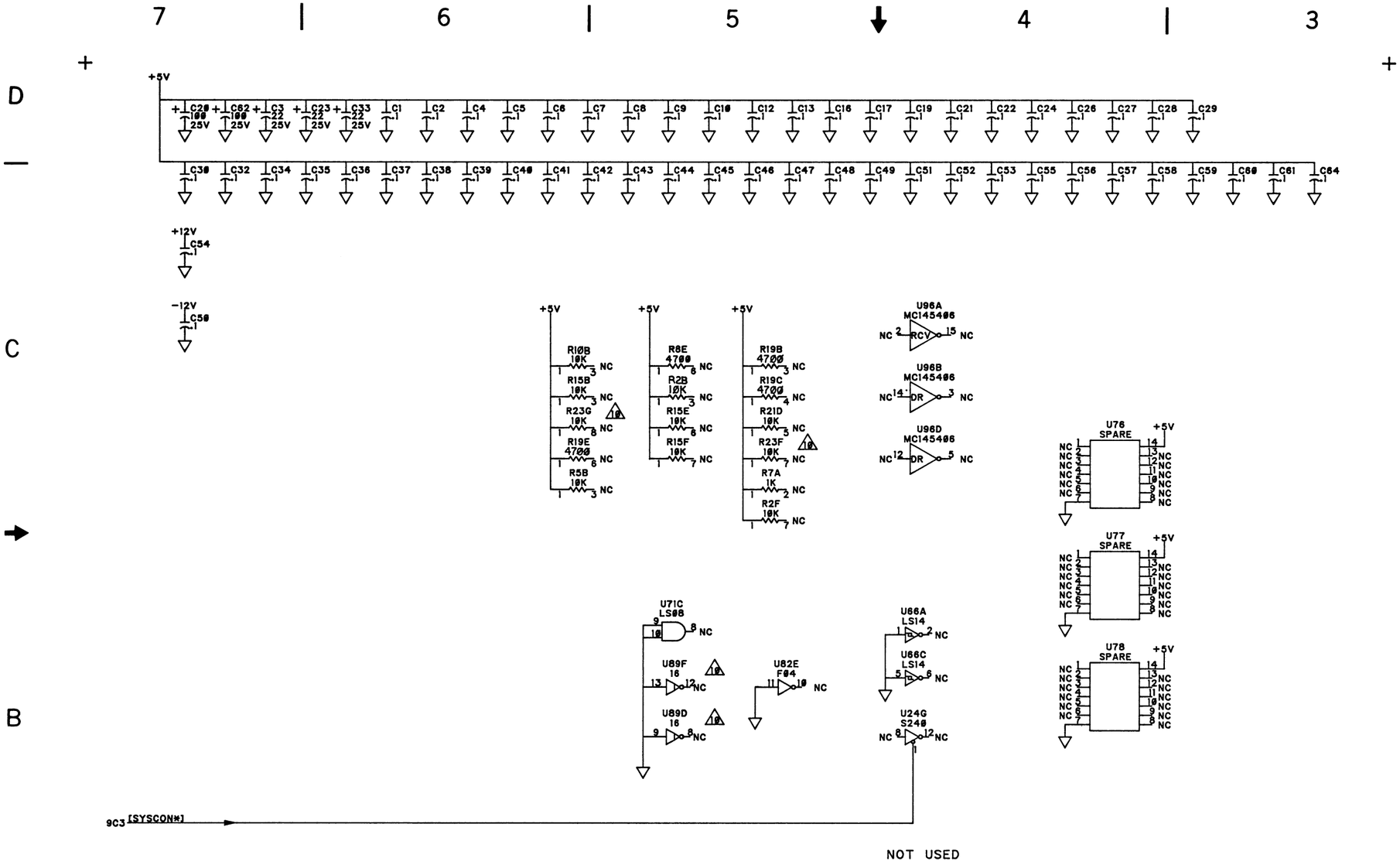
TABLE 1

REF DES	TYPE 4	GND	+5V	SH
DL1	25ØNS	7	14	15
DL2	3ØNS	7	14	6,14,18
DL3	1ØØNS	7	14	6
DL5	5ØØNS	7	14	2Ø
DL6	3ØNS	7	14	9,18,22
U1	M5K4256L	4	12	8
U2	M5K4256L	4	12	8
U3	M5K4256L	4	12	8
U4	M5K4256L	4	12	8
U5	M5K4256L	4	12	8
U6	M5K4256L	4	12	8
U7	M5K4256L	4	12	8
U8	M5K4256L	4	12	8
U9	74F245	1Ø	2Ø	1Ø
U1Ø	74LS794	1Ø	2Ø	23
U11	74F543	12	24	14
U12	74F245	1Ø	2Ø	1Ø
U13	74LS794	1Ø	2Ø	23
U14	74F543	12	24	14
U15	M5K4256L	4	12	8
U16	M5K4256L	4	12	8
U17	M5K4256L	4	12	8
U18	M5K4256L	4	12	8
U19	M5K4256L	4	12	8
U2Ø	M5K4256L	4	12	8
U21	M5K4256L	4	12	8
U22	M5K4256L	4	12	8
U23	74F157	8	16	11
U24	74S24Ø	1Ø	2Ø	2,9,18
U25	74S38	7	14	18
U26	74F157	8	16	11
U27	PAL16R4	12	24	17
U28	PAL2ØL8A	12	24	14
U29	74S244	1Ø	2Ø	7
U3Ø	PAL2ØL8A	12	24	9
U31	PAL16R4	12	24	17
U32	74FØØ	7	14	6
U33	74FØØ	7	14	6,7
U34	7407	7	14	17
U35	74LS14	7	14	6,7,17
U36	MC68Ø1Ø	53	14	7
U36	MC68Ø1Ø	16	49	7
U37	74S244	1Ø	2Ø	14
U38	74S244	1Ø	2Ø	21
U39	74S51	7	14	6,11
U4Ø	74F74	7	14	6,7
U41	74LS393	7	14	15
U42	74S38	7	14	15,18,19,23
U43	74LS244	1Ø	2Ø	9
U44	74ALS645	1Ø	2Ø	14
U45	PAL2ØL8B	12	24	9
U46	74LS74A	7	14	15
U47	74LS32	7	14	16,18
XU48	SOCKET			16
U49	74ALS645	1Ø	2Ø	14
U5Ø	74LS682	1Ø	2Ø	9
U51	74LS24Ø	1Ø	2Ø	21
U52	74LS682	1Ø	2Ø	9
U53	PAL2ØL8A	12	24	22

TABLE 1 CONT.

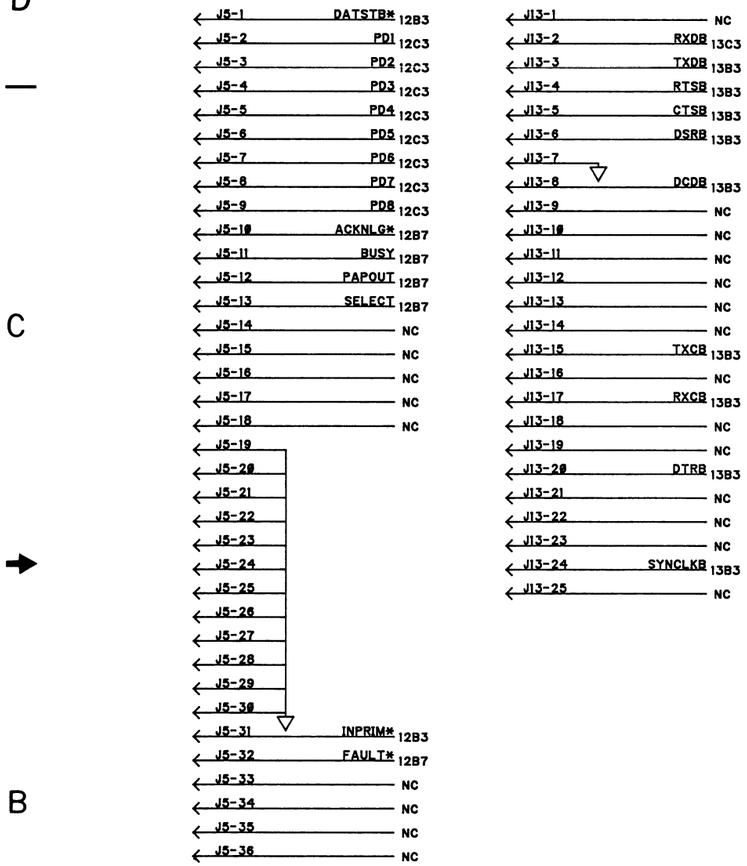
REF DES	TYPE 4	GND	+5V	+12V	-12V	SH
U54	74F74	7	14			6,7
U55	74FØ8	7	14			23
XU56	27512	14	28			1Ø
U57	74ALS645	1Ø	2Ø			14
U58	PAL16L8A	1Ø	2Ø			9
U59	74LS682	1Ø	2Ø			9
U6Ø	MC1455	1	8			6
U61	74FØ8	7	14			15
U62	74F74	7	14			18
XU63	27512	14	28			1Ø
U64	PAL16L8	1Ø	2Ø			15
U65	74S244	1Ø	2Ø			12
U66	74LS14	7	14			15,18
U67	74F245	1Ø	2Ø			12
U68	74F64	7	14			6
U69	74F32	7	14			6,9,14,17
XU7Ø	SOCKET					16
U71	74LSØ8	7	14			2,13,23
U72	PAL2ØR4	12	24			18
U73	MC68238	38	12			12
U74	MC3456	7	14			15
U75	SN75175	8	16			13
U76	SPARE					2
U77	SPARE					2
U78	SPARE					2
U79	74FØ8	7	14			6,18
U8Ø	74LSØ8	7	14			6,18
U81	SN75174	8	16			13
U82	74FØ4	7	14			2,6,11,12,13,21
U83	74F32	7	14			7,14,16
U84	Z8530	31	9			13
U85	74LSØ4	7	14			2,13,15,18,22
U86	74S3Ø	7	14			7
U87	74LSØ8	7	14			9,1Ø,2Ø,22
U88	74FØØ	7	14			1Ø,14,2Ø
U89	7416	7	14			2,19
U9Ø	MC145406	9	16	1	8	13
U91	74FØ4	7	14			6,7,9,15,2Ø
U92	74FØØ	7	14			9,18
U93	74F1Ø	7	14			18,21,22
U94	74LS74A	7	14			1Ø,23
U95	74S3Ø	7	14			2Ø
U96	MC145406	9	16	1	8	2,13
U97	74LS74	7	14			6,2Ø
U98	WD177Ø	14	15			19
U99	NCR538Ø	11	31			2Ø
U1ØØ	7407	7	14			19
U1Ø1	74LS21	7	14			21,22
U1Ø2	74F02	7	14			6,2Ø,22
U1Ø3	74LSØ8	7	14			2,22
U1Ø4	74LS138	8	16			22
U1Ø5	74F74	7	14			21,22
U1Ø6	PAL16R4	1Ø	2Ø			2Ø
U1Ø7	74LS244	1Ø	2Ø			9,19
Y1	K1100	7	14			7
Y2	K1100	7	14			7

FIGURE 5-6. MVME1Ø5/1Ø6/1Ø7 SCHEMATIC DIAGRAM (SHEET 1 OF 23)



63DW3438B REV D SH 2 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 2 OF 23)



CONNECTORS

63DW3438B REV A SH 3 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 3 OF 23)

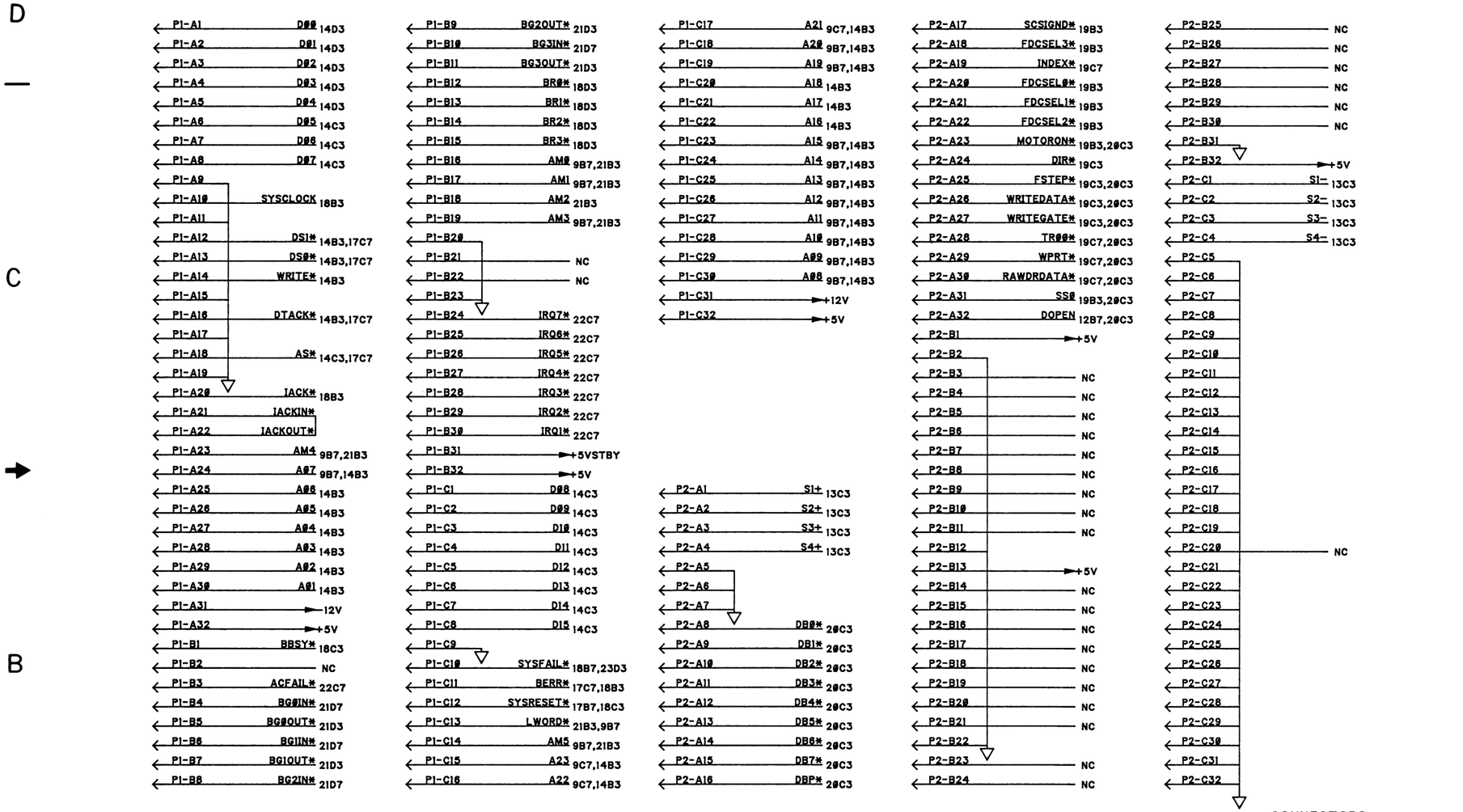
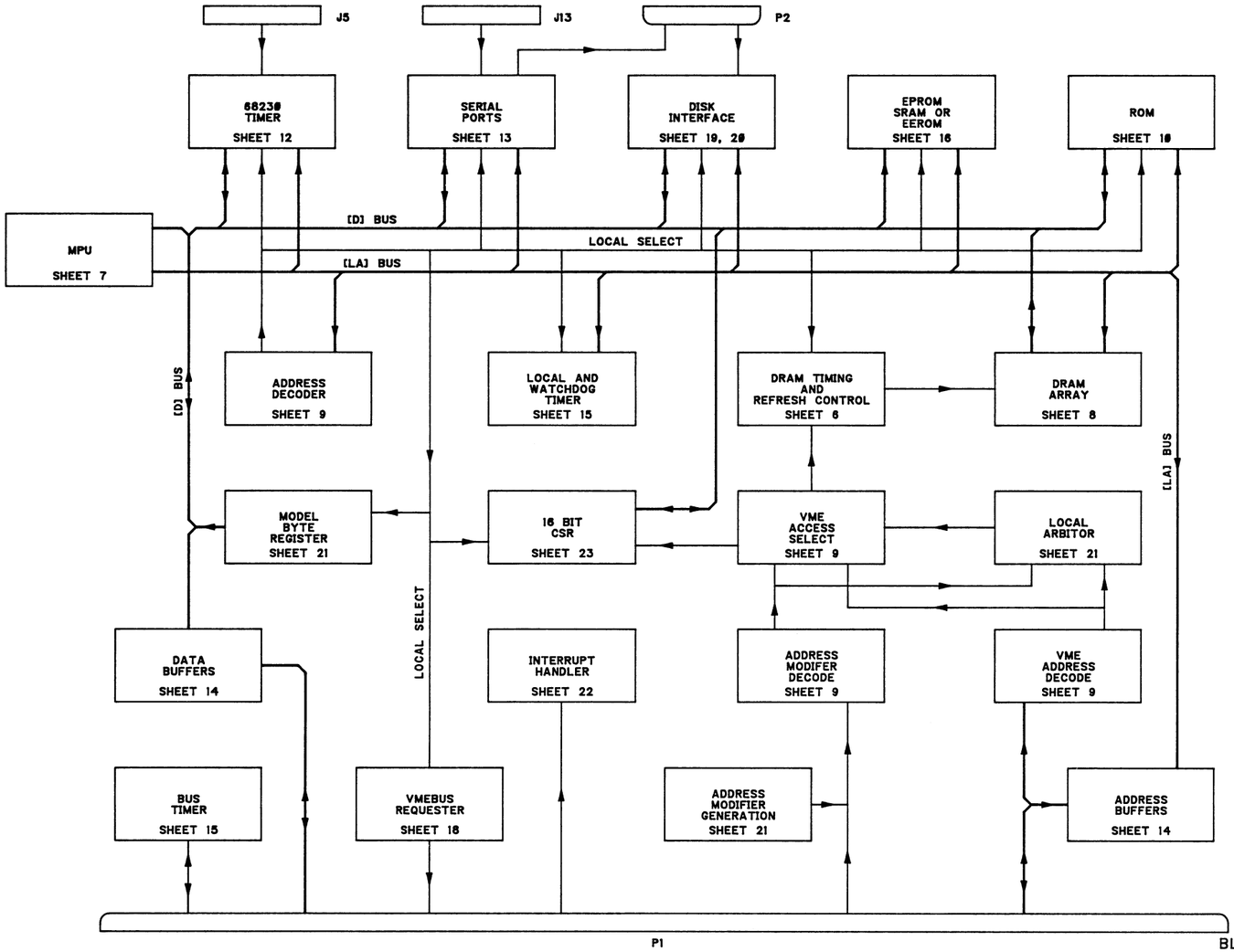
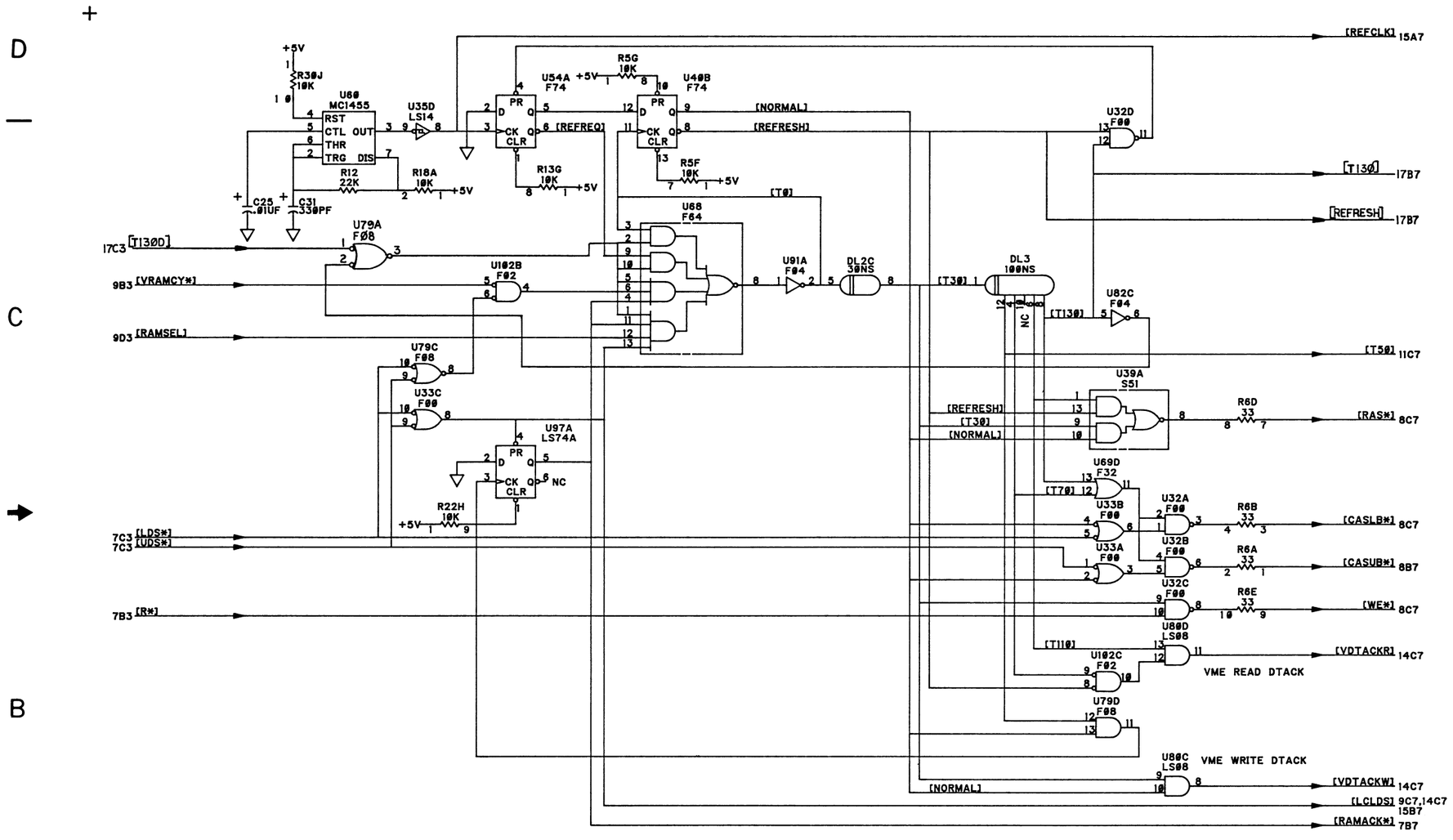


FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 4 OF 23)



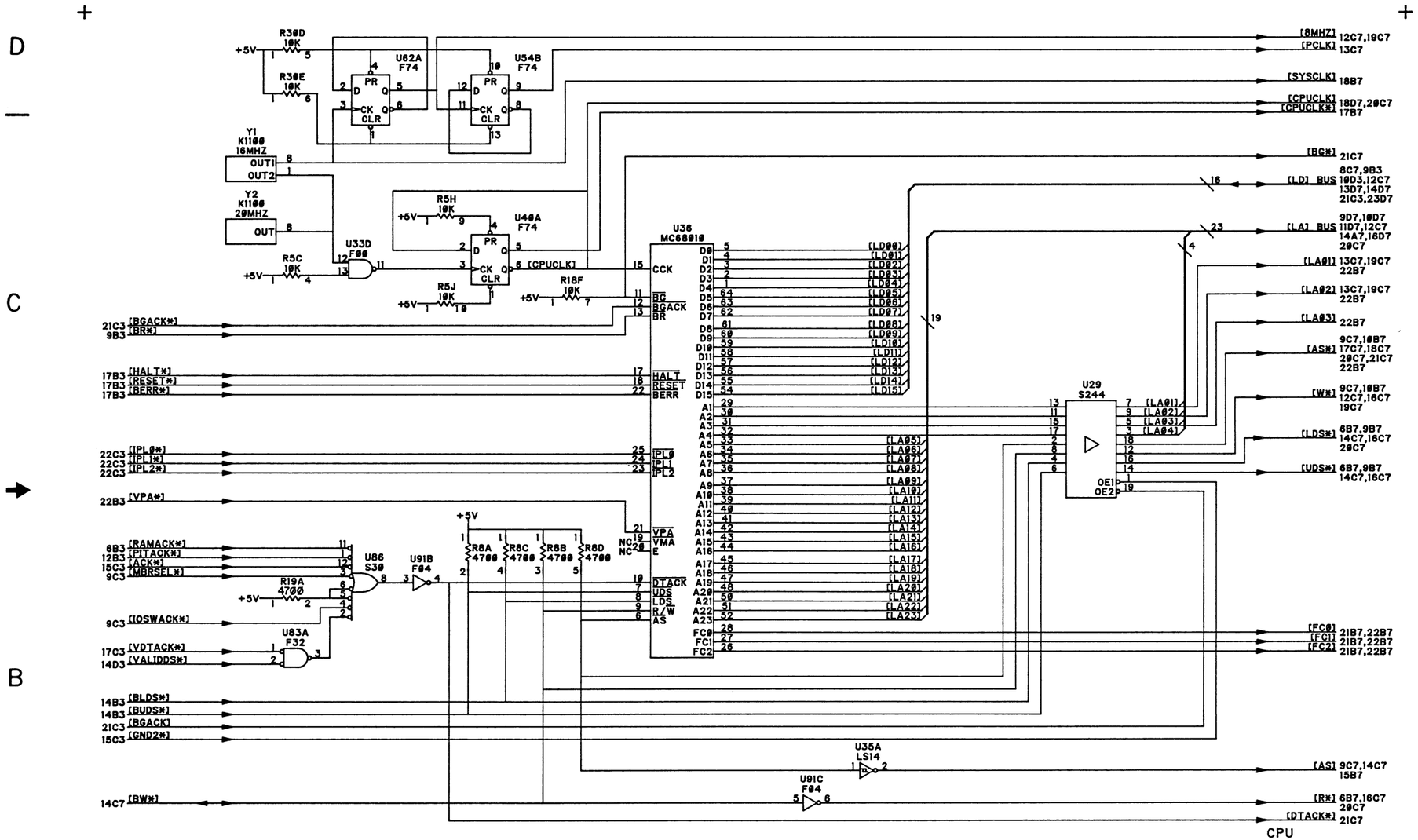
BLOCK DIAGRAM
63DW3438B REV A SH 5 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 5 OF 23)



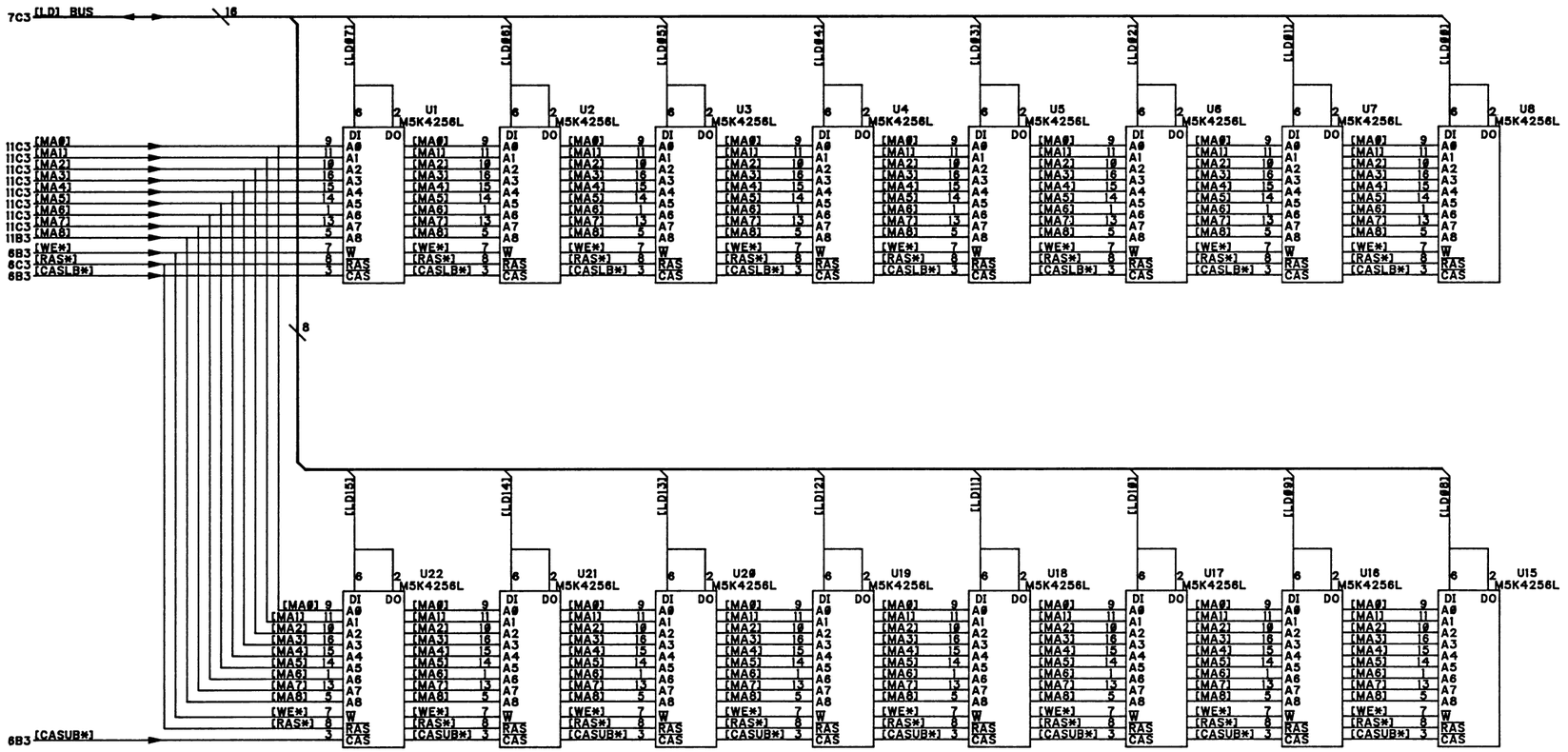
MEMORY TIMING
63DW3438B REV C SH 6 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM
(SHEET 6 OF 23)



63DW3438B REV D SH 7 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 7 OF 23)



RAM ARRAY
63DW3438B REV B SH 8 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM
(SHEET 8 OF 23)

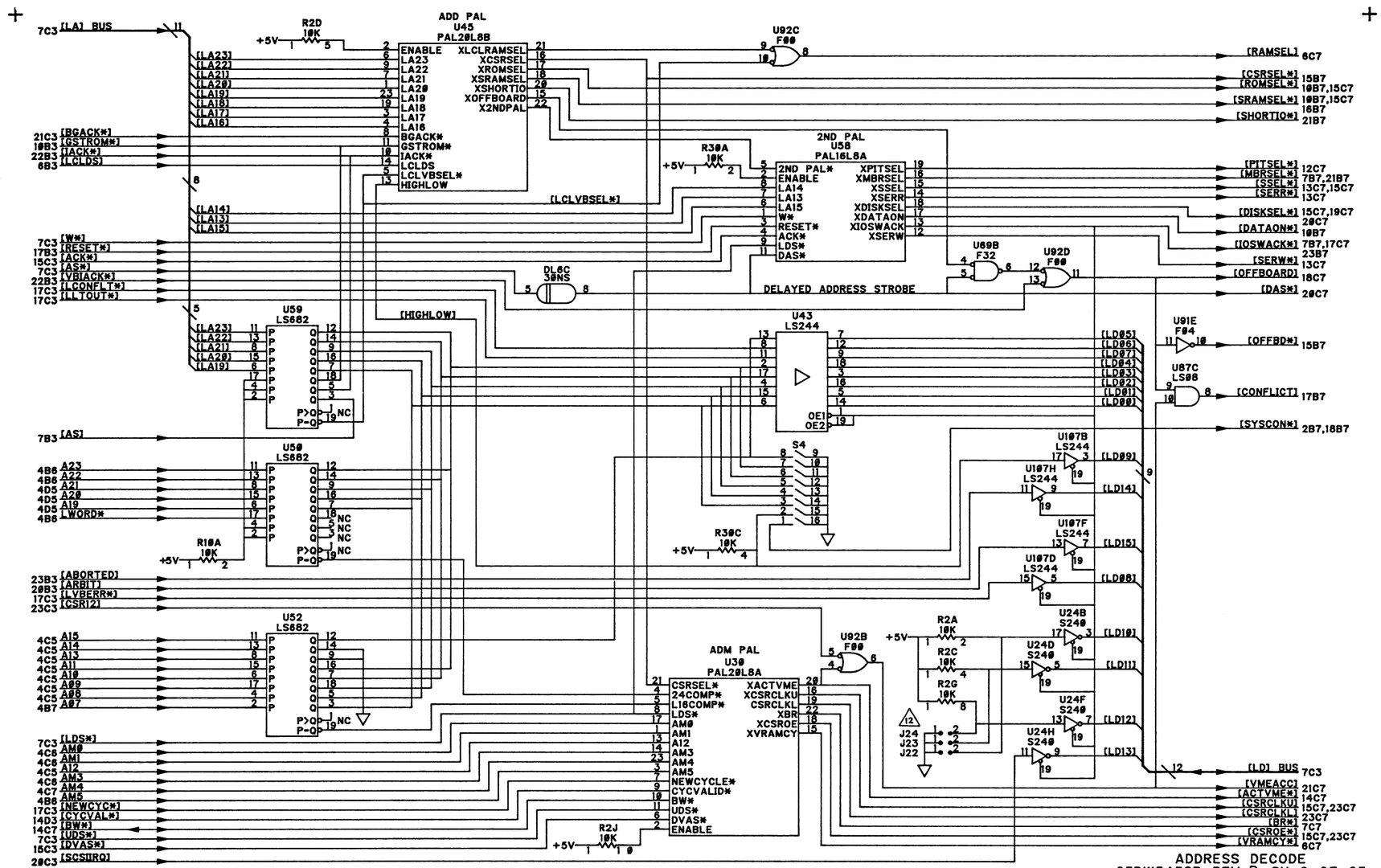
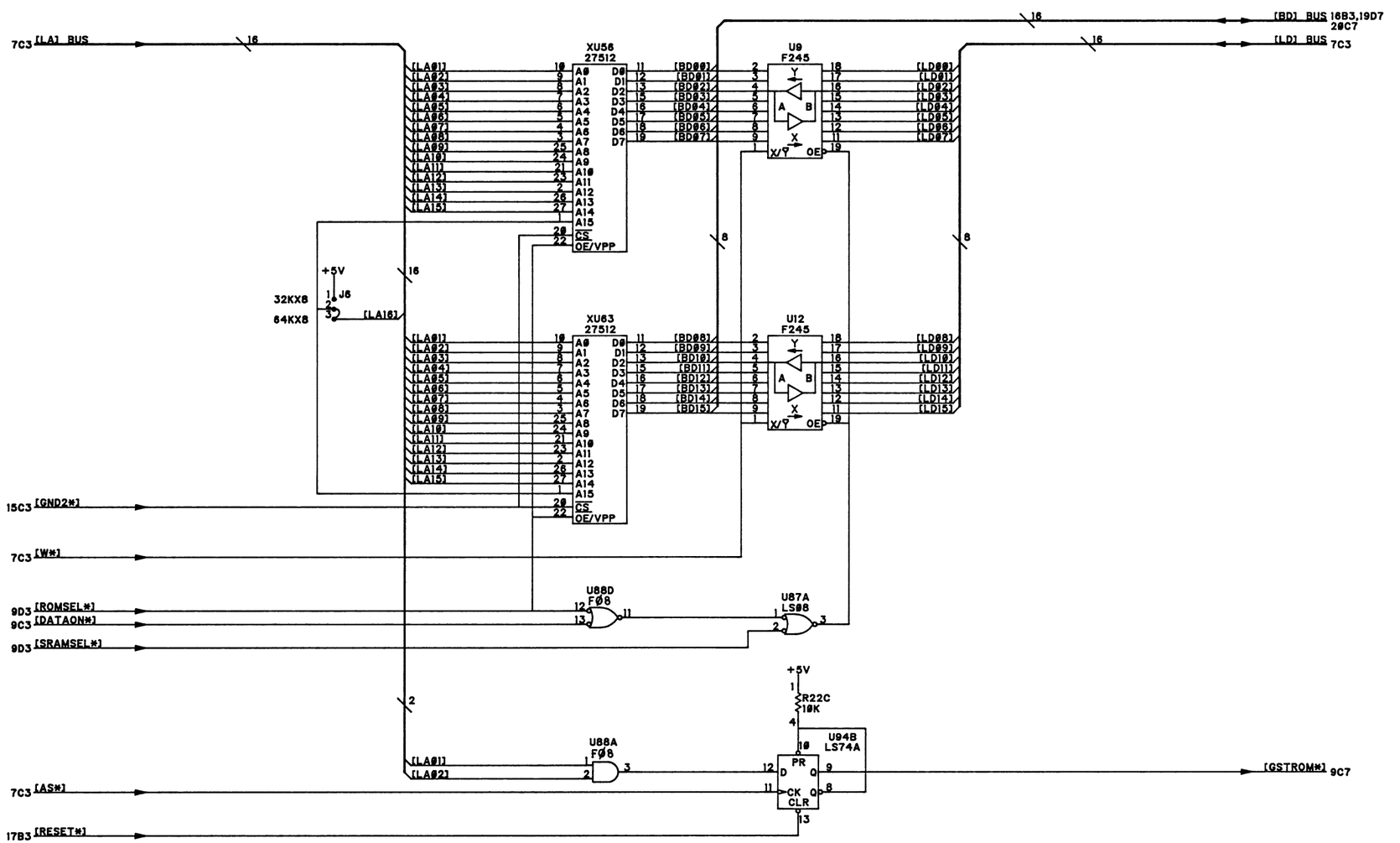
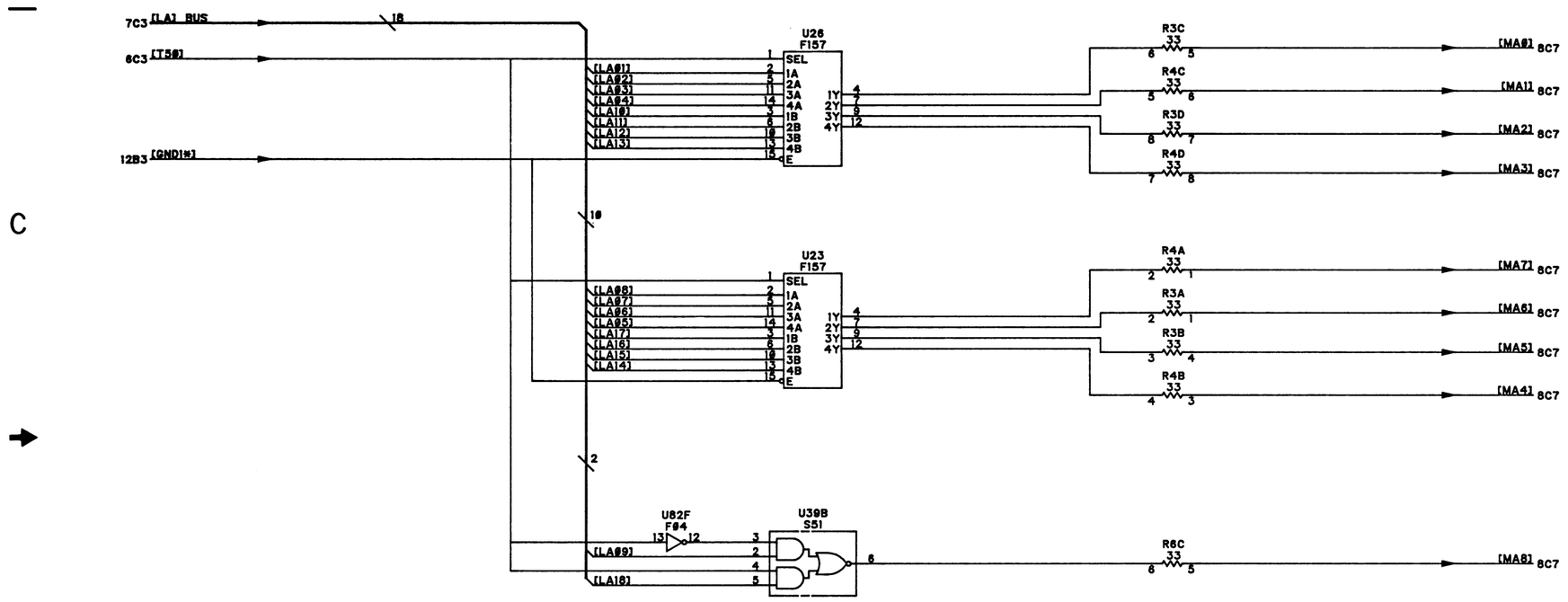


FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 9 OF 23)



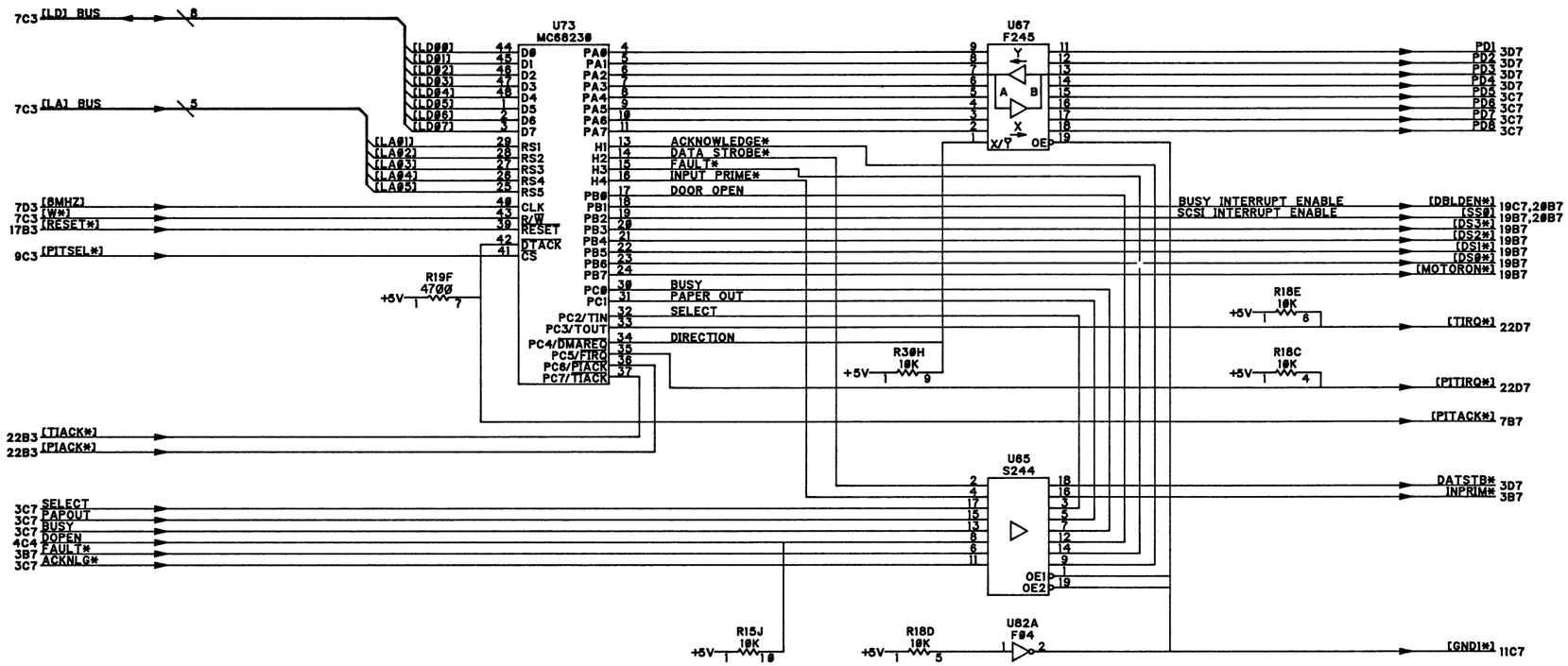
EPROM
63DW3438B REV D SH 1Ø OF 23

FIGURE 5-6. MVME1Ø5/1Ø6/1Ø7 SCHEMATIC DIAGRAM (SHEET 1Ø OF 23)



MEMORY ADDRESS MUX
63DW3438B REV A SH 11 OF 23

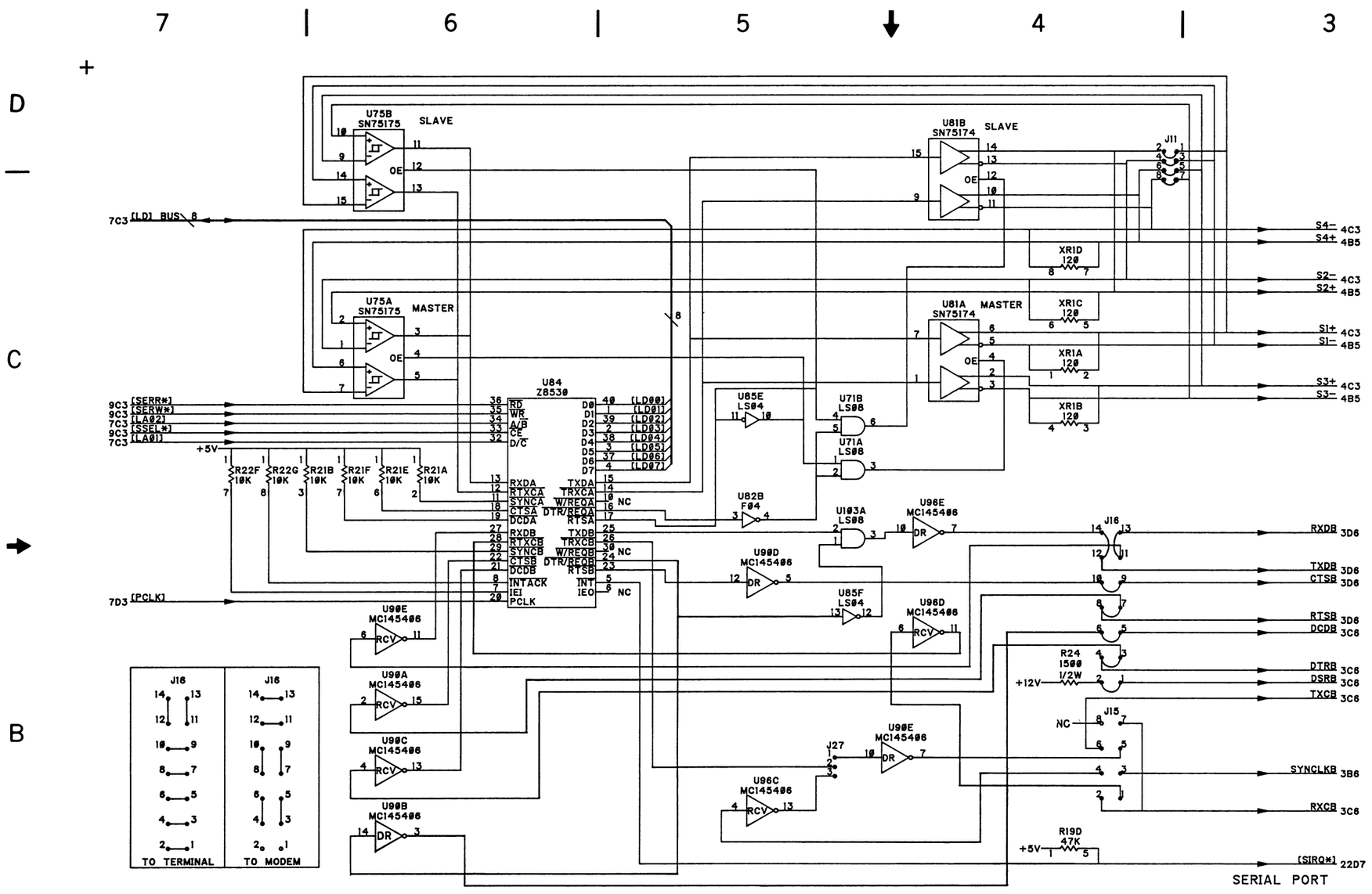
FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM
(SHEET 11 OF 23)



TIMER

63DW3438B REV B SH 12 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 12 OF 23)



63DW3438B REV D SH 13 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 13 OF 23)

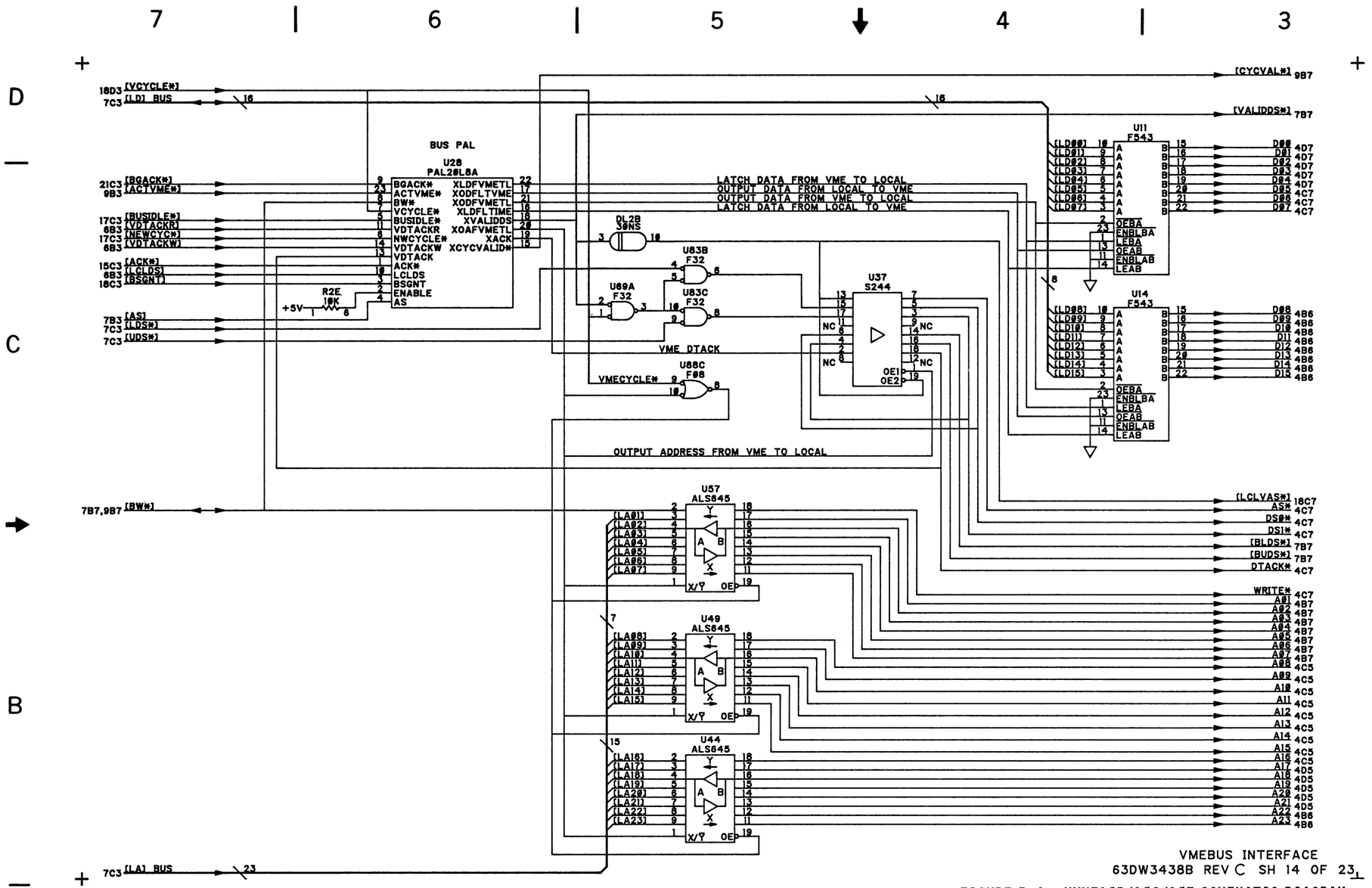
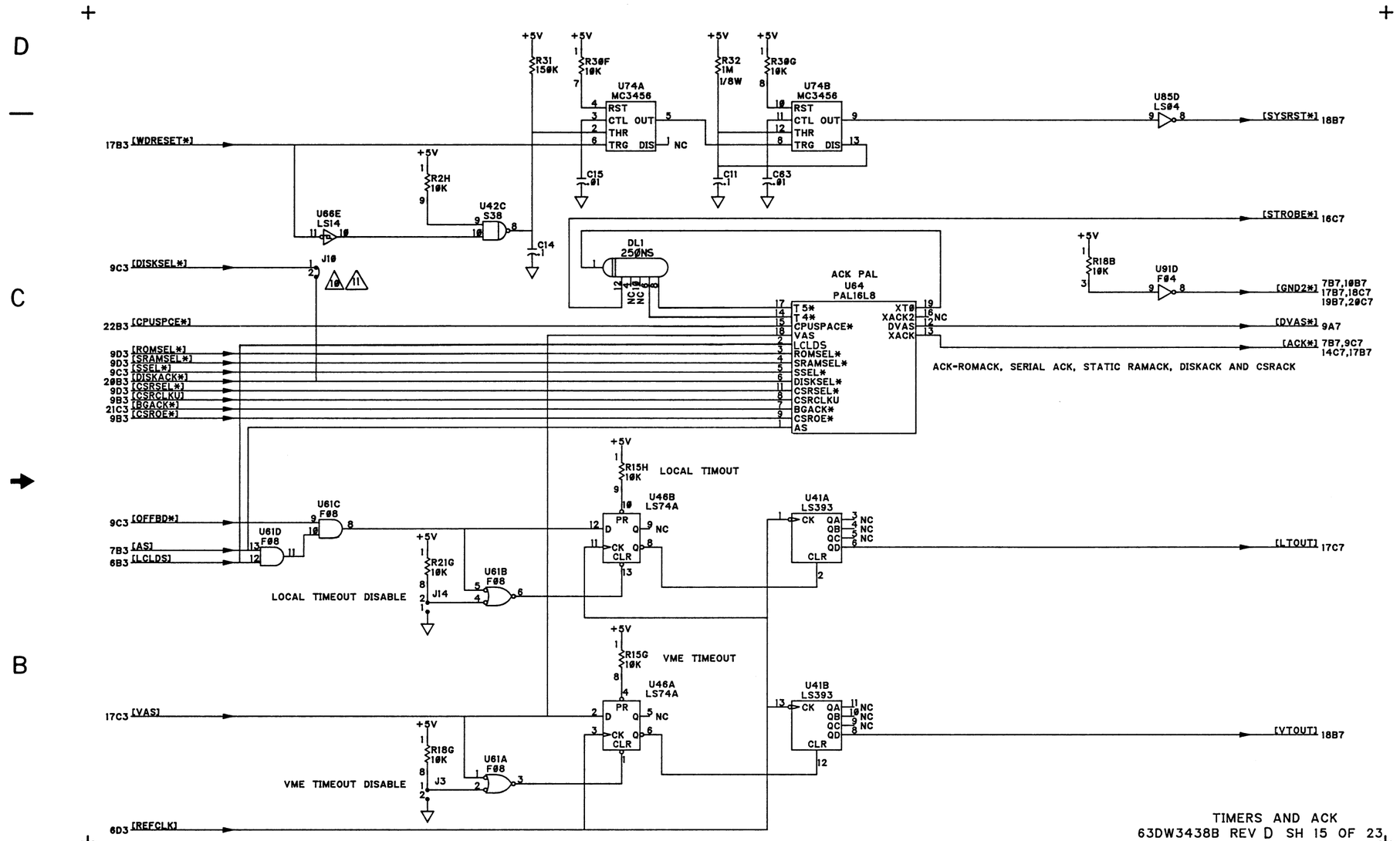
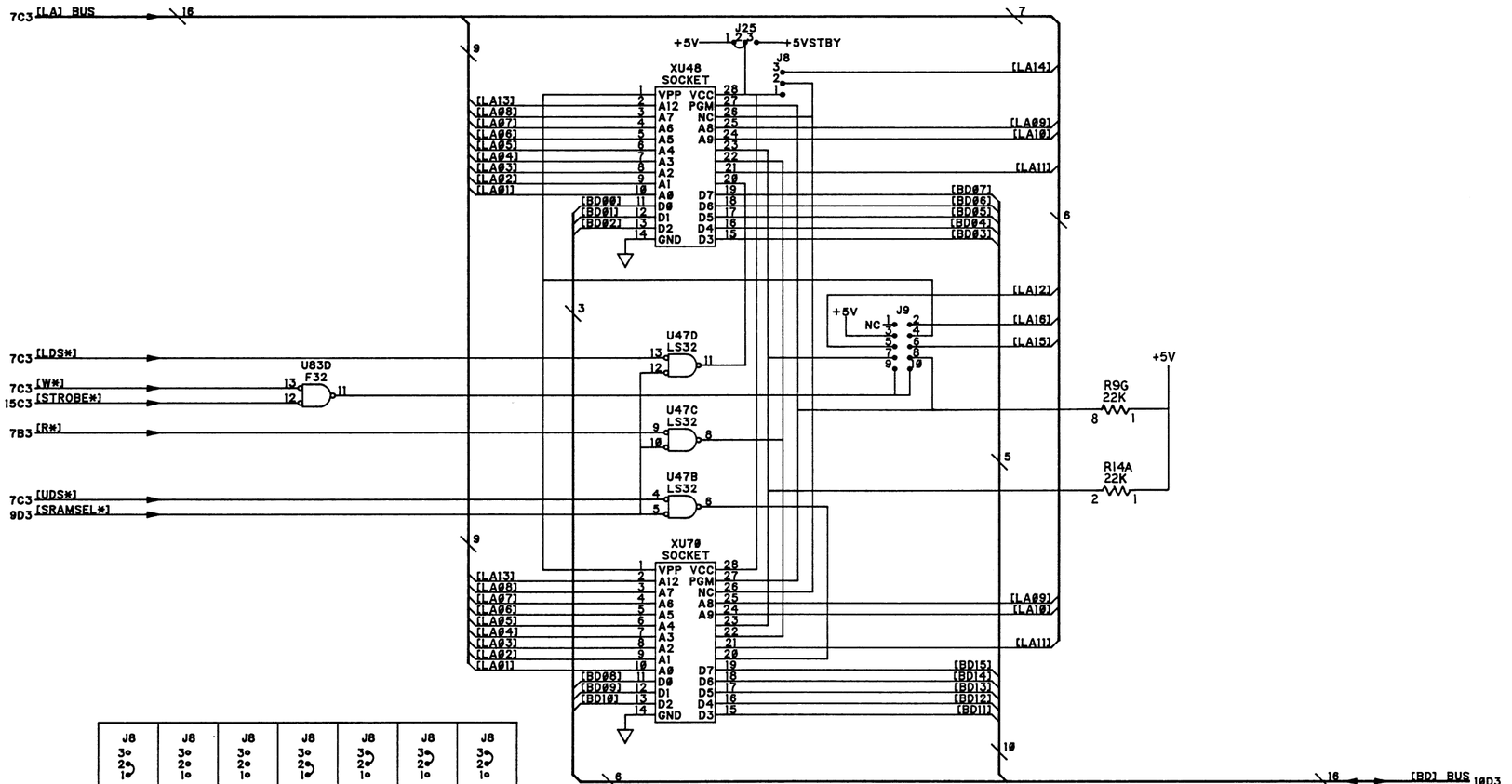


FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM
(SHEET 14 OF 23)



TIMERS AND ACK
63DW3438B REV D SH 15 OF 23

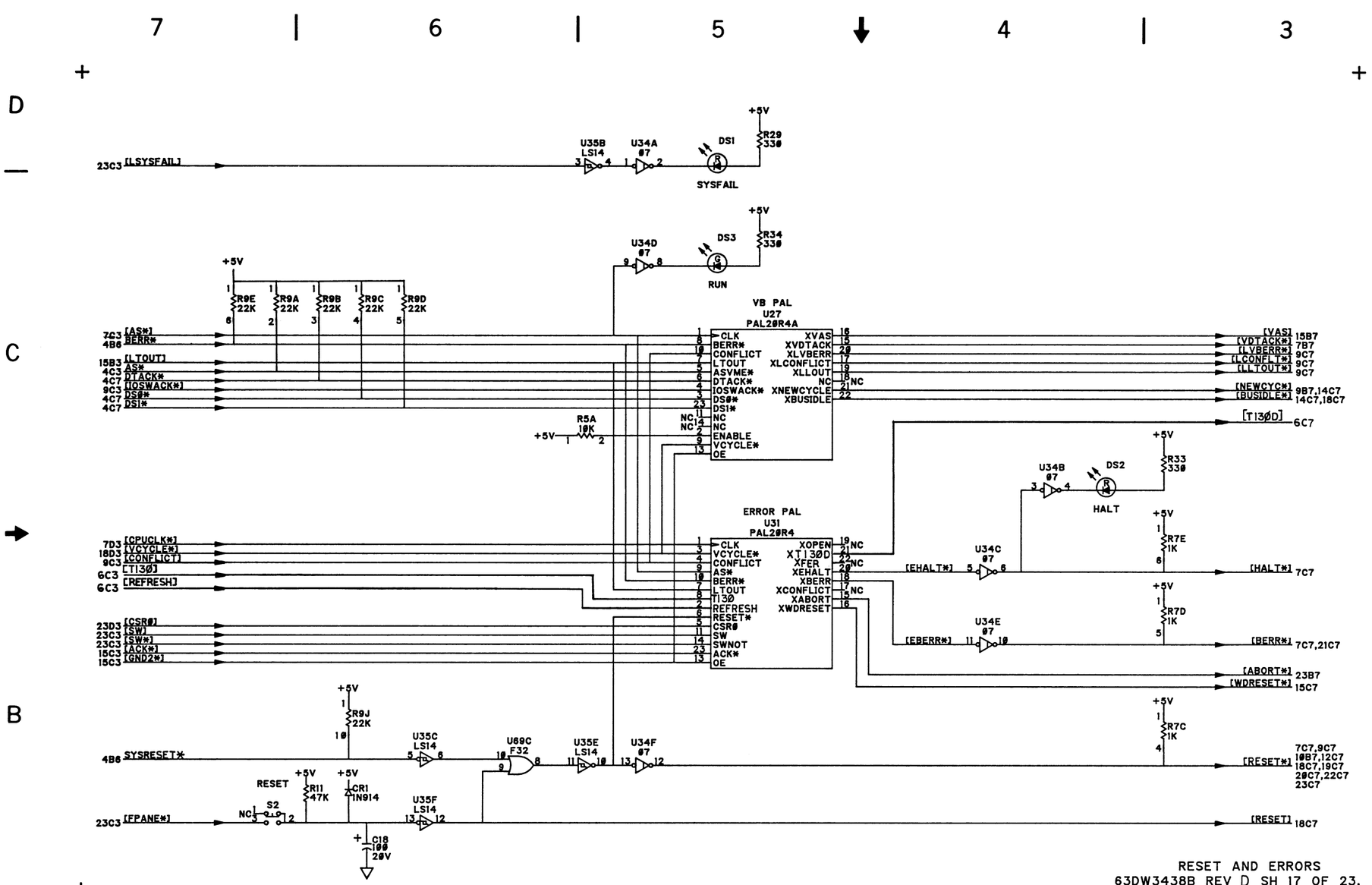
FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 15 OF 23)



ROM/RAM SOCKETS

63DW3438B REV D SH 16 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 16 OF 23)



RESET AND ERRORS
63DW3438B REV D SH 17 OF 23

FIGURE 5-6. MVME1Ø5/1Ø6/1Ø7 SCHEMATIC DIAGRAM (SHEET 17 OF 23)

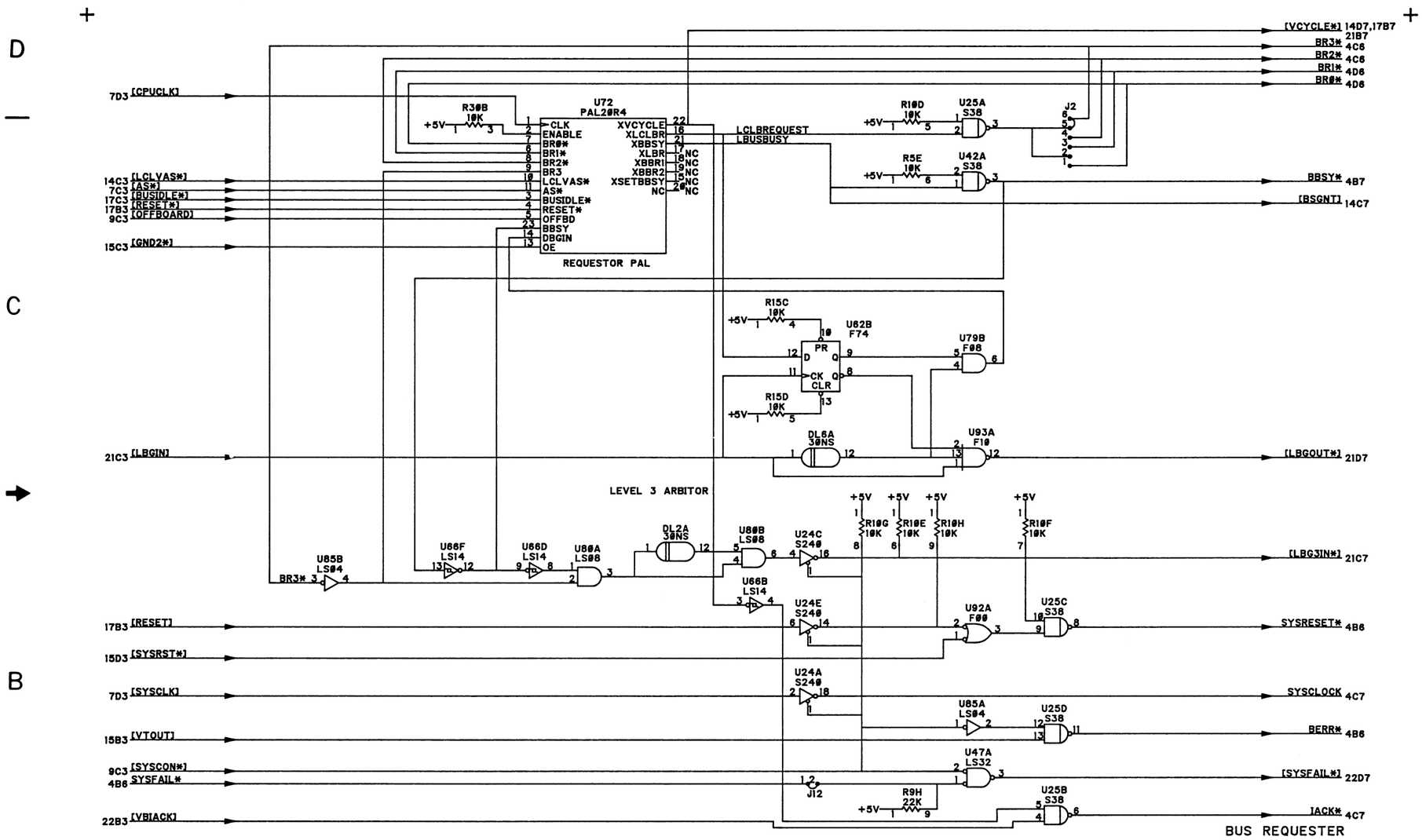
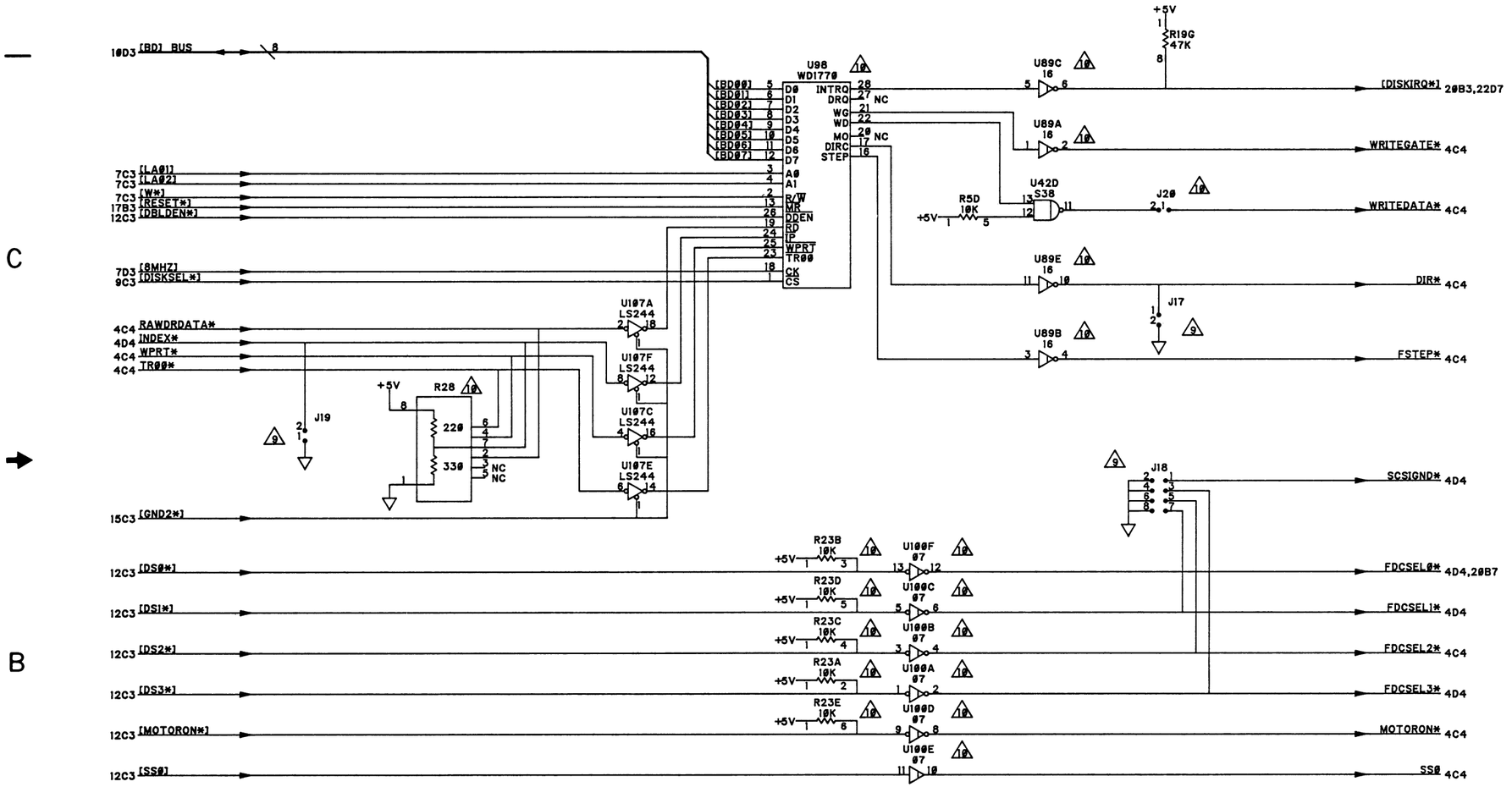


FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 18 OF 23)



FLOPPY INTERFACE
MVME106 ONLY

63DW3438B REV SH 19 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM
(SHEET 19 OF 23)

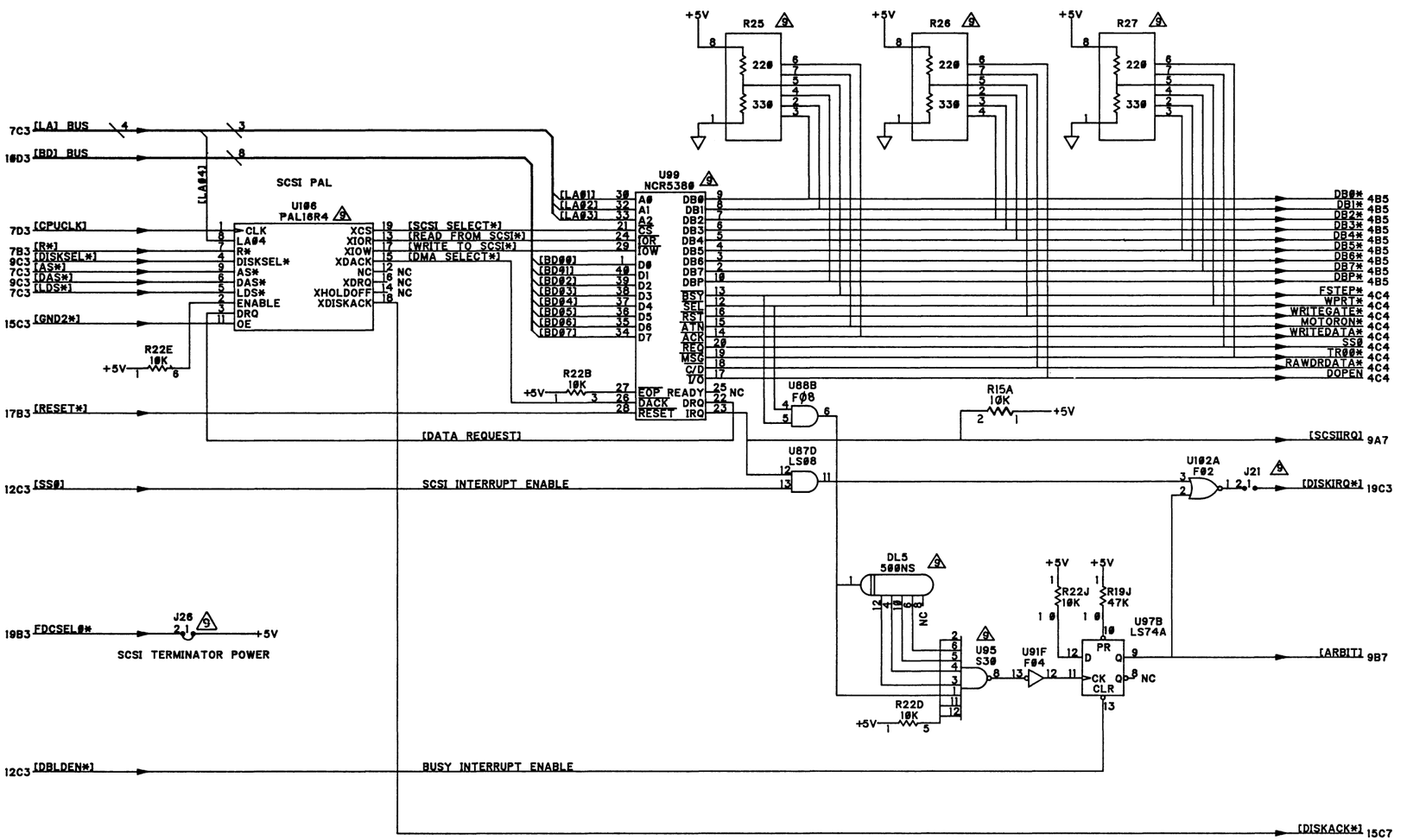
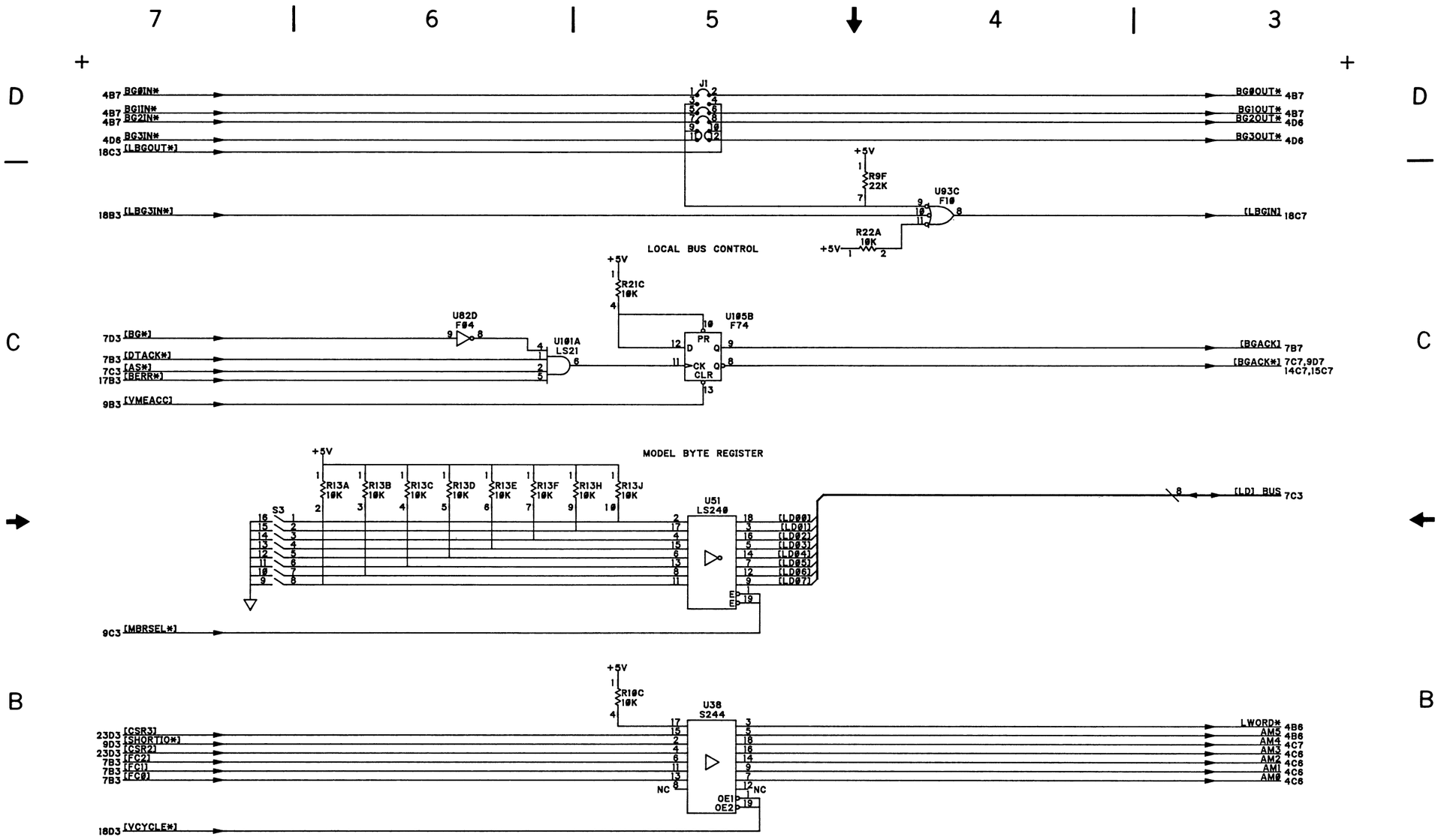
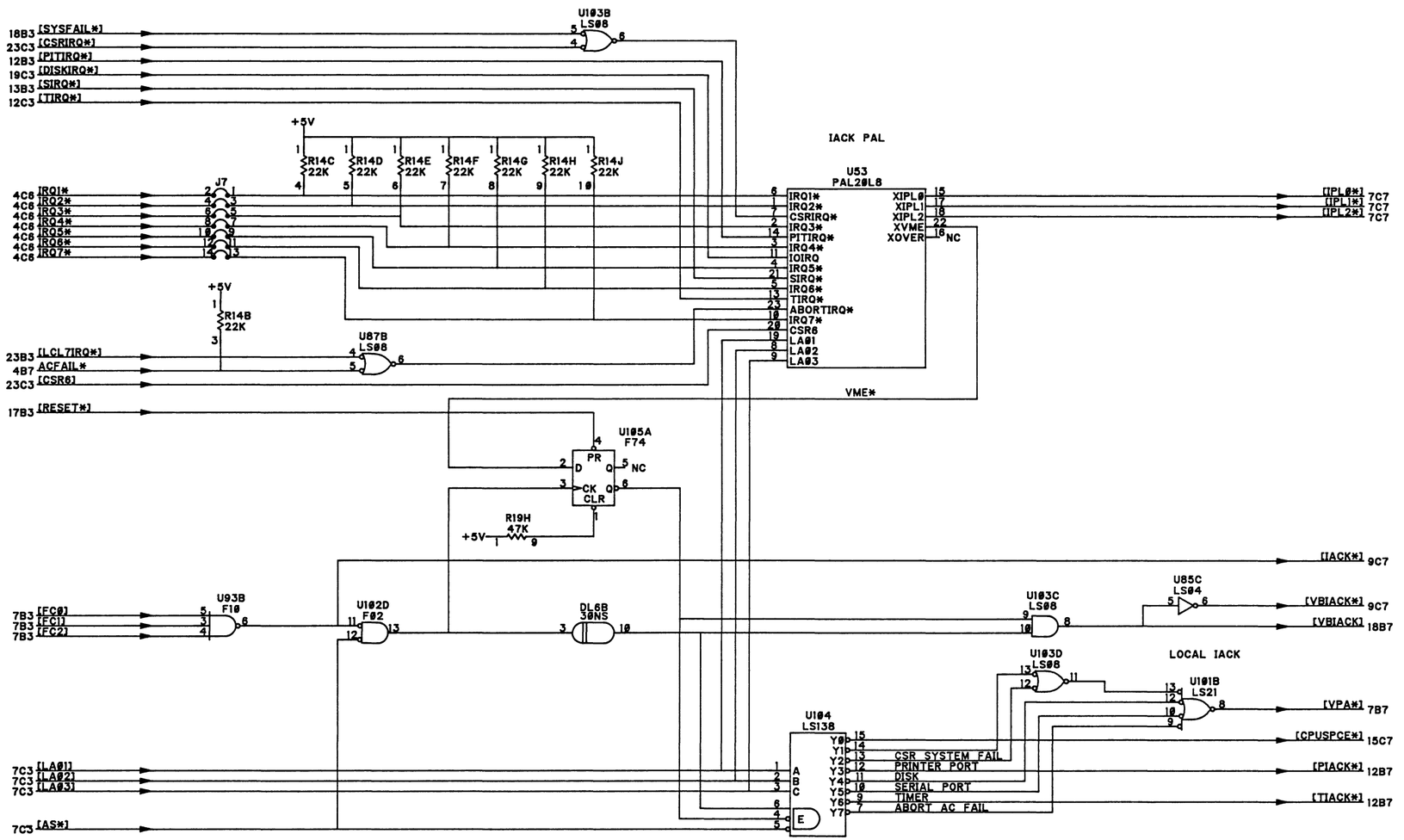


FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM
(SHEET 20 OF 23)



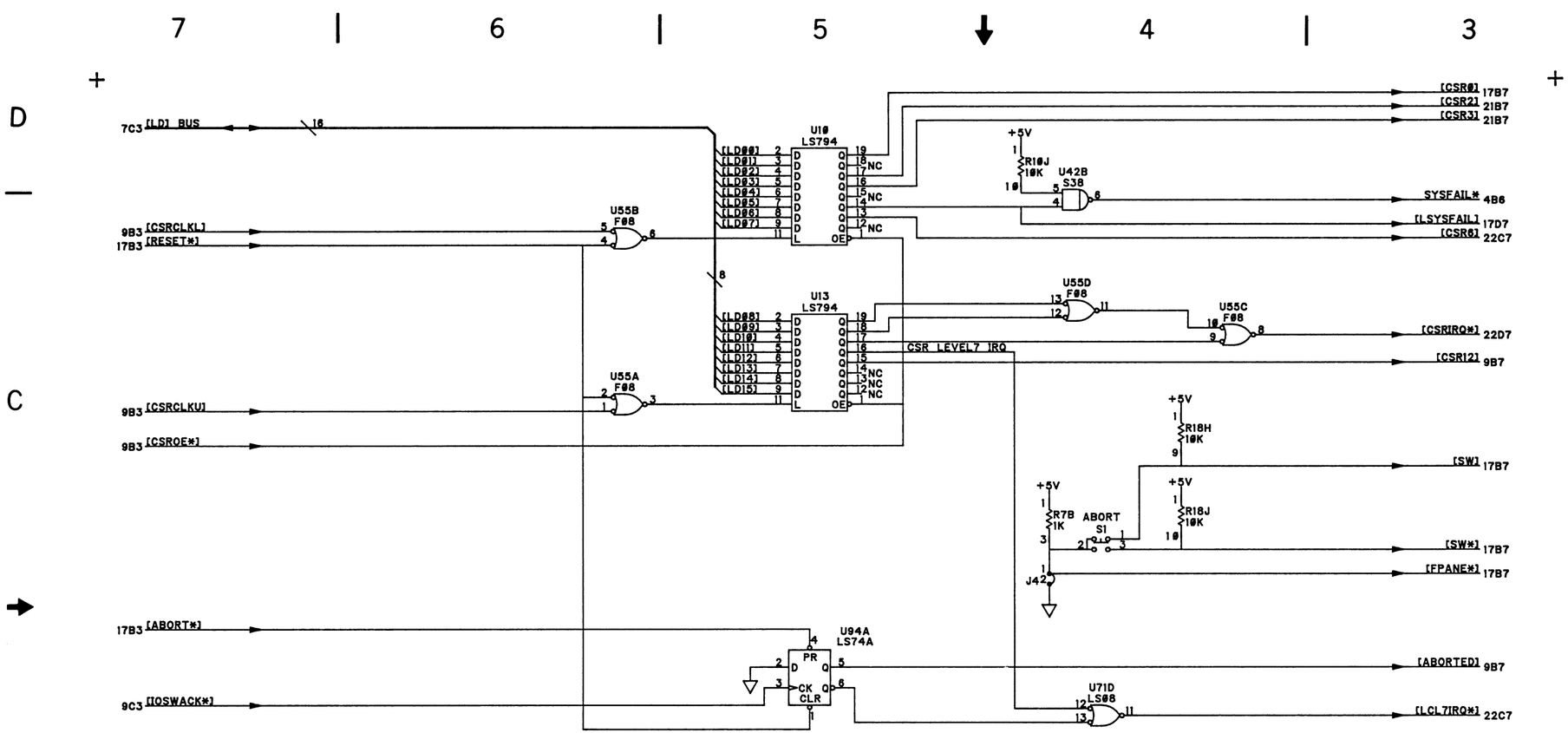
MODEL BYTE AND BUS CONTROL
63DW3438B REV B SH 21 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM (SHEET 21 OF 23)



INTERRUPT HANDLER
63DW3438B REV B SH 22 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM
(SHEET 22 OF 23)



CSR
63DW3438B REV B SH 23 OF 23

FIGURE 5-6. MVME105/106/107 SCHEMATIC DIAGRAM
(SHEET 23 OF 23)

APPENDIX A - ALLOWABLE RAM AND EPROM DEVICES

The following is a list of suggested RAM and EPROM devices for use with the SBC auxiliary RAM/ROM sockets U48 and U7Ø.

2K x 8 Static RAM		
MK481Ø2/12(B)-25	Mostek	2K x 8 Static RAM w/Battery and RTC
MK482Ø2(B)-25	Mostek	2K x 8 Static RAM w/Battery
DS122Ø	Dallas Semi-Connector	2K x 8 Static RAM w/Battery
8K x 8 Static RAM		
MK48AØ8-25	Mostek	8K x 8 Static RAM w/Battery
DS1225	Dallas Semi-Connector	8K x 8 Static RAM w/Battery
32K x 8 Static RAM		
DS1235	Dallas Semi-Connector	32K x 8 Static RAM w/Battery
2K x 8 EPROM		
NMC91817-25	National Semi-Connector	2K x 8 EPROM
8K x 8 EPROM		
NMC98C64-25	National Semi-Connector	8K x 8 EPROM

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