PRELIMINARY INFORMATION

MSC 4808

MULTIBUS PARITY MEMORY

PRELIMINARY USER'S MANUAL

This preliminary manual is incomplete and some parts are subject to change. A final version of the manual will be supplied when the MSC 4808 becomes available.

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7-26-83

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Chapter 1

Introduction

1.1 Description

The MSC 4808 is a Multibus-compatible[1] memory expansion board which can supply up to 512K bytes of additional memory to an existing Multibus system. The board can store and transfer either 8-bit or 16-bit (two byte) words, and provides circuitry for initialization, parity generation and checking, and parity error reporting.

Addressing may be controlled in 1K byte increments. A parity error generates an interrupt and places error information in a register which is available through a user selected I/O address.

The MSC 4808 is available in three separate configurations, depending on the amount of memory installed. Table 1-1 lists the available memory sizes and corresponding MSC part numbers.

CONFIGURATION	PART NUMBER
128K bytes	4808-003
256K bytes	4808-002
512K bytes	4808-001

Table 1-1
MSC 4808 CONFIGURATIONS

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1. Multibus is a registered trademark of Intel Corporation.

1.2 Specifications

1.2.1 General

Product:	MSC 4808 Expansion Memory Board
Bus:	IEEE 796 Multibus
Memory:	Up to 512K bytes parity DRAM using 64K elements (256K X 18)
Word Length:	16 bits (two 8-bit bytes)
Warranty:	One year, parts and labor

1.2.2 Power

Voltage required:	+5V DC
Operating Current:	5.0 A maximum
Standby Current:	3.5 A maximum
Power Down Current:	1.2 A maximum

1.2.3 Environment

	Operating	Storage
Temperature	0o to 50o C (32o TO 122o F)	-40o to 85o C (-40o TO 185o F)
Relative Humidity	0 to 90% without condensation	
Maximum Altitude	3,050 meters (10,000 feet)	15,250 meters (50,000 feet)

1.2.4 Physical Dimensions

Length	12.00 inches	(30.48 cm)
Width	6.75 inches	(17.15 cm)
Depth	0.50 inches	(1.27 cm)

1.2.5 Access/Cycle Time

Access time:	350 ns, typical
Cycle time:	550 ns, typical
Refresh cycle:	550 ns

1.2.6 Pin Assignments

Table 1-3 lists pin numbers, mnemonics, and signal descriptions for the P1 connector of the MSC 4808 board. These pin assignments are compatible with the IEEE 796 Multibus standard.

1.3 Bank-in-Use Indication LEDs

The MSC 4808 board contains two LEDs which indicate the current RAM bank in use. CR3 and CR4 provide a binary readout of the bank in use (0-3). Interpretation of these LEDs is shown in Table 1-2. When a parity error occurs, the bank of the error is latched, so the LEDs will continue to display the bank in error.

CR4	CR3	Bank in Use
OFF	OFF	0
OFF	ON	1
ON	OFF	2
ON	ON	3

Table 1-2
LED Bank-in-Use Readout

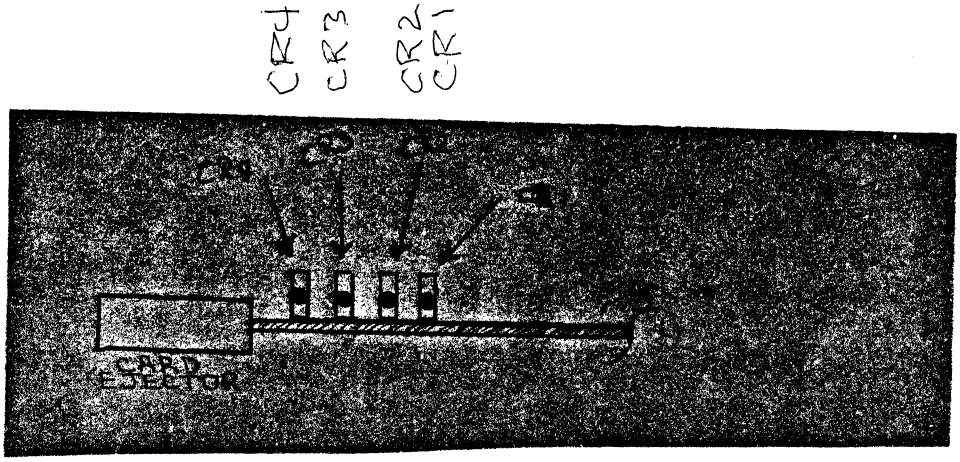

Figure 1-1
LED Locations

1.4 Error Indication LEDs

The MSC 4808 board contains two LEDs (CR1 and CR2) which light to indicate that an error has occurred. When the board is positioned in a horizontal Multibus chassis, these LEDs are at the front of the board near the left-hand side.

	COMPONENT SIDE			CIRCUIT SIDE		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
	1	GND	Signal Ground	2	GND	Signal Ground
	3	+5V	+5 volts DC	4	+5V	+5 volts DC
POWER	5	+5V	+5 volts DC	6	+5V	+5 volts DC
SUPPLIES	7	+12V	+12 volts DC	8	+12V	+12 volts DC
	9		Reserved	10		Reserved
	11	GND	Signal Ground	12	GND	Signal Ground
	13	N/A		14	INIT/	Initialize
	15	N/A		16	N/A	
	17	N/A		18	N/A	
	19	MRDC/	Memory Read Cmd	20	MWTC/	Memory Write Cmd
	21	IORC/	I/O Read Command	22	IOWC/	I/O Write Command
	23	XACK/	Transfer Acknowledge	24	INH1/	Inhibit 1 (Disable RAM)
BUS	25	N/A		26	N/A	
CONTROLS	27	BHEN/	Byte High Enable	28	AD10/	
	29	N/A		30	AD11/	Address
	31	N/A		32	AD12/	Bus
	33	N/A		34	AD13/	
	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
ADDRESS	49	ADR8/	Address	50	ADR9/	Address
	51	ADR6/	Bus	52	ADR7/	Bus
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
DATA	65	DAT8/	Data	66	DAT9/	Data
	67	DAT6/	Bus	68	DAT7/	Bus
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
	75	GND	Signal Ground	76	GND	Signal Ground
	77	Resv'd		78	Resv'd	
POWER	79	-12V	-12 volts DC	80	-12V	-12 volts DC
SUPPLIES	81	+5V	+5 volts DC	82	+5V	+5 volts DC
	83	+5V	+5 Volts DC	84	+5V	+5 volts DC
	85	GND	Signal Ground	86	GND	Signal Ground

Note: The slash ("/") following a mnemonic indicates that the signal is active low.

Table 1-3
Multibus Pin Assignments

COMPONENT SIDE			CIRCUIT SIDE		
PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
3	5VB	+5V Battery	4	5VB	+5V battery
9	ONBRD	On-board parity	10	ONBDREF	On-board refresh
			20	MPRO/	Memory protect
27	PAR1/	Parity 1 (low byte)			
28	PAR2/	Parity 2(high byte)			
			40	OFBDREF	Off-board refresh
55	AD16/	Address Bus	56	AD17/	Address bus
57	AD14/	Address Bus	58	AD15/	Address bus

Note: Not all versions of the Multibus P2 connector use all of these pins for these functions. The user should check his chassis pin assignments to see whether or not these signals are usable in a given application. Since all of these signals are jumper-selectable, they may be eliminated if not needed.

Table 1-4
Multibus P2 Connector Pin Assignments as used in MSC 4808

Chapter 2

Installation

2.1 Unpacking and Inspection

Remove all packing material and visually inspect the board for any apparent damage. Any damage which occurred during shipping should be reported immediately to both the carrier and Monolithic Systems Corporation. Damaged or missing items should be reported to the Monolithic Systems Corporation Customer Service Department, 1-303-770-7400.

2.2 Preparation

Before inserting the board in the Multibus chassis, certain user-selectable jumpers must be installed.

2.2.1 Memory Address Jumpers

Three sets of jumpers must be configured in order to set the memory address range of the MSC 4808: (1) the 4 megabyte bank select, (2) the lowest address which the board will respond to, and (3) the highest address that the board will respond to.

The entire address range of the board must fit within one 4-megabyte segment of memory set by jumpers E51-52 and E53-54.

The lowest address recognized by the board must be set by jumpers as listed in Tables 2-2 through 2-5.

The highest address recognized by the board must be set by jumpers as listed in Tables 2-6 through 2-9. The difference between the lowest address and the highest address recognized by the board should be exactly the memory capacity of the board.

For example, if a 512 Kb board is to reside in the lowest 4-megabyte bank and is to start at 16 Kb (4000H), the ending address will be 528 Kb (84000H),

and it will be configured as follows:

- The 4-megabyte bank-select must choose the first bank, so E51-52 and E53-54 must both be removed.

- The 1-megabyte select jumpers for the starting address must be set for zero, since 4000H is in the first megabyte of memory space. (Jumpers E31-32 and E29-30 are installed.)

- The 64-kilobyte select jumpers for the starting address must be set for zero, since 16 Kb is in the first 64 Kb of memory. (All jumpers E21-22, E23-24, E25-26, E27-28 are installed.)

- The 4-kilobyte select jumpers for the starting address must be set for 16 Kb. Jumpers E19-20 and E9-10 are installed.

- The 1-kilobyte select jumpers for the starting address must be set for zero, since 16 Kb is on an even 4 Kb boundary. Jumpers E13-14 and E15-16 are installed.

- The 1-megabyte select jumpers for the ending address must be set for zero, since 84000H is in the first megabyte of memory space. Jumpers E45-46 and E47-48 are installed.

- The 64-kilobyte select jumpers for the ending address must be set for 512 Kb (80000H). Jumpers E37-38, E39-40, and E41-42 are installed.

- The 4-kilobyte select jumpers for the ending address must be set for 16 Kb. Jumpers E1-2, E3-4, and E35-36 are installed.

- The 1-kilobyte select jumpers for the ending address must be set for zero, since 528 Kb is on an even 4 Kb boundary. Jumpers E5-6 and E7-8 are installed.

4 Megabyte Bank Select Jumpers

	AD17 E53-54	AD16 E51-52
0-3 Mb (0H - 3FFFFFH)		
4-7 Mb (400000-7FFFFF)		X
8-11 Mb (800000-BFFFFF)	X	
12-15 Mb (C00000-FFFFFF)	X	X

Note: X = jumper installed

Table 2-1
4 Megabyte Bank Select Jumpers

Lowest Address Select Jumpers
1 Megabyte Select

	AD15 E31-32	AD14 E29-30
0 Mb (000000H-0FFFFFH)	X	X
1 Mb (100000H-1FFFFFH)	X	
2 Mb (200000H-2FFFFFH)		X
3 Mb (300000H-3FFFFFH)		

Table 2-2
Lowest Address Select Jumpers
1 Megabyte Select

Lowest Address Select Jumpers 64 Kb Select (within megabyte)	E27-28 AD13	E25-26 AD12	E23-24 AD11	E21-22 AD10
0 Kb (00000H-0FFFFH	X	X	X	X
64 Kb (10000H-1FFFFH)	X	X	X	
128 Kb (20000H-2FFFFH)	X	X		X
192 Kb (30000H-3FFFFH)	X	X		
256 Kb (40000H-4FFFFH)	X		X	X
320 Kb (50000H-5FFFFH)	X		X	
384 Kb (60000H-6FFFFH)	X			X
448 Kb (70000H-7FFFFH)	X			
512 Kb (80000H-8FFFFH)		X	X	X
576 Kb (90000H-9FFFFH)		X	X	
640 Kb (A0000H-AFFFFH)		X		X
704 Kb (B0000H-BFFFFH)		X		
768 Kb (C0000H-CFFFFH)			X	X
832 Kb (D0000H-DFFFFH)			X	
896 Kb (E0000H-EFFFFH)				X
960 Kb (F0000H-FFFFFH)				

Table 2-3
Lowest Address Select Jumpers
64 Kb Select (within megabyte)

Lowest Address Select Jumpers 4 Kb Select (within selected 64 Kb)	AD0F E19-20	AD0E E17-18	AD0D E9-10	AD0C E11-12
0 Kb (0000H-0FFFH)	X	X	X	X
4 Kb (1000H-1FFFH)	X	X	X	
8 Kb (2000H-2FFFH)	X	X		X
12 Kb (3000H-3FFFH)	X	X		
16 Kb (4000H-4FFFH)	X		X	X
20 Kb (5000H-5FFFH)	X		X	
24 Kb (6000H-6FFFH)	X			X
28 Kb (7000H-7FFFH)	X			
32 Kb (8000H-8FFFH)		X	X	X
36 Kb (9000H-9FFFH)		X	X	
40 Kb (A000H-AFFFH)		X		X
44 Kb (B000H-BFFFH)		X		
48 Kb (C000H-CFFFH)			X	X
52 Kb (D000H-DFFFH)			X	
56 Kb (E000H-EFFFH)				X
60 Kb (F000H-FFFFH)				

Table 2-4
Lowest Address Select Jumpers
4 Kb Select (within selected 64 Kb)

Lowest Address Select Jumpers
1 Kb Select (within selected 4 Kb)

	AD0B E13-14	AD0A E15-16
0 Kb (000H)	X	X
1 Kb (400H)	X	
2 Kb (800H)		X
3 Kb (C00H)		

Table 2-5
Lowest Address Select Jumpers
1 Kb Select (within selected 4 Kb)

Highest Address Select Jumpers
1 Megabyte Select

	AD15 E47-48	AD14 E45-46
0 Mb (000000H-0FFFFFH)	X	X
1 Mb (100000H-1FFFFFH)	X	
2 Mb (200000H-2FFFFFH)		X
3 Mb (300000H-3FFFFFH)		

Table 2-6
Highest Address Select Jumpers
1 Megabyte Select

Highest Address Select Jumpers 64 Kb Select (within megabyte)	AD13 E43-44	AD12 E41-42	AD11 E39-40	AD10 E37-38
0 Kb (00000H-0FFFFH)	X	X	X	X
64 Kb (10000H-1FFFFH)	X	X	X	
128 Kb (20000H-2FFFFH)	X	X		X
192 Kb (30000H-3FFFFH)	X	X		
256 Kb (40000H-4FFFFH)	X		X	X
320 Kb (50000H-5FFFFH)	X		X	
384 Kb (60000H-6FFFFH)	X			X
448 Kb (70000H-7FFFFH)	X			
512 Kb (80000H-8FFFFH)		X	X	X
576 Kb (90000H-9FFFFH)		X	X	
640 Kb (A0000H-AFFFFH)		X		X
704 Kb (B0000H-BFFFFH)		X		
768 Kb (C0000H-CFFFFH)			X	X
832 Kb (D0000H-DFFFFH)			X	
896 Kb (E0000H-EFFFFH)				X
960 Kb (F0000H-FFFFFH)				

Table 2-7
Highest Address Select Jumpers
64 Kb Select (within megabyte)

Highest Address Select Jumpers 4 Kb Select (within selected 64 Kb)	AD0F E35-36	AD0E E33-34	AD0D E1-2	AD0C E3-4
0 Kb (0000H-0FFFH)	X	X	X	X
4 Kb (1000H-1FFFH)	X	X	X	
8 Kb (2000H-2FFFH)	X	X		X
12 Kb (3000H-3FFFH)	X	X		
16 Kb (4000H-4FFFH)	X		X	X
20 Kb (5000H-5FFFH)	X		X	
24 Kb (6000H-6FFFH)	X			X
28 Kb (7000H-7FFFH)	X			
32 Kb (8000H-8FFFH)		X	X	X
36 Kb (9000H-9FFFH)		X	X	
40 Kb (A000H-AFFFH)		X		X
44 Kb (B000H-BFFFH)		X		
48 Kb (C000H-CFFFH)			X	X
52 Kb (D000H-DFFFH)			X	
56 Kb (E000H-EFFFH)				X
60 Kb (F000H-FFFFH)				

Table 2-8
Highest Address Select Jumpers
4 Kb Select (within selected 64 Kb)

Highest Address Select Jumpers
1 Kb Select (within selected 4 Kb)

	AD0B E5-6	AD0A E7-8
0 Kb (000H)	X	X
1 Kb (400H)	X	
2 Kb (800H)		X
3 Kb (C00H)		

Table 2-9
Highest Address Select Jumpers
1 Kb Select (within selected 4 Kb)

2.2.2 I/O Address Selection Jumpers

Two selections must be made concerning the I/O address for the parity flag register: (1) how many I/O address bits are valid with the processor in use, and (2) the actual I/O address. Jumpers listed in Table 2-10 determine how many address bits are decoded by the I/O address recognition circuitry, and jumpers listed in Table 2-11 determine the address of the register.

I/O Address Space	Install Jumpers	Possible addresses
8 bit	E86-87, E83-84, E80-81 E77-78, E74-75, E71-72 E68-69, E65-66	00H-0FH, 40H-4FH
12 bit	E87-88, E85-84, E82-81, E78-79, E74-75, E71-72, E68-69, E65-66	000H-00FH, 040H-04FH
16 bit	E87-88, E84-85, E81-82 E78-79, E75-76, E72-73 E69-70, E66-67	0000H-000FH, 0040H-004FH

Table 2-10
I/O Address Size Jumpers

Address	AD06 E63-64	AD03 E61-62	AD02 E59-60	AD01 E57-58	AD00 E55-56
00H	X	X	X	X	X
01H	X	X	X	X	
02H	X	X	X		X
03H	X	X	X		
04H	X	X		X	X
05H	X	X		X	
06H	X	X			X
07H	X	X			
08H	X		X	X	X
09H	X		X	X	
0AH	X		X		X
0BH	X		X		
0CH	X			X	X
0DH	X			X	
0EH	X				X
0FH	X				
40H		X	X	X	X
41H		X	X	X	
42H		X	X		X
43H		X	X		
44H		X		X	X
45H		X		X	
46H		X			X
47H		X			
48H			X	X	X
49H			X	X	
4AH			X		X
4BH			X		
4CH				X	X
4DH				X	
4EH					X
4FH					

Table 2-11
Parity Flag Register I/O Address Selection Jumpers

2.2.3 Interrupt Line Select Jumpers (E123-E138)

With one of the jumper pairs of E123-138 connected, a parity error will cause an interrupt, and data related to the error becomes available to the user.

Jumper pins E123 through E138 may be utilized to assert an interrupt signal on one of the eight Multibus interrupt request lines (INT0-INT7) whenever an error occurs. Remember that according to the IEEE Multibus specifications, INT0 has the highest priority and INT7 has the lowest

priority.

Table 2-12 shows how the jumpers must be connected to assert a signal on the desired interrupt line when a parity error occurs.

INTERRUPT REQUEST LINE	JUMPERS
INT0	E137-138
INT1	E135-136
INT2	E133-134
INT3	E131-132
INT4	E129-130
INT5	E127-128
INT6	E125-126
INT7	E123-124

Table 2-12
Multibus Interrupt Jumper Selection

2.2.4 Power Jumpers

If the user's backplane supports P2 connections for battery backup, the MSC 4808 board must also be configured for normal or battery backup operation as shown in Table 2-13.

Mode	Jumpers
Battery Backup	E154-156, E159-157
Normal	E156-158, E157-E155

Table 2-13
Power Jumper Configurations

2.2.5 Half Full/Full Jumpers

If the board is configured with 512 Kb of RAM, E152-153 should be installed. If only 256 Kb of RAM is installed, E151-153 should be installed.

2.2.6 Off-Board Parity Circuitry

If the user's backplane supports P2 connections for the use of off-board parity circuitry and off-board parity circuitry is to be used, E113-114 should be installed to enable this function. Installation of E117-118 will place PAR1/ on the bus (P2 connector) and installation of E119-120 will place PAR2/ on the bus.

2.2.7 On-Board/Off-Board Refresh Generation Jumpers

Jumpers E114-115-116 and E121-122 determine whether on-board or off-board refresh is to be used. For off-board refresh, E121-~~122~~ 124 must be installed. If off-board refresh is required only when ONBDREF (P2 pin 10) if false, E114-115 should be installed. If off-board refresh is always to be required, E114-116 should be installed. For normal on-board refresh under all circumstances, none of these jumpers should be installed.

	E114-115	E114-116	E121-~~122~~ 124
Off-board Refresh Required over OFBDREF		X	X
Off-board Refresh Required when ONBDREF is false	X		X
Refresh generated On-board			(no jumpers required)

X = Installed

Table 2-14
On-board/Off-board Refresh Generation Jumpers

2.2.8 Other Jumpers

All other jumpers have been factory set to conform with the memory size and configuration of the board and should NOT be altered.

2.3 Insertion

The MSC 4808 is now ready to be inserted into the Multibus chassis. Disconnect power to the chassis and remove the appropriate cover(s) to gain access. Firmly push the board into the desired slot until it is properly seated in the backplane. Replace the cover(s) and restore power to the chassis.

Chapter 3

Operation

3.1 Timing and Control

The Multibus processor, acting as master, generates all access requests and addresses. The MSC 4808 memory board generates the appropriate responses and internal timing.

3.2 Initialization

During power-up, the INIT/ signal goes "low", inhibiting all Multibus commands while the memory array is initialized to a known internal state. The parity error report register should be cleared with an I/O write to its jumper-selected address on powerup.

3.3 Addressing

RAM selection is controlled by using the fourteen most significant Multibus address lines (ADRA - AD17). Address selection is in 1K groups. Bank selection information is also provided for the memory array and for the parity error reporting section.

3.4 Data Transfers

The MSC 4808 can transfer either 8-bit or 16-bit data words. There are three types of data transfers:

1. Transfer of even "low-order" bytes.

2. Transfer of odd "high-order" bytes.

3. Transfer of a 16-bit word.

These three types of transfers are controlled by Multibus lines BHEN/ and ADR0/.

In the first type of transfer, BHEN/ and ADR0/ are both "inactive", indicating the transfer of even (low-order) eight-bit bytes. This transfer takes place across data lines DAT0/ through DAT7/.

The second type of transfer takes place when BHEN/ is "inactive" and ADR0/ is "active", indicating the transfer of an odd (high-order) byte. The odd byte is transferred through the Swap Byte Buffer to DAT0/ through DAT7/.

The third type of transfer takes place when both BHEN/ and ADR0/ are "active". This is a 16-bit (two-byte) transfer. The even (low-order) byte is transferred on DAT0/ through DAT7/; and the odd (high-order) byte is transferred on DAT8/ through DATF/.

3.5 Memory Write

During the write operation (MWTC/), the Multibus data is presented to the memory and parity array. If the cycle is a byte write, the data from the Multibus will be transferred to the correct byte prior to being written into memory. The memory indicates acceptance of the data by returning a Transfer Acknowledge (XACK/) signal, allowing the bus master to remove the address, command and data from the Multibus interface.

3.6 Memory Read

Data is transferred to the Multibus data lines and a Transfer Acknowledge (XACK/) is returned, indicating that data is now on the bus. When the bus master receives the acknowledge, it strobes in the data and removes the command (MRDC/) from the Multibus.

3.7 Error Annunciation and Logging

There are three ways to detect the occurrence of a parity error:

1. Visual examination of the LED indicators.
2. Generation of a Multibus interrupt by jumper option.
3. Polling of the parity error register.

When a parity error occurs, the error information (high or low byte parity and bank in error) is latched into the error register and the LED display. It will remain there until (a) the board is reinitialized or (b) the parity reporting register is written. In the normal configuration, the error will cause a bus interrupt. The Multibus processor will respond to the interrupt and in the process will write the parity reporting register in order to clear it.

3.7.1 Reporting LEDs

The reporting LEDs are to be interpreted as follows:

CR1:	Low byte parity error
CR2:	High byte parity error
CR3:	Least significant bit of bank number
CR4:	Most significant bit of bank number

Thus, if either CR1 or CR2 is lit, an error has occurred. CR3 and CR4 indicate the location of the error in binary form. Thus if neither of these two are lit, the error has occurred in bank 0. If both are lit, the error has occurred in bank 3, etc. See Table 1-2 for complete information. Note that CR3 and CR4 are continuously monitoring the bank in use until a parity error occurs, at which time the bank of the error is latched.

3.7.2 Parity Reporting Register

The parity reporting register is located at an I/O address which may be jumper-selected as described in Chapter 2. It includes all of the information found in the LED display, but the form is somewhat different.

A write to this address will clear the register. This should be done on powerup and after a parity error has been handled.

The register can be read by a simple read to the jumper-selectable I/O address. See Figure 3-1 for the format.

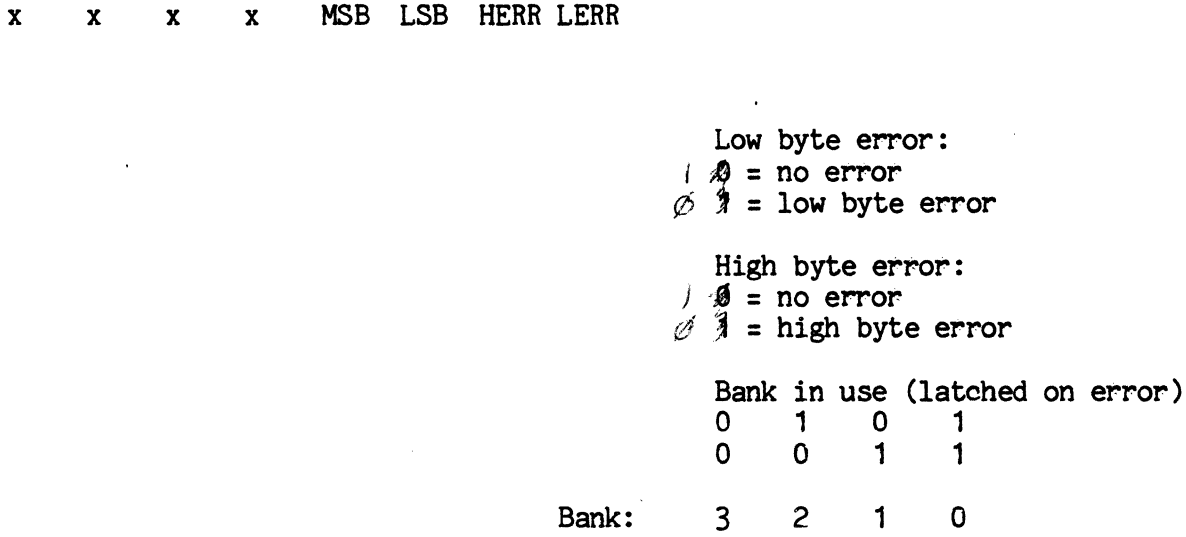

Figure 3-1
Parity Error Reporting Register

Chapter 4

Preventive Maintenance and Troubleshooting

4.1 Preventive Maintenance

The MSC 4808 requires a minimum of maintenance. However, the board should be inspected and cleaned periodically, and it is important to avoid voltage fluctuations.

4.1.1 Visual Inspection

The board should be inspected for loose wiring, loose or broken components, and discoloration of parts. The inspection should be preformed with a minimum of prying or moving of wiring and components.

4.1.2 Cleaning

Cleaning should be limited to removal of excess dust or dirt particles. NEVER use abrasives on the gold fingers of the edge connectors. Low pressure compressed air can be used for removing dust or dirt, and an aerosol cleaner--with light brushing--can be used to clean the gold contacts.

4.1.3 Voltage Margins

All DC voltages should be maintained within 5% of the stated values.

4.2 Troubleshooting

If a diagnostic or other test indicates that the memory board is defective, check all voltages before making any replacements.

If a bit error is detected, the defective element may be located using the memory array layout shown in Figure xxxxx.

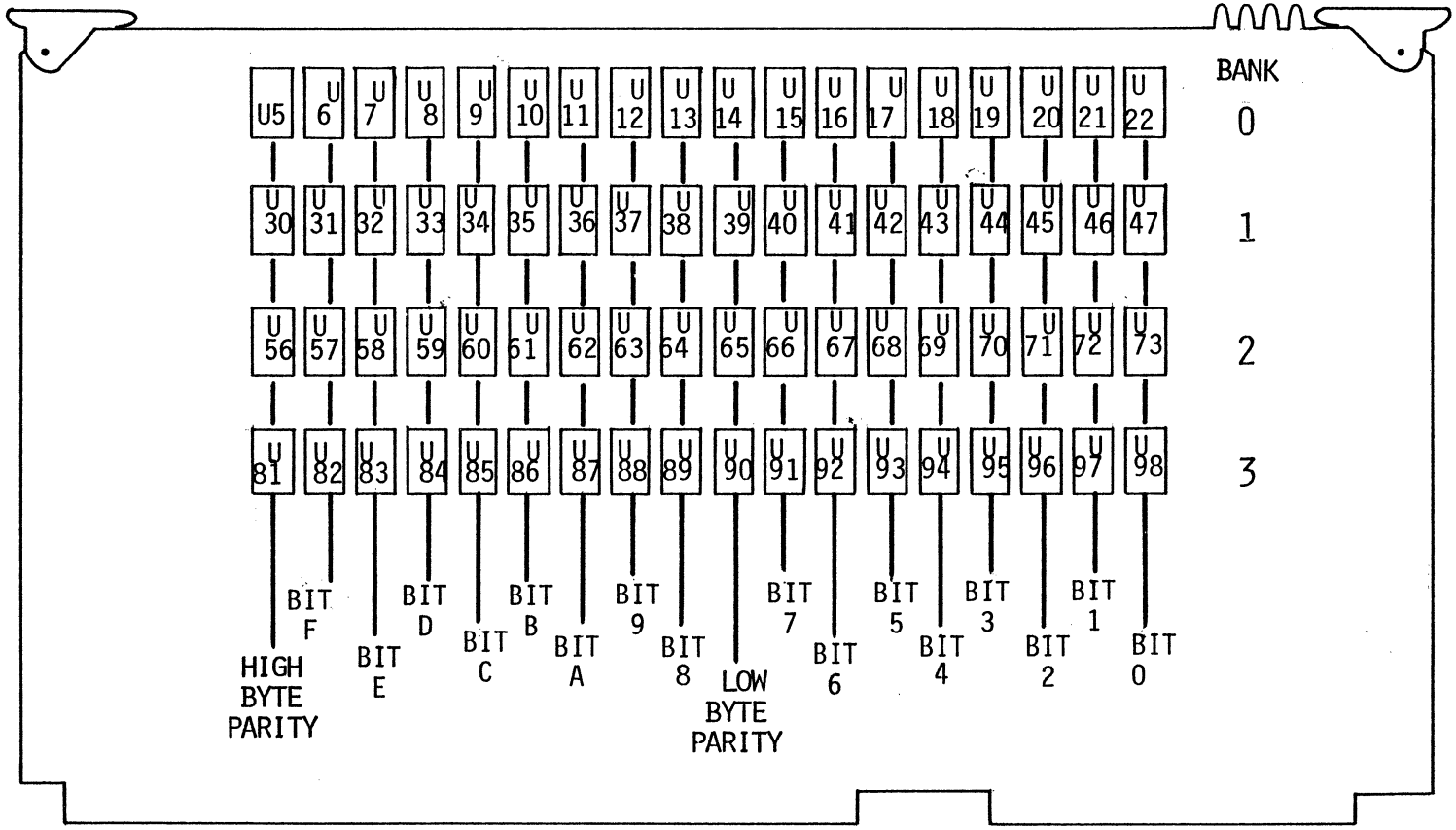
BANK
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
0
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
1
U56
U57
U58
U59
U60
U61
U62
U63
U64
U65
U66
U67
U68
U69
U70
U71
U72
U73
2
U81
U82
U83
U84
U85
U86
U87
U88
U89
U90
U91
U92
U93
U94
U95
U96
U97
U98
3
HIGH BYTE PARITY
BIT F
BIT E
BIT D
BIT C
BIT B
BIT A
BIT 9
BIT 8
LOW BYTE PARITY
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0

Figure 4-1
MSC 4808 Memory Array

Chapter 5

WARRANTY

5.1 General

Monolithic Systems Corporation (MSC) warrants for a period of one (1) year from the date of shipment that each item of equipment manufactured by MSC shall be free from defects in material and workmanship under normal use and service.

In the event of a failure of a product covered by this warranty, MSC will repair such product without charge provided the warrantor's examination concludes to its satisfaction that the product was defective. The warrantor may at its option, replace the product in lieu of repair. If the failure has been caused by misuse, neglect, accident, user modification, or abnormal conditions of operations, the warranty shall become void and product subject to normal repair charges. In such cases, an estimate will be submitted before repair is performed.

All replaced products and/or components shall become MSC property.

The foregoing warranty is in lieu of all other warranties, promises, affirmations, or representations, whatsoever, expressed or implied, including, but not limited to, any implied warranty of merchantability or implied warranty of fitness of equipment for a particular purpose, and of any other obligations on the part of the seller.

5.2 Warranty Registration

To implement the warranty, please complete the WARRANTY REGISTRATION card located at the front of this manual and return it to Monolithic Systems Corporation.

5.3 Warranty Service

To obtain warranty service, the buyer must:

1. Contact MSC and provide Customer Service with part number, serial number, and nature of defect. Customer Service will issue a Warranty Return Authorization number.

2. Pack product in original container, if available, or in a rigid container of adequate size. Product should be wrapped to protect it from static discharge and packed in a shock absorbing material. Include Warranty Return Authorization number on outside of shipping container.

3. Ship product prepaid to MSC Customer Service, 84 Inverness Circle East, Englewood, Colorado 80112.

4. MSC will return the product prepaid via U.P.S. Request for any other transportation will be subject to customer expense.

A D D E N D U M
To MSC 4808 User's Manual

CORRECTION OF ENDING ADDRESS JUMPER CONFIGURATION

When setting the ending address on the MSC 4808 memory board, remember that the actual ending address is one byte less than the value commonly referenced, and that the ending address should be set to the range listed as one kilobyte less in the tables. In other words, the ending address jumpers should be set for the last K byte actually used.

For example, if the board is configured for the full 512K byte capacity and is to be addressed from 128K bytes (20000 Hex) to 640K bytes (A0000 Hex), the actual ending address is one byte less than 640K bytes or 655,359 bytes (9FFFF Hex). Accordingly, the jumpers should be set for the 639K byte range. Use Tables 2-6 through 2-9 in the preliminary MSC 4808 User's Manual (dated 7/26/83) to select the appropriate jumpers.

For this example, to set the ending address install jumpers E47-48, E45-46, E41-42 and E39-40.

If additional assistance is required, call the MSC Customer Service Department at (303) 770-7400.