MITS 3200 USER'S MANUAL

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CHANGE RECORD

Revision	Date	Pages
A	4/78	Initial Release

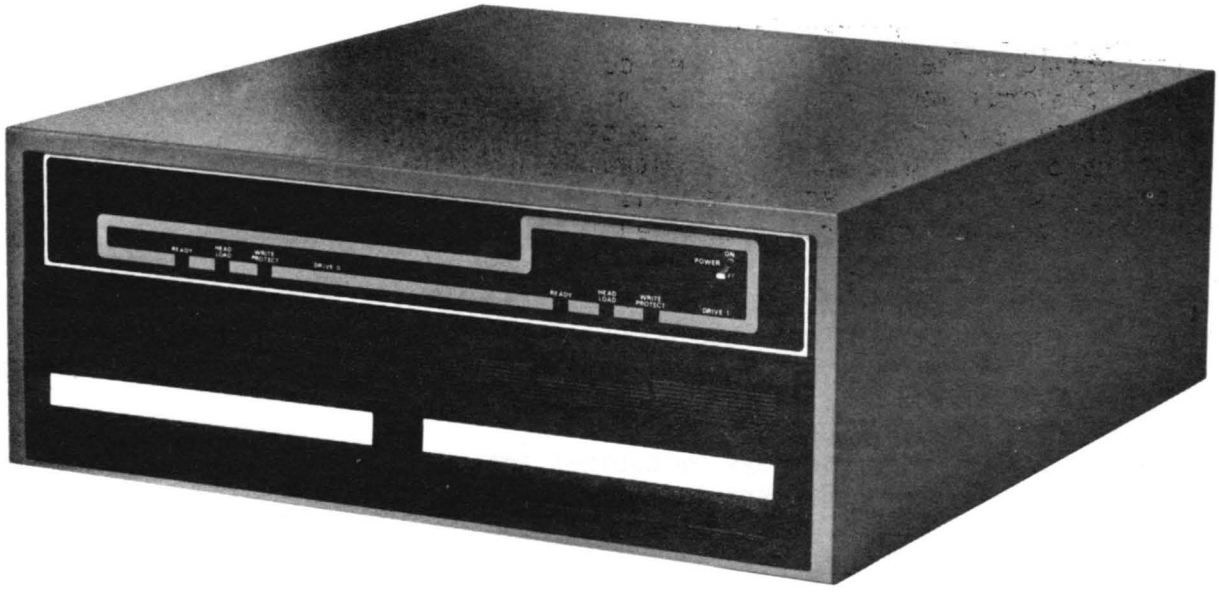
1 DESCRIPTION

1-1 GENERAL DESCRIPTION

The MITS 3200 Floppy Disk System is a complete single or dual floppy-disk memory system that can be used with any S-100 bus computer.

The MITS 3200 Floppy Disk System has a capacity of 310K bytes per disk (620K bytes total for a dual disk system). The Floppy Disk System consists of two Disk Controller printed circuit boards that connect to the S-100 bus, and a Disk Drive unit, containing one or two PERTEC FD-510 Disk Drives, a Power Supply and one or two Buffer/Address/Line Driver PC boards. The Disk Drive has two 20 pair flat cables on the back panel. One is the input from the Disk Controller, and the other is the output to additional Disk Drives. Up to 16 drives (8 dual disk drive cabinets) may be attached to one Controller.

The Disk Controller transfers data to and from the Disk serially at 250K bits/second. The Disk Controller converts the serial data to and from 8-bit parallel words (one word every 32 microseconds). The computer transfers the data, word by word, to or from the disk, depending on whether the disk is reading or writing. The Disk Controller also controls all mechanical functions of the Disk Drives as well as presenting disk status to the computer. All timing functions are hard wired to free the computer for other tasks.



Floppy Disk System, MITS 3202

1 DESCRIPTION

1-2 OVERALL SYSTEM DESCRIPTION

The MITS Floppy Disk System is a functional part of a complete computer system.

The Floppy Disk System is used for mass data storage for the S-100 bus computers, and has a capacity of 310K bytes per diskette with an average access time of 400 milliseconds. A typical system using a MITS/Altair computer consists of a MITS/Altair 8800b mainframe with an 8080A CPU, 32K of memory, an I/O card for communicating to a terminal, a PROM card for initializing the system, a set of Disk Controller cards and two Disk Drives.

The software most commonly used is Disk BASIC which resides in the lower 24K of memory and provides the Disk utilization routines. Disk BASIC includes the standard features of BASIC, plus many extra functions that significantly increase programming power. The Software Driver for the Disk Read/Write functions uses hard sectoring, allowing maximum data storage on the Diskette.

The computer interacts with the Disk Drives through two Disk Controller boards that connect to the S-100 bus. All Control, Status and Data I/O is handled through three I/O ports dedicated to Disk Control. The ciruitry in the Disk Controller consists of LSI and MSI TTL logic and performs the necessary housekeeping functions for data transfers and control of Disk Drive operations.

Inside the Floppy Disk System cabinet are one or two PERTEC FD-510 Drives, a Power Supply, Line Buffers and Addressing Circuitry.

1 DESCRIPTION

1-3 CONFIGURATIONS AVAILABLE

The MITS 3200 Series Floppy Disk System is available in several configurations to satisfy differing requirements.

Three basic configurations, each with several options are available for the Floppy Disk System.

The Model 3201 has a single disk drive in a desk cabinet; the 3201R has a single disk drive in a rack mount.

The Model 3202 has dual disk drives in a desk cabinet; the 3202R has dual disk drives in a rack mount.

Both the 3201/3201R and the 3202/3202R include two Disk Controller Boards (Disk Board No. 1 and Disk Board No. 2) which plug into the S-100 Bus computer motherboard; an interconnect cable between the Disk Boards; a cable between the Disk Boards and the back panel of the computer; an I/O cable between the computer and the disk drive unit; and a Disk Drive (single or dual) unit, with a Disk Buffer Board for each drive.

The Model 3203 is an expansion unit which consists of two disk drives and Disk Buffer Boards, plus a cable to connect to a Model 3202, giving a total of four disk drives. It is available in rack-mount style as the Model 3203R.

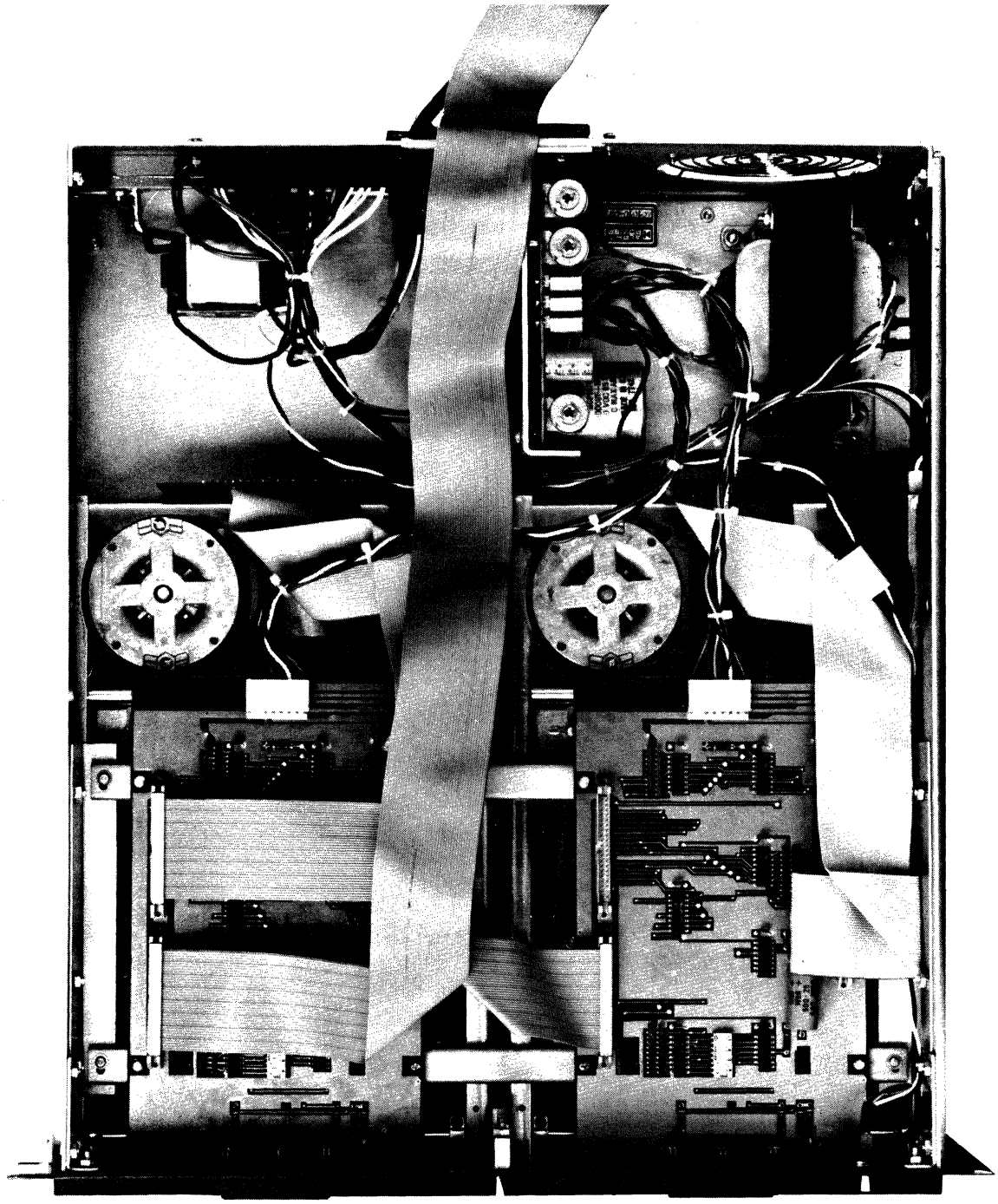
All models can be ordered for either 115 volt, 60 Hz or 220 volt, 50 Hz operation.

1-4 HARDWARE FEATURES

This section describes the hardware comprising the Floppy Disk System.

The Disk Controller, which acts as the interface between the computer and the Disk Drives, consists of two printed circuit boards. They contain over 60 ICs, and connect to the Disk Drive Unit via a 20-pair flat cable. The Controller can address up to 16 Drives.

The Disk Drive Unit consists of one or two PERTEC FD-510 Drives in a cabinet 7.25" (18.5 mm) high, 19.2" (48.8 mm) wide and 21.75" (55.3 mm) deep. A Power Supply and one or two Buffer/Address boards for selecting the Drive and interconnecting multiple Disk systems are also contained in the Disk unit. A fan is included to maintain low ambient temperature for continuous operation. The Disk Drive units interconnect to each other in "daisy chain" fashion using 20 pair flat cables and 3M type 40 pin plug-on connectors.



Interior View, MITS 3202

1 DESCRIPTION

1-5 HARDWARE SPECIFICATIONS

This section lists hardware specifications of the Floppy Disk System.

a) Access Time
   Track to track: 10 milliseconds
   Head load time: 40 milliseconds
   Head settling time: 20 milliseconds

b) Rotational speed: 360 RPM (166.7 milliseconds per revolution)

c) Tracks: 77 per Disk

d) Sectoring: Hard Sectored, 32 Sectors per track, 5.2 milliseconds per Sector (non-IBM compatible)

e) Data Transfer Rate: 250,000 bits/sec. (one 8-bit byte every 32 micro-seconds)

f) Maximum number of Drives per system: 16 (8 dual disk drives)

g) Data storage capacity: 310,000 bytes per Disk

h) Data bytes per sector: 128

i) Data bytes per track: 4,096

j) Disk Drive head life: over 20,000 hours of Diskette to Head contact

k) Disk Drive Mean Time Between Failure (MTBF): exceeds 4,000 hours

l) Disk Drive data reliability: not more than 1 in 10^9 soft (recoverable errors), 1 in 20^{12} hard (non recoverable errors)

m) Power

   Controller: 1.1 amps at +8v unregulated (from S-100 bus)
   Disk Drive Unit: 42 watts 50/60 Hz, 117/220 VAC per drive

n) Diskette: Hard Sectored, 32 Sectors + Index hole

o) Floppy Disk System Weight: 70 pounds

1-6 SOFTWARE FEATURES

This section describes some features of Disk BASIC and the Disk Bootstrap Loader.

Disk BASIC is an enhanced version of Extended BASIC which includes capabilities for saving and loading programs, and manipulating data files on the disk. It requires a minimum of 24K of RAM memory for operation and utilizes random and sequential files for storing information on the disk. Refer to the MITS BASIC Manual for detailed information.

Utility Software is included with Disk BASIC for copying Diskettes, initializing blank Diskettes, listing directories, etc.

A Disk Bootstrap Loader is available on paper tape, cassette tape, or PROM (used with an 88-PMC PROM Memory Card). The PROM Disk Bootstrap Loader allows loading of Disk BASIC in less than ten seconds from the time power is turned on. A Hard Sectored format allows storage of 310,000 data bytes per diskette.

2 INSTALLATION

2-1 CONNECTING CONTROLLER BOARDS

Use this procedure to connect the Disk Controller Boards.

a) Take cover off computer (power off).

b) Feed miniature (flat) connector ends of Controller cable through hole on connector panel in back of computer. (37-pin connector outside chassis, miniature connectors inside chassis.) Disregard this step if the computer chassis has mounting hole for 37-pin connector.

c) Facing the front of the computer lay Disk Controller Board #1 flat in front of you on the computer chassis with components up and stab connector to the right.

d) Connect the short wired cable of Disk Board #2 to the 20-pin connector on Disk Board #1 (note polarization key of connector and missing pin on the board).

e) Place Disk Board #2 flat, to the left of Disk Board #1 with components up and stab connector to the right.

f) Connect 20-pin miniature connector on Controller cable to 20-pin connector on Disk Board #2. Note keying.

g) Take 10-pin connector on Controller cable with the orange and yellow wires connected to it and connect to 10-pin connector on Disk Board #2. Note keying.

h) Take remaining 10-pin connector on Controller Cable with white and gray wires on it and connect to 10-pin connector on Disk Board #1. Note Keying.

i) Be sure wires from connector go out between card guides, and do not catch on card guides.

j) Push cards firmly into connector on computer motherboard.

k) Install 37-pin connector in bracket on back of computer, stradling 2 connector holes. Use #4-40 x 5/16 screws, #4 lockwashers and #4-40 nuts.

NOTE

If unit has holes for 37-pin socket, disregard installation of bracket. Mount connector using #4-40 hardware on INSIDE of back panel.

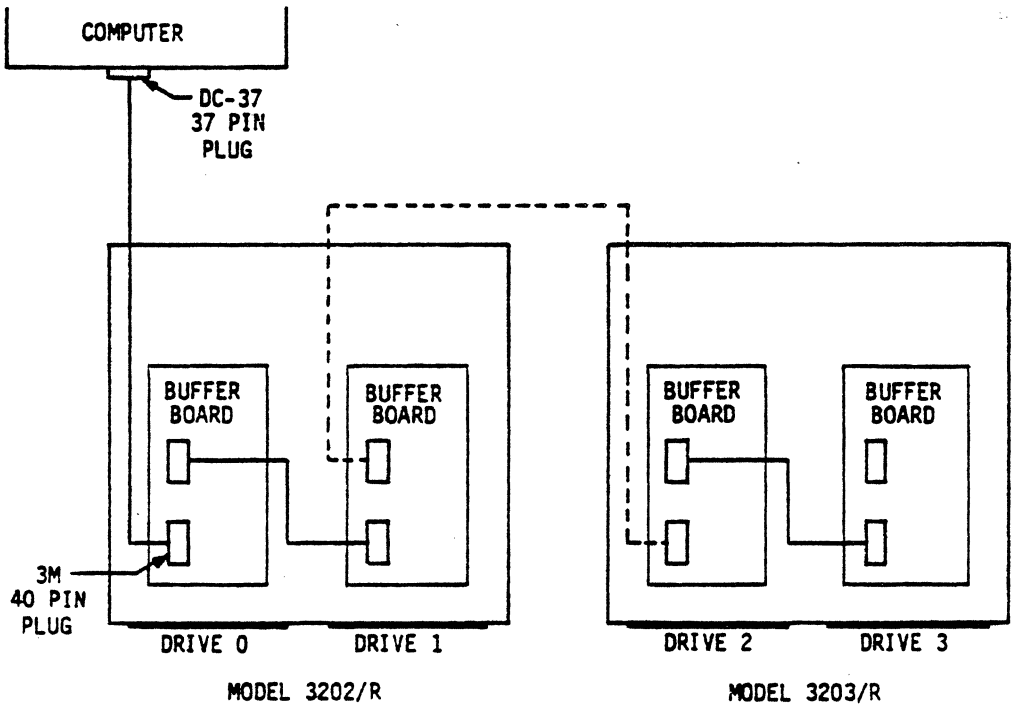
2 INSTALLATION

2-2 MULTIPLE DISK DRIVE CONNECTION

Use this procedure for interconnecting multiple disk drives.

1. With multiple disk Drives, the Disks should have sequential addresses, i.e., for a 3-Drive System you should have Disks with addresses 0, 1 and 2. They may be connected in any order. The Disk Address is determined by four switches in the Disk Buffer PC board inside the Drive and may be changed. See Section 4-22 for a chart indicating the switch positions on the Disk Buffer PC board.

2. The two drives within the dual drive cabinet are normally interconnected as shown with a short flat cable with two 3M type 40-pin plug-on connectors between the two buffer boards. To connect a second dual drive cabinet, an eleven-foot, 20 pair flat cable with two 3M type 40-pin plug on connectors is attached to the buffers as shown by the dashed line in the figure on the facing page.



Multiple Disk Drive Connection

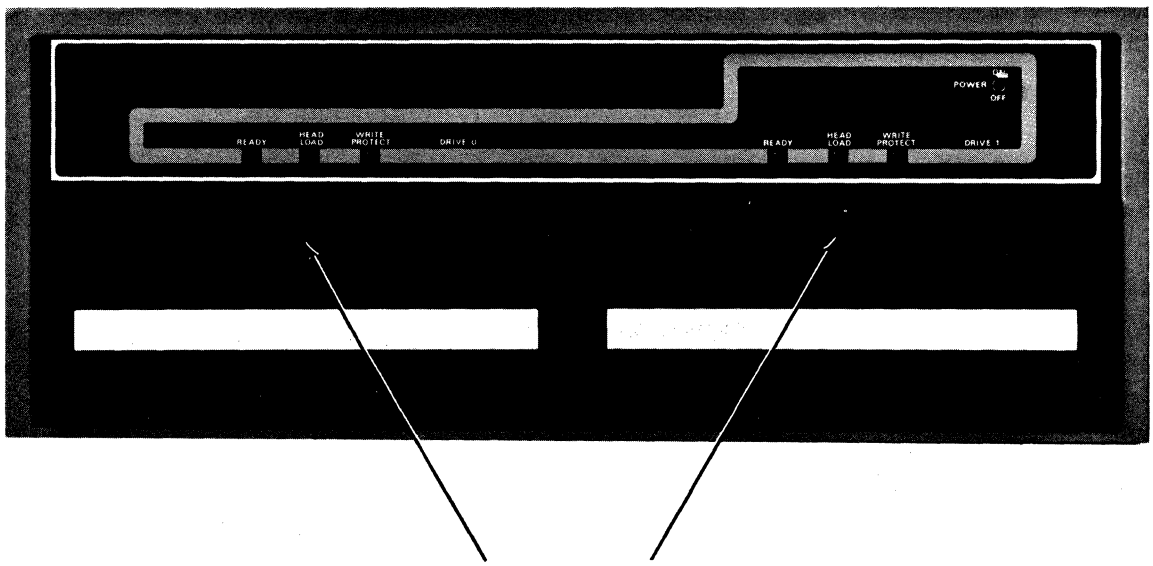
3 OPERATING INSTRUCTIONS

3-1 CONTROLS AND INDICATORS

This section describes the controls and indicators of the floppy disk system.

The controls and indicators of the floppy disk system are shown on the facing page and are described in the following table.

SWITCH/INDICATOR	FUNCTION
POWER ON/OFF Switch	Turns power on or off.
READY Indicator	Indicates that the drive is turning at the proper speed after the drive door is closed. Will remain lit if the door is opened if power stays on in the drive units.
HEAD LOAD Indicator	Indicates that the head is in contact with the diskette (read or write).
WRITE PROTECT Indicator	Indicates that the Write Protect Slot on the diskette jacket is uncovered. Data can be read from the diskette, but data cannot be written or changed.
Drive Door Indicator	Indicates that the disk drive is enabled for transfer of data (read or write), that this particular drive has been addressed for transfer of data, that the drive door is closed, and that the drive is turning at the proper speed.



Front Panel, MITS 3202

3 OPERATING INSTRUCTIONS

3-2 DISKETTE INFORMATION

Following these recommendations will eliminate most problems that could be caused by faulty diskettes.

Always keep Diskette in envelope when not in use.

Keep Diskette away from heat, magnetic fields (flourescent lights, power transformers, etc.) and dust.

Never touch recording surface of Diskette (opposite label side).

Always label the Diskette, using an adhesive label. Do not write on label after it is attached to the Diskette.

The type of Diskette used is Hard Sectored (32 Sector holes and 1 Index hole). Blank Diskettes are available from MITS Dealers.

3 OPERATING INSTRUCTIONS

3-3 OPERATING THE FLOPPY DISK SYSTEM

Use this procedure to operate the floppy disk system.

The figure on the facing page shows the items mentioned below.

1. Set the POWER ON/OFF switch to ON. Verify that the READY and WRITE PROTECT indicators are lit.

2. Open the disk drive door by lifting the tab to release the door latch. The door swings down.

3. Insert diskette into the drive with the label side up. Push in and down until the diskette catches on the diskette retainer at the bottom right of the housing.

4. Close the disk drive door by lifting the door bottom until it catches on the tab. Wait for the READY indicator to light (about 5 seconds).

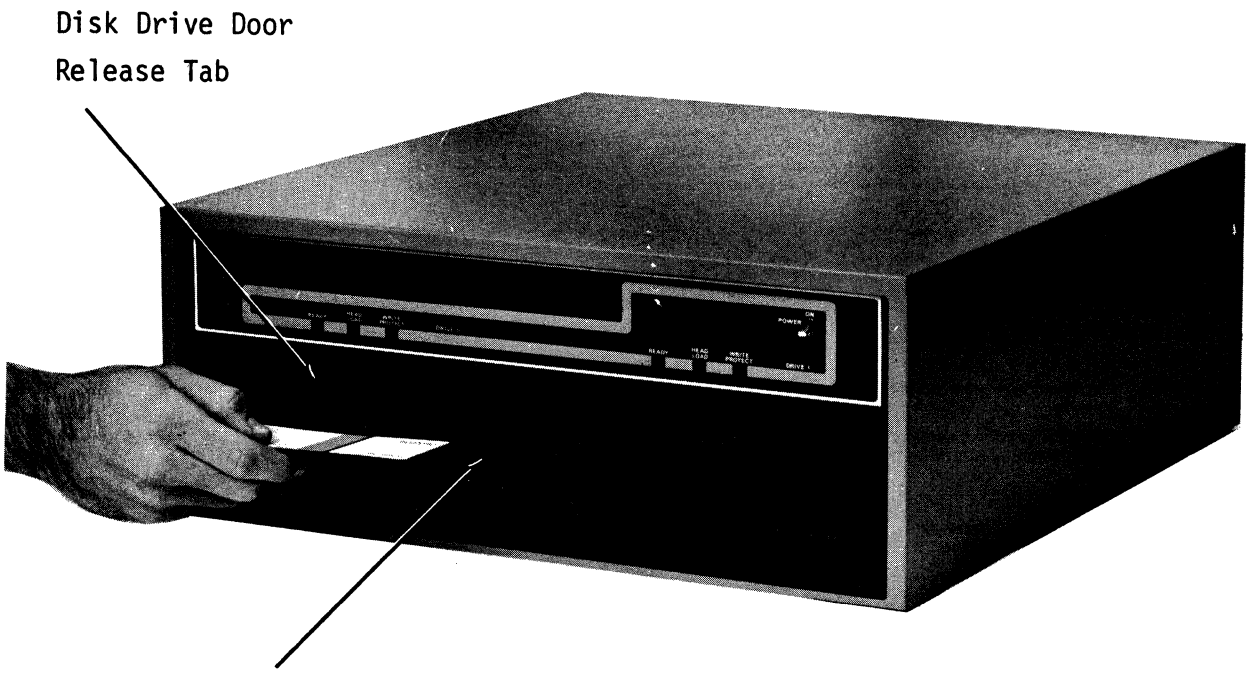
5. When the READY indicator is lit, the disk drive may be enabled and programs may be activated that access the diskette.

6. NEVER open the disk drive door or turn power off when the READY or HEAD LOAD indicators are lit. It is possible to interrupt the software during a Write function and destroy data on the Diskette.

7. Consult software documentation on methods for loading BASIC and utilizing software. For applications in which the user writes his own software, refer to Disk Controller I/O Information, Section

8. Keep the 20-pair flat interconnect cable away from power cords. If there is excess cable, fold it and secure with a rubber band.

9. It is very important that the computer and Disk Drives are connected to grounded power outlets. If you must use a grounding outlet adapter, be sure the green (ground) wire is connected to a good earth ground, such as a cold water pipe.



Inserting Diskette

4 THEORY OF OPERATION

4-1 OVERALL THEORY OF OPERATION

This section provides a brief overall description of the Disk Controller, consisting of Disk Controller Board 1, and Disk Controller Board 2.

The Disk Controller boards provide the interface between the Disk Drive Units and the S-100 bus. Serial Read Data from the Disk is converted into 8-bit parallel form by the Controller for transfer to memory via the CPU. Data is written on the Disk by converting the 8-bit bytes output from the CPU to serial form. All Read and Write Data is transferred one byte at a time through the CPU.

Disk Controller Board 1 controls I/O address selection, Sector counting, Read Data and Disk Status. Disk Controller Board 2 controls Disk Drive addressing, Write Data and Disk Drive functions.

4 THEORY OF OPERATION

4-2 FLOPPY DISK SYSTEM BLOCK DIAGRAM

This section provides a description of the block diagram provided on the facing page.

- Controller Board 1
  Controller Board 1 performs all input functions to the Altair bus (Read Data, Sector Data, Status Information) as well as Control Addressing of all Disk to Computer I/O.

- Controller Board 2
  Controller Board 2 performs all output functions from the Altair bus (Write Data, Disk Control, Disk Enable and Drive Selection).

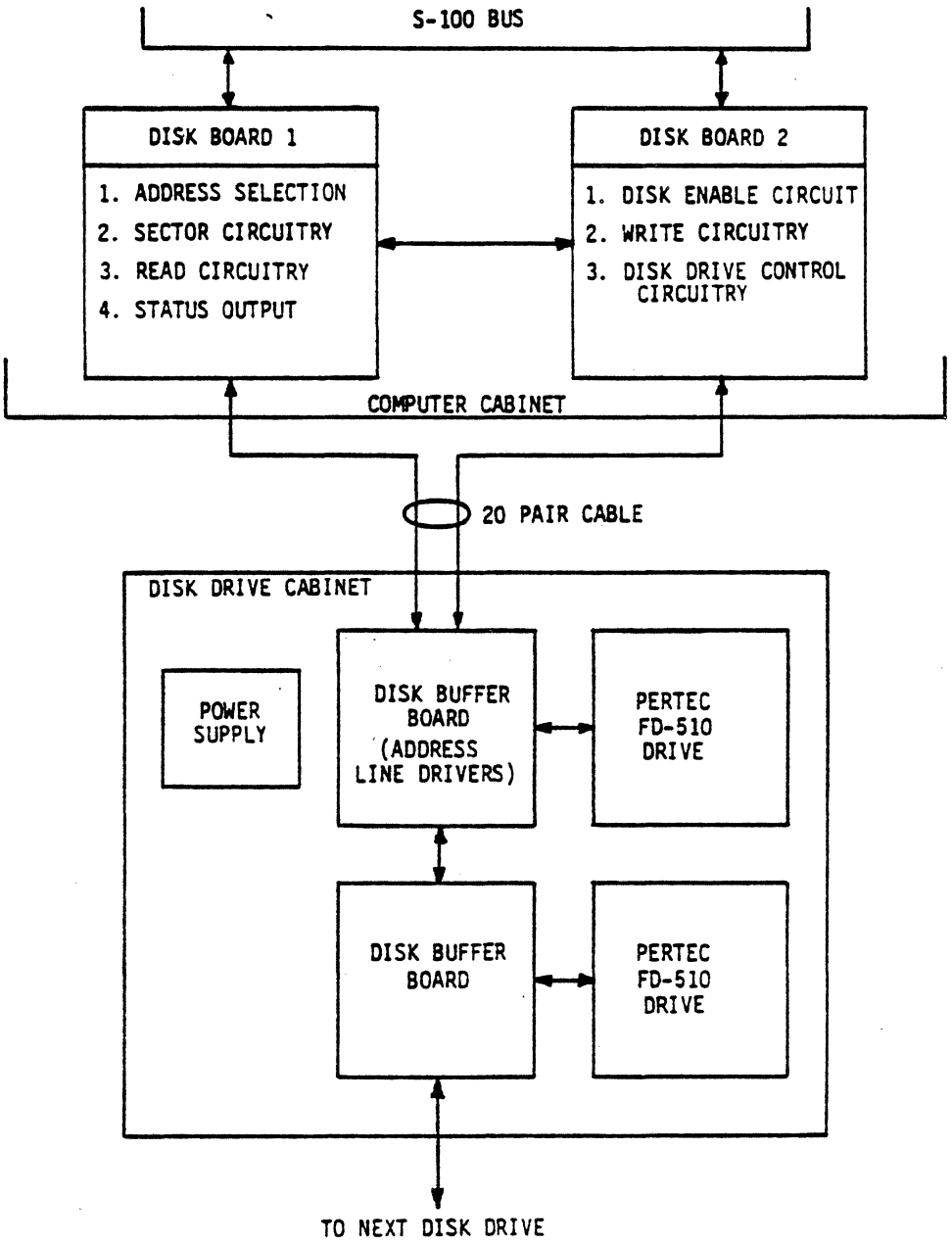
- Interconnect Cable
  A 20-pair flat cable with two 40-pin connectors (3M type plug-on) "daisy chains" one Disk Drive to another in multiple Disk Systems. Another 20-pair flat cable with a 40-pin 3M plug-on connector on one end, and a DC-37 type 37 pin connector on the other end, connects the Disk Drive to the Disk Controller.

- Disk Drive Cabinet

  - Power Supply
    The Disk Drive Cabinet contains a Power Supply for powering the Disk Buffers and Disk Drives.

  - The Disk Buffer
    The Disk Buffer board contains the necessary line drivers and receivers for interconnection with long cables to the Disk Drive. In addition, it contains the Disk Drive Address Circuitry that allows the controller to select one of 16 Disk Drives. The Disk Buffer board also contains the line drivers for connection of multiple Disk Systems.

  - The Disk Drive
    The Disk Drive (PERTEC FD-510) contains the mechanism and electronics that actually Read and Write data on the Diskette.

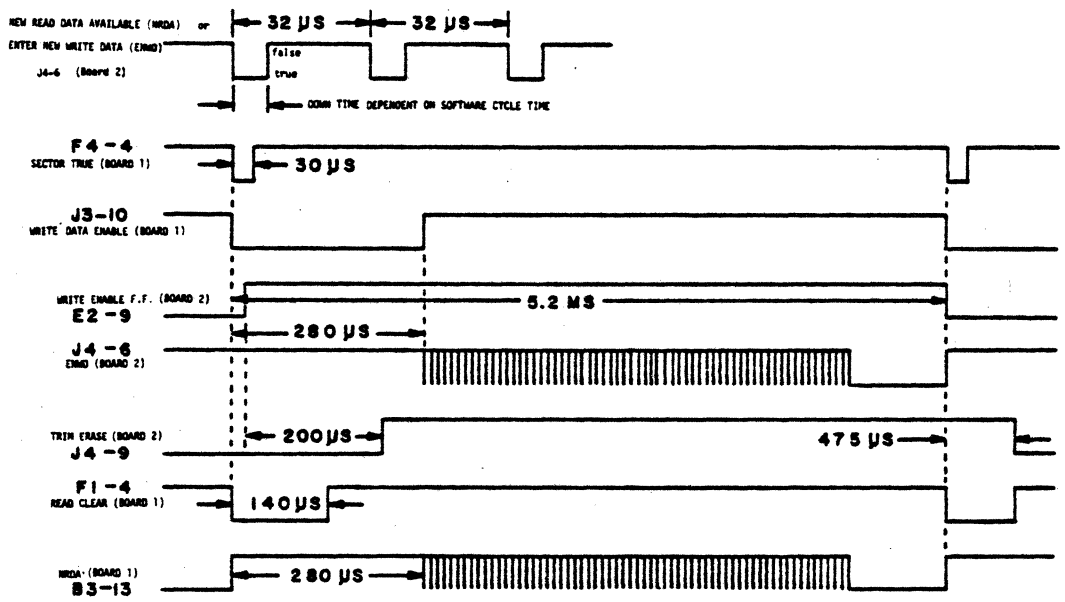


Floppy Disk System Block Diagram

4 THEORY OF OPERATION

4-3 READ/WRITE FUNCTION TIMING

The diagram below shows the timing relationships for the various signals involved in reading or writing.



Read/Write Function Timing

4 THEORY OF OPERATION

4-4 GENERAL SYSTEM OPERATION

This topic presents an overview of the system operation.

In order to begin Disk operation, the computer must select and enable the Disk Drive and Controller. The desired Disk address (000 to 017_8 is output on I/O Channel 010_8. Track 0 is found by stepping the head out to the outermost track (Output-Channel 011_8, Bit D1 = 1) and testing the Status (Input-Channel 020_8, Bit D6 = 0).

After the appropriate reference for Track 0 is found, the computer steps the head in (output-Channel 011_8, Bit D0 = 1) to the desired track, then loads the Disk Read/Write head on the Disk surface (Output 011_8, Bit D2 = 1). The head may be loaded before stepping if desired. Software is responsible for knowing which track the Disk head is on, once Track 0 has been found.

The correct Sector is located by performing an input from the Sector Channel (Input-Channel 011_8) and comparing the desired Sector number with the Sector count from the Controller circuit. After the Disk reaches the correct rotational position or Sector, the computer either performs a Read Data function (Input-Channel 012_8, D0-D7) or enters a Write Data mode. In the Write mode, the Write Circuits must be enabled (Output-Channel 011_8, D7 = 1). A few hundred microsecond delay elapses befor Write Data is requested, after which a new byte of Write Data is requested every 32 microseconds.

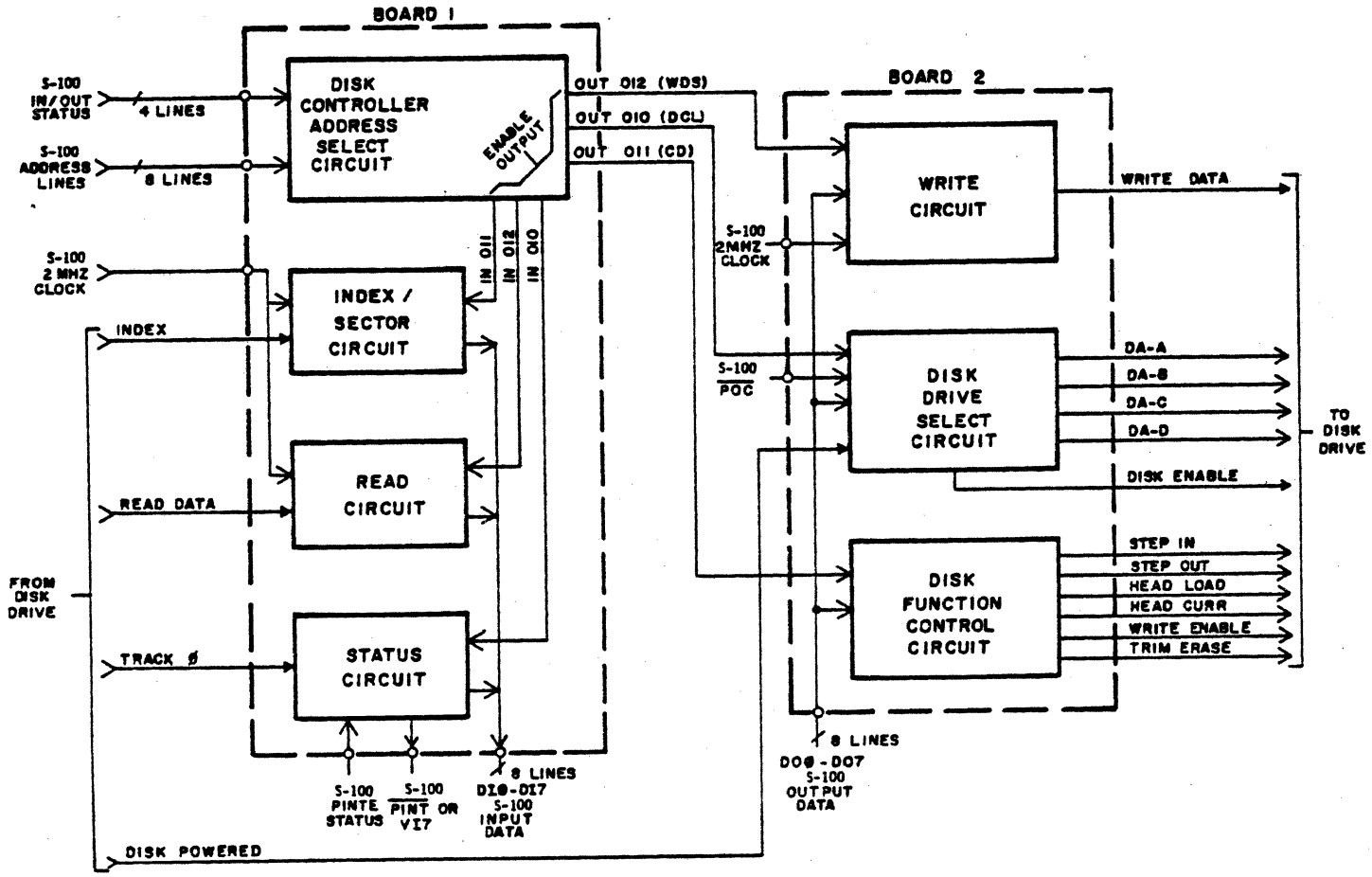
When the computer has finished accessing the Disk, Disk Control is cleared (Output-Channel 010_8, D0 through D7 - 1 or 377_8). Clearing Disk Control disables the Drive and causes all Disk functions to cease. Turning the Disk Drive power off, disconnecting the cable, or opening the Disk Drive door also clears Disk Control.

When changing access from one Drive to another, Disk Control must be cleared (Output-Channel 010_8, 377_8) before enabling the new Disk. This is to insure the Controller circuits are reset before accessing a new Drive.

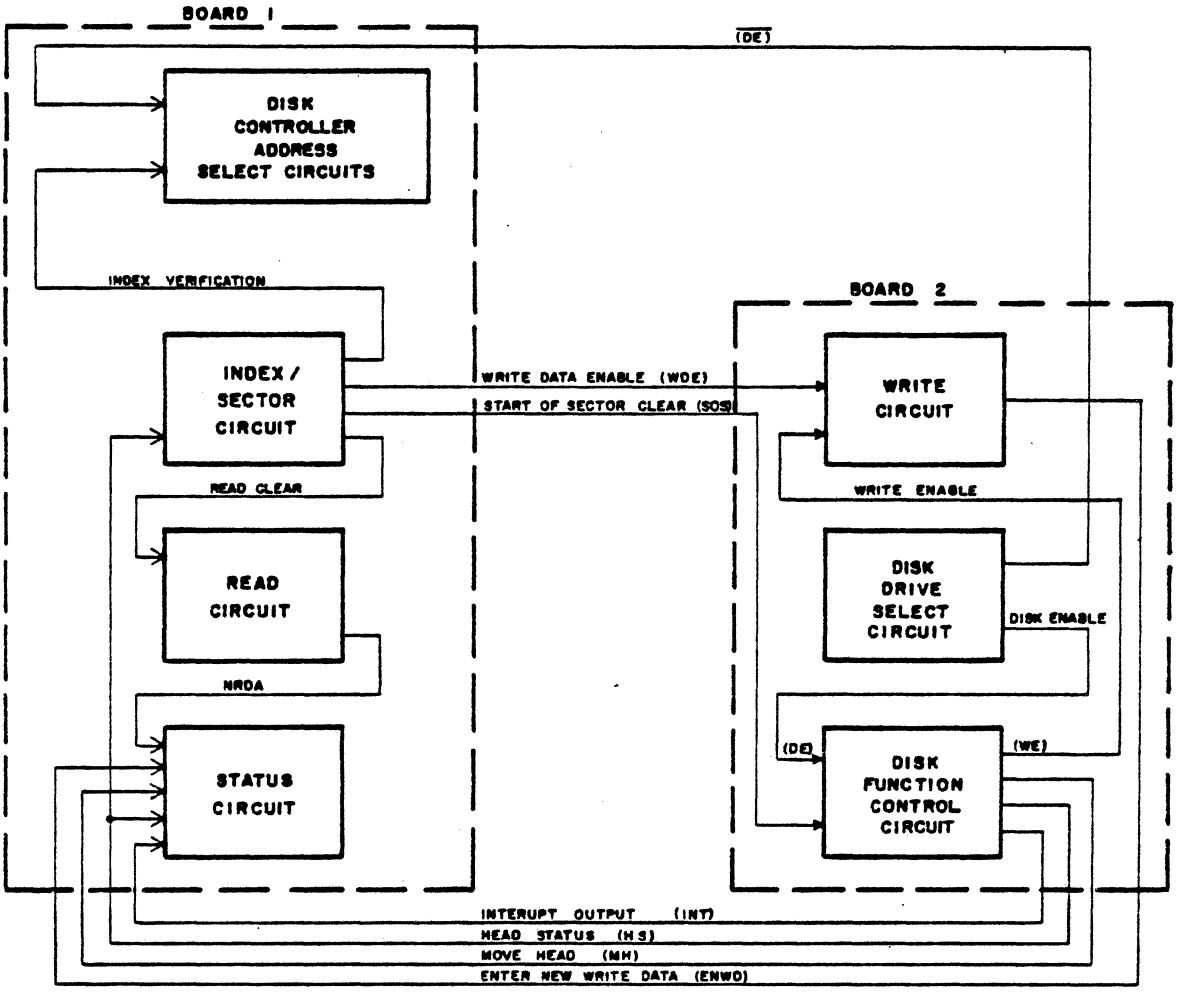
4 THEORY OF OPERATION

4-5 DISK CONTROLLER BLOCK DIAGRAMS

The Disk Controller Block Diagrams presented on this and the facing page show graphically the functions which will be described in the following sections.



Disk Controller Block Diagram
(Sheet 1. Internal Connections)



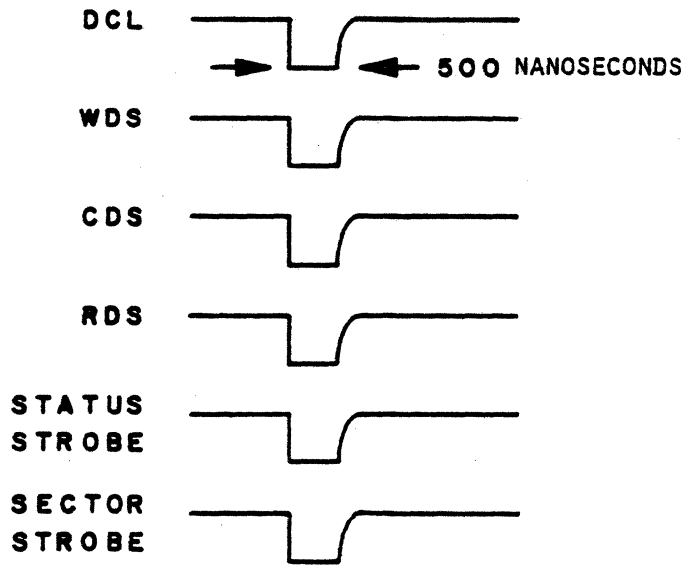
Disk Controller Block Diagram
(Sheet 2. External Connections and Address Select)

4 THEORY OF OPERATION

4-6 DISK CONTROLLER DESCRIPTION

This section gives an overall description of the function of the Disk Controller (Disk Boards 1 and 2).

The Disk Controller Address Select Circuit accepts Input and Output (I/O) instructions from the computer on I/O Channels 010_8, 011_8, and 012_8. The computer I/O Address Lines (8 lines) select one of the three above mentioned Channels, and the computer I/O Status lines (4 lines) determine whether an input or output instruction is required. An I/O instruction to any Channel results in a LOW-going 500 nanosecond pulse, as shown.



I/O Channels 010_8, 011_8, and 012_8

The three Output functions are:

1. Output on Channel 010_8: Disk Control Latch (DCL) selects Disk address latches and enables Controller.

2. Output on Channel 011_8: Control Disk (CDS) controls Disk Drive functions such as Head Load, Step In or Out, Write Enable, etc.

3. Output on Channel 012_8: Write Data Strobe (WDS) strobes Write Data bytes into write data latch during Disk Write mode. WDS also resets ENWD (Enter New Write Data) status bit until next byte is requested.

The three Input functions are:

1. Input on Channel 010_8: Places Disk status information on the computer Data Bus. Status information includes: Head Status (HS); OK To Move Head (MH); Enter New Write Data (ENWD); New Read Data Available (NRDA).

2. Input on Channel 011_8: Places the Disk Sector count on the computer Data Bus. As the Disk rotates, the Sector count is incremented every 5.2 milliseconds, and is reset to 0 upon detection of the Index hole once every rotation (166.6 milliseconds).

3. Input on Channel 012_8: Places Disk Read Data on the computer Data Bus. This input instruction resets the NRDA Status bit.

Upon an Output to Channel 010_8, the Disk Control Latch (DCL), Disk Drive Select Circuits are enabled with DA-A through DA-D selecting 1 of 16 possible Disk Drives. The Disk Powered line enables the Disk Drive Select Circuit when the Drive selected is properly connected and powered. When the Disk is selected and enabled, the Disk Enable (DE) signal is presented to the Disk Function Control Circuit, where DE enables the Status information.

The Disk Function Control Circuits, when selected, produce Interrupt Output, Move Head or Head Status signals which are transferred to the Disk Status Circuits. Control Circuits also load the head on the Disk (Head Load), step the head out (Step Out), step the head in (Step In), control head current (Head Curr) and enable the Write Circuit (Write Enable). Control signals, Disk address information and Write Data are transferred from the computer to Disk Board 2 by eight Output Data Lines (D00-D07).

Write Data is transferred to the Write Circuit upon an output to Channel 012_8, the Write Data Strobe (WDS). The rate of serial Write Data to the Disk is controlled by dividing the computer 2MHz Clock. Enter New Write Data (ENWD) is the Status signal generated by the Write Circuit when new Write Data is requested.

When Index and Sector pulses are received by the Index/Sector Circuit, and the Index pulse is detected, Sector count (beginning with Sector 0) may begin. The Index/Sector Circuit is synchronized by the computer 2MHz Clock, and upon an output to Channel 011_8, the Sector count is presented. The Index/Sector Circuit also provides a Start Of Sector Clear (SOS) signal to the Disk Function Control Circuit, a Write Data Enable (WDE) signal to the Write Circuit and the Read Clear signal to the Read Circuit. Index Verification and a True (LOW) condition on Head Status must be present before the Address Select Circuits can enable the Sector information from Channel 011_8.

When Read Data is present from the Disk Drive and transferred to the computer Data Bus, the Read Circuit is enabled by addressing Input Channel 012_8. The Read Circuit provides the NRDA (New Read Data Available) Status signal when Read Data is detected.

The Status Circuit provides information on the state of the Controller and Disk Drive. A desired track is found by referencing Track 0 (the outermost track). Track 0, NRDA and the other Status signals are enabled by addressing Input Channel 010_8. Input data is transferred from the Index/Sector Circuit, Read Circuit, or Status Circuit to the computer by eight Input Data Lines (D10-D17).

4 THEORY OF OPERATION

4-7 ADDRESS SELECT CIRCUIT

This section describes the Address Select Circuit.

The Address Control Circuit (Disk Board #1, Sheet 1) accepts I/O instructions from the computer on Channels 010_8, 011_8 and 012_8.

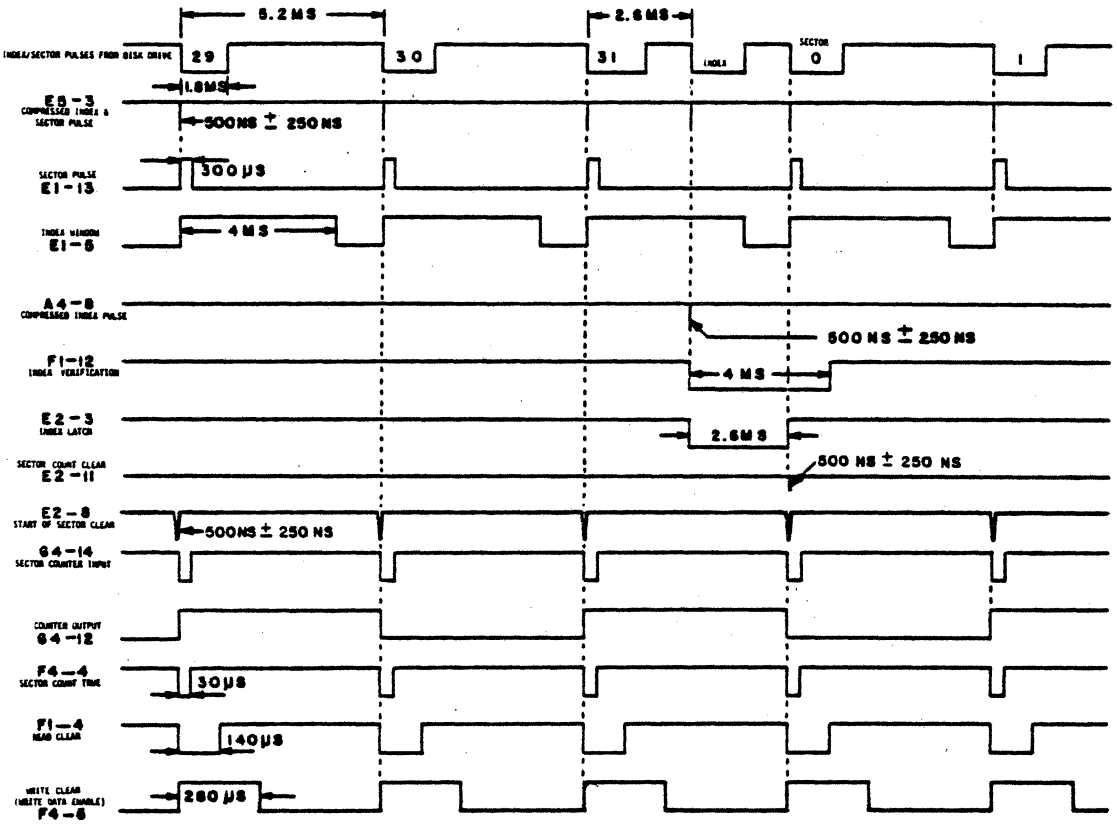
To enable any of the strobe gates A3, A4 or A5, F5 pin 8 must be enabled LOW. F5 pin 8 is LOW when address lines A15-A8 equal $01X_8$ (X represents a User Selectable condition for A8-A10). A15-A12 is LOW, inverted HIGH at G5 pins 2, 4, 6 and 8 and appear HIGH at F5. With A11 HIGH, F5 pin 8 goes LOW and is inverted HIGH to A5 pin 1. Address lines A10-A8, when equal to $XX0_8$, $XX1_8$, or $XX2_8$ (XX represents a User Selectable condition for address lines A11-A15 described above), enable one of the AND gates B4 pins 6, 8 or 12. When A8, A9 and A10 are all LOW, B4 pin 6 is enabled, allowing an Input or Output on Channel 010_8. When A9 is HIGH and A10 and A8 are LOW, B4 pin 12 is enabled, allowing an Input or Output on Channel 012_8. When A8 is HIGH and A10 and A9 are LOW, B4 pin 8 is enabled, allowing an Input or Output on Channel 011_8. AND gates B4 determine the I/O Channel to be addressed, since only one gate is enabled at a time. A specific output instruction is then selected if SOUT is HIGH and PWR is LOW, and the specific input instruction is recognized when SINP and PDBIN are HIGH. When the Disk is enabled, the Disk Enable line (DE) goes HIGH, enabling the Input Status Strobe (Channel 010_8) and allowing Index Verification Flip-Flop B3 to be clocked.

4 THEORY OF OPERATION

4-8 INDEX/SECTOR CIRCUIT (011_8 - INPUT)

This section describes the Index/Sector Circuit.

As the Diskette rotates in the Drive, an optoelectronic sensor detects the 32 Sector holes and the Index hole on the Diskette. The Sector holes generate a 1.8 millisecond pulse every 5.2 milliseconds (Refer to the figure on the facing page for timing diagram relating to Index/Sector Circuits). The Index hole, located halfway between Sector holes 31 and 0, generates a 1.8 millisecond pulse every revolution (166.7 milliseconds).



Index/Sector Timing

The Index or Sector pulse (IND) appears LOW and is inverted HIGH to E5 pin 2 (Disk Board #1, Sheet 1). E5 pin 3 is enabled LOW until E3 pin 13 is clocked. The 2 MHz Clock goes LOW at pin 49 of the bus and is inverted by J3 pin 8, clocking Sector Pulse Compressor Flip-Flop E3 pin 13. The output pulse width (500 ± 150 nanoseconds) of E5 pin 3 is dependent on the propagation time of the flip-flop and the delay time of the RC time constant of R7 and C30 (RC time constant applies to REV 1 board only). After being inverted, E5 pin 3 appears HIGH at the Index Window Gate, A4 pin 11. A4 separates the Index pulse from the Sector pulses. A2 pin 10 is enabled HIGH when E5 pin 3 goes LOW. Sector Pulse One-Shot E1 pin 13, goes HIGH for 300 microseconds, which triggers Index Window One-Shot E1 pin 5 HIGH for 4 milliseconds. A4 pin 8 is only enabled

when the Index pulse enables E5 pin 3 since E1 pin 4 and E1 pin 5 are HIGH at A4 pins 9 and 10 at this time. The 300 microsecond LOW-going pulse at E1 pin 4 also toggles 4-Bit Sector Counter G4 pin 14.

E1 pin 5 is HIGH, leaving A2 pin 8 HIGH when the Index pulse appears at A2 pin 9. As a result, A2 pin 10 is not enabled when the Index pulse appears, allowing only Sector pulses to trigger E1 pin 13. In addition to enabling E1 at pin 10, the HIGH 300 microsecond pulse at E1 pin 13 is also present at E2 pin 10. E2 pin 8 is enabled LOW when E1 pin 13 is HIGH, since E3 pin 8 is in a reset condition (E3 pin 8 HIGH). The 2MHz Clock enables Sector Pulse One-Shot-Compressor F2 pin 9 HIGH, and on the falling edge enables E3 pin 8 LOW. When E3 pin 8 goes LOW, E2 pin 8 is disabled. When E2 pin 8 is disabled HIGH, Sector Count True One-Shot F4 pin 4 toggles LOW for 30 microseconds. If it is the first Sector pulse after the Index pulse, Index Latch E2 pins 3 and 6 are reset, forcing E2 pin HIGH. The LOW at E2 pin 8 also appears on Disk Board #2, Sheet 2, as the Start of Sector Clear (SOS) signal, which clears the Write Circuit at the end of a Write mode.

After a valid Index pulse has been detected, A4 pin 8 (Disk Board #1, Sheet 1) is enabled LOW, setting the Index Latch with E2 pin 3 LOW. When E2 pin 3 is LOW, Index Latch Pulse Compressor F3 pin 13 is cleared. A4 pin 8 also triggers F1 pin 12 LOW for 4 milliseconds. After 2.6 milliseconds, the Index Latch is reset by a Sector pulse, leaving E2 pin 3 HIGH. E2 pin 11 is enabled LOW until Index Latch Pulse Compressor Flip-Flop F3 pin 13, is clocked by the 2MHz Clock pulse. The 500 (±250) nanosecond output pulse at E2 pin 11 is dependent on the propagation time of F3 pin 13 and the delay time of the RC time constant of R8 and C20 (RC time constant applies to REV 1 board only). A2 pin 1 is HIGH for 500 (±250) nanoseconds if F1 pin 12 has been triggered LOW. This clocks B3 pin 8 LOW, if B3 pin 7, the Head Status (HS ST) signal is HIGH. Head Status goes HIGH 45 milliseconds after the head is loaded on the Disk. A LOW at B3 pin 8 indicates that the correct Index pulse has been detected. The Index Latch, in allowing E2 pin 11 to be enabled, also resets 4-Bit Sector Counter G4, at pins 2 and 3. Since this occurs on the first Sector pulse after the Index pulse, a correct Sector count is guaranteed every revolution. Input Sector Strobe (Channel 011_8) is enabled when A2 pin 4 goes HIGH. This occurs only when the Index Verification Flip-Flop is set (B3 pin 8 LOW) and the Head Status signal is LOW, indicating that the head is properly loaded for Reading and Writing. Drivers H5 pins 9, 11, 5, 7, 3 and 13 are then enabled when A3 pin 8 goes LOW. The Sector count is then transferred to the bus. The correct Sector is located by comparing the desired Sector number with the Sector count from this Index/Sector Circuit. Software also checks D10 to see if it is the beginning of the Sector.

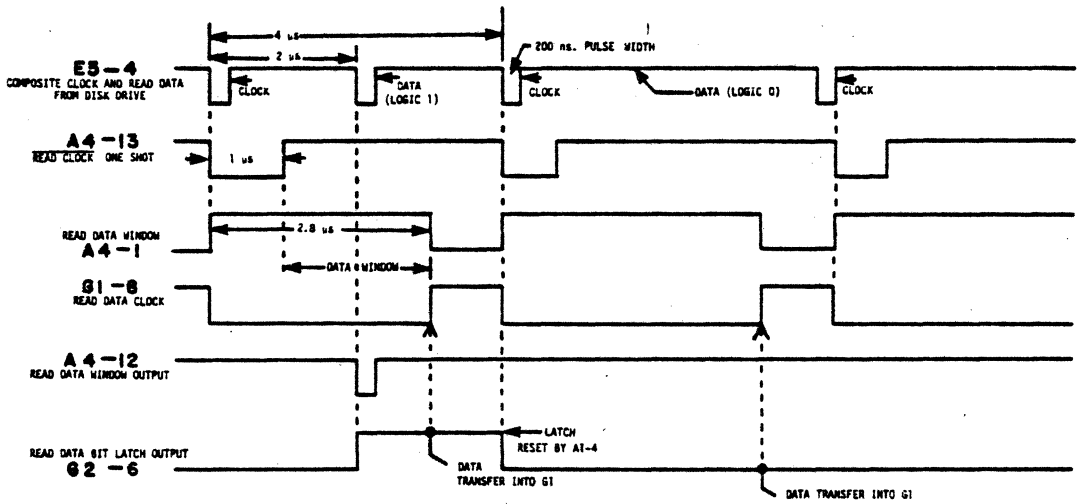
When Sector Count True One-Shot F4 pin 4 is triggered LOW for 30 microseconds, Write Clear One-Shot F4 pin 5 goes HIGH for 280 microseconds. F4 pin 5 is a timer that prevents Write Data (other than 0's from being written during the first 280 microseconds of a Sector by inhibiting the request for Write Data. When F4 pin 5 goes LOW, J3 pin 10 goes HIGH, enabling the Write Circuit to request Write Data. F1 pin 4 is also triggered by Sector Count True One-Shot F4. F1 pin 4 is a timer that turns off the Read Circuit at the beginning of every Sector by going LOW for 140 microseconds. This prevents the reading of false data, and insures proper synchronization with the read clock for detection of the sync bit.

4 THEORY OF OPERATION

4-9 READ CIRCUIT (012_8 - INPUT)

This section describes the Read Circuit.

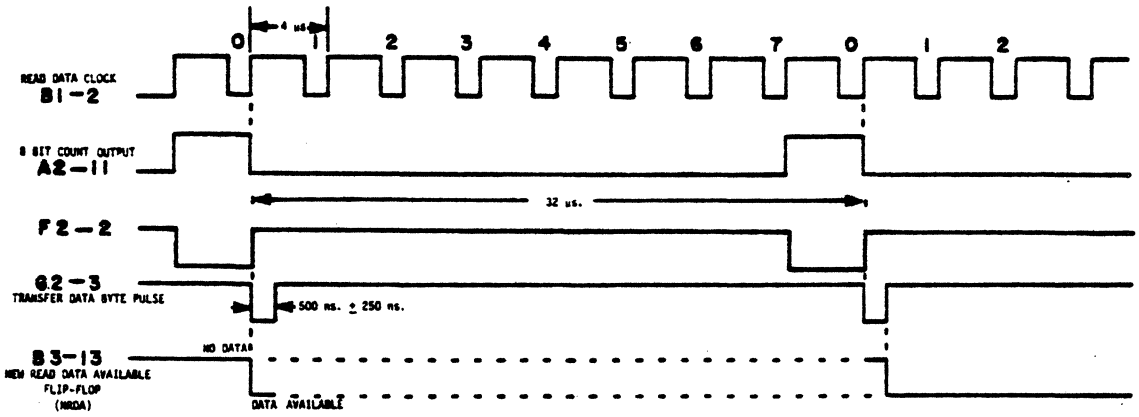
Composite read clock and data consisting of LOW-going 200 nanosecond pulses is received from the Disk Drive at Read Data Mask Gate, E5 pin 4 (Disk Board #1, Sheet 2). The read clock pulse occurs every 4 (±1) microseconds, and the read data pulse occurs 2 micorseconds later if it is a logic 1 (Refer to the Read Circuit Timing Diagram). When a clock pulse is received, E5 pin 6 is enabled HIGH, triggering Read Clock One-Shot A1 pin 4 LOW for 1 microsecond. This LOW is present at the Read Data Window Gate, A4 pin 13. A2 pin 13 is HIGH for 1 microsecond, triggering the Read Data Window Gate, A1 pin 5 HIGH and A1 pin 12 LOW for 2.8 microseconds. A1 pin 4 returns HIGH after 1 microsecond, leaving A4 pin 13 and the Read Data Bit Latch G2 pin 9 HIGH. If a logic 1 data bit is received at E5 pin 4, it is inverted HIGH by E4 pin 2 allowing A4 pin 12 to go LOW. This sets Read Data Bit Latch G2 pin 6 HIGH, indicating a logic 1 data bit has been received. After 2.8 microseconds, A1 pin 12 returns HIGH and clocks the Read Data Serial-to-Parallel Shift Register G1 pin 8. Serial Data at G2 pin 6 is then transferred to G1 pins 1 and 2. The Read Data Bit Latch is reset when A1 pin 4 receives the next clock pulse form the Disk Drive and returns LOW. If a logic 0 data bit is received at E5 pin 4 the Read Data Bit Latch remains reset (G2 pin 6 LOW), and a logic 0 is clocked into Divide-By-Eight Counter B1.



Read Circuit Timing Diagram

The sync bit is the first logic 1 data bit detected after the 140 microsecond pulse at the beginning of every Sector. B1 is held in a LOAD condition (does not count) until the sync bit is detected. Since Write Data is not enabled for 280 microseconds from the beginning of a Sector, Read Data will not be available during that time. The Divide-By-Eight Presettable Counter, B1 (refer to the Read Timing Diagram), counts eight read clocks and toggles on the trailing edge of the $\overline{Q}$ output at A1 pin 12. A2 pin 11 goes HIGH every 32 microseconds on the leading edge of the clock pulse at B1 pin 2. G1 pin 13 goes HIGH seven read data clocks after the sync bit has been detected, and clocks the Sync Bit Detector

Flip-Flop, B2 pin 8 LOW. B1 pin 15 returns LOW after 4 microseconds allowing A2 pin 13 to go HIGH. This enables G2 pin 3 LOW for 500 nanoseconds until Read Latch Pulse Compressor Flip-Flop F2 pin 1 is clocked. The output pulse width is dependent on the propagation time of the Flip-Flop and the delay time of the RC time constant of R21 and C29 (RC time constant applies to REV 1 board only). When the Read Latch Pulse Compressor Flip-Flop, F2 pin 13, is clocked by the 2MHz Clock pulse at F1 pin 1, F2 pin 13 is enabled LOW, disabling G2 pin 3. When G2 pin 3 is enabled LOW and inverted by J3 pin 6 and J3 pin 4, data present at G1 outputs A through H is transferred to the D_A through D_D inputs of Read Data Latches G3 and H1. The HIGH at J3 pin 6 also clocks New Read Data Available Flip-Flop B3 pin 13 LOW, enabling the New Read Data Available (NRDA) Status signal at H2 pin 14. As G2 pin 3 returns HIGH, the clock inputs of latches G3 and H1 go LOW and latch the data present at the D_A through D_C inputs to the Q_A through Q_D outputs. When an input is done on Channel 012_8 (Input Read Data Strobe), line drivers H4 pins 9, 3, 5 and 7 and H3 pins 5, 7 3 and 9 allow data at outputs Q_A through Q_D to be transferred to the computer Data Bus.



Read Timing Diagram

At the beginning of every Sector, the Read Clear One-Shot, F1 pin 4 (Disk Board #1, Sheet 1), goes LOW for 140 microseconds, clearing Divide By Eight Presettable Counter B1, Sync Bit Detector Flip-Flop B2, and Read Data Serial-To-Parallel Shift Register G1. When Input Read Data Strobe goes LOW, New Read Data Available Flip-Flop is cleared.

4 THEORY OF OPERATION

4-10 STATUS CIRCUIT (010_8 - INPUT)

This section describes the Status Circuit.

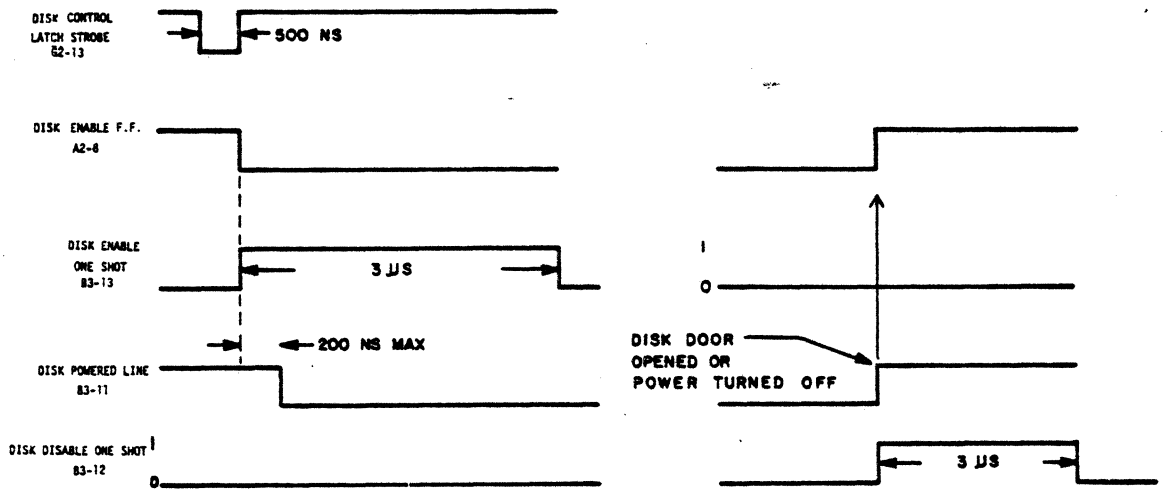
When an input occurs on Channel 010_8, Disk Status information (Disk Board #1, Sheet 2) is transferred to the computer Data Bus. Status signals include: Head Status (HS), Move Head (MH), Interrupt Status (INT STATUS), Enter New Write Data (ENWD), New Read Data Available (NRDA), and Track 0 (TRK 0). Track 0 is generated by the Disk Drive unit and indicated when the head is on the outermost track (discussed in Section 5-10). When the Input Status Strobe is enabled LOW at A3 pin 6 (Disk Board #1, Sheet 1), line drivers H3 pins 13 and 11 (Disk Board #1, Sheet 1), and H2 pins 5, 11, 9, 7, 3 and 13 are enabled, allowing Status information to be applied to the computer Data Bus.

4 THEORY OF OPERATION

4-11 DISK ENABLE CIRCUIT (010_8 - OUTPUT)

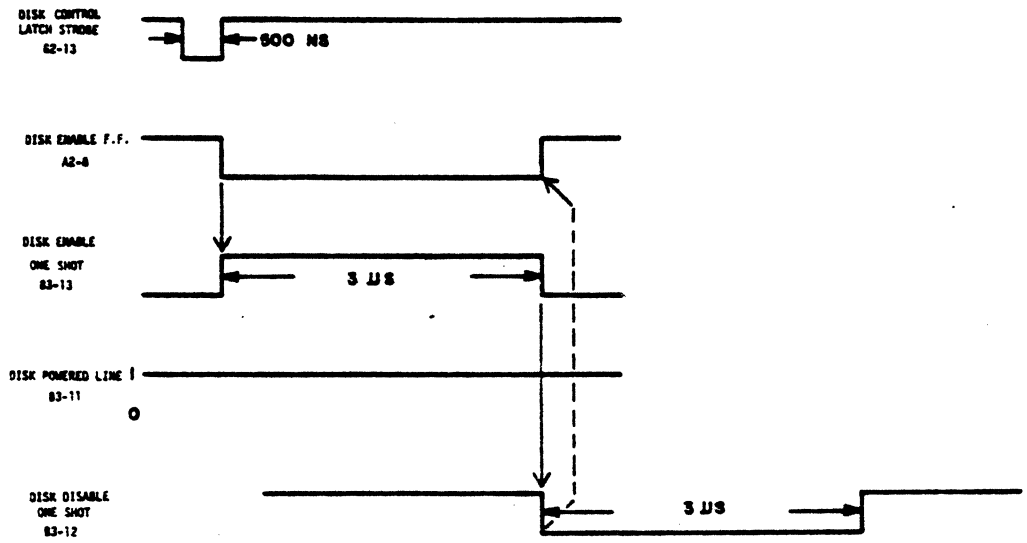
This section describes the Disk Enable Circuit.

When the Disk Control Latch Strobe (Channel 010_8 - OUT) is enabled LOW 500 nanoseconds (Disk Board #2, Sheet 1) and inverted HIGH at G2 pin 12, Disk Address Latch J3, and Disk Enable Flip-Flop A2 are clocked (Refer to the figure below). Data Out Bus lines DO0-DO3 transfer the Disk address information through inverters G4 pins 4, 2, 6 and 10 to Disk Address Latch J3 pins 2, 3, 6 and 7. As the clock goes HIGH at J3 pins 13 and 4, data is latched into the D_A through D_D inputs, and as the clock returns LOW, data present at the D_A through D_D inputs is transferred to the $\overline{Q}_A$ through $\overline{Q}_D$ outputs. The address information then enables 1 of 16 possible Disk Drives through line drivers K3 pins 5, 7, 13 and 11. The Disk Enable Flip-Flop, A2 pin 8, is clocked LOW providing the Disk Enable One-Shot B3 pin 1 (Disk Board #2, Sheet 1), allowing B3 pin HIGH for 3 microseconds 50 to 200 nanoseconds after the Disk Drive is enabled, the Disk Power line goes LOW at Disk Disable One-Shot B3 pin 11. This prevents the Disk Disable One-Shot from being triggered by the Disk Enable One-Shot.



Disk Enable Timing With Valid Disk Address (Disk Board #2, sheet 1)

If a Disk is not connected, there is no power, or the door is open, the Disk Power line stays HIGH at B3 pin 11, allowing B3 pin 9 to be triggered. B3 pin 12 is triggered LOW for 3 microseconds, enabling E2 pin 11 HIGH (Refer to the figure below). This leaves F3 pin 13 LOW, and Disk Enable Flip-Flop A2 is cleared. A2 is also cleared when POC (Power On Clear) is LOW, or by the Disk Control Latch when Data line DO7 is HIGH. This allows F3 pin 13 LOW, clearing A2 pin 6. When DO7 is HIGH, it is inverted LOW by H4 pin 8, leaving F3 pin 8 LOW. When the Disk Control Latch goes LOW, F3 pin 10 is enabled HIGH. This leaves F3 pin 13 LOW, and the Disk Enable Flip-Flop is cleared.



Disk Enable Timing With Invalid Disk Selection (Disk Board #2, sheet 1)

4 THEORY OF OPERATION

4-12 WRITE CIRCUIT (012_8 - OUTPUT)

This section describes the Write Circuit.

NOTE

This description uses the Timing Diagrams in the next section.

Software detects Sector True status, and the desired Sector is located. An output to Channel 011_8 (Control Disk Strobe), with data line DO7 LOW, enables J1 pin 10 (Disk Board #2, Sheet 2) HIGH. This toggles Write Enable Flip-Flop E2 pin 9 HIGH for 5.2 milliseconds. The HIGH at E2 pin 9 is present at E3 pin 1 (Disk Board #2, Sheet 1).

The Write Data Enable signal (refer to the Read/Write Timing Diagram) is generated when Sector Count True One-Shot F4 pin 4 (Disk Board #1, Sheet 1 is enabled LOW for 30 microseconds, triggering Write Clear One-Shot F4 pin 5 HIGH for 280 microseconds. The HIGH at F4 pin 5 is inverted LOW at J3 pin 10 and presented to the New Write Data Request Flip-Flop, J4 pin 2 (Disk Board #2, Sheet 1). The 280 microsecond delay inhibits the Enter New Write Data request at the beginning of a Sector. After 280 microseconds, J4 pin 2 goes HIGH. J4 pin 6 is toggled LOW by the next pulse from Write Byte Counter A4. J4 pin 6 goes LOW every 32 microseconds. The width of the Enter New Write Data Status pulse depends on software, and each pulse is cleared upon an output to WRT (Write) Data Strobe (Channel 012_8).

The Parallel-To-Serial Write Data Shift Register must not be clocked during the 280 microsecond delay at J4 pin 2. Clocking is inhibited when Clock Inhibit (CLOCK INHIB), H2 pin 6 is HIGH. Since WRT ENABLE is initially LOW and WRT (Write) DATA STROBE is initially HIGH, E3 pin 3 is HIGH. Logic 0 bits are written to the Disk Drive during the first 280 microseconds because H2 is not clocked, and output pin 13, cleared by a LOW on the WRT ENABLE line before the Write Circuit was enabled, is at logic 0. When J4 pin 6 is enabled LOW, software detects Enter New Write Data Status True, and outputs the first byte to Channel 012_8, enabling WRT DATA STROBE LOW. The first D7 bit written, the sync bit, must be logic 1. When WRT DATA STROBE is LOW at E3 pin 5 and E3 pin 1 is HIGH, E3 pin 3 is enabled LOW. CLOCK INHIB is then LOW, allowing H2 to shift data when clocked at pin 7.

In addition to allowing H2 to be clocked, WRT DATA STROBE also strobes data into Write Data Latches H3 and G3. Data present on the computer Data Out Bus, DO0 through DO7, is inverted by G4 pins 2, 4, 6, 10 and 12, and H4 pins 8 and 10, and transferred to the Disk Drive Control Signal Decoders (Disk Board #2, Sheet 2). When H3 and G3 go HIGH at pin 13, data is latched into the D_A through D_D inputs. WRT DATA STROBE (Channel 012_8 - OUT) goes LOW for 500 nanoseconds, is inverted HIGH by G2 pin 8 and G2 pin 10, and clocks H3 and G3. Data present at D_A through D_D is transferred to $\overline{Q}_A$ through $\overline{Q}_D$ when the clock at pin 13 goes LOW.

Data is then available at the Parallel Data Input of Parallel-To Serial Write Data Shift Register H2. Write Byte Counter A4 counts eight 500-nanosecond clock pulses from the Write Clock + Data Window Generator, A3 pin 15 to the Parallel-To-Serial Write Data Shift Register, H2 pin 15 (Refer to the Write Circuit Timing Diagram). On the eighth count, A4 pin 15 will go HIGH for 4 microseconds. This HIGH is inverted LOW by B4 pin 12 to H2 pin 15 and enables the Parallel Data Inputs ($\overline{0}$ through 7). On the next H2 pin 7 clock pulse, data present at $\overline{Q}_A$ through $\overline{Q}_D$ of the Write Data Latches is synchronously loaded into the Shift Register.

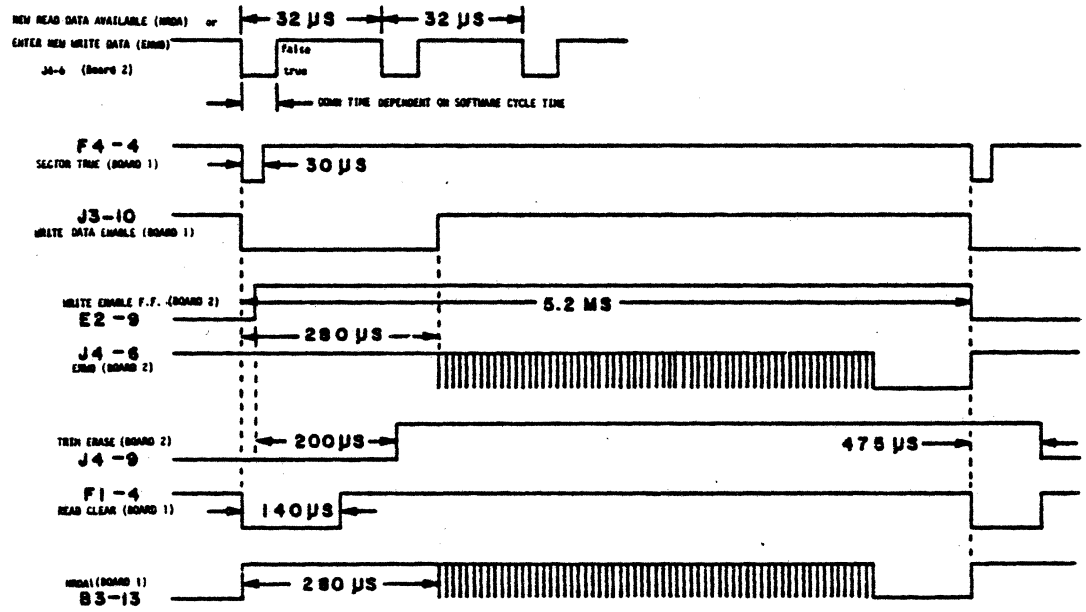
In addition to clocking the Write Byte Counter, A4 pin 2, the Write Clock + Data Window Generator, when HIGH at A3 pin 15, provides the write clock pulse to F4 pin 12. A_{OUT}, B_{OUT}, and C_{OUT} are gated together to provide the Write Data Window at E4 pin 6.

The Write Clock + Data Window Generator, A3, is enabled when the 2 MHz Clock goes LOW, and is inverted HIGH by G4 pin 8 (refer to the Write Timing Diagram). In addition to clocking A3 pin 2, the 2 MHz Clock is also present at F3 pin 3. On the eighth 2 MHz Clock pulse, occuring every 4 microseconds, A3 pin 15 (RC) is HIGH for 500 nanoseconds and, after being inverted LOW by B4 pin 6 is present at F3 pin 2. When the 2 MHz Clock pulse goes LOW at F3 pin 3, F3 pin 1 is enabled HIGH, clocking H2 pin 7. When H2 pin 15 (SER/ØPAR) is HIGH, H2 pin 13 (Serial Data Out) goes HIGH. The HIGH at H2 pin 13 is inverted by B4 pin 10 and Serial Write Data appears LOW to F4 pin 3. When A_{OUT} and B_{OUT} are HIGH, and C_{OUT} is inverted HIGH by G2 pin 6, E4 pin 6 is enabled LOW. F4 pin 1 is enabled HIGH, ensuring F4 pin 13 is LOW (Refer to the Write Circuit Timing Diagram and the Write Timing Diagram), and the Disk WRT DATA input is enabled through line driver K3 pin 9. The Write Data Windows are developed halfway between the write clocks which are generated every 4 microseconds.

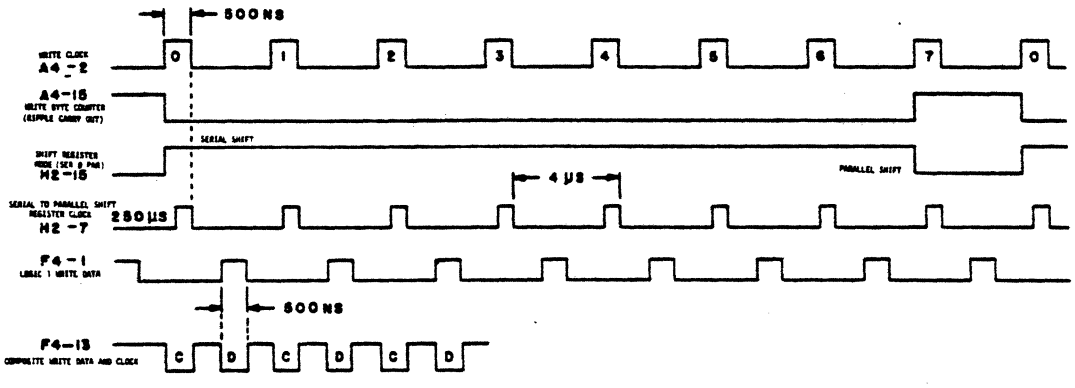
The Write Clock + Data Window Generator, A3, the Write Byte Counter, A4, and the Parallel-To-Serial Write Data Shift Register, H2, are cleared when WRT ENABLE is LOW.

4-13 WRITE CIRCUIT TIMING DIAGRAMS

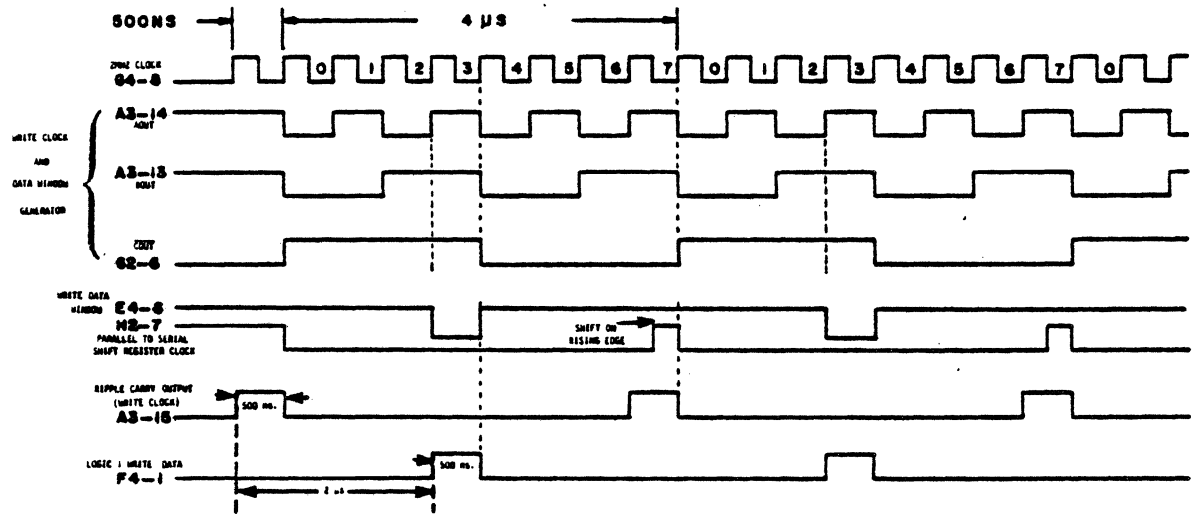
These timing Diagrams are referenced in the previous section.



Read/Write Timing Diagram



Write Circuit Timing Diagram



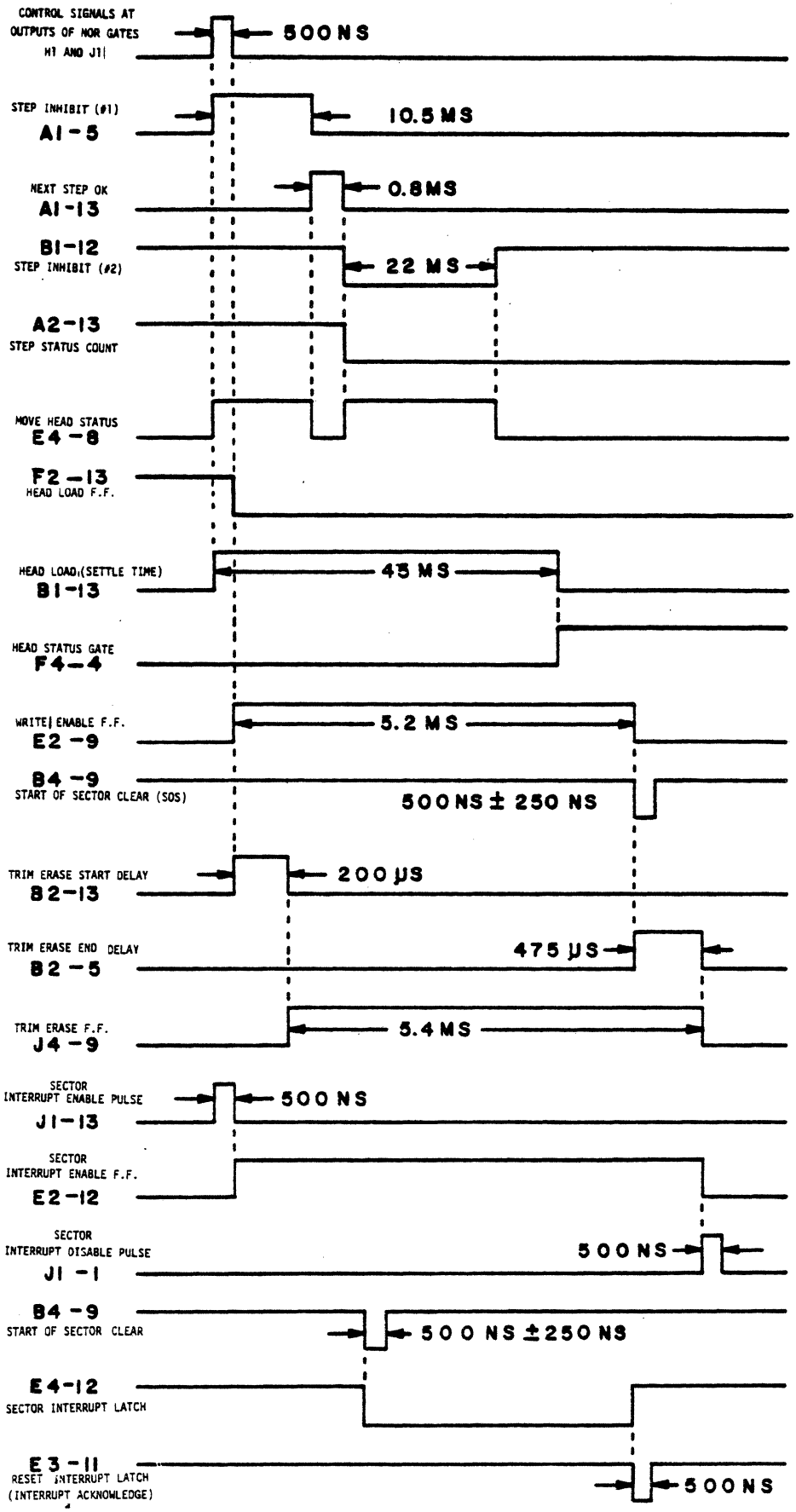
Write Timing Diagram

4 THEORY OF OPERATION

4-14 DISK FUNCTION CONTROL CIRCUIT (011_8 - OUTPUT)

This section describes the Disk Function Circuit.

Channel 011_8 - OUT controls Disk operations when both Disk Drive and Controller are enabled. Data line D00 through D07 (Disk Board #2, Sheet 1) transfer the control information from the computer Data Out Bus to the Disk Drive Unit. HIGH signals on the Data lines are inverted by G4 and H4 and appear as D00 through D07 at Control Signal Decoding Gates H1 and J1 (Disk Board #2, Sheet 2). Before the decoding gates can be enabled, the Control Disk Strobe (011_8 - OUT) line must be enabled LOW (500 nanosecond pulse). Refer to the Disk Function Control Timing Diagram on the facing page for timing diagrams relating to Disk Control Functions discussed in Sections 4-15 through 4-19.



Disk Function Control Timing Diagram

4-15 MOVE HEAD AND HEAD STATUS

This section describes the Move Head and Head Status Circuits.

When D00 or D01 is LOW at H1 pins 11 and 8 (Disk Board #2, Sheet 2, gate H1 pin 13 or 10 is enabled HIGH. The HIGH at H1 pin 10 is inverted to LOW by inverting-line-driver J2 pin 5 to the Disk Drive providing the Step Out control signal. Simultaneous Step Out and Step In commands are ignored by the Disk Drive. Step Out steps the Disk head out one position to lower numbered tracks (outer edge of Diskette). The HIGH at pin 10 is also present at F1 pin 3. The HIGH at H1 pin 13 is inverted LOW by inverting-line-driver J2 pin 3, to provide the Disk Drive Step In control signal. Step In steps Disk head in one position to higher numbered track (towards center of Diskette). The HIGH at H1 pin 13 is also present at F1 pin 2. F1 pin 1 pulses LOW for 500 nanoseconds, triggering the Step Inhibit One-Shot, A1 pin 5, HIGH for 10.5 milliseconds. The LOW at A1 pin 12 clears the Step Status Count Flip-Flop, A2 pin 2, and is also present at E4 pin 10. On the falling edge of the 10.5 millisecond pulse at A1 pin 5, the Next Step OK One-Shot, A1 pin 13, is triggered HIGH for 0.8 milliseconds. For stepping more than one track, software detects the 0.8 millisecond window and issues another step pulse. Move Head Status Gate E4 pin 8 is enabled LOW during the time A1 pin 13 is HIGH. A LOW Status at E4 pin 8 is the Move Head signal. As A1 pin 13 returns LOW for 22 milliseconds. When A1 pin 12 and B1 pin 12 have returned HIGH, the Move Head Status Gate, E4 pin 8, will be enabled LOW, provided E1 pin 8 of the Write Trim Erase Gate is LOW. E4 pin 8 provides the Move Head signal to the computer when Input Status Strobe (Channel 010_8 - INP) is enabled as described in Section 4-10. When LOW, Move Head indicates head movement is allowed.

4 THEORY OF OPERATION

4-16 HEAD LOAD AND STATUS

This section describes the Head Load and Status Circuits.

When a step command is issued and A1 pin 5 (Disk Board #2, Sheet 2) is triggered, the pulse from A1 pin 5 is gated through to the Head Load One-Shot, B1 pin 1 by F1 pin 4. When DO2 is LOW, H1 pin 4 is enabled HIGH for 500 nanoseconds. F1 pin 4 is LOW triggering Head Load One-Shot B1 pin 13 HIGH for 45 milliseconds. The HIGH at B1 pin 13 is present at F4 pin 6. H1 pin 4 going LOW clocks Head Load Flip-Flop F2 allowing pin 13 LOW. This LOW is present at F4 pin 5. After the 45 milliseconds delay, B1 pin 13 will return LOW, enabling a HIGH at F4 pin 4. This provides the Head Status signal to the Sector Status Inhibit Gate, A1 pin 5 (Disk Board #1, Sheet 1), and to the computer bus when Input Status Strobe (Channel 010_8 - INP) is enabled as described in Section 4-10. Head Status indicates when the head is properly loaded for both Writing and Reading data.

The Head Load (HD LOAD) signal is enabled when E1 pin 2 (Disk Board #2, Sheet 2) is LOW. This occurs when Head Load Flip-Flop F2 pin 13 is toggled LOW. HD LOAD is also held LOW when Write Trim Erase Gate E1 pin 8 is enabled HIGH and inverted by B4 pin 4. E1 pin 8 insures that the head is loaded during the Write or Trim Erase mode. When the Disk is enabled, a LOW on the Clear line is present at F1 pin 8. When $\overline{DO3}$ is LOW, H1 pin 1 is enabled HIGH. This leaves F1 pin 10 LOW, clearing Head Load Flip-Flop F2 pin 13. The Write Trim Erase Gate is enabled LOW and inverted HIGH to E1 pin 1, and the Head Load Flip-Flop, F2 pin 12, is cleared HIGH and appears at E1 pin 2. E1 pin 3 is enabled LOW and inverted by line driver J2 pin 13. A HIGH at J2 pin 13 removes the head from the Disk surface. The head may be unloaded immediately after Write Enable.

4 THEORY OF OPERATION

4-17 INTERRUPT OUTPUT

This section describes the handling of Interrupt Outputs.

When $\overline{DO4}$ goes LOW, J1 pin 13 (Disk Board #2, Sheet 2) is enabled for 500 nanoseconds, applying a clock pulse to Sector Interrupt Enable Flip-Flop E2. E2 pin 12 is enabled HIGH and present at Sector Interrupt Latch E4. E4 pin 12 is normally HIGH in a Reset condition. The Reset Interrupt Latch Gate, E3 pin 11, is normally HIGH and applied to E4 pin 1 when an interrupt is acknowledged by the computer's Central Processing Unit (CPU). When START OF SECTOR CLR goes LOW for 500 ($\pm$250) nanoseconds, E4 pin 12 is latched LOW providing the Disk Drive Interrupt signal. When PDBIN and SINTA go HIGH for 500 nanoseconds and 1.5 microseconds respectively, E3 pin 11 goes LOW and E4 pin 12 is reset HIGH. Flip-Flop E2 pin 12 is cleared LOW when J1 pin 1 goes HIGH for 500 nanoseconds. E1 pin 6 is HIGH and inverted LOW at H4 pin 2, clearing Flip-Flop E2. Software must enable interrupts in the CPU and have an appropriate service routine in memory to enable the Interrupt signal.

4-18 HEAD CURRENT

This section describes the Head Current Circuit.

When $\overline{D06}$ is LOW, J1 pin 4 (Disk Board #2, Sheet 2) goes HIGH for 500 nanoseconds, clocking Head Current Switch Flip-Flop F2. F2 pin 9 goes HIGH, and is inverted LOW by line driver J2 pin 7, producing the Disk Drive Head Current (HD CURR) signal. HD CURR must be enabled when outputting a Write instruction with the head on tracks 43 through 76. This reduces head current and optimizes resolution on inner tracks.

START OF SECTOR CLR is HIGH at inverter B4 pin 9 and Sector Interrupt Latch E3 pin 9. B4 pin 8 inverts SECTOR CLR LOW at F1 pin 12. F1 pin 13 is enabled HIGH by a LOW at F1 pin 11 on the CLEAR line. When START OF SECTOR CLR goes LOW for 500 (±250) nanoseconds, F1 pin 13 is LOW, clearing Head Current Switch Flip-Flop and Write Enable Flip-Flop E2.

4-19 WRITE ENABLE AND TRIM ERASE

This section describes the Write Enable and Trim Erase Circuits.

When $\overline{DO7}$ is LOW, J1 pin 10 is enabled HIGH, clocking Write Enable Flip-Flop E2 (Disk Board #2, Sheet 2). E2 pin 9 is HIGH for 5.2 milliseconds, and is present at B2 pin 9 and J4 pin 12, and supplies the WRT ENABLE (Write Enable) signal to latch E3 pin 1 (Disk Board #2, Sheet 1) and is inverted LOW by J2 pin 11 to provide the Disk Drive Write Enable (WRT EN) signal. When LOW, WRT ENABLE clears the Counters and Shift Registers H2, A3, and A4 (Disk Board #2, Sheet 1).

E2 pin 8 is LOW and present at B2 pin 1. This allows the Trim Erase Start Delay One-Shot, B2 pin 13, to go HIGH for 200 microseconds. When E2 pin 9 is HIGH, Trim Erase End Delay One-Shot B2 pin 5 is LOW. After 200 microseconds, B2 pin 13 returns LOW, enabling F4 pin 10 HIGH. The Trim Erase Flip-Flop, J4 pin 9, is HIGH for 5.4 milliseconds, and, inverted by J2 pin 9, produces the Disk Drive Trim Erase (TRIM ER) signal. When E2 pin 9 returns LOW, Trim Erase End Delay One-Shot B2 pin 5 is HIGH for 475 microseconds, disabling F4. When B2 pin 5 returns LOW, F4 pin 10 is enabled HIGH and clocks J4 pin 11. This allows J4 pin 9 to go LOW, disabling TRIM ER. With E1 pins 9 and 10 both HIGH, E1 pin 8 is enabled LOW and inverted by B4 pin 4 to Move Head Status Gate E4 and to E1 pin 1. The Write Enable Flip-Flop is cleared at the end of every Sector by the Start of Sector Clear pulse (described in Section 3-18).

4 THEORY OF OPERATION

4-20 DISK DRIVE UNIT

This section describes the Disk Drive Unit.

The Disk Drive Unit stores data on a magnetic disk in the same manner that a tape recorder records sound. The heart of the Disk Drive Unit is the PERTEC FD-510 Floppy Disk Drive which includes the mechanism plus the Read/ Write Circuitry. The Disk Buffer printed circuit card and the Power Supply make up the remainder of the electronics in the Disk Drive Unit.

The Disk Buffer printed circuit card acts as a line receiver and line driver for interfacing between the Disk Controller in the Computer, the FD-510 and other Disk Drive Units in multiple Drive systems. The Disk Buffer printed circuit card also contains the Disk Enable and Address Circuitry. The Power Supply has three regulated outputs; +24 volts for the Disk Drive motor, -12 volts for the Disk Drive Read Circuit, +5 volts for Disk Drive logic and the Disk Buffer printed circuit card.

4 THEORY OF OPERATION

4-21 DISK BUFFER

This section describes the Disk Buffer.

The Disk Buffer printed circuit card consists of two sections: tri-state 8T97 line drivers with line terminator resistors on their inputs, and address and enable circuitry to select the Disk Drive.

All logic signals are LOW when enabled (True) and HIGH when disabled (False). A LOW signal is 0v to -.8v and a HIGH signal is approximately 3v. Timer U3 inhibits Disk Drive selection by remaining LOW at U2 pin 1 for five seconds, allowing the Drive motor to achieve stable speed after the door is closed or the power is turned on. When the door is closed, U3 pins 3 and 4 go HIGH with U3 pin 6 remaining LOW for 5 seconds before going HIGH at U2 pin 1. U2 pin 8 is enabled LOW when the correct Disk address is selected, allowing U2 pins 2, 3, 4 and 5 to go HIGH. A LOW at U2 pin 8 allows inverting line drivers U1 to be enabled when the DISK ENABLE line ($\overline{DE}$) is LOW at U1 pin 14. This enables line drivers U5 and U7, allowing all signals to and from the Disk Controller to interact with the Disk Drive selected. Line drivers U4 and U6 are enabled only when there is an expansion unit plugged in.

4 THEORY OF OPERATION

4-22 DISK DRIVE ADDRESSING

This section shows how to assign an address to a Disk Drive Unit.

Although Disk Drives may be interconnected in any order in a multiple Drive system, the highest Disk address utilized must be one less than the number of Disk Drives in the system. All Disk Drive addresses that are used must be unique. For example, in a system implementing three Disk Drives, addresses 0, 1 and 2 are utilized.

The chart below shows the switch positions on the Disk Buffer for a given Disk Drive address.

DRIVE NO.	DISK BUFFER SWITCH 1			
	[4]	[3]	[2]	[1]
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

1 = ON
0 = OFF

4 THEORY OF OPERATION

4-23 ADAPTER CARD

This section describes the Adapter Card.

The adapter card contains an edge connector that plugs directly into the Disk Drive. It re-routes the drive signals to and from the Disk Buffer board (connector P3) that pass to the Adapter Card via a flat cable.

5 DISK DRIVE SPECIFICATIONS

5-1 PHYSICAL DESCRIPTION

Various physical parameters pertaining to the Diskette are listed below.

Tracks per inch:	48
Total number of tracks:	77
Inside track radius:	2.029" (51.6 mm)
Disk rotational speed:	360 RPM
Rotational direction (recording side):	counter-clockwise (CCW)
Read/Write track width:	0.012" (0.31 mm)

5 DISK DRIVE SPECIFICATIONS

5-2 RECORDING PARAMETERS

The following recording parameters of the FD-510 are designed to be user-controlled.

Data Transfer Rate:	250K Bits/Sec
Recording Density:	6,632 Bits/Radian (3248 BPI Inside Track)
Maximum Bits/Track:	41665 (Unformatted)
Maximum Bits/Disk:	3.2×10^6 (Unformatted)

The recording mode is frequency modulation (double frequency recording).

5 DISK DRIVE SPECIFICATIONS

5-3 PERFORMANCE CHARACTERISTICS

Pertinent performance characteristics for the FD-510 Disk Drive are listed on these pages.

Rotational Speed	360 RPM ± 1.5%
Rotational Direction	CCW viewed from recording side
Average latency	83.3 milliseconds
Start-up time	2 seconds (max)
Stop time	2 seconds (max)
Access Times	
Track-to-track	10 milliseconds (minimum seek time)
Head settling time	20 milliseconds (at last track addressed)
Head loading time	40 milliseconds (max)
Recording Characteristics	The method of recording is frequency modulation with a data rate of 250,000 bits per second.
Error Rate	The FD-510 is designed to reliably read and record data when operated within the specified conditions. The error rates, exclusive of external sources such as the user's electronics and Disk defects and contaminates, are a maximum of: 1 recoverable error per 10^9 bits 1 non-recoverable error per 10^{12} bits A recoverable error is an error that does not persist after 10 rereads and one reseek is performed.
Interference	The FD-510 is designed so that the amount of interference inherently generated and propagated through space or over associated conductors is minimized and does not interfere with the information transmitted to or received from the system. Filtering, shielding and bonding conform to good engineering practices.

Disk and Head Life

The head is capable of satisfactory (Head-to-Disk-contact) performance for 40,000 hours under normal operating conditions. Head life is considered to end when the head causes the specified machine error rates to be exceeded.

Disk wear, as a function of Head-to-Disk contact, results in a minimum Disk life of one million passes per track.

In normal application, assuming an even distribution of track usage, the Disk will last a minimum of one year. The normal life under these conditions is five years.

5 DISK DRIVE SPECIFICATIONS

5-4 PHYSICAL SPECIFICATIONS

Pertinent physical specifications of the disk drive are given below.

Magnetic Head Assembly

The magnetic head assembly consists of a lead screw driven carriage containing a pressure-pad loading device and an R/W magnetic head with a Trim Erase.

Environmental Conditions

The environmental specification for the media used in the Diskette unit will determine the temperature and humidity requirement at the site where the Diskette unit is installed. The Diskette units, however, are designed to meet the following specifications:

Temperature

Operating: +50°F (10°C) to 110°F (42°C) with a maximum gradient of 0.2°F per minute to be operated after 1 hour in ambient environment.

Non-Operating: 0°F (-18°C) to +125°F (+46°C).

Relative Humidity

Operating: 20-80%

Non-Operating: 5-95% (without condensation).

5 DISK DRIVE SPECIFICATIONS

5-5 POWER REQUIREMENTS

This section gives the primary power requirements for each FD-510 Disk Drive.

Primary power requirements:

+24v DC ± 1 volt	1.4 amperes (avg.)*
+5v DC ± .24 volt	1.1 amperes (max) 100 mv ripple
-5v DC ± .25 volt	0.3 amperes (max) 100 mv ripple

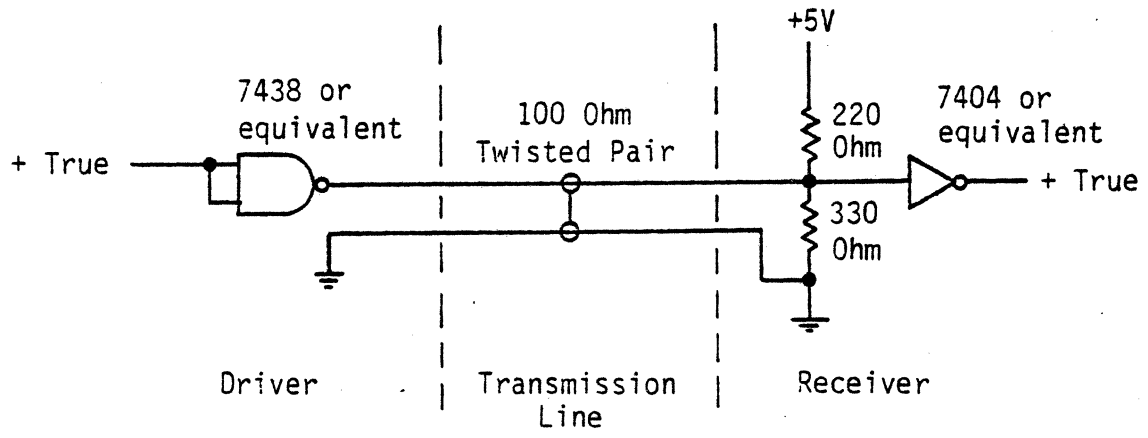
*The current load on the 24v DC line is pulsating in nature (approximating a sawtooth imposed on a steady state current of 0.5 ampere). Maximum current for Drive motor start is 6 amps, peak, for approximately 10 milliseconds, then 4 amps, peak; decreasing to 3 amps, peak after 500 milliseconds. The Drive functions to specification if the current is limited to 2 amperes at the supply.

5 DISK DRIVE SPECIFICATIONS

5-6 INTERFACE LEVELS

This section gives basic interfacing information for logic signals for the FD-510.

All interface signals are TTL compatible (see figure below). Logic True is at +0.2v (±0.2), logic False is +3.0v (+2.3 - 0.6). Interfacing cable is required to be 100 ohm twisted pair or equivalent with a maximum length of 15 feet.



Interface Configuration (Typical)

5 DISK DRIVE SPECIFICATIONS

5-7 INTERFACE PIN ASSIGNMENTS

This table gives the standard pin assignments for the FD-510 input, output, data and power signals.

	Signal	Logic	Ground
Input Control	STEP IN	11	M
	STEP OUT	15	S
	DRIVE MOTOR ON	18	V
	HEAD LOAD	16	T
	HEAD CURRENT SWITCH	7	H
	WRITE ENABLE	9	K
	TRIM ERASE	8	J
	DOOR LOCK ENABLE	2	4
Output Status	TRACK 0	19	W
	INDEX	17	U
	DOOR OPEN	6	F
	WRITE PROTECT	13	P
Data	WRITE DATA INPUT	10	L
	READ DATA OUTPUT	20	X
Power	+24V DC	A, B	D, E
	+5V DC	21	Y
	-5V DC	22	Z

Notes: 1. Drive Frame must be connected to Earth ground.

2. Disk Drive Interface Connector Amp No. 582777-1.

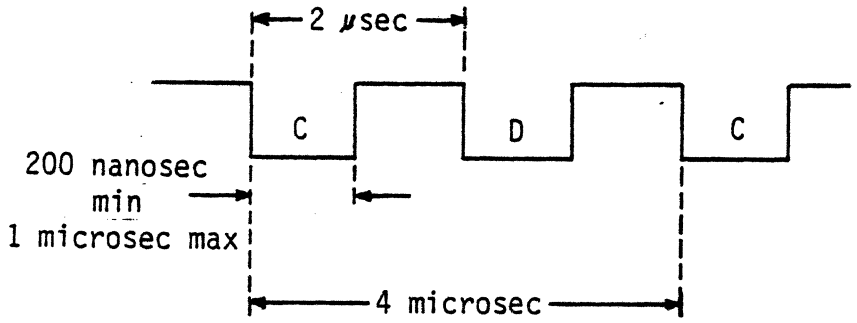
5 DISK DRIVE SPECIFICATIONS

5-8 DATA LINES

This section describes the Write Data Input and Read Data Output signals.

WRITE DATA INPUT

Serial data in double frequency mode is applied to this line for file writing in conjunction with the activation of WRITE ENABLE. Nominal data and clock should be at rates shown in figure below. The tolerance applied to these rates is primarily a function of the users method of data separation and format; however, a normal tolerance to apply to these times is ± .5%. The drive will operate satisfactorily over a ± 10% frequency range.

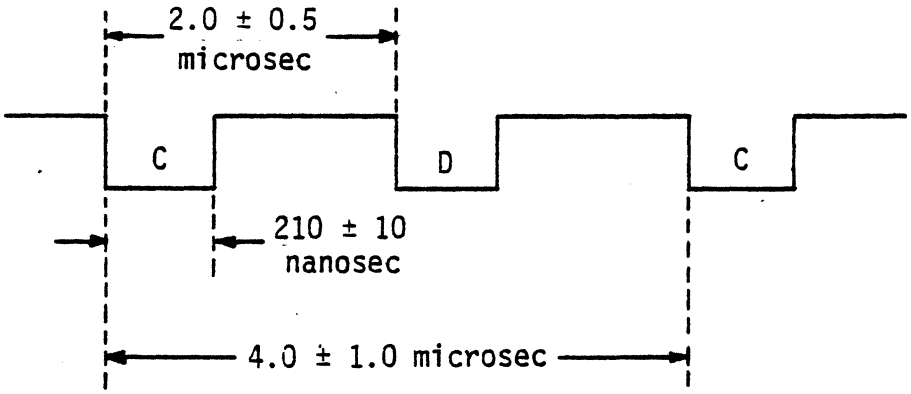


WRITE DATA INPUT Signal

READ DATA OUTPUT

The READ DATA OUTPUT line is not gated separately in the Drive electronics. When the Drive is selected, various types of signals will be present on this line, depending upon the operation being performed.

During a legitimate Read operation of a signal written at the nominal timings shown for the WRITE DATA INPUT signal, the READ DATA OUTPUT line will appear as shown below.



READ DATA OUTPUT Signal

5-9 INPUT CONTROL SIGNALS

This section describes the input control signals.

STEP IN AND STEP OUT

The head is displaced one track increment for each pulse received. A pulse on the STEP IN line moves the head to a higher order track (toward the center of the Disk) and a STEP OUT pulse moves the head to a lower order track. Both lines are to be held False when no head movement is desired.

A True pulse with a time duration of from 200 nanoseconds to 2 milliseconds causes a one step movement of the head. The pulse repetition rate must be between 10 and 11 milliseconds or greater than 30 milliseconds. When changing direction of head movement (e.g., from STEP IN to STEP OUT), delay equal to the normal head settling time must be provided.

DRIVE MOTOR ON

The Disk Drive motor starts and continues to run as long as this line is held True. The motor is up to speed and stabilized within 5 seconds.

HEAD LOAD

The HEAD LOAD solenoid energizes and remains energized as long as this line is held True. The solenoid energizes within 20 milliseconds and the Read signal is stabilized within 40 milliseconds.

HEAD CURRENT SWITCH

When writing on tracks 43 through 76, the Head Current line must be True to reduce Write current. This reduction of Write current maintains resolution integrity necessary for IBM compatibility.

WRITE ENABLE

This line enables the Write current driver to respond to input write data. WRITE ENABLE must be True only during the writing period to prevent loss of pre-recorded data.

TRIM ERASE

A True level on this line causes the recorded track (and in most cases on the adjacent track) to be erased on its edges. To assure trimming of newly recorded data, this line should be activated with timings sufficient to allow for a .032 ± .003 inch (0.82 ± .076 mm) spacing between the Read/Write and TRIM ERASE gaps.

DOOR LOCK ENABLE

The door lock function is not implemented, however, this signal does exist. A True level on this line lights the indicator locted on the FD-510 door.

5 DISK DRIVE SPECIFICATIONS

5-10 OUTPUT STATUS SIGNALS

This section describes the output status signals.

TRACK 0

The level on this line is True when the head is positioned at Track 0. It goes True approximately 20 milliseconds after the last STEP OUT command, i.e., step from track 1 to track 0. Any STEP OUT command is ignored by the Drive electronics 9 milliseconds after receiving the last command that resulted in the head being positioned at Track 0.

INDEX and SECTOR

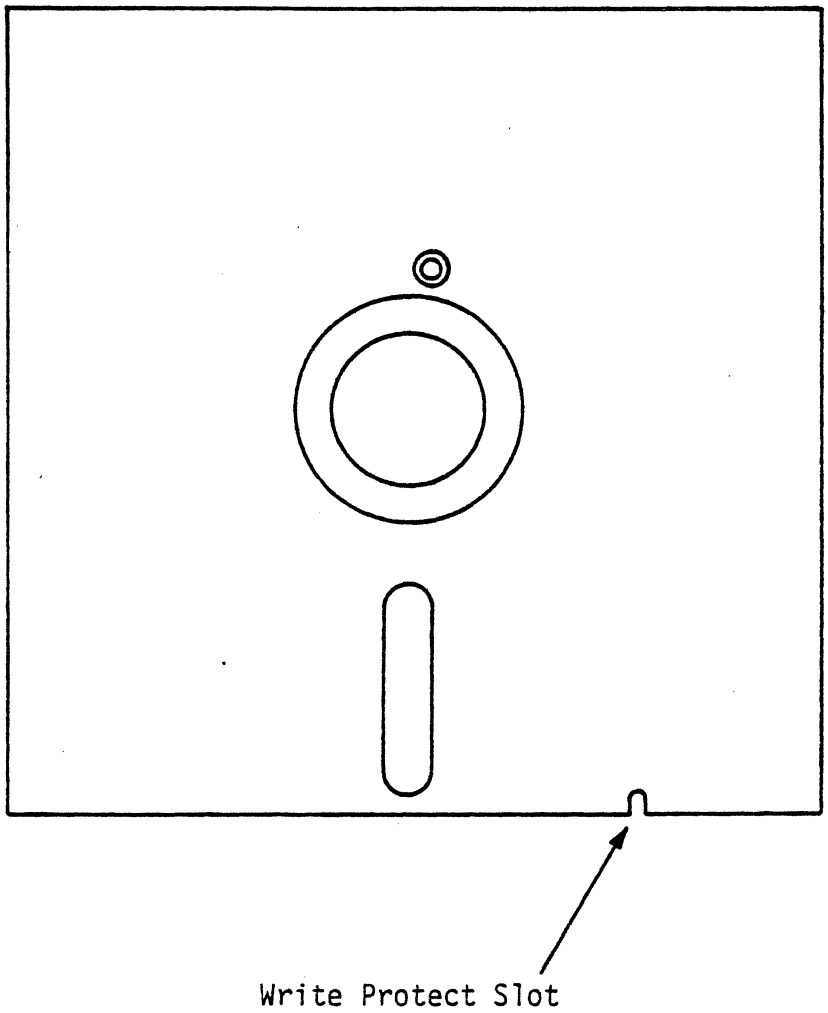
The pulse on this line indicates that the Index and Sector holes have been detected. The duration of the pulse is a function of the Disk cartridge Index hole size (typically 1.8 milliseconds). The INDEX pulse occurs once every revolution or once every 166.7 milliseconds and is located between the 32nd and the first Sectors. A pulse also occurs once every Sector (every 5.2 milliseconds).

DOOR OPEN

The DOOR OPEN line is True whenever the Disk Drive door is open. The Head Load solenoid and the Drive motor are de-energized when the door is opened and re-energized when the door is closed.

WRITE PROTECT

The write electronics are disabled if the write protect slot (see figure on the facing page) is uncovered on the diskette jacket. This signal also lights an indicator on the front panel when a diskette is write-protected.


Write Protect Slot

5 DISK DRIVE SPECIFICATIONS

5-11 SERVICEABILITY AND REPAIRABILITY

The service life, mean time between failures, and mean time to repair for the FD-510 are given in this section.

SERVICE LIFE

The Pertec FD-510 has a minimum useful life of five years or 10,000 operating hours, whichever occurs first, before the unit requires replacement or a major overhaul.

MEAN TIME BETWEEN FAILURE (MTBF)

MTBF exceeds 4000 hours. The following expression defines MTBF:

$$\text{MTBF:} \quad \frac{\text{Operating Hours}}{\text{Number of Equipment Failures}}$$

Operating hours are defined as the total power-on-hours. Equipment failures are defined as any stoppage or substandard performance of the equipment because of equipment malfunction. This excludes stoppages or substandard performance caused by operator error, adverse environmental conditions, power supply failure, controller failure, cable failure or other failure not caused by the equipment. To establish a meaningful MTBF, operating hours must be greater than 2000 hours and must include a minimum population of 1000.

MEAN TIME TO REPAIR (MTTR)

The MTTR does not exceed .5 hours. Mean-Time-to-Repair is defined as the time for an adequately trained repair person to diagnose and correct a malfunction.

6 ALIGNMENT

6-1 INTRODUCTION

This section describes the mechanical and electrical alignment procedures for the Floppy Disk System.

Maintaining proper alignment of the Disk Drive is essential for trouble free operation of the Floppy Disk System. The alignment involves the adjustment of the Index pulse timing and head positioning (track and skew). Necessary equipment includes an oscilloscope with an A + B (differential), a CE Alignment Diskette (available through MITS, part number 101661), a 1/4" nut driver, screwdrivers, and a mallet.

6 ALIGNMENT

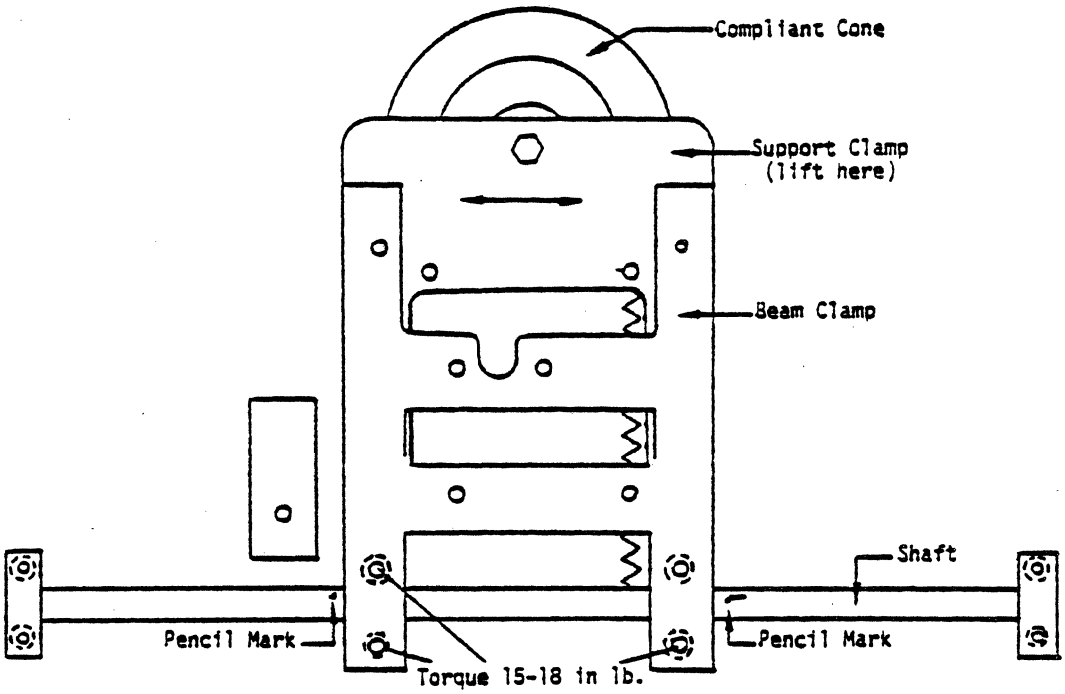
6-2 MECHANICAL ALIGNMENT

This section describes the mechanical alignment of the cone clamping mechanism.

An important part of the alignment is the adjustment of the cone clamping mechanism for the FD-510 Drive (refer to the figure on the facing page). If the clamping force is low enough to allow the Diskette to slip, the oxide around the center hole may be scraped off the Diskette and may build up on the cone. This loose oxide could contaminate the load pad, causing excessive wear to both pad and media. (Slight scratching of the Diskette at the cone clamping area is normal.)

To adjust the cone clamping mechanism, close clamping mechanism and door, and loosen the four screws (7/64 allen bit) that are holding the beam clamp to the shaft. Press firmly on the support clamp and move the beam clamp to the extreme right and left. Make a pencil mark on both ends of the shaft. Center the beam clamp between the two pencil marks. Exact centering of the beam clamp is essential for free motor spin.

While pressing firmly on both sides of the beam clamp, open the door approximately 5/8" and tighten screws progressively. With the door closed, rest one finger lightly on both the support clamp and on the compliant cone. Use a force gauge to pull upward on the end of the support clamp until you detect a slight relative motion between the cone and clamp. The clamping force should be 6 1/2 to 9 pounds. Make the proper adjustments until the correct clamping force is obtained.



Cone Clamping Mechanism Adjustment

6-3 ELECTRICAL ALIGNMENT INFORMATION

This section gives preliminary information for the electrical alignment procedures which follow.

There are two different Disk Buffer Boards used in the PERTEC FD-510, the 600-191 and 600-321. These numbers are stamped on the board. Set up your scope for A + B with B inverted and for external sync. Place the Disk Drive unit on its side and attach the scope probes as shown.

Test Connections

Probes	600-191	600-321
A and B probes	TP-3 and 5	TP-4 and 5
Sync probe (leading edge of index pulse)	TP-14	TP-10
Ground clip	TP-36	TP-1

Program 4-V (on the facing page) permits loading and stepping of the head to the desired track under sense switch control. Load Program 4-V* into memory, examine the starting location and run. A15 will load and unload the head while A8 through A14 will control the step functions.

* The Disk Exerciser Program (Program 4-V) was written by Steven Zook of the Computer Store in Santa Monica, California.

Program 4-V - Disk Exerciser Program

Address	Code	Mnemonic	Address	Code	Mnemonic
000	333	IN (CHANNEL)	055	076	MVI A,/010
001	377		056	010	
002	346	ANI (DATA)	057	323	OUT (CHANNEL)
003	017		060	011	
004	127	MOV D, A	061	333	IN (CHANNEL)
005	172	MOV A, D	062	010	
006	323	OUT (CHANNEL)	063	074	INR A
007	010		064	312	JZ/000005
010	333		065	005	
011	010		066	000	
012	074	INR A	067	075	DCR A
013	312	JZ/000005	070	346	ANI (DATA)
014	005		071	002	
015	000		072	302	JNZ/000061
016	333	IN (CHANNEL)	073	061	
017	010		074	000	
020	346	ANI (DATA)	075	171	MOV A, C
021	002		076	376	CPI (DATA)
022	302	JNZ/000016	077	115	
023	016		100	322	JNC/000042
024	000		101	042	
025	076	MVI A,/002	102	000	
026	002		103	270	CMP B
027	323	OUT (CHANNEL)	104	312	JZ/000042
030	011		105	042	
031	333	IN (CHANNEL)	106	000	
032	010		107	332	JC/000122
033	346	ANI (DATA	110	122	
034	100		111	000	
035	302	JNZ/000016	112	076	MVI A,/001
036	016		113	001	
037	000		114	323	OUT (CHANNEL)
040	006	MVI B,/000	115	011	
041	000		116	004	INR B
042	333	IN (CHANNEL)	117	303	JMP/000061
043	377		120	061	
044	007	RLC	121	000	
045	267	ORA A	122	076	MVI A,/002
046	037	RAR	123	002	
047	117	MOV C, A	124	323	OUT (CHANNEL)
050	076	MVI A,/004	125	011	
051	004		126	005	DCR B
052	322	JNC/000057	127	303	JMP/000061
053	057		130	061	
054	000		131	000	

6 ALIGNMENT

6-4 ELECTRICAL ALIGNMENT PROCEDURE 1

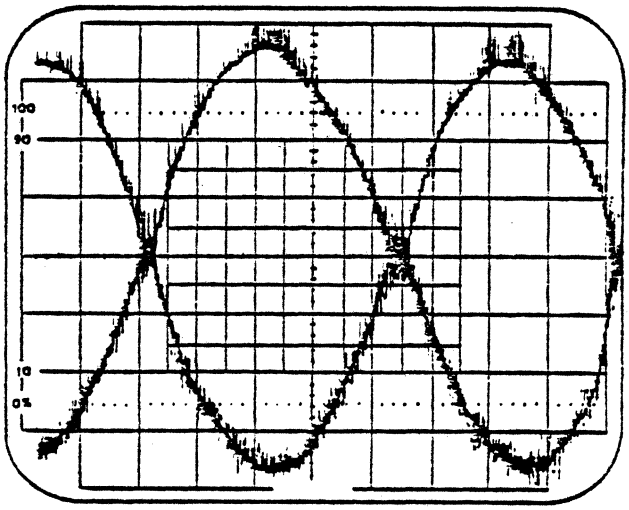
This is the first of two Electrical Alignment Procedures.

Insert the Alignment Diskette and load the magnetic head.

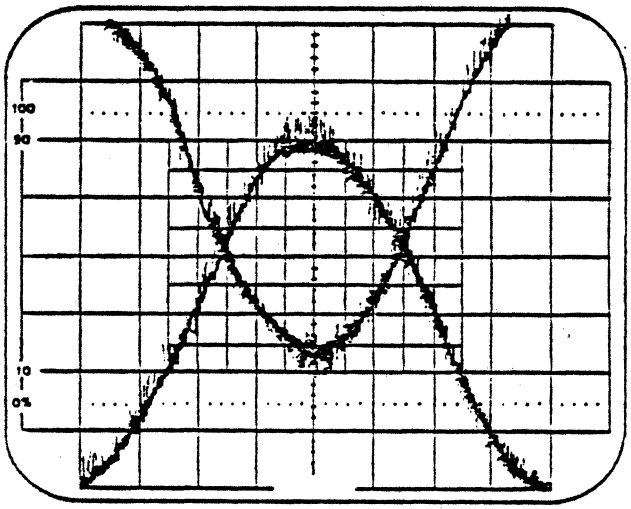
CAUTION

Do not enable the Write or Erase modes of operation while a CE Diskette is in the Drive, because alignment data on the Diskette may be destroyed.

You should now observe the "cats-eye" pattern located at Track 38. The desired waveform should be a symmetrical pattern as shown below.



Proper Alignment



Improper Alignment

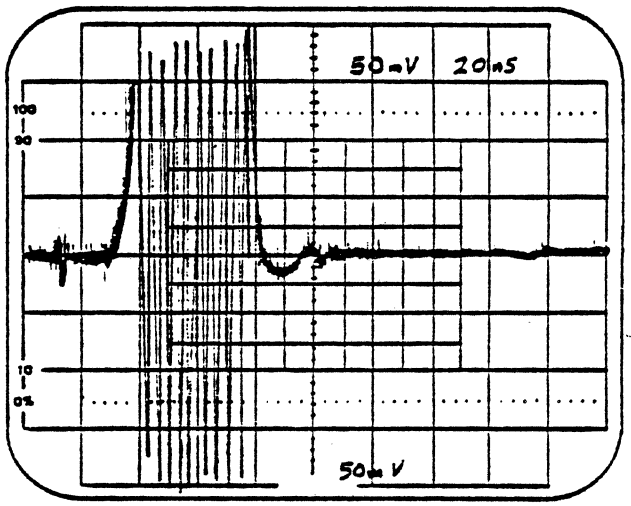
If the waveform is improper, adjust the stepping screw slightly while you observe the scope pattern to see in which direction the head must move to correct the waveform. Loosen the two 1/4" hex head mounting screws on the stepper motor (approximately 1/8 turn). Place a blunt instrument against the end of the stepper motor and tap the motor sharply while observing the cats-eye pattern. When a symmetrical pattern is achieved (one lobe of the cats-eye being 80% of the other, minimum), tighten the mounting screws snugly.

6 ALIGNMENT

6-5 ELECTRICAL ALIGNMENT PROCEDURE 2

Perform this procedure after the Electrical Alignment Procedure 1.

Step to Track 1 and set the scope horizontal time base to 20 microseconds per division. You should now observe the Index/Sensor burst shown below.



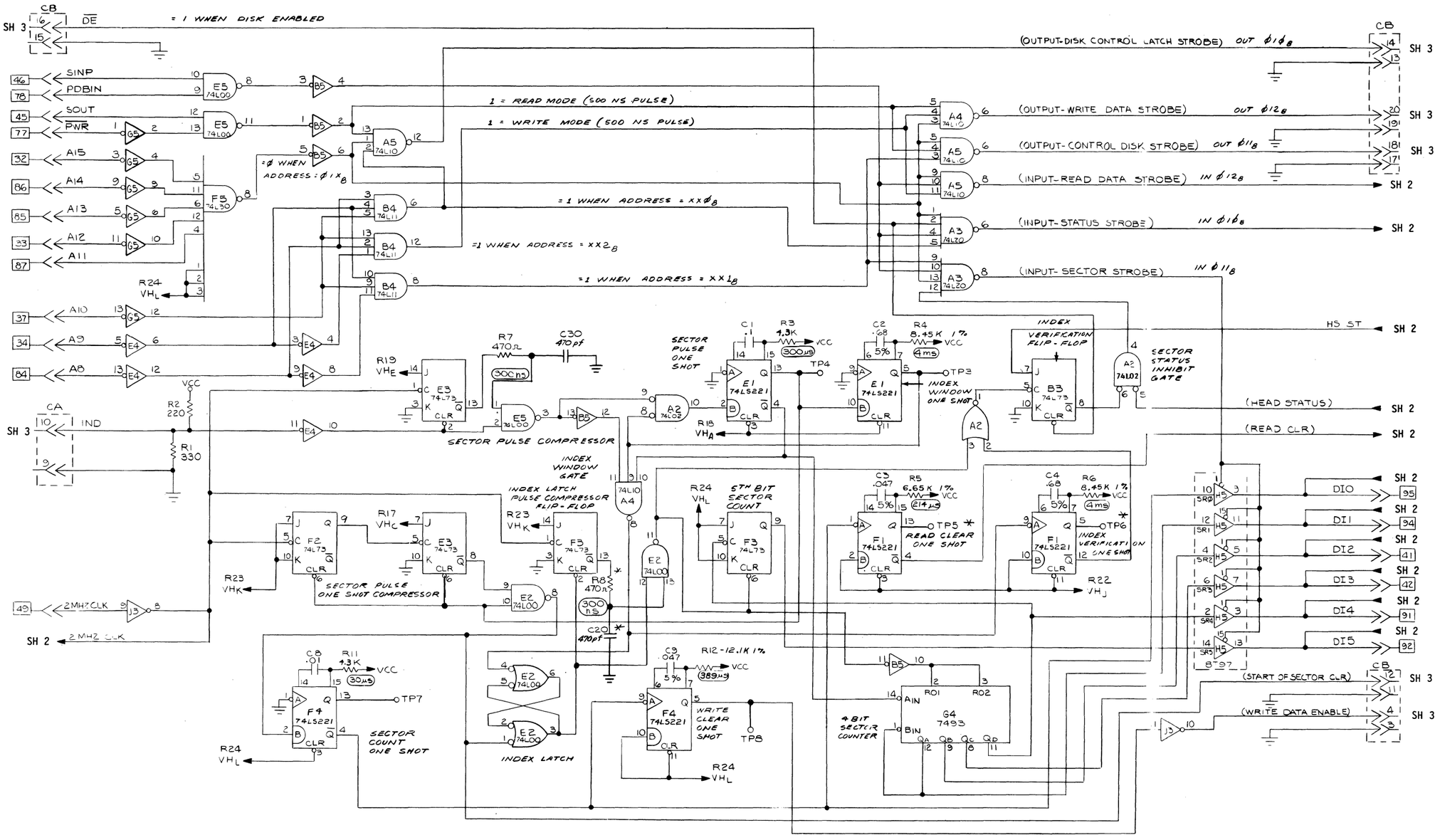
Index/Sensor Burst

Reinsert the Alignment Diskette several times to check for constant registration. If the index burst shifts more than 40 microseconds, the cone/hub mechanism is faulty, or the Alignment Diskette has too large an opening. Use the average position of the index burst for making the following adjustments.

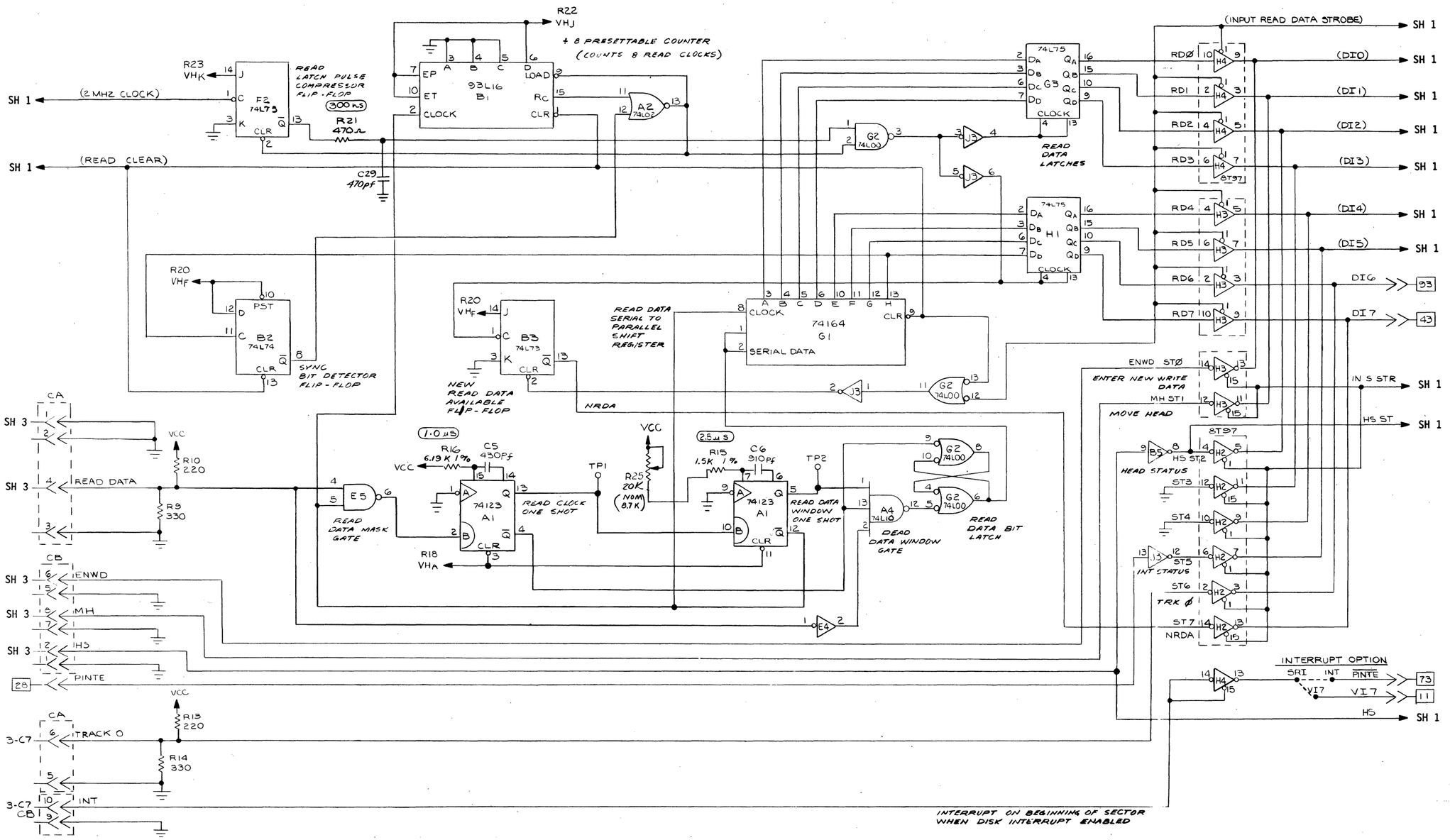
Step to Track 76 and observe the Index/Sensor burst. This burst must be within ± 20 microseconds of each other, position the stepper motor sideways to bring the burst into alignment. To position the stepper motor, insert a flat bladed screwdriver between the stepper motor frame and chassis. The screwdriver may be used as a lever to move the stepper motor in the desired direction.

Return to Track 1 to find out if the bursts are within 20 microseconds of each other. If not, repeat the previous procedure, always moving the bursts at Track 76 to meet the burst at Track 1. Then go back and check the cats-eye and realign it if necessary. Always recheck the cats-eye and bursts when you do any adjustments.

The beginning of the 40 microsecond burst should occur 40 microseconds ± 20 microseconds after the Index pulse. To adjust this pattern, loosen the screws retaining the photo-transistor bracket 1/4 turn and lightly tap the bracket until the proper burst position is obtained. Then retighten the bracket.



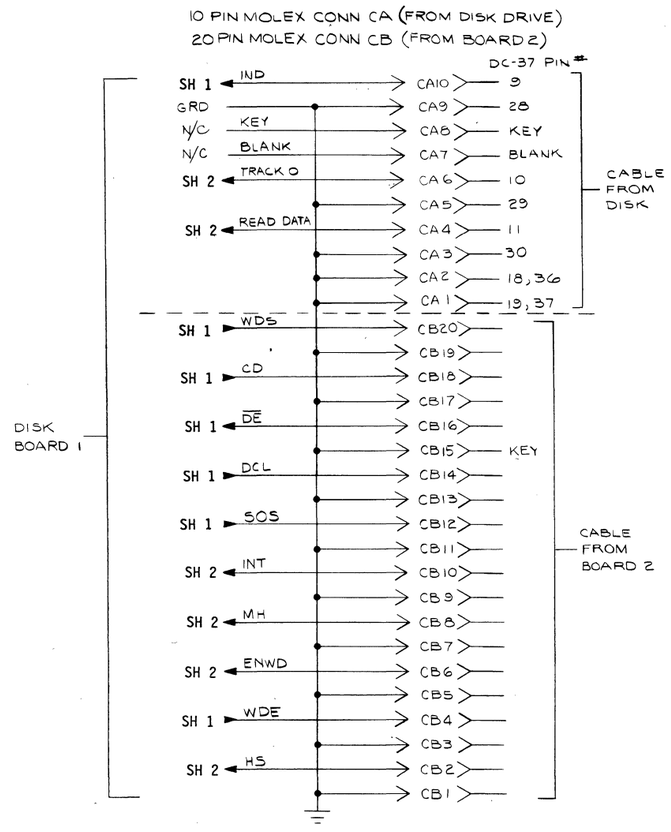
MITS 3200 SCHEMATIC DIAGRAMS
DISK BOARD #1 (Sheet 1 of 3)
ADDRESS/I-O SELECT
& SECTOR CIRCUITS



MITS 3200 SCHEMATIC DIAGRAMS

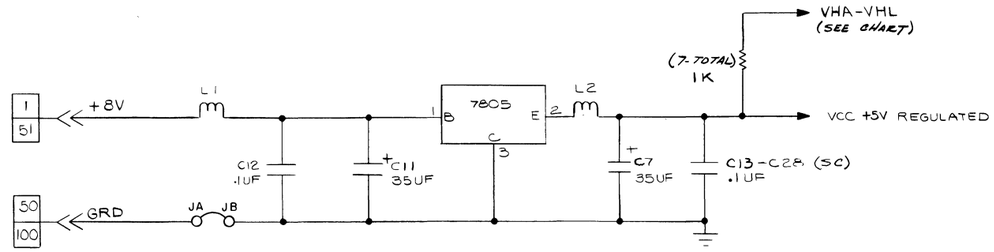
DISK BOARD #1 (Sheet 2 of 3)

READ & STATUS OUTPUT CIRCUITS



NOTES:

1. ALL DIODES IN914 UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS IN OHMS, ½ W UNLESS OTHERWISE SPECIFIED.
3. ALL CAPACITORS IN µF UNLESS OTHERWISE SPECIFIED.
4. (280 µS) NOMINAL TIME CONSTANT.

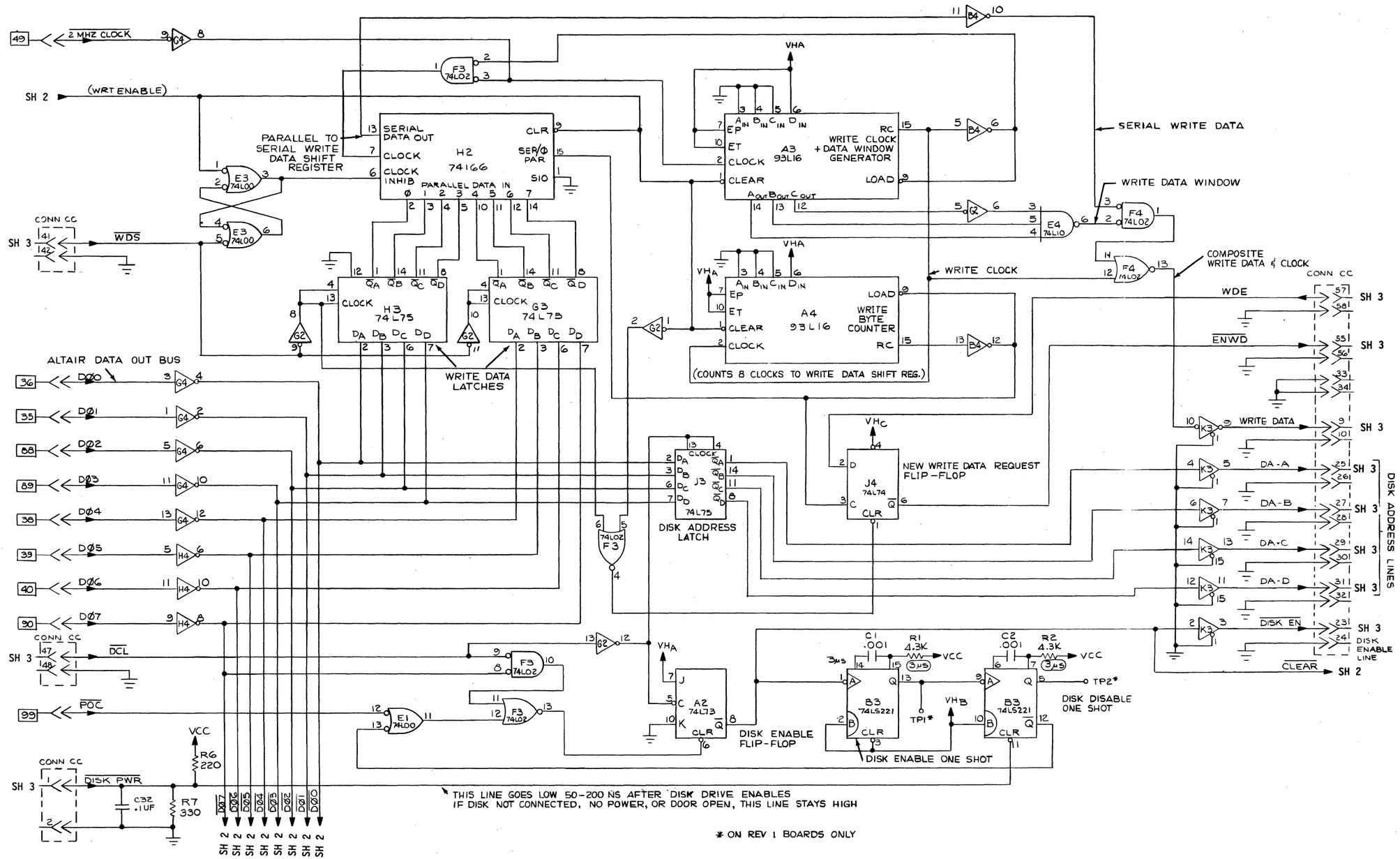


RESISTOR NO	VOLTAGE
R17	VHC
R18	VHA
R19	VHE
R20	VHF
R22	VHJ
R23	VHK
R24	VHL

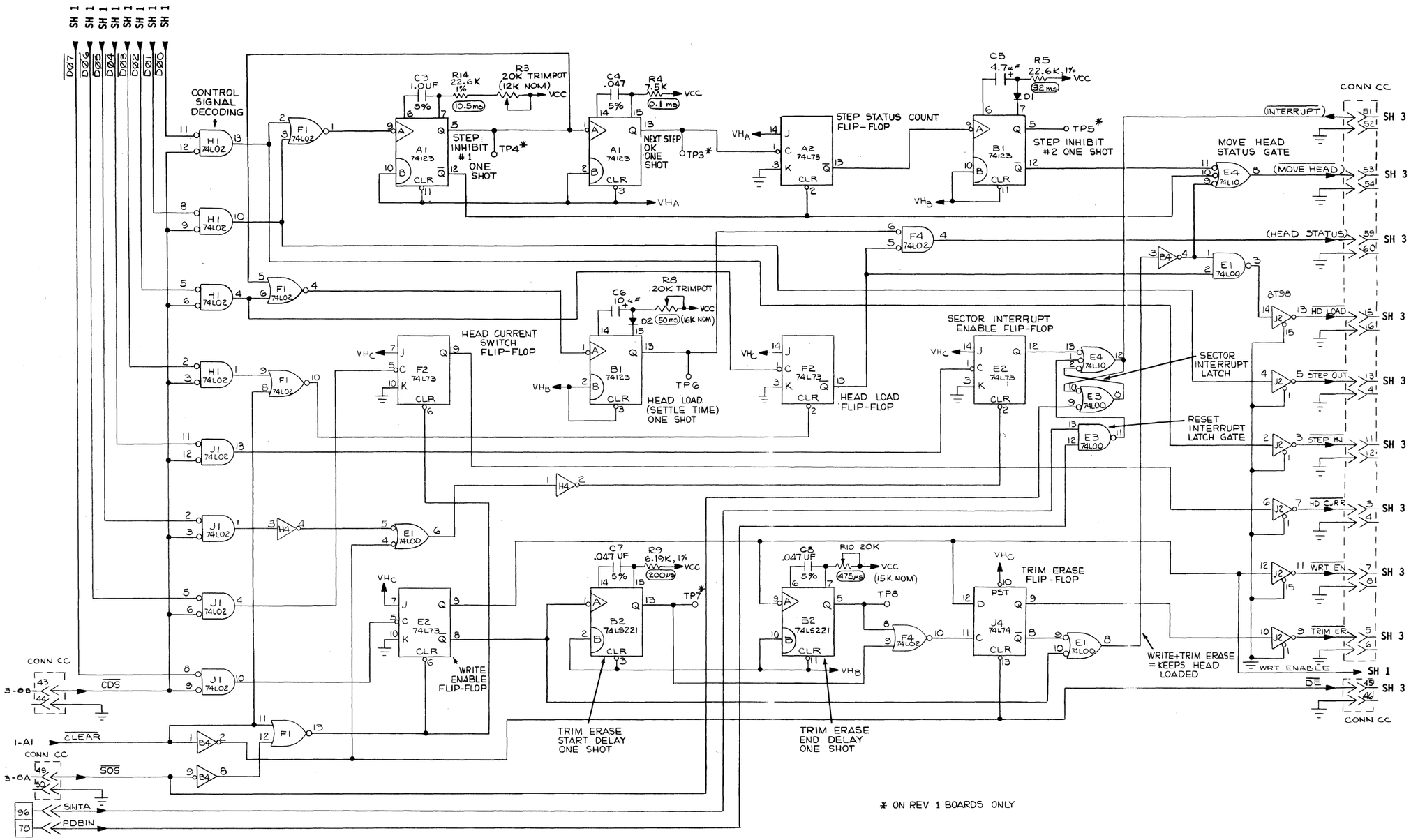
POWER SUPPLY CONNECTIONS

REF/SPARE	TYPE	VCC	GRD	SUBSTITUES
B5,E4,G5,J3	74L04	14	7	74LS04
E2,E5,G2	74L00	14	7	74LS00
B4	74L11	14	7	74LS11
A4, A5	74L10	14	7	74LS10
A3	74L20	14	7	74LS20
F5	74L30	14	7	74LS30
A2	74L02	14	7	74LS02
H2,H3,H4,H5,	8T97	16	8	74367
B3,E3,F2,F3,	74L73	4	11	74LS73
E1, F1, F4	74LS221	16	8	
G4	7493	5	10	74LS93
B1	93L16	16	8	74LS161
B2 ½	74L74	14	7	74LS74
G3, H1	74L75	5	12	74LS75
G1	74164	14	7	74LS164
K1	7805	2	3	
A1	74123	16	8	

MITS 3200 SCHEMATIC DIAGRAMS
DISK BOARD #1 (Sheet 3 of 3)
REGULATION & INTERCONNECTION

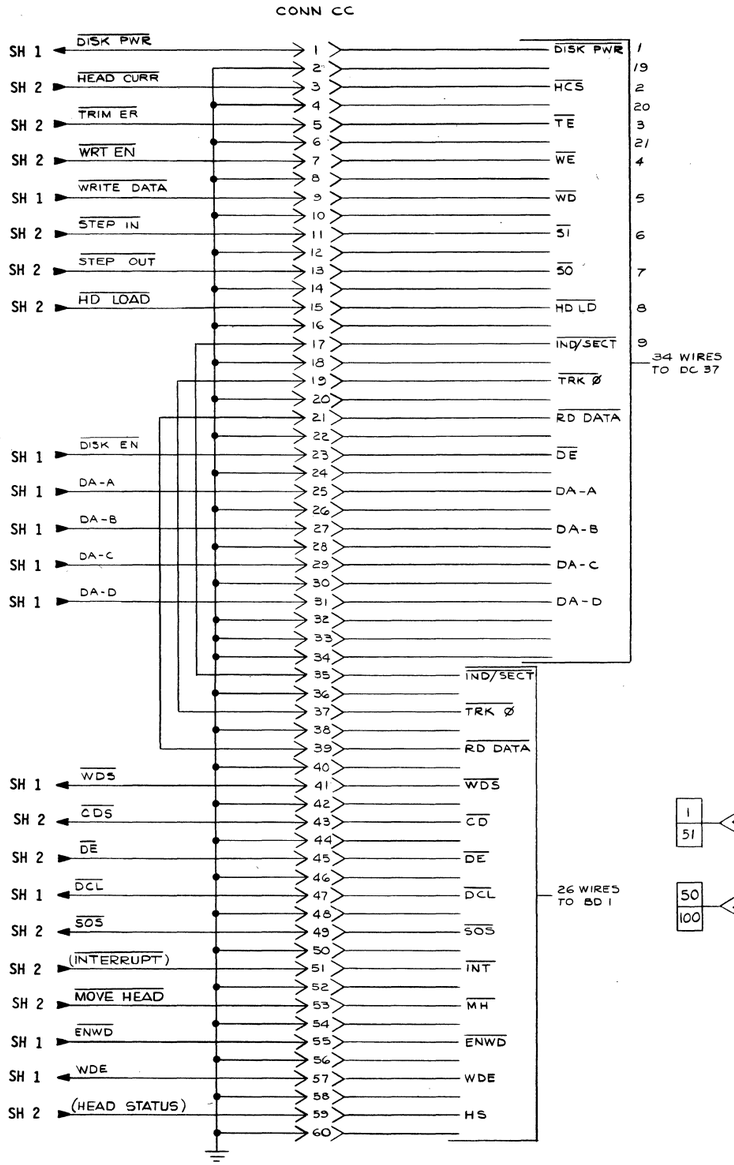


MITS 3200 SCHEMATIC DIAGRAMS
DISK BOARD #2 (Sheet 1 of 3)
WRITE CIRCUIT & DISK LATCHING

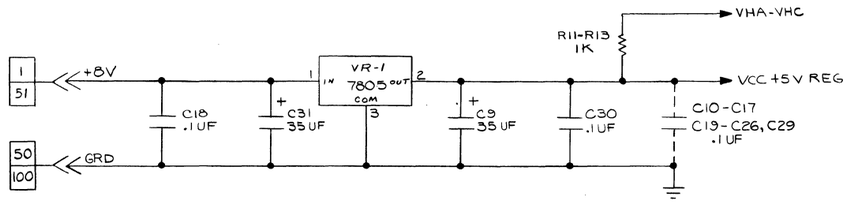


* ON REV 1 BOARDS ONLY

MITS 3200 SCHEMATIC DIAGRAMS
DISK BOARD #2 (Sheet 2 of 3)
DISK CONTROL CIRCUIT

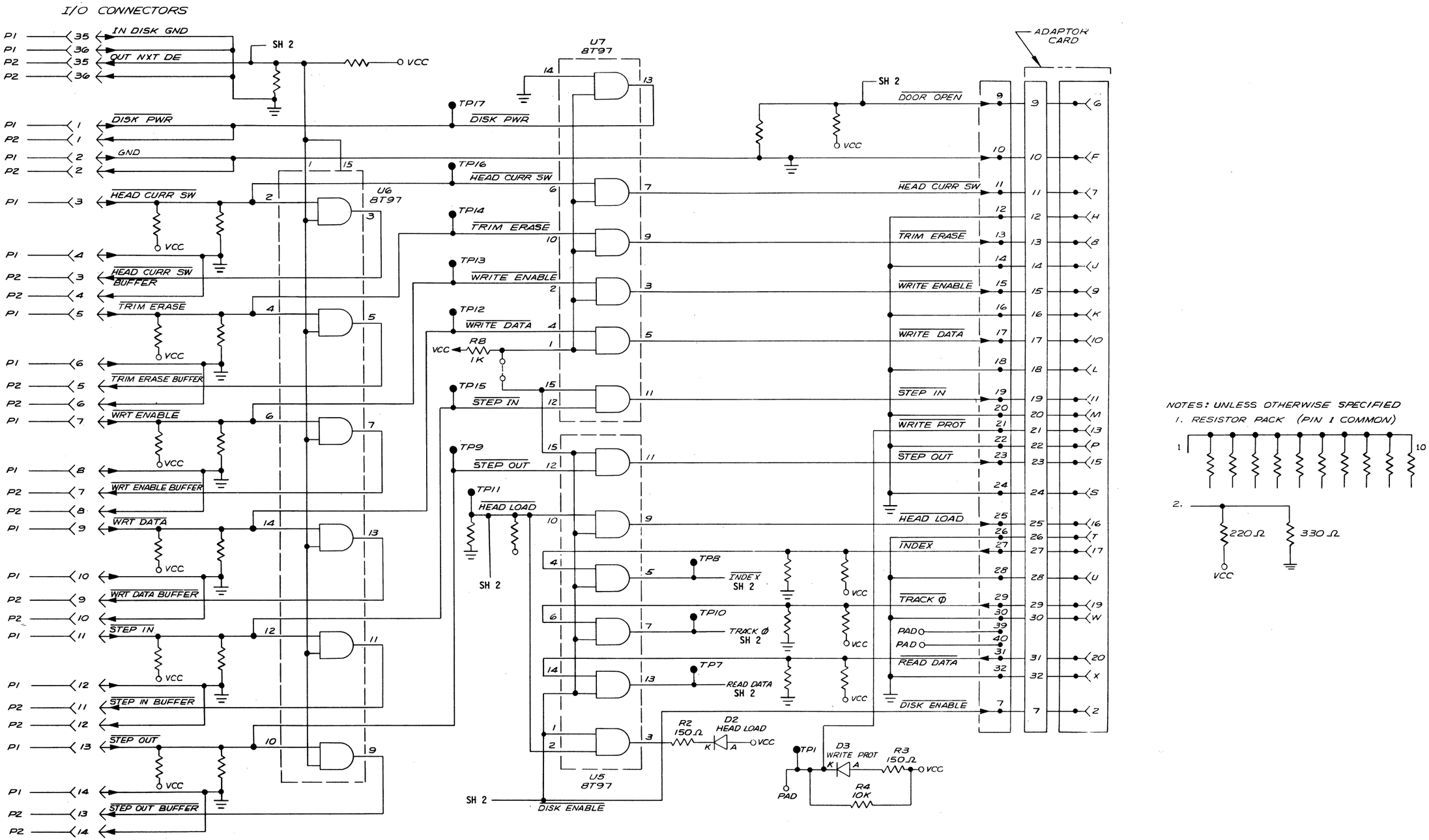


POWER CONNECTIONS				
REF	TYPE	VCC	GRD	SUBSTITUTIONS
F1,F3,F4,H1,J1	74L02	14	7	74LS02
E1,E3	74L00	14	7	74LS00
B4,G2,G4,H4	74L04	14	7	74LS04
J2	8T98	16	8	74LS68
E4	74L10	14	7	74LS10
H2	74166	16	8	74LS166
G3,H3,J3	74L75	5	12	74LS75
A3,A4	93L16	16	8	74LS161
J4	74L74	14	7	74LS74
A2,E2,F2	74L73	4	11	74LS73
A1, B1	74123	16	8	
K3	8T97	16	8	74367
VR-1	7805	2	3	
B2,B3	74LS221	16	8	



NOTES:
1. ALL RESISTORS ½ W UNLESS SPECIFIED.
2. ALL CAPACITORS IN UF.
3. ALL DIODES IN914.
4. (40 ms) NOMINAL TIME CONSTANT.

MITS 3200 SCHEMATIC DIAGRAMS
DISK BOARD #2 (Sheet 3 of 3)
REGULATION & INTERCONNECTION

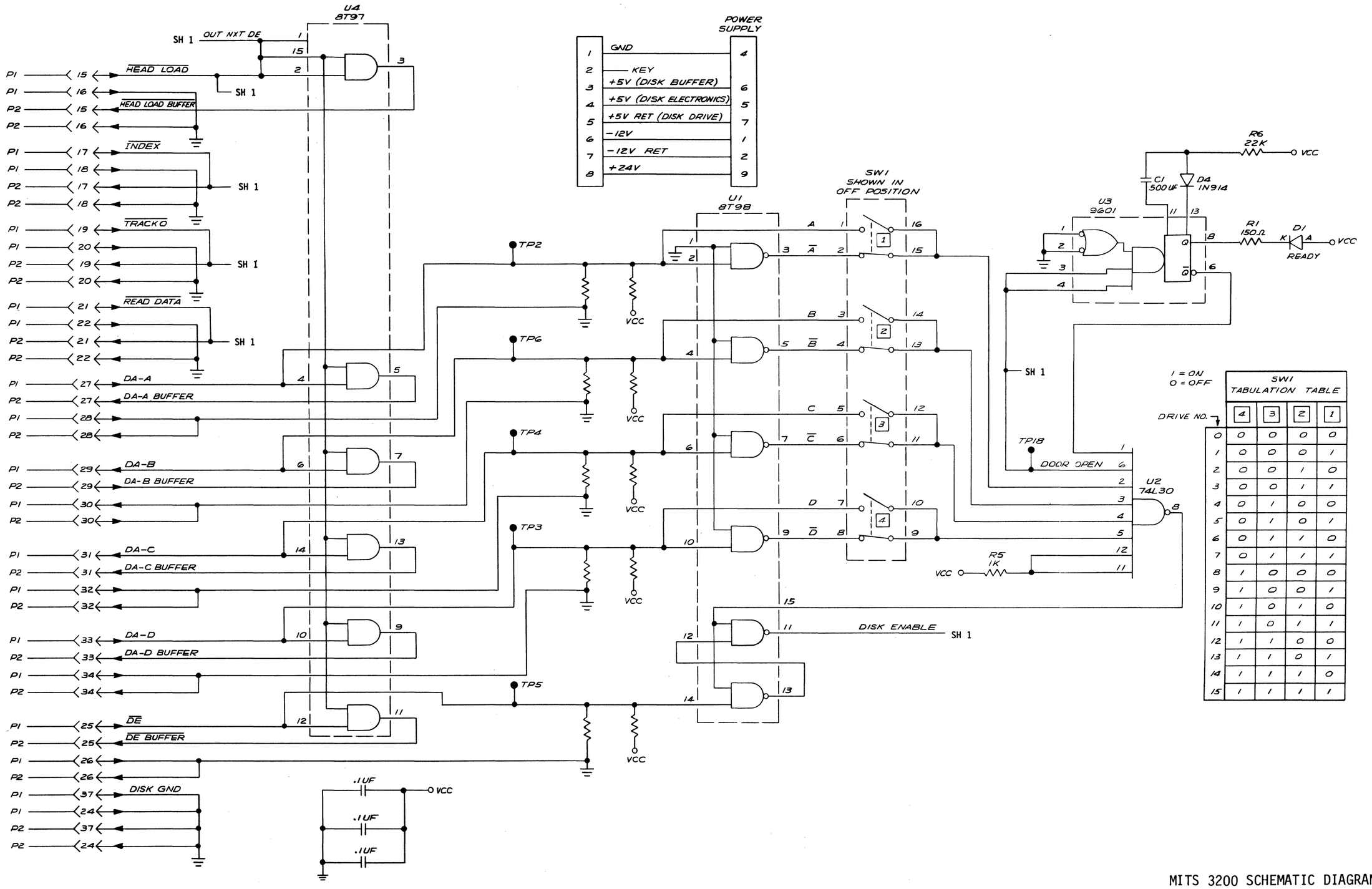


NOTES: UNLESS OTHERWISE SPECIFIED

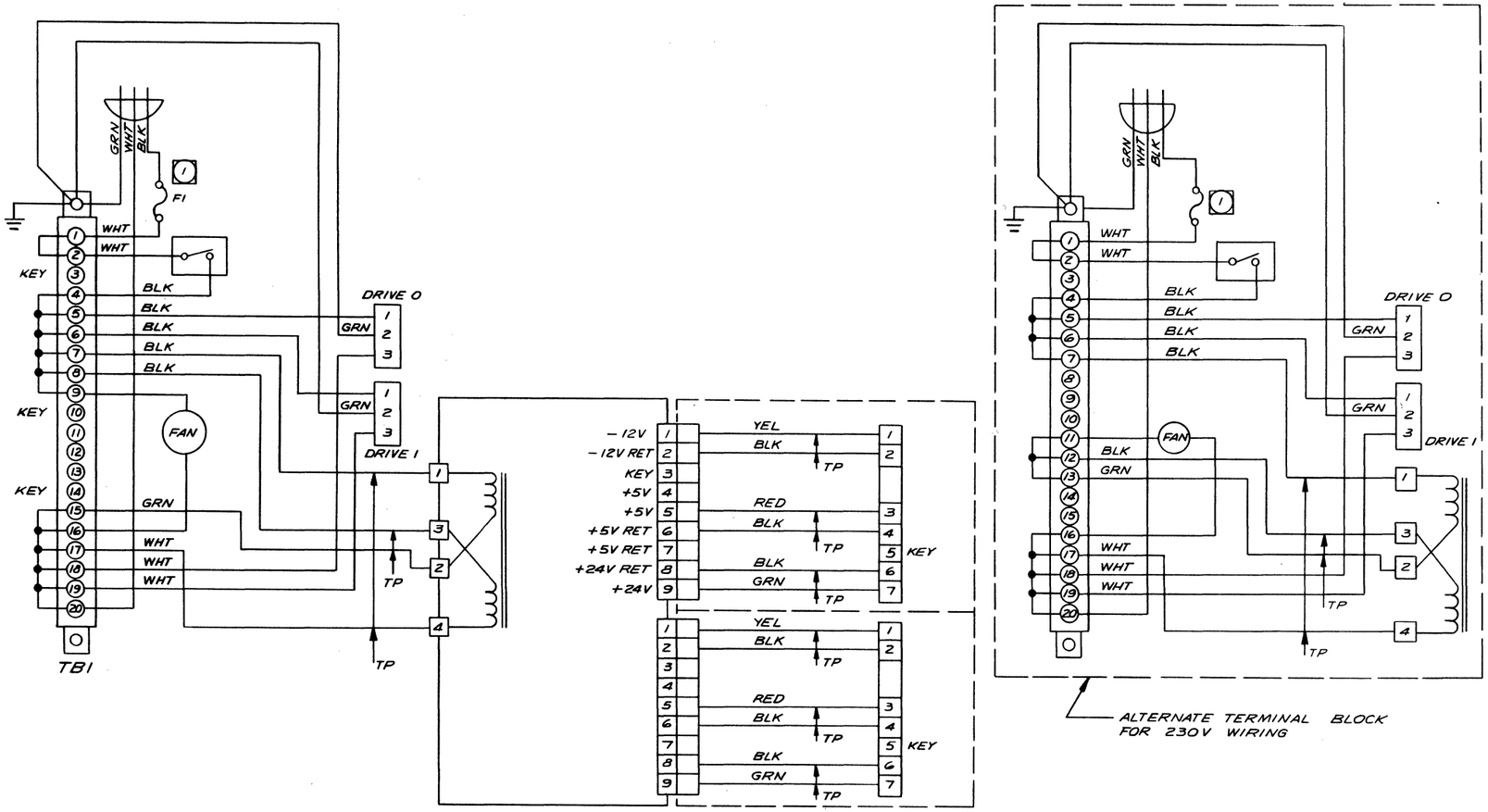
1. RESISTOR PACK (PIN 1 COMMON)

2.

MITS 3200 SCHEMATIC DIAGRAMS
DISK BUFFER BOARD (Sheet 1 of 2)



MITS 3200 SCHEMATIC DIAGRAMS
DISK BUFFER BOARD (Sheet 2 of 2)

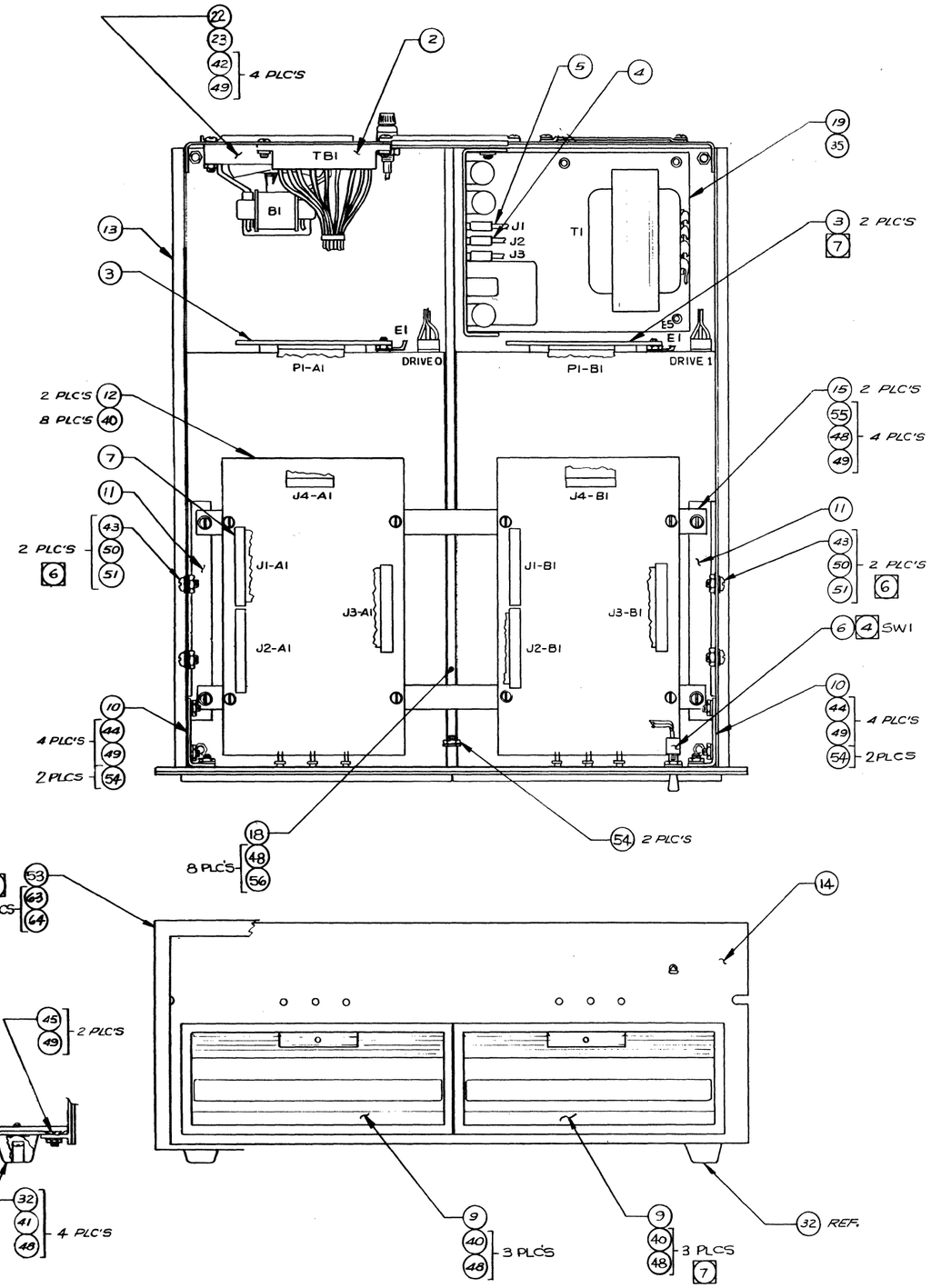


NOTES: UNLESS OTHERWISE SPECIED

(1) FOR 120V AC. USE 3.0 ASB FUSE. FOR 230V AC. USE 1.5 ASB FUSE.

2. TP INDICATES TWISTED PAIR WIRES.

MITS 3200 SCHEMATIC DIAGRAMS
POWER WIRING



HOOK UP CABLES CHART		
CABLE	FROM	TO
250176	TB1-5.18 TB1-6.19 TB1-7 TB1-8 TB1-15 TB1-17	DRIVE 0-1.3 DRIVE 1-1.3 E1 (TRANSF.) E2 (TRANSF.) E3 (TRANSF.) E4 (TRANSF.)
250166	SW1-(WHT) SW1-(BLK)	TB1-2 TB1-4
250165 (FOR -02 & -12 ONLY)	J4-A1 J4-B1	J2 (PWR SUPP.) J1 (PWR SUPP.)
250146	J1-A1	J2-B1
250161 (FOR -02 & -12 ONLY)	P1-A1 (ADAPTOR BD) P1-B1 (ADAPTOR BD)	J3-A1 J3-B1
250174	E5 (PWR SUPP) E1 DRIVE 0 E1 DRIVE 1	J3 (PWR SUPP)
692-7405	W1-GRN W1-WHT W2-BLK	E6 TB1-20 F1-1
518-0005	B1	TB1-9 TB1-16

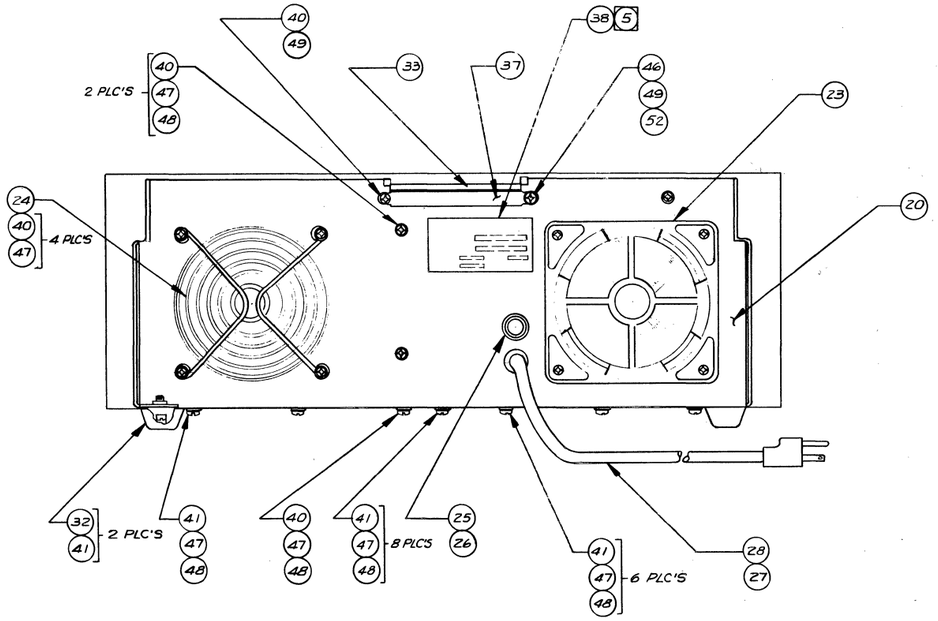
NOTES: UNLESS OTHERWISE SPECIFIED

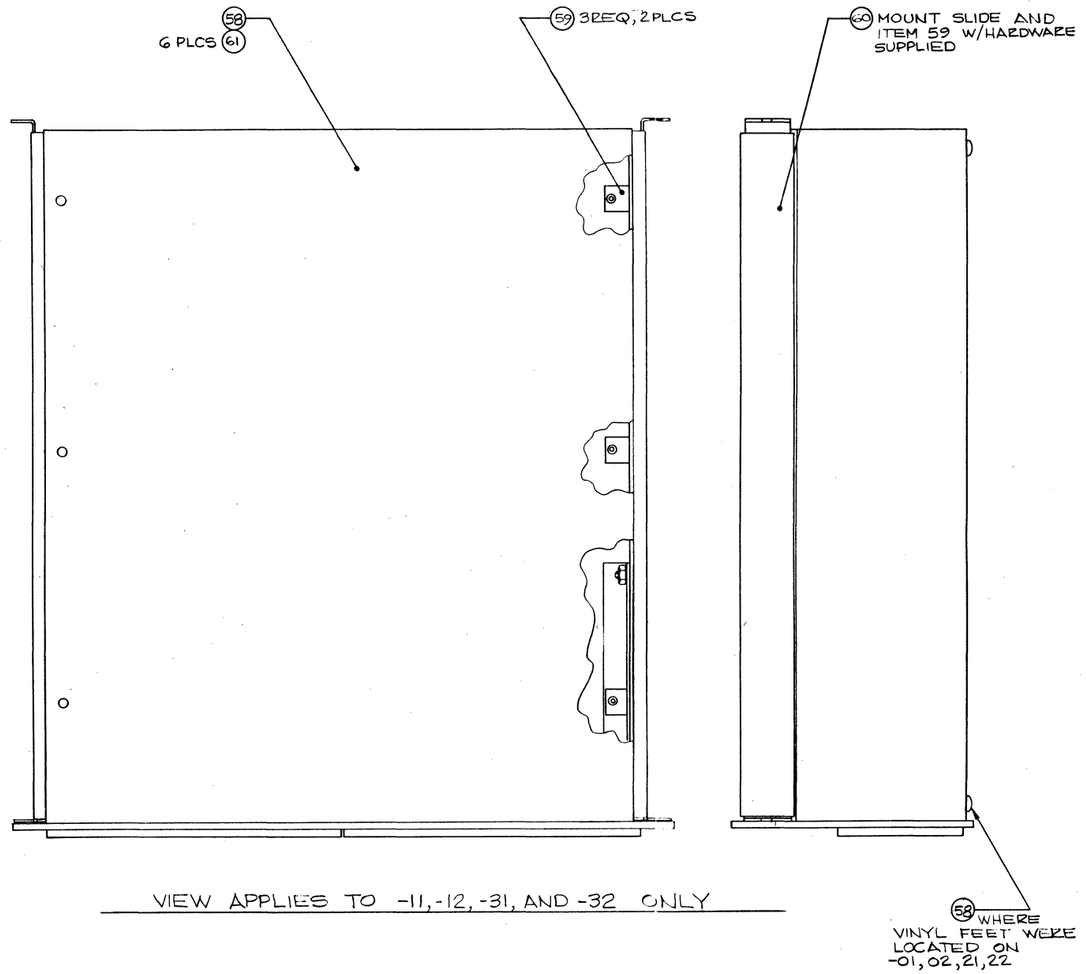
1. FOR PARTS LIST SEE SHEETS 3, 4 AND 5
2. MARK PART NUMBER, SERIAL NUMBER, MODEL NUMBER AND CURRENT REVISION LETTER APPROX. WHERE SHOWN. (SHT 2)
3. FOR CABLE WIRING SEE HOOK UP CHART. FOR ANY ADDITIONAL WIRING SEE SCHEMATIC 250154
4. SCREW AND WASHER PROVIDED WITH SWITCH.
5. DRAWING NO. INCOMPLETE WITHOUT DASH NO. SEE TABULATION TABLE FOR APPROPRIATE DASH NO.
6. PARTS APPLY TO -01,02, 21,22 ONLY
7. PARTS APPLY TO -02,12,22,32 ONLY
8. FOR 230 VAC VERSION (-21,22,31,32) THE FOLLOWING CHANGE MUST BE MADE TO WIRING ON TB1
   A) MOVE WIRE FROM PIN 8 TO PIN 12.
   B) MOVE WIRE FROM PIN 9 TO PIN 11.
   C) MOVE WIRE FROM PIN 15 TO PIN 13.
   REFER TO 200084 FOR WIRING DIAGRAM.

5

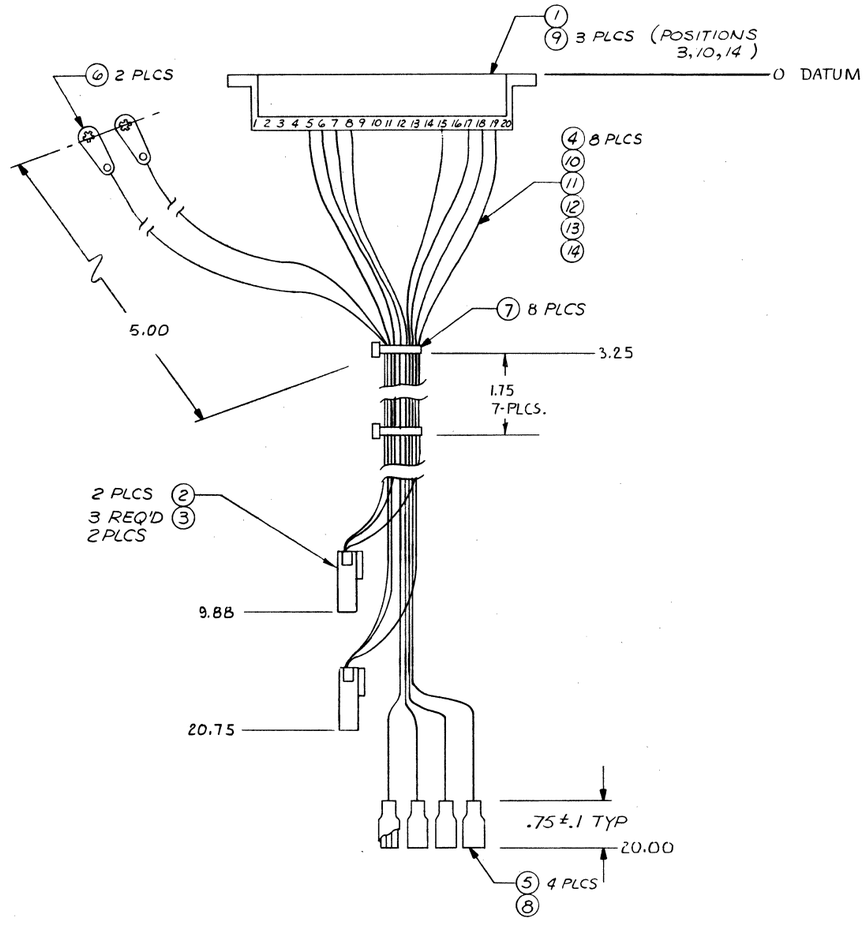
TABULATION TABLE	
DASH NO.	DESCRIPTION
-01	WITH ONE DRIVE, DESK TOP, 115VAC
-02	WITH TWO DRIVES, DESK TOP, 115VAC
-11	WITH ONE DRIVE, RACK MT, 115VAC
-12	WITH TWO DRIVES, RACK MT, 115VAC
-21	WITH ONE DRIVE, DESK TOP, 230VAC
-22	WITH TWO DRIVES, DESK TOP, 230VAC
-31	WITH ONE DRIVE, RACK MT, 230VAC
-32	WITH TWO DRIVES, RACK MT, 230VAC

MITS 3200 ASSEMBLY DRAWINGS
FLOPPY DISK SYSTEM (Sheet 1 of 2)



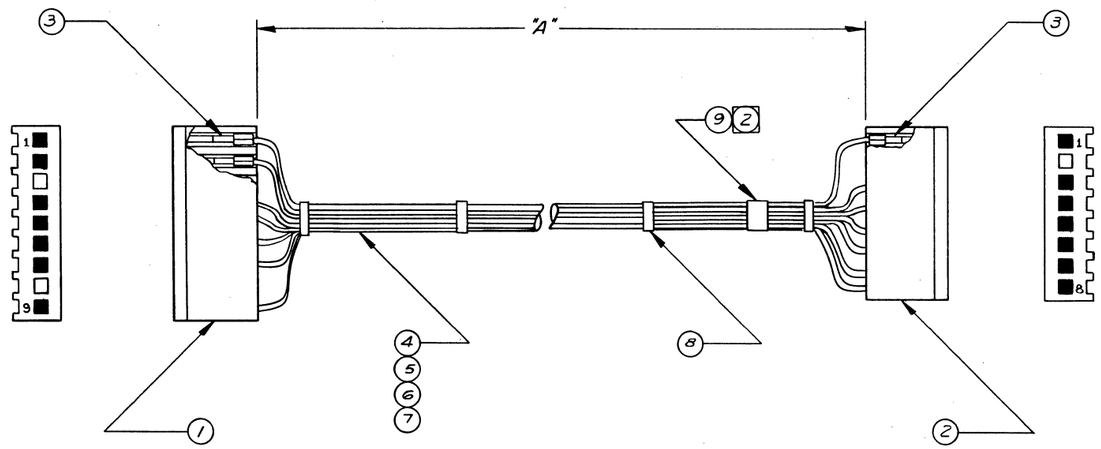


MITS 3200 ASSEMBLY DRAWINGS
FLOPPY DISK SYSTEM (Sheet 2 of 2)



1. SEE DWG NO. 250154 FOR SCHEMATIC.

NOTES: UNLESS OTHERWISE SPECIFIED



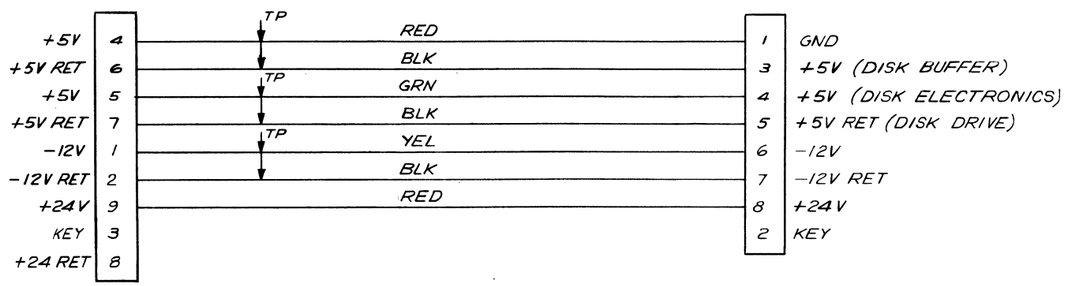
(3)

TABULATION TABLE		
DASH NO.	DIMENSION 'A'	DESCRIPTION
-101	15.00	POWER CABLE FOR BD A1
-102	11.00	POWER CABLE FOR BD B1

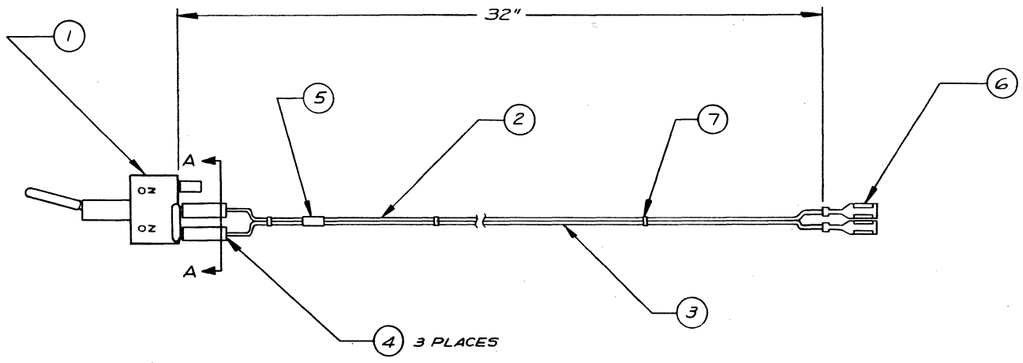
NOTES: UNLESS OTHERWISE SPECIFIED

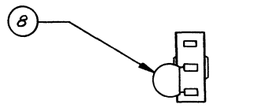
1. FOR PARTS LIST SEE SHEET 2.
2. MARK PART NUMBER AND CURRENT REVISION LETTER APPROX. WHERE SHOWN.
3. PART NUMBER INCOMPLETE WITHOUT DASH NUMBER. SEE TABULATION TABLE FOR APPROPRIATE DASH NUMBER.

WIRING DIAGRAM



MITS 3200 ASSEMBLY DRAWINGS
POWER CABLE



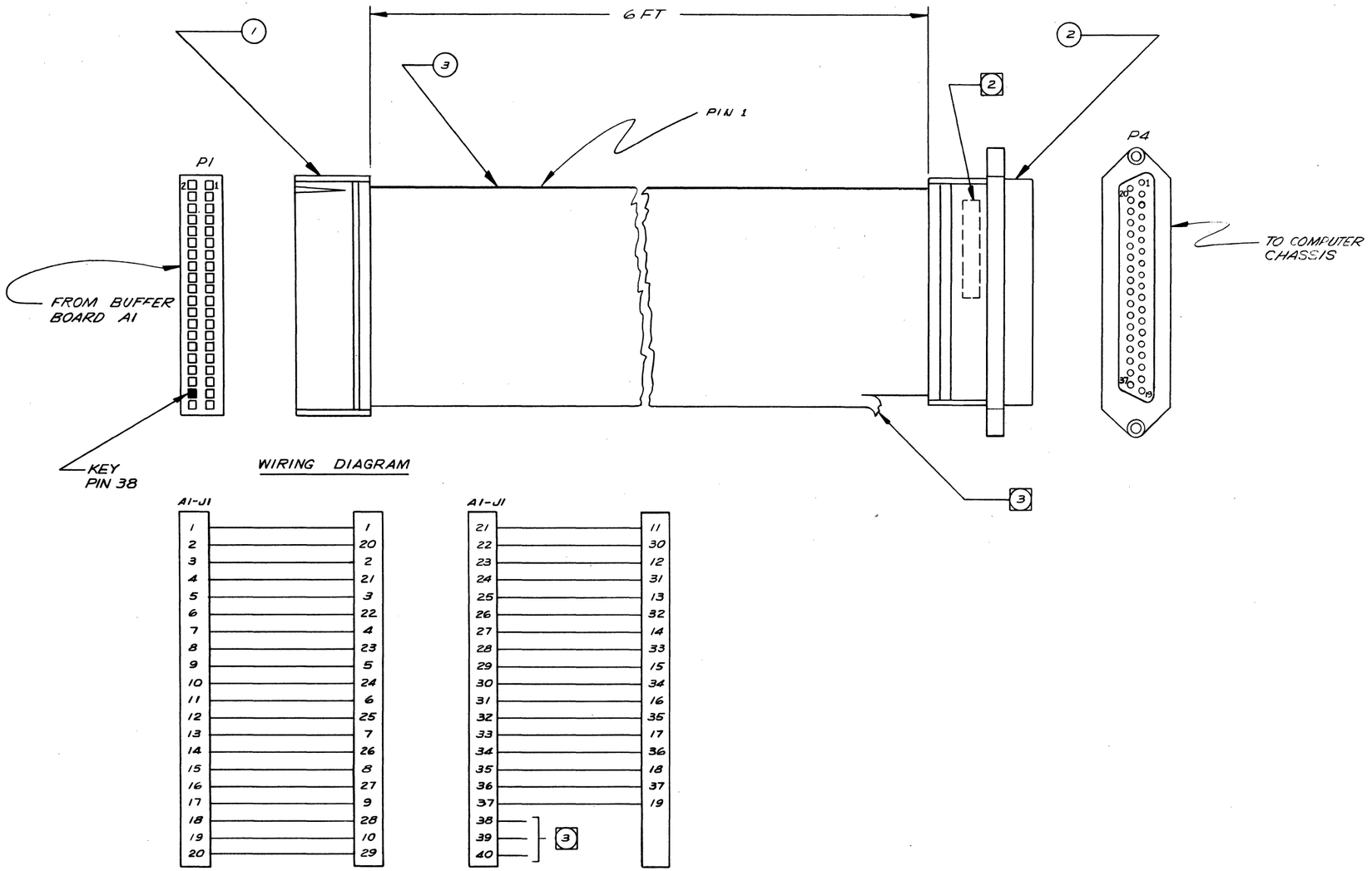


DETAIL A-A

NOTES: UNLESS OTHERWISE SPECIFED

1. FOR PARTS LIST SEE SHEET 2.

(2) MARK PART NUMBER AND CURRENT REVISION LETTER APPROX. WHERE SHOWN



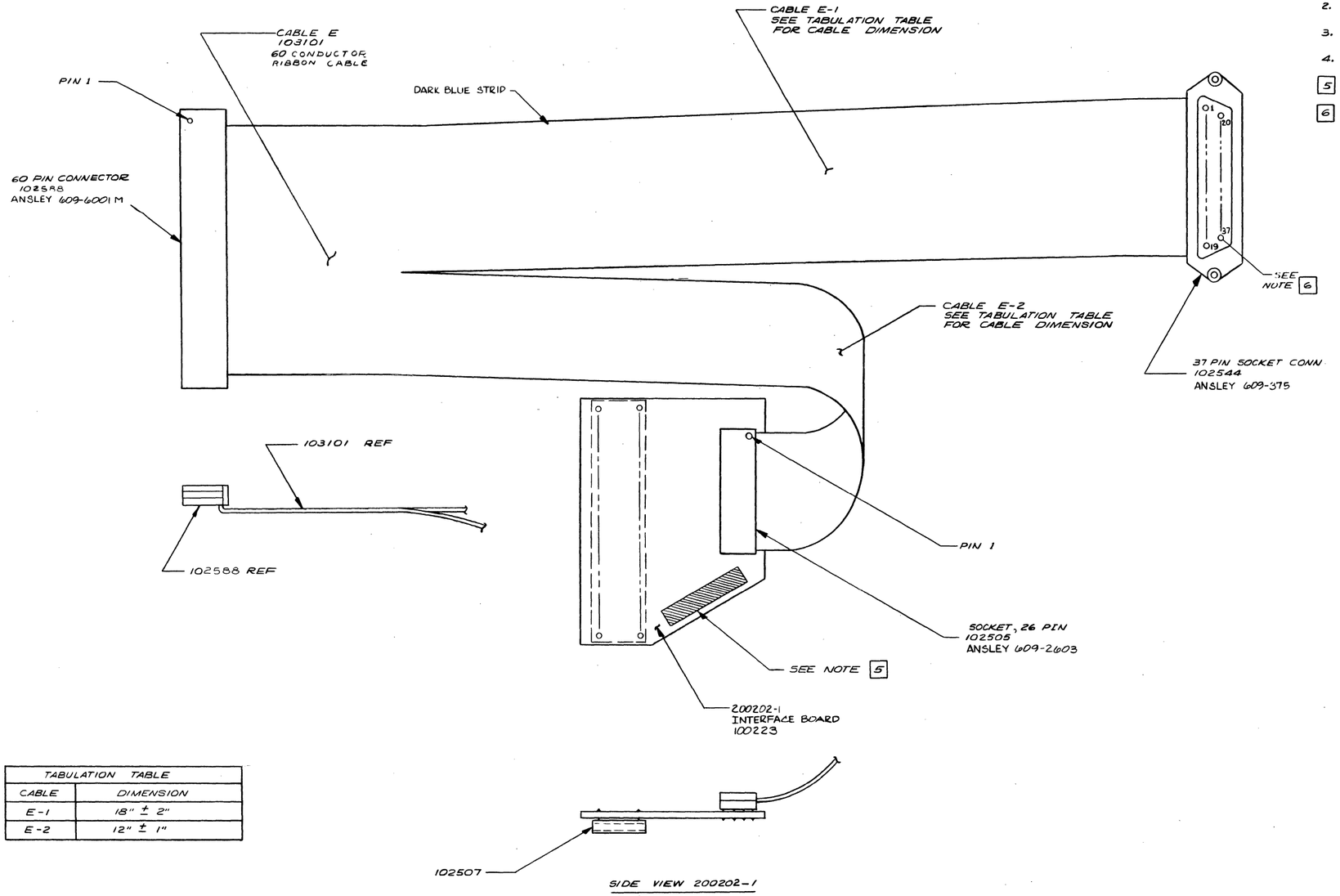
NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR PARTS LIST SEE SHEET 2.
2. MARK PART NUMBER AND CURRENT REVISION LETTER APPROX. WHERE SHOWN.
3. ON J1-A1 CUT SPARE PINS 38, 39 AND 40.

MITS 3200 ASSEMBLY DRAWINGS
I/O CABLE

NOTES: UNLESS OTHERWISE SPECIFIED

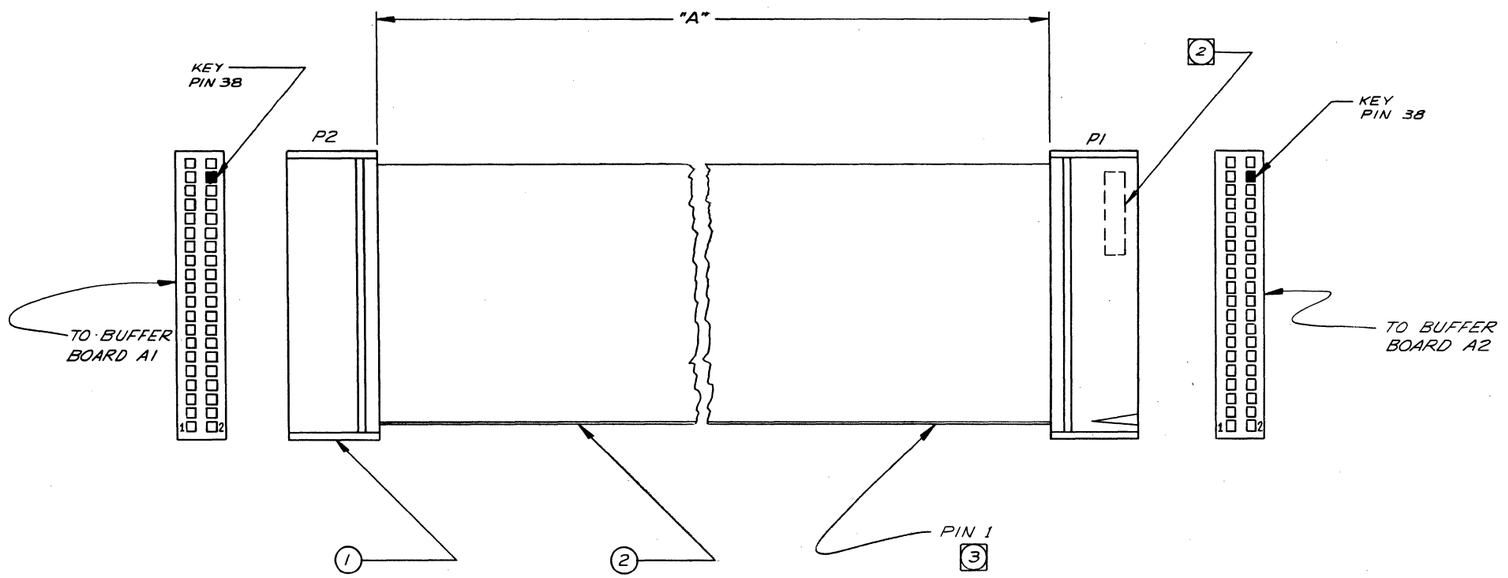
1. ASSEMBLY IDENTIFICATION NUMBER TO BE 200231-1.
2. THIS DRAWING USED IN COJUNTION WITH SCHEMATIC 200194. (NEW)
3. COMPONENT HEIGHT NOT TO EXCEED .30 ABOVE MOUNTING SURFACE OF BOARD.
4. SOLDER PER STANDARD MANUFACTURING PROCESSES.
5. MARK SERIAL NUMBER IN SHADED AREA AS SHOWN
6. CONNECTOR PINS 18, 19 AND 37 ARE NOT USED.



TABULATION TABLE	
CABLE	DIMENSION
E-1	18" ± 2"
E-2	12" ± 1"

SIDE VIEW 200202-1

MITS 3200 ASSEMBLY DRAWINGS
DISK CONTROLLER CABLE

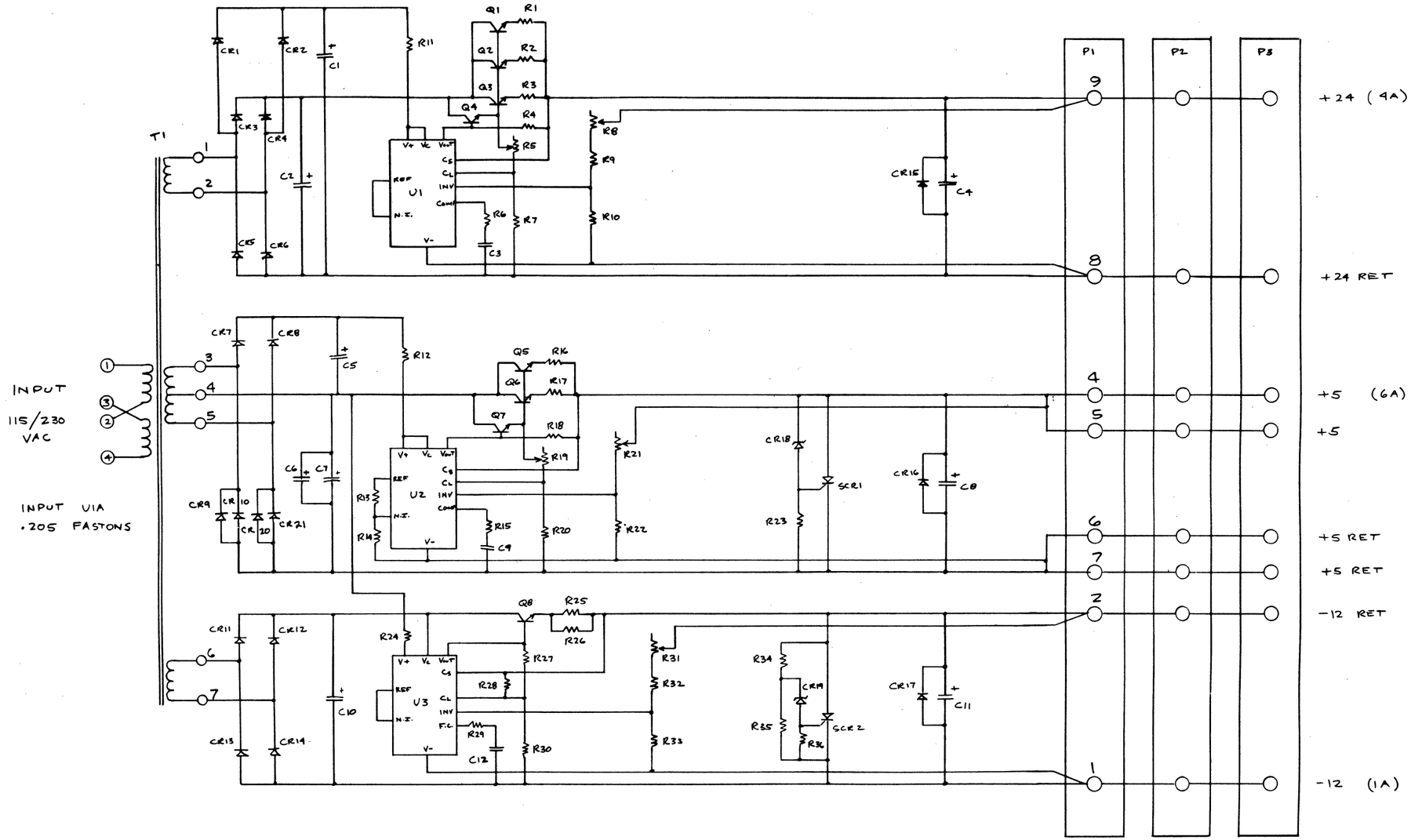


NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR PARTS LIST SEE SHEET 2.
2. MARK PART NUMBER AND CURRENT REVISION LETTER APPROX. WHERE SHOWN.
3. CABLE WIRING SHOULD BE MADE FROM A CONNECTOR NUMBER TO SAME NUMBER OF OPPOSITE CONNECTOR. EXAMPLE: P2-1 TO P1-1 OR P2-5 TO P1-5, ETC.
4. PART NUMBER INCOMPLETE WITHOUT DASH NUMBER. SEE TABULATION TABLE FOR APPROPRIATE DASH NUMBER.

4

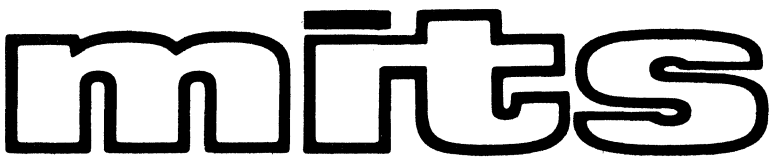
TABULATION TABLE		
DASH NO	DIMENSION "A"	DESCRIPTION
-01	12 IN.	FROM DRIVE 0 TO DRIVE 1
-02	11 FT.	FROM DRIVE 1 TO DRIVE 2



P1, 2 + 3 MOLEX CONNECTORS
P/N 09-67-1092
REMOVE PIN

MATING CONNECTOR: MOLEX
P/N 09-50-7091, PINS = 08-50-0106

MITS 3200 SCHEMATIC DIAGRAMS
POWER SUPPLY



2450 Alamo SE
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