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Project Whirlwind Servomechanisms Laboratory Massachusetts Institute of Technology Cambridge, Massachusetts

- SUBJECT: <u>A COINCIDENT-CURRENT MAGNETIC MEMORY UNIT</u> (Abstract of Report R-192, A Master's Thesis)
- To: 6345 Engineers

From: W. N. Papian

Date: September 11, 1950 (Thesis date: August 31, 1950)

A small, toroidal, ferromagnetic core whose B-H characteristic is properly "rectangular" in shape may be made to operate so that its flux polarity reverses only when the right combination of two or three magnetizing coils are coincidentally excited. The core may then be used as a coincidentcurrent binary memory device which might be assembled, with many others, into a two- or three-dimensional memory system. Selection within such a system would be ac omplished by means of physical-line switching along the two or three space coorainates.

The response times of rectangular-loop cores are found to vary over an extremely large range. To a first approximation, eddy-current shielding accounts for these response times, which range from tenths of a second for some metallic cores to less than a microsecond for some ferritic cores.

Information-retention ratios and signal ratios are defined and are used to assess the ability of a core to operate as a coincident-current memory unit. A test setup which makes it possible to obtain these ratios for different sets of operating conditions is devised and used on a number of cores. Selected results are presented and discussed relative to the pertinent hysteresis-loop shapes.

The problem is bracketed on the one hand by a metallic core (Allegheny Ludlum's MTS 4382) which has excellent signal ratios and a 20microseconds response time, and on the other hand, by a ferritic core (Ferramic 34-AF109 b.o.) which has only fair signal ratios and a 1/2-microsecond response time.

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Further development work should be aimed in two directions: toward improving materials to reduce eddy currents and increase hysteresis-loop rectangularity, and toward uncovering and solving the problems associated with assembling large numbers of these cores into a high-speed memory system.

Signeda W. N. Papian Approved: .

J. W. Forrester

WNP:ap