MASSACHUSETTS INSTITUTE OF TECHNOLOGY

PROJECT MAC

Artificial Intelligence
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WIRElist

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This Memo. describes a design aid used for the automatic production of wirelists for machine or hand wiring of wire-wrap cards.

1. Introduction

The WIRElist program is a design aid intended for use with TTL Integrated Circuits assembled on a Cambion 56 socket wire wrap board.

There are two types of data the program accepts;

1) which IC is in which socket
2) which pins are connected together on one run.

From this information the program provides the following features;

1) checking of data
2) optimization of wire order
3) listing of wire runs giving length,loading,etc.
4) listing of sockets showing IC, which sections used.
5) listing of connector pins and signal.
6) production of paper tapes for semi-automatic wire-wrap machines.

It is planned to also provide plotter drawings of the block schematics.

2. Basic Commands

2.1 The PUT command

```
PUT ICname,slot#
```

This command specifies the name of the IC to be placed in this slot (E.G. PUT MC3000,4). The description of most IC's is contained within the program. Logically separate gates, FF's, etc. within the same package are called sections. Furthermore, in the case of AND-OR gates, each AND within the same section is called a sub-section. Each pin within a SEC (or SSEC) has a unique symbolic name (E.G. IN1).

2.2 The WIRE command

```
WIRE pin1,pin2,...
```

This command logically connects together pin1 and pin2 such that they will be on the same wire run. Any number of pins may be specified, separated by commas. The format of the pin specification has three variations;

(slot# pin#) - E.G. (1 12)

This identifies the specific pin by giving the slot and IC pin (not the socket pin number) nume2ically. For 14 pin DIP's the IC pin number will correspond to a socket pin no. one higher. Slot 0 refers specially to the connector pins.

slot# A:IN2

This specifies the slot, the SEC (A) and the pin name (IN2). Sub-sections are specified by giving AC: for SSEC-C of SEC-A. Slot number is again a numeric expresion.

*run name

The program has a dictionary of run names or signal names with an entry for the high (+) and low (-) state of each signal. This allows reference to a particular run without naming a specific pin. The run name consists of a signal name of any number of characters. (excluding comma,carriage return, "(", "+", and "-".) The form "(0)" or "(1)" is used to specify whether this run name is associated with the zero or one state of a flip-flop. The plus and minus are used to indicate that the assertion of this signal is either high or gnd. For instance, the run name *FOO(1)- would show that this wire was low when FF FOO is in the "one" state. Sample run names and the reduced equivalents are given below:

*foo	*foo+
*foo(0)	*foo-
*foo(0)-	*foo+
*-foo-	*foo+
*load a0	
*fry {18,25}	

In the PUT command, if run names are given after the slot number, they will be defined as the output of the corresponding section. For example;

```
     PUT MC3000,2,LOAD A,LOAD B
     will be equivalent to
     PUT MC3000,2
```

```
WIRE *LOAD A,2 A:OUT
WIRE *LOAD B,2 B:OUT
```

The program predefines two signal names, *GND and *HIGH. Pins WIREd to *GND will not be connected together, but will be wired to the gnd pin at the socket, (along with the gnd and Vcc pins of the IC which are known to the program).

3. Other Commands 3.1 .WIREL

This commani produces the file "** WRLIST" which consists of information for each run similar to this example:

```
GATE MAM+    (49-11)10 MC3000-IN      1.0
             (49-14)13 MC3000-IN      1.0  0.3 IN.
             (49-3)2   MC3000-IN      1.0  0.4 IN.
             (49-6)5   MC3000-IN      1.0  0.3 IN.
             (50-11)10 MC3000-IN      1.0  0.3 IN.
             (50-14)13 MC3000-IN      1.0  0.3 IN.
             (50-6)5   MC3000-IN      1.0  0.3 IN.
             (50-3)2   MC3000-IN      1.0  0.3 IN.
                                     -8.0  2.2 IN. NO OUTPUT
```

The run name appears at the beginning of the first line.

Each line shows the next pin on the optimal order run.

In parenthesis is the slot#-socket pin#. For 14 pin DIP's the IC pin is shown following the close paren.

The module type and the pin type.

The loading for this pin in units of TTL-III loads.

The wire length from the last pin to this.

The last line shows the cumulative loading for this run, negative if the output driving capability is exceeded. A flag "NO OUTPUT" is shown if no gate drives this line.

3.2 .UML

This command produces the file "** UML" with the following format:

```
     41    MC2004
              SEC A
      11  OUT     AO OUT+
      12  XC      (17 11)
      13  XE      (17 12)
            SUBSEC A
      1   IN2     MAB 18+
      14  IN1     AO 18-
            SUBSEC B
      2   IN1     AO 18+
      3   IN2     MAB 18-
            SUBSEC C
      5   IN1     AO 19-
      6   IN2     MAB 19+
            SUBSEC D
      7   IN1     AO 19+
      8   IN2     MAB 19-
      9   IN3     HIGH+
```

The first line gives the socket number and the IC type.

Under headings for each SEC and SSEC a line for each pin gives the pin number, the pin name, and the connected signal or pin.

Produced at the same time is a list of connector pins and connected run names.

3.3 .UNUSD

This command examines all of the IC's looking for unused pins. There are four cases;

1) the SEC is not used
2) the SEC is an AND - connect unused pins to *HIGH
3) The SEC is an OR - connect unused pins to *GND
4) AND-OR gate - if the SSEC is used, connect remaining pins to *HIGH, otherwise connect one of the pins to *GND.

4. Using the program

```
Load program          WIRE$~H
read file             .READ KLUDGE DATA
connect unused pins   .UMUSD
create uml            .UML
                      .WIREL
                      ~Z
                      167)_    .IOT 1,1 $~X.
                      TECO~H
                      ER DSK: KLUDGE WRLIST$Y
```

If the program encounters an error it will print out a message followed by the line of input that probably caused the error. It will stop reading the file and will wait for further commands from the teletype.

4.1 Macro roccessor

The wirelist program has a macro proccessor that for most purposes is identical to the macro processor of MIDAS (described in AI memo 90 pp 16-26). Some ingenuity in the use of this "feature" will usually allow some amount of conciseness and symbolic representation at the cost of minor exasperation.

5. Appendix - List of IC definitions

Following is a list of the defined IC types. Under each SEC and SSEC there is:

pin# symbolic pin name pin type loading

```
ITS 454 CONSOLE 6 FREE. 00:51:13
MODULE UTILIZATION CHART FOO 1 THIS VERSION WIRE 30B
22:59:49 JAN 04,1929
1     SN7475               2     MC2002              3     MC2004
          SEC A                       SEC A                     SEC A
 1    Q0       Q0 10.0      11   XC      XPANDR 1.3   11   OUT     OUT 10.0
 2    IN       IN 2.0       12   XE      XPANDR 1.3   12   XC      XPANDR 10.0
 13   CLK      IN 4.0             SUBSEC A            13   XE      XPANDR 10.0
 16   Q1       Q1 10.0      1    IN3     IN 1.3             SUBSEC A
          SEC B             13   IN1     IN 1.3       1    IN2     IN 1.3
 3    IN       IN 2.0       14   IN2     IN 1.3       14   IN1     IN 1.3
 14   Q0       Q0 10.0            SUBSEC B                  SUBSEC B
 15   Q1       Q1 10.0      2    IN1     IN 1.3       2    IN1     IN 1.3
          SEC C             3    IN2     IN 1.3       3    IN2     IN 1.3
 4    CLK      IN 4.0             SUBSEC C                  SUBSEC C
 6    IN       IN 2.0       5    IN1     IN 1.3       5    IN1     IN 1.3
 10   Q1       Q1 10.0      6    IN2     IN 1.3       6    IN2     IN 1.3
 11@  Q0       Q0 10.0            SUBSEC D                  SUBSEC D
          SEC D             7    IN1     IN 1.3       7    IN1     IN 1.3
 7    IN       IN 2.0       8    IN2     IN 1.3       8    IN2     IN 1.3
 8    Q0       Q0 10.0      9    IN3     IN 1.3       9    IN3     IN 1.3
 9    Q1       Q1 10.0


4     MC3000               5     MC3002              6     MC3005
          SEC A                       SEC A                     SEC A
 1    IN1      IN 1.0       1    IN1     IN 1.0       1    IN1     IN 1.0
 2    IN2      IN 1.0       2    IN2     IN 1.0       2    IN2     IN 1.0
 3    OUT      OUT 10.0     3    OUT     OUT 10.0     12   OUT     OUT 10.0
          SEC B                       SEC B           13   IN3     IN 1.0
 4    IN1      IN 1.0       4    IN1     IN 1.0                 SEC B
 5    IN2      IN 1.0       5    IN2     IN 1.0       3    IN1     IN 1.0
 6    OUT      OUT 10.0     6    OUT     OUT 10.0     4    IN2     IN 1.0
          SEC C                       SEC C           5    IN3     IN 1.0
 8    OUT      OUT 10.0     8    OUT     OUT 10.0     6    OUT     OUT 10.0
 9    IN1      IN 1.0       9    IN1     IN 1.0                 SEC C
 10   IN2      IN 1.0       10   IN2     IN 1.0       8    OUT     OUT 10.0
          SEC D                       SEC D           9    IN1     IN 1.0
 11   OUT      OUT 10.0     11   OUT     OUT 10.0     10   IN2     IN 1.0
 12   IN1      IN 1.0       12   IN1     IN 1.0       11   IN3     IN 1.0
 13   IN2      IN 1.0       13   IN2     IN 1.0


7     MC3010               8     MC3015              9     MC3020
          SEC A                       SEC A                     SEC A
 1    IN1      IN 1.0       1    IN1     IN 1.0             SUBSEC A
 2    IN2      IN 1.0       2    IN2     IN 1.0       9    IN1     IN 1.0
 3    U        U 1.0        3    IN3     IN 1.0       10   IN2     IN 1.0
 4    IN3      IN 1.0       4    IN4     IN 1.0       11   XE      XPANDR 1.0
 5    IN4      IN 1.0       5    0       U 1.0        12   XC      XPANDR 1.0
 6    OUT      OUT 10.0     6    0       U 1.0              SUBSEC B
          SEC B             8    OUT     OUT 10.0     1    IN2     IN 1.0
 8    OUT      OUT 10.0     9    0       U 10.0       8    OUT     OUT 10.0
 9    IN1      IN 1.0       10   IN5     IN 1.0       13   IN1     IN 1.0
 10   IN2      IN 1.0       11   IN6     IN 1.0                 SEC B
 11   0        U 1.0        12   IN7     IN 1.0             SUBSEC A
 12   IN3      IN 1.0       13   IN8     IN 1.0       2    IN1     IN 1.0
 13   IN4      IN 1.0                                 3    IN2     IN 1.0
                                                            SUBSEC B
                                                      4    IN1     IN 1.0
                                                      5    IN2     IN 1.0
                                                      6    OUT     OUT 10.0
```

```
10     MC3026
           SEC  A
 1     IN1       IN 1.1
 2     IN2       IN 1.1
 3     0         U 1.1
 4     IN3       IN 1.1
 5     IN4       IN 1.1
 6     OUT       OUT 20.0
           SEC  B
 8     OUT       OUT 20.0
 9     IN1       IN 1.1
 10    IN2       IN 1.1
 11    0         U 1.1
 12    IN3       IN 1.1
 13    IN4       IN 1.1
```

```
11     MC3030
           SEC  A
 1     IN2       IN 1.0
 2     IN3       IN 1.0
 3     IN4       IN 1.0
 11    XE        XPANDR 1.0
 12    XC        XPANDR 1.0
 13    IN1       IN 1.0
           SEC  B
 4     IN1       IN 1.0
 5     IN2       IN 1.0
 6     IN3       IN 1.0
 8     IN4       IN 1.0
 9     XC        XPANDR 1.0
 10    XE        XPANDR 1.0
```

```
12     MC3060
           SEC  A
 1     CLR       IN 1.5
 2     D         IN 0.6
 3     CLK       IN 1.4
 4     SET       IN 1.0
 5     Q1        Q1 10.0
 6     Q0        Q0 10.0
          @SEC  B
 8     Q0        Q0 10.0
 9     Q1        Q1 10.0
 10    SET       IN 1.0
 11    CLK       IN 1.4
 12    D         IN 0.6
 13    CLR       IN 1.5
```

```
13     MC3061
           SEC  A
 1     CLK       IN 3.2
 2     K         IN 0.6
 3     J         IN 0.6
 4     SET       IN 1.6
 5     Q1        Q1 10.0
 6     Q0        Q0 10.0
           SEC  B
 8     Q0        Q0 10.0
 9     Q1        Q1 10.0
 10    SET       IN 1.6
 11    J         IN 0.6
 12    K         IN 0.6
 13    CLK       IN 3.2
```

```
14     MC3001
           SEC  A
 1     IN1       IN 1.0
 2     IN2       IN 1.0
 3     OUT       OUT 10.0
           SEC  B
 4     IN1       IN Q.0
 5     IN2       IN 1.0
 6     OUT       OUT 10.0
           SEC  C
 8     OUT       OUT 10.0
 9     IN1       IN 1.0
 10    IN2       IN 1.0
           SEC  D
 11    OUT       OUT 10.0
 12    IN1       IN 1.0
 13    IN2       IN 1.0
```

```
15     MC3003
           SEC  A
 1     IN1       IN 1.0
 2     IN2       IN 1.0
 3     OUT       OUT 10.0
           SEC  B
 4     IN1       IN 1.0
 5     IN2       IN 1.0
 6     OUT       OUT 10.0
           SEC  C
 8     OUT       OUT 10.0
 9     IN1       IN 1.0
 10    IN2       IN 1.0
           SEC  D
 11    OUT       OUT 10.0
 12    IN1       IN 1.0
 13    IN2       IN 1.0
```

```
16     MC3026
           SEC  A
 1     IN1       IN 1.1
 2     IN2       IN 1.1
 3     0         U 1.1
 4     IN3       IN 1.1
 5     IN4       IN 1.1
 6     OUT       OUT 20.0
           SEC  B
 8     OUT       OUT 20.0
 9     IN1       IN 1.1
 10    IN2       IN 1.1
 11    0         U 1.1
 12    IN3       IN 1.1
 13    IN4       IN 1.1
```

```
@
```